PRELIMINARY

Integrated Circuit Systems, Inc.

ICS844252-04

FEMTOCLOCKS™ CRYSTAL-TO-LVDS CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS844252-04 is a 10Gb/12Gb Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS844252-04 can synthesize 10 Gigabit Ethernet and 12 Gigabit Ethernet with a 25MHz crystal. It can also generate SATA and 10Gb Fibre Channel reference clock frequencies with the appropriate choice of crystals. The ICS844252-04 has excellent phase jitter performance and is packaged in a small 16-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- Two differential LVDS outputs
- Crystal oscillator interface designed for 18pF parallel resonant crystals
- Crystal input frequency range: 19.33MHz - 30MHz
- Output frequency range: 145MHz - 187.5MHz
- VCO frequency range: 580MHz - 750MHz
- RMS phase jitter at 156.25MHz (1.875MHz - 20MHz): 0.36ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free compliant packages

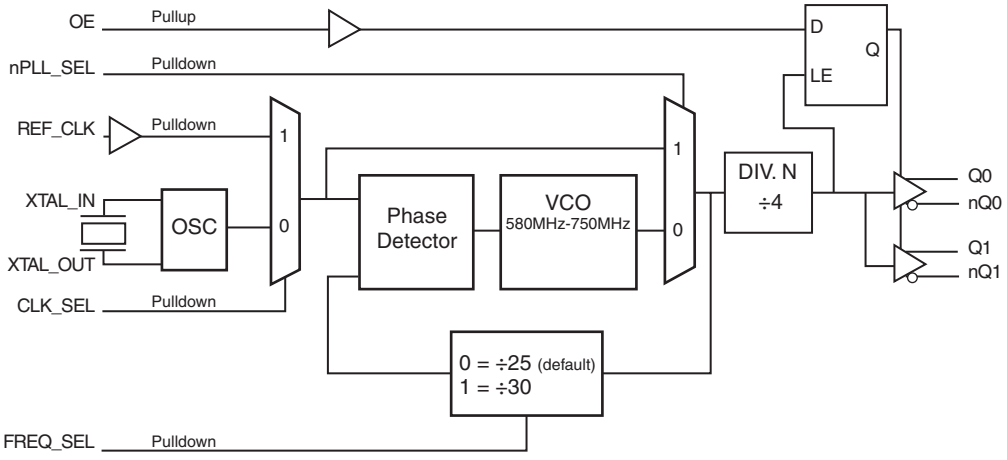
CONFIGURATION TABLE WITH 25MHZ CRYSTAL

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
25	30	750	4	187.5	12 Gigabit Ethernet
25	25	625	4	156.25	10 Gigabit Ethernet

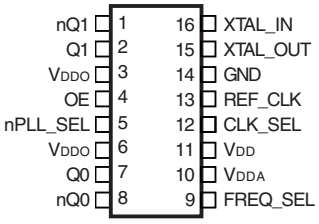
CONFIGURATION TABLE WITH SELECTABLE CRYSTALS

Inputs				Output Frequency (MHz)	Application
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide		
20	30	600	4	150	SATA
21.25	30	637.5	4	159.375	10 Gigabit Fibre Channel
24	25	600	4	150	SATA
25.5	25	637.5	4	159.375	10 Gigabit Fibre Channel
30	25	750	4	187.5	12 Gigabit Ethernet

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS844252-04
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential clock outputs. LVDS interface levels.
3, 6	V_{DDO}	Power		Output supply pins.
4	OE	Input	Pullup	Output enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL interface levels.
5	nPLL_SEL	Input	Pulldown	Selects between the PLL and reference clock as input to the divider. When Low, selects PLL. When High, selects reference clock. LVCMOS/LVTTL interface levels.
7, 8	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
9	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When Low, selects crystal inputs. When High, selects REF_CLK. LVCMOS/LVTTL interface levels.
13	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS/LVTTL interface levels.
14	GND	Power		Power supply ground.
15, 16	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characterristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			70		mA
I_{DDA}	Analog Supply Current			11		mA
I_{DDO}	Output Supply Current			40		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, CLK_SEL, FREQ_SEL, nPLL_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
		OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	REF_CLK, CLK_SEL, FREQ_SEL, nPLL_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

TABLE 3C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 4. CRYSTAL CHARACTERISTICS

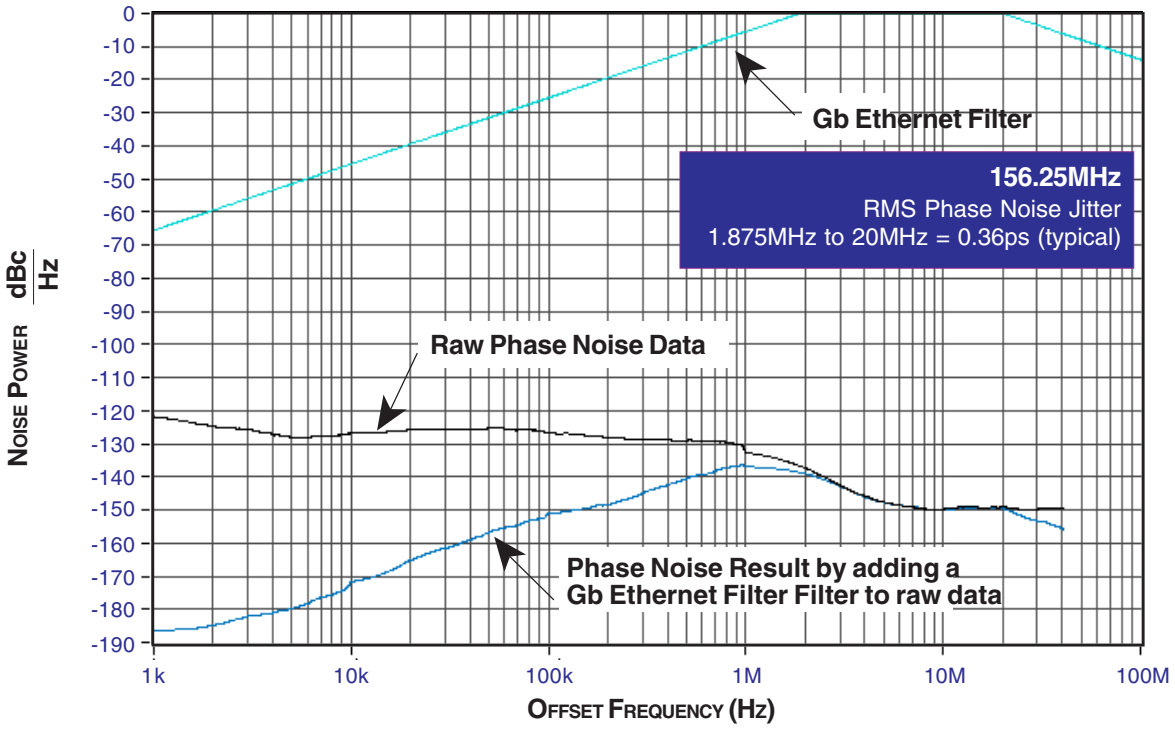
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.33		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

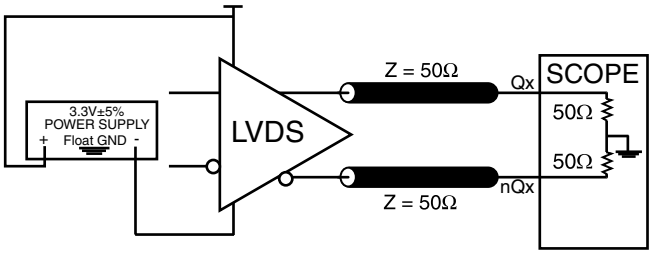
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		145		187.5	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz @ Integration Range: 1.875MHz - 20MHz		0.36		ps
		159.375MHz @ Integration Range: 1.875MHz - 20MHz		0.38		ps
		187.5MHz @ Integration Range: 1.875MHz - 20MHz		0.38		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		375		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plots following this section.

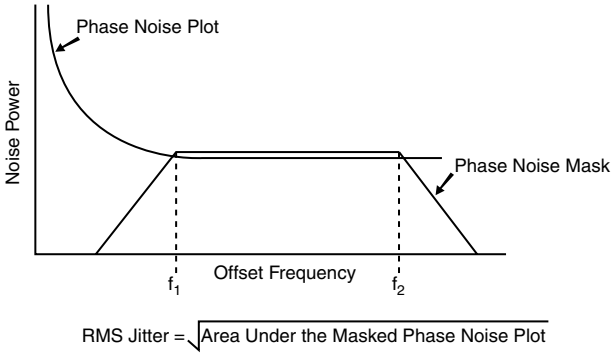
TYPICAL PHASE NOISE AT 156.25MHZ



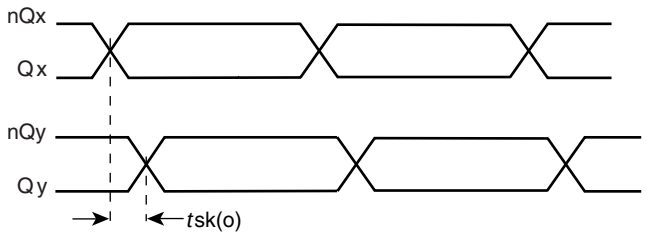
PARAMETER MEASUREMENT INFORMATION



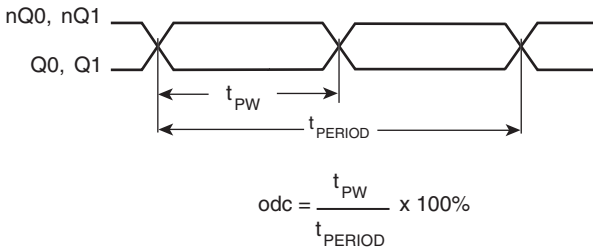
3.3V OUTPUT LOAD AC TEST CIRCUIT



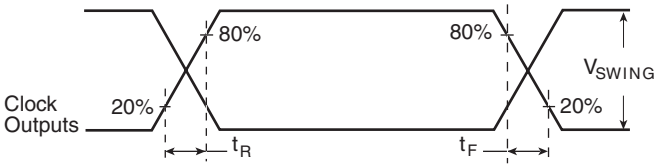
RMS PHASE JITTER



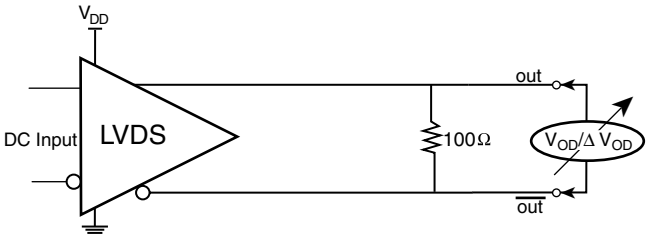
OUTPUT SKEW



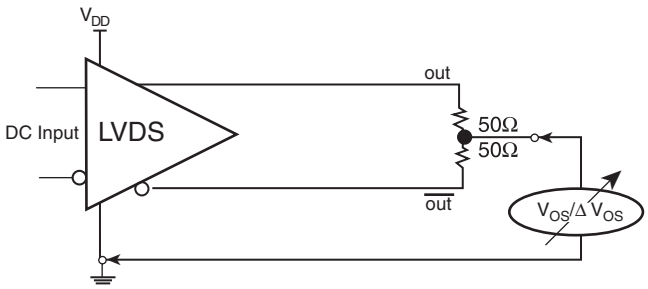
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844252-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, $V_{DDA,}$ and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

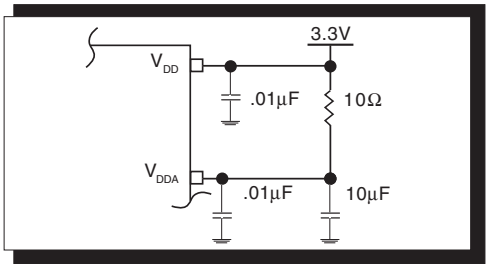


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844252-04 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

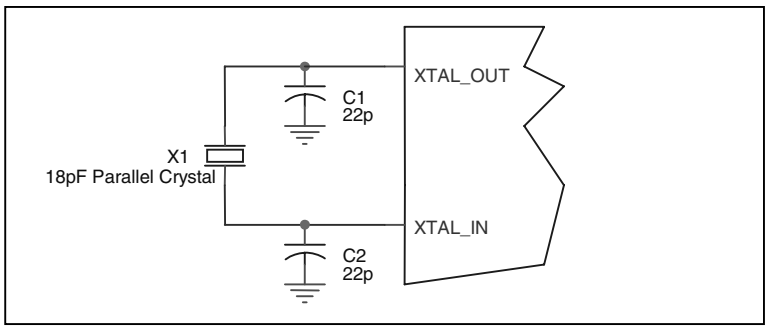


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

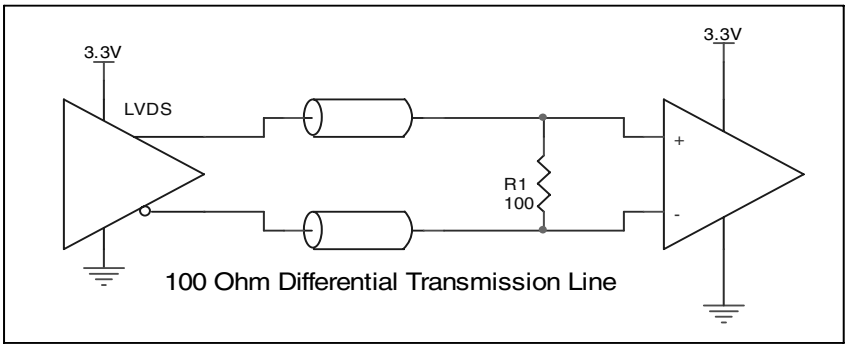


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844252-04. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS844252-04 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 70mA = **242.6mW**
- Power (output)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 40mA = **138.6mW**

  Total Power$_{_MAX}$ = 242.6mW + 138.6mW = **381.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 81.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.381W * 81.8°C/W = 101°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-LEADTSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS844252-04 is: 2234

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

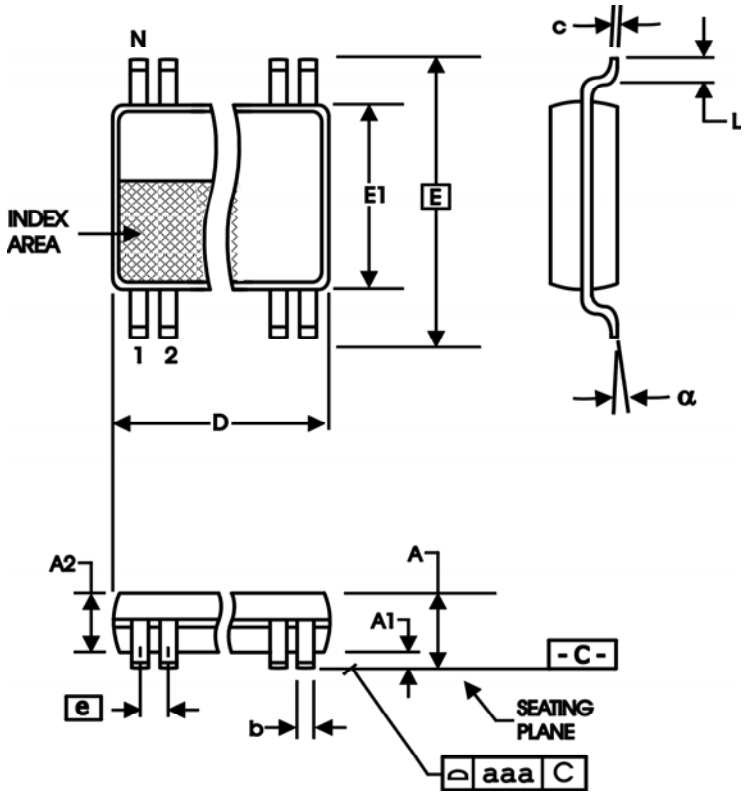


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844252AG-04	44251A04	16 Lead TSSOP	tube	0°C to 70°C
ICS844252AG-04T	44251A04	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS844252AG-04LF	TBD	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS844252AG-04LFT	TBD	16 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.