



Integrated Device Technology, Inc.

# HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) SRAM

IDT10494  
IDT100494  
IDT101494

## FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 7/8/10/15
- Low power dissipation: 700mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

## DESCRIPTION:

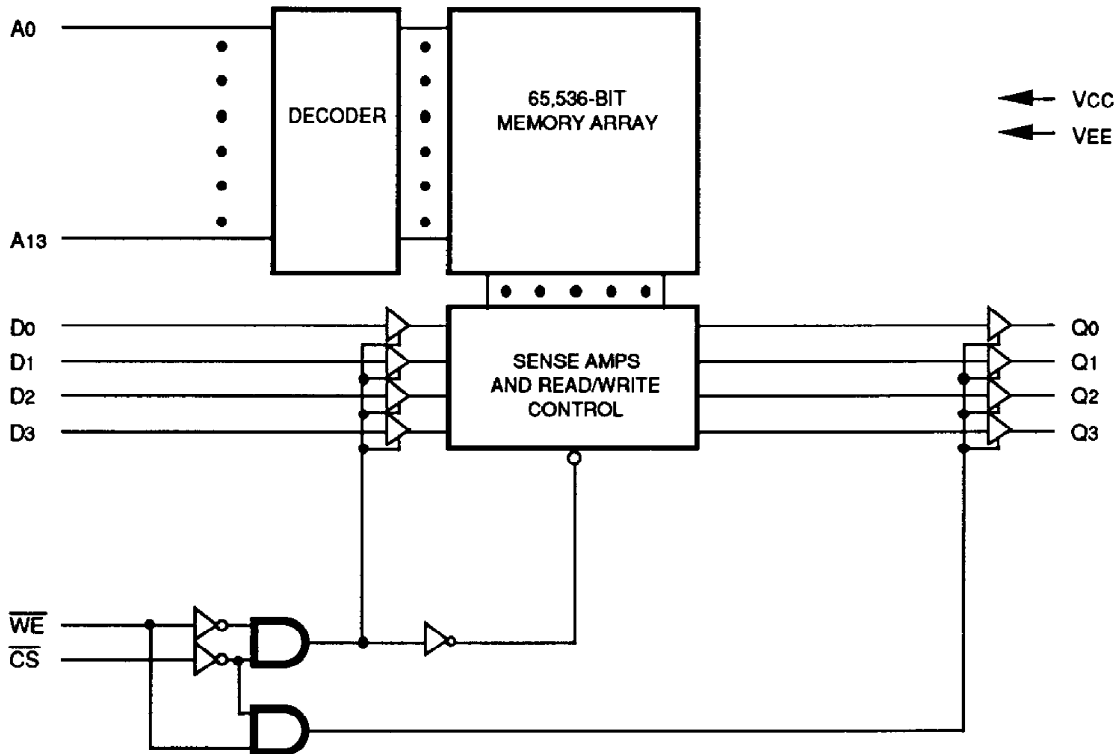
The IDT10494, IDT100494 and 101494 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: DataOUT is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

## FUNCTIONAL BLOCK DIAGRAM



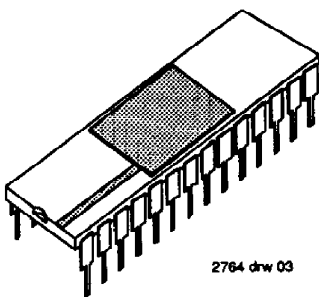
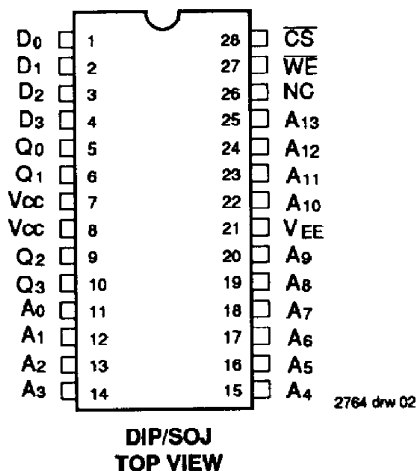
2764 drw 01

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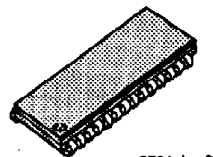
COMMERCIAL TEMPERATURE RANGE

AUGUST 1990

**PIN CONFIGURATION**



**400-Mil-Wide  
CERAMIC PACKAGE  
C28**



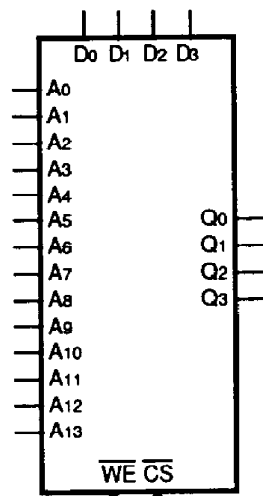
**300-Mil-Wide  
PLASTIC SOJ PACKAGE  
Y28**

**PIN DESCRIPTIONS**

Symbol	Pin Name
A <sub>0</sub> through A <sub>13</sub>	Address Inputs
D <sub>0</sub> through D <sub>3</sub>	Data Inputs
Q <sub>0</sub> through Q <sub>3</sub>	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage

2764 tbl 01

**LOGIC SYMBOL**



**16K x 4  
SRAM**

2764 drw 05

**AC OPERATING RANGES<sup>(1)</sup>**

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

NOTE:

1. Referenced to Vcc

2764 tbl 02

**CAPACITANCE (T<sub>A</sub>=+25°C, f=1.0MHz)**

Symbol	Parameter	DIP		SOJ		Unit
		Typ.	Max.	Typ.	Max.	
C <sub>IN</sub>	Input Capacitance	4	-	3	-	pF
C <sub>OUT</sub>	Output Capacitance	6	-	3	-	pF

2764 tbl 03

**TRUTH TABLE<sup>(1)</sup>**

$\overline{CS}$	$\overline{WE}$	Dataout	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H=High, L=Low, X=Don't Care

2764 tbl 04

**ECL-10K ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage With Respect to GND	+0.5 to -7.0	V
TA	Operating Temperature	0 to +75	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150
		Plastic	-55 to +125
PT	Power Dissipation	1.5	W
IOUT	DC Output Current (Output High)	-50	mA

NOTE: 2764 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ECL-10K DC ELECTRICAL CHARACTERISTICS**

(VEE = -5.2V, RL = 50Ω to -2.0V, TA = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions	Min. (B)	Typ. <sup>(1)</sup>	Max. (A)	Unit	TA
VOH	Output HIGH Voltage	V IN = V IHA or V ILB	-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
VOL	Output LOW Voltage	V IN = V IHA or V ILB	-1870 -1850 -1830	-	-1665 -1650 -1625	mV	0°C 25°C 75°C
VOHC	Output Threshold HIGH Voltage	V IN = V IHB or V ILA	-1020 -980 -920	-	-	mV	0°C 25°C 75°C
VOLC	Output Threshold LOW Voltage	V IN = V IHB or V ILA	-	-	-1645 -1630 -1605	mV	0°C 25°C 75°C
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs	-1145 -1105 -1045	-	-840 -810 -720	mV	0°C 25°C 75°C
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs	-1870 -1850 -1830	-	-1490 -1475 -1450	mV	0°C 25°C 75°C
IIH	Input HIGH Current	V IN = V IHA	CS	-	220	μA	-
			Others	-	110	μA	-
IIL	Input LOW Current	V IN = V ILB	CS	0.5	170	μA	-
			Others	-50	90	μA	-
IEE	Supply Current	All Inputs and Outputs Open	-190	-130	-	mA	-

NOTE: 2764 tbl 06

1. Typical parameters are specified at VEE = -5.2V, TA = +25°C and maximum loading.

**ECL-100K ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage With Respect to GND	+0.5 to -7.0	V
TA	Operating Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150
		Plastic	-55 to +125
PT	Power Dissipation	1.5	W
IOUT	DC Output Current (Output High)	-50	mA

2762 tbl 07

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ECL-100K DC ELECTRICAL CHARACTERISTICS**

(VEE = -4.5V, RL = 50Ω to -2.0V, TA = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions	Min. (B)	Typ. <sup>(1)</sup>	Max. (A)	Unit
VOH	Output HIGH Voltage	VIN = VIH A or VIL B	-1025	-955	-880	mV
VOL	Output LOW Voltage	VIN = VIH A or VIL B	-1810	-1715	-1620	mV
VOHC	Output Threshold HIGH Voltage	VIN = VIH B or VIL A	-1035	-	-	mV
VOLC	Output Threshold LOW Voltage	VIN = VIH B or VIL A	-	-	-1610	mV
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs	-1165	-	-880	mV
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs	-1810	-	-1475	mV
IIH	Input HIGH Current	VIN = VIH A	CS	-	220	μA
			Others	-	110	
IIL	Input LOW Current	VIN = VIL B	CS	0.5	170	μA
			Others	-50	90	
IEE	Supply Current	All Inputs and Outputs Open	-170	-110	-	mA

2762 tbl 08

**NOTE:**

1. Typical parameters are specified at VEE = -4.5V, TA = +25°C and maximum loading.

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**ECL-101K ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage With Respect to GND	+0.5 to -7.0	V
TA	Operating Temperature	0 to +75	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150
		Plastic	-55 to +125
PT	Power Dissipation	1.5	W
I <sub>OUT</sub>	DC Output Current (Output High)	-50	mA

2763 tbl 09

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ECL-101K DC ELECTRICAL CHARACTERISTICS**

(V<sub>EE</sub> = -5.2V, R<sub>L</sub> = 50Ω to -2.0V, T<sub>A</sub> = 0 to +75°C, air flow exceeding 2 m/sec)

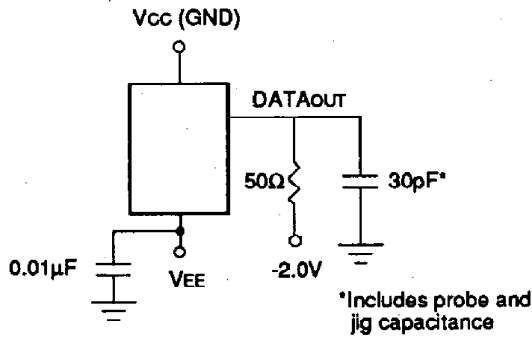
Symbol	Parameter	Test Conditions	Min. (B)	Typ. <sup>(1)</sup>	Max. (A)	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>IN</sub> = V <sub>IHA</sub> or V <sub>ILB</sub>	-1025	-955	-880	mV	
V <sub>OL</sub>	Output LOW Voltage	V <sub>IN</sub> = V <sub>IHA</sub> or V <sub>ILB</sub>	-1810	-1715	-1620	mV	
V <sub>OHc</sub>	Output Threshold HIGH Voltage	V <sub>IN</sub> = V <sub>IHB</sub> or V <sub>ILA</sub>	-1035	-	-	mV	
V <sub>OLc</sub>	Output Threshold LOW Voltage	V <sub>IN</sub> = V <sub>IHB</sub> or V <sub>ILA</sub>	-	-	-1610	mV	
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs	-1165	-	-880	mV	
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs	-1810	-	-1475	mV	
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>IHA</sub>	$\overline{CS}$	-	-	220	μA
			Others	-	-	110	
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = V <sub>ILB</sub>	$\overline{CS}$	0.5	-	170	μA
			Others	-50	-	90	
I <sub>EE</sub>	Supply Current	All Inputs and Outputs Open	-190	-130	-	mA	

2763 tbl 10

**NOTE:**

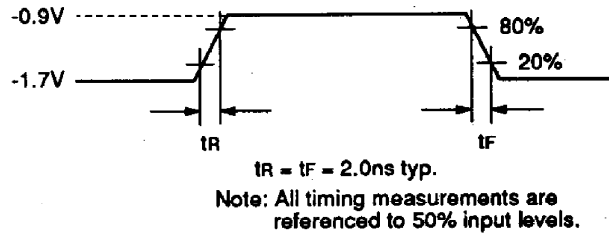
1. Typical parameters are specified at V<sub>EE</sub> = -5.2V, T<sub>A</sub> = +25°C and maximum loading.

**AC TEST LOAD CONDITION**



2764 drw 06

**AC TEST INPUT PULSE**



2764 drw 07

**RISE/FALL TIME**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	-	-	2	-	ns
tF	Output Fall Time	-	-	2	-	ns

2764 tbl 11

**FUNCTIONAL DESCRIPTION**

The IDT10494, IDT100494 and IDT101494 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 16K x 4 ECL SRAMs. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

**READ TIMING**

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select (CS). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

**WRITE TIMING**

To write data to the device, a Write Pulse need be formed on the Write Enable input (WE) to control the write to the SRAM array. While CS and ADDR must be set-up when WE goes low, DataIN can settle after the falling edge of WE, giving the datapath extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If CS is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

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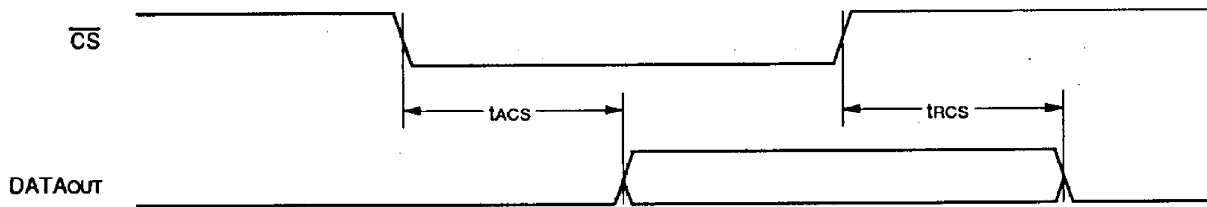
**AC ELECTRICAL CHARACTERISTICS** (Over the AC Operating Range)

Symbol	Parameter <sup>(1)</sup>	Test Condition	10494S7 100494S7 101494S7		10494S8 100494S8 101494S8		10494S10 100494S10 101494S10		10494S15 100494S15 101494S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>											
tACS	Chip Select Access Time	-	-	3	-	5	-	5	-	5	ns
tRCS	Chip Select Recovery Time	-	-	3	-	5	-	5	-	5	ns
tAA	Address Access Time	-	-	7	-	8	-	10	-	15	ns
tOH	Data Hold from Address Change	-	3	-	3	-	3	-	3	-	ns

2764 tbl 12

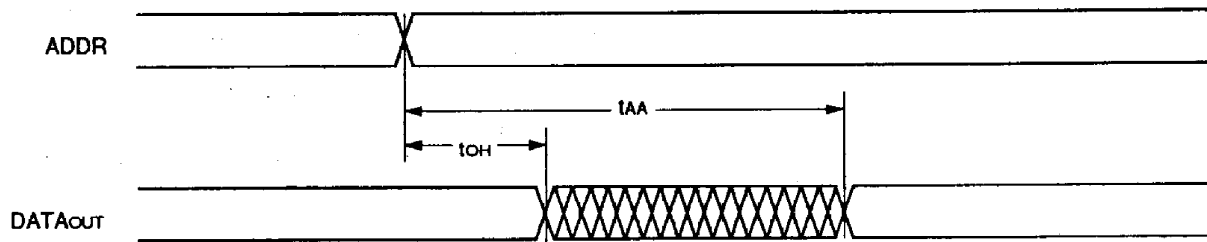
NOTE:  
 1. Input and Output reference level is 50% point of waveform.

**READ CYCLE GATED BY CHIP SELECT**



2764 drw 08

**READ CYCLE GATED BY ADDRESS**



2764 drw 09

**AC ELECTRICAL CHARACTERISTICS** (Over the AC Operating Range)

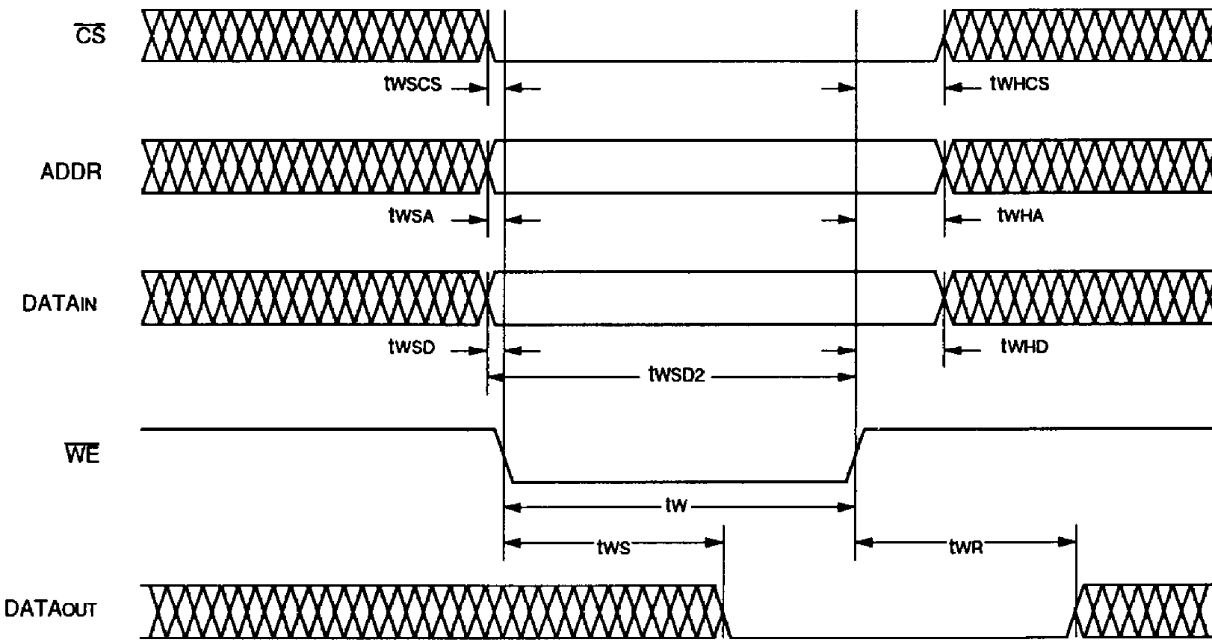
Symbol	Parameter <sup>(1)</sup>	Test Condition	10494S7 100494S7 101494S7		10494S8 100494S8 101494S8		10494S10 100494S10 101494S10		10494S15 100494S15 101494S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Cycle</b>											
tw	Write Pulse Width	tWSA = minimum	5	-	6	-	8	-	10	-	ns
tWSD	Data Set-up Time	-	0	-	0	-	0	-	2	-	ns
tWSD <sub>2</sub> <sup>(2)</sup>	Data Set-up Time to WE High	-	5	-	5	-	5	-	5	-	ns
tWSA	Address Set-up Time	tWSA = minimum	0	-	0	-	0	-	2	-	ns
tWSCS	Chip Select Set-up Time	-	0	-	0	-	0	-	2	-	ns
tWHD	Data Hold Time	-	1	-	2	-	2	-	3	-	ns
tWHA	Address Hold Time	-	1	-	2	-	2	-	3	-	ns
tWHCS	Chip Select Hold Time	-	1	-	2	-	2	-	3	-	ns
tWS	Write Disable Time	-	-	5	-	5	-	5	-	5	ns
tWR <sup>(3)</sup>	Write Recovery Time	-	-	5	-	5	-	5	-	5	ns

2764 tbl 13

**NOTES:**

1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of WE for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of WE.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Qo to Qa) when no new Address Transition occurs.

**WRITE CYCLE TIMING DIAGRAM**

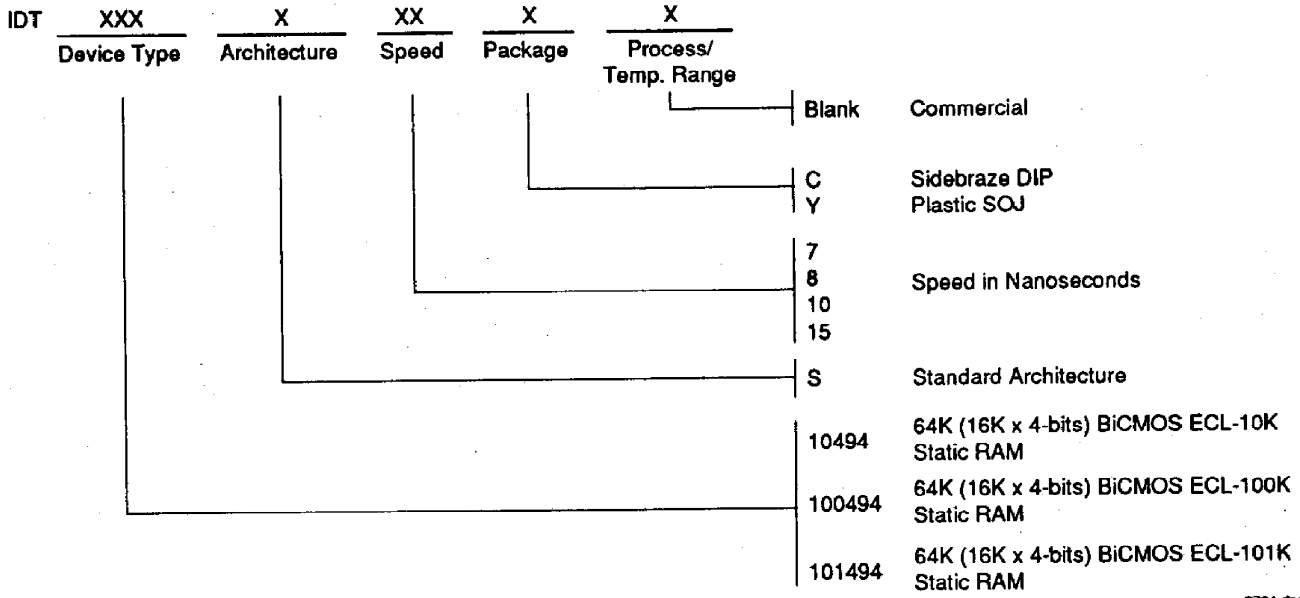


2764 drw 10

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**ORDERING INFORMATION**



2764 drw 11