CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256S IDT71256L

FEATURES:

- · High-speed address/chip select time
 - Military: 25/30/35/45/55/70/85/100/120/150ns (max.)
 - Commercial: 20/25/35/45ns (max.) Low Power only.
- Low-power operation
- Battery Backup operation 2V data retention
- Produced with advanced high-performance CMOS technology
- Input and output directly TTL-compatible
- Available in standard 28-pin (300 or 600 mil) ceramic DIP, 28-pin (600 mil) plastic DIP, 28-pin (300 mil) SOJ and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

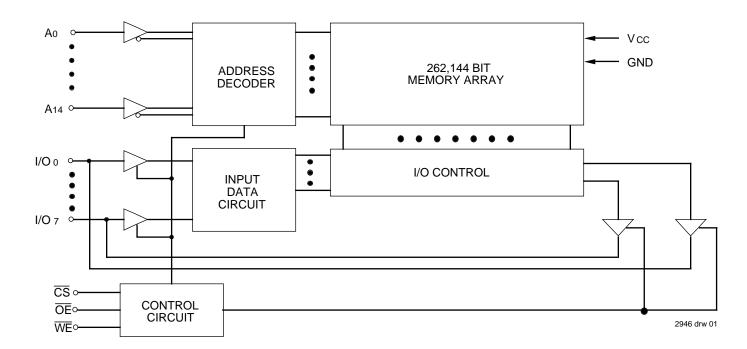
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's highperformance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When \overline{CS} goes HIGH, the circuit will automatically go to, and remain in, a low-power standby mode as long as CS remains HIGH. In the full standby mode, the low-power device consumes less than 15μW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin (300 or 600 mil) ceramic DIP, a 28-pin 300 mil J-bend SOIC, and a 28-pin (600 mil) plastic DIP, and 32-pin LCC providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

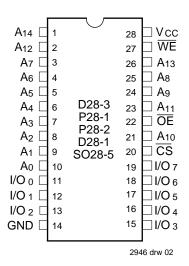
FUNCTIONAL BLOCK DIAGRAM



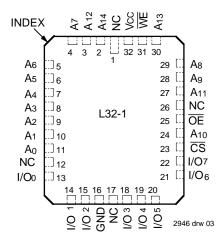
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

AUGUST 1996

PIN CONFIGURATIONS



DIP/SOJ TOP VIEW



32-Pin LCC TOP VIEW

TRUTH TABLE(1)

WE	<u>cs</u>	ŌĒ	I/O	Function
Х	Н	Х	High-Z	Standby (ISB)
Х	VHC	Х	High-Z	Standby (ISB1)
Н	L	Н	High-Z	Output Disabled
Н	L	L	Dout	Read Data
L	L	Х	DIN	Write Data

NOTE:1. H = VIH, L = VIL, X = Don't Care

2946 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	٧
ТА	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	ç
Тѕтс	Storage Temperature	-55 to +125	-65 to +150	°C
Рт	Power Dissipation	1.0	1.0	W
Іоит	DC Output Current	50	50	mA

NOTE:

2946 tbl 03

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTIONS

Name	Description
A0-A14	Addresses
I/O0–I/O7	Data Input/Output
CS	Chip Select
WE	Write Enable
ŌĒ	Output Enable
GND	Ground
VCC	Power

2946 tbl 01

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
CI/O	I/O Capacitance	Vout = 0V	11	pF

NOTE:

2046 thi 0/

 This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2946 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	_	6.0	V
VIL	Input Low Voltage	$-0.5^{(1)}$	_	0.8	V

NOTE:

2946 tbl 06

DC ELECTRICAL CHARACTERISTICS(1, 2)

 $(VCC = 5.0V \pm 10\%, VLC = 0.2V, VHC = VCC - 0.2V)$

			71256S/L20		71256S/L25		71256S/L30		71256S/L35		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
Icc Dynamic Operating Current $\overline{\text{CS}} \leq \text{VIL}$, Outputs Open $\text{Vcc} = \text{Max.}$, $f = \text{fMAX}^{(2)}$		S	_	_	_	150	_	145	_	140	mA
		L	135	_	115	130	_	125	105	120	
Curre CS ≥	Standby Power Supply Current (TTL Level)	S	_	_	_	20	_	20	_	20	mA
	CS ≥ VIH, VCC = Max., Outputs Open, f = fMax ⁽²⁾	L	3	_	3	3		3	3	3	
	Full Standby Power Supply	S	_	_	_	20	_	20	_	20	mA
	Current (CMOS Level) CS ≥ VHC, VCC = Max., f = 0	L	0.4	_	0.4	1.5	_	1.5	0.4	1.5	

			71256S/L45		71256S/L55		71256S/L70		71256S/L85 ⁽³⁾		71256S/L100 ⁽³⁾		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
Icc	Icc Dynamic Operating Current CS ≤ VIL, Outputs Open	S	-	135	_	135	_	135	_	135	_	135	mA
VCC = Max., f = fMAX ⁽²⁾	L	100	115	_	115	_	115	_	115	_	115		
ISB	Standby Power Supply Current (TTL Level)	S	_	20	_	20	_	20		20	_	20	mA
$\overline{\text{CS}} \ge \text{VIH}, \text{VCC} = \text{Max.},$ Outputs Open, $f = \text{fMAX}^{(2)}$	L	3	3	_	3	_	3		3	_	3		
ISB1	Full Standby Power Supply Current (CMOS Level)	S	-	20	_	20	_	20	_	20	_	20	mA
	$\overline{CS} \ge VHC$, $VCC = Max.$, $f = 0$	L	0.4	1.5	_	1.5	_	1.5	_	1.5	_	1.5	

NOTES:

2946 tbl 07

- 1. All values are maximum guaranteed values.
- 2. fmax = 1/trc, all address inputs cycling at fmax; f = 0 means no address pins are cycling.
- 3. Also available: 120 and 150 ns military devices.

^{1.} VIL (min.) = -3.0V for pulse width less than 20ns, once per cycle.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2946 tbl 08

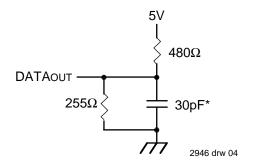


Figure 1. AC Test Load

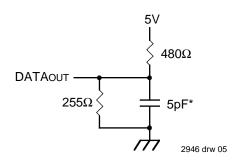


Figure 2. AC Test Load (for tcLz, toLz, tcHz, toHz, toW, tWHz)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

 $VCC = 5.0V \pm 10\%$

				IDT71256S			ID			
Symbol	Parameter	Test Condition		Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
ILI	Input Leakage Current	Vcc = Max., Vin = GND to Vcc	MIL. COM'L.	1 1	_	10 5			5 2	μА
lLO	Output Leakage Current	Vcc = Max., \overline{CS} = ViH, Vout = GND to Vcc	MIL. COM'L.		_	10 5	_		5 2	μА
Vol	Output Low Voltage	IoL = 8mA, Vcc = Min.			_	0.4	_	_	0.4	V
		IOL = 10mA, VCC = Min.		_	_	0.5		_	0.5	
Vон	Output High Voltage	IOH = -4mA, $VCC = Min$.		2.4	_		2.4		_	V

2946 tbl 09

2946 tbl 10

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VLC = 0.2V, VHC = VCC - 0.2V

					Ty Vo	p. ⁽¹⁾ :c @	Max. Vcc @		
Symbol	Parameter	Test Condition		Min.	2.0v	3.0V	2.0V	3.0V	Unit
VDR	Vcc for Data Retention	_		2.0	_	_	_	_	V
ICCDR	Data Retention Current		MIL. COM'L.	_	_	_	500 120	800 200	μА
tCDR	Chip Deselect to Data Retention Time	CS ≥ VHC		0	_	_	_	_	ns
tR ⁽³⁾	Operation Recovery Time			tRC ⁽²⁾	_	_	_	_	ns

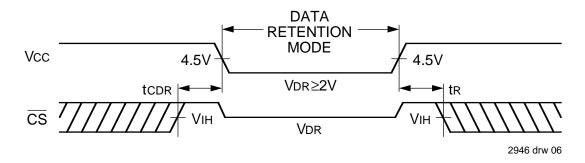
7.2

NOTES:

- 1. $TA = +25^{\circ}C$.
- 2. trc = Read Cycle Time.
- 3. This parameter is guaranteed, but not tested.

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LOW Vcc DATA RETENTION WAVEFORM



AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		71256L20 ⁽¹⁾		71256S25 71256L25		71256S30 ⁽³⁾ 71256L30 ⁽³⁾		71256S35 71256L35		71256S45 71256L45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cy	Read Cycle								ı			
trc	Read Cycle Time	20	_	25	_	30	_	35	_	45	_	ns
tAA	Address Access Time	_	20		25	_	30	_	35		45	ns
tacs	Chip Select Access Time	_	20		25		30	_	35		45	ns
tcLZ ⁽²⁾	Chip Select to Output in Low-Z	5	_	5	_	5		5	_	5	_	ns
tCHZ ⁽²⁾	Chip Deselect to Output in High-Z	_	10	_	11	_	15	_	15	_	20	ns
toE	Output Enable to Output Valid	_	10	_	11	_	13	_	15	_	20	ns
tolz(2)	Output Enable to Output in Low-Z	2	_	2	_	2	_	2	_	0	_	ns
toHZ ⁽²⁾	Output Disable to Output in High-Z	2	8	2	10	2	12	2	15	_	20	ns
tон	Output Hold from Address Change	5	_	5	_	5	_	5	_	5	_	ns
Write Cy	cle	*	•									•
twc	Write Cycle Time	20	_	25	_	30	_	35	_	45	_	ns
tcw	Chip Select to End-of-Write	15	_	20	_	25		30	_	40	_	ns
taw	Address Valid to End-of-Write	15	_	20	_	25		30	_	40	_	ns
tas	Address Set-up Time	0	_	0	_	0		0	_	0	_	ns
twp	Write Pulse Width	15	_	20	_	25	_	30	_	35		ns
twr	Write Recovery Time	0	_	0	_	0	_	0	_	0	_	ns
tow	Data to Write Time Overlap	11	_	13	_	14	_	15	_	20	_	ns
twHZ ⁽²⁾	Write Enable to Output in High-Z	_	10	_	11	_	15	_	15	_	20	ns
tDH	Data Hold from Write Time	0	_	0		0	_	0		0		ns
tow ⁽²⁾	Output Active from End-of-Write	5	_	5	_	5	_	5	_	5	_	ns

NOTES:

2946 tbl 11

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- 1. 0° to +70°C temperature range only.
- 2. This parameter guaranteed by device characterization, but is not production tested.
- 3. -55° to $+125^{\circ}$ C temperature range only.

AC ELECTRICAL CHARACTERISTICS (Vcc = $5.0V \pm 10\%$, All Temperature Ranges)

		71256S55 ⁽¹⁾ 71256L55 ⁽¹⁾		71256S70 ⁽¹⁾ 71256L70 ⁽¹⁾		71256S85 ⁽¹⁾ 71256L85 ⁽¹⁾		71256S100 ^(1,3) 71256L100 ^(1,3)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	55		70		85	_	100	_	ns
tAA	Address Access Time	_	55	_	70	_	85	_	100	ns
tACS	Chip Select Access Time	_	55	_	70	_	85	_	100	ns
tCLZ ⁽²⁾	Chip Deselect to Output in Low-Z	5	_	5	_	5	_	5	_	ns
tCHZ ⁽²⁾	Output Enable to Output in Low-Z	_	25	_	30	_	35	_	40	ns
toE	Output Enable to Output Valid	_	25	_	30	_	35	_	40	ns
tolz(2)	Output Enable to Output in Low-Z	0	_	0	_	0	_	0	_	ns
tohz ⁽²⁾	Output Disable to Output in High-Z	0	25	0	30	_	35	_	40	ns
toh	Output Hold from Address Change	5	_	5	_	5	_	5	_	ns
Write Cycle										
twc	Write Cycle Time	55	_	70	_	85	-	100	_	ns
tcw	Chip Select to End-of-Write	50	_	60	_	70	_	80	_	ns
taw	Address Valid to End-of-Write	50	_	60		70		80	_	ns
tas	Address Set-up Time	0	_	0	_	0		0	_	ns
twp	Write Pulse Width	40	_	45		50		55	_	ns
twr	Write Recovery Time	0	_	0	_	0	_	0	_	ns
tow	Data to Write Time Overlap	25	_	30	_	35		40	_	ns
tDH	Data Hold from Write Time (WE)	0	_	0		0	_	0	_	ns
twHZ ⁽²⁾	Write Enable to Output in High-Z		25	_	30	1	35	_	40	ns
tow ⁽²⁾	Output Active from End-of-Write	5	_	5	_	5	_	5	_	ns

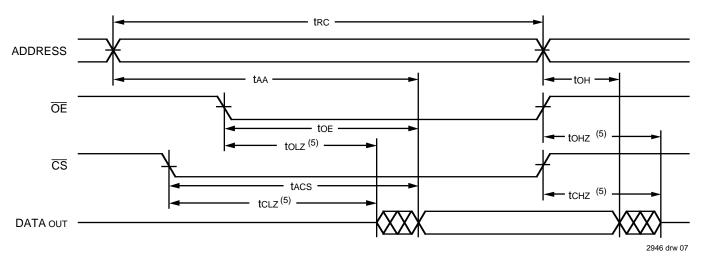
NOTES:

2946 tbl 11

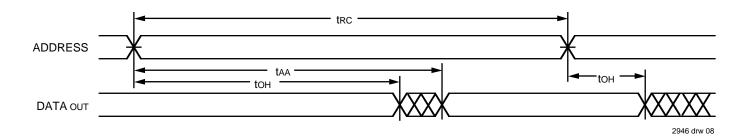
6

- -55°C to +125°C temperature range only.
 This parameter guaranteed by device characterization, but is not production tested.
- 3. Also available: 120 and 150 ns military devices.

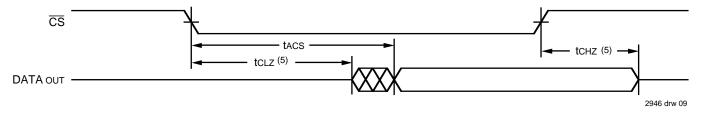
TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



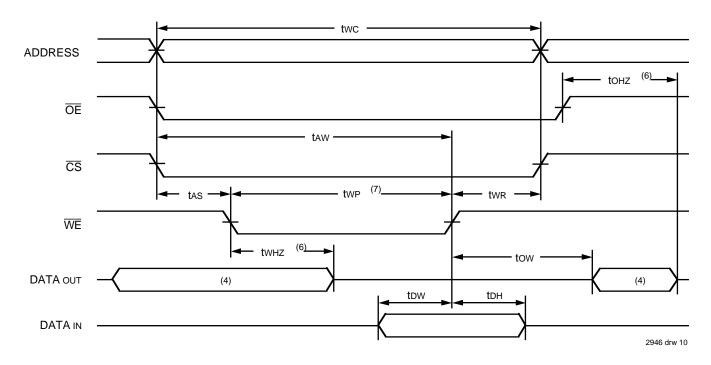
TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)



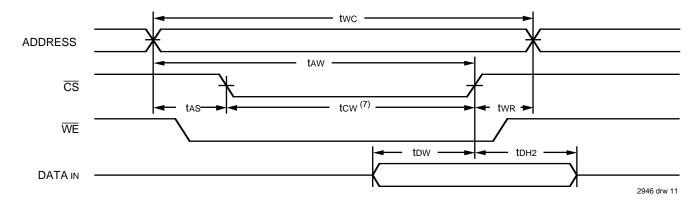
NOTES:

- WE is HIGH for Read cycle.
 Device is continuously selected, S is LOW.
- 3. Address valid prior to or coincident with $\overline{\text{CS}}$ transition LOW.
- 4. OE is LOW.
- 5. Transition is measured $\pm 200 \text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)(1, 2, 3, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING) $^{(1, 2, 3, 5)}$



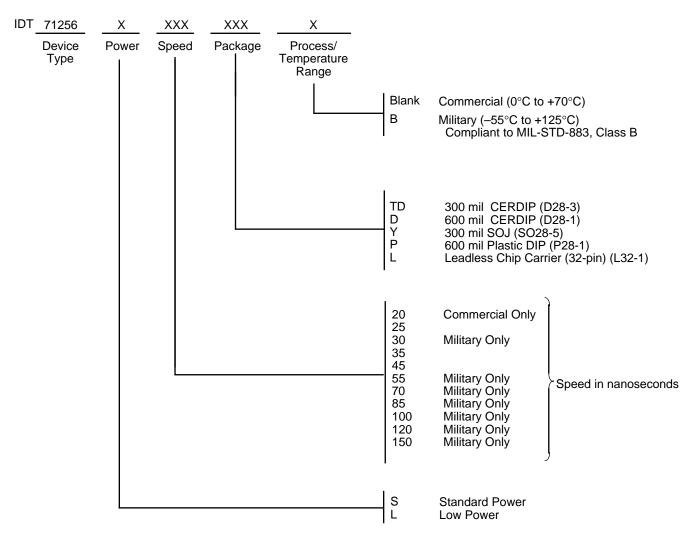
NOTES:

- 1. WE or CS must be HIGH during all address transitions.
- 2. A write occurs during the overlap of a LOW $\overline{\text{CS}}$ and a LOW $\overline{\text{WE}}$.
- 3. two is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
- 4. During this period, I/O pins are in the output state so that the input signals must not be applied.
- 5. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
- 6. Transition is measured $\pm 200 \text{mV}$ from steady state.
- 7. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of twp or (twHz + tbW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tbW. If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified twp. For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to tcw.

7.2

8

ORDERING INFORMATION



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