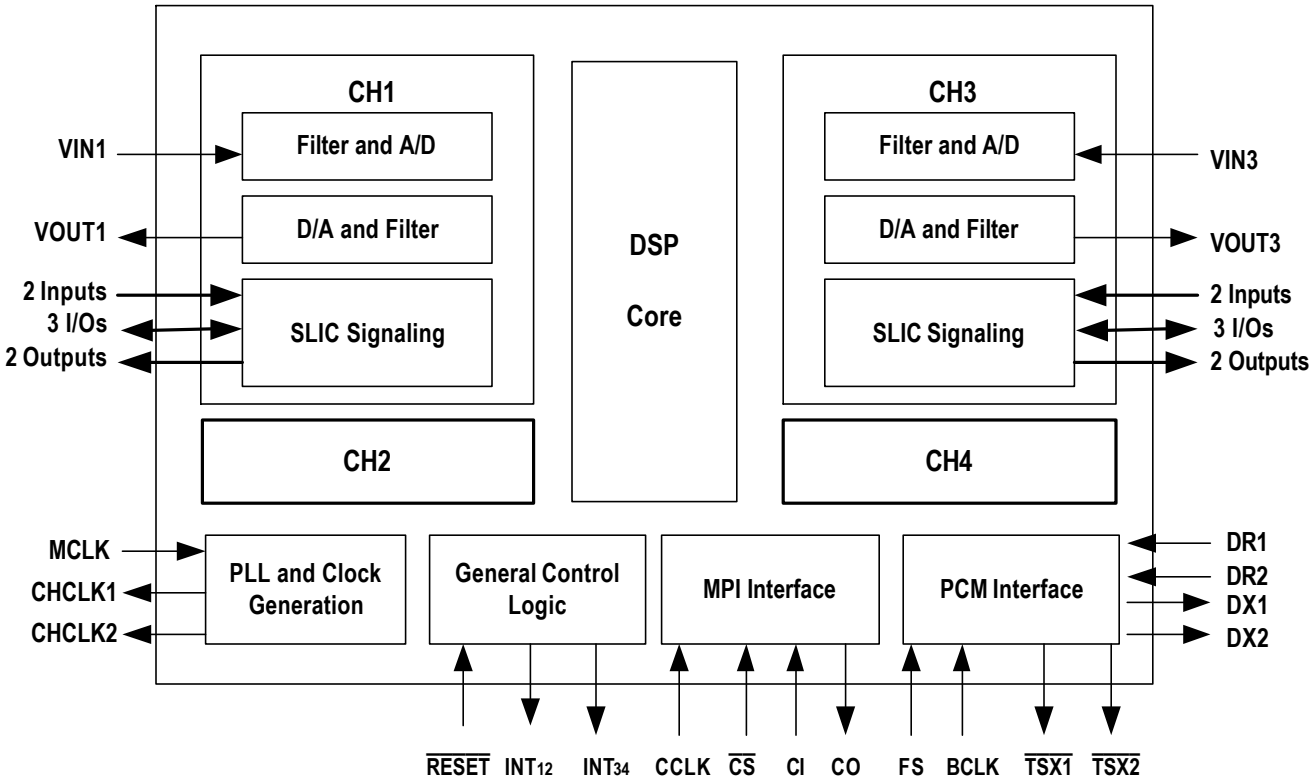
QUAD PROGRAMMABLE PCM CODEC WITH MPI INTERFACE

PRELIMINARY
IDT821054

FEATURES

- 4 channel CODEC with on-chip digital filters
- Software selectable A/μ-law, Linear Code conversion
- Meets ITU-T G.711 - G.714 requirements
- Programmable digital filters adapting to system demands:
  - *AC impedance matching*
  - *Transhybrid balance*
  - *Frequency response correction*
  - *Gain setting*
- Support two programmable PCM buses
- Flexible PCM interface with up to 128 programmable time slots, data rate from 512kbits/s to 8.192Mbits/s
- MPI control interface
- Broadcast mode for coefficient setting
- 7 SLIC signaling pins (including 2 debounced pins) per channel
- Fast hardware ring trip mechanism
- Two programmable tone generators per channel for testing, ringing and DTMF generation
- FSK generator
- Two programmable chopper clocks
- Master clock frequency selectable: 1.536MHz, 1.544MHz, 2.048MHz, 3.072MHz, 3.088MHz, 4.096MHz, 6.144MHz, 6.176 MHz or 8.192 MHz
- Advanced test capabilities
  - *3 analog loop back tests*
  - *5 digital loop back tests*
  - *Level metering function*
- High analog driving capability (300Ω AC)
- TTL and CMOS compatible digital I/O
- CODEC identification
- +5 V single power supply
- Low power consumption
- Operating temperature range: -40°C to +85°C
- Package available: PQFP_64_PM

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The IDT821054 is a feature rich, single-chip, programmable 4 channel PCM CODEC with on-chip filters. Besides the μ-Law/A-Law companding and linear Coding/decoding (14 effective bits + 2 extra sign bits), IDT821054 also provides 1 FSK generator (can be used for sending Caller-ID messages), 2 programmable Tone generators per channel (which can also generate ring signals) together with 2 programmable chopper clocks for SLIC.

The digital filters in IDT821054 provide the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. An integrated programmable DSP realizes AC Impedance Matching, Transhybrid Balance, Frequency Response Correction and Gain Setting functions. The IDT821054 supports 2 PCM buses with programmable sampling edge, which allows an extra delay of up to 7 clocks. Once the delay is determined, it is effective to all four channels of IDT821054. The device also provides 7 signaling pins to SLIC on per channel basis.

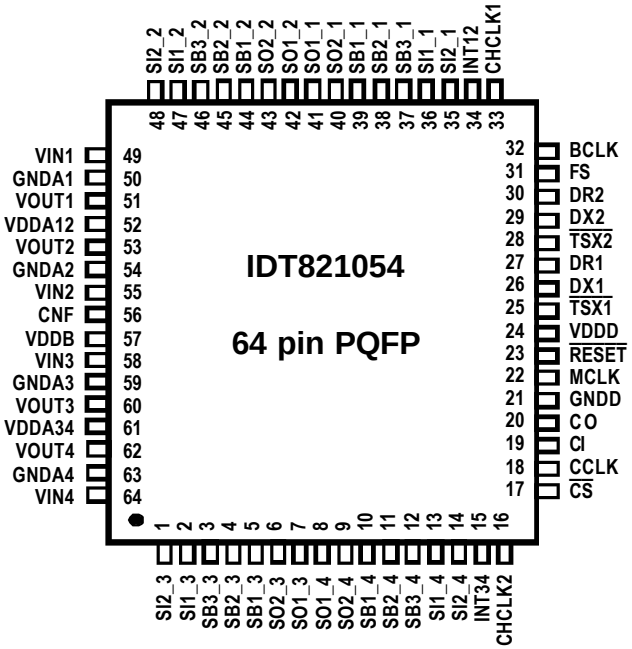
The IDT821054 has a MPI interface and supports both compressed and linear data format.

The device also offers strong test capability with several analog/digital loopbacks and level metering function. It brings convenience to system maintenance and diagnosis.

A unique feature of 'Hardware Ring Trip' is implemented in IDT821054. When off-hook signal is detected, IDT821054 can reverse an output pin to stop ringing immediately.

The IDT821054 can be used in digital telecommunication applications such as Central Office Switch, PBX, DLC and Integrated Access Devices (IADs), i.e. VoIP and VoDSL.

PIN CONFIGURATIONS



PIN DESCRIPTION

Name	Type	Pin Number	Description
GNDA1 GNDA2 GNDA3 GNDA4	P	50 54 59 63	**Analog Ground.** All ground pins should be connected together.
GNDD	P	21	**Digital Ground.** All digital signals are referred to this pin.
VDDA12 VDDA34	P	52 61	**+5V Analog Power Supply.** These pins should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDD	P	24	**+5V Digital Power Supply.**
VDDB	P	57	**+5V Analog Power Supply.** This pin should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
CNF	-	56	**Capacitor Noise Filter** This pin should be connected to ground via a 0.22μF capacitor.
VIN1-4	I	49, 55, 58, 64	**Analog Voice Inputs.** These pins should be connected to the SLIC via a capacitor (0.22 μF).
VOUT1-4	O	51, 53, 60, 62	**Voice Frequency Receiver Outputs.** These pins can drive 300 Ω AC load. It can drive transformers directly.
SI1_(1-4) SI2_(1-4)	I	36, 47, 2, 13 35, 48, 1, 14	**SLIC signalling Inputs with de-bounced function for Channel 1-4.**
SB1_(1-4) SB2_(1-4) SB3_(1-4)	I/O	39, 44, 5, 10 38, 45, 4, 11 37, 46, 3, 12	**Bi-directional SLIC Signalling I/Os for Channel 1-4, can be programmed as Input or Output.**
SO1_(1-4) SO2_(1-4)	O	41, 42, 7, 8 40, 43, 6, 9	**SLIC Signalling Outputs for Channel 1-4.**
DX1	O	26	**Transmit PCM Data Output, PCM highway One.** Transmit PCM Data to PCM-High-way One. This pin is tri-state output pin.
DX2	O	29	**Transmit PCM Data Output, PCM highway Two.** Transmit PCM Data to PCM-High-way Two. This pin is tri-state output pin.
DR1	I	27	**Receive PCM Data Input, PCM highway One.** PCM data is shifted into DR1 or DR2 by the BCLK. PCM data can be received from DR1or DR2 depending on programming command.
DR2	I	30	**Receive PCM Data Input, PCM highway Two.** PCM data is shifted into DR1 or DR2 by the BCLK. PCM data can be received from DR1or DR2. Refer to the description of DR1 pin.
FS	I	31	**Frame Synchronisation** FS is an 8 kHz synchronisation clock that identifies the beginning of the PCM frame.
BCLK	I	32	**Bit Clock.** This pin clocks out the PCM data to DX1 or DX2 pin and clocks in data from DR1 or DR2 pin. It may vary from 512kHz to 8.192 MHz, and should be synchronous with FS.
$\overline{TSX1}$ $\overline{TSX2}$	0	25 28	**Transmit Output Indicator.** $\overline{TSX1}$ becomes low when data is transmitted via DX1, open-drain. $\overline{TSX2}$ becomes low when data is transmitted via DX2, open-drain.
$\overline{CS}$	I	17	**Chip Select.** A low level on this pin enables the Serial Control Interface.
CI	I	19	**Serial Control Interface Data Input.** μ-Controller interface, Control data input, CCLK determines the data rate.
CO	O	20	**Serial Control Interface Data Tri-State Output.** μ-Controller interface, control data output pin, CCLK determines the data rate.
CCLK	I	18	**Serial Control Interface Clock.** This is the clock for Serial Control Interface. It can be up to 8.192 MHz.
MCLK	I	22	**Master Clock Input.** Master clock provides the clock for DSP. It can be 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072MHz, 3.088MHz, 4.096 MHz, 6.144MHz, 6.176MHz or 8.192 MHz.
$\overline{RESET}$	I	23	**Reset Input.** Forces the device to default mode. Active low.

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin Number	Description
INT12	O	34	**Interrupt Output Pin.** Active high interrupt signal for ch1-ch2. It reflects the changes on SLIC pins.
INT34	O	15	**Interrupt Output Pin.** Active high interrupt signal for ch3-ch4. It reflects the changes on SLIC pins.
CHCLK1	O	33	**Chopper Clock Output.** Provides a programmable (2 -28 ms) output signal synchronous to MCLK.
CHCLK2	O	16	**Chopper Clock Output.** Provides a programmable 256 kHz, or 512 kHz or 16.384 MHz output signal synchronous to MCLK.

FUNCTIONAL DESCRIPTION

The IDT821054 contains four channel PCM CODEC with on-chip digital filters. It provides the four-wire solution for the subscriber line circuitry in digital switches. The IDT821054 converts analog voice signals to digital PCM samples and digital PCM samples back to analog voice signals. Digital filters are used to bandlimit the voice signals during conversion. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) in IDT821054 provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering, sample rate conversion and PCM companding. See the Functional Block Diagram.

MPI/PCM INTERFACE

A serial Microprocessor Interface (MPI) is provided for the master device to control the IDT821054; and two PCM buses are provided to transfer the digital voice data.

MPI CONTROL MODE

The internal configuration registers (local/global), the SLIC signaling interface and the Coefficient-RAM, FSK-RAM of the IDT821054 are programmed by microprocessor via the serial control interface, which consists of four lines (pins): CCLK, $\overline{CS}$, CI and CO. All the commands and data transmitted or received are aligned in byte (8 bits). CCLK is the Serial Control Interface Clock, it can be up to 8.192MHz; $\overline{CS}$ is the Chip Selection pin, a low level on it enable the serial control interface; CI and CO are the serial control interface data input and output, carrying the control commands and data bytes to/from the IDT821054.

The data transfer is synchronized to the CCLK input. The contents of CI is latched on the rising edges of CCLK, while CO changes on the falling edges of CCLK. CCLK is the only reference of CI and CO pins. Its duty and frequency may not necessarily be standard.

When $\overline{CS}$ pin becomes low, IDT821054 treats the first byte on CI pin as command, and the rest as data. To write another command, $\overline{CS}$ pin must change from low to high to finish the previous command and then change from high to low to indicate the start of the next command. When a read/write operation is completed, $\overline{CS}$ pin must be pulled to high in 8-bit time.

During the execution of commands that are followed by output data, the device will not accept any new commands from CI pin. The data transfer sequence can be interrupted by setting $\overline{CS}$ pin high. See Figure 1 and 2.

PCM BUS

IDT821054 provides two flexible PCM buses for all 4 channels. The digital PCM data can be compressed (A/μ-law) or linear code. The data rate can be configured as the same as Bit Clock (BCLK) or half of it. The data can be transmitted or received either on BCLK rising edges or falling edges. The data transmit and receive time slot can offset from Frame Synchronization (FS) by 0 to 7 BCLK period(s). See Figure 3. All the selections are implemented by Global Command 7, which is configured for all 4 channels.

The PCM data of each channel can be assigned to any time slot of the PCM bus. The number of available time slots is determined by BCLK frequency. For example, when BCLK is 512 kHz, time slot 0-7 are available; when BCLK is 1.024 MHz, time slot 0-15 are available; when BCLK is 8.192 MHz, time slot 0-127 are available. The IDT821054 allows BCLK frequency between 512 kHz and 8.192 MHz at increments of 64 kHz.

When compressed format (8-bit wide) is selected, the voice data of one channel occupies one time slot. The TT[6:0] bits in Local Command 5 selects the transmit time slot for each channel, while the RT[6:0] bits in Local Command 6 selects the receive time slot for each channel.

When linear format is selected, the voice data is a 16-bit 2's complement number(b15 and b14 are the same as b13, which is the sign bit, b13 to b0 are effective bits). Then the voice data of one channel occupies a time slot group, which is consisted of 2 adjacent time slots. The TT[6:0] bits in Local Command 5 select the transmit time slot group for each channel, while the RT[6:0] bits in Local Command 6 select the receive time slot group for each channel.

PCM data for each individual channel can be clocked out to DX1 or DX2 pin on the programmed edges of BCLK according to time slot assignment. The transmit highway (DX1/2) is selected by the THS bit in Local Command 5. The frame sync (FS) pulse identifies the beginning of a transmit frame, or time slot 0. The PCM data is transmitted serially on DX1 or DX2 with MSB first.

PCM data for each channel can be clocked into DR1 or DR2 pin on the programmed edges of BCLK according to time slot assignment. The receive highway (DR1/2) is selected by the RHS bit in Local Command 6. The frame sync (FS) pulse identifies the beginning of a receive frame, or time slot 0. The PCM data is received serially from DR1 or DR2 with MSB first.

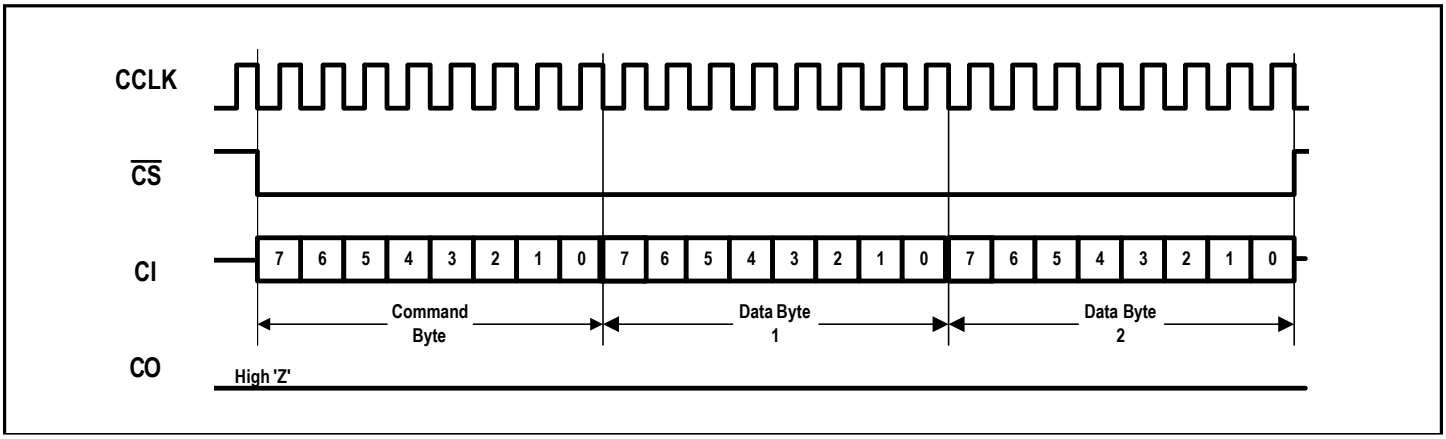


Figure 1. An Example of Serial Interface Write Mode

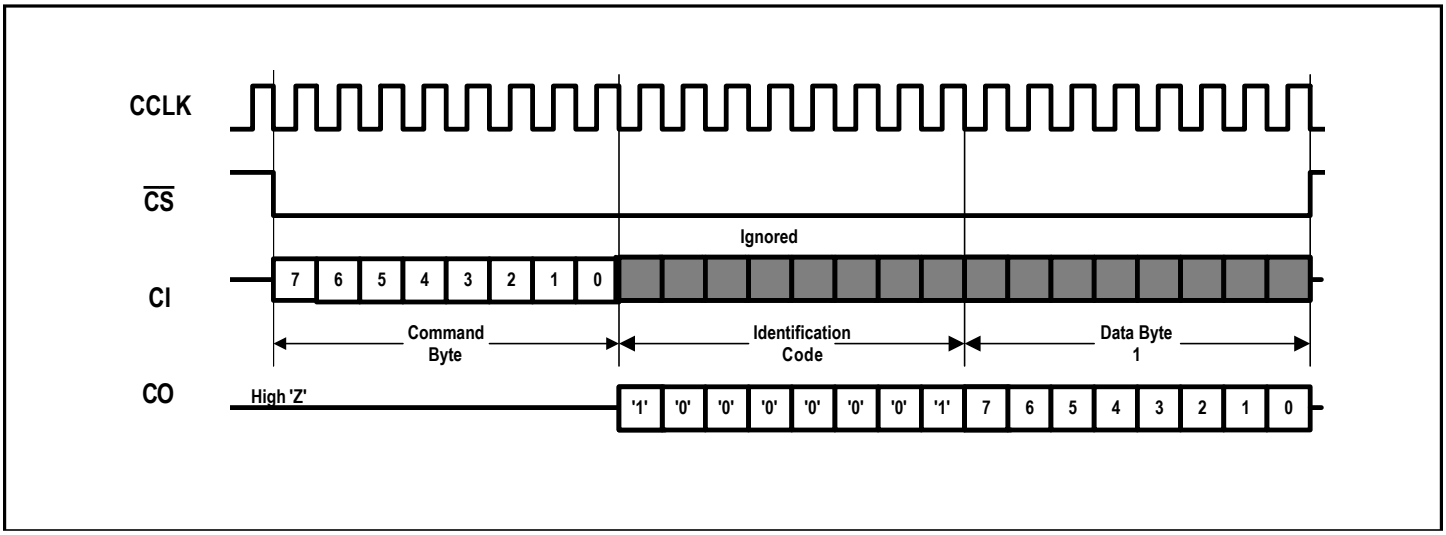


Figure 2. An Example of Serial Interface Read Mode (ID = 81H)

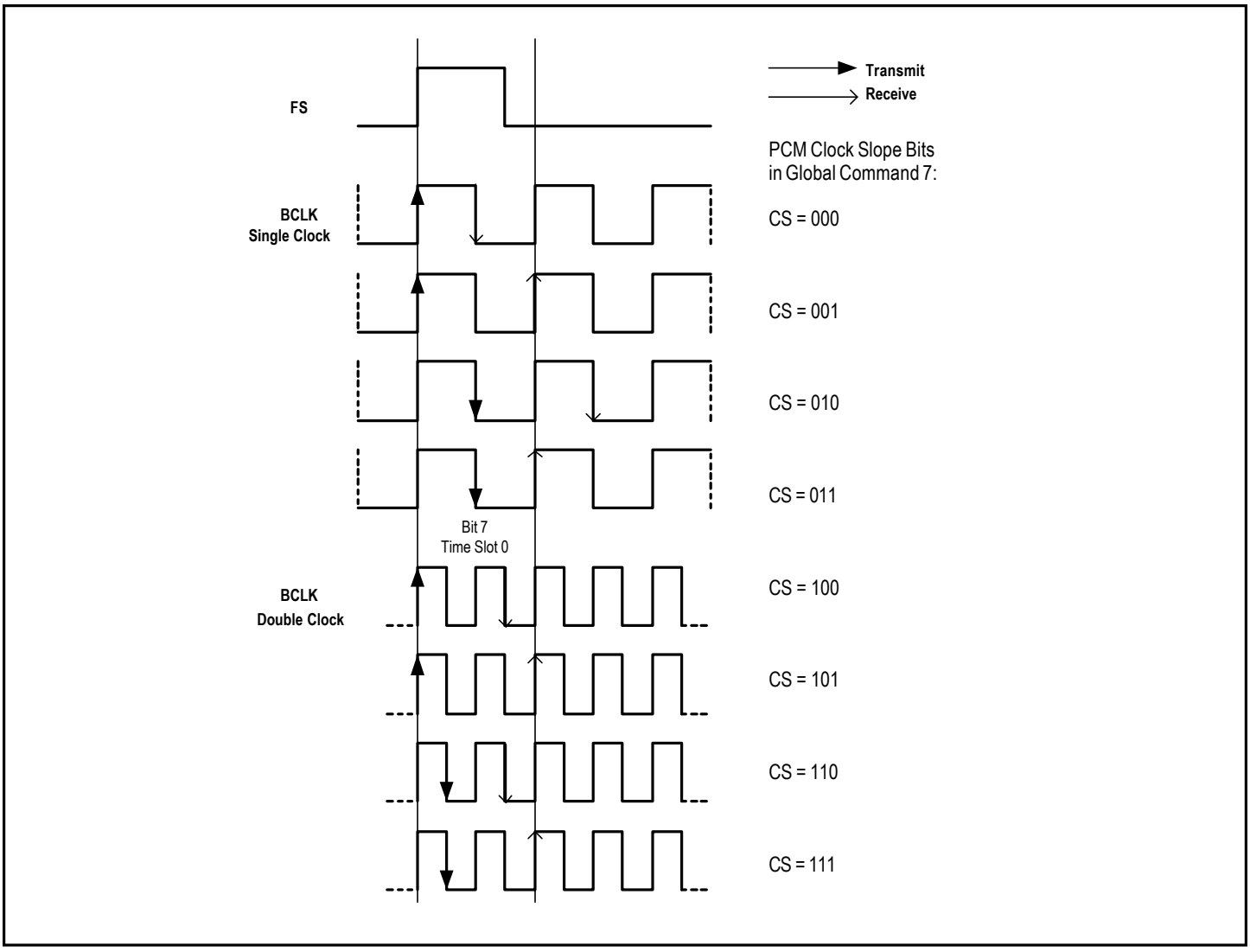


Figure 3. Sampling Edge Select Waveform

DSP PROGRAMMING

SIGNAL PROCESSING

Several blocks are programmable for signal processing. This allows users to optimize the performance of the IDT821054 for the system. Figure 4 shows the Signal Flow for each channel and indicate the programmable blocks.

The programmable digital filters are used to adjust gain and impedance, balance transhybrid and correct frequency response. All the coefficients of the digital filters can be calculated automatically by a software provided by IDT. Users should provide accurate SLIC model, impedance and gain requirements, then the software will calculate all the coefficients automatically. When these coefficients are written to the coefficient RAM of the IDT82V1054, the final AC characteristics of the line card (consists of SLIC and CODEC) will meet the ITU-T specifications.

GAIN ADJUSTMENT

The analog gain and digital gain of each channel can be adjusted separately in IDT821054.

For each individual channel, in transmit path, analog A/D gain can be selected as 0 dB or 6 dB. The selection is done by A/D Gain (GAD) bit in Local Command 9. The default analog gain for transmit path is 0 dB.

For each individual channel, in receive path, analog D/A gain can be selected as 0 dB or -6 dB. The selection is done by D/A Gain (GDA) bit in Local Command 9. The default analog gain for receive path is 0 dB.

Digital gain of transmit path (GTX) can be programmed from -3 dB to +12 dB with minimum 0.1 dB step. If CS[5] bit is '0' in Local Command 1, the digital gain in transmit path is set to be the default value. If CS[5] bit is '1' in Local Command 1, the digital gain in transmit path will be decided by the coefficient in GTX RAM.

Digital gain of receive path (GRX) can be programmed from -12 dB to +3 dB with minimum 0.1 dB step. If CS[7] bit is '0' in Local Command 1, the digital gain in receive path is set to be the default value. If CS[7] bit is '1' in Local Command 1, the digital gain in receive path will be decided by the coefficient in GRX RAM.

IMPEDANCE MATCHING

There is a programmable feedback path on each channel from VIN to VOUT in the IDT821054. It synthesizes the two-wire impedance of the SLIC. The Impedance Matching Filter (IMF) and the Gain of Impedance Scaling (GIS) are adjustable, they work together to realize impedance matching. If the CS[0] bit in Local Command 1 is '0', the IMF coefficient is set to be default value; if CS[0] is '1', the IMF coefficient is set by the IMF RAM. If the CS[2] bit in Local Command 1 is '0', the GIS coefficient is set to be default value; if CS[2] is '1', the GIS coefficient is set by the GIS RAM.

TRANSHYBRID BALANCE

Transhybrid balancing filter is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation (ECF) can be programmed. If the CS[1] bit in Local Command 1 is '0', the coefficient of ECF is set to be default value; if CS[1] is '1', the coefficient of ECF is decided by the ECF RAM.

FREQUENCY RESPONSE CORRECTION

The IDT821054 provides two filters that can be programmed to correct any frequency distortion caused by the impedance matching filter, they are: Frequency Response Correction for Transmit path (FRX) filter and Frequency Response Correction for Receive path (FRR) filter. The coefficients of FRX filter and FRR filter can be programmed. If the CS[4] bit in Local Command 1 is '0', the FRX coefficient is set to be default value, while if CS[4] is '1', the FRX coefficient is decided by the FRX RAM. If the CS[6] bit in Local Command is '0', the FRR coefficient is set to be default value, while if CS[6] is '1', the FRR coefficient is decided by the FRR RAM.

The address of the Coe-RAM including GTX, GRX, FRX, FRR, GIS, ECF and IMF RAM are listed in APPENDIX.

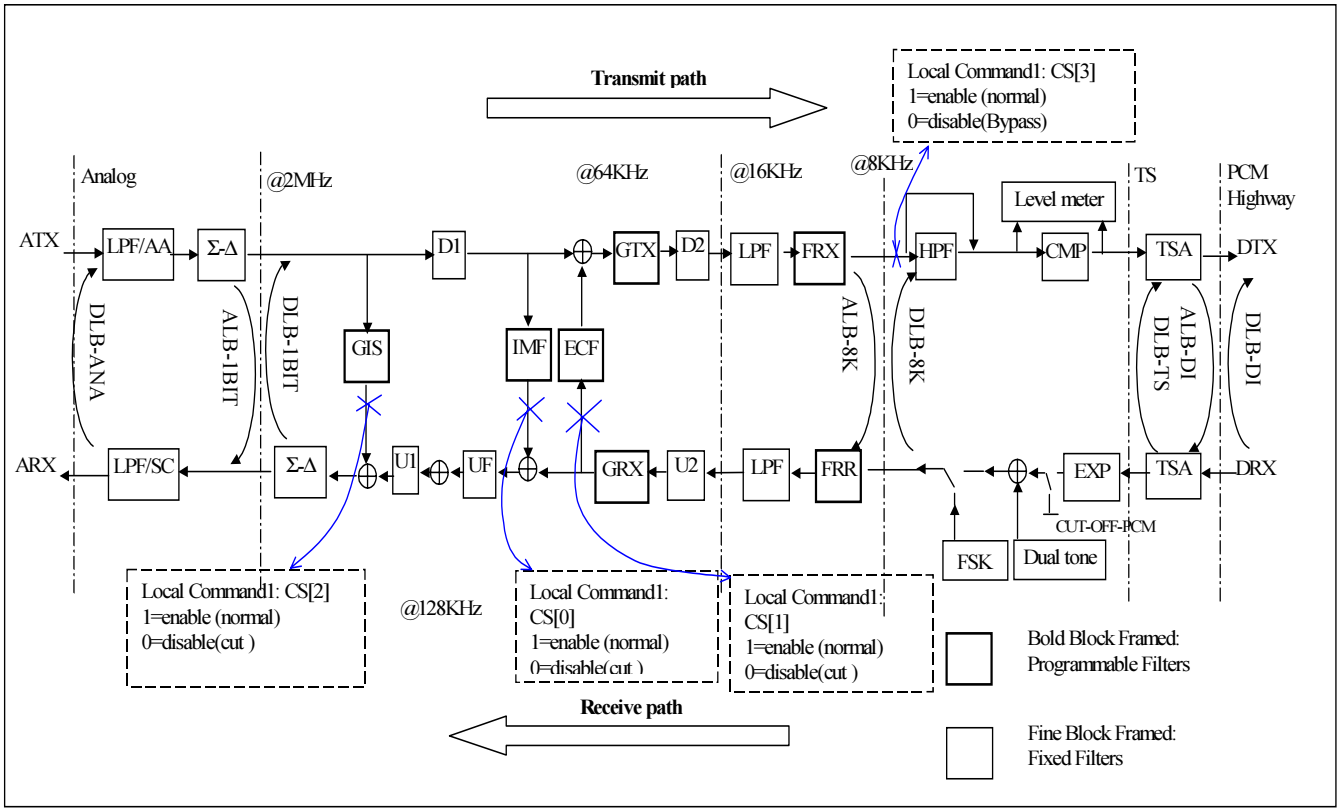


Figure 4. Signal Flow for Each Channel

Abbreviation List

LPF/AA: Anti-Alias Low-pass Filter
LPF/SC: Smoothing Low-pass Filter
LPF: Low-pass Filter
HPF: High-pass Filter
GIS: Gain for Impedance Scaling
D1: 1st Down Sample Stage
D2: 2nd Down Sample Stage
U1: 1st Up Sample Stage
U2: 2nd Up Sample Stage
UF: Up Sampling Filter (64k-128k)
IMF: Impedance Matching Filter
ECF: Echo Cancellation Filter
GTX: Gain for Transmit Path
GRX: Gain for Receive Path
FRX: Frequency Response Correction for Transmit
FRR: Frequency Response Correction for Receive
CMP: Compression
EXP: Expansion

SLIC CONTROL

The SLIC interface of IDT821054 for each channel consists of 7 pins: 2 inputs SI1 and SI2, 3 I/O pins SB1, SB2 and SB3, together with 2 outputs SO1 and SO2.

SI1 AND SI2

SLIC inputs SI1 and SI2 can be read in 2 ways - globally for all 4 channels, or locally for each individual channel.

SI1 and SI2 data of all 4 channels can be read by executing a read operation of Global Command 9. The SIA[3:0] bits of Global Command 9 represent the debounced SI1 signal of channel 4 to channel 1. The SIB[3:0] bits of Global Command 9 represent the debounced SI2 signal of channel 4 to channel 1.

Both SI1 and SI2 can be assigned to off-hook, ring trip, ground key signals or other signals. The Global Command 9 provides for users a more efficient way to obtain time-critical data such as on/off-hook and ring trip information from the SLIC inputs SI1 and SI2.

SI1 and SI2 data of each channel can also be read by Local Command 4, which provides SLIC information for the specific channel.

SB1, SB2 AND SB3

SLIC I/O pin SB1 for each channel can be configured as input or output separately, by Global Command 10. The SB1C[3:0] bits of this command correspond to the SB1 directions of channel 4 to channel 1: '0' means input and '1' means output. Similarly, the SB2C[3:0] bits of Global Command 11 determine the I/O direction of the SB2 pins for each channel, and the SB3C[3:0] bits of Global Command 12 determine the I/O direction of the SB3 pins for each channel.

When the SB1, SB2 or SB3 pin is selected as input, its information can be read by Global Command or Local Command. By executing a read operation of Global Command 10, 11 or 12, users can obtain information of SB1, SB2 or SB3 respectively. The SB1[3:0] bits in Global Command 10, the SB2[3:0] bits in Global Command 11 and the SB3[3:0] bits in Global Command 12 provide the SB1, SB2 and SB3 information respectively for all four channels. The information of SB1, SB2 and SB3 can also be read by Local Command 4, which provides information for the specific channel.

When the SB1 pin, the SB2 pin or the SB3 pin is configured as output, only Global Command 10, 11 or 12 can write data to the three pins respectively.

SO1 AND SO2

Signals on SO1 and SO2 pins can only be written on a per-channel basis.

Local Command 4 writes the 2 output pins for each channel. When Local Command 4 reads a channel's SLIC data, the SO1 and SO2 bits will be read out with the data written in at previous write operation.

HARDWARE RING TRIP

In order to prevent the damage caused by high voltage ring signal, the IDT821054 offers a hardware ring trip function to respond to the off-hook signal as fast as possible. This function can be enabled by setting RTE bit in Global Command 8.

The off-hook signal can be input via either SI1 or SI2, while the ring control signal can be output via any pin of SO1, SO2, SB1, SB2 and SB2 (when SB1-SB3 configured as output). In Global Command 8, IS bit determines which input is used and OS[2:0] bits determine which output is used.

When a valid off-hook signal arrives on SI1 or SI2, the IDT821054 will turn off the ring signal by inverting the selected output, regardless of the value in corresponding SLIC output control register (the content in the corresponding SLIC control register should be changed later). This function provides a much faster response to off-hook signal than the software ring trip which turns off the ring signal by changing the value of selected output in the corresponding register. The IPI bit in Global Command 8 is used to indicate the valid polarity of input. If the off-hook signal is active low, the IPI should be set to '0'; if the off-hook signal is active high, the IPI should be set to '1'.

The OPI bit in Global Command 8 is used to indicate the valid polarity of output. If the ring control signal is required to be low in normal status and be high to activate a ring, the OPI should be set to '1'; if it is required to be high in normal status and be low to activate a ring, the OPI should be set to '0'.

For example, in a system where the off-hook signal is active low and ring control signal is active high, the IPI in Global Command 8 should be set to '0' and the OPI bit should be set to '1'. In normal status, the selected input (off-hook signal) is high and the selected output (ring control signal) is low. When the ring is activated by setting the output (ring control signal) high, a low pulse appearing on the input (off-hook signal) will inform the device to invert the output to low and cut off the ring signal.

INTERRUPT AND INTERRUPT ENABLE

An interrupt mechanism is offered in IDT821054 for reading the SLIC input status. Each SLIC input generates interrupt respectively when it changes state.

Any of SI1, SI2, SB1, SB2 and SB3 (when SB1-SB3 are configured as inputs) can be interrupt source. As SI1 and SI2 are debounced signals while SB1, SB2 and SB3 are not, users should be careful if they select SB1 and SB2 as interrupt sources.

The IDT821054 provides an Interrupt Enable Command (Local Command 2) for each interrupt source to enable its interrupt ability. Local Command 2 contains 5 bits (IE[4:0]) for each channel. Each bit of the IE[4:0] corresponds to one interrupt source of the specific channel. The device will ignore the interrupt signal if its corresponding bit in Interrupt Enable Command is set to '0' (disable).

Multiple interrupt sources can be enabled at the same time, and they can be cleared at the same time by executing an Interrupt Clear Command (Global Command 2). Besides this, when Global Command 9 which is to read the SI data is executed, the interrupt source of both SIA and SIB for all four channels are cleared immediately. And if SB1, SB2 and SB3 are configured to be interrupt sources, a read operation of Global command 10, 11 and 12 will clear the interrupt on corresponding SB port for 4 channels. While the read operation of Local command 4 can clear all the 7 interrupt sources for the corresponding channel.

DEBOUNCE FILTERS

For each channel, IDT821054 provides two debounce filter circuits: Debounced Switch Hook (DSH) Filter for SI1 and Ground Key (GK) Filter for SI2 as shown in Figure 5. They are used to buffer the input signals on SI1 and SI2 pins before changing the state of the SLIC Debounced Input SI1/SI2 Register (Global Command 9). Frame Sync (FS) is necessary for both DSH filter and GK filter.

DSH Debounce bits in Local Command 3 can program the debounce time of SI1 input from SLIC on individual channel. The DSH filter is initially clocked at half of the frame sync rate (250 μs), and any data changing at this sample rate resets a programmable counter. The counter clocks at the

rate of 2 ms, and the count value can be varied from 0 to 30 which is determined by Local Command 3. The corresponding SIA bit in the SLIC Debounced Input SI1 Register (accessed by Global Command 9) would not be updated until the count value is reached. SI1 bit usually contains SLIC switch hook status.

GK Debounce bits in Local Command 3 can program the debounce time of SI2 input from SLIC on corresponding channel. The debounced signal will be output to SIB of SLIC Debounced Input SI2 Register (accessed by Global Command 9). The GK debounce filter consists of an up/down counter that ranges between 0 and 6. This six-state counter is clocked by the GK timer at the sampling period of 0-30 ms, as programmed by Local Command 3. When the sampled value is low, the counter is decremented by each clock pulse. When the sampled value is high, the counter is incremented by each clock pulse. When the counter increments to 6, it sets a latch whose output is routed to the corresponding SIB bit. If the counter decrements to 0, this latch is cleared and the output bit is set to 0. In other cases, the latch, the SIB status remains in their previous state without being changed. In this way, at least six consecutive GK clocks with the debounce input remaining at the same state to effect an output change.

CHOPPER CLOCK

IDT821054 offers two programmable chopper clock outputs: CHCLK1 and CHCLK2. Both CHCLK1 and CHCLK2 are synchronous to MCLK. CHCLK1 outputs signal with programmable 2-28 ms clock cycle, while the frequency of CHCLK2 can be any of 256 kHz, 512 kHz and 16.384 MHz. The frequency selection of chopper clocks can be implemented by Global Command 5. The chopper clocks can be used to drive the power supply switching regulators on SLICs.

DUAL TONE AND RING GENERATION

Each channel of IDT821054 has two tone generators, Tone 0 generator and Tone 1 generator, which can produce a gain-adjustable dual tone signal and output it to VOUT pin. The tone generators can be used to generate signals such as test tone, DTMF, dial tone, busy tone, congestion tone and Caller-ID Alerting Tone etc.

The Tone 0 generator and Tone 1 generator of each channel can be enabled or disabled independently by setting the TEN0 and TEN1 bits in Local Command 10.

The tone generator is user-programmable, the frequency and amplitude of the tone can be programmed by writing coefficient into the Coe-RAM. The frequency coefficient and amplitude coefficient can be calculated by the following formulas:

Frequency Coefficient $= 32767 * \cos(f/8000 * 2 * \pi)$

Amplitude Coefficient $= A * 32767 * \sin(f/8000 * 2 * \pi)$

Herein, 'f' is the desired frequency of the tone; 'A' is scaling parameter for the amplitude of the tone. The range of 'A' is from 0 to 1:

A = 1, corresponding to the maximum amplitude, 3.14 V;

A = 0, corresponding to minimum amplitude, 0V.

It's a linear relationship between 'A' and amplitude, which means if 'A' = β ($0 < \beta < 1$), then the amplitude will be $3.14 * \beta$ (V).

The Frequency range is from 25Hz to 3400Hz. The frequency tolerances are as the following:

25Hz < f < 40Hz, tolerance< $\pm 12\%$

40Hz < f < 60Hz, tolerance< $\pm 5\%$

60Hz < f < 100Hz, tolerance< $\pm 2.5\%$

100Hz < f < 3400Hz, tolerance< $\pm 1\%$

The Frequency Coefficient and Amplitude Coefficient should be converted to corresponding hexadecimal value before being written into the Coe-RAM. Refer to Appendix for address of Tone-RAM.

Ring signal is a special signal generated by the dual tone generators. When only one tone generator is enabled or both tone generators produce the same tone, and frequency of the tone is set as ring signal required (10 Hz to 100 Hz), the VOUT pin will output the Ring signal.

FSK SIGNAL GENERATION

The IDT821054 provides a FSK signal generator to send Caller-ID messages. Generally, the procedure of sending Caller-ID messages by FSK codes is as the following:

Step 1: Start, Send Seizure Signal;

Step 2: Send Mark Signal;

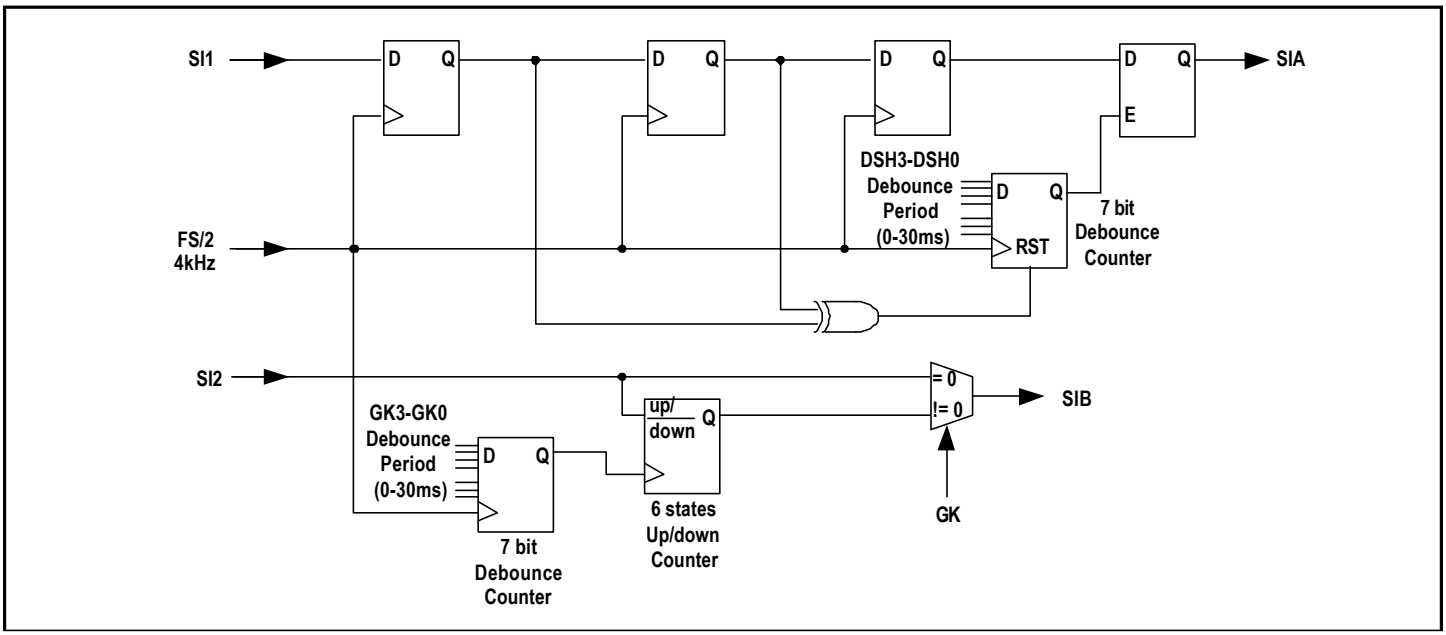


Figure 5. Debounce Filters

Step 3: Send one byte Caller-ID message, then send Flag Signal;
Step 4: If the messages to be sent are finished, stop;
otherwise, return to step 3.

Herein, the Seizure Signal is a string of '01' pairs to inform telephone set that Caller-ID message will come; the Mark Signal is a string of '1', which follows the Seizure Signal to inform telephone set that Caller-ID message is coming; while the Flag Signal is a string of '1' sending between two bytes of Caller-ID message, with this the telephone set can have enough time to process the received byte.

According to the generic procedure of FSK signal sending, a recommended programming flow chart for IDT821054 FSK generator is shown in the following page.

To make it easy for users to understand the flow chart, several notes is given below:

1. The FSK function block will be enabled when FSK On/Off bit (FO) in Global Command 17 is set to '1'. After finishing sending the FSK signal, the FO bit should be set to '0' to disable the generation function.

2. The FSK Start bit (FS) in Global Command 17 is used to indicate the start of the FSK signal generation, when FS is '0' which means the function block is idle, users can go on with the operation; when FS is '1' which means FSK generator is busy, users should wait until it turns to '0' (after the message data in the FSK-RAM having been sent, the FS bit will be cleared to '0' automatically).

3. The length of the Seizure Signal, Mark Signal and Flag Signal are different in different system, for IDT821054, they can be programmed by Global Command 15, 16 and 13 respectively. It should be noted that, the Seizure Length is two times of the value that set in Global Command 15, for example, if the SL[7:0] bits of Global Command 15 is 1(d), it means that the Seizure Length is 2(d).

4. As is described in "Addressing of FSK-RAM", the FSK-RAM consists of 32 words, and each word consists of 16 bits (2 bytes), so it can contain up to 64 bytes of message at one time. If the message data is longer than 64 bytes, users should write them into the FSK-RAM two or more times according to the length of the message.

5. The "Data length" is the number of data bytes written in the FSK-RAM and needed to be sent out. During the transmission of FSK signal, an internal counter will count the number of data bytes that have been transmitted, once it reaches the Data length, the FSK transmission is completed and the FS bit is set to '0'.

6. Because there is only one FSK-RAM shared by four channels of the channel selection is done by the FCS[2:0] bits of Global Command 17.

7. The FSK signal generated by the IDT821054 follows the BELL 202 and CCITT V.23 specifications. Users can select BT or Bellcore standard by setting the BT/Bellcore Select bit (BS) in Global Command 17. The difference between BT and Bellcore is shown in Table 1.

8. The "Mark After Send" bit (MAS) is useful if the total message data is longer than 64 bytes. If the MAS is set to '1', then after sending one frame of FSK-RAM message(=< 64 bytes), IDT821054 will keep sending a series of '1' to hold the communication channel for sending next frame of FSK message, and at the same time, users can update the FSK-RAM with new data. This series of '1' will stop by set the MAS bit to '0' or set the FO bit to '0'.

9. It should be noted that, when write/read message data to/from the FSK-RAM via serial microprocessor interface, the sequence of read/write is MSB first; but the FSK generator will send these signal (message data) out through channel port with LSB first.

Refer to the IDT821054 Application Note for more information.

Table 1 - BT/Bellcore Standard of FSK Signal

Item	BT	Bellcore
Mark(1) frequency	1300 Hz ± 1.5%	1200Hz ± 1.1%
Space (0) frequency	2100 Hz ± 1.1%	2200 Hz ± 1.1%
Transmission rate	1200 baud ± 1%	1200 baud ± 1 %
Word format	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'	1 start bit which is '0' 8 word bits (with least significant bit LSB first) 1 stop bit which is '1'

LEVEL METERING

The IDT821054 has a level meter which can be shared by all 4 signal channels. The level meter is designed to emulate the off-chip PCM test equipment so as to facilitate the line-card, subscriber line and users telephone set monitoring. The level meter tests the returned signal and reports the measurement result via MPI interface. When combined with Tone Generation and Loopback modes, this allows the microprocessor to test channel integrity. CS[1:0] bits in Global Command 21 select the channel, signal on which will be metered.

Level Metering function is enabled by setting LMO bit to '1' in Global Command 21. There is a Level Meter Counter register for this function. It can be accessed by Global Command 20. This register is used to configure the number of time cycles for sampling PCM data (8 kHz sampling rate). The output of Level Meter will be sent to Level Meter Result Low and Level Meter Result High registers (Global Command 18 and 19). The LVLL register contains the lower 7 bits of the output and a data-ready bit (LVLL[0]), while the LVLH register contains the higher 8 bits of the output. An internal accumulator sums the rectified samples until the number configured by Level Meter Counter register is reached. By then, the LVLL[0] bit is set to '1' and accumulation result is latched into the LVLL and LVLH registers simultaneously.

Once the LVLH register is read, the LVLL[0] bit will be reset. The LVLL[0] bit will be set high again by a new data available. The contents in LVLL and LVLH will be overwritten by later metering result if they are not read out yet. In Level Metering result read operation, it is highly recommended to read LVLL first.

L/C bit in Global Command 21 determines the mode of Level Meter operation. When L/C bit is '0', the Level Meter will measure the linear PCM data, and if LVLL[0] bit is '1' , the measure result will be output to LVLH and LVLL. When L/C bit is '1', compressed PCM will be output transparently to LVLH.

The calculation and method of level metering will be described in the Application Note.

CHANNEL POWER DOWN/STANDBY MODE

Each individual channel of IDT821054 can be powered down independently by Local Command 9. When the channel is powered down (enters into standby mode), The transmission and reception of PCM data, D/A and A/D converters are disabled. In this way, power consumption of the device can be reduced. When IDT821054 is powered up or reset, all

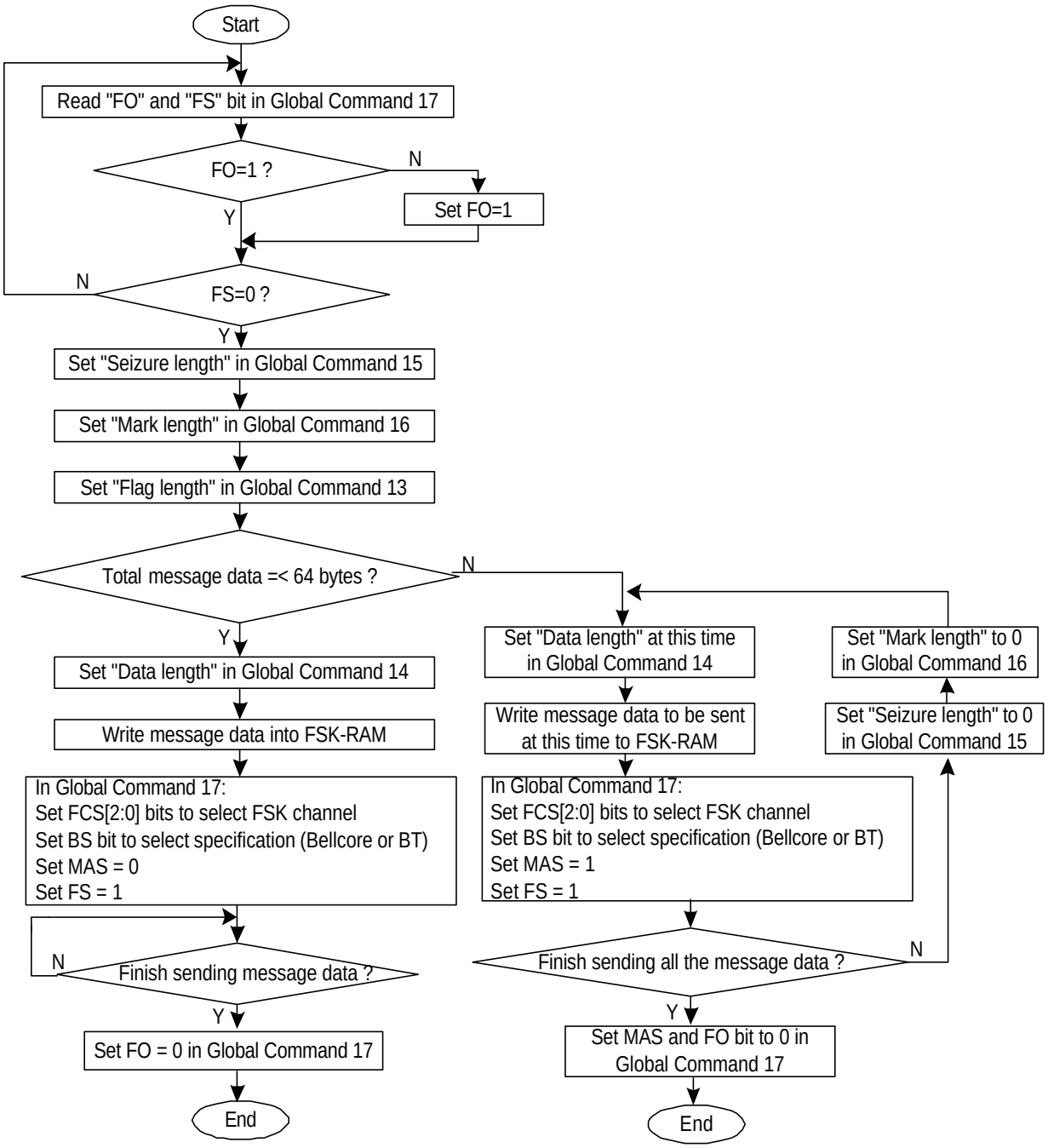


Figure 6. A Recommended Programming Flow Chart for FSK Generator

four channels will be powered down. All circuits that contain programmed information retain their data when powered down. MPI (Microprocessor Interface) is always active so that new command could be received and executed.

POWER DOWN/SUSPEND MODE

A suspend mode is offered to the whole chip to save power. In this mode, the PLL block is turned off and DSP operation is disabled. This mode saves much more power consumption than standby mode. In this mode, only Global Command and Local Command can be executed. RAM operation is disabled as internal clock has been turned off. The PLL blocks can be powered down by Global Command 22. Suspend mode can be entered by powering down PLL and all channels.

OPERATING THE IDT821054

PROGRAMMING DESCRIPTION

The programming of IDT821054 can be easily realized by writing commands to registers or RAMs on the chip via the CI pin and reading data back via the CO pin.

A Channel Program Enable command (Global Command 6) is provided by IDT821054 to facilitate the addressing of individual or multiple channels. Each bit of the higher four bits of this command (CE[0] to CE[3]) is assigned to one specific channel. The channel or channels are enabled when their corresponding bits are set high. If two or more bits, or all of the bits of CE[3:0] are high, all the channels enabled will be addressed. Therefore, a Broadcast mode can be implemented by simply enable all the channels in the device before performing other write-operation. The Broadcast mode is very useful in initializing IDT821054 such as coefficient setting in a large system. But in read operation, multiple addressing is not allowed.

IDT821054 provides an Identification Code to distinguish itself from other device of the system. When being read, IDT821054 outputs an Identification Code of 81H before data bytes, which indicate that the following data is from IDT821054.

COMMAND TYPE AND COMMAND FORMAT

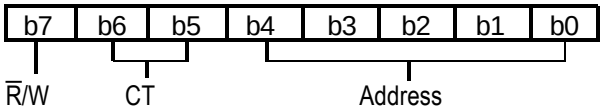
IDT821054 provides three types of register/RAM commands, they are:

Local Command (LC), which is used to configure each channel by reading/writing the Local Registers, there are 10 Local Registers per channel available;

Global Command (GC), which is used to configure all 4 channels by reading/writing the Global Registers, there are totally 22 Global Registers shared by four channels;

RAM Command (RC), which is used to read/write Coe-RAM and FSK-RAM, there are 40 words (divided into 5 blocks) with 14 bits per word Coe-RAM for each channel, and 32 words (divided into 4 blocks) with 16 bits per word FSK-RAM shared by four channels. When a RC is executed, 8 words of RAM (14 or 16 bits/word) will be accessed.

The format of register/RAM command is as the following:



$\overline{R}$/W : Read/Write Command bit.
- b7 = 0: Read Command
- b7 = 1: Write Command

CT : Command Type
- b6 b5 = 00: LC - Local Command
- b6 b5 = 01: GC - Global Command
- b6 b5 = 10: Not Allowed
- b6 b5 = 11: RC - RAM Command

Address: Specify which register or which block of RAM will be read or written.

For both Local Command and Global Command, b[4:0] are used to address the Local Registers or Global Registers.

For RAM Command, b4 is used to distinguish the Coe-RAM and the FSK RAM:
- b4 = 0: The RAM Command is for Coe-RAM
- b4 = 1: The RAM Command is for FSK-RAM

When the RAM Command is for Coe-RAM, b[3:0] are used to address the blocks in the Coe-RAM. When the RAM Command is for FSK-RAM, b3 is always '0' and b[2:0] are used to address the blocks in the FSK-RAM.

ADDRESSING LOCAL REGISTER

When using Local Command, the Channel Enable Command (Global Command 6) must be used first to specify which channel will be addressed, then the Local Command follows. If Global Command 6 enable more than one channel, then all the channels enabled will be addressed by one Local Command at one time.

The b[4:0] of a Local Command determine which one of the 10 Local Registers will be addressed for the configured channel.

IDT821054 provides a Consecutive Adjacent Addressing for Read/Write Local Registers. If the address for Local Register is specified in a Local Command, then, according to the value of 'b1b0' of the address, there will be 1 to 4 adjacent local registers will be read/write automatically with the highest order first. For example, if the address of the register specified by the Local Command is end with '11' (b1b0='11'), 4 adjacent registers will be Read/Write by this Command. If b1b0 ='10', then 3 adjacent registers will be Read/Write. If b1b0 = '01', then only 2 adjacent registers will be Read/Write. If b1b0 = '00', then only this specified register will be Read/Write. The details of the Consecutive Adjacent Addressing is shown in the following table.

Table 2 - Consecutive Adjacent Addressing

Address Specified by Local Command	In/Out Data	Registers being $\overline{R}$/W
b4 b3 b2 b1 b0		
X X X 1 1	Byte 1	X X X 11
(b1b0 = 11, 4 bytes DATA)	Byte 2	X X X 10
	Byte 3	X X X 01
	Byte 4	X X X 00
X X X 1 0	Byte 1	X X X 10
(b1b0 = 10, 3 bytes DATA)	Byte 2	X X X 01
	Byte 3	X X X 00
X X X 0 1	Byte 1	X X X 01
(b1b0 = 01, 2 bytes DATA)	Byte 2	X X X 00
X X X 0 0	Byte 1	X X X 00
(b1b0 = 00, 1 byte DATA)		

When addressing Local Registers, the procedure of Consecutive Adjacent Addressing can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ changes from low to high, the operation of the current register and the next adjacent registers will be aborted. However, it does not affect those results in the previous operation.

ADDRESSING GLOBAL REGISTER

The address of the 22 Global Registers is : 00000 - 10101

For the adjacent 22 Global Registers, IDT821054 also provides a Consecutive Adjacent Addressing for Read/Write operation, as it does for Local Registers. The procedure of Consecutive Adjacent Addressing can be stopped by $\overline{CS}$ signal at any time.

ADDRESSING COE-RAM

IDT821054 provides 40 words of Coe-RAM for per channel. They are divided into 5 blocks, each block contains 8 words. The 5 blocks are:
- IMF RAM (Word 0 - Word 7), for Impedance Matching Filter coefficient;
- ECF RAM (Word 8 - Word 15), for Echo Cancellation Filter coefficient;

- GIS RAM (Word 16 - Word 19) and Tone Generator RAM (Word 20 - Word 23), for Gain of Impedance Scaling and amplitude or frequency coefficient for Tone Generator;

- FRX RAM (Word 24 - Word 30) and GTX RAM (Word 31), for coefficient of Frequency Response Correction in Transmit Path and Gain in Transmit Path;

- FRR RAM (Word 32 - Word 38) and GRX RAM (Word 39), for coefficient of Frequency Response Correction in Receive Path and Gain in Receive Path.

Refer to APPENDIX (Coe-RAM Mapping) for information about Coe-RAM address.

Each word in the Coe-RAM is 14-bit (b[13:0]) wide. To write a Coe-RAM word, 16 bits (b[15:0]) (or, two 8-bit bytes) are needed to fulfill with MSB first, but the lowest two bits (b[1:0]) will be ignored. When read, each Coe-RAM word will output 16 bits with MSB first, but the last two bits (b[1:0]) are meaningless.

When addressing Coe-RAM, Global Command 6 (Channel Enable) must be used first to specify the channel(s), then the address (b[2:0]) in the followed RAM Command indicates which block of the Coe-RAM for the channel(s) will be addressed.

When the address of a Coe-RAM block is specified in a RAM Command, all 8 words in this block will be Read/Write automatically, with the highest order word first.

When addressing Coe-RAM, the procedure of Consecutive Adjacent Addressing can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ changes from low to high, the operation of the current RAM word and the next adjacent RAM words will be aborted. However, it does not affect those results in the previous operation.

ADDRESSING FSK-RAM

The FSK-RAM is consisted of 4 blocks, each block has eight 16-bit words. The total 32 words of FSK-RAM are shared by four channels, only one channel can used it at one time.

To write a FSK-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill with MSB first. When being read, each FSK-RAM word in FSK-RAM will output 16 bits with MSB first.

Only b[2:0] of a FSK-RAM Command are needed to address the 4 blocks in FSK-RAM, b3 should be always '0', and b4 is always '1' to indicate the address is for FSK-RAM.

When the address of a FSK-RAM block is specified in a FSK-RAM Command, all 8 words in the block will be Read/Write automatically, with the highest order word first.

EXAMPLES OF IDT821054 COMMANDS

1. An example of Local Command write and read (byte transmission sequence):

Table 3 - Local Command Transmission Sequence

Data Transmitted On CI Pin	Data Received on CO Pin
Global Command 6 (Channel Program Enable byte) Local Command byte, Write Data byte 1 . . . Data byte m*	
Global Command 6 (Channel Program Enable byte) Local Command byte, Read	
	Identification Code (81H) Data byte 1 . . . Data byte m*

2. An example of Global Command write and read (byte transmission sequence):

Table 4 - Global Command Transmission Sequence

Data Transmitted On CI Pin	Data Received on CO Pin
Global Command byte, Write Data byte 1 . . . Data byte m*	
Global Command byte, Read	
	Identification Code (81H) Data byte 1 . . . Data byte m*

3. An example of Coe-RAM Command write and read (byte transmission sequence):

Table 5 - Coe-RAM Command Transmission Sequence

Data Transmitted On CI Pin	Data Received on CO Pin
Global Command 6 (Channel Program Enable byte) Coe-RAM Command byte, Write Data word 1 (Data_H, Data_L**) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L)	
Global Command 6 (Channel Program Enable byte) Coe-RAM Command byte, Read	
	Identification Code (81H) Data word 1 (Data_H, Data_L **) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L)

4. An example of FSK-RAM Command write and read (byte transmission sequence):

Table 6 - FSK-RAM Command Transmission Sequence

Data Transmitted On CI Pin	Data Received on CO Pin
FSK-RAM Command byte, Write Data word 1 (Data_H, Data_L**) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L)	
FSK-RAM Command byte, Read	
	Identification Code (81H) Data word 1 (Data_H, Data_L **) Data word 2 (Data_H, Data_L) . . . Data word 8 (Data_H, Data_L)

Notes:

* The number of the data bytes can be 1 to 4 depending on the two bits 'b1b0' of the Local/Global Command.

** When addressing the Coe-RAM, the data word is 14-bit wide, the lowest two bits in Data_L of each word are ignored; When addressing the FSK-RAM, the data word is 16-bit wide.

POWER-ON SEQUENCE

To power on IDT821054, users should follow this sequence:

1. Apply ground first;
2. Apply VCC, finish signal connections and set $\overline{\text{RESET}}$ low, thus the device goes into default state;
3. Set $\overline{\text{RESET}}$ high;
4. Select master clock frequency;
5. Program filter coefficients and other parameters as required;

DEFAULT STATE AFTER RESET

When the IDT821054 is powered on, or reset either by $\overline{\text{RESET}}$ pin or by command, the device defaults to the following state:

1. All four channels are powered down and in standby mode;
2. All loopbacks and cutoff are disabled;
3. DX1 pin is selected for all channels to transmit data, DR1 pin is selected for all channels to receive data;
4. The master clock frequency is 2.048 MHz;
5. Transmit and receive time slots are set to be 0-3 respectively for channel 1-4. The PCM data rate is the same as Bit Clock frequency. Data is transmitted on rising edges and received on falling edges;
6. A-Law is selected;
7. Coefficients of GRX, FRR, GTX, FRX, GIS, ECF and IMF are set to be default values. High-Pass Filters are disabled. Refer to Figure 4 and Local Command 1 for details.
8. SB1, SB2 and SB3 are configured as inputs;
9. SI1 and SI2 are configured as no debounce;
10. All interrupts are disabled, all pending interrupts are cleared;
11. All feature function blocks including FSK, Dual Tone, Ring Trip and Level Metering are turned off;
12. CHCLK1 and CHCLK2 are set to be high.

The data stored in RAM will not be changed or lost by any kind of resets. In this way, the RAM data will not lost unless the device is powered down physically.

COMMANDS LIST

Notes: 1. $\overline{R}$/W = 0: Read; $\overline{R}$/W = 1: Write
2. *R* means Reserved for future use. This bit will always be filled in ' 0 ' in Write-Command, and be ignored in Read-command.

GLOBAL COMMANDS:

1. No Operation (A0H) / Version Number (20H), Write/Read

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	0	0	0
I/O Data	0	0	0	0	0	0	0	1

By executing this read-command (20H), users can read out the version number of the IDT821054. The default value is 01H.
When executing the no operation command (A0H), a data byte (FFH) must follow to ensure proper operation.

2. Interrupt Clear (A1H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	0	1

All interrupts on SLIC I/O will be cleared by this command. When executing this command, a data byte (FFH) must follow to ensure proper operation.

3. Software Reset (A2H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	0

This command resets all Local Registers, but doesn't reset Global Registers and RAMs. When executing this command, a data byte (FFH) must follow to ensure proper operation.

4. Hardware Reset (A3H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	1

The action of this command is equivalent to pulling the $\overline{RESET}$ pin low (Refer to page 16 for information about $\overline{RESET}$ operation). When executing this command, a data byte (FFH) must follow to ensure proper operation.

5. Chopper Clock Select (24H/A4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	0
I/O data	*R*	*R*	CHclk2 [1]	CHclk2 [0]	CHclk1 [3]	CHclk1 [2]	CHclk1 [1]	CHclk1 [0]

This command is used to determine the CHclk2 and CHclk1 output signals, the frequency is shown below:

CHclk2[1:0]=00: chclk2 outputs 1 permanently (default);
CHclk2[1:0]=01: chclk2 outputs digital signal at the frequency of 512 kHz;
CHclk2[1:0]=10: chclk2 outputs digital signal at the frequency of 256 kHz;
CHclk2[1:0]=11: chclk2 outputs digital signal at the frequency of 16384 kHz;
CHclk1[3:0]=0000: chclk1 outputs 1 permanently (default);
CHclk1[3:0]=0001: chclk1 outputs digital signal at the frequency of 1000/2 Hz;
CHclk1[3:0]=0010: chclk1 outputs digital signal at the frequency of 1000/4 Hz;
CHclk1[3:0]=0011: at the frequency of 1000/6 Hz;
CHclk1[3:0]=0100: at the frequency of 1000/8 Hz;
CHclk1[3:0]=0101: at the frequency of 1000/10 Hz;
CHclk1[3:0]=0110: at the frequency of 1000/12 Hz;
CHclk1[3:0]=0111: at the frequency of 1000/14 Hz;
CHclk1[3:0]=1000: at the frequency of 1000/16 Hz;
CHclk1[3:0]=1001: at the frequency of 1000/18 Hz;
CHclk1[3:0]=1010: at the frequency of 1000/20 Hz;
CHclk1[3:0]=1011: at the frequency of 1000/22 Hz;
CHclk1[3:0]=1100: at the frequency of 1000/24 Hz;
CHclk1[3:0]=1101: at the frequency of 1000/26 Hz;
CHclk1[3:0]=1110: at the frequency of 1000/28 Hz;
CHclk1[3:0]=1111: chclk1 outputs 0 permanently.

6. MCLK Selection and Channel Program Enable (25H/A5), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	0	1	0	1
I/O data	CE[3]	CE[2]	CE[1]	CE[0]	Sel[3]	Sel[2]	Sel[1]	Sel[0]

The higher 4 bits of this command (CE[3:0]) are used to specify channel(s) before a Local Command or a Coe-RAM Command is executed. CE[0], CE[1], CE[2] and CE[3] indicate the program enable state of channel 1, channel 2, channel 3 and channel 4 respectively.

CE[0]=0: Disabled, Channel 1 can't receive programming commands (default);
CE[0]=1: Enabled, Channel 1 can receive programming commands;
CE[1]=0: Disabled, Channel 2 can't receive programming commands (default);
CE[1]=1: Enabled, Channel 2 can receive programming commands;
CE[2]=0: Disabled, Channel 3 can't receive programming commands (default);
CE[2]=1: Enabled, Channel 3 can receive programming commands;
CE[3]=0: Disabled, Channel 4 can't receive programming commands (default);
CE[3]=1: Enabled, Channel 4 can receive programming commands.

The lower 4 bits of this command (Sel[3:0] are used to determine the frequency of the Master Clock:

Sel[3:0]=0000: 8.192MHz
Sel[3:0]=0001: 4.096MHz
Sel[3:0]=0010: 2.048MHz (default)
Sel[3:0]=0110: 1.536MHz
Sel[3:0]=1110: 1.544MHz
Sel[3:0]=0101: 3.072MHz
Sel[3:0]=1101: 3.088MHz
Sel[3:0]=0100: 6.144MHz
Sel[3:0]=1100: 6.176MHz

7. A/μ-law, Linear/Compressed code, Clock slope and Delay time select (26H/A6), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	0	1	1	0
I/O data	A-μ	VDS	CS[2]	CS[1]	CS[0]	OC[2]	OC[1]	OC[0]

A/μ-law select bit (A-μ) selects the companding law:

A-μ = 0: A-law is selected (default)
A-μ = 1: μ-law is selected.

Voice Data select bit (VDS) defines the format of the voice data:

VDS = 0: Compressed code (default)
VDS = 1: Linear code

Clock slope (CS[2:0]) selects single or double clock and clock edges of transmitting and receiving data:

CS[2] = 0: Single clock (default)
CS[2] = 1: Double clock
CS[1:0]=00: transmits data on rising edges of BCLK, receives data on falling edges of it
CS[1:0]=01: transmits data on rising edges of BCLK, receives data on rising edges of it
CS[1:0]=10: transmits data on falling edges of BCLK, receives data on falling edges of it
CS[1:0]=11: transmits data on falling edges of BCLK, receives data on rising edges of it

PCM data Offset Configuration bits (OC[2:0]) determine the number of clocks that PCM data transmit and receive time slot is offset from FS signal:

OC[2:0] = 000: 0 BCLK period (default);
OC[2:0] = 001: 1 BCLK period;
OC[2:0] = 010: 2 BCLK periods;
OC[2:0] = 011: 3 BCLK periods;
OC[2:0] = 100: 4 BCLK periods;
OC[2:0] = 101: 5 BCLK periods;
OC[2:0] = 110: 6 BCLK periods;
OC[2:0] = 111: 7 BCLK periods.

8. SLIC Ring Trip Setting and Control (27H/A7H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	0	1	1	1
I/O data	OPI	*R*	IPI	IS	RTE	OS[2]	OS[1]	OS[0]

Output Polarity Indicator bit (OPI) indicates the valid polarity of output:

OPI=0: the selected output pin changes from low to high to activate the ring (default);

OPI=1: the selected output pin changes from high to low to activate the ring.

Input Polarity Indicator bit (IPI) indicates the valid polarity of input:

IPI=0: active low default); IPI=1: active high.

Input Selection bit (IS) determines which input will be selected as the off-hook indication signal source.

IS = 0: SI1 is selected (default); IS = 1: SI2 is selected.

Ring Trip Enable bit (RTE) enables or disables the ring trip function block:

RTE = 0: the ring trip function block is disabled (default);

RTE = 1: the ring trip function block is enabled.

Output Selection bits (OS[2:0]) determine which output will be selected as the ring control signal source.

OS[2:0] = 000 - 010: not defined;

OS[2:0] = 011: SB1 is selected (when it's configured as an output);

OS[2:0] = 100: SB2 is selected (when it's configured as an output);

OS[2:0] = 101: SB3 is selected (when it's configured as an output);

OS[2:0] = 110: SO1 is selected;

OS[2:0] = 111: SO2 is selected.

9. Read SI Data (28H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	0
I/O data	SIB[3]	SIB[2]	SIB[1]	SIB[0]	SIA[3]	SIA[2]	SIA[1]	SIA[0]

SIA bits contain SLIC status which SLIC Interface Pin SI1 receives. The value of SIA [0], SIA[1], SIA[2] and SIA[3] represent the debounced data on Channel 1, channel 2, channel 3 and channel 4 respectively.

SIB bits contain SLIC ground key status which SLIC Interface Pin SI2 receives. The value of SIB [0], SIB[1], SIB[2] and SIB[3] represent the debounced data on Channel 1, channel 2, channel 3 and channel 4 respectively.

10. SB1 Direction Control, SB1 Data (29H/A9H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	0	1
I/O data	SB1C[3]	SB1C[2]	SB1C[1]	SB1C[0]	SB1[3]	SB1[2]	SB1[1]	SB1[0]

SLIC SB1 direction control bits (SB1C[3:0]) configure the direction of SLIC bidirectional interface pin SB1.

SB1C[0]=0: SB1 pin of channel 1 is configured as input (default);

SB1C[0]=1: SB1 pin of channel 1 is configured as output;

SB1C[1]=0: SB1 pin of channel 2 is configured as input (default);

SB1C[1]=1: SB1 pin of channel 2 is configured as output;

SB1C[2]=0: SB1 pin of channel 3 is configured as input (default);

SB1C[2]=1: SB1 pin of channel 3 is configured as output;

SB1C[3]=0: SB1 pin of channel 4 is configured as input (default);

SB1C[3]=1: SB1 pin of channel 4 is configured as output.

SB1[3:0] bits contain the information of SLIC bidirectional pin SB1. The SB1[0], SB1[1], SB1[2] and SB1[3] contain the SB1 data of channel 1, channel 2, channel 3 and channel 4 respectively.

11. SB2 Direction Control, SB2 Data (2AH/AAH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	1	0
I/O data	SB2C[3]	SB2C[2]	SB2C[1]	SB2C[0]	SB2[3]	SB2[2]	SB2[1]	SB2[0]

SLIC SB2 direction control bits (SB2C[3:0]) configure the direction of SLIC bidirectional interface pin SB2.

SB2C[0]=0: SB2 pin of channel 1 is configured as input (default);

SB2C[0]=1: SB2 pin of channel 1 is configured as output;

SB2C[1]=0: SB2 pin of channel 2 is configured as input (default);

SB2C[1]=1: SB2 pin of channel 2 is configured as output;

SB2C[2]=0: SB2 pin of channel 3 is configured as input (default);

SB2C[2]=1: SB2 pin of channel 3 is configured as output;

SB2C[3]=0: SB2 pin of channel 4 is configured as input (default);

SB2C[3]=1: SB2 pin of channel 4 is configured as output.

SB2[3:0] bits contain the information of SLIC bidirectional pin SB2. The SB2[0], SB2[1], SB2[2] and SB2[3] contain the SB2 data of channel 1, channel 2, channel 3 and channel 4 respectively.

12. SB3 Direction Control, SB3 Data (2BH/ABH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	1	1
I/O data	SB3C[3]	SB3C[2]	SB3C[1]	SB3C[0]	SB3[3]	SB3[2]	SB3[1]	SB3[0]

SLIC SB3 direction control bits (SB3C[3:0]) configure the direction of SLIC bidirectional interface pin SB3.

SB3C[0]=0: SB3 pin of channel 1 is configured as input (default);
SB3C[0]=1: SB3 pin of channel 1 is configured as output;
SB3C[1]=0: SB3 pin of channel 2 is configured as input (default);
SB3C[1]=1: SB3 pin of channel 2 is configured as output;
SB3C[2]=0: SB3 pin of channel 3 is configured as input (default);
SB3C[2]=1: SB3 pin of channel 3 is configured as output;
SB3C[3]=0: SB3 pin of channel 4 is configured as input (default);
SB3C[3]=1: SB3 pin of channel 4 is configured as output.

SB3[3:0] bits contain the information of SLIC bidirectional pin SB3. The SB3[0], SB3[1], SB3[2] and SB3[3] contain the SB3 data of channel 1, channel 2, channel 3 and channel 4 respectively.

13. FSK Flag Length (2CH/ACH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	0	0
I/O data	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]

Flag Length bits (FL[7:0]) determine the number of flag bits '1' which will be transmitted between the transmission of message bytes. The value is valid from 0 to 255(d). The default value is 0(d). If 0(d) is selected, no flag signal will be sent.

14. FSK Data Length (2DH/ADH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	0	1
I/O data	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]	WL[1]	WL[0]

Data Length bits (WL[7:0]) determine the number of all the data bits which will be transmitted except flag. The value is valid from 0 to 64(d). Any value larger than 64(d) will be taken as 64(d) by the CPU.

The default value of this register is 0(d). When 0(d) is selected, none of the word data will be sent out. When Mark After Send (MAS bit in Global Command 17) is set to '1', the mark signal will be sent; while Mark After Send is set to '0', the transmission of mark signal will be terminated.

15. FSK Seizure Length (2EH/AEH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	1	0
I/O data	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]

Seizure Length bits (SL[7:0]) determine the number of '01' pairs which represent seizure phase(Seizure Length is two times of the value in SL[7:0], which is valid from 0 to 255(d), corresponding to Seizure Length 0 to 510). The default value is 0(d). When 0(d) is selected, no seizure signal will be sent.

16. FSK Mark Length (2FH/AFH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	1	1
I/O data	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]

Mark Length bits (ML[7:0]) determine the number of mark bits '1' which will be transmitted in initial flag phase. The value is valid from 0 to 255(d). The default value is 0(d). When 0(d) is selected, no mark signal will be sent.

17. FSK Start, Mark After Send, BT/Bellcore Select, FSK Channel Select and FSK On/Off (30H/B0H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	0	0	0
I/O data	*R*	*R*	FCS[1]	FCS[0]	FO	BS	MAS	FS

FSK Channel Select bits (FCS[1:0]) selects the channel on which FSK operation will be implemented.
FCS[1:0] = 00: Channel 0 is selected (default);
FCS[1:0] = 01: Channel 1 is selected;
FCS[1:0] = 10: Channel 2 is selected;
FCS[1:0] = 11: Channel 3 is selected;
FSK On/Off (FO) enables or disables the whole FSK function block.
FO = 0: FSK is disabled (default);
FO = 1: FSK is enabled.
BT/Bellcore Select bit (BS) determines which specification the IDT821054 follows:
BS = 0: Bellcore specification is selected (default);
BS = 1: BT specification is selected.
Mark After Send bit (MAS) determines the FSK block operation after the word data has been sent.
MAS = 0: The output will be muted after sending out word data (default);
MAS = 1: After sending one frame of message data (=< 64 bytes), IDT821054 keeps sending a series of '1' until the MAS bit is set to '0' and the FS bit is set to '1'.
FSK Start bit (FS) should be set to '1' when users are going to send out FSK data. It will be cleared to the default value '0' at the end of word data. When Seizure Length, Mark Length together with Data Length bits are all set to 0, the Transmit Start bit will be reset to '0' immediately after it is set to '1'.
FS = 0: disable; FS = 1: transmit start.

18. Level Meter Result Low Register (31H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	1
I/O data	LVLL[7]	LVLL[6]	LVLL[5]	LVLL[4]	LVLL[3]	LVLL[2]	LVLL[1]	LVLL[0]

This register contains the lower 8 bits of Level Meter output with the default value of '0000-0000', LVLL[0] is the high active data_ready bit. To read the level meter result, users should read the low register which contains LVLL[7:0] data first, then read the high register which contains LVLH[7:0] data. Once the high register is read, the LVLL[0] bit is cleared immediately.

19. Level Meter Result High Register (32H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	1	0
I/O data	LVLH[7]	LVLH[6]	LVLH[5]	LVLH[4]	LVLH[3]	LVLH[2]	LVLH[1]	LVLH[0]

This register contains the higher 8 bits of Level Metering output with the default value of 0(d).

20. Level Meter Count Number (33H/B3H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	0	1	1
I/O data	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]

Level Meter Count Number register is used to configure the number of time cycles for sampling PCM data.
CN[7:0] = 0000-0000: the linear or compressed PCM data is output to LVLH and LVLL directly;
CN[7:0] = N: PCM data is sampled for N * 125 μs (N from 1 to 255).

21. Level Meter Channel Select, Linear/Compressed, Level Meter On/off (34H/B4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	1	0	0
I/O data	*R*	*R*	*R*	*R*	LMO	L/C	CS[1]	CS[0]

Level Meter On/off bit (LMO) enables/disable the level meter.
LMO = 0: Level meter is disabled (default);
LMO = 1: Level meter is enabled.
Linear/Compressed bit (L/C) determines the mode of level meter operation.
L/C = 0: Message mode is selected, compressed PCM will be output to LVLH and LVLL transparently.
L/C = 1: Meter mode is selected, linear PCM data will be metered and output to LVLH and LVLL, when data_ready bit in LVLL register is '1'.

Level Meter Channel Select bits (CS[1:0]) select the channel, data on which will be level metered.

CS[1:0] = 00: Channel 0 is selected (default);
CS[1:0] = 01: Channel 1 is selected;
CS[1:0] = 10: Channel 2 is selected;
CS[1:0] = 11: Channel 3 is selected;

22. Loop Control and PLL Power Down (35H/B5H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	1	0	1
I/O data	*R*	*R*	PPD	DLB_ANA	ALB_8k	DLB_8k	DLB_DI	ALB_DI

PLL Power Down bit (PPD) controls the operation of Phase Lock Loop.

PPD = 0: PLL disable, the device is in normal operation (default);
PPD = 1: PLL is powered down. The device works in Power-Saving mode. All clocks stop running.

Loop Control bits determine the loopback status. Refer to Figure 4 for detail information.

DLB_ANA = 0: Digital Loopback via Analog Interface is disabled (default);
DLB_ANA = 1: Digital Loopback via Analog Interface is enabled;
ALB_8k = 0: Analog Loopback via 8 kHz Interface is disabled (default);
ALB_8k = 1: Analog Loopback via 8 kHz Interface is enabled;
DLB_8k = 0: Digital Loopback via 8 kHz Interface is disabled (default);
DLB_8k = 1: Digital Loopback via 8 kHz Interface is enabled;
DLB_DI = 0: Digital Loopback from DR to DX is disabled (default);
DLB_DI = 1: Digital Loopback from DR to DX is enabled;
ALB_DI = 0: Analog Loopback from DX to DR is disabled (default);
ALB_DI = 1: Analog Loopback from DX to DR is enabled.

LOCAL COMMANDS:

1. Coefficient Select (00H/80H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	0	0
I/O data	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]

Coefficient Select bits (CS[7:0]) are used to control digital filters and function blocks on corresponding channel such as Impedance Matching Filter, Echo Cancellation Filter, High-Pass Filter, Gain for Impedance Scaling, Gain in Transmit/Receive Path and Frequency Response Correction in Transmit/ Receive Path. See Figure 4 for detail. It should be noted that Impedance Matching Filter and Gain for Impedance Scaling are working together to adjust impedance. That is to say, CS[0] and CS[2] should be set to the same value to ensure the correct operation.

CS [7] = 0: Gain in Receive Path coefficient is set to be default value;
CS [7] = 1: Gain in Receive Path coefficient is set by GRX RAM.
CS [6] = 0: Frequency Response Correction in Receive Path coefficient is set to be default value;
CS [6] = 1: Frequency Response Correction in Receive Path coefficient is set by FRR RAM;
CS [5] = 0: Gain in Transmit Path coefficient is set to be default value;
CS [5] = 1: Gain in Transmit Path coefficient is set by GTX RAM;
CS [4] = 0: Frequency Response Correction in Transmit Path coefficient is set to be default value;
CS [4] = 1: Frequency Response Correction in Transmit Path coefficient is set by FRX RAM;
CS [3] = 0: High-Pass Filter is bypassed/disabled (default);
CS [3] = 1: High-Pass Filter is enabled;
CS [2] = 0: Gain for Impedance Scaling coefficient is set to be default value;
CS [2] = 1: Gain for Impedance Scaling coefficient is set by GIS RAM;
CS [1] = 0: Echo Cancellation Filter coefficient is set to be default value;
CS [1] = 1: Echo Cancellation Filter coefficient is set by ECF RAM;
CS [0] = 0: Impedance Matching Filter coefficient is set to be default value;
CS [0] = 1: Impedance Matching Filter coefficient is set by IMF RAM;

2. Loop Status Control and SLIC Input Interrupt Enable (01H/81H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	0	1
I/O data	IE[4]	IE[3]	IE[2]	IE[1]	IE[0]	LPC[2]	LPC[1]	LPC[0]

SLIC Input Interrupt Enable bits IE[4:0] enable or disable the interrupt signal on each channel.

IE[4] = 0: Interrupt disable. Interrupt signal on SB3 (when it is selected as an input) will be ignored (default);
IE[4] = 1: Interrupt enable. Interrupt signal on SB3 (when it is selected as an input) will be recognized;
IE[3] = 0: Interrupt disable. Interrupt signal on SB2 (when it is selected as an input) will be ignored (default);
IE[3] = 1: Interrupt enable. Interrupt signal on SB2 (when it is selected as an input) will be recognized;
IE[2] = 0: Interrupt disable. Interrupt signal on SB2 (when it is selected as an input) will be ignored (default);
IE[2] = 1: Interrupt enable. Interrupt signal on SB1 (when it is selected as an input) will be recognized;
IE[1] = 0: Interrupt disable. Interrupt signal on SI2 will be ignored (default);
IE[1] = 1: Interrupt enable. Interrupt signal on SI2 will be recognized;
IE[0] = 0: Interrupt disable. Interrupt signal on SI1 will be ignored (default);
IE[0] = 1: Interrupt enable. Interrupt signal on SI1 will be recognized;

Loop Status Control Bits (LPC[2:0]) determine the loopback status on corresponding channel. Refer to Figure 4 for detail information.

LPC[2] = 0: Digital Loopback via Time slots is disabled on the corresponding channel (default);
LPC[2] = 1: Digital Loopback via Time slots is enabled on the corresponding channel.
LPC[1] = 0: Analog Loopback via Onebit is disabled on the corresponding channel (default);
LPC[1] = 1: Analog Loopback via Onebit is enabled on the corresponding channel;
LPC[0] = 0: Digital Loopback via Onebit is disabled on the corresponding channel (default);
LPC[0] = 1: Digital loopback via Onebit is enabled on the corresponding channel;

3. DSH Debounce and GK Debounce (02H/82H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	1	0
I/O data	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]

DSH Debounce bits DSH[3:0] set the debounce time of SI1 input from SLIC for corresponding channel.

DSH[3:0] = 0000: 0 ms (default);
DSH[3:0] = 0001: 2 ms;
DSH[3:0] = 0010: 4 ms;
DSH[3:0] = 0011: 6 ms;
DSH[3:0] = 0100: 8 ms;
DSH[3:0] = 0101: 10 ms;
DSH[3:0] = 0110: 12 ms;
DSH[3:0] = 0111: 14 ms;
DSH[3:0] = 1000: 16 ms;
DSH[3:0] = 1001: 18 ms;
DSH[3:0] = 1010: 20 ms;
DSH[3:0] = 1011: 22 ms;
DSH[3:0] = 1100: 24 ms;
DSH[3:0] = 1101: 26 ms;
DSH[3:0] = 1110: 28 ms;
DSH[3:0] = 1111: 30 ms.

GK Debounce bits GK[3:0] set the debounce time of SI2 input from SLIC for corresponding channel.

GK[3:0] = 0000: 0 ms (default);
GK[3:0] = 0001: 2 ms;
GK[3:0] = 0010: 4 ms;
GK[3:0] = 0011: 6 ms;
GK[3:0] = 0100: 8 ms;
GK[3:0] = 0101: 10 ms;
GK[3:0] = 0110: 12 ms;
GK[3:0] = 0111: 14 ms;
GK[3:0] = 1000: 16 ms;
GK[3:0] = 1001: 18 ms;
GK[3:0] = 1010: 20 ms;
GK[3:0] = 1011: 22 ms;
GK[3:0] = 1100: 24 ms;
GK[3:0] = 1101: 26 ms;
GK[3:0] = 1110: 28 ms;
GK[3:0] = 1111: 30 ms;

4. Channel I/O Data (03H/83H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	1	1
I/O data	*R*	SO2	SO1	SB3	SB2	SB1	SI2	SI1

Channel I/O Data bits contain the information of SLIC I/O pins SI1, SI2, SB1, SB2, SB3, SO1 and SO2 on corresponding channel.

If SB1, SB2 or SB3 is configured as output, this command can not be used to write to SB1, SB2 or SB3. Writing to SB1, SB2 or SB3 can only be performed by Global Command 10, 11 and 12, respectively.

5. Transmit Time Slot and Transmit Highway Selection (04H/84H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	0	0
I/O data	THS	TT[6]	TT[5]	TT[4]	TT[3]	TT[2]	TT[1]	TT[0]

Transmit Time Slot Bits (TT[6:0]) determine which time slot will be used to transmit data for corresponding channel. The valid value is 0d - 127d corresponding to Time slot 0 to Time slot 127. The default value is 0d.

Transmit Highway Selection bit (THS) selects the PCM highway on corresponding channel to transmit voice data.

THS = 0: DX1 is selected (default);
THS = 1: DX2 is selected.

6. Receive Time Slot and Receive Highway Selection (05H/85H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	0	1
I/O data	RHS	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

Receive Time Slot Bits RT[6:0] determine which time slot will be used to receive data for corresponding channel. The valid value is 0d - 127d corresponding to Time slot 0 to Time slot 127. The default value is 0d.

Receive Highway Selection bit RHS selects the PCM highway on corresponding channel to receive voice data.

RHS = 0: DR1 is selected (default);

RHS = 1: DR2 is selected.

7. PCM Data Low byte [7:0] (06H/86H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	1	0
I/O data	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]

This command is used for MCU to monitor the transmit (A to D) PCM data. For linear Code, the low 8 bits of the PCM data will be output at CO pin, and at the same time, the transmit data will be output to PCM bus without any interference. For compressed code (A/μ-Law), the total 8 bit PCM data will be output at CO pin.

8. PCM Data High byte [15:8] (07H/87H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	1	1	1
I/O data	PCM[15]	PCM[14]	PCM[13]	PCM[12]	PCM[11]	PCM[10]	PCM[9]	PCM[8]

This command is used for MCU to monitor the transmit (A to D) PCM data. For linear Code, the high 8 bits of the PCM data will be output at CO pin, and at the same time, the transmit data will be output to PCM bus without any interference. For compressed code (A/μ-Law), this command is not used.

9. A/D Gain, D/A Gain, Power Down and PCM Receive Path Cutoff (08H/88H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	0	0
I/O data	PD	PCMCT	GAD	GDA	0	0	0	0

Channel Power Down bit (PD) selects the operation mode on corresponding channel:

PD = 0: the corresponding channel is in normal operation;

PD = 1: the corresponding channel is powered down (default).

PCMCT bit determines the operation of PCM Receive Path on corresponding channel:

PCMCT = 0: PCM Receive Path is in normal operation (default);

PCMCT = 1: PCM Receive Path is cut off.

A/D Gain bit (GAD) sets the gain of analog A/D for corresponding channel:

GAD = 0: 0 dB (default); GAD = 1: +6 dB.

D/A Gain bit (GDA) sets the gain of analog D/A for corresponding channel:

GDA = 0: 0 dB (default); GDA = 1: -6 dB.

Attention: The lower 4 bits of the I/O data byte that follows this write-command (88H) must be '0000' to ensure proper operation.

10. Tone On/Off and Tone Program Enable (09H/89H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	0	1
I/O data	*R*	*R*	*R*	*R*	1	1	TEN1	TEN0

TEN1 = 0: Tone1 generator is disable (default);

TEN1 = 1: Tone1 generator is enable.

TEN0 = 0: Tone0 generator is disable (default);

TEN0 = 1: Tone0 generator is enable.

Attention: The b2 and b3 of the I/O data byte that follows this write-command (89H) must be '11' to ensure proper operation.

ABSOLUTE MAXIMUM RATINGS

Rating	Com'l & Ind'l	Unit
Power Supply Voltage	≤ 6.5	V
Voltage on Any Pin with Respect to Ground	-0.5 to 5.5	V
Package Power Dissipation	≤1.5	W
Storage Temperature	-65 to +150	°C

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	4.75		5.25	V

NOTE: MCLK: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz with tolerance of ± 50 ppm

ELECTRICAL CHARACTERISTICS

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.8	V	DX, I_L = 8 mA All other digital outputs, I_L = 4 mA.
V_{OH}	Output High Voltage	VDD - 0.6			V	DX, I_L = -8 mA All other digital outputs, I_L = -4 mA.
I_I	Input Current	-10		10	µA	All digital inputs, GND<VIN<VDD
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Test Conditions
I_{DD1}	Operating Current		50		mA	All channels are active.
I_{DD0}	Standby Current			6	mA	All channels are powered down, with MCLK present.

Note: Power measurements are made at MCLK = 2.048MHz, outputs unloaded.

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{OUT1}	Output Voltage, VOUT	2.25	2.4	2.6	V	Alternating ±zero µ-law PCM code applied to DR
V_{OUT2}	Output Voltage Swing, VOUT	3.25			Vp-p	R_L = 300 Ω
R_I	Input Resistance, VIN	30	40	60	kΩ	0.25 V < VIN < 4.75 V
R_O	Output Resistance VOUT			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR.
R_L	Load Resistance, VOUT	300			Ω	External loading
C_L	Load Capacitance, VOUT			100	pF	External loading

TRANSMISSION CHARACTERISTICS

0 dBm0 is defined as 0.775 Vrms for A-law and 0.769 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected. Typical values are for V_{DD} = 5V and T_A = 25°C.

Absolute Gain

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XA}	Transmit Gain, Absolute	-0.25		0.25	dB	Signal input of 0 dBm0, μ-law or A-law
G_{RA}	Receive Gain, Absolute	-0.25		0.25	dB	Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0 1020 Hz , R_L = 10 kΩ

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to –37 dBm0 (exclude –37 dBm0)	-0.25		0.25	dB	
	-37 dBm0 to -50 dBm0 (exclude –50 dBm0)	-0.5		0.50	dB	
	-50 dBm0 to -55 dBm0	-1.4		1.4	dB	
GT_R	Receive Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0 (exclude –40 dBm0)	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0 (exclude –50 dBm0)	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XR}	Transmit Gain, Relative to G_{XA}					
	f = 50 Hz	-0.15		-30	dB	
	f = 60 Hz	-0.15		-30	dB	
	f = 300 Hz	-0.1		0.2	dB	High-pass filter is enabled.
	f between 300 Hz and 3400 Hz	-0.15		0.15	dB	
	f = 3600 Hz	-0.15		-0.1	dB	
	f = 4600 Hz and above	-0.15		-35	dB	
G_{RR}	Receive Gain, Relative to G_{RA}					
	f below 300 Hz			0	dB	
	f = 300 Hz to 3400 Hz	-0.15		0.15	dB	High-pass filter is enabled.
	f = 3600 Hz			-0.2	dB	
	f = 4600 Hz and above			-35	dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
D_{XR}	Transmit Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			280	μs	
	f = 600 Hz –1000 Hz			150	μs	
	f = 1000 Hz – 2600 Hz			80	μs	
	f = 2600 Hz – 2800 Hz			280	μs	
D_{RR}	Receive Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			50	μs	
	f = 600 Hz –1000 Hz			80	μs	
	f = 1000 Hz – 2600 Hz			120	μs	
	f = 2600 Hz – 2800 Hz			150	μs	

TRANSMISSION CHARACTERISTICS (CONTINUED)

Distortion

Parameter	Description	Min	Typ	Max	Units	Test Conditions
STDX	Transmit Signal to Total Distortion Ratio					ITU-T O.132
	A-law :					Sine Wave Method,Psophometric Weighted for A-law, C Message Weighted for μ-law.
	Input level = 0 dBm0	36			dB	
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	30			dB	
	Input level = -45 dBm0	24			dB	
	μ-law :					
	Input level = 0 dBm0	36			dB	
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	31			dB	
	Input level = -45 dBm0	27			dB	
STDR	Receive Signal to Total Distortion Ratio					ITU-T O.132
	A-law :					
	Input level = 0 dBm0	36			dB	Sine Wave Method,Psophometric Weighted for A-law;Sine Wave Method,C Message Weighted for μ-law;
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	30			dB	
	Input level = -45 dBm0	24			dB	
	μ-law :					
	Input level = 0 dBm0	36			dB	
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	31			dB	
	Input level = -45 dBm0	27			dB	
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation Distortion			-42	dBm0	Transmit or receive,two frequencies in the range (300 Hz– 3400 Hz) at –6 dBm0

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise, C Message Weighted for μ-law			15	dBrnC0	
NXP	Transmit Noise, Psophometric Weighted for A-law			-70	dBm0p	
NRC	Receive Noise, C Message Weighted for μ-law			10	dBrnC0	
NRP	Receive Noise, Psophometric Weighted for A-law			-80	dBm0p	
NRS	Noise, Single Frequency			-53	dBm0	VIN = 0 Vrms, tested at VOUT
	f = 0 kHz – 100 kHz					
PSRX	Power Supply Rejection Transmit					VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
PSRR	Power Supply Rejection Receive					PCM code is positive one LSB, VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
SOS	Spurious Out-of-Band Signals at VOUT Relative to Input PCM code applied:					0 dBm0, 300 Hz – 3400 Hz input
	4600 Hz – 20 kHz			-40	dB	
	20 kHz – 50 kHz			-30	dB	

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XTX-R	Transmit to Receive Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. Idle PCM code into channel under test.
XTR-X	Receive to Transmit Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. VIN = 0 Vrms for channel under test.
XTX-X	Transmit to Transmit Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. VIN = 0 Vrms for channel under test.
XTR-R	Receive to Receive Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling from VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN. Idle PCM code into DR.
XT_{R-X}	Receive to Transmit Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into DR. VIN = 0 Vrms.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

TIMING CHARACTERISTICS

Reset and Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t0	Reset pulse width	50			µs	
t1	CCLK period	122		100k	ns	
t2	CCLK pulse width	48			ns	
t3	CCLK Rise and Fall Time			25	ns	
t4	BCLK period	122			ns	
t5	BCLK pulse width	48			ns	
t6	BCLK Rise and Fall time			15	ns	
t7	MCLK pulse width	48			ns	
t8	MCLK Rise and Fall time			15	ns	

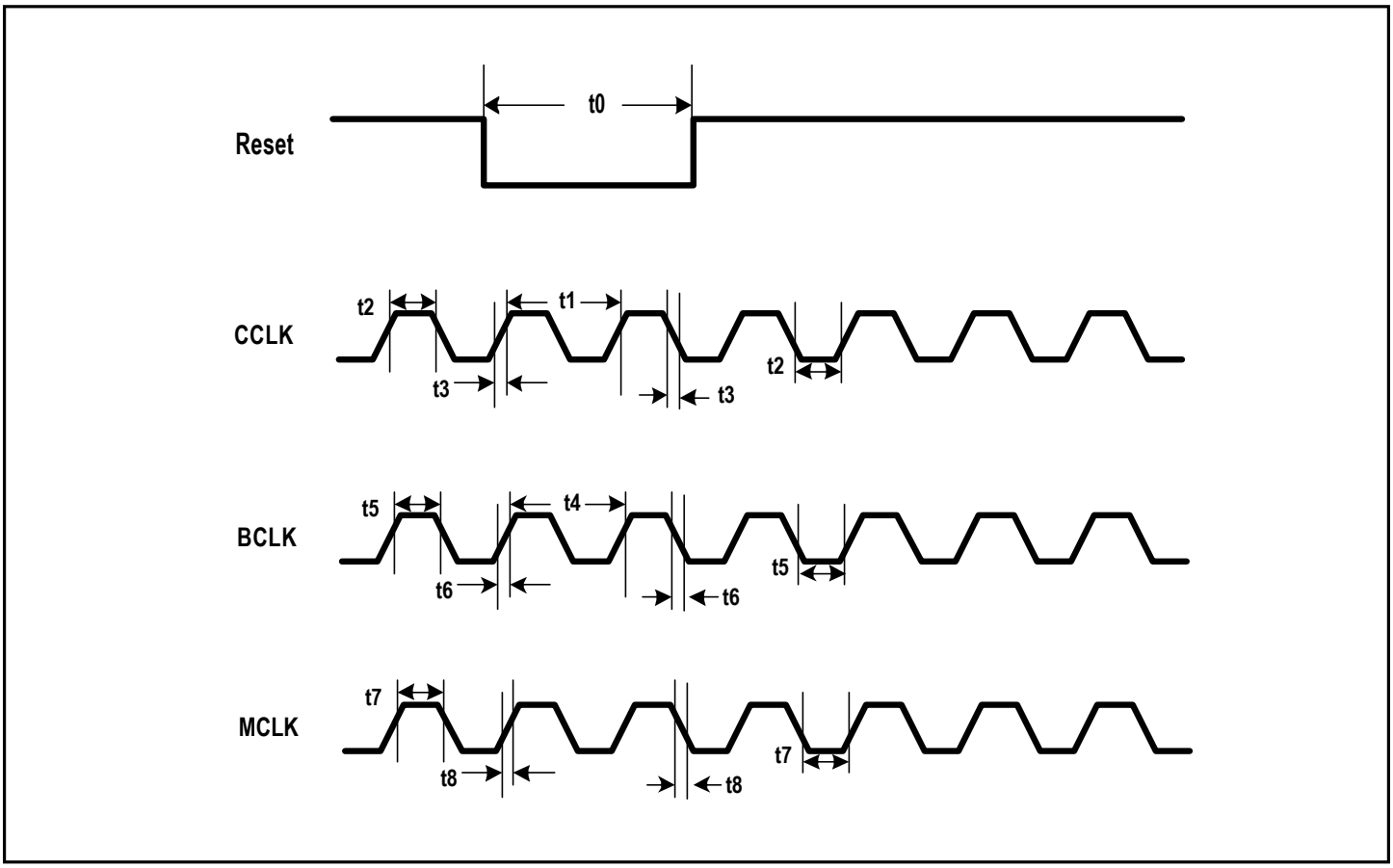


Figure 7. Reset and Clock Timing

Microprocessor Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t11	$\overline{CS}$ setup time	15		70	ns	
t13	$\overline{CS}$ pulse width		8n*t1 (n>=2)		ns	
t14	$\overline{CS}$ off time	250			ns	
t15	Input data setup time	30			ns	
t16	Input data hold time	30			ns	
t17	SLIC output latch valid			1000	ns	
t21	Output data turn on delay			50	ns	
t22	Output data hold time	0			ns	
t23	Output data turn off delay			50	ns	
t24	Output data valid	0		50	ns	

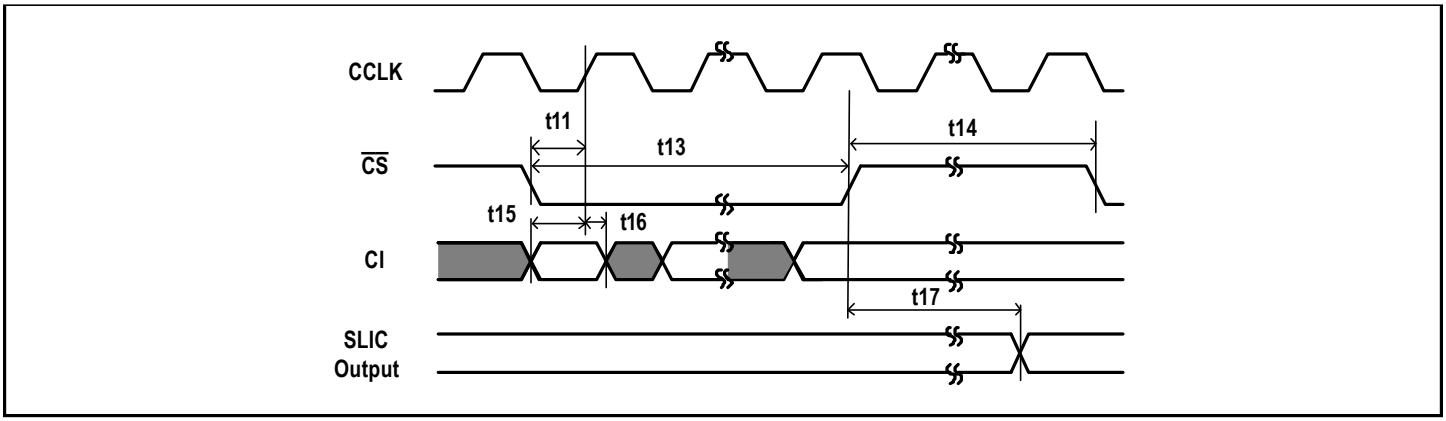


Figure 8. MPI Input Timing

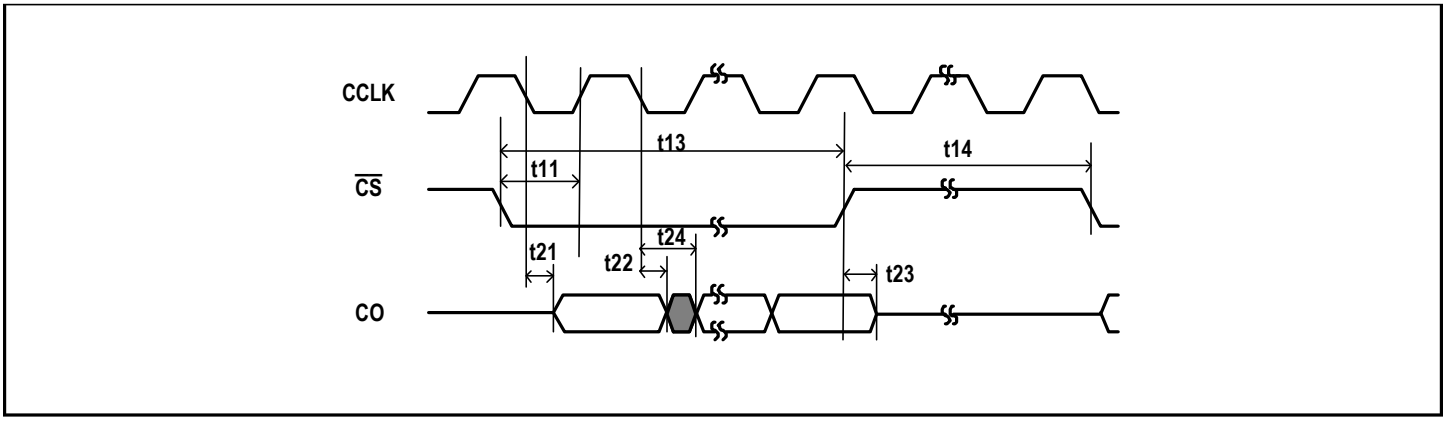


Figure 9. MPI Output Timing

PCM Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t51	Data enable delay time	5		70	ns	
t52	Data delay time from BCLK	5		70	ns	
t53	Data float delay time	5		70	ns	
t54	Frame sync setup time	25		t4 - 50	ns	
t55	Frame sync hold time	50			ns	
t56	$\overline{TSX1}$ or $\overline{TSX2}$ enable delay time	5		80	ns	
t57	$\overline{TSX1}$ or $\overline{TSX2}$ disable delay time	5		80	ns	
t61	Receive data setup time	25			ns	
t62	Receive data hold time	5			ns	

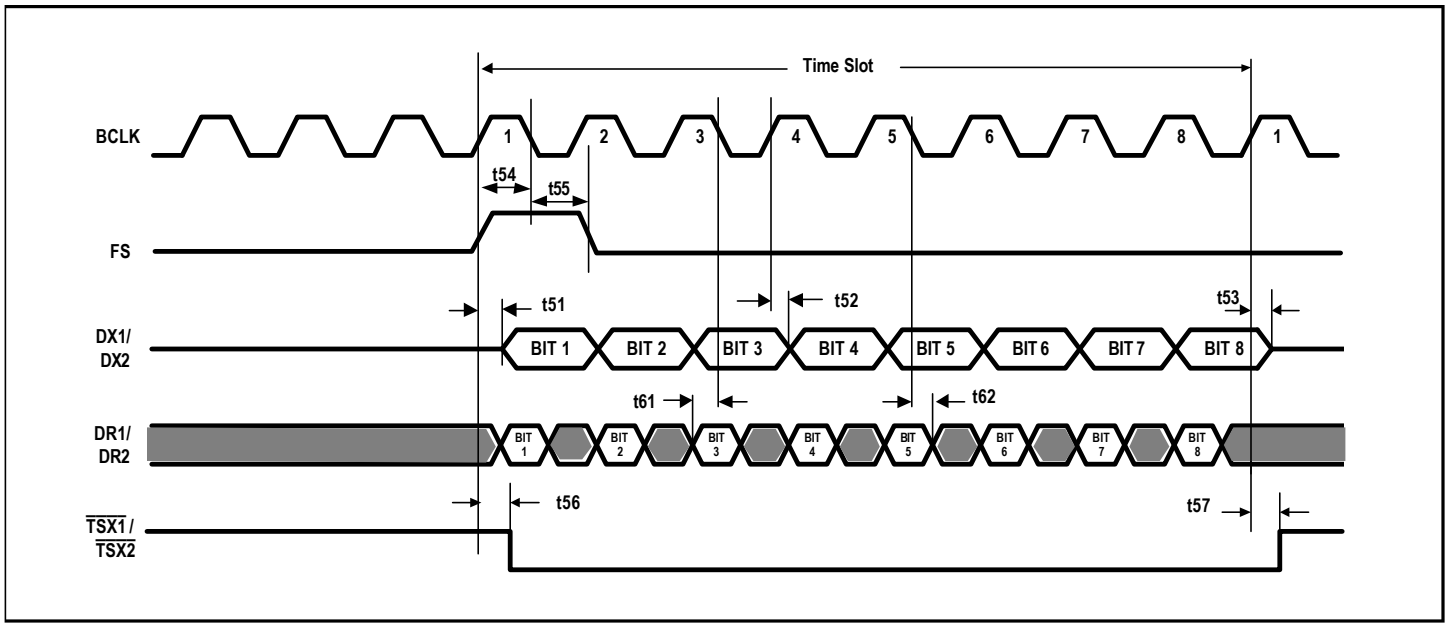


Figure 10. Transmit and Receive Timing *

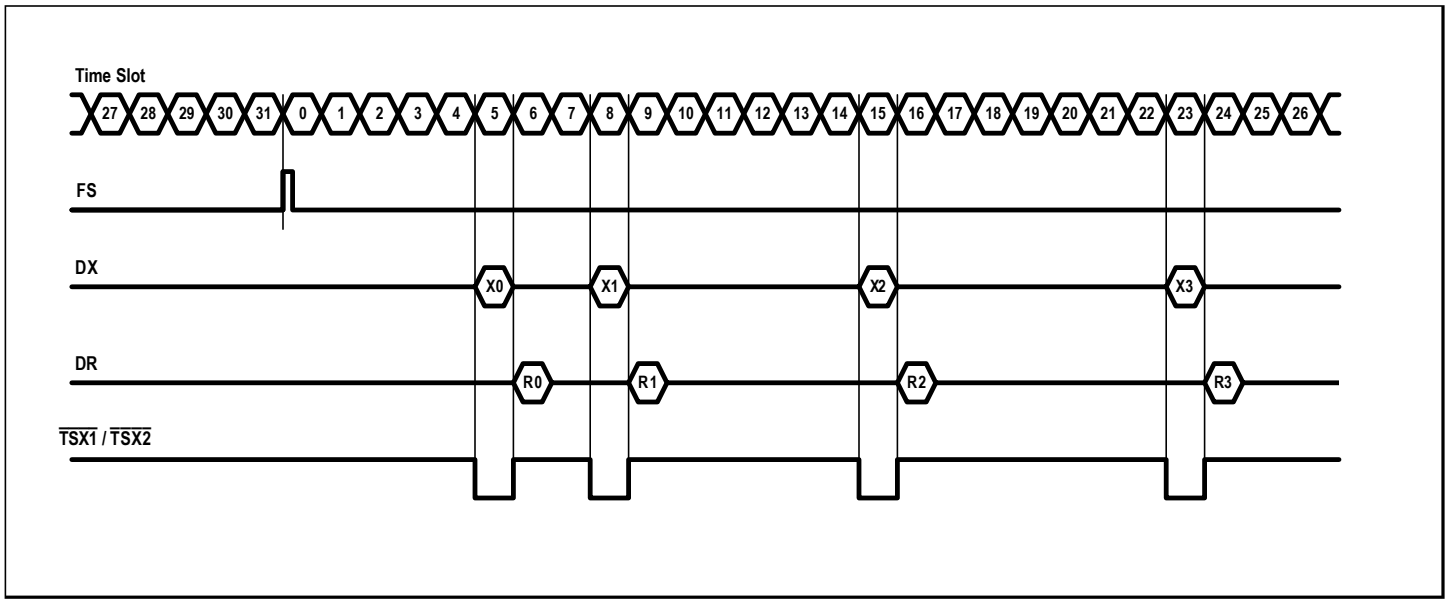
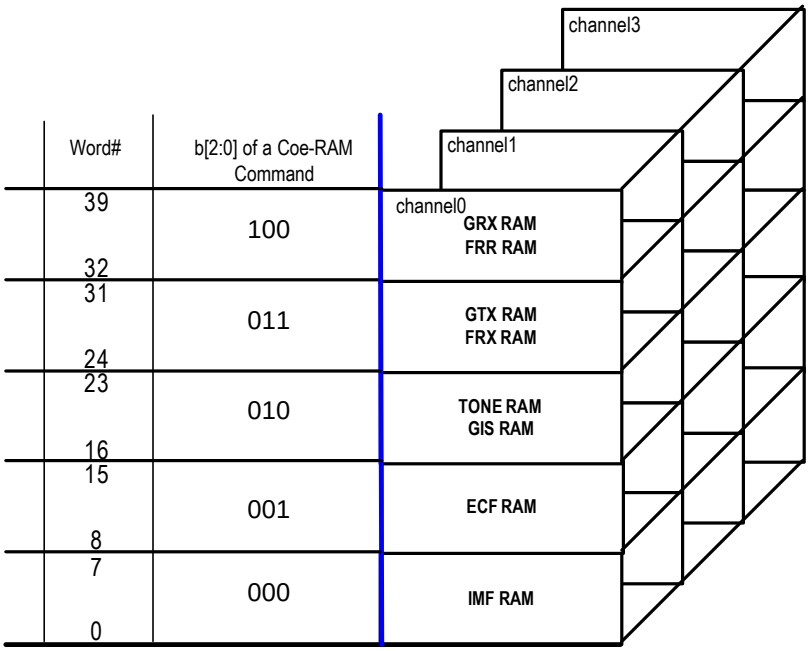


Figure 11. Typical Frame Sync Timing (2 MHz Operation)

Note*: These timing diagram only apply to the situation when data clock in on falling edges and clock out on rising edges.

APPENDIX: IDT821054 Coe-RAM Address Mapping



Generally, 6 bits of address are needed to locate each word of the 40 Coe-RAM words. The 40 words of Coe-RAM are divided into 5 blocks with 8 words per block in IDT821054, so only 3 bits of address are needed to locate each of the block. When the address of a Coe-RAM block (b[2:0]) is specified in a Coe-RAM Command, all 8 words of this block will be addressed automatically, with the highest order word first (IDT821054 will count down from '111' to '000' so that it accesses the 8 words successively). Refer to page 14 and 15 for more information.

The address assignment for the 40 words Coe-RAM is shown in the following table. The number in the "Address" column is the actual address of the Coe-RAM word, as the IDT821054 handles the lower 3 bits automatically, only the higher 3 bits (in bold style) are needed for a Coe-RAM Command. It should be noted that, when addressing the GRX RAM, the FRR RAM will be addressed at the same time.

Table 7 - Coe-RAM Address Allocation

Word #	Address	Function	Word #	Address	Function
39	**100**,111	GRX RAM	19	**010**,011	GIS RAM
38	**100**,110	FRR RAM	18	**010**,010	
37	**100**,101		17	**010**,001	
36	**100**,100		16	**010**,000	
35	**100**,011		15	**001**,111	ECF RAM
34	**100**,010		14	**001**,110	
33	**100**,001		13	**001**,101	
32	**100**,000		12	**001**,100	
31	**011**,111	GTX RAM	11	**001**,011	
30	**011**,110	FRX RAM	10	**001**,010	
29	**011**,101		9	**001**,001	
28	**011**,100		8	**001**,000	
27	**011**,011		7	**000**,111	IMF RAM
26	**011**,010		6	**000**,110	
25	**011**,001		5	**000**,101	
24	**011**,000		4	**000**,100	
23	**010**,111	Amplitude Coefficient of Tone Generator 1	3	**000**,011	
22	**010**,110	Frequency Coefficient of Tone Generator 1	2	**000**,010	
21	**010**,101	Amplitude Coefficient of Tone Generator 0	1	**000**,001	
20	**010**,100	Frequency Coefficient of Tone Generator 0	0	**000**,000	

Data Sheet Document History

12/21/2001	pgs. 8, 22, 26, 27
01/03/2002	pg. 24
01/23/2002	pgs. 1, 2, 5, 7, 11, 15, 21
02/19/2002	pg. 27

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