3.3V CMOS 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16282

FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 1.65V ± 3.6V**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in TVSOP package**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Suitable for heavy loads**

APPLICATIONS:

- **SDRAM Modules**
- **PC Motherboards**
- **Workstations**

DESCRIPTION:

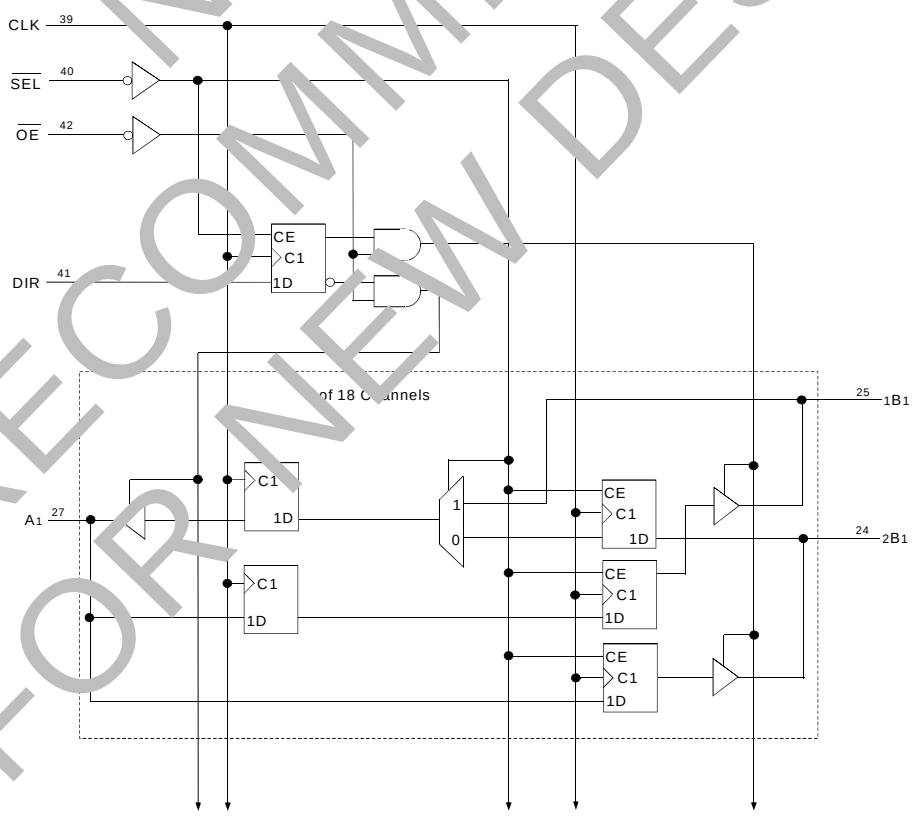
This 18-bit to 36-bit registered bus exchanger is manufactured using advanced dual metal CMOS technology. This device is intended for use in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The ALVCH16282 provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select ($\overline{SEL}$) input selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ($\overline{OE}$) and the DIR input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

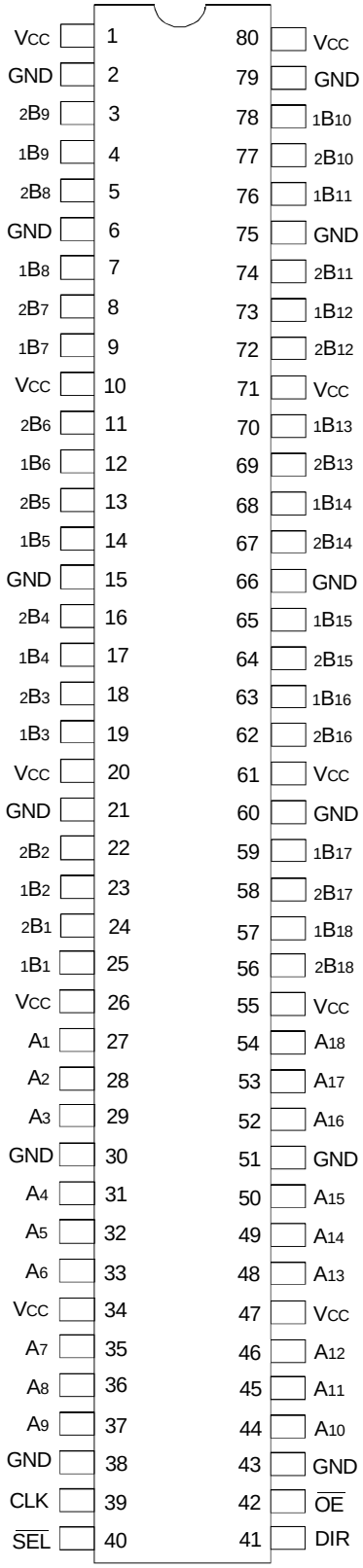
The ALVCH16282 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16282 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK}	Continuous Clamp Current, V_I < 0 or V_I > V_{CC}	±50	mA
I_{OK}	Continuous Clamp Current, V_O < 0	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	—	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	—	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Input (Active LOW)
CLK	Register Input Clock
$\overline{SEL}$	Select Input
Ax	Data Inputs or 3-State Outputs(1)
xBx	Data Inputs or 3-State Outputs(1)
DIR	Direction Control Input

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES(1)

A-TO-B STORAGE ($\overline{OE}$ = L AND DIR = H)

Inputs			Outputs	
$\overline{SEL}$	CLK	Ax	1Bx	2Bx
H	X	X	$1B_0$(2)	$2B_0$(2)
L	↑	L	L(3)	L
L	↑	H	H(3)	H

B-TO-A STORAGE ($\overline{OE}$ = L AND DIR = L)

Inputs				Output
$\overline{SEL}$	CLK	1Bx	2Bx	Ax
H	↑	X	L	L(4)
H	↑	X	H	H(4)
L	↑	L	X	L
L	↑	H	X	H

OUTPUT ENABLE

Inputs				Outputs	
CLK	$\overline{OE}$	$\overline{SEL}$	DIR	Ax	1Bx, 2Bx
↑	H	X	X	Z	Z
↑	L	L	H	Z	Active
↑	L	L	L	Active	Z
X	L	H	X	A_0(2)	$1B_0$(2), $2B_0$(2)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition
2. Output level before the indicated steady-state input conditions were established.
3. Two CLK edges are needed to propagate data.
4. Two CLK edges are needed to propagate data. The data is loaded in the first register when $\overline{SEL}$ is LOW and propagates to the second register when $\overline{SEL}$ is HIGH.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 1.65V to 1.95V		0.65 x V_{CC}	—	—	V
		V_{CC} = 2.3V to 2.7V		1.7	—	—	
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 1.65V to 1.95V		—	—	0.35 x V_{CC}	V
		V_{CC} = 2.3V to 2.7V		—	—	0.7	
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(excluding bus-hold pins)		V_O = GND	—	—	±10	
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	–75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	–45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA
I_{BHLO}							

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 1.65V to 3.6V	I_{OH} = –4mA	V_{CC}–1.2	—	V
		V_{CC} = 1.65V	I_{OH} = –4mA	1.2	—	
		V_{CC} = 2.3V	I_{OH} = –6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = –12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = –24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 1.65V to 3.6V	I_{OL} = 4mA	—	0.45	V
		V_{CC} = 1.65V	I_{OL} = 4mA	—	0.45	
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	282	310	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		208	228	

SWITCHING CHARACTERISTICS(1)

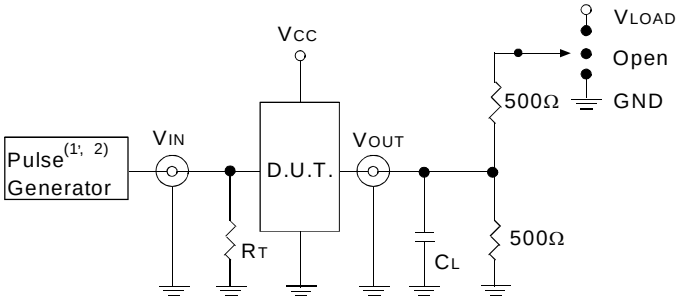
Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Ax	1	6.1	—	5.5	1.4	5	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to xBx	1.2	6.3	—	5.7	1.6	5.3	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to Ax	1.5	6.5	1.3	6.1	1.2	5.7	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to xBx	1.5	6.5	1.3	6.1	1.2	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to Ax	1.5	6.9	1.3	6.3	1.2	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to xBx	1.5	6.9	1.3	6.3	1.2	5.7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Ax	1.3	6.9	—	6.3	1.2	5.7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to xBx	2.3	8.7	—	8.1	2.3	7.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Ax	1.5	7	—	5.6	1.8	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to xBx	2.1	7.9	—	6.4	2.3	6.4	ns
t_{SU}	Set-up Time, Ax data before CLK↑	2.4	—	2.3	—	2	—	ns
t_{SU}	Set-up Time, xBx data before CLK↑	2.2	—	2.2	—	1.8	—	ns
t_{SU}	Set-up Time, DIR data before CLK↑	2.2	—	2.1	—	1.7	—	ns
t_{SU}	Set-up Time, $\overline{SEL}$ before CLK↑	2	—	2	—	1.8	—	ns
t_H	Hold Time, Ax data after CLK↑	0.5	—	0.5	—	0.7	—	ns
t_H	Hold Time, xBx data after $\overline{LE}$	0.5	—	0.5	—	0.6	—	ns
t_H	Hold Time, DIR after CLK↑	0.5	—	0.5	—	0.5	—	ns
t_H	Hold Time, $\overline{SEL}$ after CLK↑	0.7	—	0.7	—	0.8	—	ns
t_W	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns

NOTE:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$=3.3V±0.3V	$V_{CC}^{(1)}$=2.7V	$V_{CC}^{(2)}$=2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



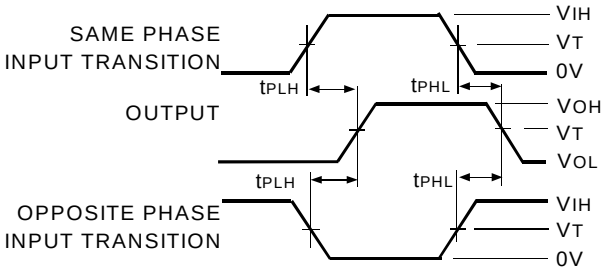
Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

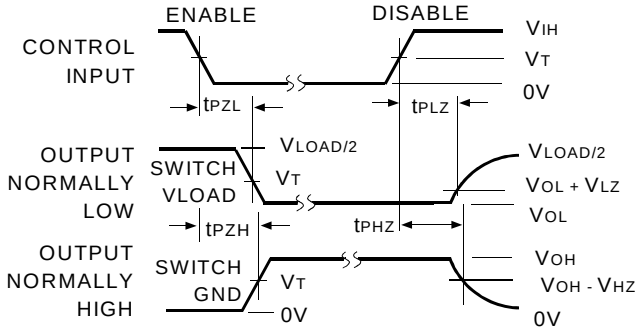
NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

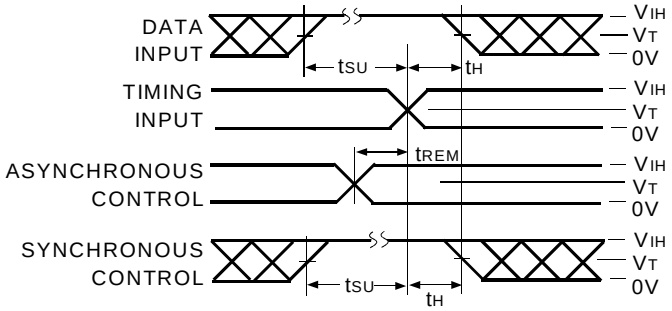


Propagation Delay

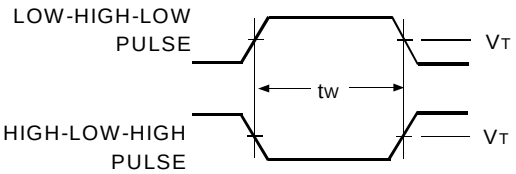


Enable and Disable Times

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

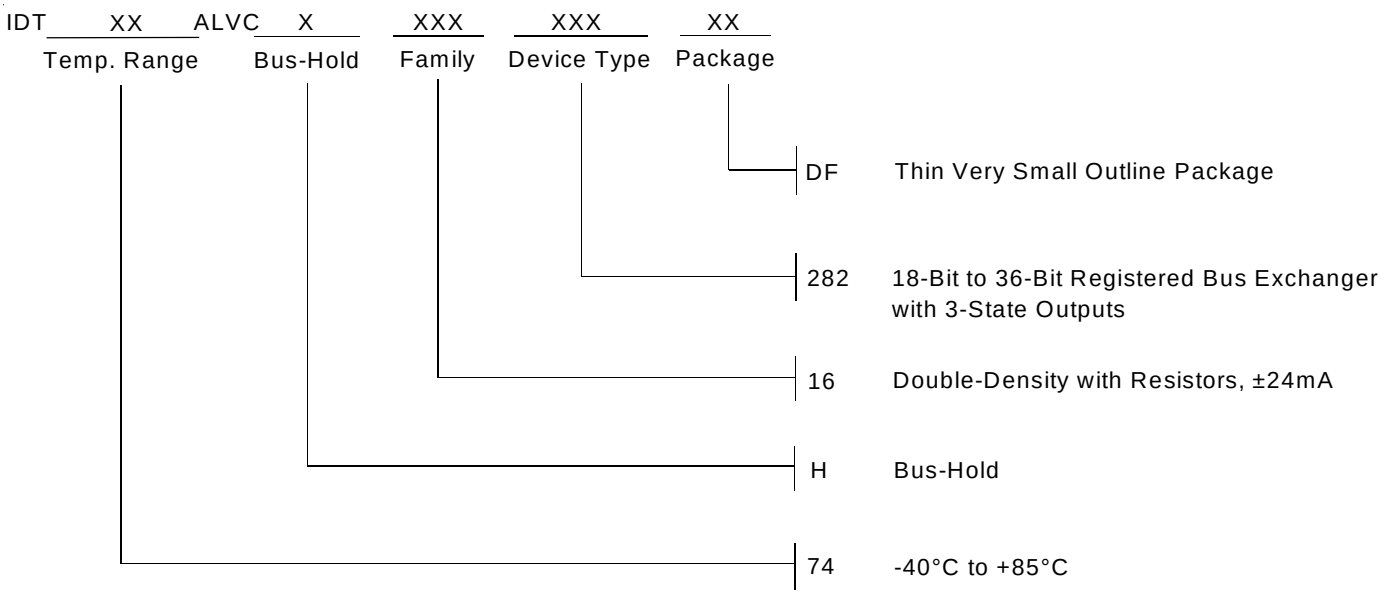


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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