



# 3.3V CMOS 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCHG162282

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP package
- Commercial range of 0°C to +70°C
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- CMOS power levels (0.4 $\mu$ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low switching noise

## APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

## DESCRIPTION:

This 18-bit to 36-bit registered bus exchanger is manufactured using advanced dual metal CMOS technology. The ALVCHG162282 is intended for use in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

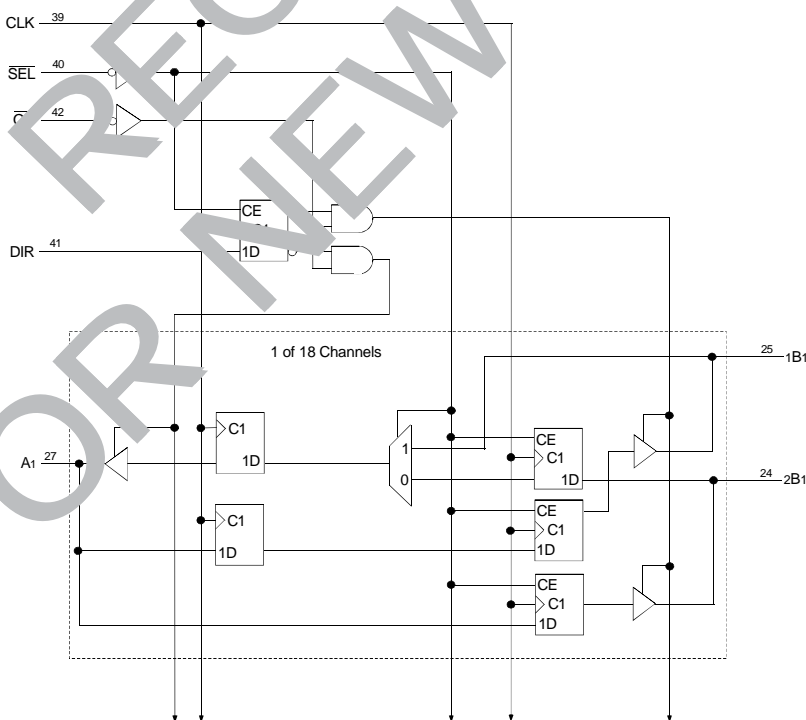
The ALVCHG162282 provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select ( $\overline{SEL}$ ) input selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ( $\overline{OE}$ ) and the direction-control (DIR) input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

A port outputs have equivalent 50 $\Omega$  series resistors. B port outputs have equivalent 20 $\Omega$  series resistors.

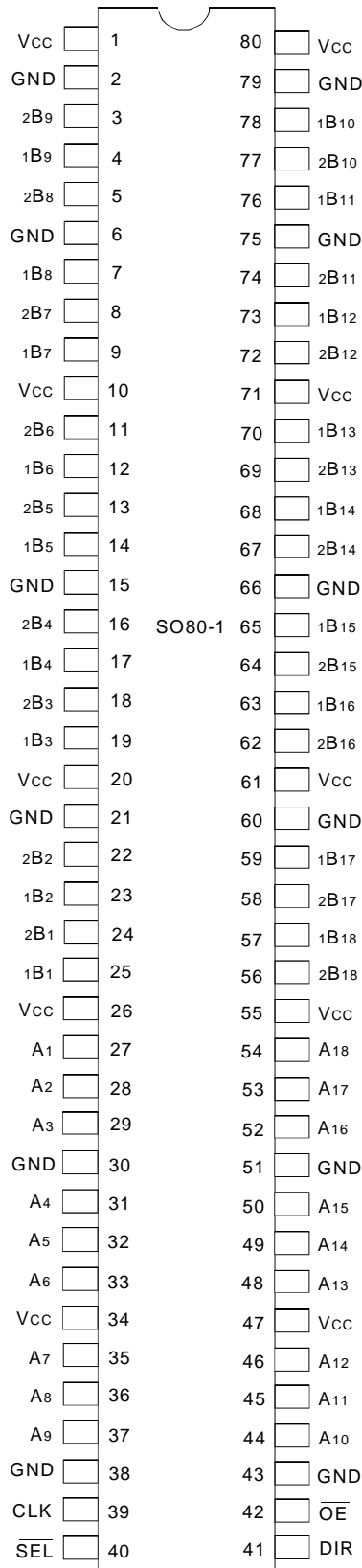
The switching characteristics in this spec, are based on 25pF (A Port) and 80pF (B Port) loads, but production test is accomplished with the standard 50pF load.

The ALVCHG162282 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TVSOP  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	- 0.5 to Vcc + 0.5	V
TSTG	Storage Temperature	- 65 to + 150	°C
IOUT	DC Output Current	- 50 to + 50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > Vcc	± 50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub>	Continuous Current through each Vcc or GND	±100	mA

NEW16link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Control Inputs	V <sub>IN</sub> = Vcc or GND	4	—	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	—	pF
C <sub>I/O</sub>	I/O Port Capacitance (A or B ports)	V <sub>OUT</sub> = Vcc or GND	8.5	—	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Input (Active LOW)
CLK	Register Input Clock
$\overline{SEL}$	Select Input
A <sub>x</sub>	Data Inputs <sup>(1)</sup> or 3-State Outputs
xB <sub>x</sub>	Data Inputs <sup>(1)</sup> or 3-State Outputs
DIR	Direction Control Input

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES<sup>(1)</sup>A-TO-B STORAGE ( $\overline{OE} = L, DIR = H$ )

Inputs			Outputs	
$\overline{SEL}$	CLK	Ax	1Bx	2Bx
H	X	X	1B <sub>0</sub> <sup>(2)</sup>	2B <sub>0</sub> <sup>(2)</sup>
L	↑	L	L <sup>(3)</sup>	L
L	↑	H	H <sup>(3)</sup>	H

OUTPUT ENABLE

Inputs				Outputs	
CLK	$\overline{OE}$	$\overline{SEL}$	DIR	Ax	1Bx, 2Bx
↑	H	X	X	Z	Z
↑	L	L	H	Z	Active
↑	L	L	L	Active	Z
X	L	H	X	A <sub>0</sub> <sup>(2)</sup>	1B <sub>0</sub> -2B <sub>0</sub> <sup>(2)</sup>

B-TO-A STORAGE ( $\overline{OE} = L, DIR = L$ )

Inputs				Outputs
$\overline{SEL}$	CLK	1Bx	2Bx	Ax
H	↑	X	L	L <sup>(4)</sup>
H	↑	X	H	H <sup>(4)</sup>
L	↑	L	X	L
L	↑	H	X	H

## NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH Transition
- Output level before indicated steady-state input conditions were established.
- Two CLK edges are needed to propagate the data.
- Two CLK edges are needed to propagate the data. The data is loaded in the first register when  $\overline{SEL}$  is LOW and propagates to the second register when  $\overline{SEL}$  is HIGH.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 3V to 3.6V		2	—	—	V
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 3V to 3.6V		—	—	0.8	V
I <sub>IH</sub>	Input HIGH Current <sup>(2)</sup>	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	± 5	μA
I <sub>IL</sub>	Input LOW Current <sup>(2)</sup>	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	± 5	
I <sub>OZH</sub>	High Impedance Output Current (excludes bus-hold pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = V <sub>CC</sub>	—	—	± 10	μA
I <sub>OZL</sub>			V <sub>O</sub> = GND	—	—	± 10	μA
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	40	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> – 0.6V, other inputs at V <sub>CC</sub> or GND	V <sub>CC</sub> = 3-3.6V	—	—	750	μA

## NOTES

- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- For control I/P's only excludes bus-hold current.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3.0V	V <sub>I</sub> = 2.0V	-75	—	—	μA
IBHL			V <sub>I</sub> = 0.8V	75	—	—	
IBHHO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA
IBHLO							

## NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
	(A port to B port)	V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -8mA	2	—	
	(B port to A port)		I <sub>OH</sub> = -6mA	2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3.0V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
	(A port to B port)	V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 8mA	—	0.8	
	(B port to A port)		I <sub>OL</sub> = 6mA	—	0.8	

## NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = 0°C to +70°C.

OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	80	pF
CPD	Power Dissipation Capacitance Outputs disabled		60	pF

SWITCHING CHARACTERISTICS,  $C_L = 25\text{pF}$  (A port),  $80\text{pF}$  (B port) <sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to Ax	1.5	5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLK to xBx	1.5	7.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time CLK to Ax	1.5	6.3	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time CLK to xBx	1.5	9.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to Ax	1.5	6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to xBx	1.5	9.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time CLK to Ax	1.5	6.4	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time CLK to xBx	1.5	7.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to Ax	1.5	5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to xBx	1.5	7.6	ns
t <sub>su</sub>	Setup Time, HIGH or LOW, Ax data before CLK $\uparrow$	1.5	—	ns
t <sub>su</sub>	Setup Time, HIGH or LOW, xBx data before CLK $\uparrow$	2	—	ns
t <sub>su</sub>	Setup Time, HIGH or LOW, DIR before CLK $\uparrow$	2	—	ns
t <sub>su</sub>	Setup Time, HIGH or LOW, $\overline{SEL}$ before CLK $\uparrow$	2	—	ns
t <sub>h</sub>	Hold Time, HIGH or LOW, Ax data after CLK $\uparrow$	0.3	—	ns
t <sub>h</sub>	Hold Time, HIGH or LOW, xBx data after CLK $\uparrow$	0.3	—	ns
t <sub>h</sub>	Hold Time, HIGH or LOW, DIR after CLK $\uparrow$	0.3	—	ns
t <sub>h</sub>	Hold Time, HIGH or LOW, $\overline{SEL}$ after CLK $\uparrow$	0.3	—	ns
t <sub>w</sub>	Pulse Duration, CLK HIGH or LOW	2.3 <sup>(2)</sup>	—	ns
f <sub>CLOCK</sub>		—	160	MHz

**NOTES:**

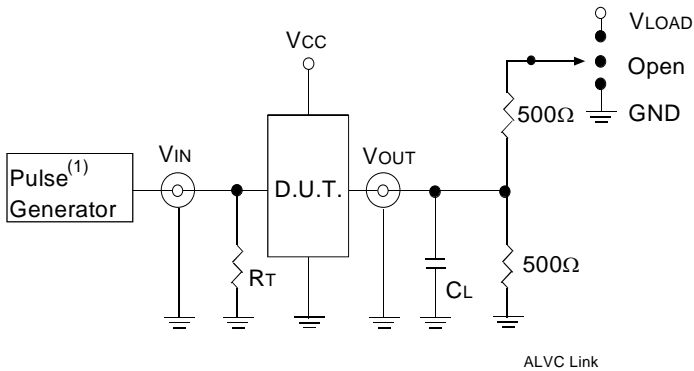
1. See test circuits and waveforms.  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ .
2. This parameter is warranted but not production tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1) = 3.3V ± 0.3V	Unit
V <sub>LOAD</sub>	6	V
V <sub>IH</sub>	2.7	V
V <sub>T</sub>	1.5	V
V <sub>LZ</sub>	300	mV
V <sub>HZ</sub>	300	mV
C <sub>L</sub>	25pF (A Port), 80pF (B Port)	pF

### TEST CIRCUITS FOR ALL OUTPUTS



#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

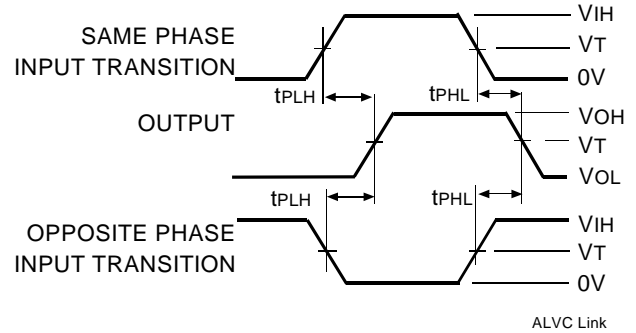
#### NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ .5ns

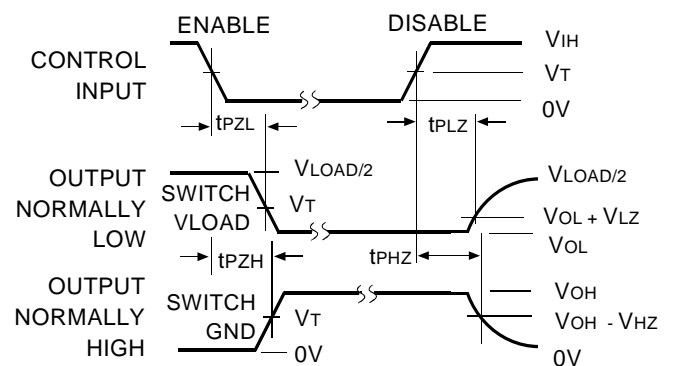
### SWITCH POSITION

Test	Switch
Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

### PROPAGATION DELAY



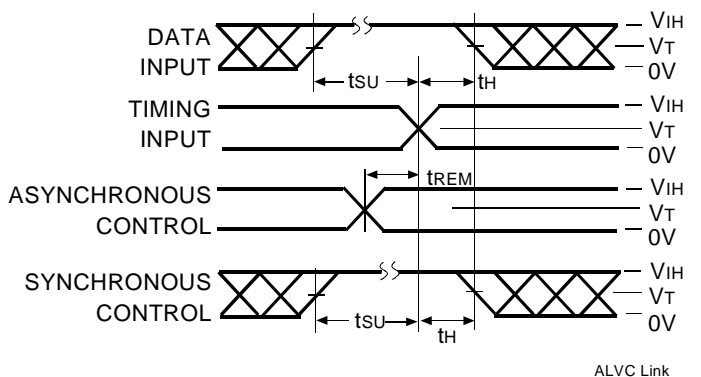
### ENABLE AND DISABLE TIMES



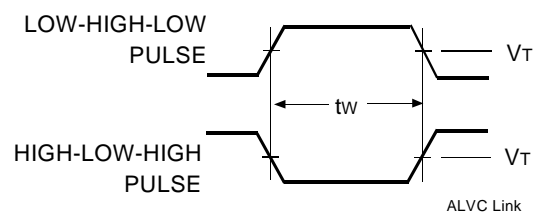
#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

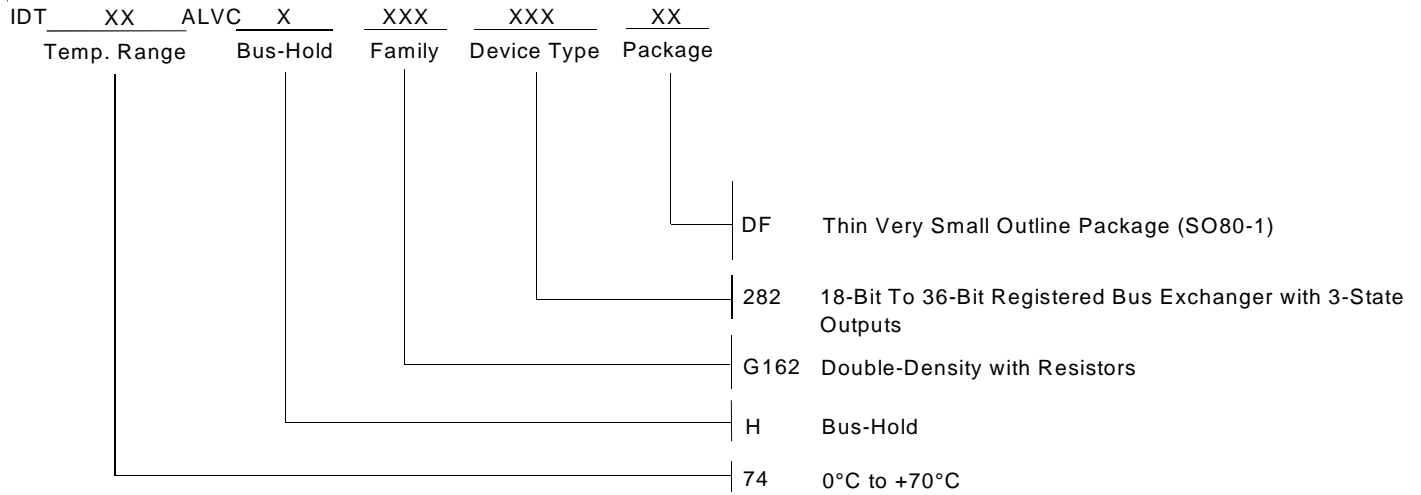
### SET-UP, HOLD, AND RELEASE TIMES



### PULSE WIDTH



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