

25-BIT CONFIGURABLE REGISTERED BUFFER FOR DDR2
ICSSSTUAF32866C

Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VDD operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. ICSSSTUAF32866C operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high, and $\overline{\text{CLK}}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

A - Pair Configuration (C01 = 0, C11 = 1 and C02 = 0, C12 = 1)

Parity that arrives one cycle after the data input to which it applies is checked on the PAR_IN of the first register. The second register produces PPO and QERR signals. The QERR of the first register is left floating. The valid error information is latched on the QERR output of the second register. If an error occurs QERR is latched low for two cycles or until RESET is low.

B - Single Configuration (C0 = 0, C1 = 0)

The device supports low-power standby operation. When the RESET input ($\overline{\text{RESET}}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when RESET is low all registers are reset, and all outputs are forced low. The LVCMOS RESET and Cn inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR-II RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the

design of the ICSSSTUAF32866C must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ input is low, the Qn outputs will function normally. The RESET input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and will force the outputs low. If the $\overline{\text{DCS}}$ -control functionality is not desired, then the $\overline{\text{CSR}}$ input can be hardwired to ground, in which case, the setup-time requirement for $\overline{\text{DCS}}$ would be the same as for the other D data inputs. Package options include 96-ball LFBGA (MO-205CC).

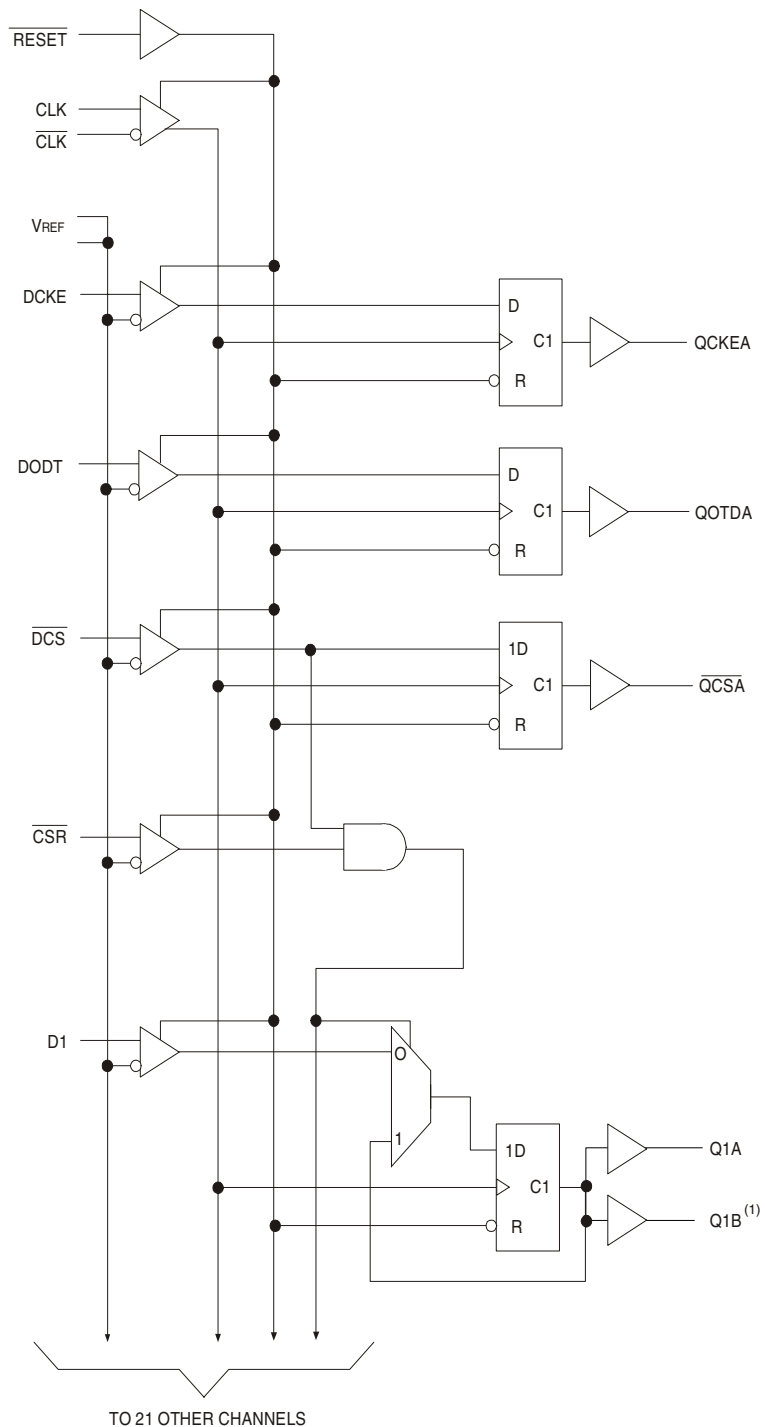
Features

- 25-bit 1:1 or 14-bit 1:2 registered buffer with parity check functionality
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on C0, C1, and RESET inputs
- Low voltage operation: VDD = 1.7V to 1.9V
- Drop-in replacement for ICSSSTUA32864
- Available in 96-ball BGA package

Applications

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS98ULPA877A or IDTCSPUA877A
- Ideal for DDR2 400, 533, and 667

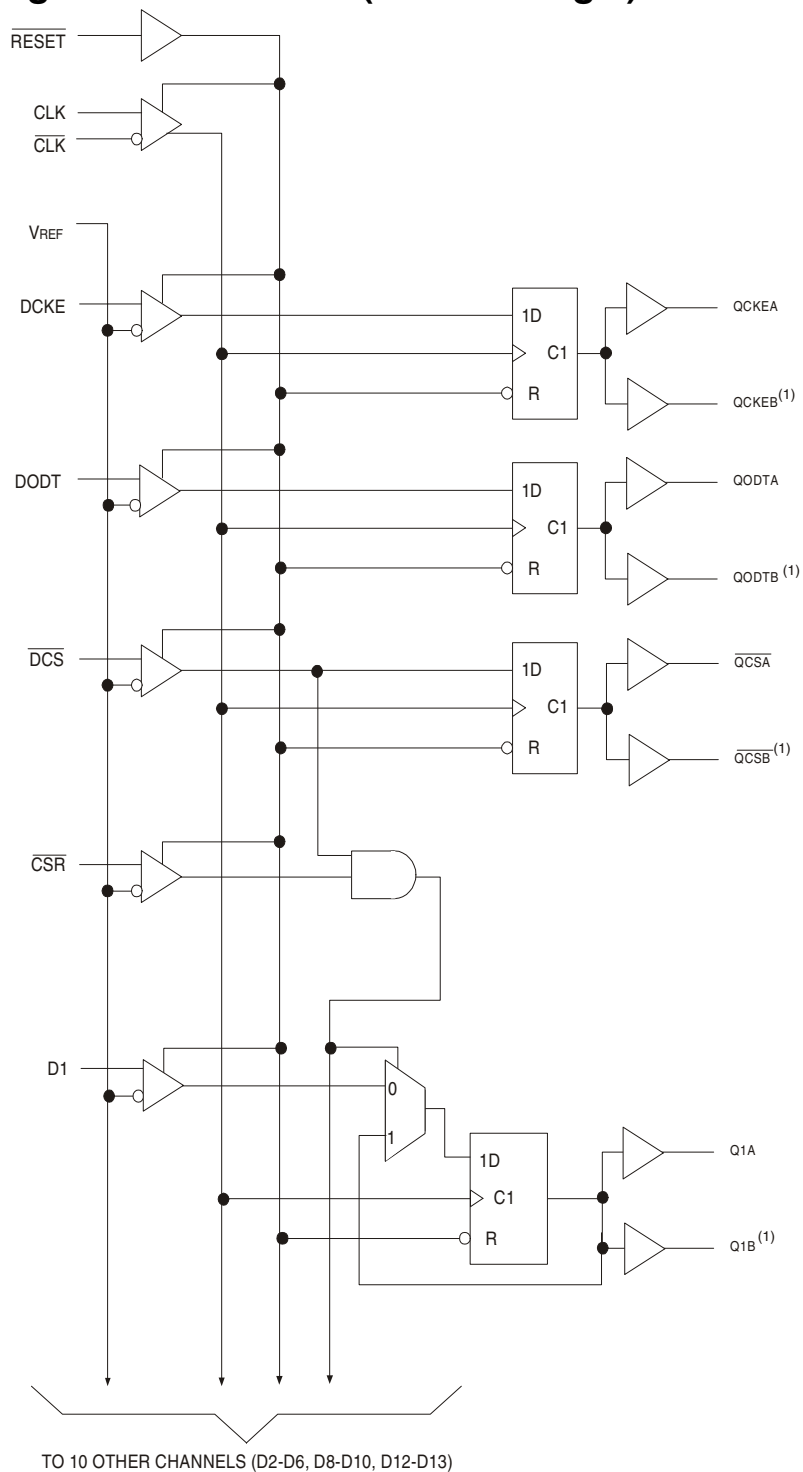
Functional Block Diagram for 1:1 Mode (Positive Logic)



NOTE:

1. Disabled in 1:1 configuration.

Functional Block Diagram for 1:2 Mode (Positive Logic)



NOTE:

1. Disabled in 1:1 configuration.

Pin Configurations

14 BIT 1:2 REGISTERS

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------|--------------------|------|-----|-------------------|-------------------|
| A | DCKE | PPO | VREF | VDD | QCKEA | QCKEB |
| B | D2 | NC | GND | GND | Q2A | Q2B |
| C | D3 | NC | VDD | VDD | Q3A | Q3B |
| D | D0DT | \overline{QERR} | GND | GND | Q0DTA | Q0DTB |
| E | D5 | NC | VDD | VDD | Q5A | Q5B |
| F | D6 | NC | GND | GND | Q6A | Q6B |
| G | PAR_IN | \overline{RESET} | VDD | VDD | C1 | C0 |
| H | CLK | \overline{DCS} | GND | GND | \overline{QCSA} | \overline{QCSB} |
| J | \overline{CLK} | \overline{CSR} | VDD | VDD | ZOH | ZOL |
| K | D8 | NC | GND | GND | Q8A | Q8B |
| L | D9 | NC | VDD | VDD | Q9A | Q9B |
| M | D10 | NC | GND | GND | Q10A | Q10B |
| N | D11 | NC | VDD | VDD | Q11A | Q11B |
| P | D12 | NC | GND | GND | Q12A | Q12B |
| R | D13 | NC | VDD | VDD | Q13A | Q13B |
| T | D14 | NC | VREF | VDD | Q14A | Q14B |

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------|--------------------|------|-----|-------------------|-------------------|
| A | D1 | PPO | VREF | VDD | Q1A | Q1B |
| B | D2 | NC | GND | GND | Q2A | Q2B |
| C | D3 | NC | VDD | VDD | Q3A | Q3B |
| D | D4 | \overline{QERR} | GND | GND | Q4A | Q4B |
| E | D5 | NC | VDD | VDD | Q5A | Q5B |
| F | D6 | NC | GND | GND | Q6A | Q6B |
| G | PAR_IN | \overline{RESET} | VDD | VDD | C1 | C0 |
| H | CLK | \overline{DCS} | GND | GND | \overline{QCSA} | \overline{QCSB} |
| J | \overline{CLK} | \overline{CSR} | VDD | VDD | ZOH | ZOL |
| K | D8 | NC | GND | GND | Q8A | Q8B |
| L | D9 | NC | VDD | VDD | Q9A | Q9B |
| M | D10 | NC | GND | GND | Q10A | Q10B |
| N | D0DT | NC | VDD | VDD | Q0DTA | Q0DTB |
| P | D12 | NC | GND | GND | Q12A | Q12B |
| R | D13 | NC | VDD | VDD | Q13A | Q13B |
| T | DCKE | NC | VREF | VDD | QCKEA | QCKEB |

REGISTER A (C0 = 0, C1 = 1)

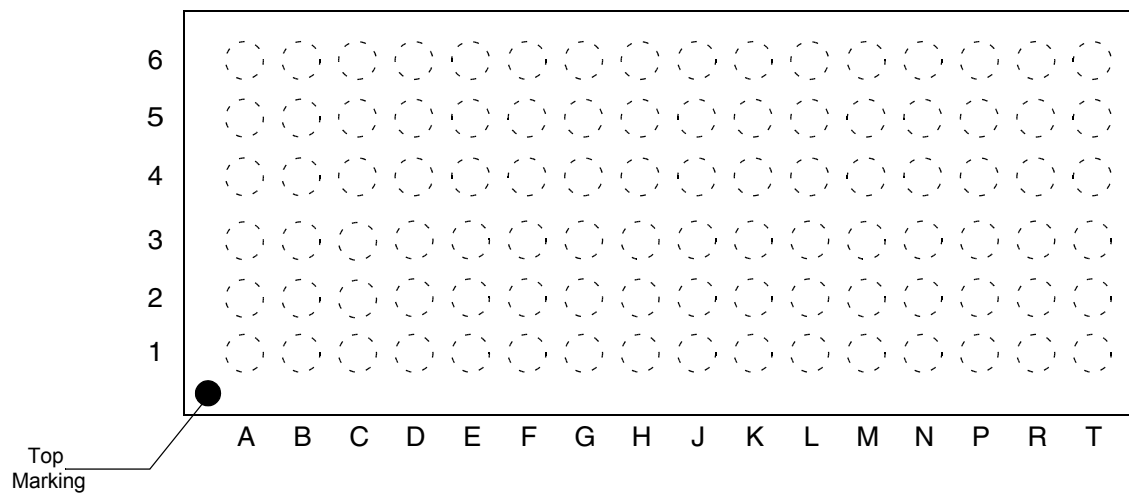
REGISTER B (C0 = 1, C1 = 1)

25 BIT 1:1 REGISTER

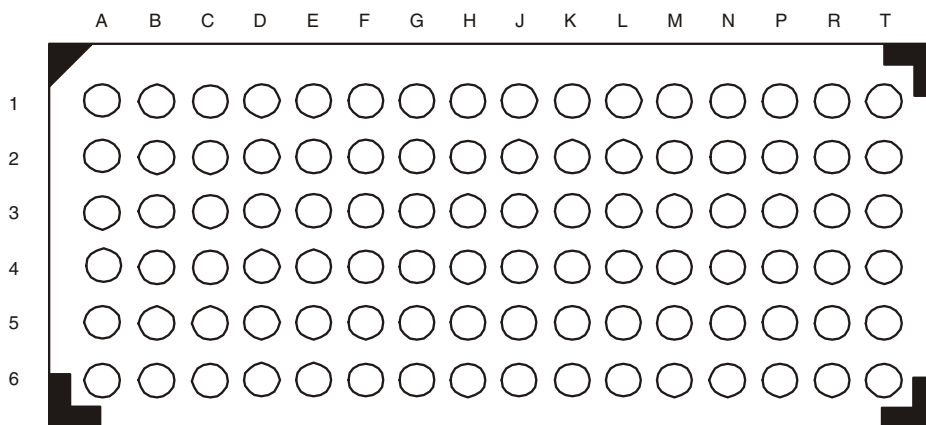
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------|--------------------|------|-----|------------------|-----|
| A | DCKE | PPO | VREF | VDD | QCKE | NC |
| B | D2 | D15 | GND | GND | Q2 | Q15 |
| C | D3 | D16 | VDD | VDD | Q3 | Q16 |
| D | D0DT | \overline{QERR} | GND | GND | Q0DT | NC |
| E | D5 | D17 | VDD | VDD | Q5 | Q17 |
| F | D6 | D18 | GND | GND | Q6 | Q18 |
| G | PAR_IN | \overline{RESET} | VDD | VDD | C1 | C0 |
| H | CLK | \overline{DCS} | GND | GND | \overline{QCS} | NC |
| J | \overline{CLK} | \overline{CSR} | VDD | VDD | ZOH | ZOL |
| K | D8 | D19 | GND | GND | Q8 | Q19 |
| L | D9 | D20 | VDD | VDD | Q9 | Q20 |
| M | D10 | D21 | GND | GND | Q10 | Q21 |
| N | D11 | D22 | VDD | VDD | Q11 | Q22 |
| P | D12 | D23 | GND | GND | Q12 | Q23 |
| R | D13 | D24 | VDD | VDD | Q13 | Q24 |
| T | D14 | D25 | VREF | VDD | Q14 | Q25 |

C0 = 0, C1 = 0

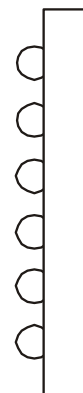
96 Ball LFBGA Package Attributes



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Function Table

| Inputs ¹ | | | | | | Outputs | | |
|---------------------------|-------------------------|-------------------------|------------------|-------------------------|-------------------|---------|-------------------------|---------------|
| $\overline{\text{RESET}}$ | $\overline{\text{DCS}}$ | $\overline{\text{CSR}}$ | CLK | $\overline{\text{CLK}}$ | Dn, DODT, DCKE | Qn | $\overline{\text{QCS}}$ | QODT, QCKE |
| H | L | L | ↑ | ↓ | L | L | L | L |
| H | L | L | ↑ | ↓ | H | H | L | H |
| H | L | L | L or H | L or H | X | Q_0^2 | Q_0^2 | Q_0^2 |
| H | L | H | ↑ | ↓ | L | L | L | L |
| H | L | H | ↑ | ↓ | H | H | L | H |
| H | L | H | L or H | L or H | X | Q_0^2 | Q_0^2 | Q_0^2 |
| H | H | L | ↑ | ↓ | L | L | H | L |
| H | H | L | ↑ | ↓ | H | H | H | H |
| H | H | L | L or H | L or H | X | Q_0^2 | Q_0^2 | Q_0^2 |
| H | H | H | ↑ | ↓ | L | Q_0^2 | H | L |
| H | H | H | ↑ | ↓ | H | Q_0^2 | H | H |
| H | H | H | L or H | L or H | X | Q_0^2 | Q_0^2 | Q_0^2 |
| L | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | L | L | L |

1 H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↑ = LOW to HIGH

↓ = HIGH to LOW

2 Output level before the indicated steady-state conditions were established.

Parity and Standby Function Table

| Inputs ¹ | | | | | | | Outputs | |
|---------------------------|-------------------------|-------------------------|------------------|-------------------------|--------------------------------------|---------------------|-------------------------|---------------------------------------|
| $\overline{\text{RESET}}$ | $\overline{\text{DCS}}$ | $\overline{\text{CSR}}$ | CLK | $\overline{\text{CLK}}$ | Σ of Inputs = H (D1 - D25) | PAR_IN ² | $\overline{\text{PPO}}$ | $\overline{\text{QERR}}$ ³ |
| H | L | X | ↑ | ↓ | Even | L | L | H |
| H | L | X | ↑ | ↓ | Odd | L | H | L |
| H | L | X | ↑ | ↓ | Even | H | H | L |
| H | L | X | ↑ | ↓ | Odd | H | L | H |
| H | X | L | ↑ | ↓ | Even | L | L | H |
| H | X | L | ↑ | ↓ | Odd | L | H | L |
| H | X | L | ↑ | ↓ | Even | H | H | L |
| H | X | L | ↑ | ↓ | Odd | H | L | H |
| H | H | H | ↑ | ↓ | X | X | PPO ₀ | $\overline{\text{QERR}}_0$ |
| H | X | X | L or H | L or H | X | X | PPO ₀ | $\overline{\text{QERR}}_0$ |
| L | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating | L | H |

1 H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↑ = LOW to HIGH

↓ = HIGH to LOW

Data Inputs = D2, D3, D5, D6, D8 - D25 when C0 = 0 and C1 = 0.

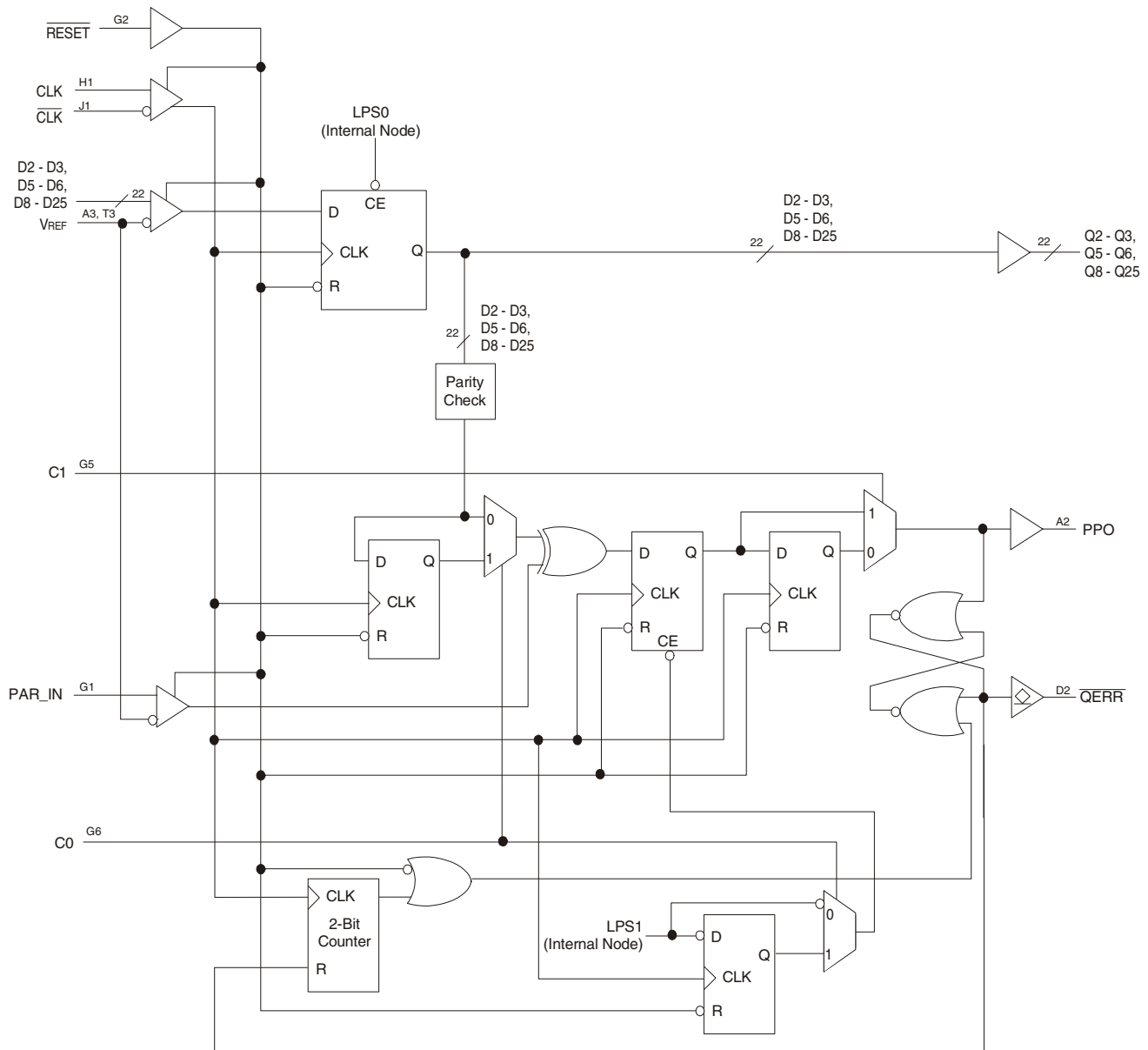
Data Inputs = D2, D3, D5, D6, D8 - D14 when C0 = 0 and C1 = 1.

Data Inputs = D1 - D6, D8 - D10, D12, D13 when C0 = 1 and C1 = 1.

2 PAR_IN arrives one clock cycle after the data to which it applies when C0 = 0, and two clock cycles when C0 = 1.

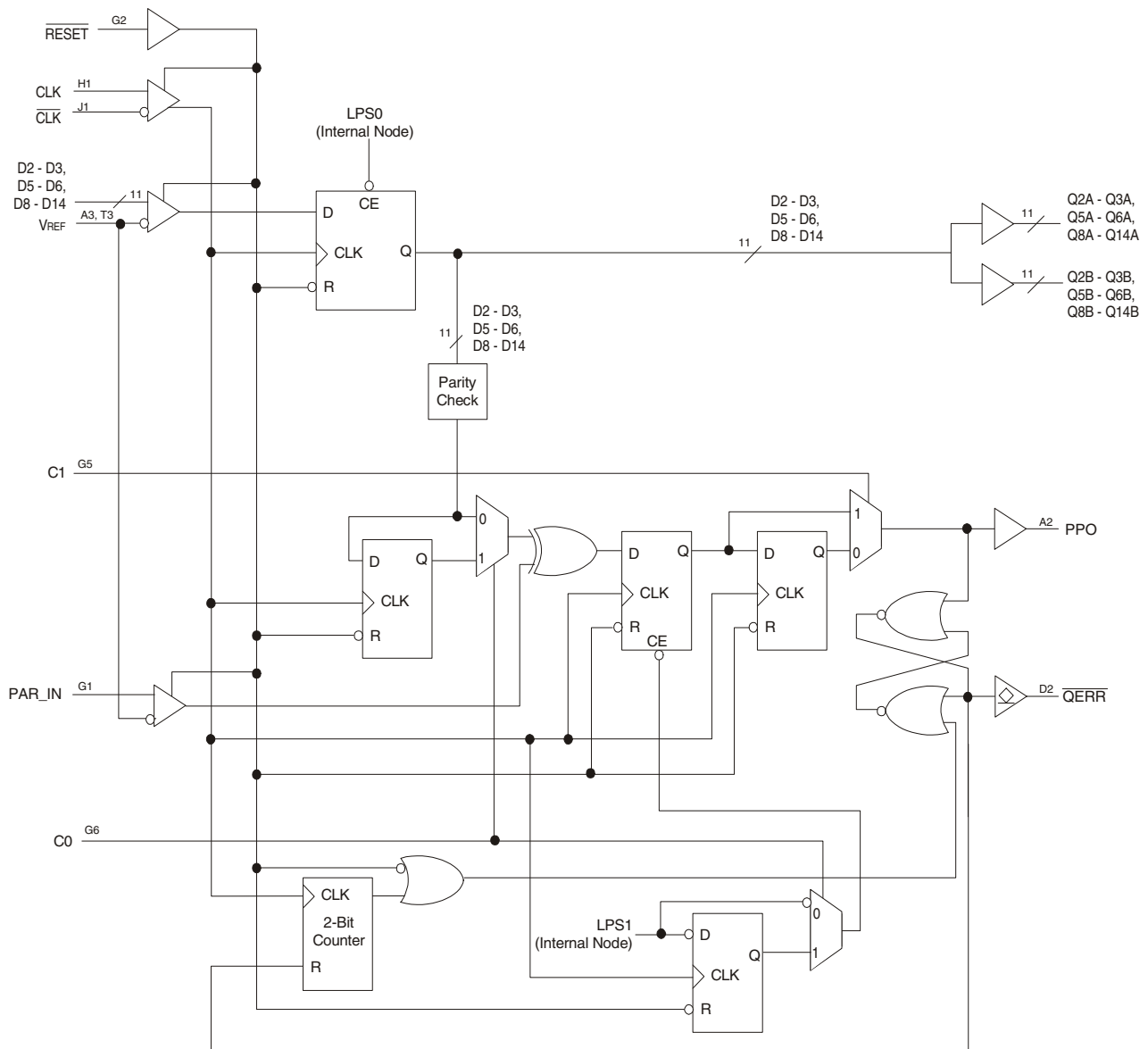
3 This transition assumes $\overline{\text{QERR}}$ is HIGH at the crossing of CLK going HIGH and $\overline{\text{CLK}}$ going LOW. If $\overline{\text{QERR}}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{\text{RESET}}$ is driven LOW.

Logic Diagram (1:1)



Parity Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0

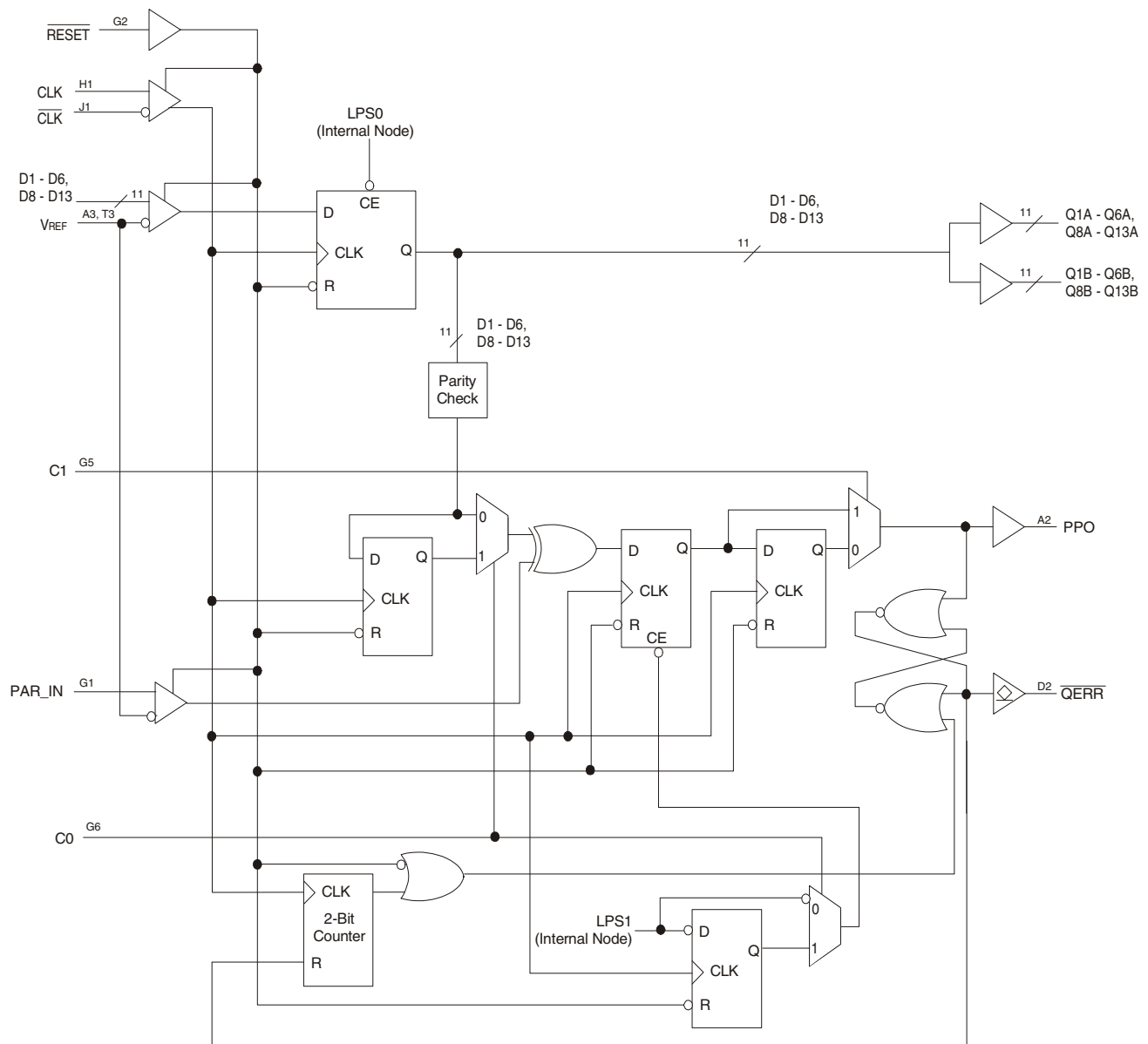
Logic Diagram (1:2)



Parity Logic Diagram for 1:2 Register - A Configuration (Positive Logic);

C0 = 0, C1 = 1

Logic Diagram (1:2)



Parity Logic Diagram for 1:2 Register - B Configuration (Positive Logic);

C0 = 1, C1 = 1

Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Item | | Rating |
|---|--------------|---------------------|
| Supply Voltage, VDD | | -0.5V to 2.5V |
| Input Voltage Range, Vi ¹ | | -0.5V to 2.5V |
| Output Voltage Range, Vo ^{1,2} | | -0.5V to VDD + 0.5V |
| Input Clamp Current, I _{IK} | | ±50mA |
| Output Clamp Current, I _{OK} | | ±50mA |
| Continuous Output Clamp Current, I _O | | ±50mA |
| Continuous Current through each VDD or GND | | ±100mA |
| Package Thermal Impedance (θ _{JA}) ³ | 0m/s Airflow | 70.9°C/W |
| | 1m/s Airflow | 65°C/W |
| Storage Temperature | | -65 to +150°C |

1 The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.

2 This current will flow only when the output is in the high state level Vo > VDDQ.

3 The package thermal impedance is calculated in accordance with JESD 51.

Terminal Functions

| Terminal Name | Electrical Characteristics | Description |
|---|----------------------------|--|
| GND | Ground Input | Ground |
| VDD | 1.8V nominal | Power Supply Voltage |
| VREF | 0.9V nominal | Input Reference Clock |
| ZOH | Input | Reserved for future use |
| ZOL | Input | Reserved for future use |
| CLK | Differential Input | Positive Master Clock Input |
| $\overline{\text{CLK}}$ | Differential Input | Negative Master Clock Input |
| C0, C1 | LVC MOS Input | Configuration Control Inputs |
| $\overline{\text{RESET}}$ | LVC MOS Input | Asynchronous Reset Input. Resets registers and disables VREF data and clock differential-input receivers. |
| $\overline{\text{CSR}}$, $\overline{\text{DCS}}$ | SSTL_18 Input | Chip Select Inputs. Disables outputs D1 - D24 output switching when both inputs are HIGH. |
| D1 - D25 | SSTL_18 Input | Data Input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$. |
| DODT | SSTL_18 Input | The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls |
| DCKE | SSTL_18 Input | The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls |
| Q1 - Q25 | 1.8V CMOS | Data Outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls |
| $\overline{\text{QCS}}$ | 1.8V CMOS | Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls |
| QODT | 1.8V CMOS | Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls |
| QCKE | 1.8V CMOS | Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls |
| PPO | 1.8V CMOS | Partial Parity Output. Indicates off parity of D1 - D25 |
| PAR_IN | SSTL_18 Input | Parity Input arrives one cycle after corresponding data input |
| $\overline{\text{QERR}}$ | Open Drain Output | Output Error bit, generated one cycle after the corresponding data output |

Operating Characteristics

The $\overline{\text{RESET}}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is LOW.

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|--------|---|--|--------------|-----------|--------------|-------|
| VDDQ | I/O Supply Voltage | | 1.7 | | 1.9 | V |
| VREF | Reference Voltage | | 0.49 * VDD | 0.5 * VDD | 0.51 * VDD | V |
| VTT | Termination Voltage | | VREF - 0.04 | VREF | VREF + 0.04 | V |
| VI | Input Voltage | | 0 | | VDD | V |
| VIH | AC High-Level Input Voltage | Data, $\overline{\text{CSR}}$, and PAR_IN inputs | VREF + 0.25 | | | V |
| VIL | AC Low-Level Input Voltage | | | | VREF - 0.25 | |
| VIH | DC High-Level Input Voltage | | VREF + 0.125 | | | |
| VIL | DC Low-Level Input Voltage | | | | VREF - 0.125 | |
| VIH | High-Level Input Voltage | $\overline{\text{RESET}}$, C0, C1 | 0.65 * VDDQ | | | V |
| VIL | Low-Level Input Voltage | | | | 0.35 * VDDQ | |
| VICR | Common Mode Input Range | CLK, $\overline{\text{CLK}}$ | 0.675 | | 1.125 | V |
| VID | Differential Input Voltage | | 600 | | | mV |
| IOH | High-Level Output Current | | | | -8 | mA |
| IOL | Low-Level Output Current | | | | 8 | |
| IERROL | $\overline{\text{QERR}}$ LOW Level Output Current | | 25 | | | mA |
| TA | Operating Free-Air Temperature | | 0 | | +70 | °C |

DC Electrical Characteristics Over Operating Range

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{DD} = 1.7\text{V}$ to 1.9V .

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Units |
|-------------|--|--|----------|------|------|------|-------------------------------------|
| V_{IK} | | $I_I = -18\text{mA}$ | | | | -1.2 | V |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -6\text{mA}$ | | 1.2 | | | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 6\text{mA}$ | | | | 0.5 | V |
| V_{ERROL} | \overline{QERR} Output LOW Voltage | $I_{ERROL} = 25\text{mA}$, $V_{DD} = 1.7\text{V}$ | | | | 0.5 | V |
| I_{IL} | All Inputs | $V_I = V_{DD}$ or GND; $V_{DD} = 1.9\text{V}$ | | -5 | | +5 | μA |
| I_{DD} | Static Standby | $I_O = 0$, $V_{DD} = 1.9\text{V}$, $\overline{RESET} = \text{GND}$ | | | | 100 | μA |
| | Static Operating | $I_O = 0$, $V_{DD} = 1.9\text{V}$, $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $\text{CLK} = \overline{\text{CLK}} = V_{IH(AC)}$ or $V_{IL(AC)}$ | | | | 10 | mA |
| | | $I_O = 0$, $V_{DD} = 1.9\text{V}$, $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $\text{CLK} = V_{IH(AC)}$, $\overline{\text{CLK}} = V_{IL(AC)}$ | | | 90 | | |
| I_{DDD} | Dynamic Operating (clock only) | $I_O = 0$, $V_{DD} = 1.8\text{V}$, $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle | | | 210 | | $\mu\text{A/Clock MHz}$ |
| | Dynamic Operating (per each data input) | $I_O = 0$, $V_{DD} = 1.8\text{V}$, $\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. | 1:1 mode | | 65 | | $\mu\text{A/Clock MHz/ Data Input}$ |
| | | | 1:2 mode | | 120 | | |
| C_{IN} | Data Inputs | $V_I = V_{REF} \pm 350\text{mV}$ | | 2 | | 3 | pF |
| | CLK and $\overline{\text{CLK}}$ | $V_{ICR} = 1.25\text{V}$, $V_{IPP} = 360\text{mV}$ | | 2 | | 3 | |
| | \overline{RESET} | $V_I = V_{DD}$ or GND | | | 5 | | |

Timing Requirements Over Recommended Operating Free-Air Temperature Range

| Symbol | Parameter | V _{DD} = 1.8V ± 0.1V | | Units |
|---------------------------------|--|--|------|-------|
| | | Min. | Max. | |
| f _{CLOCK} | Clock Frequency | | 410 | MHz |
| t _W | Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW | 1 | | ns |
| t _{ACT} ¹ | Differential Inputs Active Time | | 10 | ns |
| t _{INACT} ² | Differential Inputs Inactive Time | | 15 | ns |
| t _{SU} | Setup Time | $\overline{\text{DCS}}$ before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow , $\overline{\text{CSR}}$ HIGH; $\overline{\text{CSR}}$ before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow , $\overline{\text{DCS}}$ HIGH | 0.7 | ns |
| | | $\overline{\text{DCS}}$ before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow , $\overline{\text{CSR}}$ LOW | 0.5 | |
| | | DODT, DODKE, and data before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow | 0.5 | |
| | | PAR_IN before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow | 0.5 | |
| t _H | Hold Time | $\overline{\text{DCS}}$, DODT, DODKE, and data after CLK \uparrow , $\overline{\text{CLK}}$ \downarrow | 0.5 | ns |
| | | PAR_IN after CLK \uparrow , $\overline{\text{CLK}}$ \downarrow | 0.5 | |

1 VREF must be held at a valid input voltage level and data inputs must be held at valid logic levels for a minimum time of t_{ACT}(max) after RESET is taken HIGH.

2 VREF, data, and clock inputs must be held at a valid input voltage levels (not floating) for a minimum time of t_{INACT}(max) after RESET is taken LOW.

Switching Characteristics Over Recommended Free Air Operating Range (unless otherwise noted)

| Symbol | Parameter | V _{DD} = 1.8V ± 0.1V | | Units |
|--------------------|---|-------------------------------|------|-------|
| | | Min. | Max. | |
| f _{MAX} | Max Input Clock Frequency | 410 | | MHz |
| t _{PDM} | Propagation Delay, single bit switching, CLK \uparrow to $\overline{\text{CLK}}$ \downarrow to Q _n | 1.3 | 1.9 | ns |
| t _{PDMSS} | Propagation Delay, simultaneous switching, CLK \uparrow to $\overline{\text{CLK}}$ \downarrow to Q _n | | 2 | ns |
| t _{PD} | Propagation Delay, CLK and $\overline{\text{CLK}}$ to PPO | 0.5 | 1.7 | ns |
| t _{LH} | LOW to HIGH Propagation Delay, CLK \uparrow to $\overline{\text{CLK}}$ \downarrow to $\overline{\text{QERR}}$ | 1.2 | 3 | ns |
| t _{HL} | HIGH to LOW Propagation Delay, CLK \uparrow to $\overline{\text{CLK}}$ \downarrow to $\overline{\text{QERR}}$ | 1 | 2.4 | ns |
| t _{PHL} | HIGH to LOW Propagation Delay, $\overline{\text{RESET}}$ \downarrow to PPO to Q _n \downarrow | | 3 | ns |
| t _{PLH} | LOW to HIGH Propagation Delay, $\overline{\text{RESET}}$ \downarrow to $\overline{\text{QERR}}$ \uparrow | | 3 | ns |

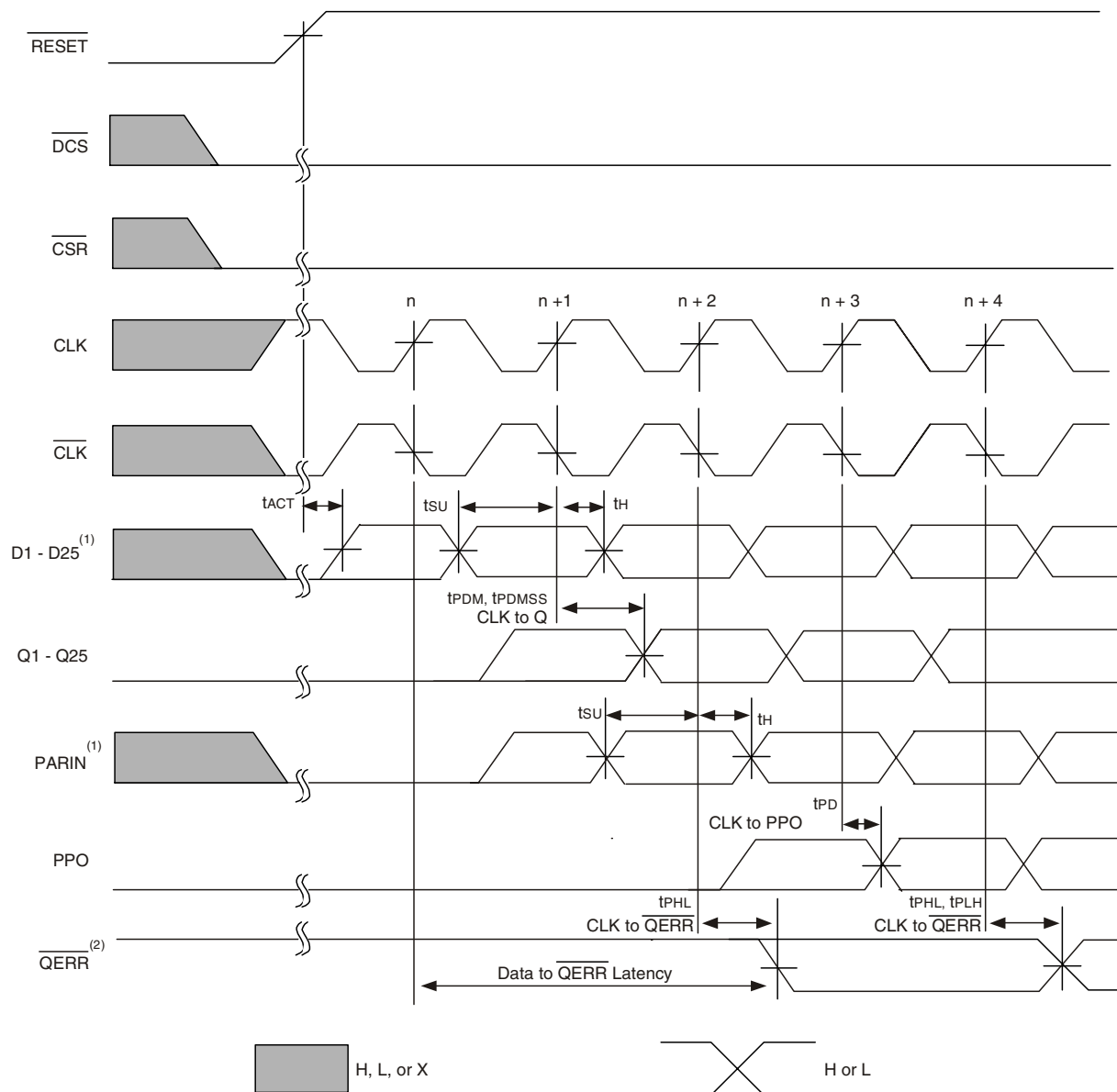
Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range

| Parameter | V _{DD} = 1.8V ± 0.1V | | Units |
|---------------------------------|-------------------------------|------|-------|
| | Min. | Max. | |
| dV/dt _r | 1 | 4 | V/ns |
| dV/dt _f | 1 | 4 | V/ns |
| dV/dt _Δ ¹ | | 1 | V/ns |

1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

Register Timing

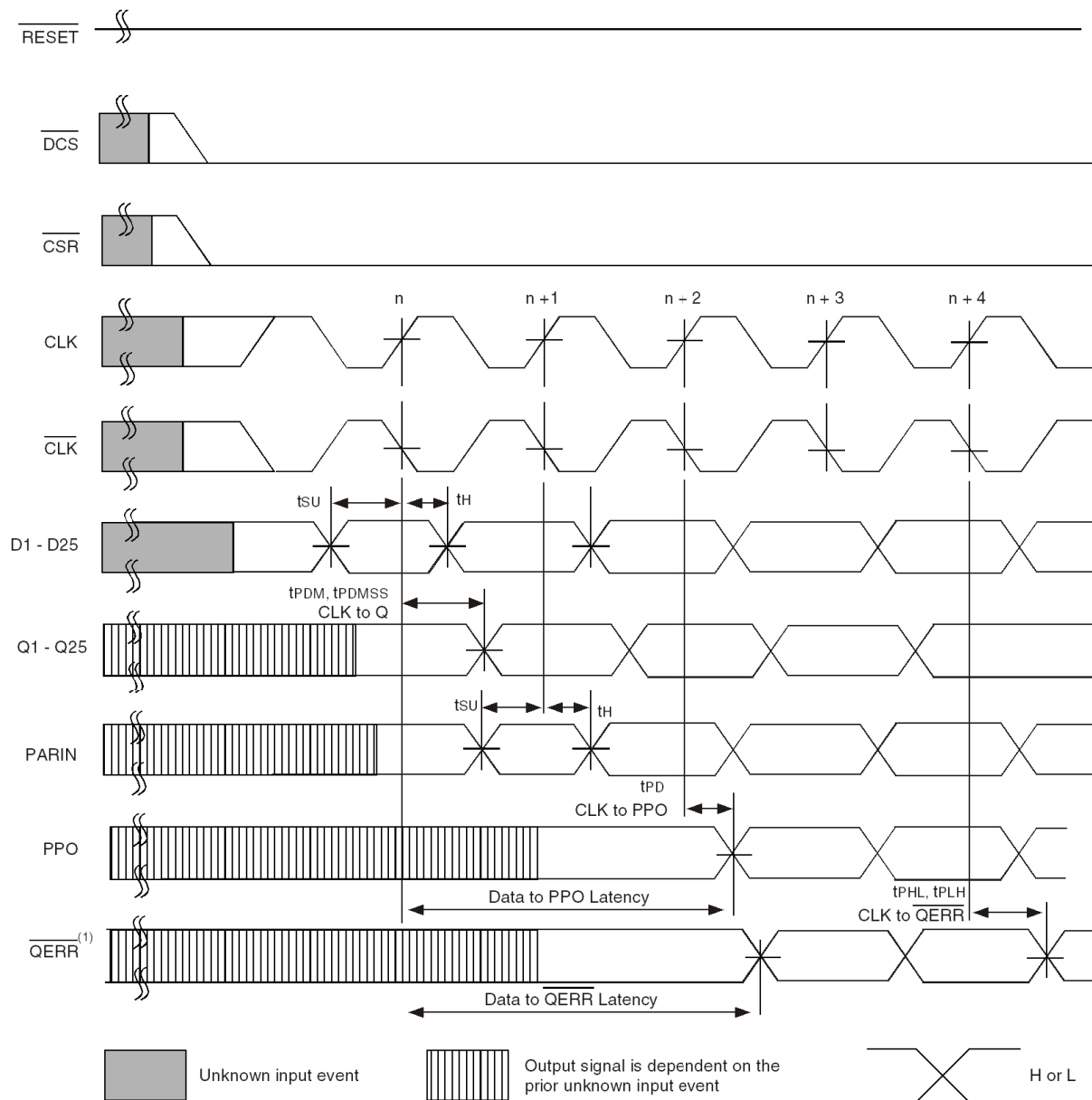


Timing Diagram for SSTUAF32866C Used as a Single Device; C0 = 0, C1 = 0, \overline{RESET} Switches from L to H

NOTES:

1. After \overline{RESET} is switched from LOW to HIGH, all data and PAR_IN inputs signals must be set and held low for a minimum time of t_{ACTMAX} , to avoid false error.
2. If the data is clocked in on the n clock pulse, the \overline{QERR} output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse.

Register Timing

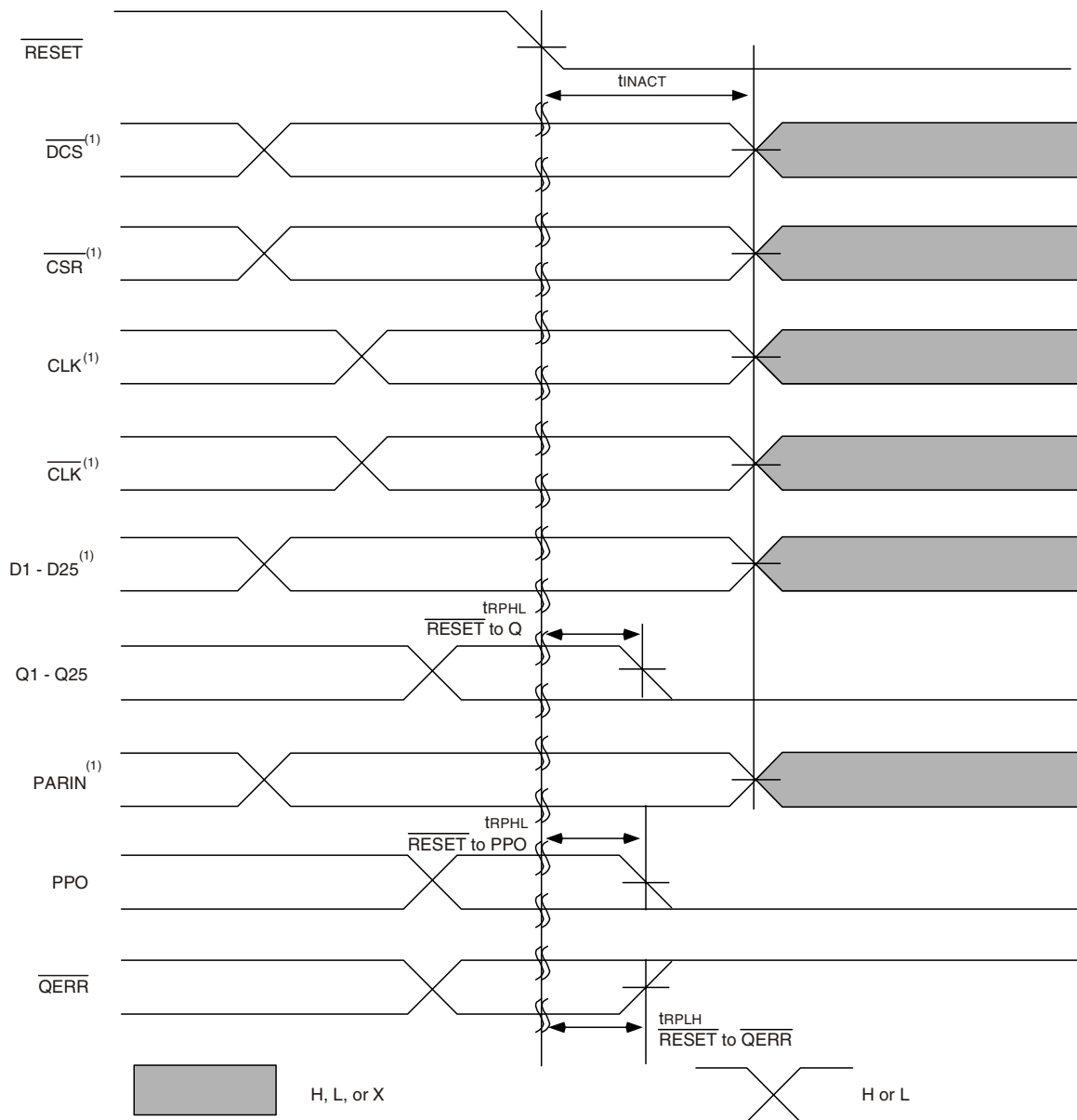


Timing Diagram for the First SSTUAF32866C Used as a Single Device; C0 = 0, C1 = 0, $\overline{\text{RESET}}$ Held HIGH

NOTE:

1. If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

Register Timing

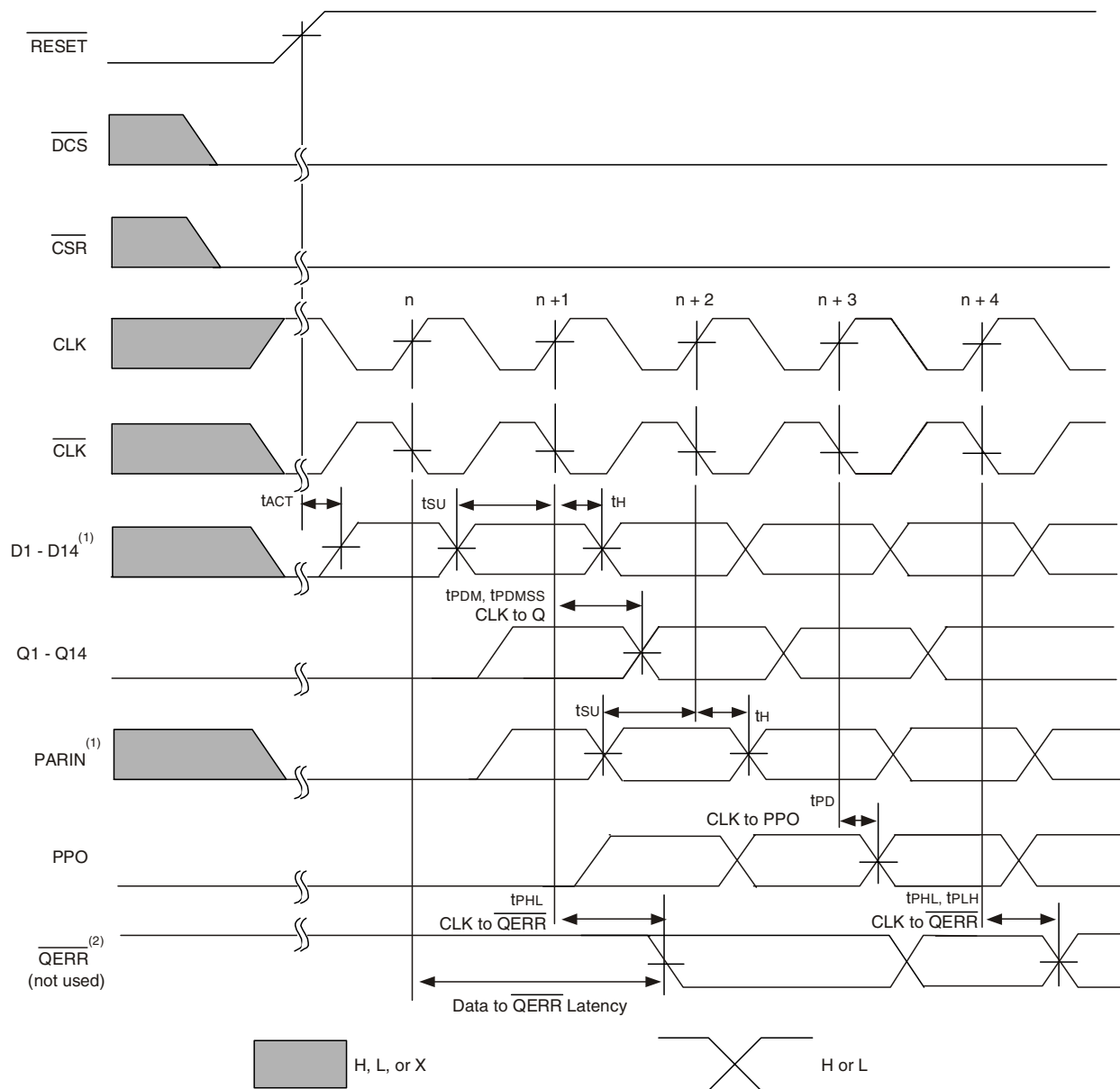


Timing Diagram for SSTUAF32866C Used as a Single Device; C0 = 0, C1 = 0, $\overline{\text{RESET}}$ Switches from H to L

NOTE:

1. After $\overline{\text{RESET}}$ is switched from HIGH to LOW, all data and clock inputs signals must be set and held at valid logic levels (not floating) for a minimum time of **tINACTMAX**.

Register Timing

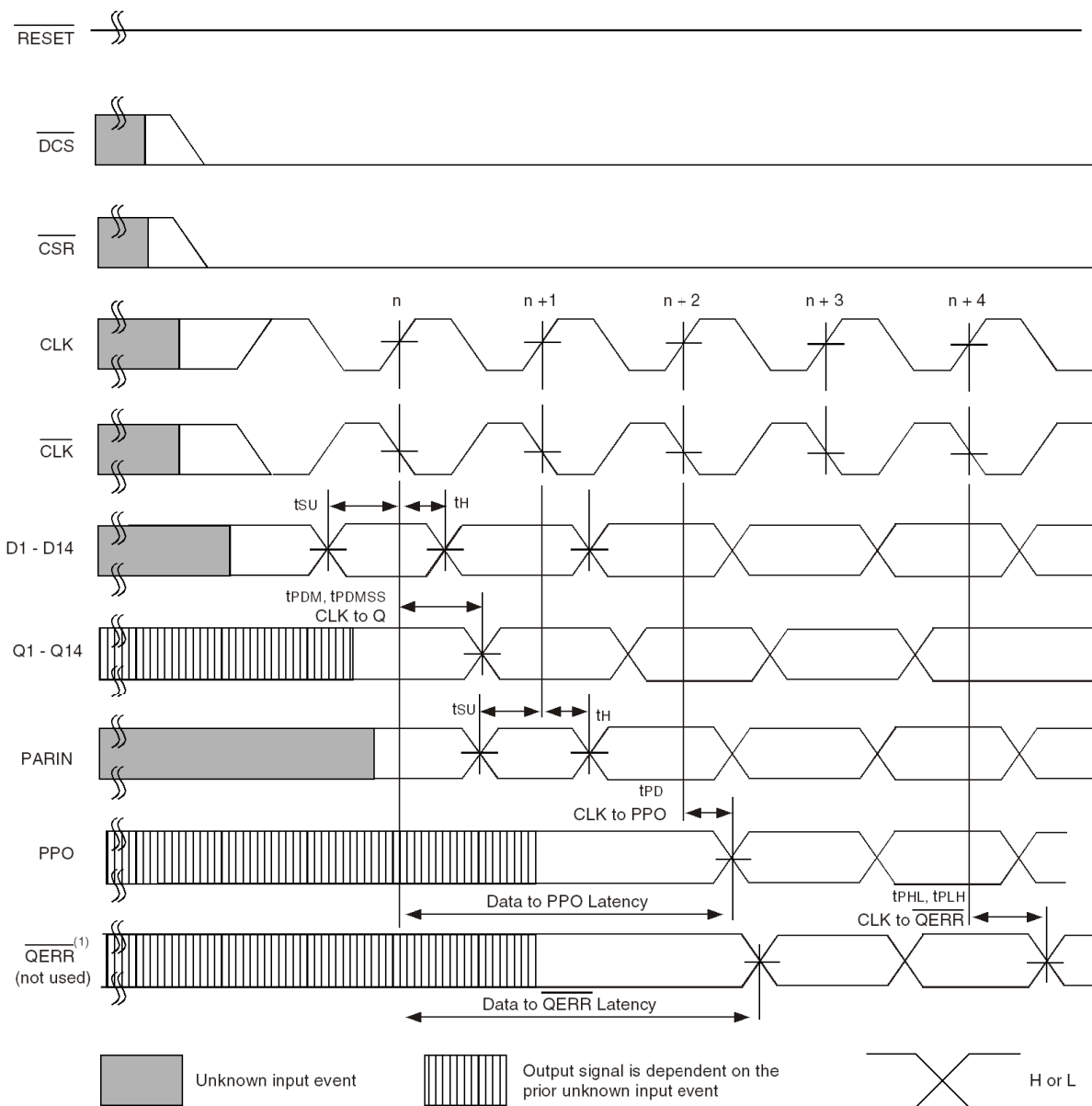


Timing Diagram for the First SSTUAF32866C (1:2 Register-A Configuration) Device Used in a Pair; C0 = 0, C1 = 1, \overline{RESET} Switches from L to H

NOTES:

1. After \overline{RESET} is switched from LOW to HIGH, all data and PAR_IN inputs signals must be set and held low for a minimum time of t_{ACTMAX} , to avoid false error.
2. If the data is clocked in on the n clock pulse, the \overline{QERR} output signal will be generated on the n+1 clock pulse, and it will be valid on the n+2 clock pulse.

Register Timing

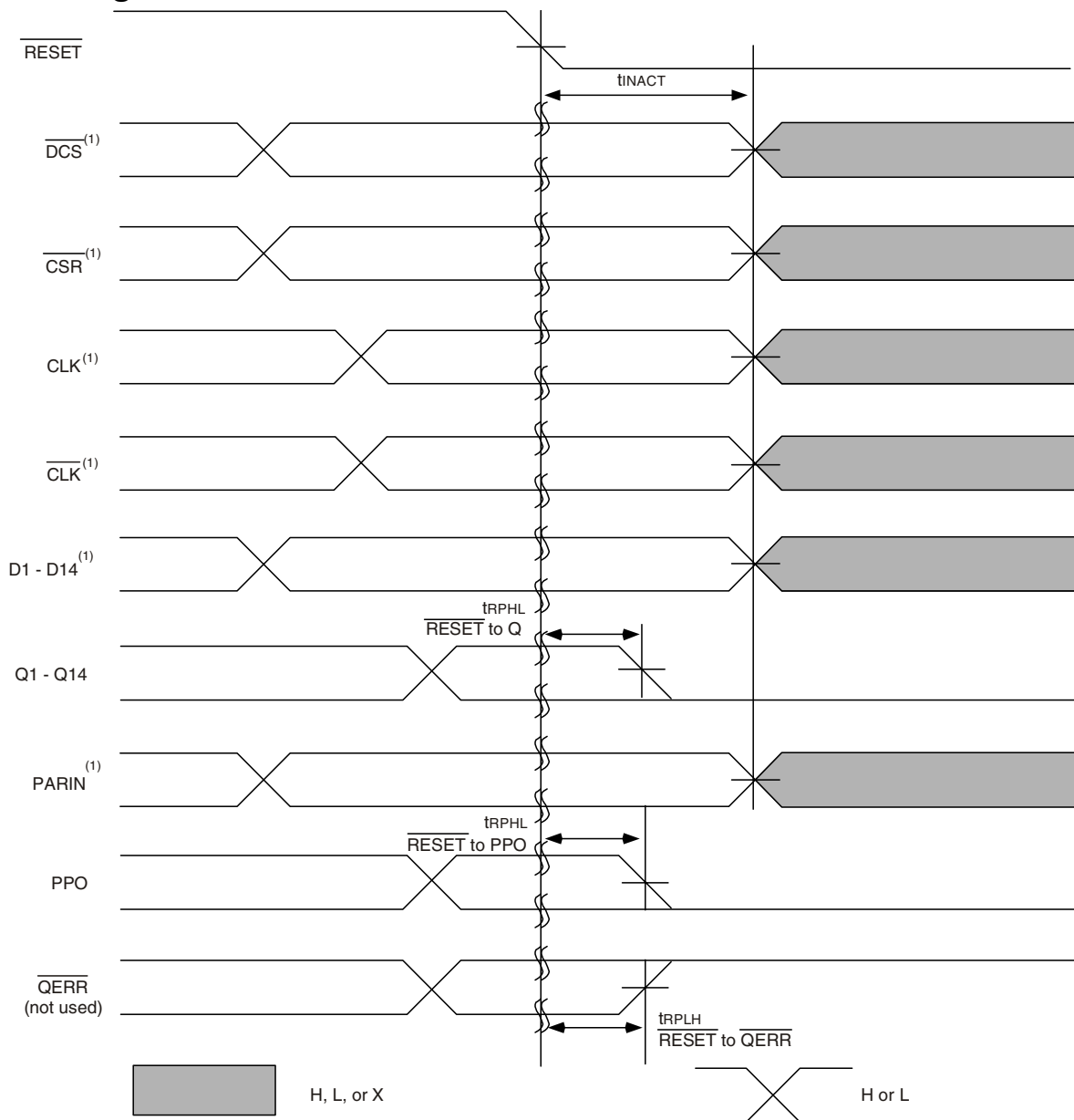


Timing Diagram for the First SSTUAF32866C (1:2 Register-A Configuration) Device Used in a Pair; C0 = 0, C1 = 1, $\overline{\text{RESET}}$ Held HIGH

NOTE:

1. If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the $n+1$ clock pulse, and it will be valid on the $n+2$ clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

Register Timing

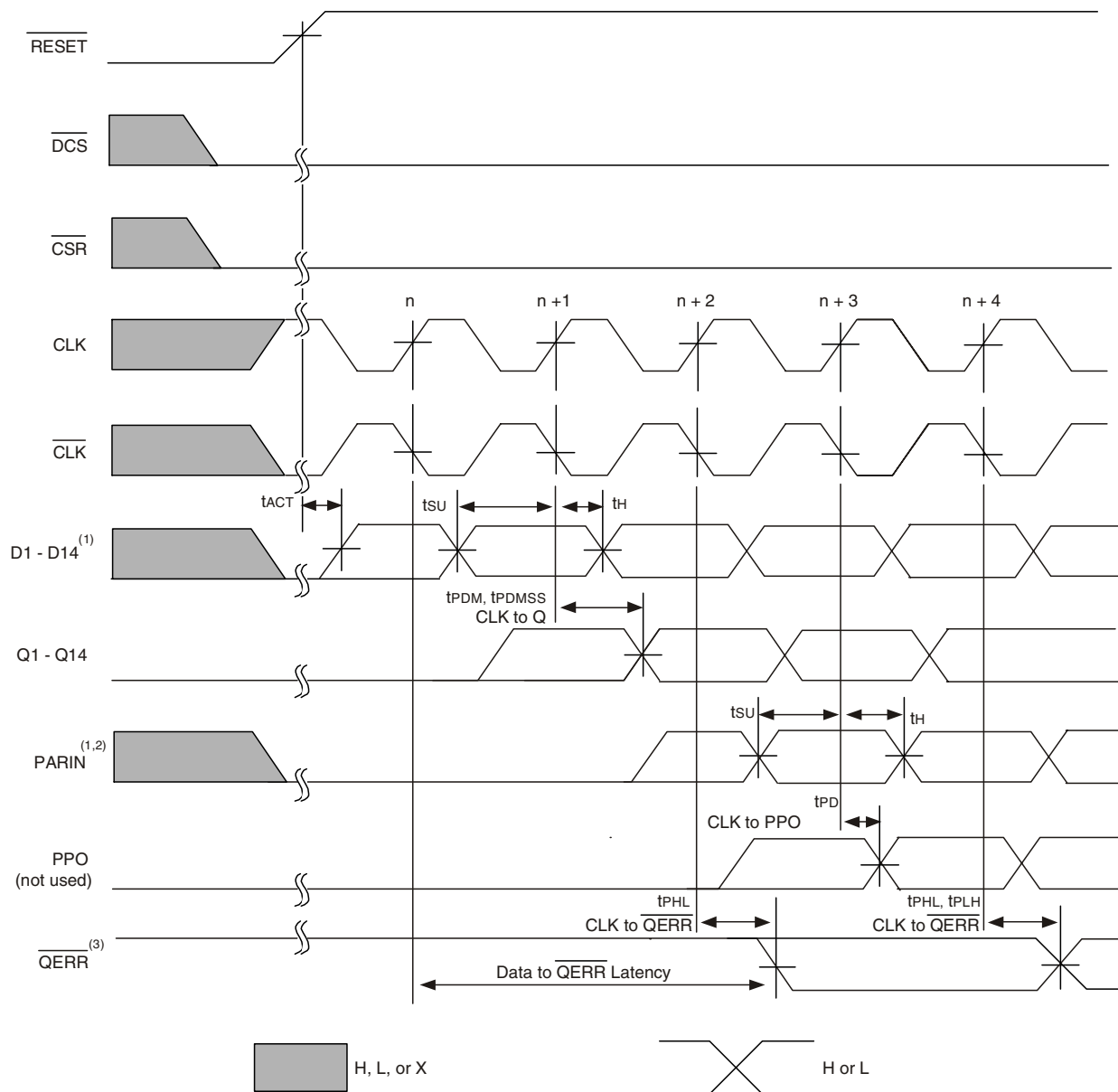


Timing Diagram for the First SSTUAF32866C (1:2 Register-A Configuration) Device Used in a Pair; C0 = 1, C1 = 1; RESET Switches from H to L

NOTE:

1. After RESET is switched from HIGH to LOW, all data and clock inputs signals must be set and held at valid logic levels (not floating) for a minimum time of $t_{INACTMAX}$.

Register Timing

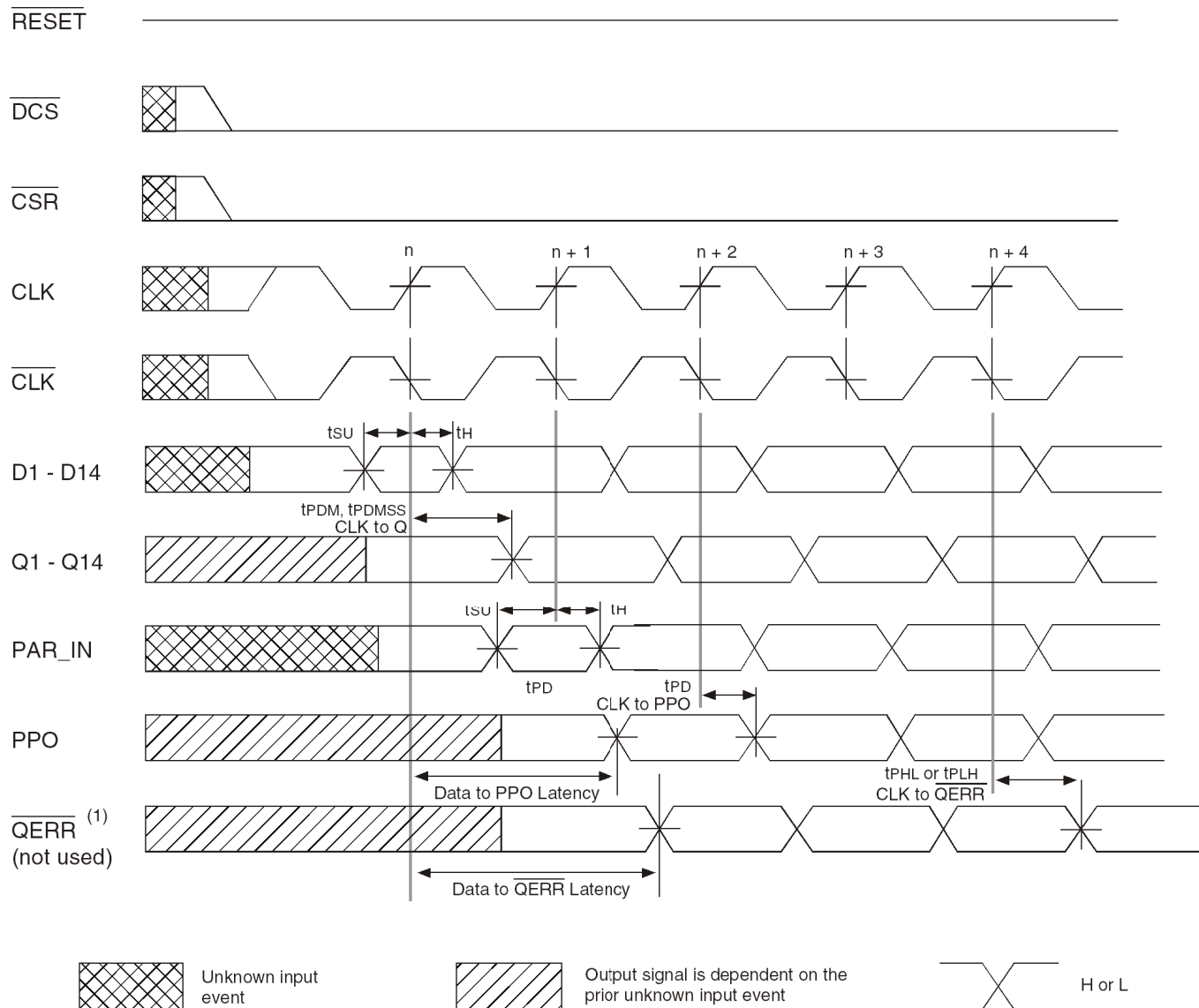


Timing Diagram for the Second SSTUAF32866C (1:2 Register-B Configuration) Device Used in a Pair; C0 = 1, C1 = 1, RESET Switches from L to H

NOTES:

1. After RESET is switched from LOW to HIGH, all data and PAR_IN inputs signals must be set and held low for a minimum time of tACTmax, to avoid false error.
2. PAR_IN is driven from PPO of the first SSTUAF32866 device.
3. If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse.

Register Timing

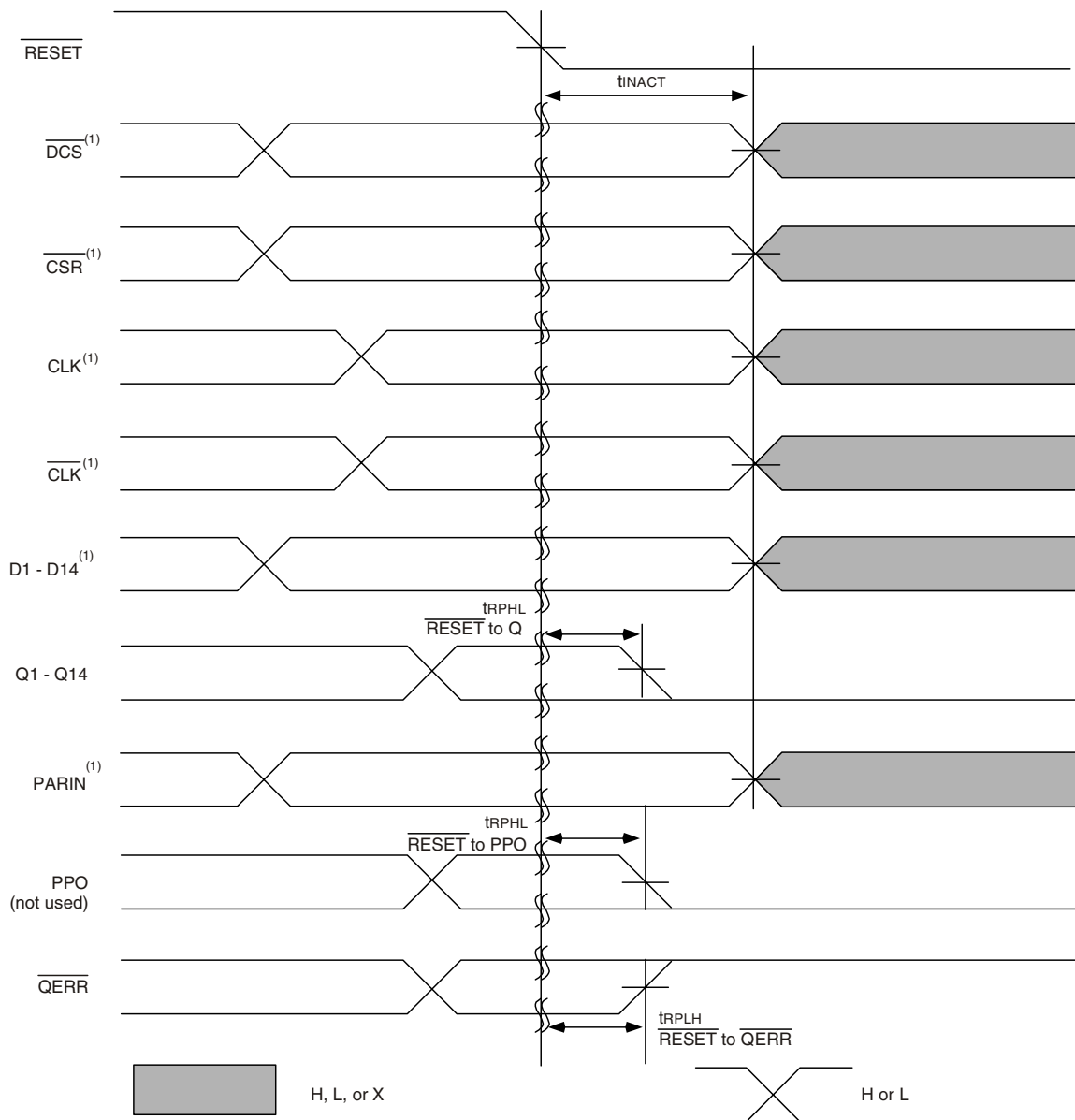


Timing Diagram for the Second SSTUAF32866C (1:2 Register-B Configuration) Device Used in a Pair; C0 = 1, C1 = 1, $\overline{\text{RESET}}$ Held HIGH

NOTES:

- 1.If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the $n+1$ clock pulse, and it will be valid on the $n+2$ clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.
- 2.PAR_IN is driven from PPO of the first SSTUAF32866 device.

Register Timing

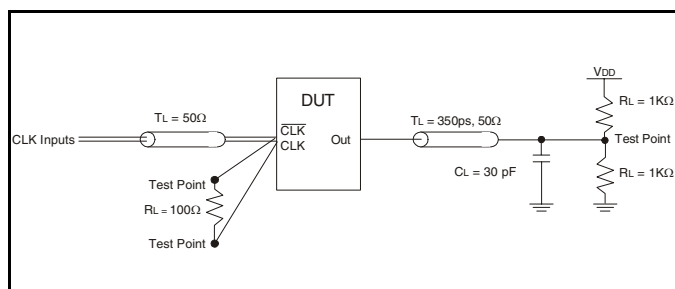


Timing Diagram for the First SSTUAF32866C (1:2 Register-A Configuration) Device Used in a Pair; C0 = 1, C1 = 1; RESET Switches from H to L

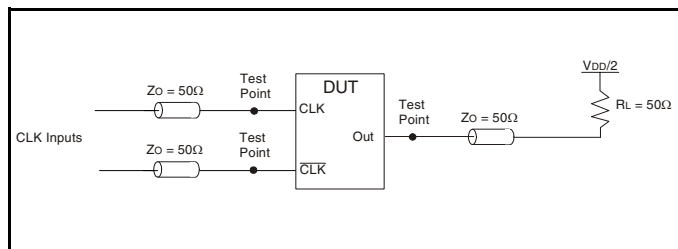
NOTE:

1. After RESET is switched from HIGH to LOW, all data and clock inputs signals must be set and held at valid logic levels (not floating) for a minimum time of $t_{INACTMAX}$.

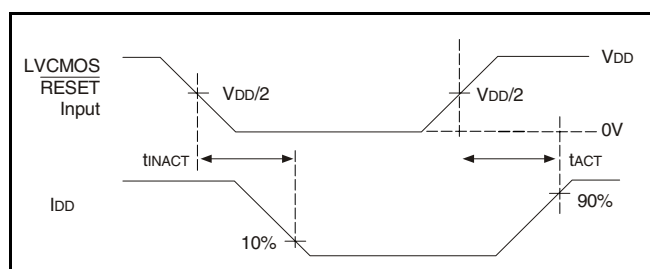
Test Circuits and Waveforms ($V_{DD} = 1.8V \pm 0.1V$)



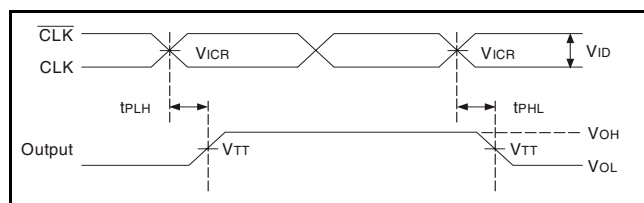
Simulation Load Circuit



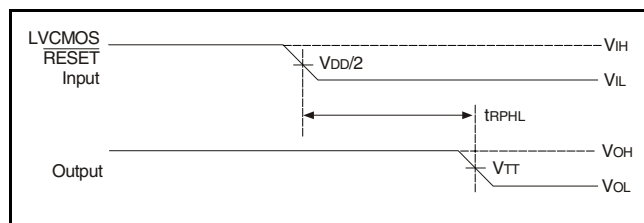
Production-Test Load Circuit



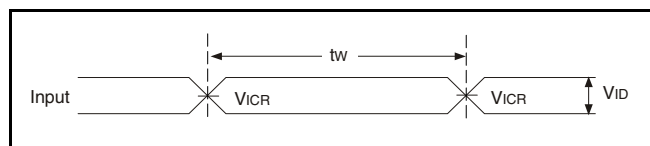
Voltage and Current Waveforms Inputs Active and Inactive Times



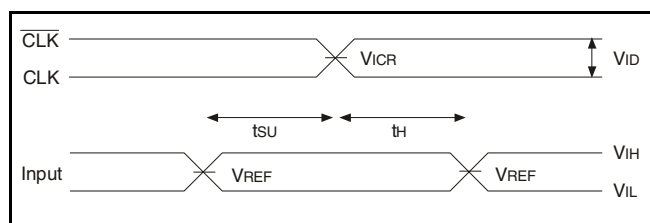
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration

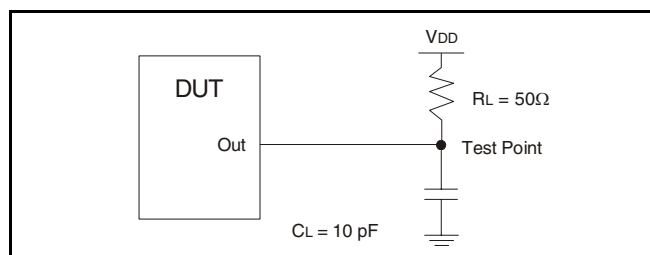


Voltage Waveforms - Setup and Hold Times

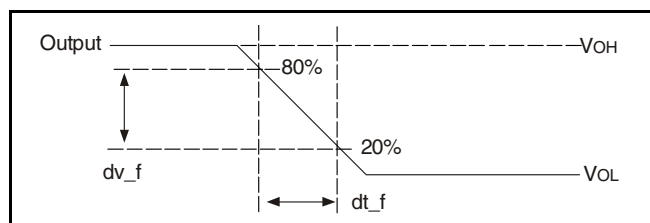
NOTES:

1. CL includes probe and jig capacitance.
2. IDD tested with clock and data inputs held at VDD or GND, and $I_O = 0mA$
3. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$, input slew rate = $1 V/ns \pm 20\%$ (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF} + 250mV$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS input.
7. $V_{IL} = V_{REF} - 250mV$ (AC voltage levels) for differential inputs. $V_{IL} = GND$ for LVC MOS input.
8. $V_{ID} = 600mV$.
9. tPLH and tPHL are the same as tPDM.

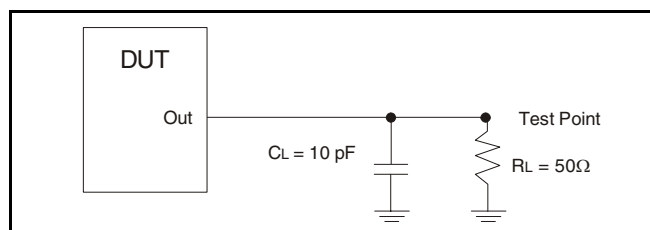
Test Circuits and Waveforms ($V_{DD} = 1.8V \pm 0.1V$)



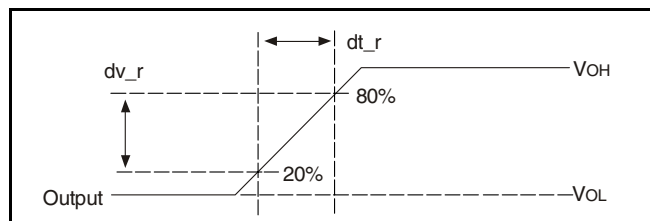
Load Circuit: High-to-Low Slew-Rate Adjustment



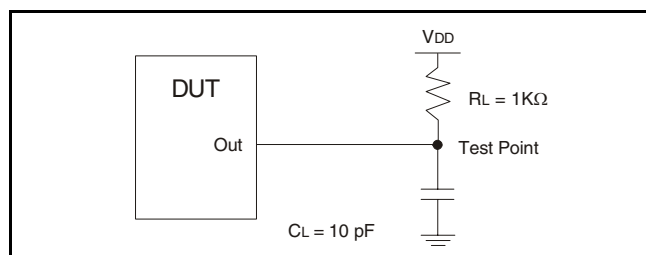
Voltage Waveforms: High-to-Low Slew-Rate Adjustment



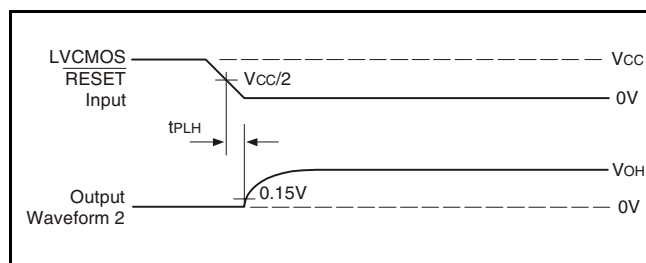
Load Circuit: Low-to-High Slew-Rate Adjustment



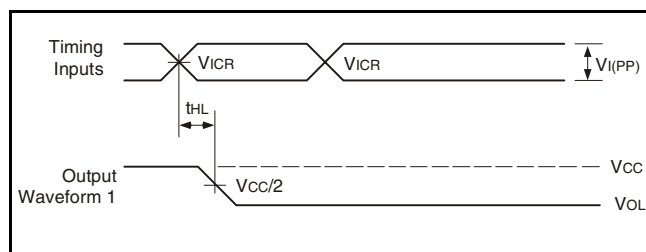
Voltage Waveforms: Low-to-High Slew-Rate Adjustment



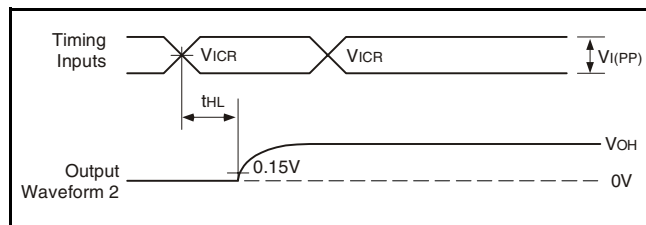
Load Circuit: Error Output Measurements



Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to RESET input)



Voltage Waveforms: Open Drain Output High-to-Low Transition Time (with respect to clock inputs)

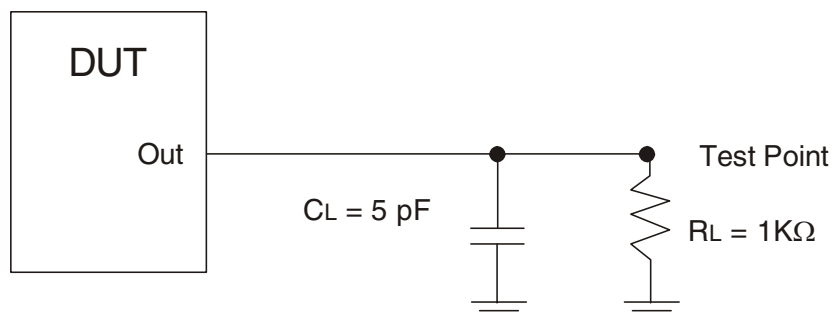


Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to clock inputs)

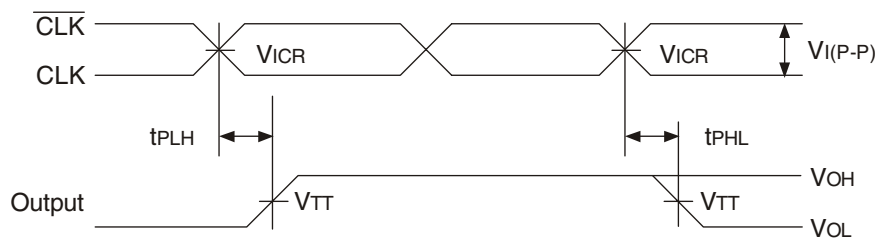
NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{MHz}$, $Z_o = 50\Omega$, input slew rate = $1\text{ V/ns} \pm 20\%$ (unless otherwise specified).

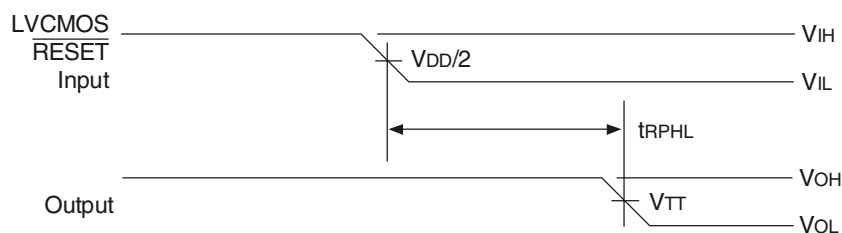
Test Circuits and Waveforms ($V_{DD} = 1.8V \pm 0.1V$)



Load Circuit: Partial-Parity-Out Load Circuit



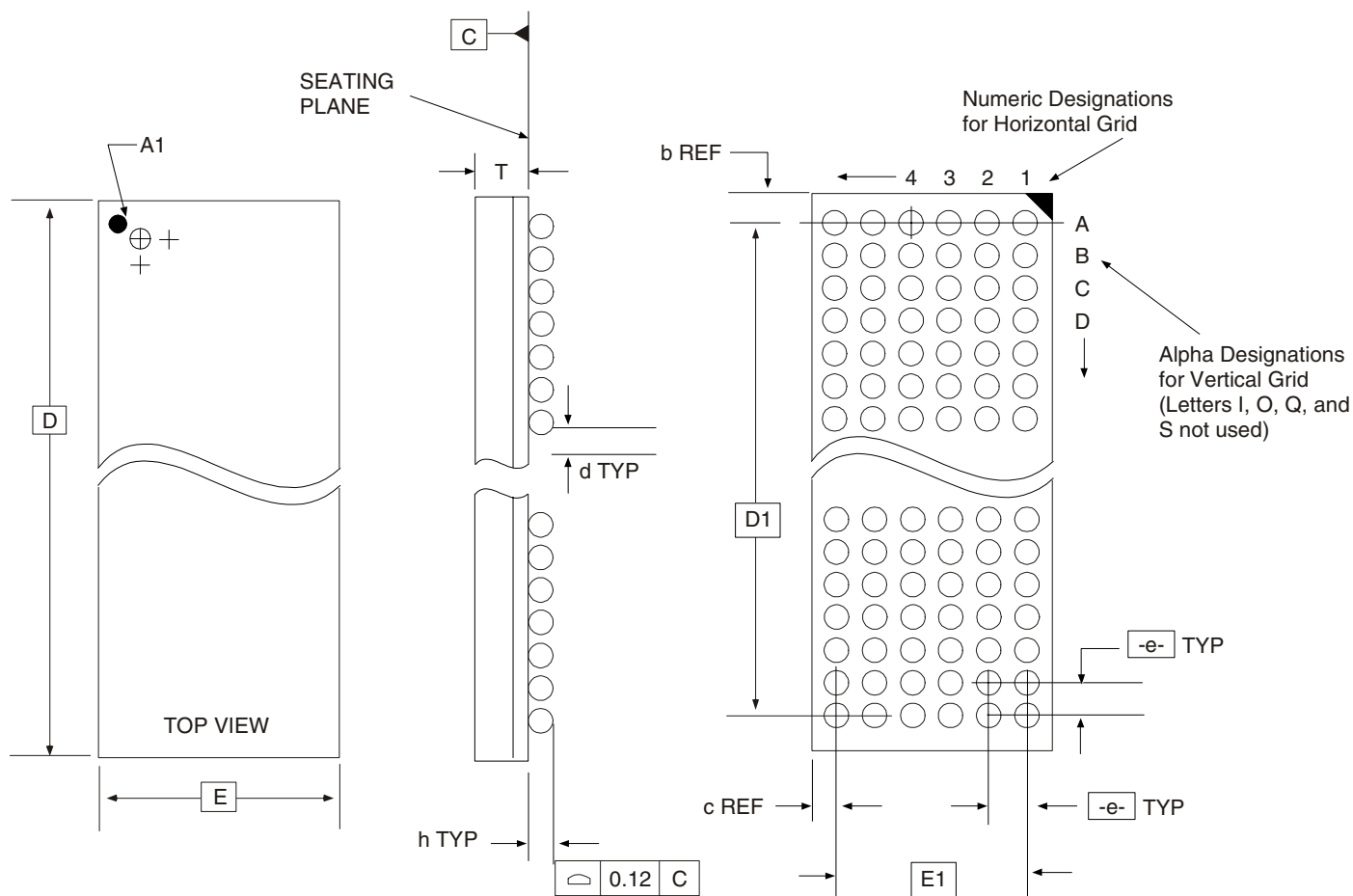
Load Circuit: Partial-Parity-Out Voltage Waveforms Propagation Delay Times (with respect to clock inputs)



Load Circuit: Partial-Parity-Out Voltage Waveforms Propagation Delay Times (with respect to $\overline{\text{RESET}}$ input)

Package Outline and Package Dimensions - BGA

Package dimensions are kept current with JEDEC Publication No. 95



ALL DIMENSIONS IN MILLIMETERS

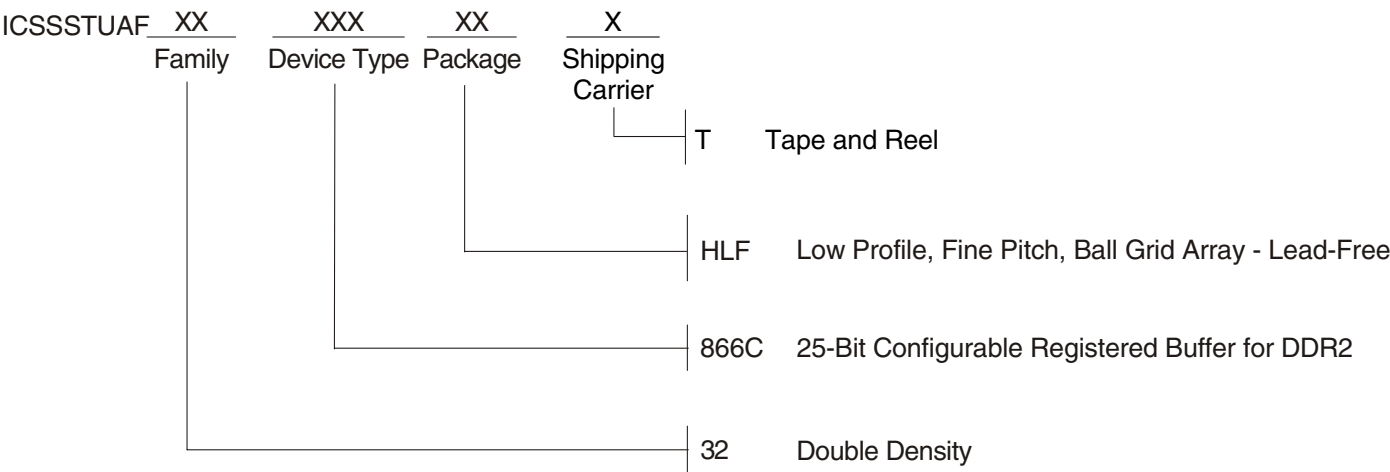
| D | E | T | e | ---- BALL GRID ---- | | Max. TOTAL | d | h | REF. DIMENSIONS | |
|-----------|----------|-----------|----------|---------------------|------|---------------|-----------|-----------|-----------------|------|
| | | | | HORIZ | VERT | | | | b | c |
| | | Min/Max | | | | | Min/Max | Min/Max | | |
| 13.50 Bsc | 5.50 Bsc | 1.20/1.40 | 0.80 Bsc | 6 | 16 | 96 | 0.40/0.50 | 0.25/0.41 | 0.75 | 0.75 |

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205

10-0055C

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