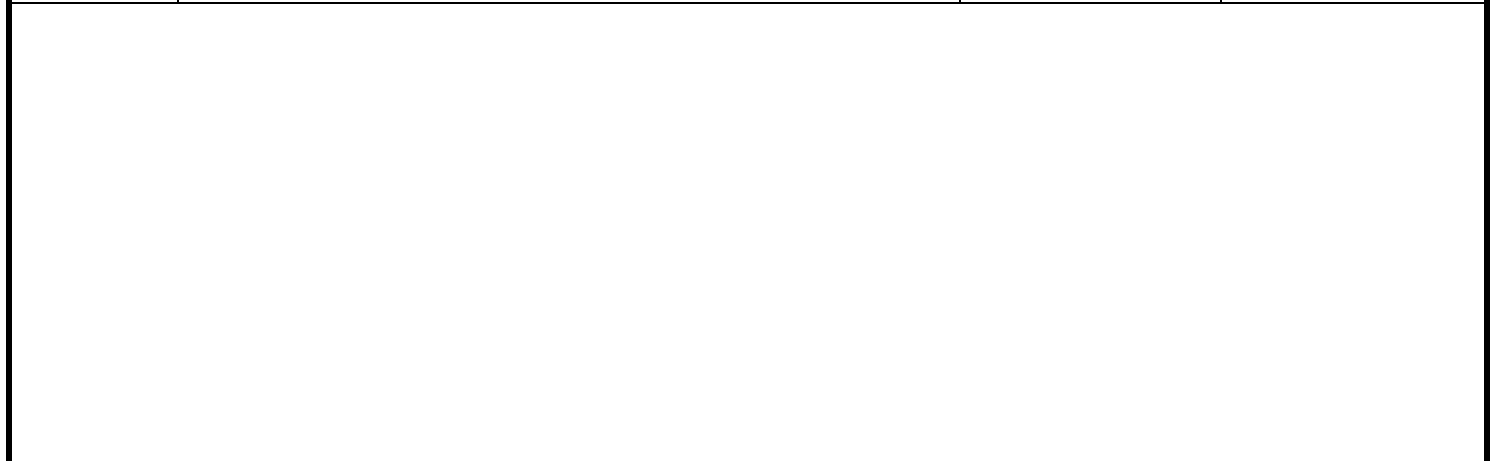


REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add appendix A for device type 02 only. Make editorial changes throughout.	97-04-09	R. MONNIN
B	Make change to 1.4, 30.2.1, I <sub>S(OFF)</sub> overvoltage and I <sub>D(OFF)</sub> overvoltage tests. - ro	97-09-12	R. MONNIN
C	Make change to boilerplate and add device class T for device type 02. - ro	98-12-02	R. MONNIN
D	Add level P to table I. Make change to 1.5 and glassivation as specified under APPENDIX A. - ro	99-04-22	R. MONNIN
E	Make change to enable delay waveform as specified on figure 6 - ro	00-04-14	R. MONNIN
F	Make changes to supply voltage and V <sub>REF</sub> to GND limits as specified under 1.3. Make clarification to paragraphs 4.4.4.2 and 4.4.4.3. - ro	04-06-25	R. MONNIN

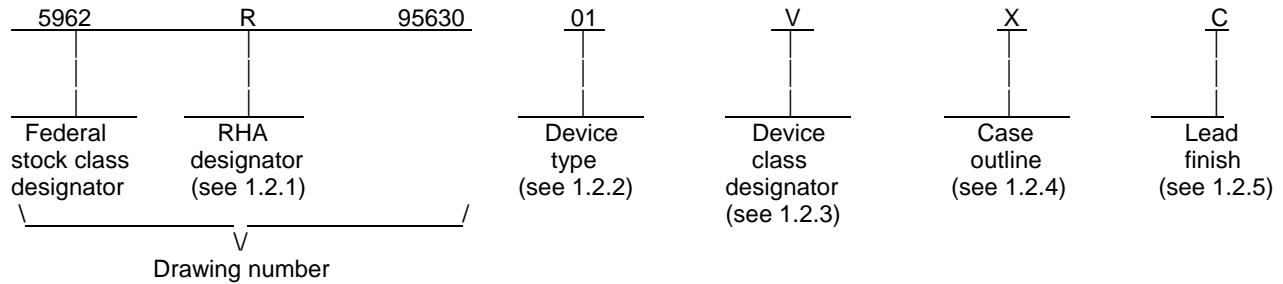


REV																					
SHEET																					
REV	F	F	F	F	F	F	F	F	F	F	F	F									
SHEET	15	16	17	18	19	20	21	22	23	24	25	26									
REV STATUS				REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	14		
PMIC N/A					PREPARED BY RICK OFFICER	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dscc.dla.mil">http://www.dscc.dla.mil</a></p> <p align="center"><b>MICROCIRCUIT, LINEAR, RADIATION  HARDENED, SINGLE 16-CHANNEL ANALOG  MUX / DEMUX WITH OVERVOLTAGE  PROTECTION, MONOLITHIC SILICON</b></p>															
<p align="center"><b>STANDARD  MICROCIRCUIT  DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE  FOR USE BY ALL  DEPARTMENTS  AND AGENCIES OF THE  DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>					CHECKED BY RAJESH PITHADIA																
					APPROVED BY RAYMOND MONNIN																
					DRAWING APPROVAL DATE 95-08-23																
				REVISION LEVEL F	SIZE A	CAGE CODE <b>67268</b>	<b>5962-95630</b>														
				SHEET 1 OF 26																	

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HS-1840RH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection
02	HS-1840ARH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CDIP2-T28	28	Dual-in-line
Y	CDFP3-F28	28	Flat pack

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1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage between V+ and V- :	
Device type 01 .....	+40 V
Device type 02 .....	+33 V
Supply voltage between V+ and GND :	
Device type 01 .....	+20 V
Device type 02 .....	+16.5 V
Supply voltage between V- and GND :	
Device type 01 .....	-20 V
Device type 02 .....	-16.5 V
V <sub>REF</sub> to GND :	
Device type 01 .....	+20 V
Device type 02 .....	+16.5 V
Digital input overvoltage range .....	$((\text{GND}) - 4 \text{ V}) \leq V_A \leq ((V_{\text{REF}}) + 4 \text{ V})$
Analog input overvoltage range (power on/off):	
Device type 01 .....	$-25 \text{ V} \leq V_S \leq +25 \text{ V}$
Device type 02 .....	$-35 \text{ V} \leq V_S \leq +35 \text{ V}$
Storage temperature range .....	-65°C to +150°C
Maximum package power dissipation (P <sub>D</sub> ): 2/	
Case X .....	1600 mW
Case Y .....	1400 mW
Lead temperature (soldering, 10 seconds) .....	+275°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ):	
Case X .....	83.1°C/W
Case Y .....	49.1°C/W

1.4 Recommended operating conditions.

Positive supply voltage (V+) .....	+15 V
Negative supply voltage (V-).....	-15 V
V <sub>REF</sub> .....	5 V dc
V <sub>AH</sub> .....	4.0 V dc
V <sub>AL</sub> .....	0.8 V dc
V <sub>EN</sub> .....	0.8 V dc
Ambient operating temperature range (T <sub>A</sub> ).....	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ The derating factor for case X shall be 20.4 mW/°C, above T<sub>A</sub> = +95°C, and for case Y shall be 18.5 mW/°C above T<sub>A</sub> = +95°C.

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1.5 Radiation features. 3/

SEP effective let no upsets:

Device type 01 .....	110 MeV/cm <sup>2</sup> /mg
Device type 02 .....	120 MeV/cm <sup>2</sup> /mg
Maximum total dose available: (dose rate = 50 – 300 rad(Si)/s)	
Device classes M, Q, and V:	
Device type 01 .....	200 Krads (Si)
Device type 02 .....	300 Krads (Si)
Device class T:	
Device type 02 .....	100 Krads (Si)
Dose rate upset:	
Device type 01 .....	>1 x 10 <sup>8</sup> rad(Si)/s
Device type 02 .....	Not tested
Latch up .....	None

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or [www.dodssp.daps.mil](http://www.dodssp.daps.mil) or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3/ Guaranteed by process design, but not tested, unless specified in table I herein.

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### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 82 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current, <u>2/</u> address or enable pins	I <sub>AH</sub>	Measure inputs sequentially, ground all used pins.  <u>3/</u> M, D, P, L, R, F	1,2,3	01,02	-1.0	1.0	μA
			<u>3/</u>		-1.0	1.0	
	I <sub>AL</sub>	<u>3/</u> M, D, P, L, R, F	1,2,3	01,02	-1.0	1.0	μA
			<u>3/</u>		-1.0	1.0	
Leakage current into the source terminal of an off switch	I <sub>S(OFF)</sub>	V <sub>S</sub> = -10 V, all unused inputs and output equal +10 V, see figure 5	1	01,02	-10	+10	nA
			2,3		-100	+100	
		<u>4/</u> M, D, P, L, R, F	<u>3/</u>		-100	+100	
		V <sub>S</sub> = +10 V, all unused inputs and output equal -10 V, see figure 5	1		-10	+10	nA
	2,3		-100	+100			
	<u>4/</u> M, D, P, L, R, F	<u>3/</u>	-100	+100			
	Leakage current into the source terminal of an off switch with power off	I <sub>S(OFF)</sub> power off	V <sub>S</sub> = +25 V, V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0 V, V <sub>-</sub> = 0 V, V <sub>+</sub> = 0 V, V <sub>REF</sub> = 0 V, all unused inputs tied to GND, see figure 5	1	01,02	-50	+50
2,3				-100		+100	
<u>3/</u> M, D, P, L, R, F			<u>3/</u>	-100		+100	
Leakage current into the source terminal of an off switch with overvoltage applied	I <sub>S(OFF)</sub> over- voltage	V <sub>D</sub> = 0 V, all unused inputs tied to GND, see figure 5	1,2,3	01,02	-1	+1	μA
			<u>5/</u> <u>4/</u> M, D, P, L, R, F		<u>3/</u>	-1.5	
		V <sub>D</sub> = 0 V, all unused inputs tied to GND, see figure 5	1,2,3		-1	+1	μA
			<u>6/</u> <u>4/</u> M, D, P, L, R, F		<u>3/</u>	-1.5	

See footnotes at end table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Leakage current into the drain terminal of an off switch with overvoltage applied	I <sub>D(OFF)</sub> over-voltage	V <sub>D</sub> = 0 V, all unused inputs tied to GND, see figure 5	1,2,3	01,02	-1	+1	μA
			<u>5/</u> M, D, P, L, R, F <u>4/</u>		1 <u>3/</u>	-1	
		V <sub>D</sub> = 0 V, all unused inputs tied to GND, see figure 5	1,2,3	01,02	-1	+1	μA
			<u>6/</u> M, D, P, L, R, F <u>4/</u>		1 <u>3/</u>	-1	
Leakage current into the drain terminal of an off switch	I <sub>D(OFF)</sub>	V <sub>D</sub> = -10 V, all unused inputs = +10 V, see figure 5	1	01,02	-10	+10	nA
			2,3		-100	+100	
			<u>4/</u> M, D, P, L, R, F <u>4/</u>		1 <u>3/</u>	-100	
Leakage current into the drain terminal of an off switch	I <sub>D(OFF)</sub>	V <sub>D</sub> = +10 V, all unused inputs = -10 V, see figure 5	1	01,02	-10	+10	nA
			2,3		-100	+100	
			<u>4/</u> M, D, P, L, R, F <u>4/</u>		1 <u>3/</u>	-100	
Leakage current from an on driver into the switch (drain and source)	I <sub>D(ON)</sub>	V <sub>S</sub> = +10 V, V <sub>D</sub> = +10 V, V <sub>EN</sub> = 0.8 V, all unused input = -10 V, see figure 5	1	01,02	-10	+10	nA
			2,3		-100	+100	
			<u>7/</u> M, D, P, L, R, F <u>7/</u>		1 <u>3/</u>	-100	
		V <sub>S</sub> = -10 V, V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V, all unused input = +10 V, see figure 5	1	01,02	-10	+10	nA
			2,3		-100	+100	
			<u>7/</u> M, D, P, L, R, F <u>7/</u>		1 <u>3/</u>	-100	

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DEFENSE SUPPLY CENTER COLUMBUS  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**F**

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SHEET  
**7**

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit		
					Min	Max			
Positive supply current	I+	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0.8 V	1,2,3	01,02	0.05	0.5	mA		
		<u>M, D, P, L, R, F 7/</u>	<u>1 3/</u>		0.05	0.5			
Negative power supply	I-	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0.8 V	1,2,3	01,02	0.05	0.5	mA		
		<u>M, D, P, L, R, F 7/</u>	<u>1 3/</u>		0.05	0.5			
Positive standby supply current	+ISBY	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 4.0 V	1,2,3	01,02	0.05	0.5	mA		
		<u>M, D, P, L, R, F 4/</u>	<u>1 3/</u>		0.05	0.5			
Negative standby power supply	-ISBY	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 4.0 V	1,2,3	01,02	0.05	0.5	mA		
		<u>M, D, P, L, R, F 4/</u>	<u>1 3/</u>		0.05	0.5			
Switch on resistance	R <sub>DS(ON)</sub>	V <sub>S</sub> = +15 V, I <sub>D</sub> = -1 mA, V <sub>EN</sub> = 0.8 V, see figure 5	1,2,3	01	---	1.0	kΩ		
				02	0.5	3.0			
				<u>M, D, P, L, R, F 7/</u>	<u>1 3/</u>	01		---	1.0
				02	0.5	3.0			
		V <sub>S</sub> = -5 V, I <sub>D</sub> = +1 mA, V <sub>EN</sub> = 0.8 V, see figure 5	1,2,3	01	---	4.0			
					02	0.5	3.0		
					<u>M, D, P, L, R, F 7/</u>	<u>1 3/</u>	01	---	4.0
					02	0.5	3.0		
		V <sub>S</sub> = +5 V, I <sub>D</sub> = -1 mA, V <sub>EN</sub> = 0.8 V, see figure 5	1,2,3	01	---	2.5			
					02	0.5	3.0		
					<u>M, D, P, L, R, F 7/</u>	<u>1 3/</u>	01	---	2.5
					02	0.5	3.0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Capacitance: digital input	C <sub>A</sub>	V <sub>+</sub> = V <sub>-</sub> = 0 V, f = 1 MHz, T <sub>A</sub> = +25°C, see 4.4.1c	4	01,02		7	pF	
Capacitance: channel input	C <sub>S(OFF)</sub>	V <sub>+</sub> = V <sub>-</sub> = 0 V, f = 1 MHz, T <sub>A</sub> = +25°C, see 4.4.1c	4	01,02		5	pF	
Capacitance: channel output	C <sub>D(OFF)</sub>	V <sub>+</sub> = V <sub>-</sub> = 0 V, f = 1 MHz, T <sub>A</sub> = +25°C, see 4.4.1c	4	01,02		50	pF	
Off isolation input or output	V <sub>ISO</sub>	V <sub>EN</sub> = 4.0 V, f = 200 kHz, C <sub>L</sub> = 7 pF, R <sub>L</sub> = 1 kΩ, V <sub>S</sub> = 3 V <sub>RMS</sub> , T <sub>A</sub> = +25°C, see 4.4.1c	4	01,02	-45		dB	
Functional test		See 4.4.1d	7,8A,8B	01,02				
Break-before-make time delay	t <sub>D</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ, see figure 6	9	01,02	25		ns	
			10,11		5			
			M, D, P, L, R, F <u>4/ 7/ 8/</u>		9 <u>3/</u>	5		
Propagation delay time address inputs to I/O channels	t <sub>ON(A)</sub> , t <sub>OFF(A)</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 10 MΩ, see figure 6	9	01		0.6	μs	
				02		1.25		
			10,11	01		1.0		
				02		1.5		
			M, D, P, L, R, F <u>4/ 7/ 8/</u>	9 <u>3/</u>	01			3.0
				02		1.5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Propagation delay time enable to I/O channels	t <sub>ON(EN)</sub> , t <sub>OFF(EN)</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ, see figure 6	9	01		0.6	μs	
				02		1.25		
			10,11	01		1.0		
				02		1.5		
			M, D, P, L, R, F <sup>4/ 7/ 8/</sup>	9 <sup>3/</sup>	01			3.0
					02			1.5

<sup>1/</sup> V<sub>AH</sub> (logic level high) = 4.0 V dc, V<sub>AL</sub> (logic level low) = 0.8 V dc, V<sub>+</sub> = +15 V dc, V<sub>-</sub> = -15 V dc, V<sub>EN</sub> = 4.0 V unless otherwise specified, and V<sub>REF</sub> = 5.0 V dc.

<sup>2/</sup> Input current of one node.

<sup>3/</sup> Devices supplied to this drawing will meet all levels M, D, P, L, R, for device type 01 (device classes M, Q, and V) and levels M, D, P, L, R, F for device type 02 (device classes M, Q, or V) and levels M, D, P, L, R, for device type 02 (device class T). However, device type 01 (device classes M, Q, and V) is only tested at the "R" level and device type 02 (device classes M, Q, and V) is only tested at the "F" level, and device type 02 (class T) is only tested at the "R" level. (see paragraph 1.5 herein). Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T<sub>A</sub> = +25°C.

<sup>4/</sup> V<sub>EN</sub> = 4.5 V

<sup>5/</sup> For device type 01, V<sub>S</sub> = +25 V. For device type 02, V<sub>S</sub> = +35 V.

<sup>6/</sup> For device type 01, V<sub>S</sub> = -25 V. For device type 02, V<sub>S</sub> = -35 V.

<sup>7/</sup> V<sub>EN</sub> = 0.5 V

<sup>8/</sup> V<sub>AH</sub> = 4.5 V and V<sub>AL</sub> = 0.5 V

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Device types	01 and 02
Case outlines	X and Y
Terminal number	Terminal symbol
1	V+
2	NC
3	NC
4	IN 16
5	IN 15
6	IN 14
7	IN 13
8	IN 12
9	IN 11
10	IN 10
11	IN 9
12	GND
13	V <sub>REF</sub>
14	A3
15	A2
16	A1
17	A0
18	$\overline{\text{EN}}$
19	IN 1
20	IN 2
21	IN 3
22	IN 4
23	IN 5
24	IN 6
25	IN 7
26	IN 8
27	V-
28	OUT

NC = No connection

FIGURE 1. Terminal connections.

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Truth table					
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	$\overline{\text{EN}}$	On channel
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

FIGURE 2. Truth table.

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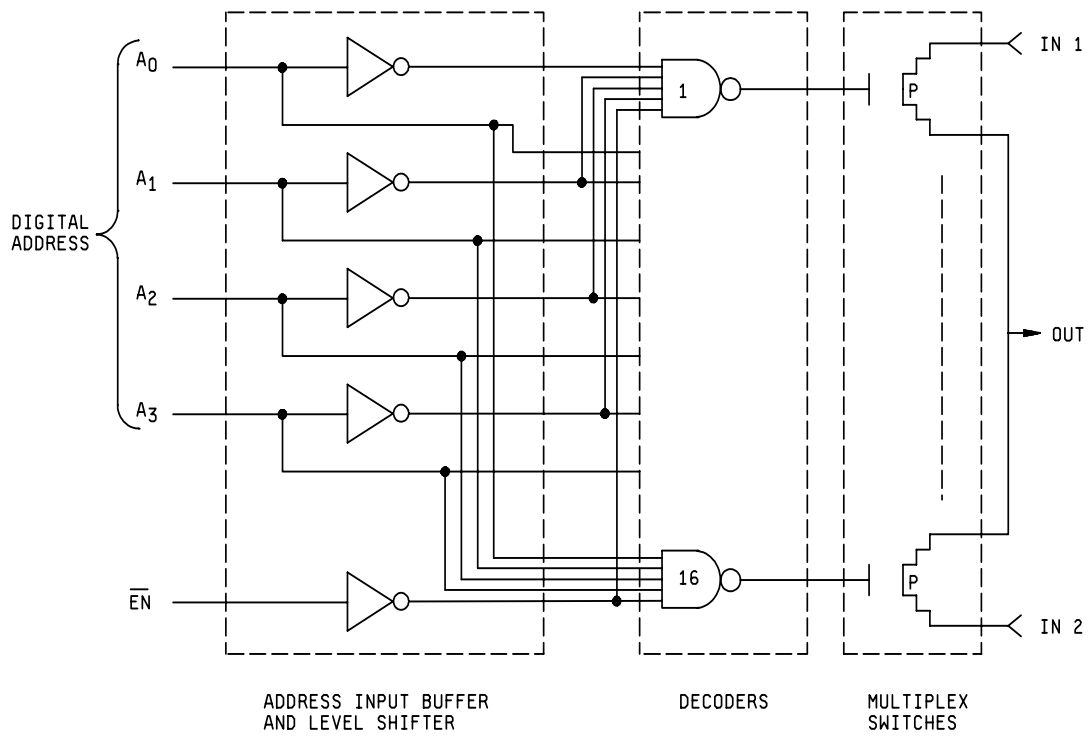


FIGURE 3. Logic diagram.

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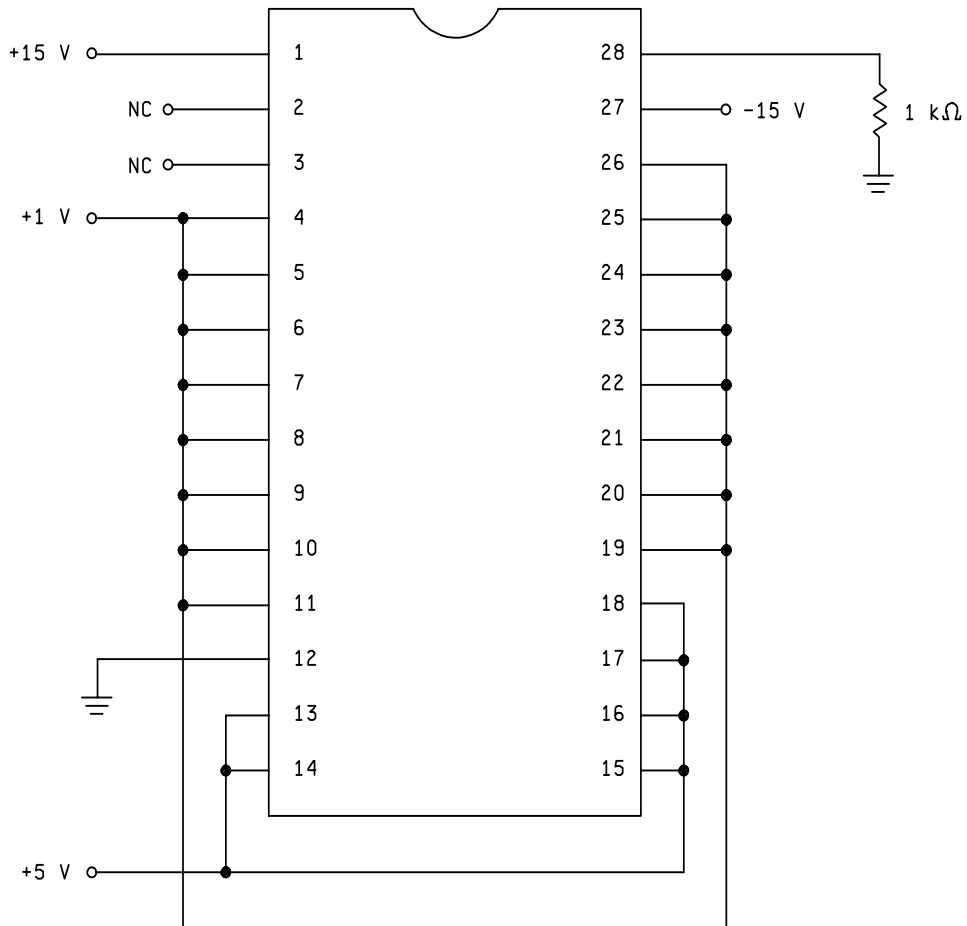
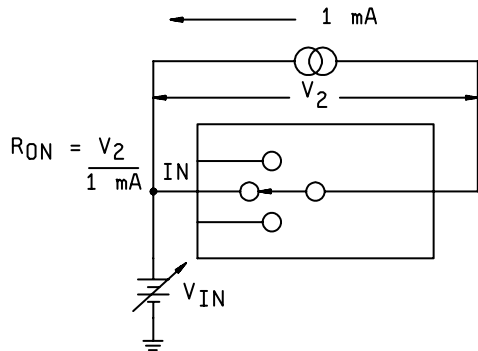


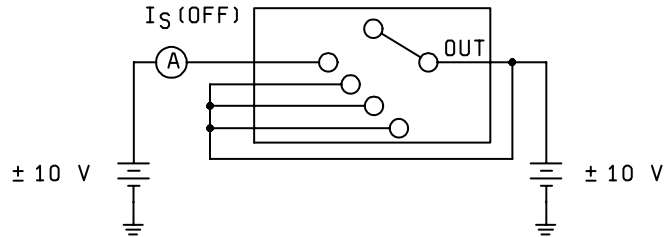
FIGURE 4. Radiation exposure circuit.

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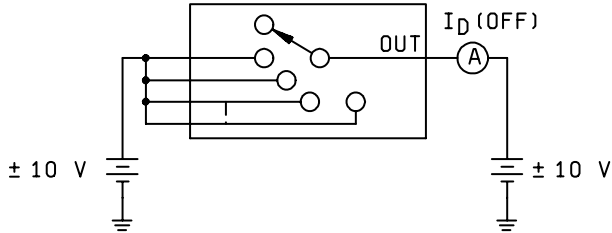
ON RESISTANCE VS. INPUT SIGNAL LEVEL



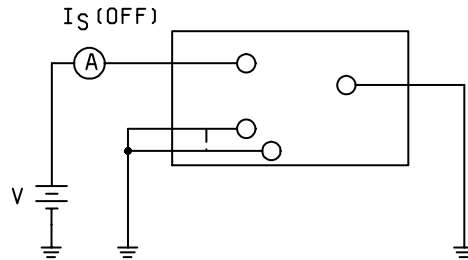
$I_S$  (OFF) LEAKAGE CURRENT



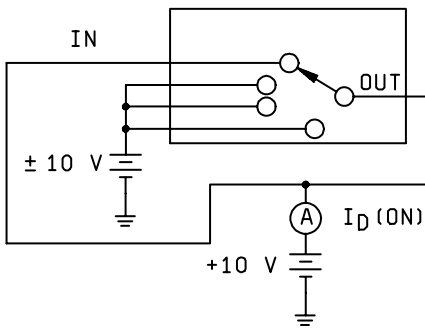
$I_D$  (OFF) LEAKAGE CURRENT



$I_S$  (OFF) WITH POWER OFF



$I_D$  (ON) LEAKAGE CURRENT



ANALOG INPUT OVERVOLTAGE

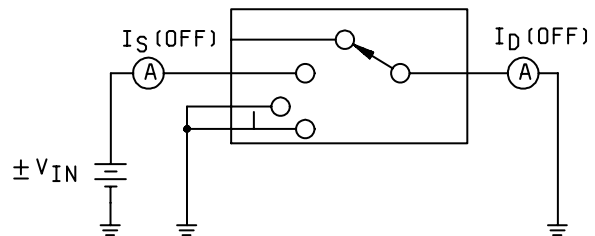


FIGURE 5. Test circuits for dc levels.

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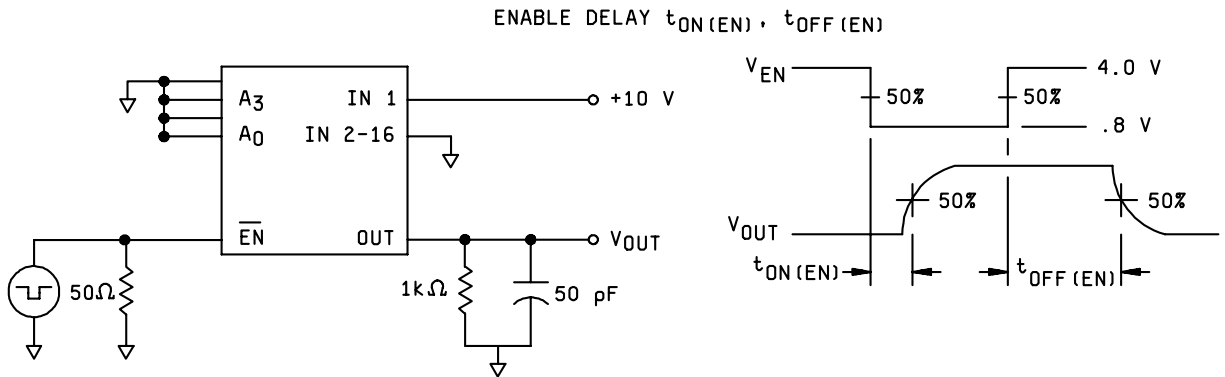
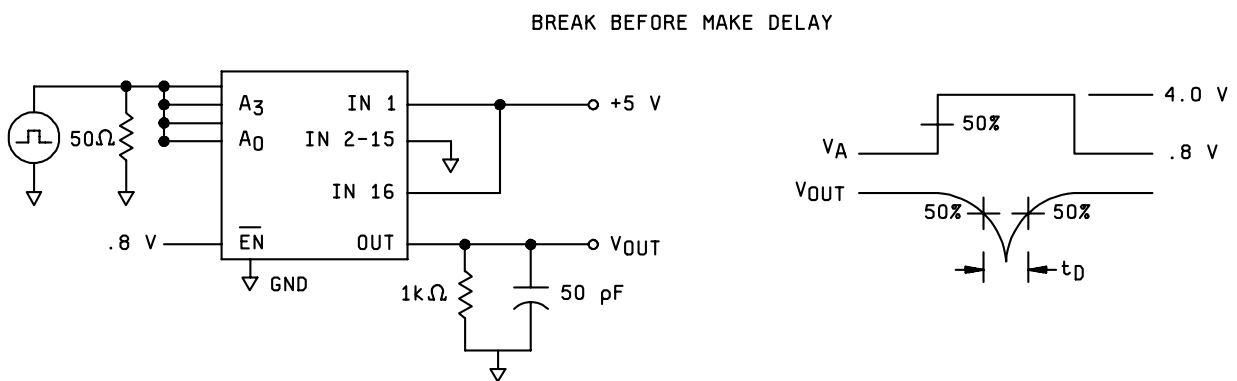
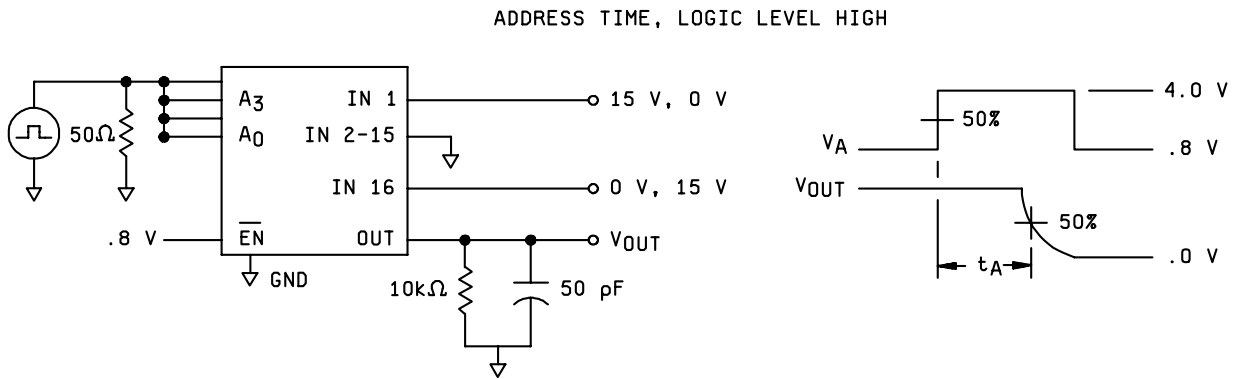


FIGURE 6. Test circuits and waveforms for ac levels.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein.

For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's (QM) plan, including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For devices classes Q, T, and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 as specified in the QM plan including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,7,8A, <u>1/</u> 8B,9,10,11	1,2,3,7,8A, <u>1/</u> 8B,9,10,11	1,2,3, <u>1/ 2/</u> 7,8A,8B,9, 10,11	
Group A test requirements (see 4.4)	1,2,3,4,7,8A,8B,9, 10,11	1,2,3,4,7,8A, 8B,9,10,11	1,2,3,4,7, <u>2/</u> 8A,8B,9,10, 11	
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8A,8B, 9,10,11	1,2,3,7,8A,8B, 9,10,11	1,2,3,7,8A, 8B,9,10,11	
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	

1/ PDA applies to subgroup 1. For class V, 1, 7, and Δ.

2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table I).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C<sub>A</sub>, C<sub>S</sub>, C<sub>D</sub>, and V<sub>ISO</sub> measurements) should be measured for initial qualification and after any process or design changes which may affect input or output capacitance.
- d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. T<sub>A</sub> = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE IIB. Burn-in delta parameters (+25°C) and group C delta parameters.

Parameters	Symbol	Conditions	Delta limits
Input leakage current, address, or enable pins	$I_{AH}$	Measure inputs sequentially, ground all unbiased pins	$\pm 100$ nA
Leakage current into the source terminal of an "Off" switch	$+I_{S(OFF)}$	$V_S = +10$ V, all unused and output = -10 V, $V_{EN} = 4.0$ V	$\pm 20$ nA
	$-I_{S(OFF)}$	$V_S = -10$ V, all unused inputs and outputs = +10 V, $V_{EN} = 4.0$ V	$\pm 20$ nA
Leakage current into the drain terminal of an "Off" switch	$+I_{D(OFF)}$	$V_D = +10$ V, all unused inputs = -10 V, $V_{EN} = 4.0$ V	$\pm 20$ nA
	$-I_{D(OFF)}$	$V_D = -10$ V, all unused inputs = +10 V, $V_{EN} = 4.0$ V	$\pm 20$ nA
Leakage current from an "On" driver into the switch (drain and source)	$+I_{D(ON)}$	$V_S = +10$ V, all unused inputs = -10 V, $V_{EN} = 0.8$ V, $V_D = +10$ V	$\pm 20$ nA
	$-I_{D(ON)}$	$V_S = -10$ V, all unused inputs = +10 V, $V_D = -10$ V, $V_{EN} = 0.8$ V	$\pm 20$ nA
Switch on resistance	$R_{(ON)}$	$V_S = +15$ V, $I_D = -1$ mA, $V_{EN} = 0.8$ V	$\pm 150$ $\Omega$
		$V_S = -5$ V, $I_D = +1$ mA, $V_{EN} = 0.8$ V	$\pm 250$ $\Omega$
Positive supply current	$I_+$	$V_{EN} = 0.8$ V	$\pm 50$ $\mu$ A
Negative supply current	$I_-$	$V_{EN} = 0.8$ V	$\pm 50$ $\mu$ A
Positive standby supply current	$+I_{SBY}$	$V_{EN} = 4.0$ V	$\pm 50$ $\mu$ A
Negative standby supply current	$-I_{SBY}$	$V_{EN} = 4.0$ V	$\pm 50$ $\mu$ A

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4.4.2.2 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein. For device class T, the RHA requirements shall be in accordance with the Class T Radiation Requirements of MIL-PRF-38535. The end-point electrical parameters for class T devices shall be as specified in Table I, Group A subgroups, or as modified in the QM plan.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein. For device class T, the total dose requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535 ( see 1.5 herein).

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When specified in the purchase order or contract dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified in the purchase order or contract dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.5 herein).

- a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.
- b. Transient dose rate upset testing for class Q, T, and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract SEP testing shall be required on class T and V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or ≥ 10<sup>6</sup> ions/cm<sup>2</sup>.
- c. The flux shall be between 10<sup>2</sup> and 10<sup>5</sup> ions/cm<sup>2</sup>/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.
- f. Bias conditions shall be defined by the manufacturer for the latchup measurements.
- g. Test four devices with zero failures.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

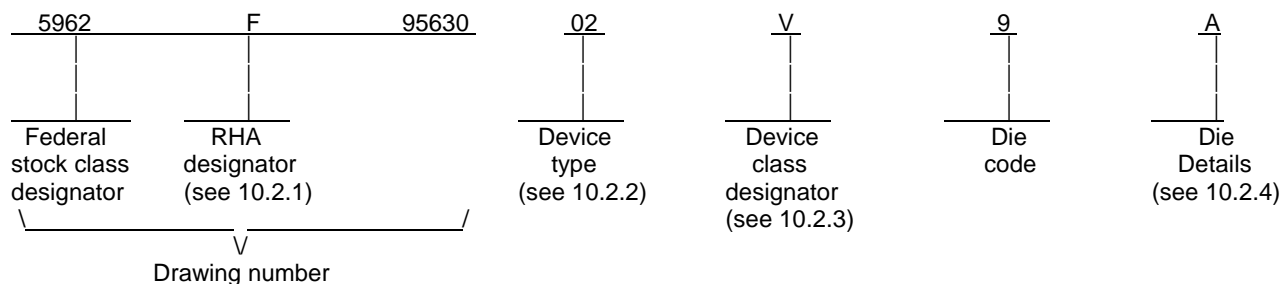
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APPENDIX A  
APPENDIX A FORMS A PART OF SMD 5962-95630

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
02	HS-1840ARH	Radiation hardened DI single 16-channel analog MUX / DEMUX with high impedance analog input overvoltage protection

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
02	A-1

A.1.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
02	A-1

A.1.2.4.3. Interface materials.

Die type	Figure number
02	A-1

A.1.2.4.4. Assembly related information.

Die type	Figure number
02	A-1

A.1.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

A.2. APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-95630</b>
		REVISION LEVEL <b>F</b>	SHEET <b>23</b>

APPENDIX A  
APPENDIX A FORMS A PART OF SMD 5962-95630

DEPARTMENT OF DEFENSE HANDBOOK

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or [www.dodssp.daps.mil](http://www.dodssp.daps.mil) or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

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A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

- a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.
- b) 100% wafer probe (see paragraph A.3.4).
- c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

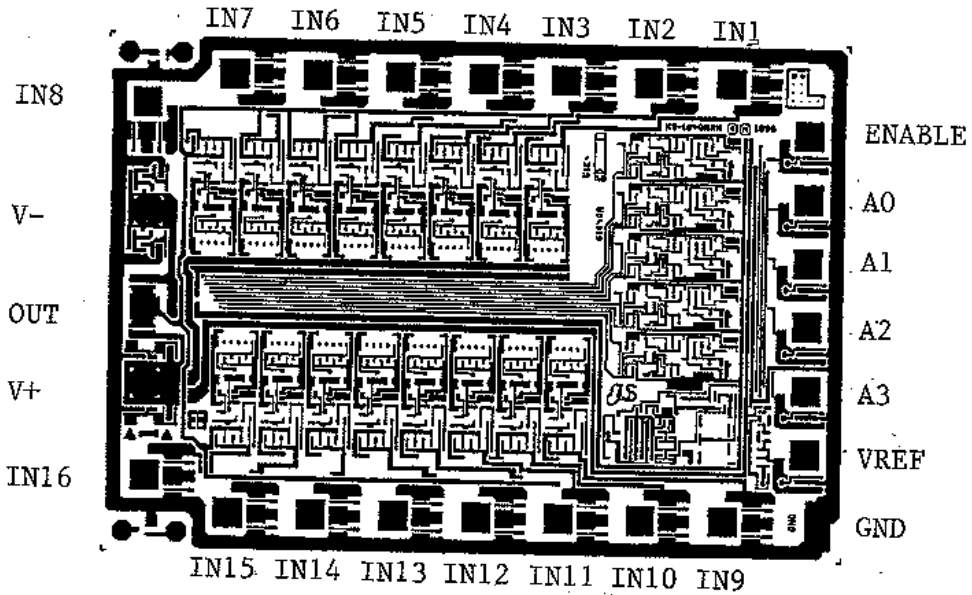
A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

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NOTE: Pad numbers reflect terminal numbers when placed in case outlines X and Y (see figure 1).



Die physical dimensions.  
 Die size: 4080 microns x 2820 microns.  
 Die thickness:  $19 \pm 1$  mils.

Interface materials.  
 Top metallization: Al Si Cu  $16.0 \text{ k\AA} \pm 2 \text{ k\AA}$   
 Backside metallization: None

Glassivation.  
 Type: PSG  
 Thickness:  $8.0 \text{ k\AA} \pm 1.0 \text{ k\AA}$

Substrate: DI (dielectric isolation)

Assembly related information.  
 Substrate potential: Unbiased  
 Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-06-25

Approved sources of supply for SMD 5962-95630 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R9563001VXC	<u>3/</u>	HS1-1840RH-Q
5962R9563001VYC	<u>3/</u>	HS9-1840RH-Q
5962R9563001QXC	<u>3/</u>	HS1-1840RH-8
5962R9563001QYC	<u>3/</u>	HS9-1840RH-8
5962F9563002VXC	34371	HS1-1840ARH-Q
5962F9563002VYC	34371	HS9-1840ARH-Q
5962F9563002QXC	34371	HS1-1840ARH-8
5962F9563002QYC	34371	HS9-1840ARH-8
5962F9563002V9A	34371	HS0-1840ARH-Q
5962R9563002TXC	34371	HS1-1840ARH-T
5962R9563002TYC	34371	HS9-1840ARH-T

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ No longer available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued

Vendor CAGE  
number

34371

Vendor name  
and address

Intersil Corporation  
P.O. Box 883  
Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.