Device Information

CD4011BMS

Printer Friendly Version

NAND, 2-Input, Quad, Rad-Hard, CMOS, Logic

Get Datasheet

Ordering Information

Part No.	Status	Temp.	Package	MSL	SMD	Price US $	
CD4011BDMSR	Active	Mil	14 Ld SBDIP	N/A	5962R9662101VCC	Contact Us	Buy
CD4011BKMSR	Active	Mil	14 Ld FlatPack	N/A	5962R9662101VXC	Contact Us	Buy

The price listed is the manufacturer's suggested retail price for quantities between 100 and 999 units. However, prices in today's market are fluid and may change without notice.
MSL = Moisture Sensitivity Level - per IPC/JEDEC J-STD-020
SMD = Standard Microcircuit Drawing

Description

CD4011BMS - Quad 2 Input
CD4012BMS - Dual 4 Input
CD4023BMS - Triple 3 Input

CD4011BMS, CD4012BMS, and CD4023BMS NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4011BMS, CD4012BMS and the CD4023BMS is supplied in these 14 lead outline packages:

	CD4011B	CD4012B	CD4023B
Braze Seal DIP	H4Q	H4H	H4Q
Frit Seal DIP	H1B	H1B	H1B
Ceramic Flatpack	H3W	H3W	H3W

Key Features

- High-Voltage Types (20V Rating)
- Propagation Delay Time = 60ns (typ.) at CL = 50pF, VDD = 10V
- Buffered Inputs and Outputs
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1µA at 18V Over Full Package- Temperature Range; 100nA at 18V and +25ºC
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, “Standard Specifications for Description of “B” Series CMOS Device’s

Related Documentation

Datasheet(s):

- Radiation Hardened CMOS NAND Gates