Device Information

CD40109BMS

Printer Friendly Version

Level Shifter, Low to High, Quad, Rad-Hard, CMOS, Logic

Get Datasheet

Ordering Information

Part No.	Status	Temp.	Package	MSL	SMD	Price US $	
CD40109BDMSR	Active	-	16 Ld SBDIP	N/A	5962R9664501VEC	Contact Us	Buy
CD40109BKMSR	Active	-	16 Ld FlatPack	N/A	5962R9664501VXC	Contact Us	Buy
CD40109BKNSR	Active	-		N/A	5962R9664502VXC	Contact Us	Buy

The price listed is the manufacturer's suggested retail price for quantities between 100 and 999 units. However, prices in today's market are fluid and may change without notice.
MSL = Moisture Sensitivity Level - per IPC/JEDEC J-STD-020
SMD = Standard Microcircuit Drawing

Description

CD40109BMS contains four low-to-high voltage level shifting circuits. Each circuit will shift a low voltage digital logic input signal (A, B, C, D) with logical 1 = VCC and logical 0 = VSS to a higher voltage output signal (E, F, G, H) with logical 1 = VDD and logical 0 = VSS.

The CD40109BMS, unlike other low-to-high level shifting circuits, does not require the presence of the high voltage supply (VDD) before the application of either the low voltage supply (VCC) or the input signals. There are no restrictions on the sequence of application of VDD, VCC, or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between VSS and at least 0.7VCC; VCC may exceed VDD, and input signals may exceed VCC and VDD. When operated in the mode VCC > VDD, the CD40109BMS will operate as a high-to-low level shifter.

The CD40109BMS also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high impedance state in the corresponding output.

The CD40109BMS is supplied in these 16-lead outline packages:

Braze Seal DIP H4T
Frit Seal DIP H1E
Ceramic Flatpack H6W

Key Features

- High Voltage Type (20V Rating)
- Independence of Power Supply Sequence Considerations
  - VCC can Exceed VDD
  - Input Signals can Exceed Both VCC and VDD
- Up and Down Level Shifting Capability
- Three-State Outputs with Separate Enable Controls
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and +25ºC
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VCC = 5V, VDD = 10V
  - 2V at VCC = 10V, VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, “Standard Specifications for Description of ‘B’ Series CMOS Devices”

Related Documentation

Datasheet(s):
- Radiation Hardened CMOS Quad Low-to-High Voltage Level Shifter

Military SMD(s):
- Radiation Hardened CMOS Quad Low-to-High Voltage Level Shifter

Parametric Data

RH Level	100

Applications

- High or Low Level Shifting with Three-State Outputs for Unidirectional or Bidirectional Bussing
- Isolation of Logic Subsystems Using Separate Power Supplies from Supply Sequencing, Supply Loss and Supply Regulation Considerations

Related Devices Parametric Table

CD4504BMS	Buffer, Voltage Level Shifter, TTL to CMOS, CMOS to CMOS, Hex, Rad-Hard, CMOS, Logic