CA3272A, CA3292A

Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output

July 1997

Features

- Load Current Switching 600mA
- Suitable for Resistive or Inductive Loads
- Fault Mode Diagnostic Flag Output
- CA3292A Over-Voltage Zener Clamp
- Independent Over-Current Limiting
- Independent Over-Temperature Shutdown
- Temperature Shutdown Hysteresis
- 5V CMOS or TTL Input Logic
- High Dissipation Power-Frame Package
- Operating Temperature Range -40^{o}C to 125^{o}C

Applications

- Solenoids
- Relays
- Lamps
- Steppers
- Injectors
- Motors

System Applications

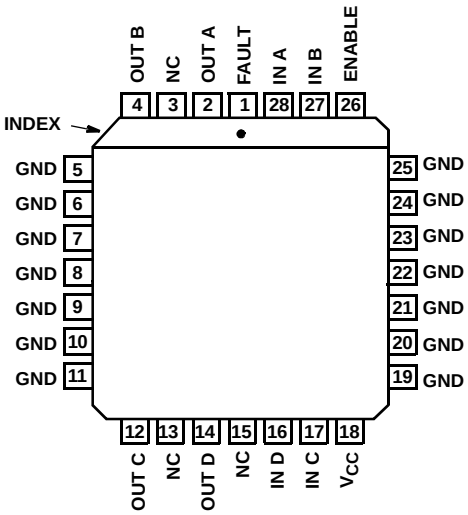
- Automotive
- Appliance
- Industrial Control
- Robotics

Ordering Information

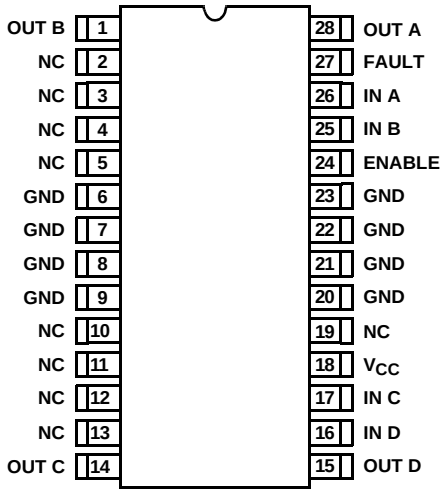
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3272AQ	-40 to 125	28 Ld PLCC	N28.45
CA3292AQ	-40 to 125	28 Ld PLCC	N28.45
CA3272AM	-40 to 125	28 Ld SOIC	M28.3
CA3292AM	-40 to 125	28 Ld SOIC	M28.3

Pinouts

CA3272A, CA3292A (PLCC)
TOP VIEW



CA3272A, CA3292A (SOIC)
TOP VIEW



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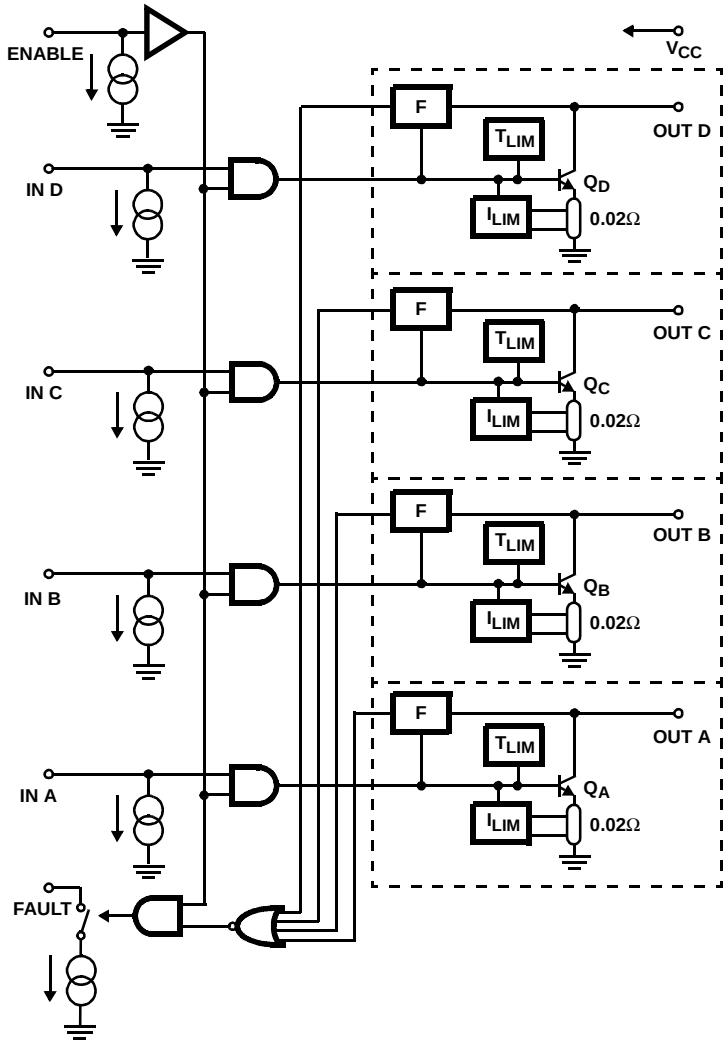
Block Diagram of the CA3272A



TRUTH TABLE

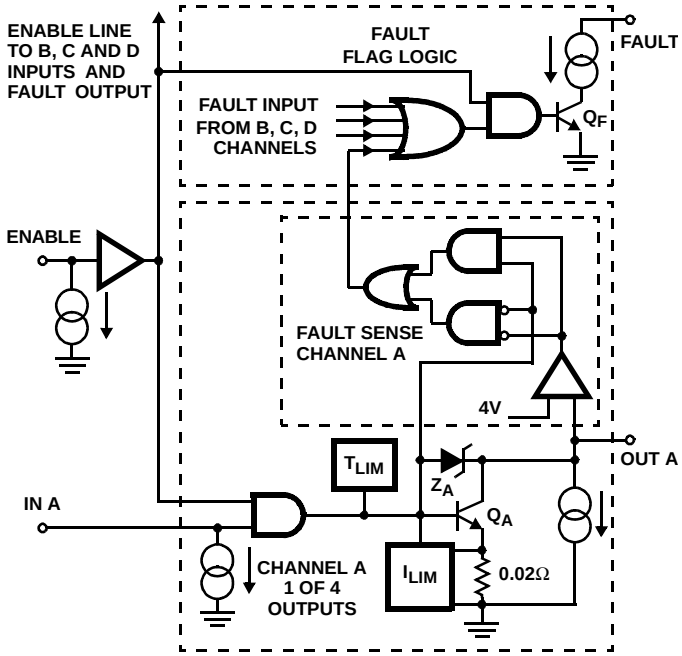
ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

Block Diagram of the CA3292A

(1 of 4 Outputs Shown with Expanded Fault Logic)

NOTE: The CA3292A is identical to the CA3272A except for the collector-to-base Zener diode on each low side power output driver (shown here as Z_A). The Zener diode clamp is used as an over-voltage clamp to protect the output when switching inductive loads. When the output voltage exceeds the Zener threshold, Q_A conducts to suppress further increase in output voltage. The fault sense and fault flag logic circuits are the same in the CA3272A and CA3292A.



Absolute Maximum Ratings

Output Voltage, V_O (CA3272A) . . . . . +60V
Output Sustaining Voltage, $V_{CE(SUS)}$ (CA3272A) 40V
Output Voltage, V_O (CA3292A) . . . . . V_{CLAMP}
Maximum Output Clamp Energy (CA3292A) . . . . . (Note 8)
Output Transient Current, (Note 1) . . . . . 1.6A Max.
Output Load Current, (Note 2) 0.7A
Supply Voltage, V_{CC} . . . . . +7V
Logic Input Voltage, V_{IN} 15V
FAULT Output Voltage, V_F 16V

Operating Conditions

Temperature Range . . . . . -40^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} ($^oC/W$)
For surface mount without added copper ground area:
CA3272AQ, CA3292AQ (PLCC) . . . . . $45^oC/W$
CA3272AM, CA3292AM (SOIC) . . . . . $56^oC/W$
For surface mount with 2 sq. in. of added copper ground area:
CA3272AQ, CA3292AQ (PLCC) . . . . . $36^oC/W$
CA3272AM, CA3292AM (SOIC) . . . . . $35^oC/W$
See Maximum Power Dissipation vs Temperature Curves, Figures 6 and 7.
Maximum Junction Temperature (Plastic Packages) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC, PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$T_A = -40^oC$ to 125^oC, $V_{CC} = 5.5V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT PARAMETERS						
Output (OFF) Current	I_{CEX}	$V_{IN} = 0.8V$; $V_{EN} = 5.5V$; (Note 4) $V_{CE} = 60V$ for CA3272A $V_{CE} = 24V$ for CA3292A	-	30	100	µA
Output Sustaining Voltage: CA3272A	$V_{CE(SUS)}$	Note 7	40	-	-	V
Output Clamp Voltage: CA3292A	V_{CLAMP}	$I_C = 300µA$; $V_{EN} = 0.8V$	28	32	36	V
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 2V$, $V_{CC} = 4.75V$, $I_C = 400mA$, $T_A = 125^oC$	-	-	0.3	V
		$I_C = 500mA$, $T_A = 25^oC$	-	-	0.4	V
		$I_C = 600mA$, $T_A = -40^oC$	-	-	0.5	V
LOGIC INPUT THRESHOLDS						
Input Low Voltage	V_{IL}	$V_{CC} = 3.5V$	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	V
Input Low Current	I_{IL}	$V_{IN} = V_{EN} = 0.8V$; $V_{CC} = 4.75V$	10	45	70	µA
Input High Current	I_{IH}	$V_{IN} = V_{EN} = 5.5V$	10	45	70	µA
SUPPLY CURRENT						
All Outputs ON	$I_{CC(ON)}$	$V_{IN} = V_{EN} = 5.5V$; $I_{OUTA} = I_{OUTB} = I_{OUTC} = I_{OUTD} = 400mA$	-	-	65	mA
All Outputs OFF	$I_{CC(OFF)}$	$V_{IN} = 0V$	-	-	10	mA
PROPAGATION DELAY						
Turn-ON Delay	t_{PHL}	$I_{LOAD} = 500mA$	-	3	10	µs
Turn-OFF Delay	t_{PLH}	$I_{LOAD} = 500mA$	-	3	10	µs
FAULT PARAMETERS						
Output Low Current, $I_{F(SINK)}$ (with Fault)	I_{OL}	$V_{IN} = 0.8V$; $V_{EN} = 2.0V$; $V_F = 4V$ V_{OUT} = Low = 1V; (Note 5)	1	2	4	mA
Output High Current, $I_{F(LK)}$	I_{OH}	No Fault (Note 5)	-	-	20	µA
Output Low Voltage	V_{OL}	External Load Equal Min. I_{OL}	-	0.2	0.4	V
Output Driver Fault Sense, High Threshold (Open)	V_{HTHD}	$V_{IN} = 0.8V$; $V_{EN} = 2V$ (Note 6)	3	4	5.5	V

Electrical Specifications T_A = -40°C to 125°C, V_{CC} = 5.5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Driver Fault Sense, Low Threshold (Short)	V_{LTHD}	V_{IN} = V_{EN} = 2V (Note 6)	3	4	5.5	V
PROTECTION PARAMETERS						
Over-Current Limiting	I_{LIM}	V_{IN} = V_{EN} = 2V, V_{OUT} = 4Ω to 16V	0.7	-	Note 1	A
Over-Temperature Limiting (Junction Temperature)	T_{LIM}		-	165	-	°C
Over-Temperature Limiting, Hysteresis	T_{HYS}		-	15	-	Δ°C
DESIGN PARAMETERS						
Input Capacitance	C_{IN}		-	3	-	pF
Enable Capacitance	C_{EN}		-	4.6	-	pF

NOTES:

1. Output Transient Currents are controlled by on-chip limiting for each output. Under short-circuit conditions with voltage applied to the collector of the output transistor and with the output transistor turned ON, the current will increase to 1.2A, typical. Over-Current Limiting protects a short circuit condition for a normal operating range of output supply voltage. During a short circuit condition, the output driver will shortly thereafter (approximately 5ms) go into Over-Temperature Shutdown. While Over-Current Limiting may range to peak currents as high as 1.6A, each output will typically withstand a direct short circuit at normal single battery supply levels. Excessive dissipation before thermal shutdown occurs may cause damage to the chip for supply voltages greater than 16V. When sequentially switched, the outputs are rated to withstand peak current, cold turn-on conditions of lamp loads such as #168 or #194 lamps.
2. The total DC current with all 4 outputs ON should not exceed the total of (4 x 0.7A + Max. I_{CC}) ~ 2.85A. This level of current will significantly increase the chip temperature due to increased dissipation and may cause thermal shutdown in high ambient temperature conditions (See Absolute Maximum Ratings for Dissipation). Any one output may be allowed to exceed 0.7A but may be subject to Over-Current Limiting above the I_{LIM} minimum limit of 0.7A. No single output should be loaded to more than Over-Current Limiting above the I_{LIM} minimum limit of 0.7A. As a practical limit, no single output should be loaded to more than 1A maximum.
3. The PLCC and SOIC packages have power lead frame construction through the ground pins to conduct heat from the frame to the PC Board ground area. Thermal resistance, θ_{JA} is given for a surface mount of the 28 lead PLCC and the 28 lead SOIC packages on a 1 oz. copper PC board with minimal ground area and with a 2 square inches of ground area.
4. I_{CEX} is the static leakage current at each output when that output is OFF (ENABLE Low). Refer to the Figure 3 illustration of an output stage. The value of I_{CEX} is both the leakage into the output driver and a pull-down current sink, $I_{O(SINK)}$. The purpose of the current sink is to detect open load conditions.
5. The I_{OL} value of "Output Low Current, $I_{F(SINK)}$" at the FAULT pin is both the static leakage of the output driver Q_F and the current sink, $I_{F(SINK)}$. The current sink is active only when a fault exists. When no fault exists, the I_{OH} current at the FAULT pin is the maximum leakage current, $I_{F(LK)}$. Refer to Figure 2 for an illustration of the FAULT output and associated external components. Refer to FAULT LOGIC TABLE for Fault Modes.
6. The Voltages, V_{HTHD}, V_{LTHD} are the comparator threshold reference values (Min. and Max. Range) sensed as a high and low state transitions for voltage forced at the outputs. V_{HTHD} indicates an open load fault when the output is decreased to less than the threshold. V_{LTHD} indicates a shorted load when the output is increased greater than the threshold. The output voltage is changed until the FAULT pin indicates a Low (Fault). Refer to Figure 2 for test value of external resistor. Refer to I_{OL} and I_{OH} FAULT PARAMETERS Test Limits to determine V_{OL} and V_{OH} at the FAULT pin.
7. Tested with 120mA switched off in a Load of 70mH and 32Ω series resistance;
   CA3272A: Outputs clamped with an external Zener diode, limiting V_{OUT} to the $V_{CE(SUS)}$ maximum rating of +40V.
   CA3292A: Outputs limited to the V_{CLAMP} voltage by the internal collector-to-base Zener diode and output transistor clamp.
8. The single pulse clamp energy rating for the CA3292A is defined over a range of operating conditions. The Clamp Energy is a function of the Load Inductance, Load Resistance, Clamp Voltage, Supply Voltage, the Saturated ON Resistance (V_{SAT}) and the Steady State Load Current at the instant of Turn-OFF. Refer to Figure 5 for the Safe Operating Area when driving inductive loads. Rating limits for Energy vs Single Pulse Width Time are plotted for different coil values. Refer to Application Note - AN9416 for pulse energy calculation methods.

Applications

The CA3272A and CA3292A are quad-gated inverting low-side power drivers with a fault diagnostic flag output. Both circuits are rated for 125^{o}C ambient temperature applications and have current limiting and thermal shutdown. While functionally similar to the CA3262AQ, they differ in the mode of over-voltage protection and have the added feature of a FAULT flag output. Also, as shown in Figure 1, the inputs to channels A, B, C, D and ENABLE have internal pulldowns to turn “OFF” the outputs when the inputs are floating.

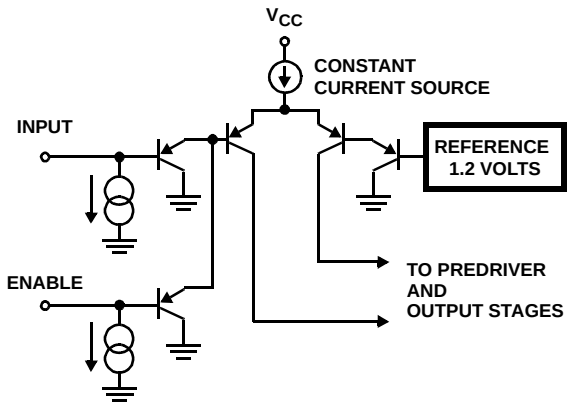


FIGURE 1. SCHEMATIC OF ONE INPUT STAGE

As noted in the Block Diagrams, the CA3292A is equivalent to the CA3272A except that it has internal clamp diodes on the outputs to handle inductive switching pulses from the output load. The structure of each CA3292A output includes a Zener diode from collector-to-base of the output transistor. This is a different form of protection from other quad drivers with current steering clamp diodes on each output, paired to one of two “CLAMP” output pins. The CA3292A output transistor will turn-on at the Zener diode clamp voltage threshold which is typically 32V and the output transistor will dump the pulse energy through the output driver to ground.

Each output driver is capable of switching 600mA load currents and operate at 125^{o}C ambient temperature without interaction between the outputs. The CA3272A and CA3292A can drive four incandescent lamp loads without modulating their brilliance when the “cold” lamps are energized. The outputs can be connected in parallel to drive larger loads. Over-current or short circuit output load conditions are fault protected by current limiting with a typical limit value of 1.2A. The current limiting range is set for 0.6A to 1.6A. The output stage does not change state (oscillate) when in the current limit mode.

FAULT LOGIC TABLE

IN	OUT	FAULT	MODE
H	L	H	Normal
H	H	L	Over Current, Over Temperature Open Load or Short to Power Supply
L	L	L	
L	H	H	Normal

Any one output that faults (see Fault Logic Table) will switch the FAULT output at pin 1 to a constant current pull-down.

The Fault Logic circuit, as shown in the Block Diagram for the CA3292A, applies to both the CA3272A and CA3292A. The Fault Sense circuits do not override or control the power switching circuits of the IC. Their primary function is to provide an external diagnostic fault flag output. Each Power Switching Channel has diagnostic fault sensing input to the Fault Logic. The Fault Logic block of the functional Block Diagram illustrates the logic functions associated with Fault detection. The diagnostic output for each of the four channels of switching is processed through the fault logic circuit associated with each channel. It is then passed to an OR gate which controls the FAULT flag output transistor, Q_F thru A 2 input AND gate.

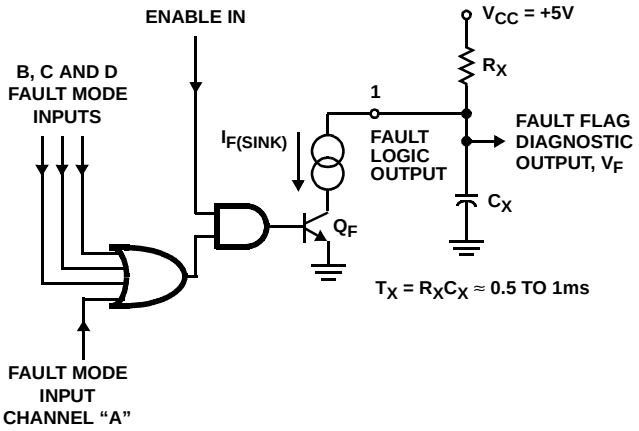


FIGURE 2. EXTERNAL FAULT OUTPUT CIRCUIT AND $I_{F(SINK)}$ AS FAULT SINK PULLDOWN CURRENT, WHICH IS ACTIVATED BY TRANSISTOR, Q_F, WHEN A FAULT EXISTS

The ENABLE input is common to each of the 4 power switches and also disables the FAULT flag output at the 2 input AND gate when it is low. The Fault Logic circuit senses the IN and OUT states and switches Q_F “ON” if a fault is detected. Transistor Q_F activates a sink current source to pull-down the FAULT pin to a 0 (low) state when the fault is detected. Both shorted and open load conditions are detected.

It is normal for thermal shutdown and current limiting to occur sequentially during a short circuit fault condition. A precaution applies for potential damage from high transient dissipation during thermal shutdown. (See Note 1 following the Electrical Specifications Table).

Each of the outputs are independently protected with over-current limiting and over-temperature shutdown with thermal hysteresis. If an output is shorted, the remaining outputs function normally unless the temperature rise of the other output devices can be made to exceed their shutdown temperature of 165^{o}C typical. When the junction temperature of a driver exceeds the 165^{o}C thermal shutdown value, that output is turned off. When an output is shutdown, the resulting decrease in power dissipation allows the junction temperature to decrease. When the junction temperature decreases by approximately 15^{o}C, the output is turned on.

The output will continue to turn on and off for as long as the shorted condition exists or until shutdown by the input logic. The resulting frequency and duty cycle of the output current flow is determined by the ambient temperature, the thermal resistance of the package in the application and the total power dissipation in the package. Since each output is independently protected, the frequency and duty cycle of the current flow into multiple shorted outputs will not be related in time. Long lead lengths in the load circuit may lead to oscillatory behavior if more than two output loads are shorted.

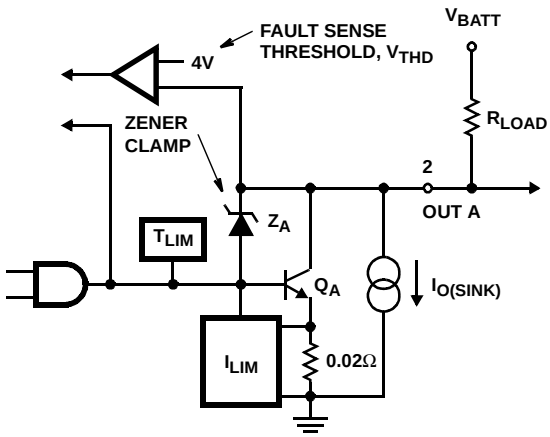


FIGURE 3. OUTPUT OPEN LOAD DETECTION WHERE $I_{O(SINK)}$ IS AN ACTIVE CURRENT SINK PULLDOWN FOR OPEN-LOAD FAULT DETECTION. THE CURRENT I_{CEX} IS $I_{O(SINK)}$ PLUS LEAKAGE CURRENTS OF THE OUTPUT DRIVER

Since a diagnostic flag indicates when an output is shorted, this information can be used as input to a microprocessor or dedicated logic circuit to provide a fast switch-off when a short occurs and, by sequence action, can be used to determine which output is shorted. A fault condition in any output load will cause the FAULT output to switch to a logic “low”. Since a fault condition may be detected during switching, use of an appropriate size capacitor to filter the FAULT output is recommended. The recommended FAULT output circuit is shown in Figure 2. This will prevent the FAULT output voltage from reaching a logic level “0” within the maximum switching time.

The FAULT detection circuitry compares the state of the input and the state of the output for each A, B, C and D channel. The output is considered to be in a high state if the voltage exceeds the typical FAULT threshold reference voltage, V_{THD} of 4V. If the output voltage is less than V_{THD}, the output is considered to be in a low state. For example, if the input is high and the output is less than V_{THD}, a normal “ON” condition exists and the FAULT output is high. If the input is high and the output is greater than V_{THD}, a shorted load condition is indicated and the FAULT output is low. When the input is low and the output is greater than V_{THD}, a normal “OFF” condition is indicated and the FAULT output is high. If the input is low and the output is less than V_{THD}, an open load condition exists and the FAULT output is low. The Output Driver Fault Sense state is determined by high and low comparator threshold limits which are defined in the Fault Parameters section of the Electrical Specifications.

The FAULT output diagram of Figure 2 shows the circuit component interface for sensing a diagnostic fault condition. As noted, the time constant of $T_X = R_X C_X$ should be greater than the ON-OFF output switching times to avoid false fault readings during switching. For applications requiring fast period repetition rates, the maximum time constant should be significantly less than the period of switching. The shortest practical time constant is preferred to limit the duration of a fault condition.

To match a standard CMOS or TTL interface, the switched current at the FAULT pin must be converted to V_{IH} and V_{IL} voltage levels using the R_X external pullup resistor. The minimum specified I_{OL} limit at the FAULT output defines the Low (Fault) state which is used to test for a V_{OL} maximum limit of 0.4V. This makes the calculation for the V_{IL} input level relatively simple. Where V_F is the FAULT output voltage, V_{CC} is the power supply voltage, R_X is the pullup resistor to V_{CC} from the FAULT pin and I_{OL} is the fault condition sink current, $I_{O(SINK)}$, the low state equation is:

$$V_F = V_{CC} - R_X I_{OL} \leq V_{IL} \quad \text{(EQ. 1)}$$

As an example: Since TTL is the worst case for a low state, V_{IL} = 0.8V. Using V_{CC} = 5V, maximum $V_F = V_{OL}$ = 0.4V and minimum I_{OL} = 1mA for the CA3272A and CA3292A. At the worst case limit, the minimum value of R_X is:

$$R_X = (V_{CC} - V_{IL})/I_{OL} = (5 - 0.4)V/0.001mA = 4.6k\Omega$$

The preferred value for R_X would be greater than the values calculated.

For the logic V_{IH} High (normal state),

$$V_F = V_{CC} - R_X I_{OH} \geq V_{IH} \quad \text{(EQ. 2)}$$

Where the I_{OH} current is the specified leakage current, $I_{F(LK)}$ at the FAULT pin, it remains to check the calculated value for R_X as a leakage current times the chosen pullup resistance. To determine that the minimum V_{OH} from the FAULT pin is greater than V_{IH} to an external logic match, V_F is calculated using Equation 2. For example, using the minimum R_X resistor value calculated for the CA3272A,

$$V_F = [5 - (4.6k\Omega \times 20\mu A)] = 4.9V$$

which is more than suitable for CMOS or TTL Input switching levels; suggesting that a larger value of R_X (such as 10kΩ) could be used for a better noise margin in the Low fault state.

To detect an open load, each output has an internal low-level current sink, shown in Figure 3, which acts as a pull-down under open load fault conditions and is always active. The magnitude of this current plus any leakage associated with the output transistor will always be less than 100µA. (The data sheet specification for I_{CEX} includes this internal low-level sink current). The output load resistance must be chosen such that the voltage at the output will not be less than V_{THD} when the I_{CEX} sink current flows through it under worse case conditions with minimum supply voltage. For example, assume a 6.5V minimum driver output supply voltage, a FAULT threshold reference voltage of V_{THD} = 5.5V and an output current sink of I_{CEX} = 100µA. Calculate the maximum load resistance that will

not result in a FAULT output low state when the output is OFF.

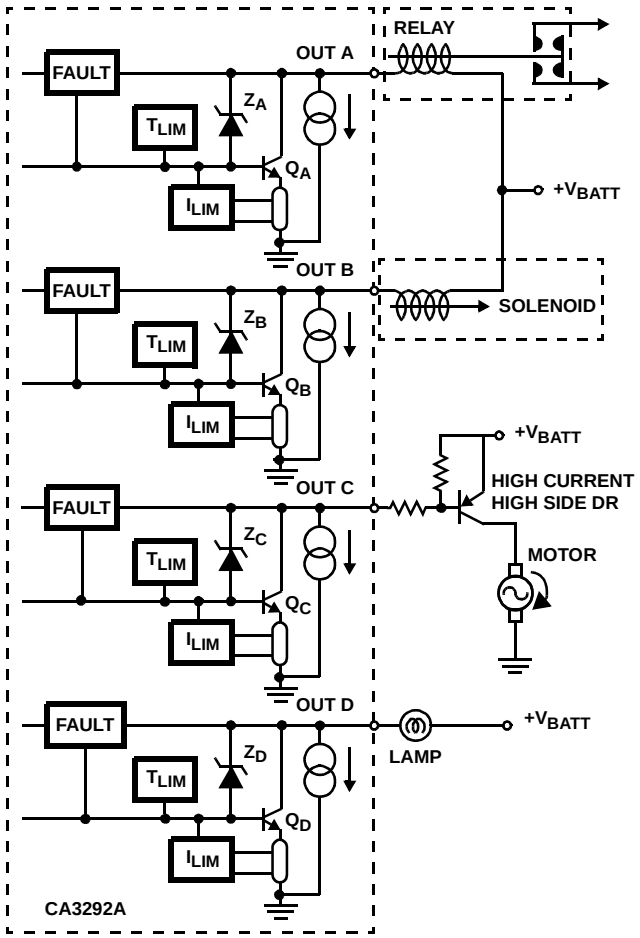
$$R_{LOAD}(max) = [V_{SUPPLY}(min) - V_{THD}(max)] / I_{CEX}(max) \quad \text{(EQ. 3)}$$

$$R_{LOAD}(max) = (6.5V - 5.5V) / 100\mu A = 10k\Omega \quad \text{(EQ. 4)}$$

Since the CA3272A do not have on-chip diodes to clamp voltage spikes which may be generated during inductive switching of the load circuit, an external Zener diode (30V or less is recommended) should be connected between the output terminal and ground. Only those outputs used to switch inductive loads require this protection. Note that since the rate of change of output current is very high, even small values of inductance can generate voltage spikes of considerable amplitude on the output terminals which may require clamping. External free-wheeling diodes returned to the supply voltage are generally not acceptable as inductive clamps if the supply voltage exceeds 30V during transients. Typical loads for either the CA3272A or CA3292A are shown in the application circuit of Figure 4A. Where inductive loads are driven from outputs A and B, no external Zener diode clamp is needed for the CA3292A but is required for the CA3272A as shown in Figure 4B.

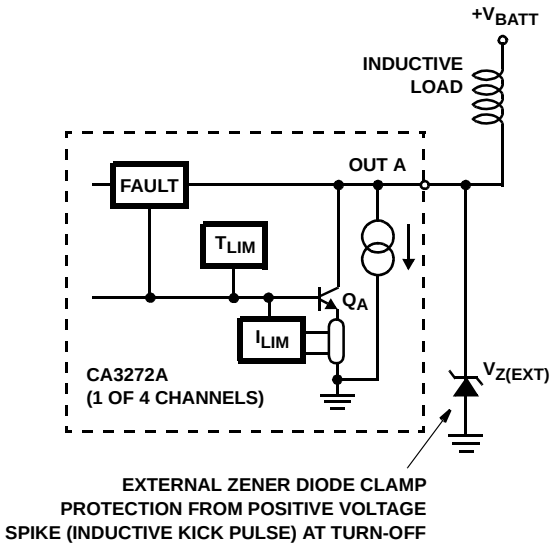
The CA3272A and CA3292A are supplied in specially configured power packages to conduct heat from the junction through the mounting structure and device leads to the PC Board. The ground leads are directly connected to the mounting pad of the chip. The junction-to-air thermal resistance, θ_{JA} may be significantly improved by suitable layout design of the PC board to which the package is soldered. Two or more square inches of PC Board ground area next to the device ground pins is recommended. The PC Board ground layer should be on the device side of the board with open space for heat radiation.

Refer to Application Note AN9416 for additional thermal information. Further information is provided on pulse energy calculation methods for inductive load applications with detail explaining the Safe Operating Area shown in Figure 5. The SOA area for single energy transients is below the dotted lines for the given ambient temperature conditions. The energy locus plots of the three inductive coils were made for arbitrarily chosen values of inductance and are shown here for reference information. The RL time constant, ambient temperature, clamp voltage and the stored energy in the coil determine the SOA limits.



NOTE: The internal drive circuit with self protection and fault output is the CA3292A with the over voltage Zener diode clamp.

FIGURE 4A. TYPICAL APPLICATION CIRCUIT SHOWING OUTPUT LOAD CONTROL CAPABILITY OF THE CA3272A OR CA3292A



NOTE: The $V_{CE(SUS)}$ voltage rating is the maximum voltage for full load switching.

FIGURE 4B. CA3272A OVER-VOLTAGE PROTECTION IS AN EXTERNAL ZENER DIODE CLAMP WHERE $V_{Z(EXT)} \leq V_{CE(SUS)}$

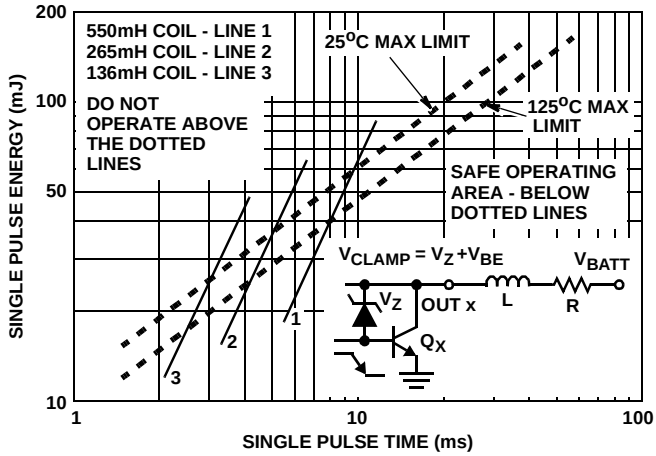


FIGURE 5. CA3292A SINGLE PULSE INDUCTIVE FLYBACK CLAMP ENERGY SOA RATING CHART FOR EACH OUTPUT DRIVER

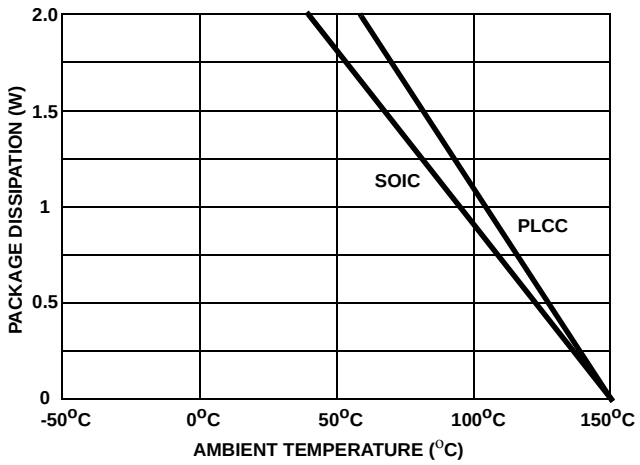


FIGURE 6. MAXIMUM POWER DISSIPATION RATING vs TEMPERATURE FOR THE CA3272AQ, CA3292AQ PLCC PACKAGE AND THE CA3272AM, CA3292AM SOIC PACKAGE WITH NO ADDITIONAL PC BOARD AREA FOR HEAT SINKINGS

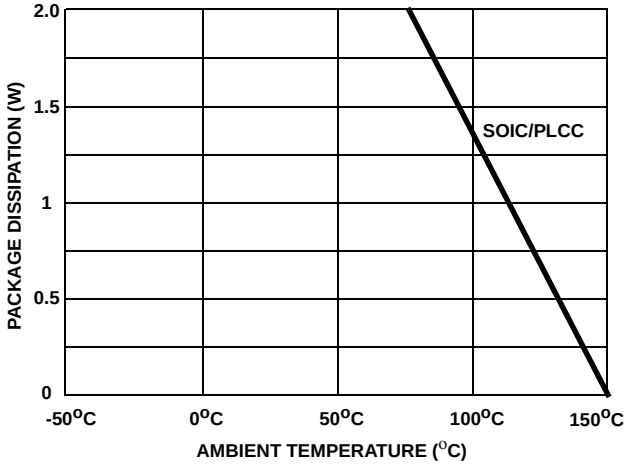
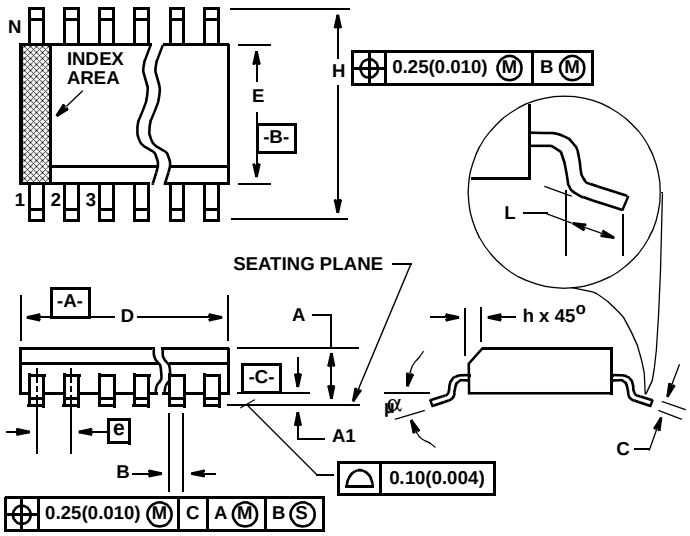


FIGURE 7. MAXIMUM POWER DISSIPATION RATING vs TEMPERATURE FOR THE CA3272AQ, CA3292AQ PLCC PACKAGE AND THE CA3272AM, CA3292AM SOIC PACKAGE WITH 2 SQ. IN. OF 1 OZ. COPPER PC BOARD AREA FOR HEAT SINKING

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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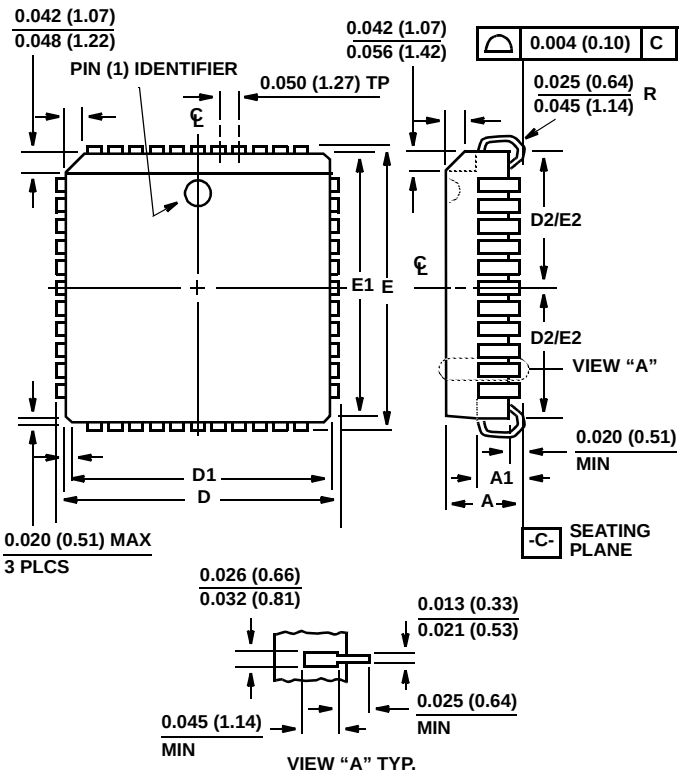
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.