HS-6564RH

NOT RECOMMENDED FOR NEW DESIGNS
See HS-65647RH or
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

September 1997

Radiation Hardened 8K x 8, 16K x 4 CMOS RAM Module

Features

- Radiation Hardened EPI CMOS
  - Total Dose 1 x 10^5 RAD (Si)
  - Transient Upset > 1 x 10^8 RAD (Si)/s
  - Latch-Up Free to > 1 x 10^{12} RAD (Si)/s
- Low Power Standby 4.4mW Maximum
- Low Power Operation 308mW/MHz Maximum
- Data Retention 3.0V Minimum
- TTL Compatible In/Out
- Three State Outputs
- Fast Access Time 250ns Maximum
- Military Temperature Range -55°C to +125°C
- On Chip Address Registers
- Organizable 8K x 8 or 16K x 4
- 40 Pin DIP Pinout 2.000" x 0.900"

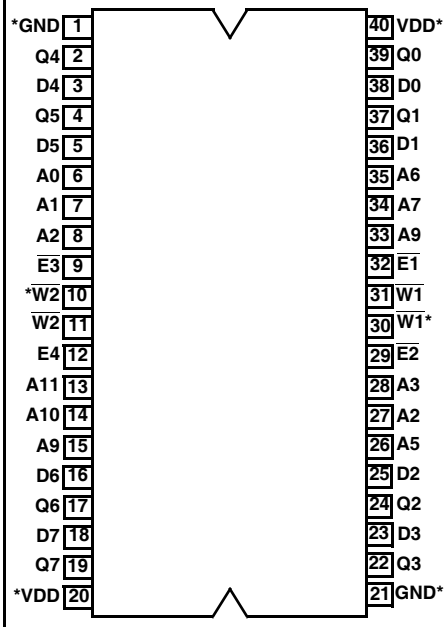
Description

The HS-6564RH is a radiation hardened 64K bit, synchronous CMOS RAM module. It consists of 16 HS-6504RH 4K x 1 radiation hardened CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The individual RAMs are fabricated using the Intersil radiation hardened guard ring, self-aligned silicon gate technology. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are seperate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile readswrite memory by using very small batteries mounted directly on the memory circuit board.

Pinout

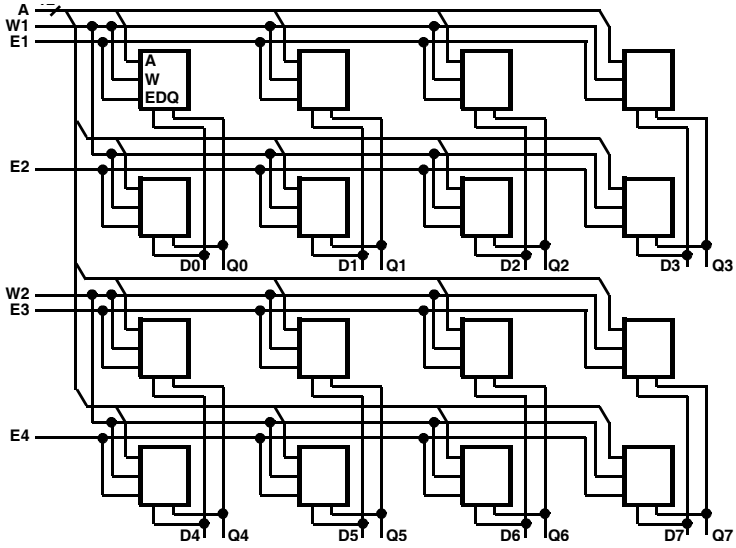
HS5-6564RH 40 PIN CERAMIC MODULE
INTERNAL PACKAGE CODE "HSQ"
TOP VIEW



* Pins 20 and 40 (VDD) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect both VDD pins and both Ground pins to the board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



File Number **3032.1**

Absolute Maximum Ratings

Supply Voltage . . . . . -3.0V to +7.0V
Input or Output Voltage Applied . . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Junction Temperature. . . . . $+175^oC$
Lead Temperature (Soldering 10s). . . . . $+300^oC$
Typical Derating Factor . . . . . 48mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
40 Pin Ceramic Module Package	TBD	TBD

Maximum Package Power Dissipation at $+125^oC$
40 Pin Ceramic Module Package . . . . . .TBD
Gate Count . . . . . 53,336 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55^oC to $+125^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	1600	µA
Operating Supply Current (8K x 8) (Note 1)	IDDOP1	f = 1MHz, IO = 0 VI = VDD or GND	-	56	mA
Operating Supply Current (16K x 4) (Note 1)	IDDOP2	f = 1MHz, IO = 0 VI = VDD or GND	-	28	mA
Data Retention Supply Current	IDDDR	IO = 0, VDD = 3.0 VI = VDD or GND	-	1200	µA
Data Retention Supply Current	VDDDR		3.0	-	V
Address Input Leakage	IIA	GND ≤ VI ≤ VDD	-20	+20	µA
Data Input Leakage (8K x 8)	IID1	GND ≤ VI ≤ VDD	-3	+3	µA
Data Input Leakage (16K x 4)	IID2	GND ≤ VI ≤ VDD	-5	+5	µA
Enable Input Leakage (8K x 8)	IIE1	GND ≤ VI ≤ VDD	-10	+10	µA
Enable Input Leakage (16K x 4)	IIE2	GND ≤ VI ≤ VDD	-5	+5	µA
Write Enable Input Leakage (Each)	IIW	GND ≤ VI ≤ VDD	-10	+10	µA
Output Leakage (8K x 8)	IOZ1	GND ≤ VO ≤ VDD	-20	+20	µA
Output Leakage (16K x 4)	IOZ2	GND ≤ VO ≤ VDD	-40	+40	µA
Input Low Voltage	VIL		-	0.8	V
Input High Level (Except $\overline{E}$ and $\overline{W}$)	VIH1		VDD -1.5	-	V
Input High Level ($\overline{E}$ and $\overline{W}$)	VIH2		VDD -1.0	-	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTES:
1. Operating supply current is proportional to operating frequency. IDDOP is specified at an operating frequency of 1MHz indicating repetitive accessing at a 1µs rate. Operating at slower rates will decrease IDDOP proportionally.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	350	ns
Address Access Time (TAVQV = TELQV + TAVEL)	TAVQV	Note 1	-	400	ns
Chip Enable Low	TELEH	Note 1	350	-	ns
Chip Enable High	TEHEL	Note 1	130	-	ns
Address Setup Time	TAVEL	Note 1	50	-	ns
Address Hold Time	TELAX	Note 1	50	-	ns
Write Enable Low	TWLWH	Note 1	150	-	ns
Write Enable Setup Time	TWLEH	Note 1	250	-	ns
Early Write Setup Time	TWLEL	Note 1	10	-	ns
Early Write Hold Time	TELWX	Note 1	100	-	ns
Data Setup Time	TDVWL	Note 1	10	-	ns
Early Write Data Setup Time	TDVEL	Note 1	90	-	ns
Data Hold Time	TWLDX	Note 1	100	-	ns
Early Write Data Hold Time	TELDX	Note 1	100	-	ns
Early Write Pulse Hold Time	TELWH	Note 1	250	-	ns

NOTE:

1. Inputs TRISE = TFALL $\leq$ 20ns: Outputs : CLOAD = 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Address Input Capacitance	CIA	f = 1MHz, VI = VDD or GND	-	200	pF
Data Input Capacitance (8K x 8)	CID1	f = 1MHz, VI = VDD or GND	-	50	pF
Data Input Capacitance (16K x 4)	CID2	f = 1MHz, VI = VDD or GND	-	100	pF
Enable Input Capacitance (8K x 8)	CIE1	f = 1MHz, VI = VDD or GND	-	160	pF
Enable Input Capacitance (16K x 4)	CIE2	f = 1MHz, VI = VDD or GND	-	80	pF
Write Enable Input Capacitance (Each)	CIW	f = 1MHz, VI = VDD or GND	-	100	pF
Output Capacitance (8K x 8)	CO1	f = 1MHz, VO = VDD or GND	-	50	pF
Output Capacitance (16K x 4)	CO2	f = 1MHz, VO = VDD or GND	-	100	pF
Output Enable Time	TELQX		-	75	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Output Disable Time	TEHQZ		-	75	ns
Data Valid to Write (Read-Modify-Write)	TQVWL		100	-	ns
Read or Write Cycle Time	TELEL		480	-	ns

NOTE:

1. Inputs: TRISE = TFALL ≤ 20ns. Outputs: CLOAD = 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

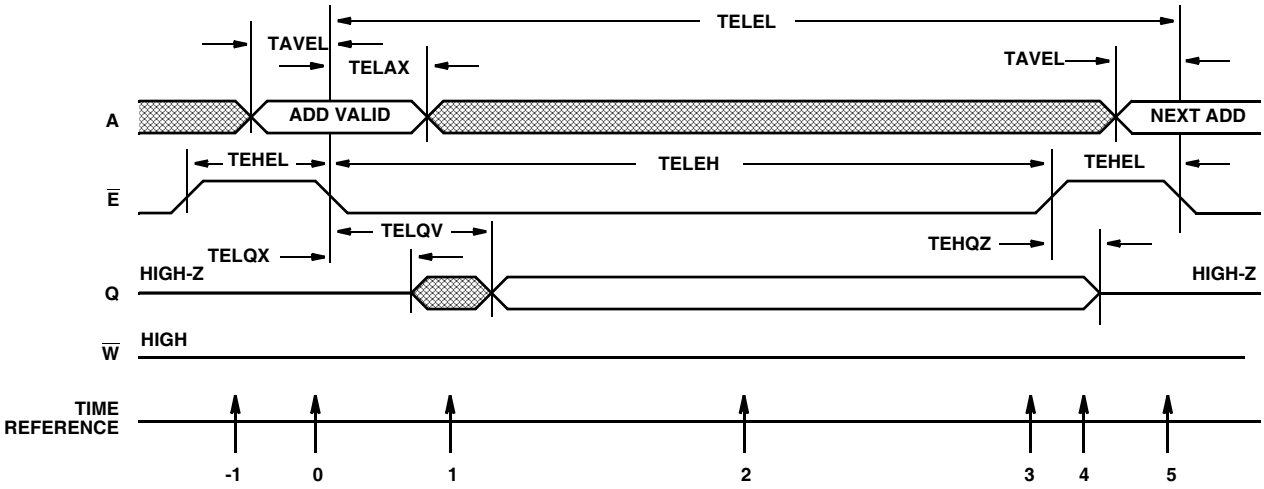
NOTE: Circuits are Burned-in as HS-6504RH discrete units, see HS-6504RH for appropriate burn-in delta information.

TABLE 6. APPLICABLE SUBGROUPS

NOTE: Quality Conformance Inspection (QCI) applies to the individual HS-6564RH devices, not to the assembled module. See HS-6504RH for further information.

Timing Waveforms

READ CYCLE



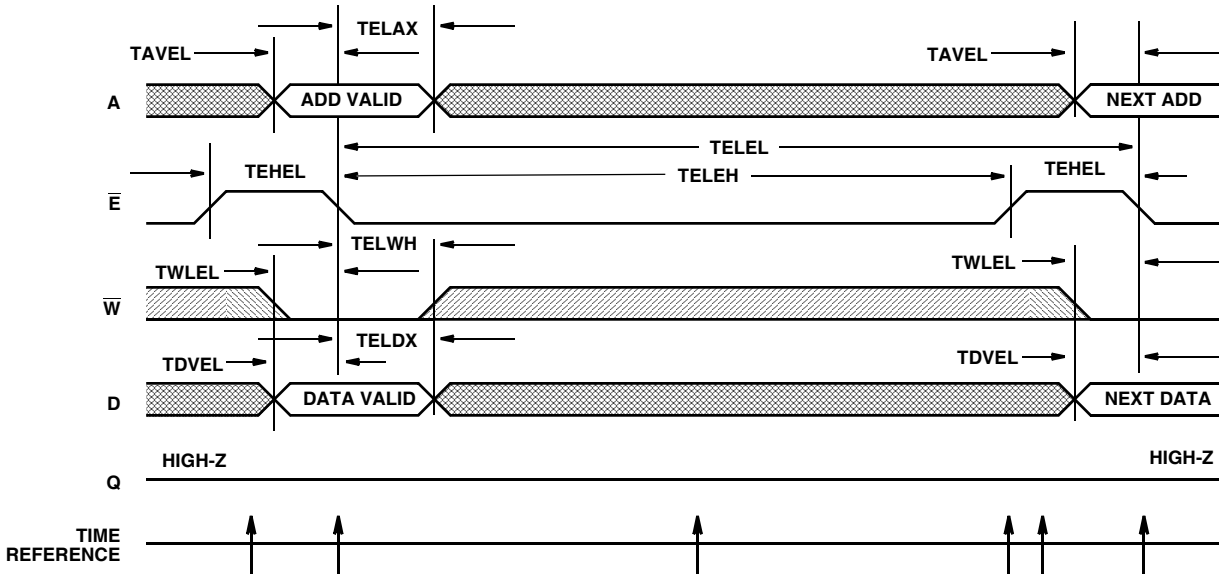
TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

EARLY WRITE CYCLE



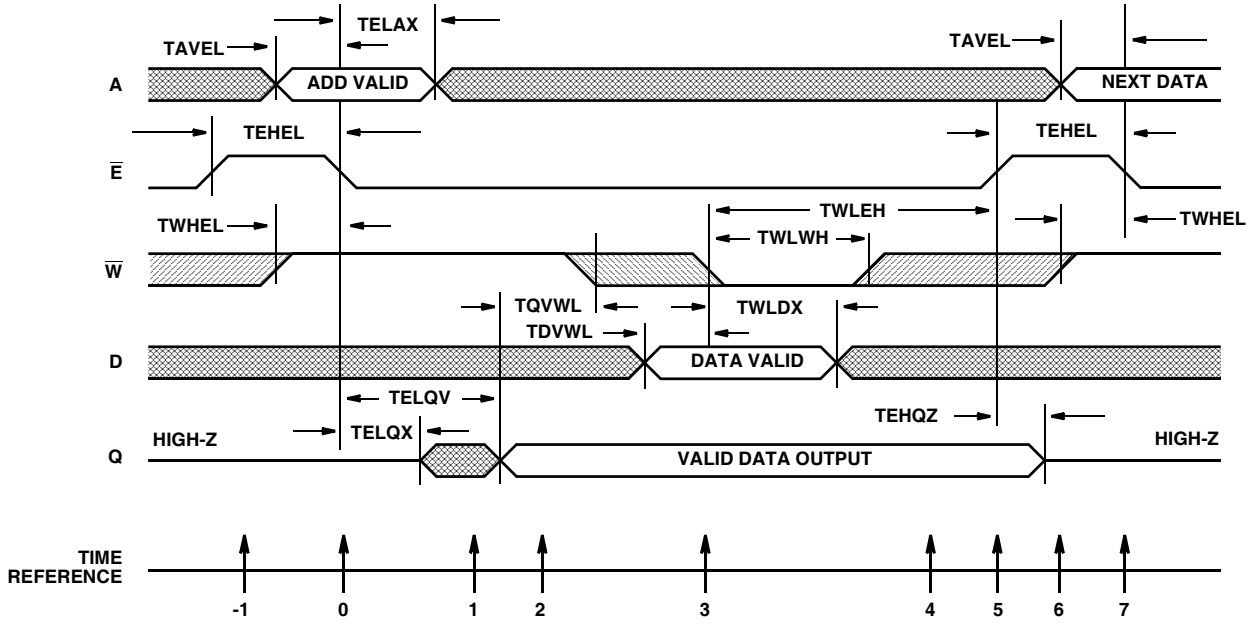
TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT Q	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D		
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Complete
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for the cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

READ MODIFY WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT Q	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D		
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid, Read and Modify Time
3	L	↓	X	V	V	Write Begins, Data is Latched
4	L	X	X	X	V	Write in Progress Internally
5	↑	X	X	X	V	Write Complete
6	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
7	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and output. The output goes to a high impedane and the RAM is ready for the next cycle.

NOTE: In the above descriptions the numbers in parenthesis (T = n) refers to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Organization Guide

To Organize 8K x 8:

Connect:	$\overline{E1}$ with $\overline{E3}$	(Pins 9 + 32)
	$\overline{E2}$ with $\overline{E4}$	(Pins 12 + 29)
	$\overline{W1}$ with $\overline{W2}$	(Pins 11 + 31)

To Organize 16K x 4:

Connect:	Q0 with Q4	(Pins 2 + 39)
	D0 with D4	(Pins 3 + 38)
	Q1 with Q5	(Pins 4 + 37)
	D1 with D5	(Pins 5 + 36)
	D2 with D6	(Pins 16 + 25)
	Q2 with Q6	(Pins 17 + 24)
	D3 with D7	(Pins 18 + 23)
	Q3 with Q7	(Pins 19 + 22)
Optional	$\overline{W1}$ may be common with $\overline{W2}$	(Pins 11 + 31)

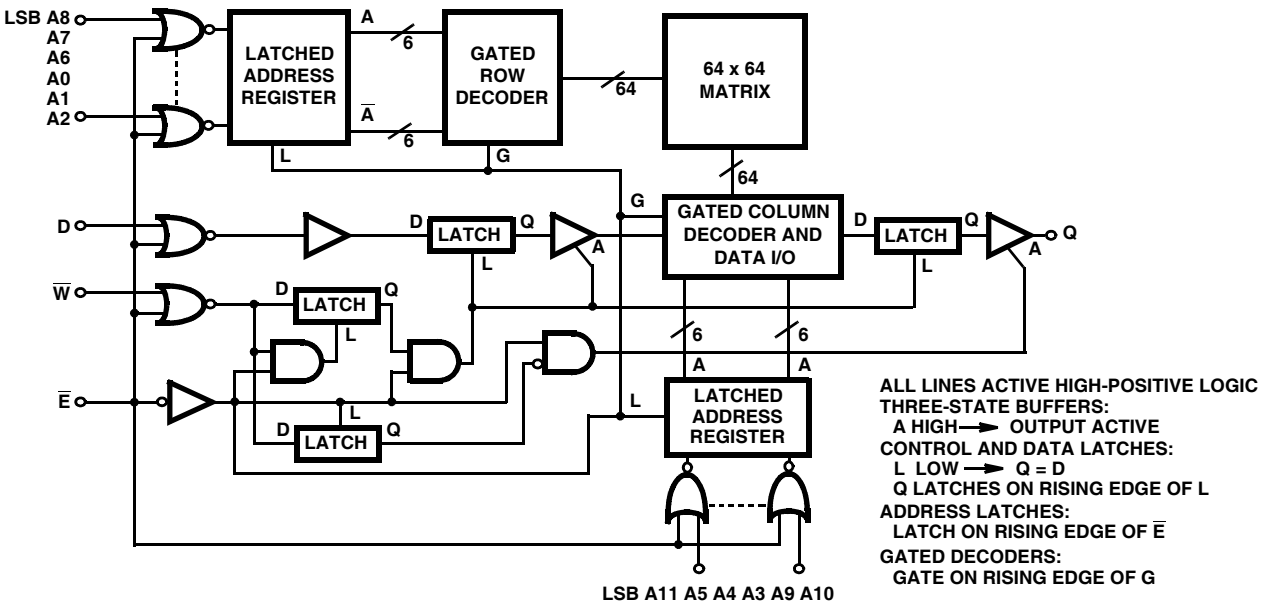
Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E1}$ and $\overline{E2}$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoid.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HS-6564RH have conductive lids. These lids are electrically floating, not connected to VDD or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

HS-6504RH (One of Sixteen)



Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HS-6564RH RAM array. Both fine line, close tolerance layout and standard “easy” layout board sizes are shown in the comparison.

We urge you to contact your local Intersil office of sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Con sider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.

64K ARRAY OR 16 4K RAMs ON A PC BOARD vs. THE HS-6564RH

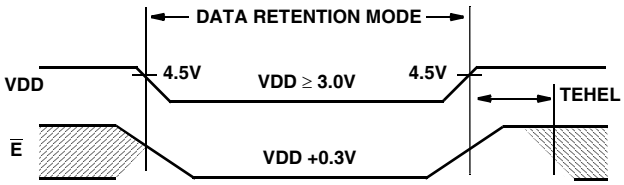
PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 Square Inches
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 Square Inches
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 Square Inches
HS-6564RH	Two Sided Mounting Multilayer Alumina Substrate	2 Square Inches

Low Voltage Data Retention

INTERSIL CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VDD +0.3V to VDD - 0.3V.
2. All other inputs should be held either high (at CMOS VDD) or at ground to minimize IDDDR.
3. Inputs which are held high (e.g. $\overline{E}$) must be kept between VDD +0.3V and 70% of VDD during the power up and power down transitions.
4. The RAM can begin operation one TEHEL after VDD reaches the minimum operating voltage (4.5 volts).

DATA RETENTION MODE



Burn-In/Irradiation Circuits

Intersil - Space Level Product Flow

HS4-6504RH LCCs are fully tested and processed through the Intersil space level (-Q) product flow (see page 8-91) and are assembled onto a ceramic substrate for the HS5-6564RH module.

Temperature Cycle - 10 Cycles

Serialization

Electrical Tests Subgroups 1, 7, 9; Read and Record Subgroup 1 only

Electrical Tests Subgroups 3, 8B, 11; Read and Record Subgroup 3 only

Electrical Tests Subgroups 2, 8A, 10; Read and Record Subgroups 2 only

Gross Leak Method 1014, 100%

Fine Lead Method 1014, 100%

Customer Source Inspection (Note 1)

External Visual Inspection Method 2009

Data package Generation (Note 3)

NOTES:

1. These steps are optional, and should be listed on the purchase order if required.
2. This data comes from the testing and processing of the HS5-6504RH LCC’s.
3. Data package contains:
   - Assembly Attributes (post seal)
   - Test Attributes (includes Group A)
   - Shippable Serial Number List
   - Radiation Testing Certificate of Conformance (Note 2)
   - Wafer Lot Acceptance Report (includes SEM report) (Note 2)
   - X-Ray Report and Film (Note 2)
   - Test Variables Data