HS-83C55RH

Radiation Hardened 16K Bit CMOS ROM

September 1997

NOT RECOMMENDED FOR NEW DESIGNS
SEE HS-65647RH or
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

Features

- Radiation Hardened EPI-CM
  - Total Dose 1 x 10^5 RAD(S
  - Transient Upset > 1 x 10^8 R
  - Latch-Up Free > 1 x 10^{12} RA
- 2048 Words x 8 Bits ROM
- Electrically Equivalent to Sandia 002
- Pin Compatible with Intel 8355
- Bus Compatible with HS-80C85RH
- Single 5 Volt Power Supply
- Low Standby Current 100μA Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two General Purpose 8-Bit I/O Ports
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range -55°C to +125°C

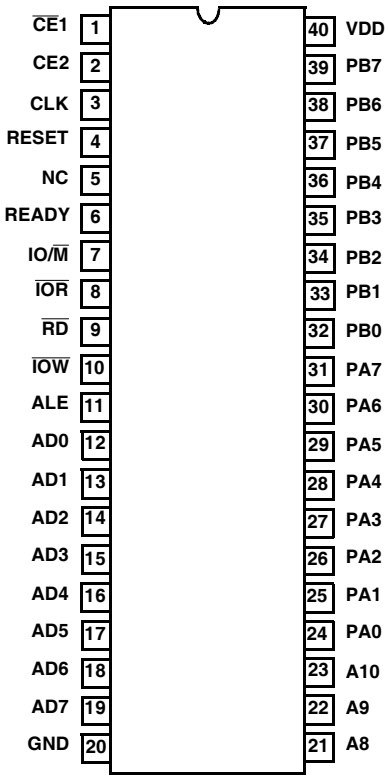
Description

The HS-83C55RH is a radiation hardened ROM and I/O chip fabricated using the Intersil radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

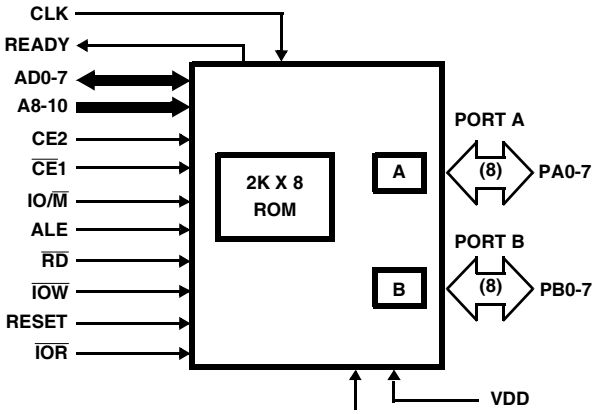
The HS-83C55RH is intended for use with the HS-80C85RH radiation hardened microprocessor system.

The ROM portion is designed as 16,384 mask programmable cells organized in a 2048 word x 8-bit format. A maximum post irradiation access time of 340ns allows the HS-83C55RH to be used with the HS-80C85RH CPU without any wait states. This ROM is designed for operation utilizing a single 5 volt power supply.

HS-83C55RH 40 LEAD BRAZE SEAL DIP
COMPLIANT OUTLINE D5, CONFIGURATION 3
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.

File Number **3045.2**

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
ALE	11	I	Address Latch Enable: When high, AD0-7, IO/$\overline{M}$, A8-0, CE2, and $\overline{CE}$1, enter the address latches. The signals (AD, IO/$\overline{M}$, A8-10, CE2, CE1) are latched in at the trailing edge of ALE.*
AD0-7	12-19	I	Address/Data Bus (Bidirectional): The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched chip enables are active, the output buffers present data on the bus.
A8-10	21, 22, 23	I	Address Bus: High order bits of the ROM address. They do not affect I/O operations.
$\overline{CE}$1,CE2	1, 2	I	Chip Enable Inputs: $\overline{CE}$1 is active low and CE2 is active high.The HS-83C55RH can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them In. If either Chip Enable input is not active, the AD0-7 and READY outputs will be in a high impedance state.
IO/$\overline{M}$	7	I	I/O Memory: If the latched IO/$\overline{M}$ is high when $\overline{RD}$ Is low, the output data comes from an I/O port. If it is low, the output data comes from the ROM.
$\overline{RD}$	9	I	Read: If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD0-7 output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD0-7 output buffers are 3-stated.
$\overline{IOW}$	10	I	I/O Write: If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD0 to be written with the data on AD0-7. The state of IO/$\overline{M}$ is ignored.
CLK	3	I	Clock: Used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$1, low, CE2 high and ALE high.
READY	6	O	READY: A 3-state output controlled by $\overline{CE}$1, CE2, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.
PA0-7	24-31	I/O	Port A: General purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD0, AD1. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD0 and AD1 low, or IO/$\overline{M}$ high, RD low, active chip enables, and AD0 and AD1, LOW.
PB0-7	32-39	I/O	Port B: This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD0 and a 0 from AD1.
RESET	4	I	Reset: An input high causes all pins in Port A and B to assume input-mode. (Clear DDR Register.)
$\overline{IOR}$	8	I	I/O Read: When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to VCC.
VDD	40	I	Voltage: +5 Volt
GND	20	I	Ground: Ground Reference.

* ALE must be clocked once after power up.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65^{o}C to +150^{o}C
Junction Temperature. . . . . +175^{o}C
Lead Temperature (Soldering 10s). . . . . +300^{o}C
Typical Derating Factor . . . . . .1.5mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25.8^{o}C/W	9.9^{o}C/W

Maximum Package Power Dissipation at +125^{o}C
Braze Seal DIP Package 1.94W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range. . . . . -55^{o}C to +125^{o}C
Input Low Voltage . . . . . .0V to +0.8V
Input High Voltage. . . . . VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Devices are Guaranteed at Worst Case Limits and Over Radiation. Dynamic Current is Proportional to Operating Frequency.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V Pin Under Test = VDD	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	1.0	µA
	IIL	VDD = 5.25V, VIN = 5.25V Pin Under Test = 0V	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-1.0	-	µA
High Level Output Voltage	VOH	VDD = 4.75V, IOH = -2.0mA	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	4.25	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IOL = 2.0mA,	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	0.5	V
Output Leakage Current	IOZL	VDD = 5.25V, VIN = 0V	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-10	-	µA
	IOZH	VDD = 5.25V, VIN = 5.25V	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	10	µA
Static Current	IDDSB	VDD = 5.25V	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	100	µA
Dynamic Current	IDDOP	VDD = 5.25V, f = 1MHz	1, 2, 3	-55^{o}C, +25^{o}C, or +125^{o}C	-	5.0	mA/MHz
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD - 0.5, VIL = 0.8V	7, 8A, 8B	-55^{o}C, +25^{o}C, or +125^{o}C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC Tests are Guaranteed Through Functional Testing with the Clock Period Equal to 500ns. TRDE + TRDF are the Only Read and Record Parameters. Output Timings are Measured with a Capacitive Load CL = 170pF, VIH = 4.25, and VIL = 0.8V

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Data Bus Float After Read	TRDF	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	0	110	ns
Read Control to Data Bus Enable	TRDE	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	10	-	ns
Clock Pulse Width Low	T1	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	40	-	ns
Clock Pulse Width High	T2	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	70	-	ns
Clock Rise and Fall Times	TR, TF	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	-	100	ns
Address to Latch Setup Time	TAL	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	60	-	ns
Address Hold Time After Latch	TLA	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	60	-	ns
Latch to Read/Write Control	TLC	9, 10, 11	-55^{o}C, +25^{o}C, +125^{o}C	140	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC Tests are Guaranteed Through Functional Testing with the Clock Period Equal to 500ns. TRDE + TRDF are the Only Read and Record Parameters. Output Timings are Measured with a Capacitive Load CL = 170pF, VIH = 4.25, and VIL = 0.8V

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Valid Out Delay from Read Control (Note 1)	TRD	9, 10, 11	-55°C, +25°C, +125°C	-	140	ns
Address Stable to Data Out Valid (Note 2)	TAD	9, 10, 11	-55°C, +25°C, +125°C	-	340	ns
Latch Enable Width	TLL	9, 10, 11	-55°C, +25°C, +125°C	120	-	ns
Read/Write Control of Latch Enable	TCL	9, 10, 11	-55°C, +25°C, +125°C	40	-	ns
Read/Write Control Width	TCC	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
Data In to Write Setup Time	TDW	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
Data In Hold Time After Write	TWD	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Write to Port Output	TWP	9, 10, 11	-55°C, +25°C, +125°C	-	300	ns
Port Input Setup Time	TPR	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
Port Input Hold Time	TRP	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
Ready Hold Time	TRYH	9, 10, 11	-55°C, +25°C, +125°C	0	160	ns
Address CE to Ready	TARY	9, 10, 11	-55°C, +25°C, +125°C	-	160	ns
Recovery Time Between Controls	TRV	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns

NOTES:

1. Or TAD - (TAL + TLC), whichever is greater.
2. Defines ALE to Data Out Valid in conjunction with TAL.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF

NOTE:

1. All measurements referenced to device ground.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

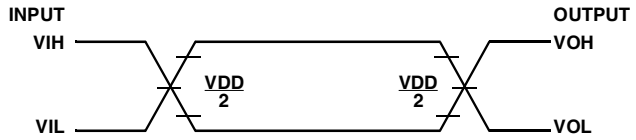
NOTE: The post irradiation test conditions and limits are the same as those listed in Table 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

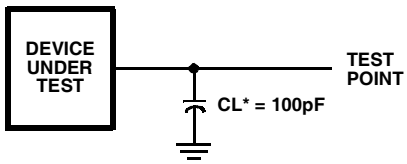
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
Input Leakage Current	IIH	± 100nA
Static Current	IDDSB	±30µA

A.C. Testing Input, Output Waveform

INPUT/OUTPUT



A.C. Testing Load Circuit (Note 1)



A.C. TESTING: All input signals must switch between VIL max and VIH min, tr and tf must be less than or equal to 15ns.

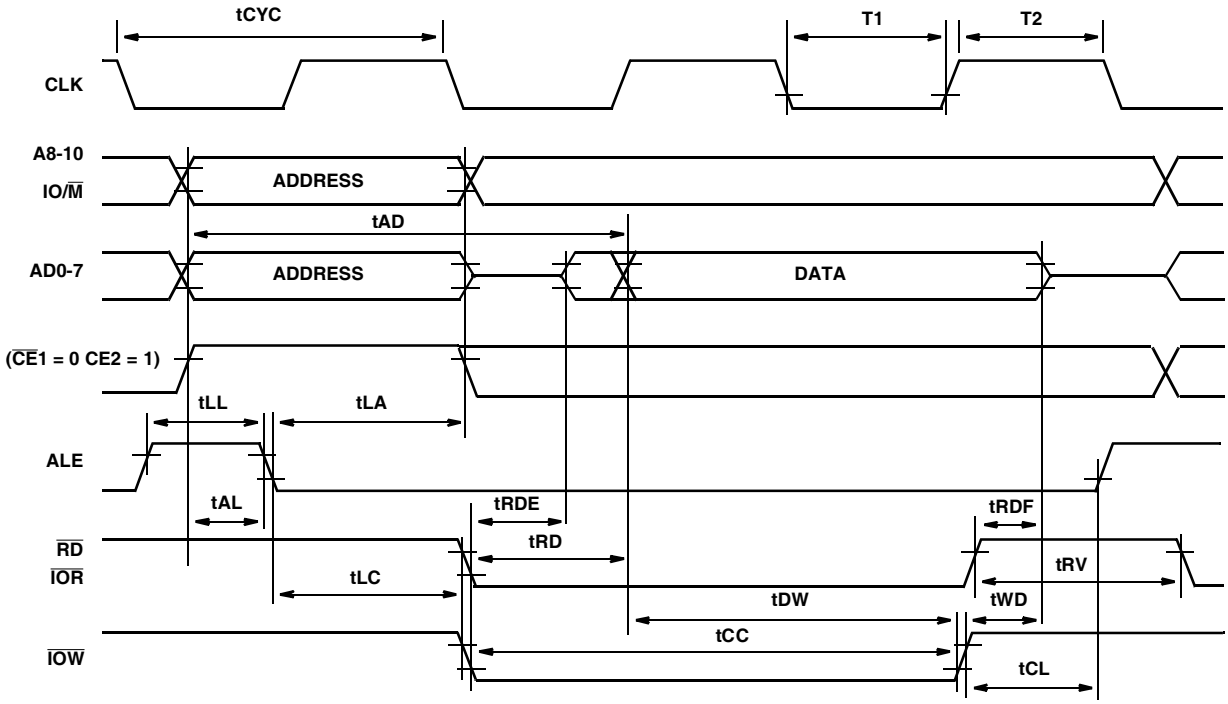
* CL includes stray and jig capacitance.

NOTES:

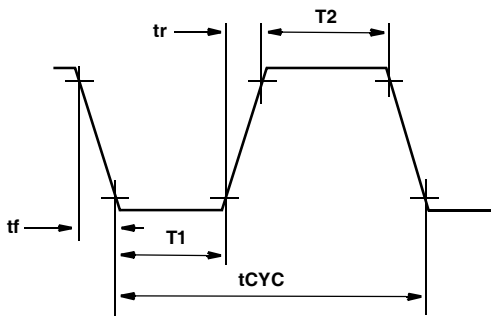
1. Output timings are measured with purely capacitive load.
2. Devices screened to more rigorous electrical specifiecations are available. Contact your nearest Intersil representative for details.

Waveforms

ROM READ AND I/O READ AND WRITE

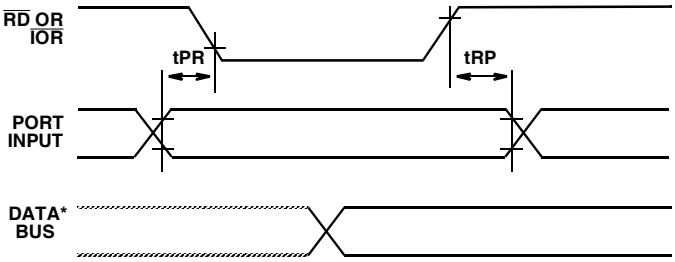


83C55RH CLOCK SPECIFICATIONS



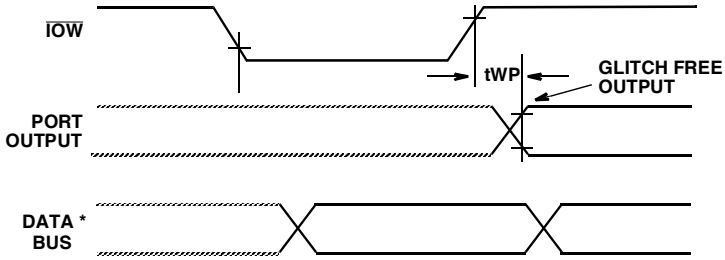
Waveforms (Continued)

INPUT MODE



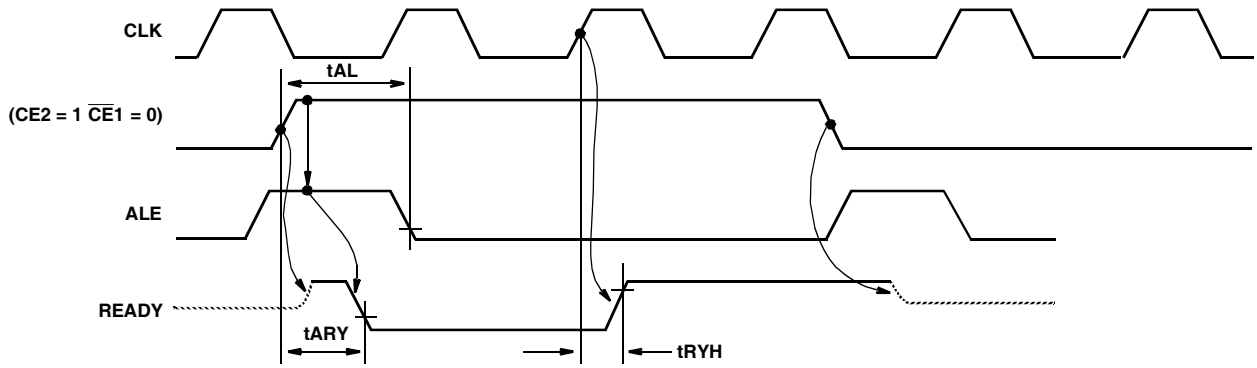
* DATA BUS TIMING IS SHOWN IN FIGURE 4.

OUTPUT MODE



* DATA BUS TIMING IS SHOWN IN FIGURE 4.

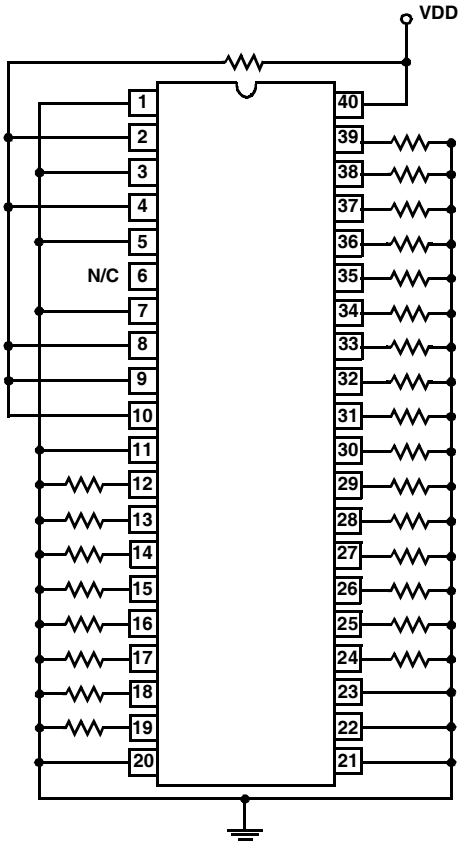
WAIT STATE



NOTE: READY = 0

Burn-In Circuits

HS-83C55RH 40 PIN DIP

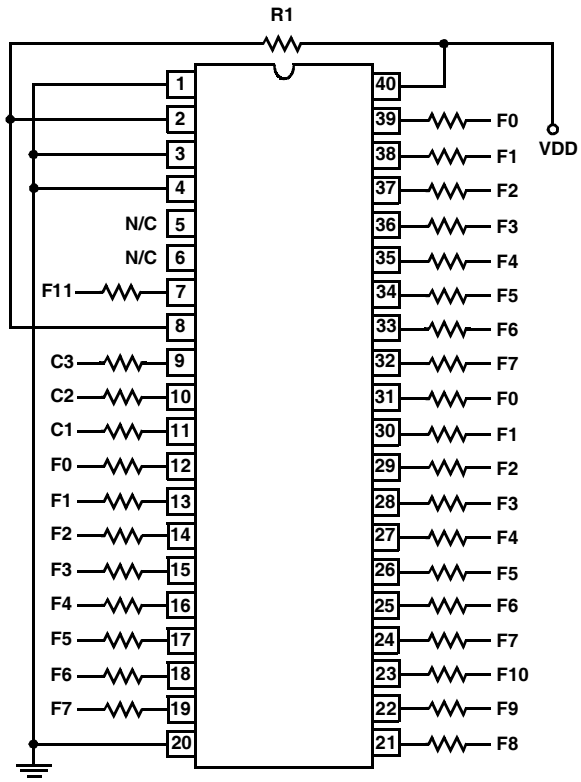


STATIC

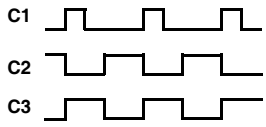
NOTES:

VDD = 10V ± 10%
16K ROM
T_A Min = 125°C
All Resistors are 10kΩ ± 10%, 1.4 Watt
Part is static sensitive. Voltage must be ramped.

HS-83C55RH 40 PIN DIP



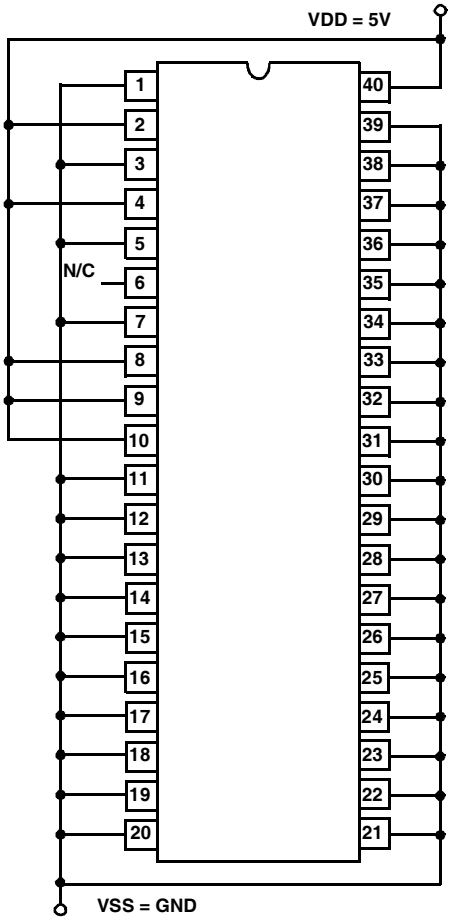
DYNAMIC



NOTES:

VDD = 10V ± 10%
16K ROM
T_A = 125°C
C2 = $\overline{C3}$
R1 = 100KΩ ± 10%, 1/4 Watt.
All other resistors 10KΩ ± 10%, 1/4 Watt.
Part is static sensitive. Voltage must be ramped.
C2 thru C3 = 200kHz and have 50% duty cycles.
C1 = 200kHz and have 20% duty cycle.
F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . . F11 = F10/2
Frequencies Fn defined by: Fn = F(n-1)/2 where F0 = 100kHz e.g. F1 = 50kHz, F2 = 25kHz . . . All Fn's have 50% duty cycle.
Part is static sensitive.

Irradiation Circuit



Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality in a ceramic DIP.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Circuit is shown on a previous page.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Intersil Representative for de-

Radiation Effects

The HS-83C55RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Intersil performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

1. Latch-up free to doses $\geq$ 1 x 10^{12} rads/sec.
2. Upset (loss of stored data $\geq$ 1 x 10^8 rads/sec.

Intersil - Space Level Product Flow -Q (Note 1)

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection Method 2010, Condition A

Gamma Radiation Assurance Tests Method 1019

Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Note 2)

Temperature Cycling Method 1010, Condition C

Constant Acceleration Method 2001, Condition E Min, Y1

Particle Impact Noise Detection Method 2020, Condition A

Electrical Tests Intersil's Option

Serialization

X-Ray Inspection Method 2012

Electrical Tests Subgroup 1; Read and Record (TO)

Static Burn-In Method 1015, Condition B, 72 Hours, +125^{o}C Minimum

Electrical Tests Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Dynamic Burn-In Method 1015 Condition D, 240 Hours, +125^{o}C (Note 3)

Electrical Tests Subgroup 1; Read and Record (T2)

Alternate Group A Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1

Burn-In Delta Calculation (TO-T2)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Electrical Test Subgroup 3; Read and Record

Alternate Group A Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1

Marking

Electrical Tests Subgroup 2; Read and Record

Alternate Group A Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1

Gross Leak Method 1014, 100%

Fine Leak Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters:
B-5/ Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11
B-6; Subgroups 1, 7, 9

Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9

External Visual Inspection Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 Shall apply; unless otherwise specified.
2. These steps are optional and should be listed on the individual purchase order(s), when required.
3. Intersil reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015
4. For group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly attributes (Post Seal)
   Test attributes (includes Group A)
   Shippable serial number list
   Radiation testing certificate of conformance
   Wafer lot acceptance report (including SEM report)
   X-ray report and film
   Test variables data

Metallization Topology

DIE DIMENSIONS:
179.1 x 189.0 x 14 ± 1mils

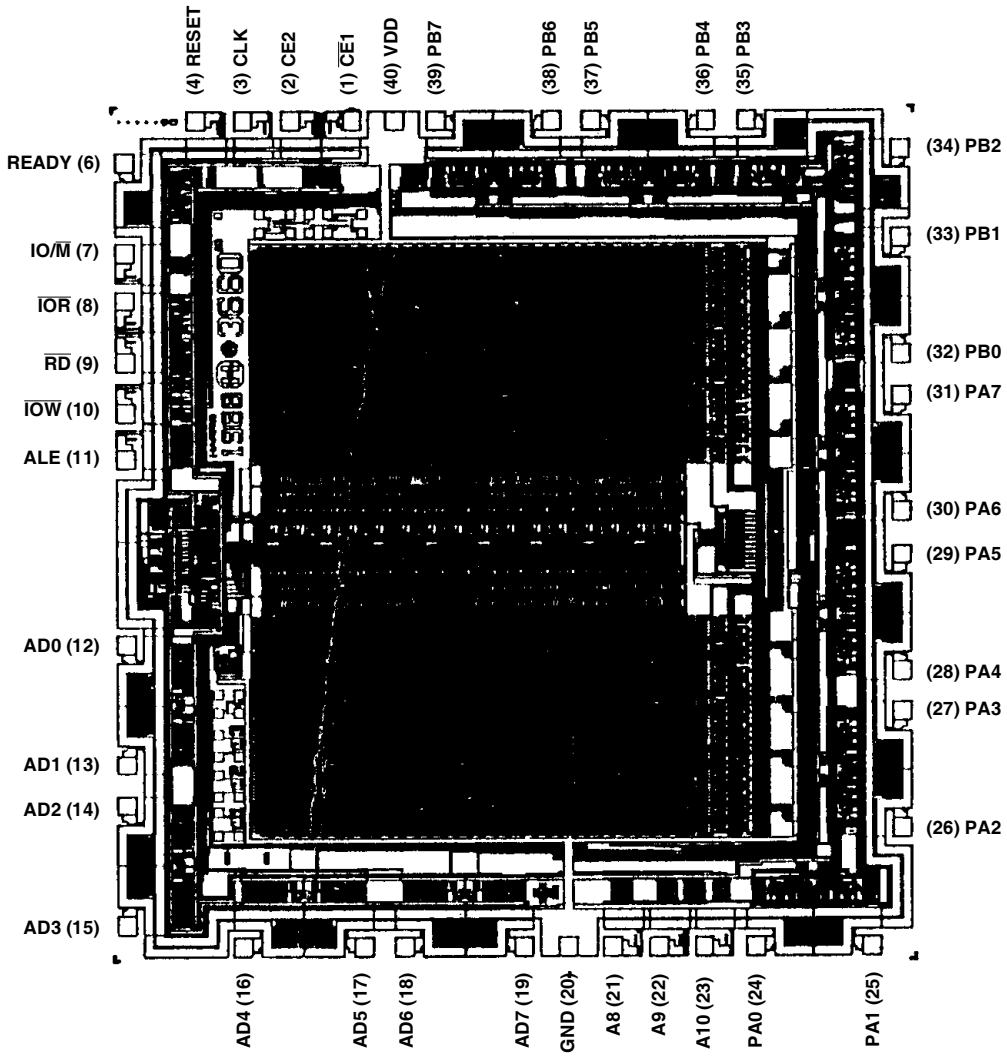
METALLIZATION:
Type: Si Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HS-83C55RH



Functional Description

ROM Section

The HS-83C55RH contains an 8-bit address latch which allows it to interface directly to the HS-80C85RH Microprocessor without additional hardware.

The R0M section of the Chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the R0M location addressed by the latched address are put out through AD0-7 output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD0-1. Two 8-bit Data Direction Registers (DDR) in the HS-83C55RH determine the input/output status of each pin in the corresponding ports. A “O” in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A “1” in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the HS-83C55RH are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR’s Cannot be read.

AD1	AD0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD0-7 is written into the I/O port selected by the latched value of AD0-1. During this operation all I/O bits of selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output). A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD0-7.

To clarify the function of the I/O ports and Data Direction Registers, Figure 1 shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch’s output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

Figure 1 also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

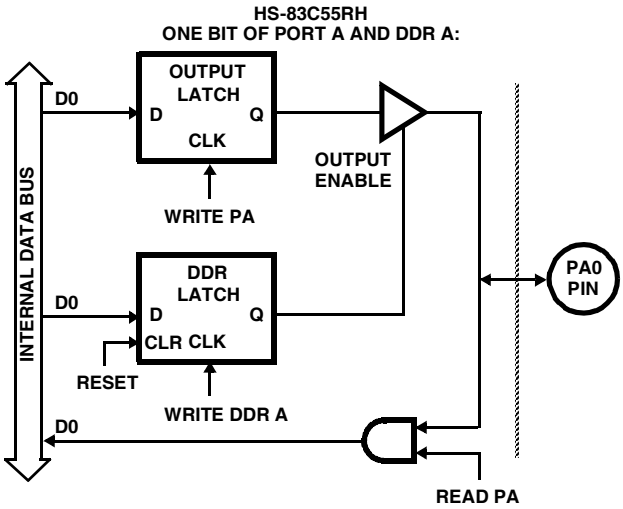
System Interface with HS-8OC85RH

A system using the HS-83C55RH can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE2 and $\overline{CE}$1. By using a combination of unused address lines A11-15 and the Chip Enable inputs, the system can use up to 5 each HS-83C55RHs without requiring a CE decoder. See Figure 3.

If a memory mapped I/O approach is used the HS-83C55RH will be selected by the combination of both the Chip Enables and IO/M using AD8-15 address lines. See Figure 2.



Write PA = ($\overline{IOW}$ = 0) (Chip Enables Active) (Port A Address Selected)
Write DDR A = ($\overline{IOW}$ = 0) (Chip Enables Active) (DDR A Address Selected)
Read PA = {[(IO/$\overline{M}$ = 1) ($\overline{RD}$ = 0)] + ($\overline{IOR}$ = 0)} (Chip Enables Active) (Port A Address Selected)

NOTE: Write PA is not qualified by IO/$\overline{M}$.

FIGURE 1. HS-83C55RH ONE BIT OF PORT A AND DDR A

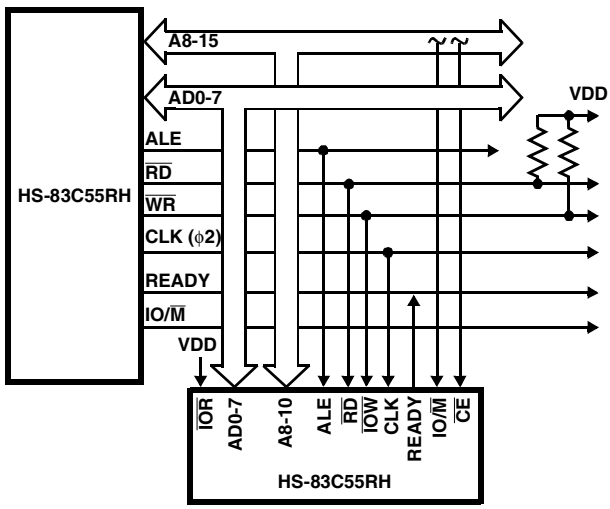
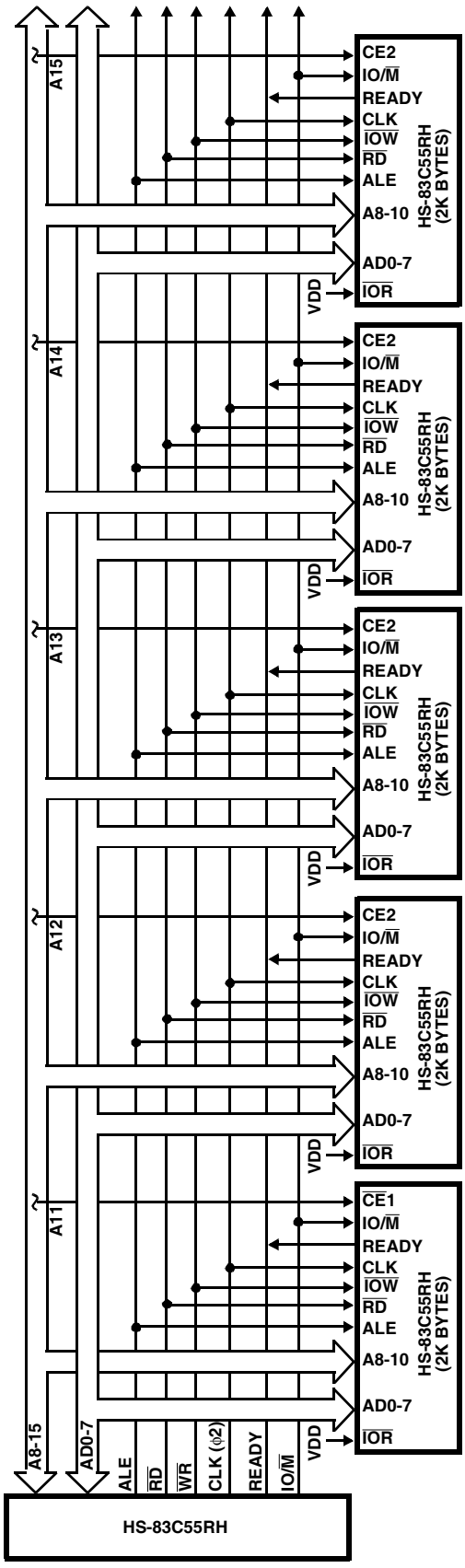


FIGURE 2. HS-83C55RH IN HS-80C85RH SYSTEM (MEMORY\MAPPED I/O)



NOTE: Use $\overline{CE}1$, for the first HS-83C55RH in the system, and CE2 for the other HS-83C55RH's. Permits up Is 5 HS-83C55RH's in a system without CE decoder.

FIGURE 3. HS-83C55RH IN HS-8OC85RH SYSTEM (STANDARD I/O)