

# CD4046BMS

## December 1992

## Features

- Very Low Power Consumption: 70μW (typ.) at VCO fo = 10kHz, VDD = 5V
- Operating Frequency Range Up to 1.4 MHz (typ.) at VDD = 10V, RI = 5k $\Omega$
- Low Frequency Drift: 0.04%/°C (typ.) at VDD = 10V
- Choice of Two Phase Comparators:
  - Exclusive-OR Network (I)
  - Edge-Controlled Memory Network with Phase-Pulse Output for Lock Indication (II)
- High VCO Linearity: <1% (typ.) at VDD = 10V
- VCO Inhibit Control for ON-OFF Keying and Ultra-Low Standby Power Consumption
- Source-Follower Output of VCO Control Input (Demod. Output)
- Zener Diode to Assist Supply Regulation
- Standardize, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

## Applications

- FM Demodulator and Modulator
- Frequency Synthesis and Multiplication
- Frequency Discriminator
- Data Synchronization
- Voltage-to-Frequency Conversion
- Tone Decoding
- FSK Modems
- Signal Conditioning

## Description

CD4046BMS CMOS Micropower Phase-Locked Loop (PLL) consists of a low power linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

**CMOS Micropower Phase Locked Loop** 

The CD4046BMS is supplied in these 16-lead outline packages:

Braze Seal DIP H4W Frit Seal DIP H1F Ceramic Flatpack H6W

## VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance  $(10^{12\Omega})$  of the VCO simplifies the design of low pass filters by permitting the designer a wide choice of resistorto-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (RS) of  $10k\Omega$  or more should be connected from this terminal to VSS. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the Intersil CD4024, CD4018, CD4020, CD4029, and CD4050. One or more CD4018 (Preset Table Divide-By-N Counter) or CD4029 (Presettable Up/Down Counter) or CD4029 (Presettable Divideby-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by "N" Counter), together with the CD4046BMS (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.



## **Phase Comparators**

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels (logic "0"  $\leq$ 30% (VDD-VSS). logic "1"  $\geq$ 70% (VDD - VSS)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase-comparator I is an exclusive -OR network; it operates analogously to an overdriven balanced mixer. To maximize the lock range, the signal and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to VDD/2. The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency ( $f_0$ ).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range (2fc).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range (2fL). The capture range is  $\leq$  the lock range.

With phase-comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between  $0^{\circ}$  and  $180^{\circ}$ , and is  $90^{\circ}$  at the center frequency. Figure 1 shows the typical, triangular, phase-to-output response characteristic of phase comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of  $f_{\circ}$  is shown in Figure 2.



### FIGURE 1. PHASE-COMPARATOR I CHARACTERISTICS AT LOW-PASS FILTER OUTPUT



## FIGURE 2. TYPICAL WAVEFORMS FOR CMOS PHASE-LOCKED LOOP EMPLOYING PHASE COMPARATOR IN LOCKED CONDITION OF ${\sf f}_{\rm o}.$

Phase comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n- type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to VDD or down to VSS, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3) state) the remainder of the time. If the signal and comparator input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase differences. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and ntype output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Figure 15 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

## **Absolute Maximum Ratings**

DC Supply Voltage Range, (VDD)0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs0.5V to VDD +0.5V
DC Input Current, Any One Input±10mA
Operating Temperature Range55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)65°C to +150°C
Lead Temperature (During Soldering)+265°C
At Distance 1/16 $\pm$ 1/32 Inch (1.59mm $\pm$ 0.79mm) from case for
10s Maximum

## **Reliability Information**

Thermal Resistance	$\theta_{ia}$	$\theta_{ic}$
Ceramic DIP and FRIT Package	80°Ć/W	20°Ć/W
Flatpack Package	70°C/W	20°C/W
Maximum Package Power Dissipation (P	D) at +125°C	;
For TA = -55°C to +100°C (Package Ty	ype D, F, K).	500mW
For TA = +100°C to +125°C (Package	Type D, F, K)	Derate
Linea	rity at 12mW	/ <sup>o</sup> C to 200mW
Device Dissipation per Output Transistor		100mW

PARAMETER         SYMBOL         CONDITIONS (NOTE 1)         SUBGROUPS         TEMPERATURE         MIN         MAX         UNIT:           Supply Current         IDD         VDD = 20V, VIN = VDD or GND         1         +25°C         -         100         µA           Input Leakage Current         IIIL         VIN = VDD or GND         VDD = 10V, VIN = VDD or GND         3         -         100         0         -         nA           Input Leakage Current         IIIL         VIN = VDD or GND         VDD = 18V         3         -55°C         -100         -         nA           Input Leakage Current         IIIH         VIN = VDD or GND         VDD = 10V         2         +125°C         -         100         nA           Output Voltage         VOL15         VDD = 15V, No Load         1, 2, 3         +25°C, +125°C, -55°C         -         50         mV           Output Voltage         VOH15         VDD = 15V, No Load (Nete 3)         1, 2, 3         +25°C, +125°C, -55°C         -         50         mV           Output Current (Sink)         IOL15         VDD = 5V, VOUT = 0.5V         1         +25°C         1.4         mA           Output Current (Sink)         IOL15         VDD = 5V, VOUT = 2.5V         1         +25°C				Gi			LIM	ITS	
	PARAMETER	SYMBOL		NOTE 1)	SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Supply Current	IDD	VDD = 20V, VIN = VD	D or GND	1	+25°C	-	10	μA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$					2	+125°C	-	1000	μΑ
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			VDD = 18V, VIN = VD	D or GND	3	-55°C	-	10	μΑ
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$					2	+125°C	-1000	-	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$				VDD = 18V	3	-55°C	-100	-	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$					2	+125°C	-	1000	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$				VDD = 18V	3	-55°C	-	100	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Voltage	VOL15	VDD = 15V, No Load	•	1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Voltage	VOH15	VDD = 15V, No Load	(Note 3)	1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.	.4V	1	+25°C	0.53	-	mA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0	0.5V	1	+25°C	1.4	-	mA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1	1.5V	1	+25°C	3.5	-	mA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.	.6V	1	+25°C	-	-0.53	mA
	Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.	.5V	1	+25°C	-	-1.8	mA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Current (Source)	IOH10	VDD = 10V, VOUT = 9	9.5V	1	+25°C	-	-1.4	mA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Output Current (Source)	IOH15	VDD = 15V, VOUT = 1	13.5V	1	+25°C	-	-3.5	mA
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	N Threshold Voltage	VNTH	VDD = 10V, ISS = -10	μΑ	1	+25°C	-2.8	-0.7	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	٩	1	+25°C	0.7	2.8	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Functional	F	VDD = 2.8V, VIN = VD	DD or GND	7	+25°C	VOH >	VOL <	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			VDD = 20V, VIN = VD	D or GND	7	+25°C	VDD/2	VDD/2	
VDD = 3V, VIN = VDD or GND         8B         -55°C           Input Voltage Low (Note 2)         VIL         VDD = 5V, VOH > 4.5V, VOL < 0.5V			VDD = 18V, VIN = VD	D or GND	8A	+125°C			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			VDD = 3V, VIN = VDD	) or GND	8B	-55°C			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5	V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5	V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13 VOL < 1.5V	3.5V,	1, 2, 3	+25°C, +125°C, -55°C	-	4	V
3 State Leakage       IOZL       VIN = VDD or GND       VDD = 20V       1 $+25^{\circ}C$ $-100$ $-$ nA         Current       VOUT = 0V       VDD = 18V       3 $-55^{\circ}C$ $-100$ $-$ nA         3 State Leakage       IOZH       VIN = VDD or GND       VDD = 20V       1 $+25^{\circ}C$ $-100$ $-$ nA         3 State Leakage       IOZH       VIN = VDD or GND       VDD = 20V       1 $+25^{\circ}C$ $-$ 100       nA         Current       VOUT = VDD       VDD = 20V       1 $+25^{\circ}C$ $-$ 100       nA	Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13 VOL < 1.5V	/DD = 15V, VOH > 13.5V, /OL < 1.5V		+25°C, +125°C, -55°C	11	-	V
Current         VOUT = 0V         2         +125°C         -1000         -         nA           VDD = 18V         3         -55°C         -100         -         nA           3 State Leakage         IOZH         VIN = VDD or GND         VDD = 20V         1         +25°C         -         100         nA           Current         VOUT = VDD         VDD = 20V         1         +25°C         -         100         nA	3 State Leakage	IOZL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
VDD = 18V         3         -55°C         -100         -         nA           3 State Leakage         IOZH         VIN = VDD or GND         VDD = 20V         1         +25°C         -         100         nA           Current         VOUT = VDD         VDD = 20V         1         +25°C         -         100         nA	Current		VOUT = 0V		2	+125°C	-1000	-	nA
3 State Leakage IOZH VIN = VDD or GND VDD = 20V 1 +25°C - 100 nA				VDD = 18V	3	-55°C	-100	-	nA
	3 State Leakage	IOZH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
1000 - 1000   2   +125°C   -   1000   nA	Current		VOUT = VDD		2	+125°C	-	1000	nA
VDD = 18V 3 -55°C - 100 nA				VDD = 18V	3	-55°C	-	100	nA

## TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

	TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)									
			GROUP A		LIM	IITS				
PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS			
Quiescent Leakage	BIAS LKG	VDD = 20V, VIN = VDD or GND	1	+25°C	-	4	mA			
Phase Comparator (Bias Amp Leakage)		PIN 14 Open Pin 5 = VDD	3	-55°C	-	4	mA			
		VDD = 20V, VIN = VDD or GND	1	+25°C	-	160	μΑ			
		PIN 14 = VSS or VDD Pin 5 = VDD	3	-55°C	-	160	μA			

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NOTES: 1. All voltages referenced to device GND, 100% testing being 3. For accuracy, voltage is measured differentially to VDD. Limit implemented.

2. Go/No Go test with limits applied to inputs.

is 0.050V max.

## TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

			GROUP A		LIM	ITS	
PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
AC Coupled Signal Input Voltage Sensitivity (Peak to Peak)	VS	VDD = 5V, Input Frequency = 100kHz Sine Wave	9	+25°C	-	360	mV

NOTES:

1. Go/No Go test with limits applied to inputs.

					LIMITS		
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
(Source)				-55°C	-	-0.64	mA
Output Current	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
(Source)				-55°C	-	-2.0	mA
Output Current	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
(Source)				-55°C	-	-1.6	mA
Output Current	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
(Source)				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

## TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

		LIMITS						
DADAMETED	SYMBOL		CONDITIONS	NOTES		MIN	MAY	
FARAMETER	STWBOL		CONDITIONS	NOTES	TEWFERATORE	IVIIIN	IVIAA	UNITS
Quiescent Leakage Phase Comparator	BIAS LKG	VDD = 5 VIN =	Pin 14 Open Pin 5 = VDD	1, 2	+25°C/-55°C	-	0.2	mA
(Bias Amp Leakage)		GND or	Pin 14 = VSS or VDD Pin 5 = VDD	1, 2	+25°C/-55°C	-	20	μΑ
	VD VIN GN VD GN GN	VDD = 10 VIN =	Pin 14 Open Pin 5 = VDD	1, 2	+25°C/-55°C	-	1.0	mA
		VDD or GND	Pin 14 = VSS or VDD Pin 5 = VDD	1, 2	+25°C/-55°C	-	40	μΑ
		VDD = 15 VIN =	Pin 14 Open Pin 5 = VDD	1, 2	+25°C/-55°C	-	1.5	mA
		VDD or GND	Pin 14 = VSS or VDD Pin 5 = VDD	1, 2	+25°C/-55°C	-	80	μΑ
AC Coupled Signal In- put Voltage Sensitivity	VS	VDD = 10\ 100kHz Sir	/, Input Frequency = ne Wave	1, 2	+25°C	-	660	mV
(Peak to Peak)		VDD = 15V, Input Frequency = 100kHz Sine Wave		1, 2	+25°C	-	1800	mV

## TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

## TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

					LIM	IITS	
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH >	VOL <	V
		VDD = 3V, VIN = VDD or GND			VDD/2	VDD/2	
AC Coupled Signal Input Voltage Sensitivity	VS	VDD = 5V Input Frequency = 100kHz Sine Wave	1, 2, 3	+25°C	-	1.35 x +25 <sup>o</sup> C Limit	mV

NOTES: 1. All voltages referenced to device GND.

2. Go/No Go test with limits applied to inputs.

3. See Table 2 for +25°C limit.

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	$\pm$ 20% x Pre-Test Reading
Output Current (Source)	IOH5A	$\pm$ 20% x Pre-Test Reading

## TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25<sup>O</sup>C

	TABLE 6. AFFLICABLE SUBGROUPS								
CONFOR	MANCE GROUP	METHOD	GROUP A SUBGROUPS	READ AND RECORD					
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A					
Interim Test 1	(Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A					
Interim Test 2	(Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A					
PDA (Note	1)	100% 5004	1, 7, 9, Deltas						
Interim Test 3	3 (Post Burn-In) 100% 5004 1, 7, 9		IDD, IOL5, IOH5A						
PDA (Note	1)	100% 5004	1, 7, 9, Deltas						
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11						
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11						
Group B Subgroup B-5		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11					
Subgroup B-6		Sample 5005	1, 7, 9						
Group D	*	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3					

## TABLE 6. APPLICABLE SUBGROUPS

NOTE: 1.5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

## TABLE 7. TOTAL DOSE IRRADIATION

		TE	ST	READ ANI	DRECORD
CONFORMANCE GROUPS	METHOD	PRE-IRRAD POST-IRRAD		PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

## TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

					OSCILLATOR	
FUNCTION	OPEN	GROUND	VDD	$9V \pm -0.5V$	50kHz	25kHz
Static Burn-In 1 Note 1	1, 2, 4, 6, 7, 10, 11, 13, 15	3, 5, 8, 9, 14	12, 16			
Static Burn-In 2 Note 1	1, 2, 4, 6, 7, 10, 11, 13, 15	8	3, 5, 9, 12, 14, 16			
Dynamic Burn- In Note 1	1, 2, 4, 6, 7, 10, 11, 13, 15	8, 9	3, 5, 12, 16	2	14	-
Irradiation Note 2	1, 2, 4, 6, 7, 10, 11, 13, 15	8	3, 5, 9, 12, 14, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K  $\pm$  5%, VDD = 18V  $\pm$  0.5V

2. Each pin except VDD and GND will have a series resistor of 47K  $\pm$  5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V  $\pm$  0.5V

## **Design Information**

This information is a guide for approximating the values of external components for the CD4046BMS in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

 $5k\Omega \le R1, R2, RS \le 1M\Omega$ 

 $C1 \ge 100 pF$  at  $VDD \ge 5V$ 

C1  $\ge$  50pF at VDD  $\ge$  10V

CHARACTERISTICS	PHASE COMPARATOR USED	DESIGN INFORMATION
VCO Frequency	1	VCO Without Offset R2 = $\infty$ VCO With Offset
		<sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> MIN <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> MIN <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> MIN <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> MIN <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> O <sup>f</sup> MAX <sup>f</sup> O <sup>f</sup> O <sup></sup>
	2	Same as for Number 1
For Number Signal Input	1	VCO will adjust to center frequency, fo
	2	VCO will adjust to lowest operating frequency, fmin
Frequency Lock Range, 2fL	1, 2	2fL = full VCO frequency range
	1, 2	2fL = fmax - fmin
Frequency Capture Range, 2fC	1	IN R3 OUT $\tau I = R3C2 + C2$ IN R3 OUT $\tau I = R3C2 + C2$ IN R3 OUT $\tau I$ For 2 fC, see Ref. (2)
	2	fC = fL
Phase Angle Between Signal and Comparator	1	90° at center frequency (fo) approximating 0° and 180° at ends of lock range (2fL)
	2	Always 0 <sup>o</sup> in lock
Locks On Harmonic of Center Frequency	1	Yes
	2	No
Signal Input Noise Rejection	1	High
	2	Low

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965





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