Data Sheet August 2000 File Number 3554.2

Radiation Hardened Fast Sample and Hold

The HS-2420RH is a radiation hardened monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operation amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

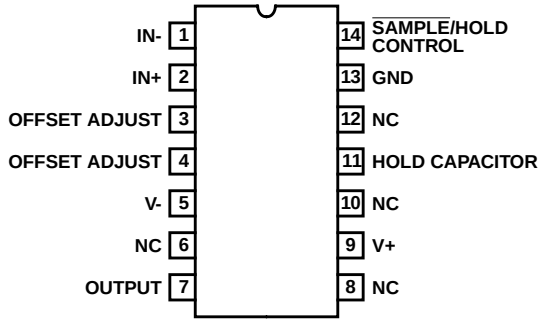
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95669. A “hot-link” is provided on our homepage for downloading.
http://www.intersil.com/spacedefense/space.asp

Pinout

14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE (CERDIP) MIL-STD-1835, GDIP1-T14
TOP VIEW



Features

- Electrically Screened to SMD # 5962-95669
- QML Qualified per MIL-PRF-38535 Requirements
- Maximum Acquisition Time
  - 10V Step to 0.1% 4µs
  - 10V Step to 0.01% 6µs
- Maximum Drift Current . . . . . 10nA (Maximum Over Temperature)
- TTL Compatible Control Input
- Power Supply Rejection . . . . . ≥80dB
- Total Dose . . . . . 100 krad(Si) (Max)
- No Latch-Up

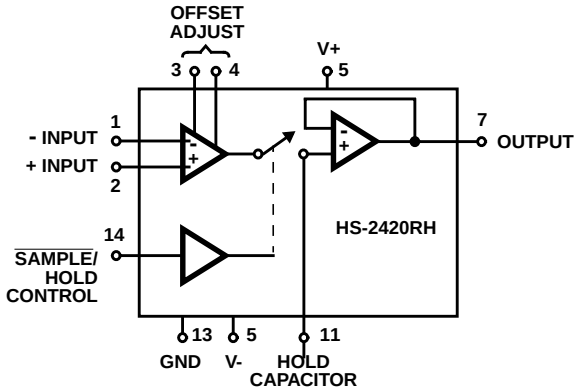
Applications

- Data Acquisition Systems
- D to A Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Op Amp

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962R9566901VCA	HS1-2420RH-Q	-55 to 125

Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

Test Circuits

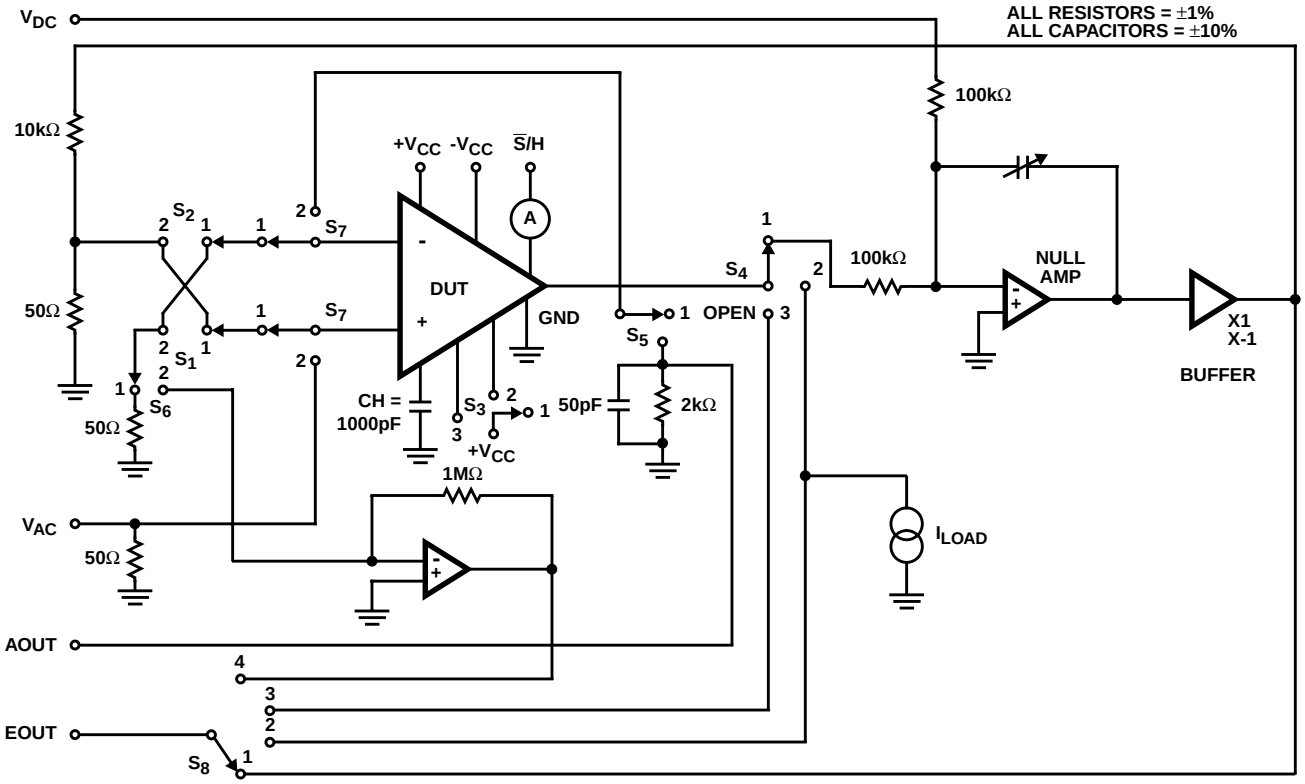
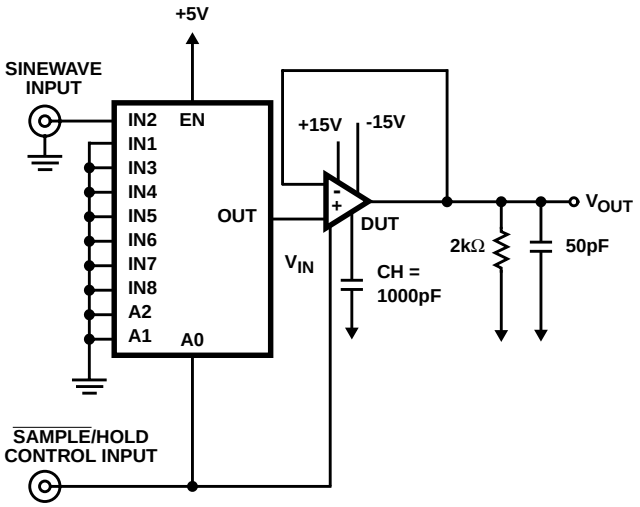


FIGURE 1. TEST FIXTURE SCHEMATIC (SWITCH POSITIONS S_1 - S_8 DETERMINE CONFIGURATION)

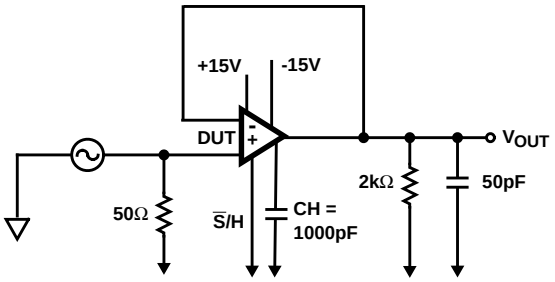


NOTE: Compute Hold Mode Feedthrough Attenuation from the Formula:

$$\text{FeedthroughAttenuation} = 20 \log \left(\frac{V_{OUT\ HOLD}}{V_{IN\ HOLD}} \right)$$

Where $V_{OUT\ HOLD}$ = Peak-Peak Value of Output Sinewave during the Hold Mode.

FIGURE 2. HOLD MODE FEEDTHROUGH ATTENUATION



NOTE: GBWP is the Frequency of V_{INPUT} at which:

$$20 \log \left(\frac{V_{OUT}}{V_{INPUT}} \right) = -3dB$$

FIGURE 3. GAIN BANDWIDTH PRODUCT

Test Circuits (Continued)

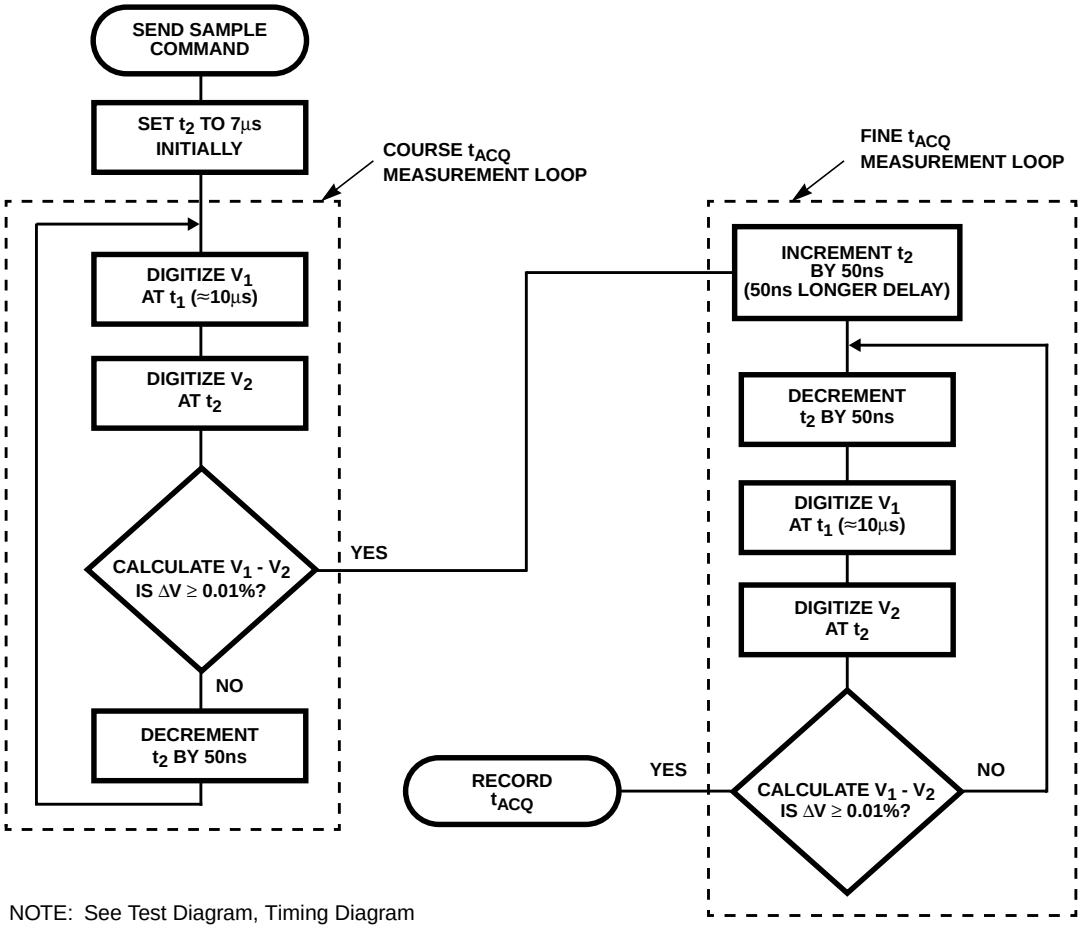


FIGURE 4. ACQUISITION TIME (t_{ACQ} TO 0.01% IS SHOWN, t_{ACQ} TO 0.1% IS DONE IN THE SAME MANNER)

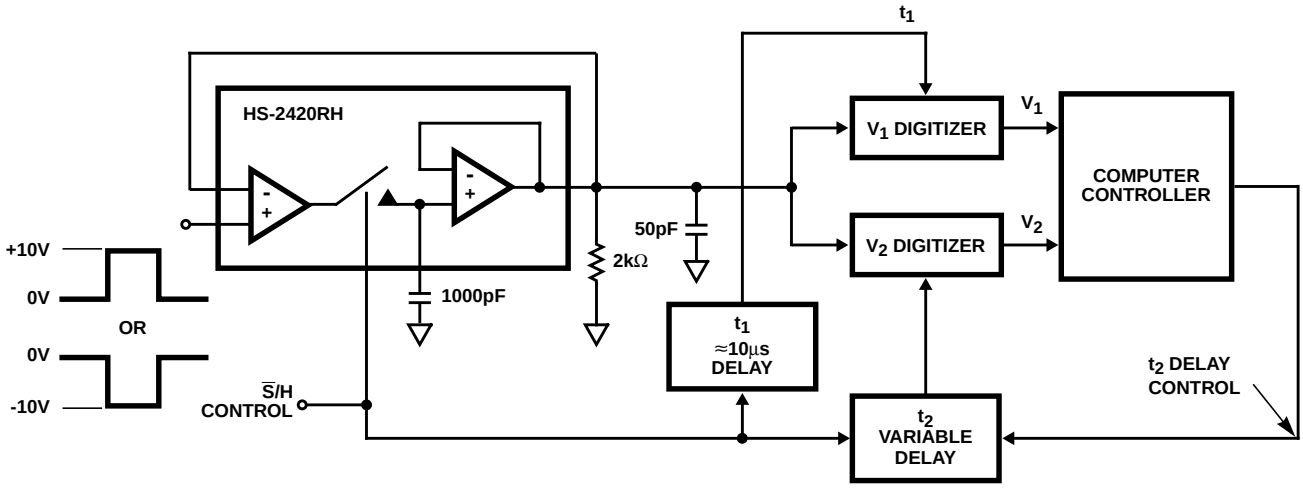


FIGURE 5.

Timing Waveforms

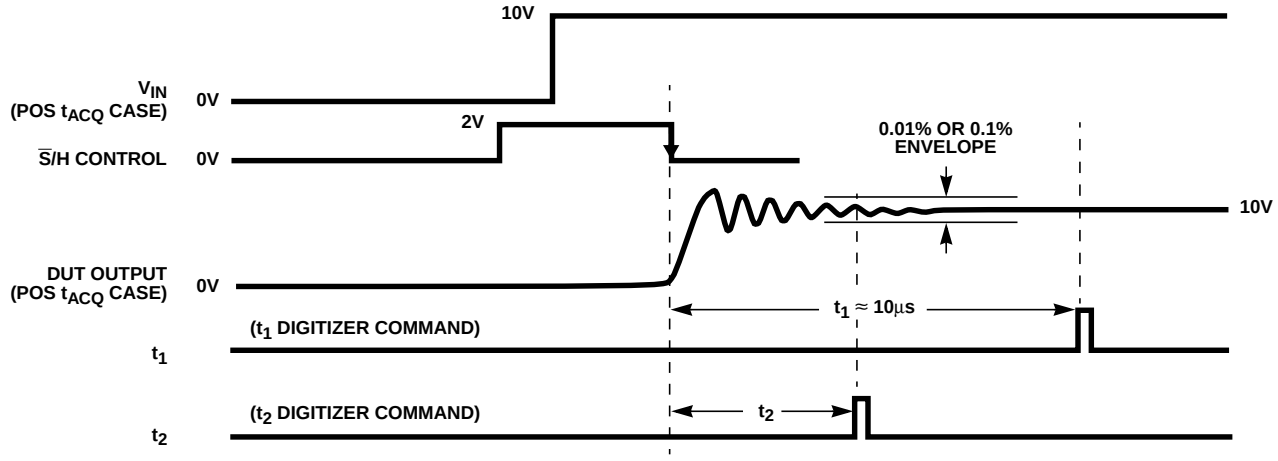


FIGURE 6. TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE t_{ACQ} CASE)

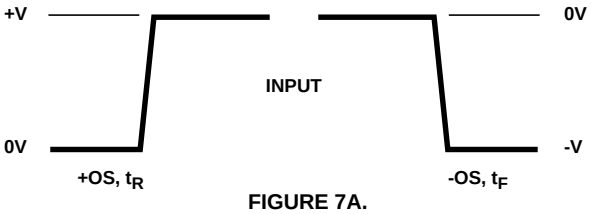


FIGURE 7A.

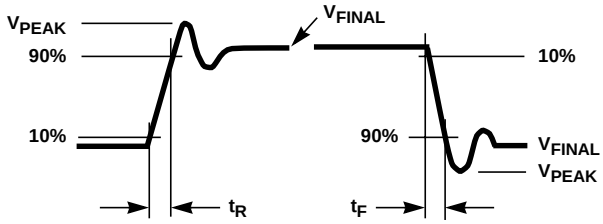


FIGURE 7B.

FIGURE 7. OVERSHOOT, RISE AND FALL TIME WAVEFORMS

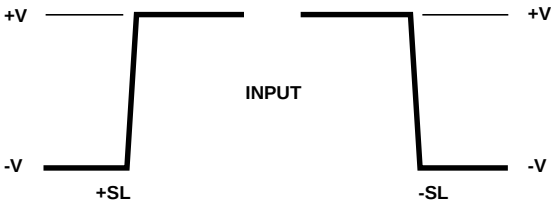


FIGURE 8A.

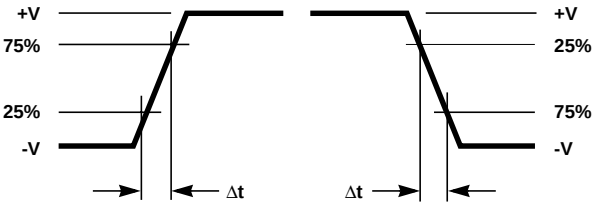


FIGURE 8B.

FIGURE 8. SLEW RATE WAVEFORMS

Typical Performance Curves $V_{SUPPLY} = \pm 15V_{DC}$, $T_A = 25^oC$, CH = 1000pF, Unless Otherwise Specified

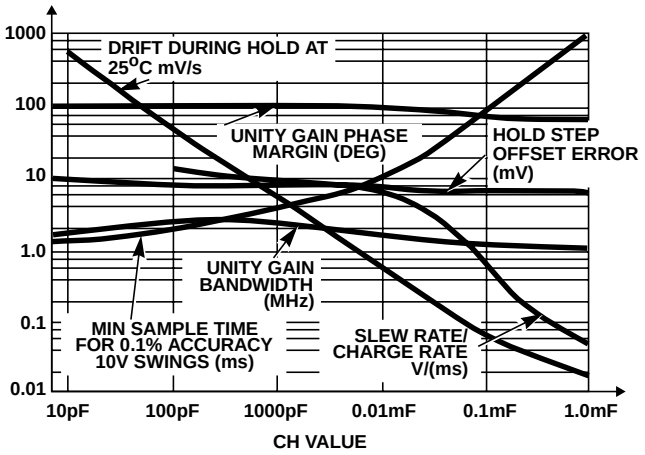


FIGURE 9. TYPICAL SAMPLE AND HOLD PERFORMANCE vs HOLDING CAPACITOR

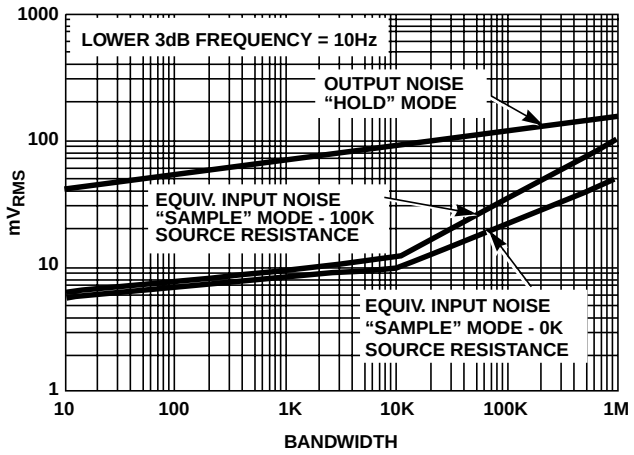


FIGURE 10. BROADBAND NOISE CHARACTERISTICS

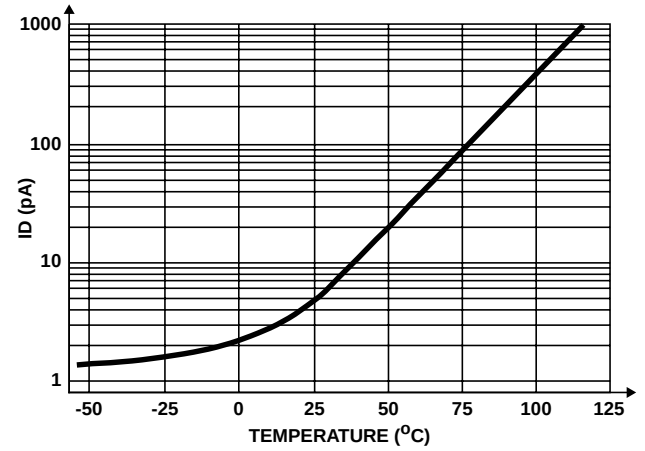


FIGURE 11. DRIFT CURRENT vs TEMPERATURE

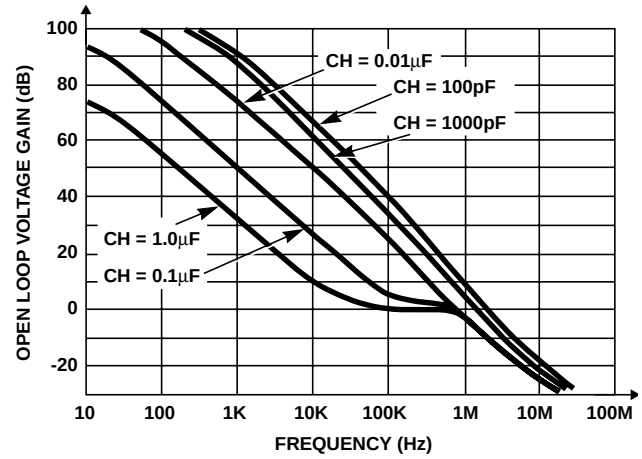


FIGURE 12. OPEN LOOP FREQUENCY RESPONSE

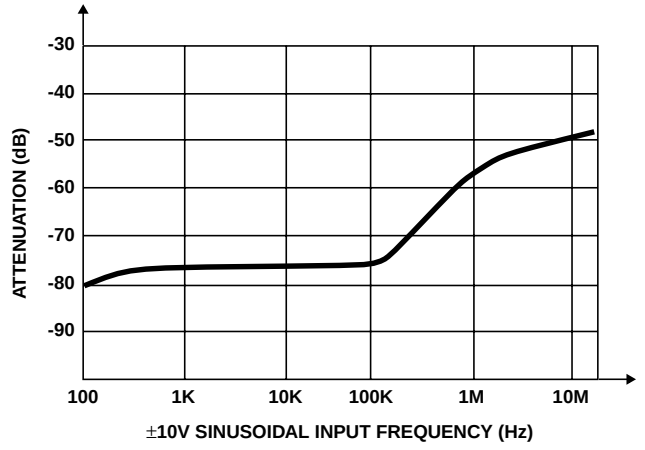


FIGURE 13. HOLD MODE FEEDTHROUGH ATTENUATION CH = 1000pF

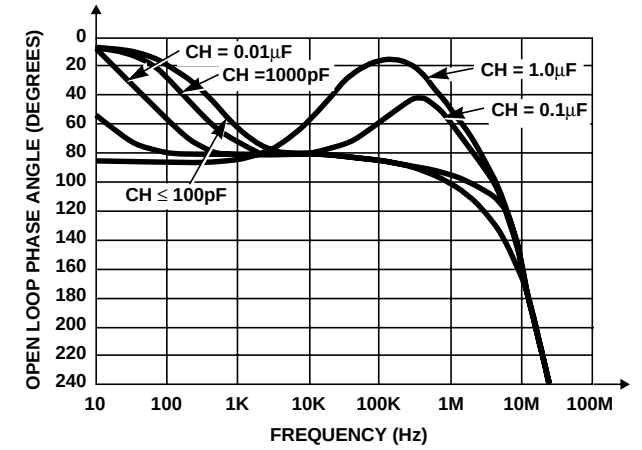
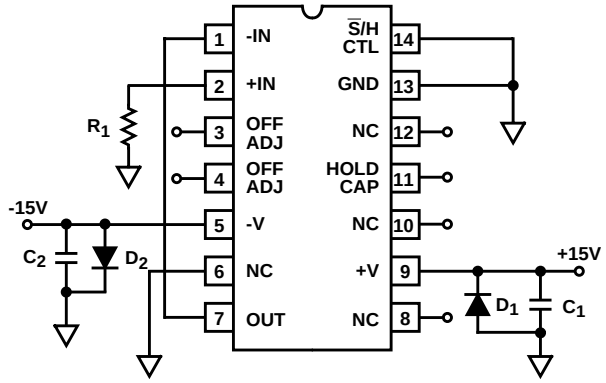


FIGURE 14. OPEN LOOP PHASE RESPONSE

Burn-In Circuit

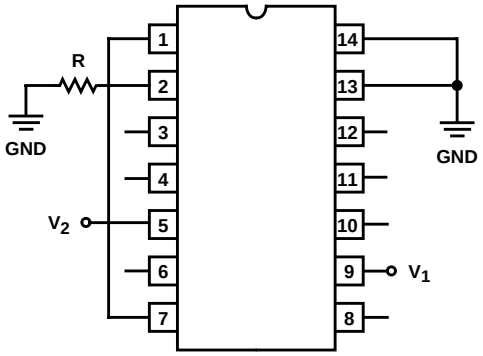
HS-2420RH CERDIP



NOTES:

R_1 = 100kΩ ±5% (per socket)
$C_1 = C_2$ = 0.1µF (one per row) or 0.01µF (one per socket)
$D_1 = D_2$ = 1N4002 or equivalent (per board)

Irradiation Circuit



NOTES:

V_1 = +15V
V_2 = -15V
R = 100kΩ

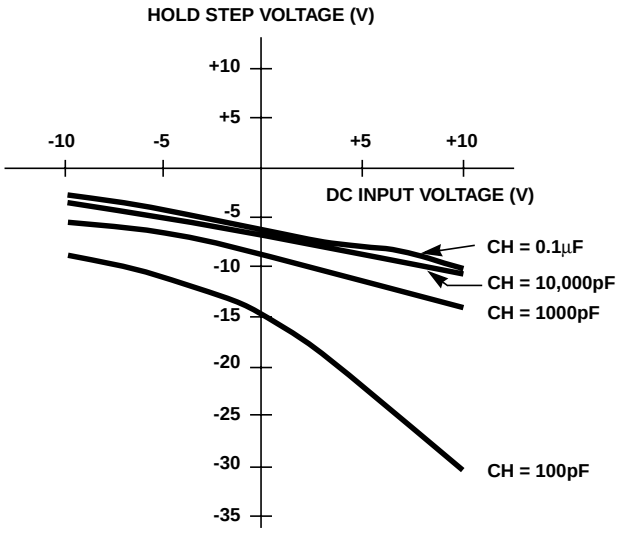


FIGURE 15. HOLD STEP vs INPUT VOLTAGE

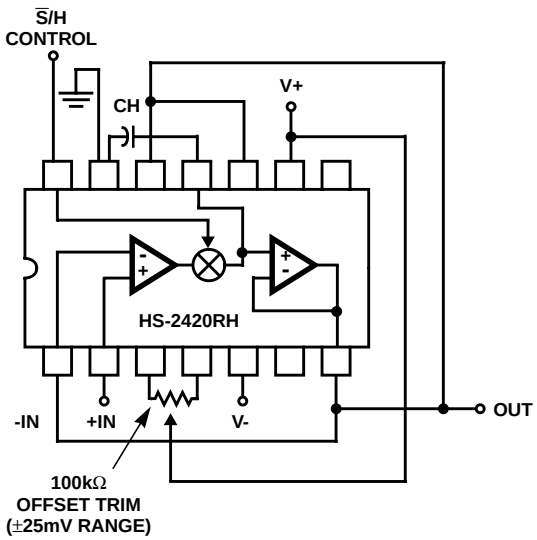


FIGURE 16. BASIC SAMPLE-AND-HOLD (TOP VIEW)

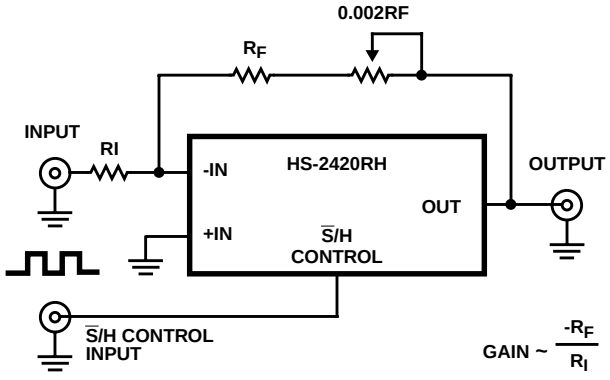


FIGURE 17. INVERTING CONFIGURATION

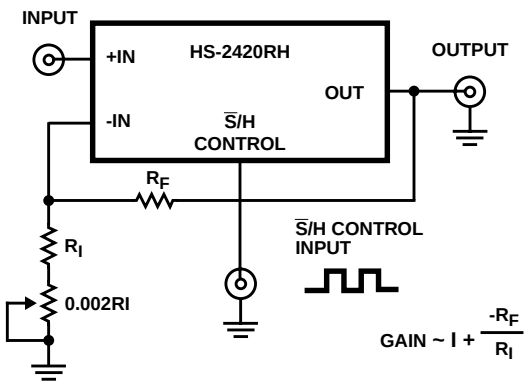


FIGURE 18. NONINVERTING CONFIGURATION

Offset and Gain Adjustment

Offset Adjustment

The offset voltage of the HS-2420RH may be adjusted using a 100kΩ trim pot, as shown in Figure 15. The recommended adjustment procedure is:

1. Apply 0V to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.
2. Adjust the trim pot for 0V output in the hold mode.

Gain Adjustment

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (CH = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage (V-10 NOMINAL). Adjust the trim pot for an output hold voltage of:

$$\frac{(\text{V-10 NOMINAL}) + (-10\text{V})}{2}$$

Die Characteristics

DIE DIMENSIONS:

97 mils x 61 mils x 19 mils

METALLIZATION:

Type: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Silox
Thickness: 14kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:

$2.0 \times 10^5 A/cm^2$

TRANSISTOR COUNT:

78

PROCESS:

Bipolar-Di

Metallization Mask Layout

HS-2420RH