

### Features

- CMOS/SOS Low Power
- R2R Output, Segmented for Low "Glitch"
- CMOS/TTL Compatible Inputs
- Fast Settling: (Typ) to  $1/2$  LSB ..... 20ns
- Feedthrough Latch for Clocked or Unclocked Use
- Accuracy (Typ) .....  $\pm 0.5$  LSB
- Data Complement Control
- High Update Rate (Typ) ..... 50MHz
- Unipolar or Bipolar Operation

### Applications

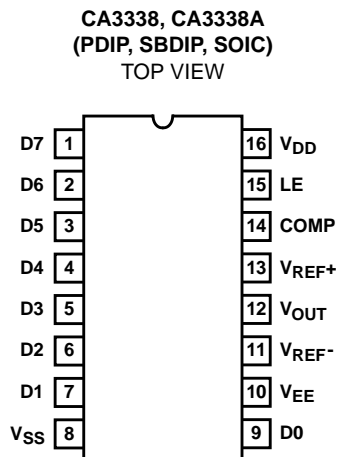
- TV/Video Display
- High Speed Oscilloscope Display
- Digital Waveform Generator
- Direct Digital Synthesis

### Description

The CA3338 family are CMOS/SOS high speed R2R voltage output digital-to-analog converters. They can operate from a single +5V supply, at video speeds, and can produce "rail-to-rail" output swings. Internal level shifters and a pin for an optional second supply provide for an output range below digital ground. The data complement control allows the inversion of input data while the latch enable control provides either feedthrough or latched operation. Both ends of the R2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, "glitch" energy has been kept very low by segmenting and thermometer encoding of the upper 3 bits.

The CA3338 is manufactured on a sapphire substrate to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

### Pinout



### Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3338E	$\pm 1.0$ LSB	-40 to 85	16 Ld PDIP	E16.3
CA3338AE	$\pm 0.75$ LSB	-40 to 85	16 Ld PDIP	E16.3
CA3338D	$\pm 1.0$ LSB	-55 to 125	16 Ld SBDIP	D16.3
CA3338AD	$\pm 0.75$ LSB	-55 to 125	16 Ld SBDIP	D16.3
CA3338M	$\pm 1.0$ LSB	-40 to 85	16 Ld SOIC	M16.3
CA3338AM	$\pm 0.75$ LSB	-40 to 85	16 Ld SOIC	M16.3

The schematic diagram illustrates the internal architecture of the 7-bit digital thermometer circuit. It consists of the following main blocks and components:

- Input Stage:** The 7-bit digital input (D0-D6) is connected to a series of 7 AND gates. The inputs to these AND gates are also connected to a 7-bit digital input (D0-D6) and a 7-bit digital output (D0-D6) through a series of inverters.
- LEVEL SHIFTERS:** A block of 7 level shifters that convert the input signals to the appropriate logic levels for the subsequent stages.
- 3-BIT TO 7-LINE THERMOMETER ENCODER:** A block that takes a 3-bit digital input and produces a 7-bit thermometer code output.
- FEEDTHROUGH LATCHES:** A block of 7 feedthrough latches that store the thermometer code output from the encoder.
- Output Stage:** The output of the feedthrough latches is connected to a series of 7 comparators. Each comparator compares the thermometer code output with a reference voltage (VREF+ or VREF-). The output of each comparator is connected to a resistor network (8R, 4R, 2R) and a 7-bit digital output (D0-D6).
- Power and Ground:** The circuit is powered by VDD (pin 16) and VSS (pin 8). The output is connected to VREF+ (pin 13) and VREF- (pin 11). The ground connection is VEE (pin 10).

# CA3338, CA3338A

## Absolute Maximum Ratings

DC Supply-Voltage Range . . . . . -0.5V to +8V  
 ( $V_{DD} - V_{SS}$  or  $V_{DD} - V_{EE}$ , Whichever is Greater)  
 Input Voltage Range  
 Digital Inputs (LE, COMP D0 - D7) . . . . .  $V_{SS} - 0.5V$  to  $V_{DD} + 0.5V$   
 Analog Pins ( $V_{REF+}$ ,  $V_{REF-}$ ,  $V_{OUT}$ ) . . . . .  $V_{DD} - 8V$  to  $V_{DD} + 0.5V$   
 DC Input Current  
 Digital Inputs (LE, COMP, D0 - D7) . . . . .  $\pm 20mA$   
 Recommended Supply Voltage Range . . . . . 4.5V to 7.5V

## Operating Conditions

Temperature Range ( $T_A$ )  
 Ceramic Package, D suffix . . . . . -55°C to 125°C  
 Plastic Package, E suffix, M suffix . . . . . -40°C to 85°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  $\theta_{JC}$  (°C/W)  
 SBDIP Package . . . . . 75 24  
 PDIP Package . . . . . 100 N/A  
 SOIC Package . . . . . 100 N/A  
 Maximum Junction Temperature  
 Ceramic Package . . . . . 175°C  
 Plastic Packages . . . . . 150°C  
 Maximum Storage Temperature Range,  $T_{STG}$  . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C  
 (SOIC - Lead Tips Only)

**Electrical Specifications**  $T_A = 25^\circ C$ ,  $V_{DD} = 5V$ ,  $V_{REF+} = 4.608V$ ,  $V_{SS} = V_{EE} = V_{REF-} = GND$ , LE Clocked at 20MHz,  $R_L \geq 1 M\Omega$ , Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>ACCURACY</b>					
Resolution		8	-	-	Bits
Integral Linearity Error	See Figure 4				
CA3338		-	-	$\pm 1$	LSB
CA3338A		-	-	$\pm 0.75$	LSB
Differential Linearity Error	See Figure 4				
CA3338		-	-	$\pm 0.75$	LSB
CA3338A		-	-	$\pm 0.5$	LSB
Gain Error	Input Code = FF <sub>HEX</sub> , See Figure 3				
CA3338		-	-	$\pm 0.75$	LSB
CA3338A		-	-	$\pm 0.5$	LSB
Offset Error	Input Code = 00 <sub>HEX</sub> ; See Figure 3	-	-	$\pm 0.25$	LSB
<b>DIGITAL INPUT TIMING</b>					
Update Rate	To Maintain $1/2$ LSB Settling	DC	50	-	MHz
Update Rate	$V_{REF-} = V_{EE} = -2.5V$ , $V_{REF+} = +2.5V$	DC	20	-	MHz
Set Up Time $t_{SU1}$	For Low Glitch	-	-2	-	ns
Set Up Time $t_{SU2}$	For Data Store	-	8	-	ns
Hold Time $t_H$	For Data Store	-	5	-	ns
Latch Pulse Width $t_W$	For Data Store	-	5	-	ns
Latch Pulse Width $t_W$	$V_{REF-} = V_{EE} = -2.5V$ , $V_{REF+} = +2.5V$	-	25	-	ns
<b>OUTPUT PARAMETERS</b> $R_L$ Adjusted for 1V <sub>P-P</sub> Output					
Output Delay $t_{D1}$	From LE Edge	-	25	-	ns
Output Delay $t_{D2}$	From Data Changing	-	22	-	ns
Rise Time $t_r$	10% to 90% of Output	-	4	-	ns
Settling Time $t_s$	10% to Settling to $1/2$ LSB	-	20	-	ns
Output Impedance	$V_{REF+} = 6V$ , $V_{DD} = 6V$	120	160	200	$\Omega$
Glitch Area		-	150	-	pV/s
Glitch Area	$V_{REF-} = V_{EE} = -2.5V$ , $V_{REF+} = +2.5V$	-	250	-	pV/s

## CA3338, CA3338A

**Electrical Specifications**  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{REF+} = 4.608\text{V}$ ,  $V_{SS} = V_{EE} = V_{REF-} = \text{GND}$ , LE Clocked at 20MHz,  $R_L \geq 1\text{ M}\Omega$ , Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>REFERENCE VOLTAGE</b>					
$V_{REF+}$ Range	(+) Full Scale, Note 1	$V_{REF-} + 3$	-	$V_{DD}$	V
$V_{REF-}$ Range	(-) Full Scale, Note 1	$V_{EE}$	-	$V_{REF+} - 3$	V
$V_{REF+}$ Input Current	$V_{REF+} = 6\text{V}$ , $V_{DD} = 6\text{V}$	-	40	50	mA
<b>SUPPLY VOLTAGE</b>					
Static $I_{DD}$ or $I_{EE}$	LE = Low, D0 - D7 = High	-	100	220	$\mu\text{A}$
	LE = Low, D0 - D7 = Low	-	-	100	$\mu\text{A}$
Dynamic $I_{DD}$ or $I_{EE}$	$V_{OUT} = 10\text{MHz}$ , 0V to 5V Square Wave	-	20	-	mA
Dynamic $I_{DD}$ or $I_{EE}$	$V_{OUT} = 10\text{MHz}$ , $\pm 2.5\text{V}$ Square Wave	-	25	-	mA
$V_{DD}$ Rejection	50kHz Sine Wave Applied	-	3	-	mV/V
$V_{EE}$ Rejection	50kHz Sine Wave Applied	-	1	-	mV/V
<b>DIGITAL INPUTS</b> D0 - D7, LE, COMP					
High Level Input Voltage	Note 1	2	-	-	V
Low Level Input Voltage	Note 1	-	-	0.8	V
Leakage Current		-	$\pm 1$	$\pm 5$	$\mu\text{A}$
Capacitance		-	5	-	pF
<b>TEMPERATURE COEFFICIENTS</b>					
Output Impedance		-	200	-	ppm/ $^\circ\text{C}$

NOTE:

- Parameter not tested. but guaranteed by design or characterization.

### Pin Descriptions

PIN	NAME	DESCRIPTION
1	D7	Most Significant Bit  Input Data Bits (High = True)
2	D6	
3	D5	
4	D4	
5	D3	
6	D2	
7	D1	
8	$V_{SS}$	Digital Ground
9	D0	Least Significant Bit. Input Data Bit
10	$V_{EE}$	Analog Ground
11	$V_{REF-}$	Reference Voltage Negative Input
12	$V_{OUT}$	Analog Output
13	$V_{REF+}$	Reference Voltage Positive Input
14	COMP	Data Complement Control input. Active High
15	LE	Latch Enable Input. Active Low
16	$V_{DD}$	Digital Power Supply, +5V

### Digital Signal Path

The digital inputs (LE, COMP, and D0 - D7) are of TTL compatible HCT High Speed CMOS design: the loading is essentially capacitive and the logic threshold is typically 1.5V.

The 8 data bits, D0 (weighted  $2^0$ ) through D7 (weighted  $2^7$ ), are applied to Exclusive OR gates (see Functional Diagram). The COMP (data complement) control provides the second input to the gates: if COMP is high, the data bits will be inverted as they pass through.

The input data and the LE (latch enable) signals are next applied to a level shifter. The inputs, operating between the levels of  $V_{DD}$  and  $V_{SS}$ , are shifted to operate between  $V_{DD}$  and  $V_{EE}$ .  $V_{EE}$  optionally at ground or at a negative voltage, will be discussed under bipolar operation. All further logic elements except the output drivers operate from the  $V_{DD}$  and  $V_{EE}$  supplies.

The upper 3 bits of data, D5 through D7, are input to a 3-to-7 line bar graph encoder. The encoder outputs and D0 through D4 are applied to a feedthrough latch, which is controlled by LE (latch enable).

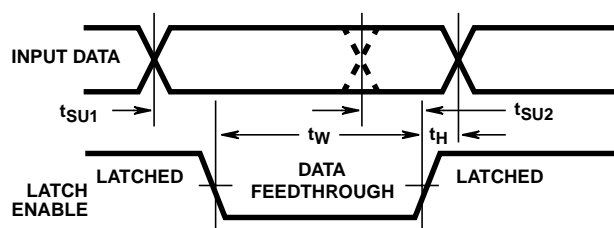


FIGURE 1. DATA TO LATCH ENABLE TIMING

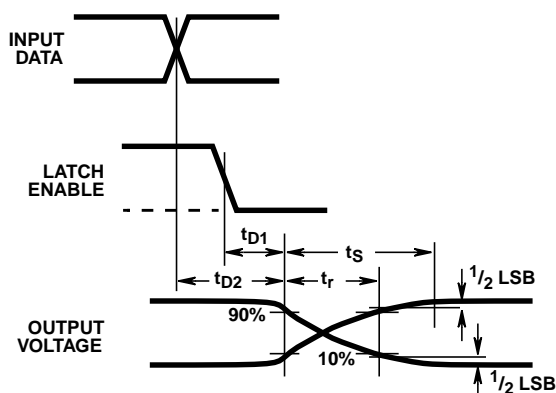


FIGURE 2. DATA AND LATCH ENABLE TO OUTPUT TIMING

### Latch Operation

Data is fed from input to output while LE is low: LE should be tied low for non-clocked operation.

Non-clocked operation or changing data while LE is low is not recommended for applications requiring low output "glitch" energy: there is no guarantee of the simultaneous changing of input data or the equal propagation delay of all bits through the converter. Several parameters are given if the converter is to be used in either of these modes:  $t_{D2}$  gives the delay from the input changing to the output changing (10%), while  $t_{SU2}$  and  $t_H$  give the set up and hold times (referred to LE rising edge) needed to latch data. See Figures 1 and 2.

Clocked operation is needed for low "glitch" energy use. Data must meet the given  $t_{SU1}$  set up time to the LE falling edge, and the  $t_H$  hold time from the LE rising edge. The delay to the output changing,  $t_{D1}$ , is now referred to the LE falling edge.

There is no need for a square wave LE clock; LE must only meet the minimum  $t_W$  pulse width for successful latch operation. Generally, output timing (desired accuracy of settling) sets the upper limit of usable clock frequency.

### Output Structure

The latches feed data to a row of high current CMOS drivers, which in turn feed a modified R2R ladder network.

The "N" channel (pull down) transistor of each driver plus the bottom "2R" resistor are returned to  $V_{REF-}$  this is the (-) full-scale reference. The "P" channel (pull up) transistor of each driver is returned to  $V_{REF+}$ , the (+) full-scale reference.

In unipolar operation,  $V_{REF-}$  would typically be returned to analog ground, but may be raised above ground (see specifications). There is substantial code dependent current that flows from  $V_{REF+}$  to  $V_{REF-}$  (see  $V_{REF+}$  input current in specifications), so  $V_{REF-}$  should have a low impedance path to ground.

In bipolar operation,  $V_{REF-}$  would be returned to a negative voltage (the maximum voltage rating to  $V_{DD}$  must be observed).  $V_{EE}$ , which supplies the gate potential for the output drivers, must be returned to a point at least as negative as  $V_{REF-}$ . Note that the maximum clocking speed decreases when the bipolar mode is used.

### Static Characteristics

The ideal 8-bit D/A would have an output equal to  $V_{REF-}$  with an input code of 00<sub>HEX</sub> (zero scale output), and an output equal to 255/256 of  $V_{REF+}$  (referred to  $V_{REF-}$ ) with an input code of FF<sub>HEX</sub> (full scale output). The difference between the ideal and actual values of these two parameters are the OFF-SET and GAIN errors, respectively; see Figure 3.

If the code into an 8-bit D/A is changed by 1 count, the output should change by 1/255 (full scale output - zero scale output). A deviation from this step size is a differential linearity error, see Figure 4. Note that the error is expressed in fractions of the ideal step size (usually called an LSB). Also note that if the (-) differential linearity error is less (in absolute numbers) than 1 LSB, the device is monotonic. (The output will always increase for increasing code or decrease for decreasing code).

If the code into an 8-bit D/A is at any value, say "N", the output voltage should be N/255 of the full scale output (referred to the zero scale output). Any deviation from that output is an integral linearity error, usually expressed in LSBs. See Figure 4.

Note that OFFSET and GAIN errors do not affect integral linearity, as the linearity is referenced to actual zero and full scale outputs, not ideal. Absolute accuracy would have to also take these errors into account.

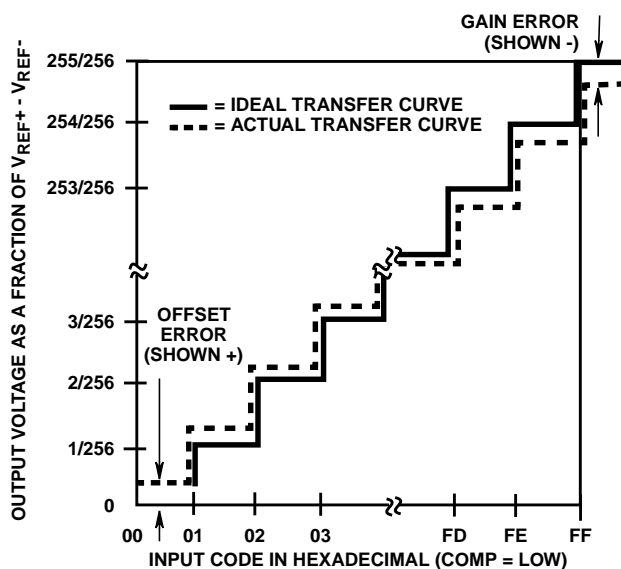


FIGURE 3. D/A OFFSET AND GAIN ERROR

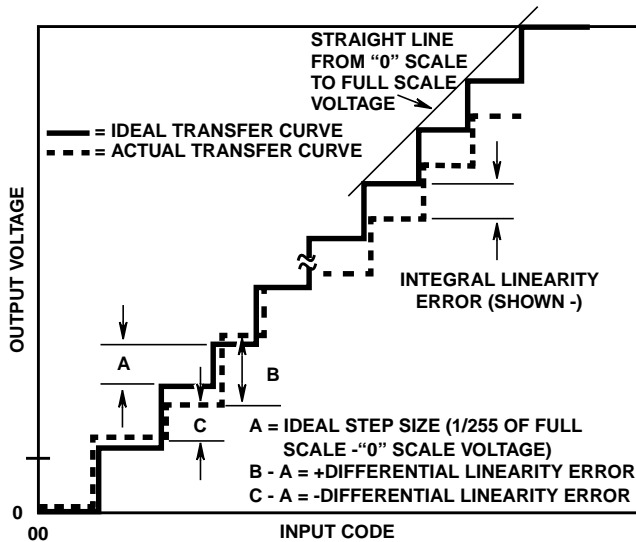


FIGURE 4. D/A INTEGRAL AND DIFFERENTIAL LINEARITY ERROR

### Dynamic Characteristics

Keeping the full-scale range ( $V_{REF+} - V_{REF-}$ ) as high as possible gives the best linearity and lowest "glitch" energy (referred to 1V). This provides the best "P" and "N" channel gate drives (hence saturation resistance) and propagation

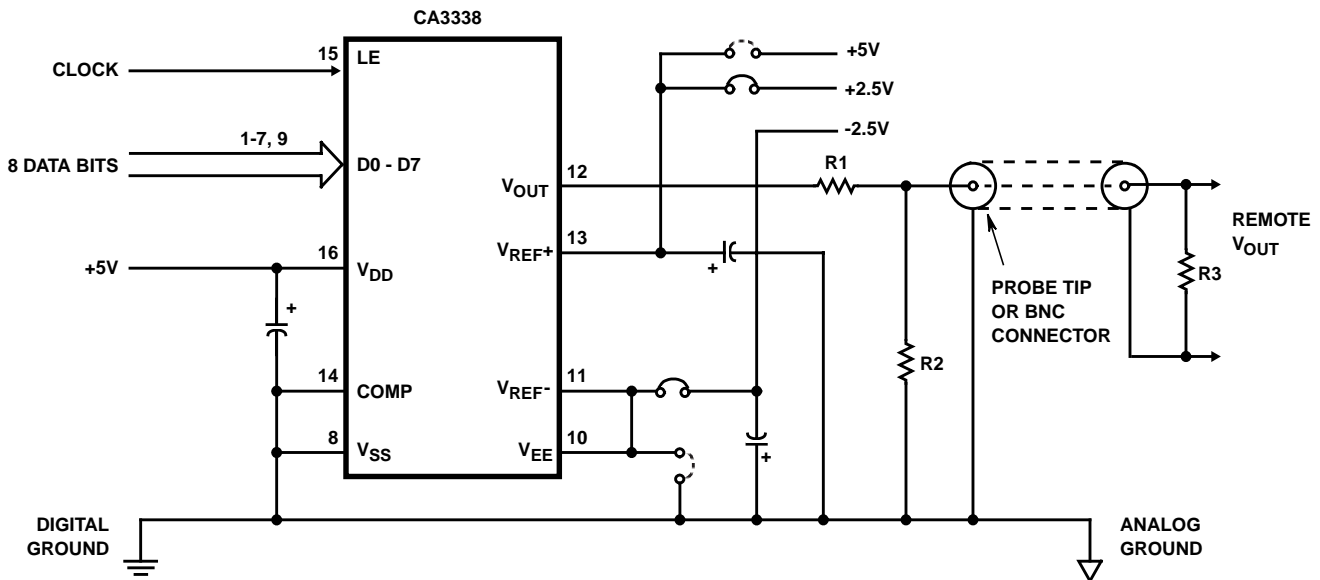
delays. The  $V_{REF+}$  (and  $V_{REF-}$  if bipolar) terminal should be well bypassed as near the chip as possible.

"Glitch" energy is defined as a spurious voltage that occurs as the output is changed from one voltage to another. In a binary input converter, it is usually highest at the most significant bit transition ( $7F_{HEX}$  to  $80_{HEX}$  for an 8 bit device), and can be measured by displaying the output as the input code alternates around that point. The "glitch" energy is the area between the actual output display and an ideal one LSB step voltage (subtracting negative area from positive), at either the positive or negative-going step. It is usually expressed in pV/s.

The CA3338 uses a modified R2R ladder, where the 3 most significant bits drive a bar graph decoder and 7 equally weighted resistors. This makes the "glitch" energy at each  $1/8$  scale transition ( $1F_{HEX}$  to  $20_{HEX}$ ,  $3F_{HEX}$  to  $40_{HEX}$ , etc.) essentially equal, and far less than the MSB transition would otherwise display.

For the purpose of comparison to other converters, the output should be resistively divided to 1V full scale. Figure 5 shows a typical hook-up for checking "glitch" energy or settling time.

The settling time of the A/D is mainly a function of the output resistance (approximately  $160\Omega$  in parallel with the load resistance) and the load plus internal chip capacitance. Both "glitch" energy and settling time measurements require very good circuit and probe grounding: a probe tip connector such as Tektronix part number 131-0258-00 is recommended.



FUNCTION	CONNECTOR	R1	R2	R3	V <sub>OUT</sub> (P-P)
Oscilloscope Display	Probe Tip	82Ω	62Ω	N/C	1V
Match 93Ω Cable	BNC	75	160	93	1V
Match 75Ω Cable	BNC	18	130	75	1V
Match 50Ω Cable	BNC	Short	75	50	0.79V

#### NOTES:

- $V_{OUT(P-P)}$  is approximate, and will vary as  $R_{OUT}$  of D/A varies.
- All drawn capacitors are 0.1μF multilayer ceramic/4.7μF tantalum.
- Dashed connections are for unipolar operation. Solid connection are for bipolar operation.

FIGURE 5. CA3338 DYNAMIC TEST CIRCUIT

## CA3338, CA3338A

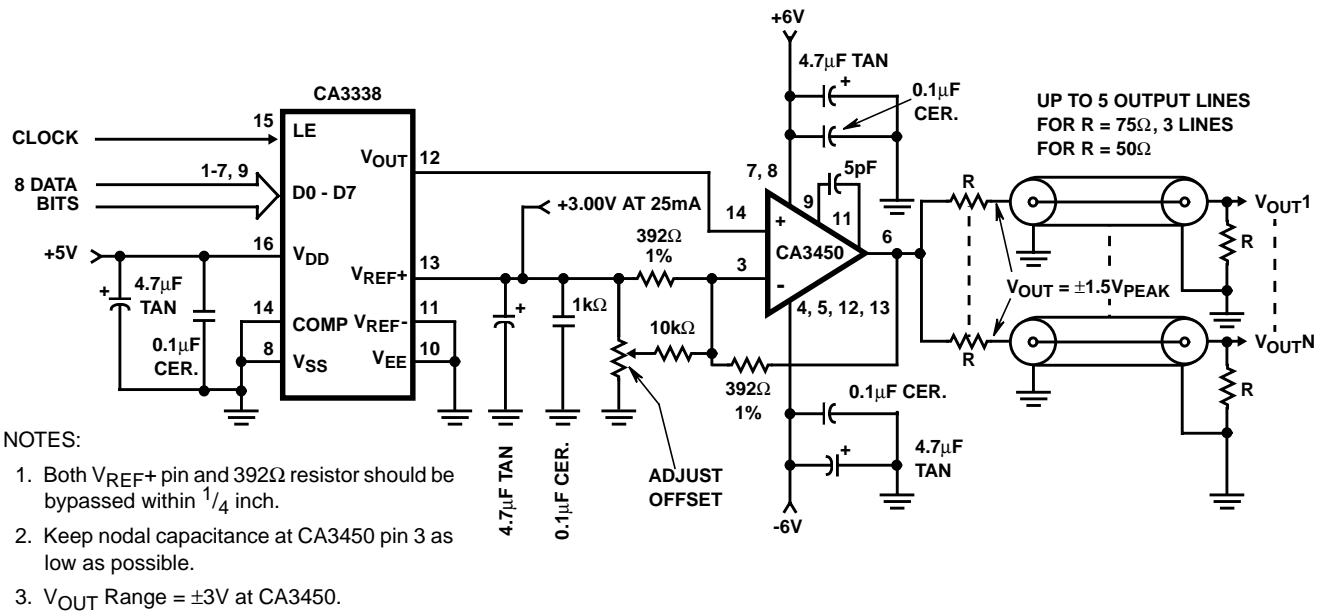


FIGURE 6. CA3338 AND CA3450 FOR DRIVING MULTIPLE COAXIAL LINES

TABLE 1. OUTPUT VOLTAGE vs INPUT CODE AND  $V_{REF}$

$V_{REF+}$ $V_{REF-}$ STEP SIZE	5.12V 0 0.0200V	5.00V 0 0.0195V	4.608V 0 0.0180V	2.56V -2.56V 0.0200V	2.50V -2.50V 0.0195V
Input Code					
11111112 = FF <sub>HEX</sub>	5.1000V	4.9805V	4.5900V	2.5400V	2.4805V
111111102 = FE <sub>HEX</sub>	5.0800	4.9610	4.5720	2.5200	2.4610
•					
•					
•					
10000001 <sub>2</sub> = 81 <sub>HEX</sub>	2.5800	2.5195	2.3220	0.0200	0.0195
10000000 <sub>2</sub> = 80 <sub>HEX</sub>	2.5600	2.5000	2.3040	0.0000	0.0000
01111111 <sub>2</sub> = 7F <sub>HEX</sub>	2.5400	2.4805	2.2860	-0.0200	-0.0195
•					
•					
•					
00000001 <sub>2</sub> = 01 <sub>HEX</sub>	0.0200	0.0195	0.0180	-2.5400	-2.4805
00000000 <sub>2</sub> = 00 <sub>HEX</sub>	0.0000	0.0000	0.0000	-2.5600	-2.5000

### Applications

The output of the CA3338 can be resistively divided to match a doubly terminated  $50\Omega$  or  $75\Omega$  line, although peak-to-peak swings of less than 1V may result. The output magnitude will also vary with the converter's output impedance. Figure 5 shows such an application. Note that because of the HCT input structure, the CA3338 could be operated up to  $+7.5V V_{DD}$  and  $V_{REF+}$  supplies and still accept 0V to 5V CMOS input voltages.

If larger voltage swings or better accuracy is desired, a high speed output buffer, such as the HA-5033, HA-2542, or CA3450, can be employed. Figure 6 shows a typical application, with the output capable of driving  $\pm 2V$  into multiple  $50\Omega$  terminated lines.

### Operating and Handling Considerations

#### HANDLING

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

#### OPERATING

##### Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the absolute maximum ratings to be exceeded.

##### Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than  $V_{DD}$  nor less than  $V_{SS}$ . Input currents must not exceed 20mA even when the power supply is off.

##### Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either  $V_{CC}$  or GND, whichever is appropriate.