REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R226-97.	97-02-28	Monica L. Poelking
B	Changes in accordance with NOR 5962-R397-97.	97-07-29	Raymond Monnin
C	Incorporate revisions A and B. Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – LTG	03-11-19	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Monica L. Poelking

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
95-12-13

MICROCIRCUIT, DIGITAL, RADIATION HARDENED CMOS, 8-STAGE STATIC SHIFT REGISTER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	**A**	**67268**	**5962-96623**

SHEET 1 OF 24

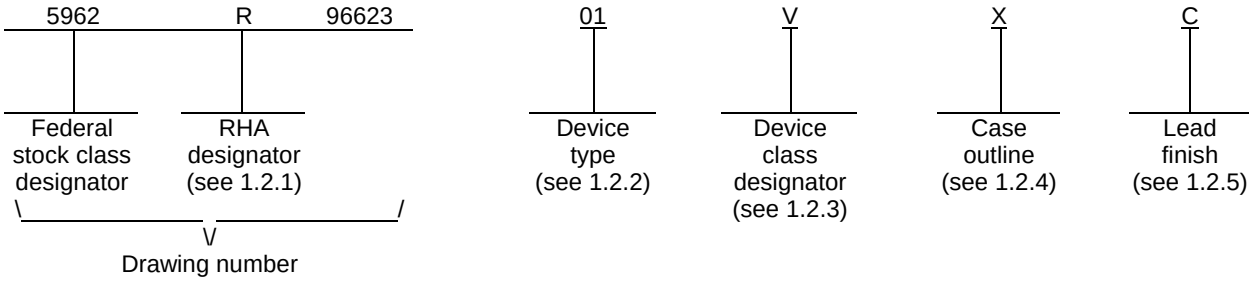
DSCC FORM 2233
APR 97

5962-E051-04

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4014B	Radiation hardened CMOS, synchronous parallel or serial input/serial output 8-stage static shift register
02	4021B	Radiation hardened CMOS, asynchronous parallel input or synchronous serial input/ serial output 8-stage static shift register
03	4014BN	Radiation hardened CMOS, synchronous parallel or serial input/serial output 8-stage static shift register with neutron irradiated die
04	4021BN	Radiation hardened CMOS, asynchronous parallel input or synchronous serial input/ serial output 8-stage static shift register with neutron irradiated die

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16	16	Dual-in-line package
X	CDFP4-F16	16	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.5 V dc to +20 V dc
Input voltage range	-0.5 V dc to V_{DD} + 0.5 V dc
DC input current, any one input	±10 mA
Device dissipation per output transistor	100 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case E	24°C/W
Case X	29°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	73°C/W
Case X	114°C/W
Junction temperature (T_J)	+175°C
Maximum power dissipation at T_A = +125°C (P_D): 4/	
Case E	0.68 W
Case X	0.44 W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	3.0 V dc to +18 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage (V_{IN})	0 V to V_{DD}
Output voltage (V_{OUT})	0 V to V_{DD}
Radiation features:	
Total dose	1 x 10^5 Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold, no upsets or latchup (see 4.4.4.5)	> 75 MeV/(cm^2/mg) 5/
Dose rate upset (20 ns pulse)	> 5 x 10^8 Rads(Si)/s 5/
Dose rate latch-up	> 2 x 10^8 Rads(Si)/s 5/
Dose rate survivability	> 5 x 10^{11} Rads(Si)/s 5/
Neutron irradiated	> 1 x 10^{14} neutrons/cm^2 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise noted.
4/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on θ_{JA}) at the following rate:

Case E	13.7 mW/°C
Case X	8.8 mW/°C

5/ Guaranteed by design or process but not tested.
6/ Device types 03 and 04 only.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified on figure 3.

3.2.5 Radiation test connections. The radiation test connections shall be as specified in table III herein.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Supply current	I_{DD}	V_{DD} = 5 V V_{IN} = 0.0 V or V_{DD}	All	1, 3 1/		5.0	µA
				2 1/		150	
		V_{DD} = 10 V V_{IN} = 0.0 V or V_{DD}	All	1, 3 1/		10	
				2 1/		300	
		V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	All	1, 3 1/		10	
				2 1/		600	
		V_{DD} = 20 V, V_{IN} = 0.0 V or V_{DD}	All	1		10	
				2		1000	
		M, D, P, L, R 2/	All	1		25	
		V_{DD} = 18 V, V_{IN} = 0.0 V or V_{DD}	All	3		10	
Low level output current (sink)	I_{OL}	V_{DD} = 5 V V_O = 0.4 V V_{IN} = 0.0 V or V_{DD}	All	1	0.53		mA
				2 1/	0.36		
				3 1/	0.64		
		V_{DD} = 10 V V_O = 0.5 V V_{IN} = 0.0 V or V_{DD}	All	1	1.4		
				2 1/	0.9		
				3 1/	1.6		
		V_{DD} = 15 V V_O = 1.5 V V_{IN} = 0.0 V or V_{DD}	All	1	3.5		
				2 1/	2.4		
				3 1/	4.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
High level output current (source)	I_{OH}	V_{DD} = 5 V V_O = 4.6 V V_{IN} = 0.0 V or V_{DD}	All	1		-0.53	mA
				2 1/		-0.36	
				3 1/		-0.64	
		V_{DD} = 5 V V_O = 2.5 V V_{IN} = 0.0 V or V_{DD}	All	1		-1.8	
				2 1/		-1.15	
				3 1/		-2.0	
		V_{DD} = 10 V V_O = 9.5 V V_{IN} = 0.0 V or V_{DD}	All	1		-1.4	
				2 1/		-0.9	
				3 1/		-1.6	
		V_{DD} = 15 V V_O = 13.5 V V_{IN} = 0.0 V or V_{DD}	All	1		-3.5	
				2 1/		-2.4	
				3 1/		-4.2	
Output voltage, high	V_{OH}	V_{DD} = 5 V, no load 1/	All	1, 2, 3	4.95		V
		V_{DD} = 10 V, no load 1/		1, 2, 3	9.95		
		V_{DD} = 15 V, no load 3/		1, 2, 3	14.95		
Output voltage, low	V_{OL}	V_{DD} = 5 V, no load 1/	All	1, 2, 3		0.05	V
		V_{DD} = 10 V, no load 1/		1, 2, 3		0.05	
		V_{DD} = 15 V, no load		1, 2, 3		0.05	
Input voltage, low	V_{IL}	V_{DD} = 5 V $V_{OH} > 4.5$ V, $V_{OL} < 0.5$ V	All	1, 2, 3		1.5	V
		V_{DD} = 10 V $V_{OH} > 9.0$ V, $V_{OL} < 1.0$ V 1/		1, 2, 3		3	
		V_{DD} = 15 V $V_{OH} > 13.5$ V, $V_{OL} < 1.5$ V		1, 2, 3		4	
Input voltage, high	V_{IH}	V_{DD} = 5 V $V_{OH} > 4.5$ V, $V_{OL} < 0.5$ V	All	1, 2, 3	3.5		V
		V_{DD} = 10 V $V_{OH} > 9.0$ V, $V_{OL} < 1.0$ V 1/		1, 2, 3	7		
		V_{DD} = 15 V $V_{OH} > 13.5$ V, $V_{OL} < 1.5$ V		1, 2, 3	11		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Input leakage current, low	I_{IL}	$V_{IN} = V_{DD}$ or GND, V_{DD} = 20 V	All	1	-100		nA
		$V_{IN} = V_{DD}$ or GND, V_{DD} = 20 V		2	-1000		
		$V_{IN} = V_{DD}$ or GND, V_{DD} = 18 V		3	-100		
Input leakage current, high	I_{IH}	$V_{IN} = V_{DD}$ or GND, V_{DD} = 20 V	All	1		100	
		$V_{IN} = V_{DD}$ or GND, V_{DD} = 20 V		2		1000	
		$V_{IN} = V_{DD}$ or GND, V_{DD} = 18 V		3		100	
N threshold voltage	V_{NTH}	V_{DD} = 10 V, I_{SS} = -10 µA	All	1	-0.7	-2.8	V
		M, D, P, L, R 2/	All	1	-0.2	-2.8	
N threshold voltage, delta	ΔV_{NTH}	V_{DD} = 10 V, I_{SS} = -10 µA M, D, P, L, R 2/	All	1		±1.0	
P threshold voltage	V_{PTH}	V_{SS} = 0.0 V, I_{DD} = 10 µA	All	1	0.7	2.8	
		M, D, P, L, R 2/	All	1	0.2	2.8	
P threshold voltage, delta	ΔV_{PTH}	V_{SS} = 0.0 V, I_{DD} = 10 µA M, D, P, L, R 2/	All	1		±1.0	
Input capacitance	C_{IN} 1/	Any input, See 4.4.1c	All	4		7.5	pF
Functional tests		V_{DD} = 2.8 V, $V_{IN} = V_{DD}$ or GND	All	7	$V_{OH} > V_{DD}/2$	$V_{OL} < V_{DD}/2$	V
		V_{DD} = 20 V, $V_{IN} = V_{DD}$ or GND		7			
		V_{DD} = 18 V, $V_{IN} = V_{DD}$ or GND	All	8A			
		M, D, P, L, R 2/	All	7			
		V_{DD} = 3.0 V, $V_{IN} = V_{DD}$ or GND	All	8B			
		M, D, P, L, R 2/	All	7			
Transition time 4/	t_{TLH}, t_{THL}	V_{DD} = 5.0 V, $V_{IN} = V_{DD}$ or GND	All	9		200	ns
				10, 11		270	
		V_{DD} = 10 V, $V_{IN} = V_{DD}$ or GND		9 1/		100	
		V_{DD} = 15 V, $V_{IN} = V_{DD}$ or GND		9 1/		80	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Propagation delay time	t_{PHL}, t_{PLH}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		320	ns
				10, 11		432	
		M, D, P, L, R 2/	All	9		432	
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND	All	9 1/		160	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9 1/		120	
Maximum clock input frequency 4/	F_{CL}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9	3.0		MHz
				10, 11	2.22		
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9 1/	6.0		
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9 1/	8.5		
Clock rise and fall time 1/ 4/ 5/	t_{RCL}, t_{FCL}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		15	µs
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		15	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		15	
Minimum hold time serial in, parallel in, parallel/serial control 1/ 4/	t_h	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		0	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		0	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		0	
Minimum clock pulse width 1/ 4/	t_W	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		180	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		80	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		50	
Minimum setup time, serial input (reference to CL) 1/ 4/	t_{S1}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	All	9		120	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		80	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		60	
Minimum setup time, parallel inputs (reference to CL) 1/ 4/	t_{S2}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	01, 03	9		80	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		50	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Units
					Min	Max	
Minimum setup time, parallel inputs (reference to P/S) 1/ 4/	t_{S3}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	02, 04	9		50	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		30	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		20	
Minimum setup time, parallel/serial control (reference to CL) 1/ 4/	t_{S4}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	01, 03	9		180	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		80	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		60	
Minimum P/S pulse width 1/ 4/	t_{WH}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	02, 04	9		160	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		80	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		50	
Minimum P/S removal time (reference to CL) 1/ 4/	t_{REM}	V_{DD} = 5.0 V, V_{IN} = V_{DD} or GND	02, 04	9		280	ns
		V_{DD} = 10 V, V_{IN} = V_{DD} or GND		9		140	
		V_{DD} = 15 V, V_{IN} = V_{DD} or GND		9		100	

1/ These tests are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which affect these characteristics.

2/ Devices supplied to this drawing will meet all levels M, D, P, L, R of irradiation. However, this device is only tested at the 'R' level. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ For accuracy, voltage is measured differentially to V_{DD}. Limit is 0.050 V Max.

4/ C_L = 50 pF, R_L = 200kΩ, input t_r, t_f < 20 ns.

5/ If more than one unit is cascaded, t_{RCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Device types	All
Case outlines	E and X
Terminal number	Terminal symbol
1	PI-8
2	Q6
3	Q8
4	PI-4
5	PI-3
6	PI-2
7	PI-1
8	V_{SS}
9	PARALLEL/SERIAL CONTROL
10	CLOCK
11	SERIAL IN
12	Q7
13	PI-5
14	PI-6
15	PI-7
16	V_{DD}

FIGURE 1. Terminal connections.

Device types 01 and 03

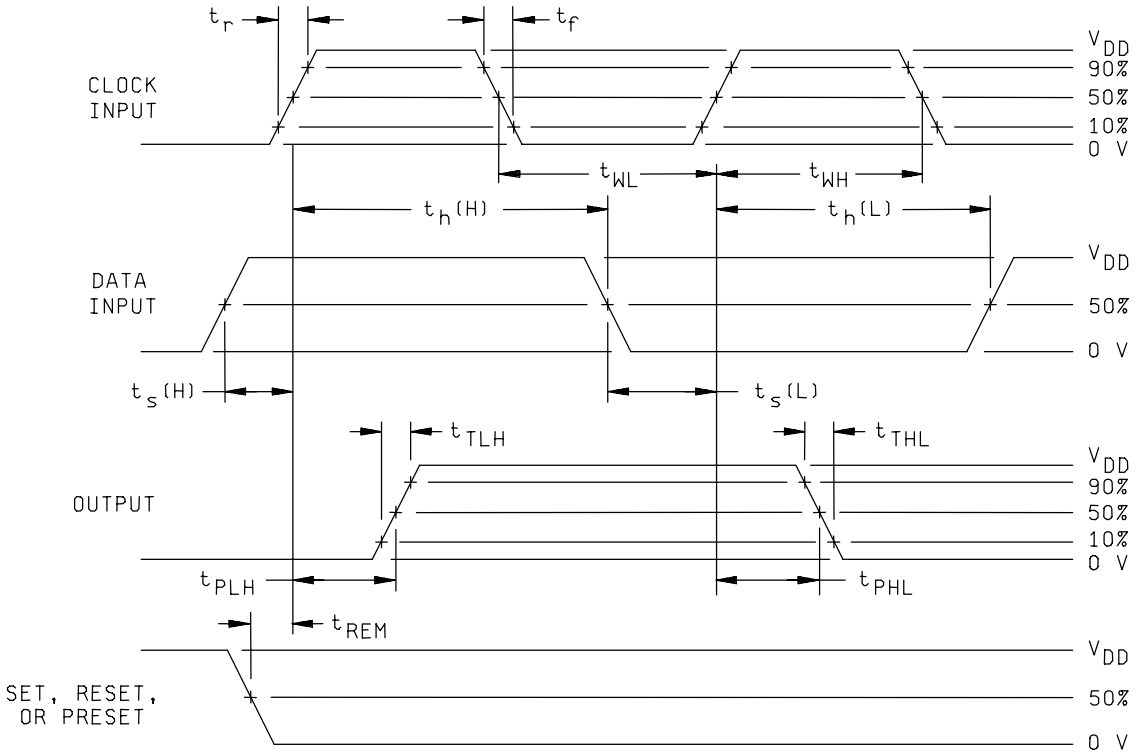
CL	SERIAL INPUT	PARALLEL/SERIAL CONTROL	PI-1	PI-n	Q1 (INTERNAL)	Qn	
↑	X	1	0	0	0	0	
↑	X	1	1	0	1	0	
↑	X	1	0	1	0	1	
↑	X	1	1	1	1	1	
↑	0	0	X	X	0	Qn-1	
↑	1	0	X	X	1	Qn-1	
↓	X	X	X	X	Q1	Qn	NC

Device types 02 and 04

CL	SERIAL INPUT	PARALLEL/SERIAL CONTROL	PI-1	PI-n	Q1 (INTERNAL)	Qn	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
↑	0	0	X	X	0	Qn-1	
↑	1	0	X	X	1	Qn-1	
↓	X	0	X	X	Q1	Qn	NC

↑ = Low to high transition
↓ = High to low transition
0 = Low logic level
1 = High logic level
X = Irrelevant
NC = No change

FIGURE 2. Truth tables.



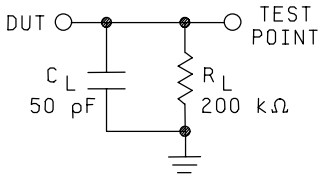


FIGURE 3. Load circuit and switching waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's quality management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth tables in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. Tests shall be sufficient to validate the limits defined in table I herein.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. Neutron irradiation for devices 03 and 04 shall be conducted in wafer form using a neutron fluence of approximately 1×10^{14} neutrons/cm^2.

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4 herein). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4 herein).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, 9, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test Delta parameters (+25°C).

Parameter	Symbol	Delta Limits
Supply current	I_{DD}	±0.1 µA
Output current (sink) V_{DD} = 5.0 V	I_{OL}	±20%
Output current (source) V_{DD} = 5.0 V, V_{OUT} = 4.6 V	I_{OH}	±20%

4.4.4.5 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

TABLE III. Irradiation test connections - Device types 01, 02, 03, and 04. 1/

Open	Ground	V_{DD} = 10 V ±0.5 V
2, 3, 12	8	1,4,5,6,7,9,10,11,13,14, 15,16

1/ Each pin except V_{DD} and GND will have a series resistor of 47KΩ ±5%, for irradiation testing.

4.5 Methods of inspection. Methods of inspection shall be as specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

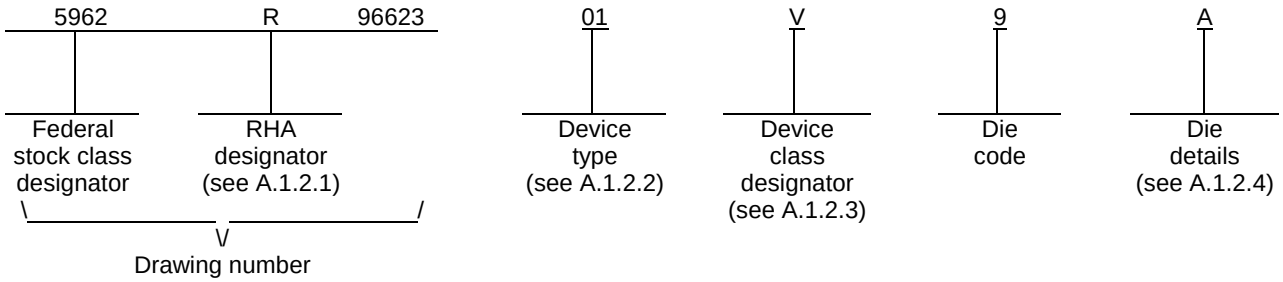
e. Occurrence of latchup (SEP).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-96623

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4014B	Radiation hardened, CMOS, synchronous parallel or serial input/serial output 8-stage static shift register
02	4021B	Radiation hardened, CMOS, asynchronous parallel input or synchronous serial input/serial output 8-stage static shift registers
03	4014BN	Radiation hardened, CMOS, synchronous parallel or serial input/serial output 8-stage static shift register with neutron irradiated die
04	4021BN	Radiation hardened, CMOS, asynchronous parallel input or synchronous serial input/serial output 8-stage static shift registers with neutron irradiated die

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die types	Figure number
01, 02, 03, 04	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die types	Figure number
01, 02, 03, 04	A-1

A.1.2.4.3 Interface materials.

Die types	Figure number
01, 02, 03, 04	A-1

A.1.2.4.4 Assembly related information.

Die types	Figure number
01, 02, 03, 04	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of the specification, standard, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth tables. The truth tables shall be as specified in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 QUALITY ASSURANCE PROVISIONS

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, test method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, test method 2010 or the alternate procedures allowed in MIL-STD-883, test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0547.

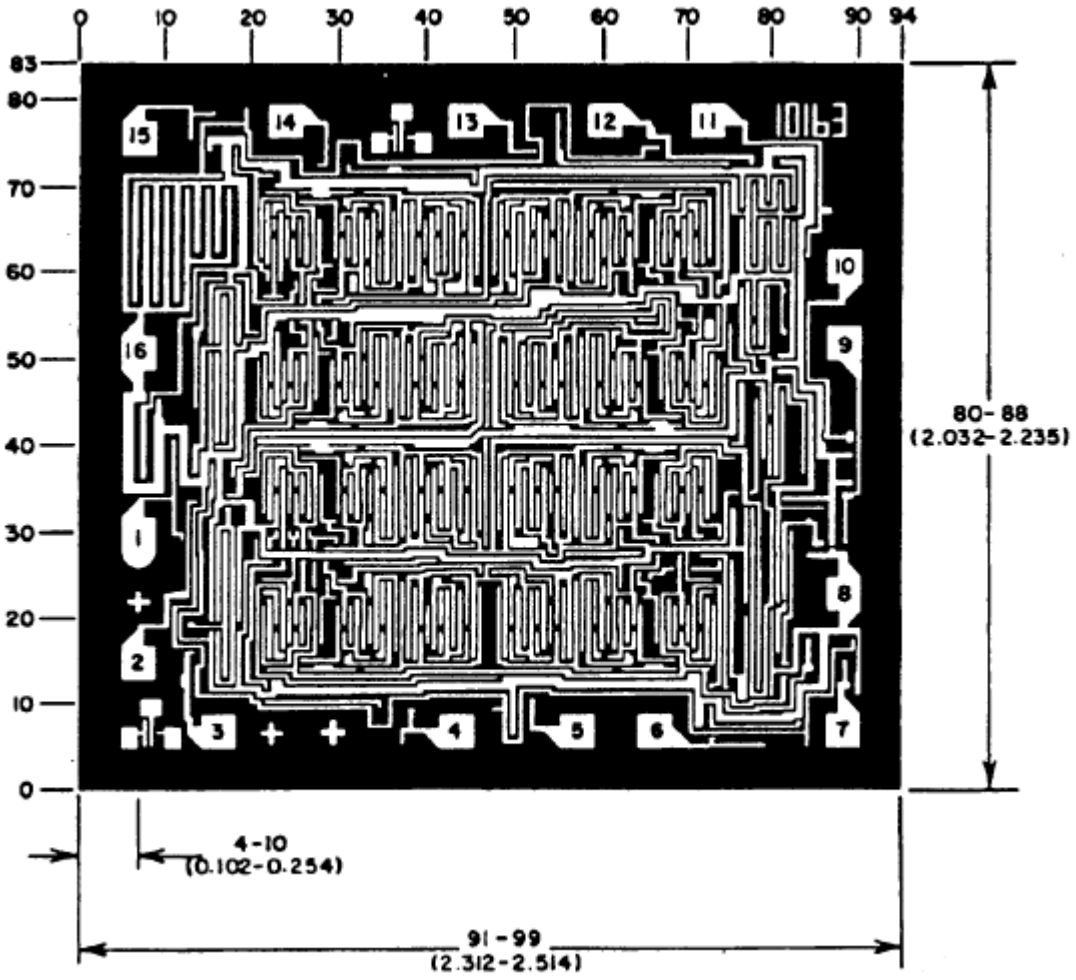
A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

Die physical dimensions.

Die size:	2108 x 2388 microns.
Die thickness:	20 ±1 mils.

Die bonding locations and electrical functions.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines E, X (see figure 1).

FIGURE A-1

Interface materials.

Top metallization:	Al	11.0kÅ – 14.0kÅ
Backside metallization:	None	
Glassivation.		
Type:	PSG	
Thickness:	10.4kÅ – 15.6kÅ	
Substrate:	Single Crystal Silicon.	

Assembly related information.

Substrate potential:	Floating or tied to V_{DD}.
Special assembly instructions:	Bond pad #16 (V_{DD}) first.

FIGURE A-1 – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-11-19

Approved sources of supply for SMD 5962-96623 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9662301VEC	3/	CD4014BDMSR
5962R9662301VXC	3/	CD4014BKMSR
5962R9662301V9A	3/	CD4014BHSR
5962R9662302VEC	34371	CD4021BDMSR
5962R9662302VXC	34371	CD4021BKMSR
5962R9662302V9A	3/	CD4021BHSR
5962R9662303VEC	3/	CD4014BDNSR
5962R9662303VXC	3/	CD4014BKNSR
5962R9662303V9A	3/	CD4014BHNSR
5962R9662304VEC	3/	CD4021BDNSR
5962R9662304VXC	3/	CD4021BKNSR
5962R9662304V9A	3/	CD4021BHNSR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 2401 Palm Bay Blvd P O Box 883 Melbourne, FL 32902-0883