

## Non-Volatile Digital Potentiometers With Up/Down (3-Wire) Interface, 10kΩ, 50kΩ, 100kΩ Resistance, 64 Taps, With/Without Output Buffer



The iPot™ ISL45005, ISL45006 DCPs are single channel 64-tap non-volatile linear digital potentiometers available in 10kΩ, 50kΩ and 100kΩ resistance. The devices consist of Up/Down serial interface, tap register, decoder, resistor array, wiper switches, NV memory and control logics.

The ISL45006 device can be configured as a two-terminal variable resistor or a three-terminal voltage divider without an output buffer, but the ISL45005 device, which has a built-in output buffer, can only be configured as a three-terminal voltage divider. Both devices can be used in a wide variety of applications.

The output of the potentiometer is determined by its wiper position, which varies linearly between its end terminals,  $R_A/V_A$  and  $R_B/V_B$ . The wiper position,  $R_W/V_W$ , is controlled by Up/Down serial interface ( $\overline{CS}$ ,  $\overline{INC}$ , and  $U/\overline{D}$ ) through the Tap Register (TR). In addition, the wiper position can also be stored into a non-volatile memory location (NVMEM0), which is then automatically recalled upon power up.

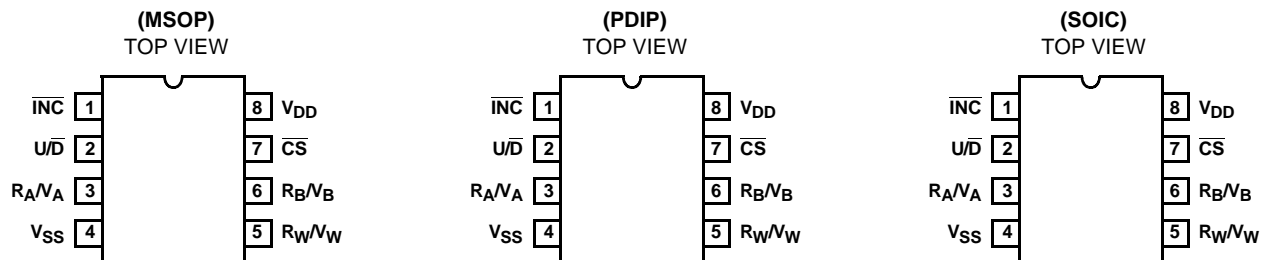
## Features

- Drop-in replacement for many popular parts
- Single linear-taper channel
- 64 taps
- 10K, 50K and 100K end-to-end resistance
- $V_{SS}$  to  $V_{DD}$  terminal voltages
- Automatic recall of wiper position when power-on
- Potentiometer control through Up/Down (3-wire) serial interface
- Endurance 100,000 cycles
- Data retention 100 years
- Package options:
  - 8-pin PDIP, SOIC or MSOP
- Industrial temperature range: -40° to 85°C
- Single supply operation: 2.7V to 5.5V

## Ordering Information

OUTPUT BUFFER	END-TO-END RESISTANCE	SOIC	PDIP	MSOP	TEMP. RANGE (°C)
No	10K	ISL45006IB01	ISL45006IP01	ISL45006IU01	-40 to 85
	50K	ISL45006IB05	ISL45006IP05	ISL45006IU05	-40 to 85
	100K	ISL45006IB10	ISL45006IP10	ISL45006IU10	-40 to 85
Yes	10K	ISL45005IB01	ISL45005IP01	ISL45005IU01	-40 to 85
	50K	ISL45005IB05	ISL45005IP05	ISL45005IU05	-40 to 85
	100K	ISL45005IB10	ISL45005IP10	ISL45005IU10	-40 to 85

**Pinouts**



**Pin Description**

PIN NAME	DESCRIPTION
$\overline{CS}$	<b>Chip Select:</b> When $\overline{CS}$ is LOW, the device is enabled. When $\overline{CS}$ is HIGH, the part is deselected and is in standby mode
$U/\overline{D}$	<b>Up/Down Control:</b> HIGH state enables the wiper to move towards the $R_A/V_A$ terminal, while LOW state implies the wiper moves towards the $R_B/V_B$ terminal
$\overline{INC}$	<b>Increment Control:</b> When $\overline{CS}$ is LOW, a HIGH-LOW transition on $\overline{INC}$ will move the wiper one increment either up or down based on the $U/\overline{D}$ input
$R_A/V_A$	<b>High terminal</b> of the device
$R_B/V_B$	<b>Low terminal</b> of the device
$R_W/V_W$	<b>Wiper Terminal:</b> Output of the resistor array is determined by the $\overline{INC}$ , $U/\overline{D}$ and $\overline{CS}$ inputs
$V_{SS}$	Ground pin, logic ground reference
$V_{DD}$	Power Supply

**NOTE:**

The terminology of high and low terminals above references to the relative position of the terminal with respect to the wiper moving direction and not the voltage potential of the terminal.

Block Diagrams

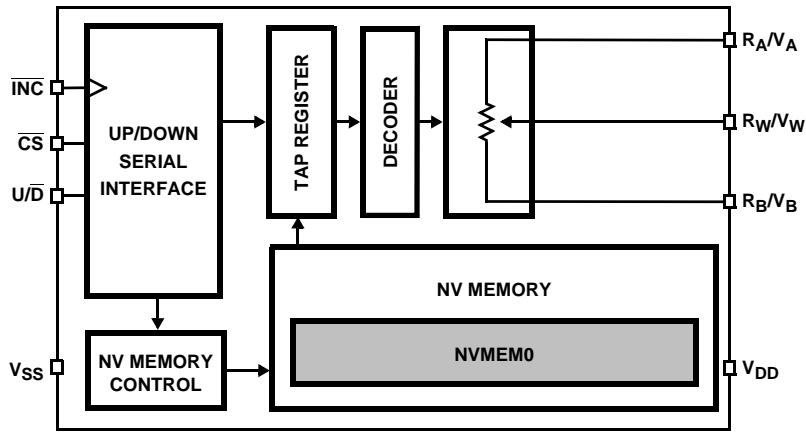


FIGURE 1. ISL45006 BLOCK DIAGRAM (RHEOSTAT/DIVIDER MODE)

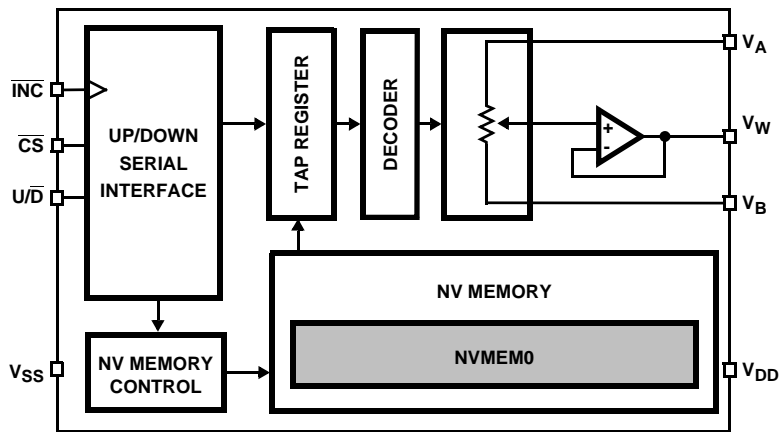


FIGURE 2. ISL45005 BLOCK DIAGRAM (DIVIDER MODE)

**Absolute Maximum Ratings**

Voltage Applied to Any Pad . . . . . ( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )  
 $V_{SS} - V_{DD}$  . . . . . -0.3 to 7.0V

**Operating Conditions**

Industrial Operating Temperature . . . . . -40°C to +85°C  
 Supply Voltage ( $V_{DD}$ ) . . . . . +2.7V to +5.5V  
 Ground Voltage ( $V_{SS}$ ) . . . . . 0V

**Thermal Information**

Thermal Resistance (Typical)  $\theta_{JA}$  (0m/s air velocity)  
 MSOP Package . . . . . 130  
 PDIP Package . . . . . 120  
 SOIC Package . . . . . 160  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 235°C (SOIC, Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**Electrical Specifications** Packaged parts.

PARAMETERS	SYMBOL	CONDITIONS (NOTE 5)	MIN	TYP	MAX	UNITS
<b>RHEOSTAT MODE</b>						
Nominal Resistance	R	T = 25°C, Wiper open	-20		+20	%
Different Non Linearity (Note 2)	R-DNL	(Note 6)	-1	±0.2	+1	LSB
Integral Non Linearity (Note 2)	R-INL	(Note 6)	-1	±0.4	+1	LSB
Tempo (Note 1)	$\Delta R_{AB}/\Delta T$			200		ppm/°C
Wiper Resistance (Note 2)	$R_W$	$V_{DD} = 5V, I = V_{DD}/R_{Total}$ (Note 7)		50		$\Omega$
		$V_{DD} = 2.7V, I = V_{DD}/R_{Total}$ (Note 7)		80		$\Omega$
Wiper Current	$I_W$		-1		1	mA
<b>DIVIDER MODE</b>						
Resolution	N		6			Bits
Different Non Linearity (Note 2)	DNL		-1	±0.5	+1	LSB
Integral Non Linearity (Note 2)	INL		-1	±0.5	+1	LSB
Temperature Coefficient (Note 1)	$\Delta W/\Delta T$	Wiper at center		+20		ppm/°C
Full Scale Error	$V_{FSE}$	Wiper at highest position	-1		0	LSB
Zero Scale Error	$V_{ZSE}$	Wiper at lowest position	0		1	LSB
<b>RESISTOR TERMINAL</b>						
Voltage Range	$V_A, V_B, V_W$		$V_{SS}$		$V_{DD}$	V
Terminal Capacitance (Note 1)	$C_A, C_B$			30		pF
Wiper Capacitance (Note 1)				30		pF
<b>DYNAMIC CHARACTERISTICS (Note 1)</b>						
Bandwidth -3dB	$BW_{10K}$	$V_{DD} = 5V, B = V_{SS}$ Wiper at center		1.5		MHz
	$BW_{50K}$			300		kHz
	$BW_{100K}$			200		kHz
<b>ANALOG OUTPUT (Buffer Enables)</b>						
Amp Output Current	$I_{OUT}$	$V_O = 1/2$ scale	3			mA
Amp Output Resistance	$R_{out}$	$I_L = 100\mu A$		1	10	$\Omega$
Total Harmonic Distortion (Note 1)	THD	$A = 2.5V, V_{DD} = 5V, f = 1kHz, V_{IN} = 1V_{RMS}$			0.08	%

## ISL45005, ISL45006

### Electrical Specifications Packaged parts. (Continued)

PARAMETERS	SYMBOL	CONDITIONS (NOTE 5)	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS/OUTPUTS</b>						
Input High Voltage	$V_{IH}$		$0.7 \times V_{DD}$			V
Input Low Voltage	$V_{IL}$				$0.3 \times V_{DD}$	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 2\text{mA}$			0.4	V
Input Leakage Current	$I_{LI}$	$\overline{CS} = V_{DD}, V_{in} = V_{SS} \sim V_{DD}$	-1		+1	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$\overline{CS} = V_{DD}, V_{in} = V_{SS} \sim V_{DD}$	-1		+1	$\mu\text{A}$
Input Capacitance (Note 1)	$C_{IN}$	$V_{DD} = 5\text{V}, f_c = 1\text{MHz}$		25		pF
Output Capacitance (Note 1)	$C_{OUT}$	$V_{DD} = 5\text{V}, f_c = 1\text{MHz}$		25		pF
<b>POWER REQUIREMENTS</b>						
Operating Voltage	$V_{DD}$		2.7		5.5	V
Operating Current	$I_{DDR}, I_{DDW}$	All operations		1	2	mA
Standby Current	$I_{SA}$ (Note 3)	Buffer = ON $\overline{CS} = \text{HIGH}$ , no load		0.5	1	mA
	$I_{SB}$ (Note 4)	Buffer = OFF $\overline{CS} = \text{HIGH}$ , no load		0.1	1	$\mu\text{A}$
Power Supply Rejection Ratio	PSRR	$V_{DD} = 5\text{V} \pm 10\%$ , Wiper at center			1	LSB/V

**NOTES:**

1. Not subject to production test.
2.  $LSB = (R_A/V_A - R_B/V_B)/(T - 1)$ ;  $DNL = (V_i - V_{i+1})/LSB + 1$  (if increment) or  $(V_i - V_{i+1})/LSB - 1$  (if decrement);  $INL = (V_i - i \cdot LSB)/LSB$ ; where  $i = [0, (T - 1)]$  and  $T = \#$  of taps of the device.
3. ISL45005 only.
4. ISL45006 only.
5. Conditions:  $V_{CC} = 2.7$  to  $5.5\text{V}$ ,  $T = 25^\circ\text{C}$  and timing measured at 50% level, unless stated.
6. Only guarantee by design.
7.  $R_{Total}$  = end-to-end resistance.

## Functional Description

### Rheostat and Divider Operations

The ISL45006 device can operate as either a two-terminal variable resistor or a three-terminal voltage divider without an output buffer. However, the ISL45005 can only operate in a three-terminal voltage divider with an output buffer.

#### RHEOSTAT CONFIGURATION

In the rheostat mode, the ISL45006 can be configured as a two-terminal resistive element, where one terminal is connected to one end of the resistor ( $R_A$  or  $R_B$ ) and the other terminal is the wiper ( $R_W$ ). The moving direction of the wiper depends upon the setting of  $U/\bar{D}$  control signal. When the  $U/\bar{D}$  is set to Up, then the wiper moves towards  $R_A$ . Conversely, when the  $U/\bar{D}$  is set to Down, then the wiper moves towards  $R_B$ . The wiper movement to either direction is controlled by toggling the  $\bar{INC}$  signal from HIGH to LOW.

This configuration controls the resistance between the wiper and either end. The wiper resistance can be adjusted by either changing the wiper position or loading a stored wiper position value from NVMEM0 upon power up.

#### DIVIDER CONFIGURATION

Additionally, the ISL45006 can also be configured as a voltage divider. With an input voltage applied to one end (usually  $V_A$ ), the ground is connected to the other end (usually  $V_B$ ). These input voltages cannot exceed the  $V_{DD}$  level or go below the  $V_{SS}$  level. The voltage on the wiper,  $V_W$ , is proportional to the wiper position with respect to the voltage difference between  $V_A$  and  $V_B$ . The moving direction of the wiper depends upon the setting of the  $U/\bar{D}$  control signal. When the  $U/\bar{D}$  is set to Up, then the wiper moves towards  $V_A$ . Conversely, when the  $U/\bar{D}$  is set to Down, then the wiper moves towards  $V_B$ . The wiper movement to either direction is controlled by toggling the  $\bar{INC}$  signal from HIGH to LOW.

Nevertheless, the ISL45005 can only be configured as a voltage divider and operate similarly as the ISL45006 device. The only difference is ISL45005 has an output buffer, but ISL45006 doesn't have.

Besides, the resistance cannot be directly measured in this configuration.

### Non-Volatile Memory (NVMEM0)

The ISL45005/ISL45006 has one NVMEM0 location available for storing the current wiper position via the Up/Down serial interface. This stored value is automatically recalled and loaded into the tap register upon power up.

## Serial Data Interface

The ISL45005/ISL45006 device has a 3-wire Up/Down Serial Interface consisting of  $\bar{CS}$ ,  $\bar{INC}$  and  $U/\bar{D}$  control signals. The key features of this interface include:

- Enabling the device
- Determining the moving direction of the wiper
- Increment/Decrement operation on the wiper
- Non-volatile storage of the present wiper position into the NVMEM0 for automatic recall at power up
- Entering into the standby mode

### Operation Overview

The wiper position can be changed either up or down by operating the  $\bar{CS}$ ,  $U/\bar{D}$  and  $\bar{INC}$  control signals.



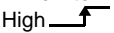
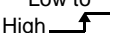
When  $\bar{CS}$  is LOW, the device is selected and the wiper can be moved by toggling the  $\bar{INC}$ . As a result, the wiper moves up when  $U/\bar{D}$  is HIGH and moves down when  $U/\bar{D}$  is LOW. The status of the  $U/\bar{D}$  can be changed even though the  $\bar{CS}$  remains LOW. This allows the system to enable the device and then move the wiper position either up or down until the desired position is reached.

When the wiper is already at the lowest position, further Down operation won't change the wiper position. Similarly, when the wiper is at the highest position, further Up operation won't change the wiper position too.

The current wiper position can be automatically stored into the NVMEM0 each time the  $\bar{CS}$  goes from LOW to HIGH while the  $\bar{INC}$  remains HIGH. Adversely, if the  $\bar{INC}$  is LOW when the  $\bar{CS}$  goes HIGH, the wiper position cannot be stored. Meanwhile, the NVMEM0 content is automatically loaded into the wiper during power on.

When the  $\bar{CS}$  is held HIGH, the device enters into Standby mode and the wiper position cannot be changed. Changing the  $\bar{CS}$  to LOW exits the Standby mode and enables the device again.

The operating modes of Up/Down interface are summarized in the table below:

$\bar{CS}$	$U/\bar{D}$	$\bar{INC}$	OPERATION
Low	High	 High to Low	Move Wiper toward $R_A/V_A$
Low	Low	 High to Low	Move Wiper toward $R_B/V_B$
Low to High 	x	High	Store Current Wiper Position
Low to High 	x	Low	No Store, Return to Standby
High	x	x	Standby

NOTE: x means don't care.

**Timing Diagram**  $V_{DD} = +2.7V$  to  $5.5V$ ,  $V_A = V_{DD}$ ,  $V_B = 0V$ ,  $T = 25^\circ C$

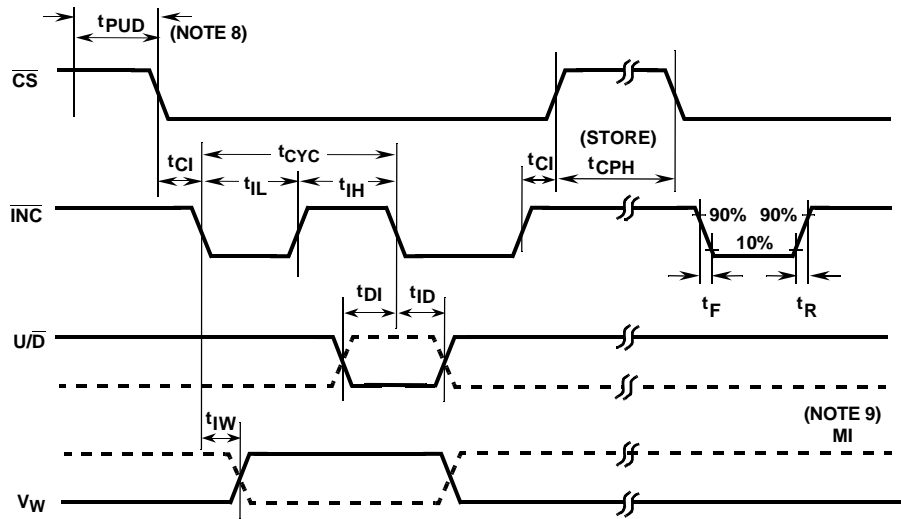


FIGURE 3. ISL45005, ISL45006 TIMING DIAGRAM

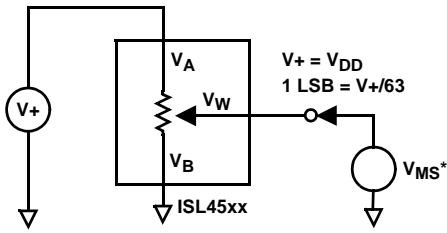
NOTES:

- 8. This only applies to the Power-Up sequence.
- 9. MI in the AC Timing diagram (Figure 3) refers to the minimum incremental change in the wiper output due to a change in the wiper position.

**Timing Parameters**

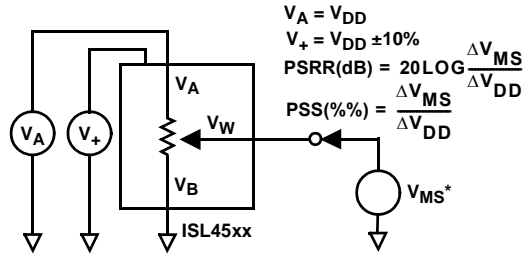
PARAMETERS	SYMBOL	MIN	MAX	UNITS
$\overline{CS}$ to $\overline{INC}$ Setup	$t_{CI}$	100		ns
$\overline{U/D}$ to $\overline{INC}$ Setup	$t_{DI}$	50		ns
$\overline{U/D}$ to $\overline{INC}$ Hold	$t_{ID}$	100		ns
$\overline{INC}$ LOW Period	$t_{IL}$	250		ns
$\overline{INC}$ HIGH Period	$t_{IH}$	250		ns
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	$t_{IC}$	1		$\mu s$
$\overline{CS}$ Deselect Time (NO STORE)	$t_{CPH}$	100		ns
$\overline{CS}$ Deselect Time (STORE)	$t_{CPH}$	15 (2.7V) 30 (5.5V)		ms
$\overline{INC}$ to Wiper Change	$t_{IW}$		5	$\mu s$
$\overline{INC}$ Cycle Time	$t_{CYC}$	1		$\mu s$
$\overline{INC}$ Input Rise and Fall Time	$t_R, t_F$		500	$\mu s$
Power-Up Delay	$t_{PUD}$		1	ms
$V_{CC}$ Power-Up Rate	$t_R V_{CC}$	0.2 (13ms, 0-2.7V)	50 (54 $\mu s$ , 0-2.7V)	V/ms

Test Circuits



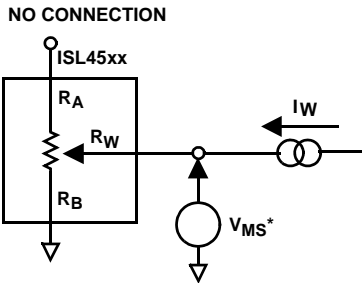
\*Assume infinite input impedance

FIGURE 4. POTENTIOMETER DIVIDER NONLINEARITY ERROR TEST CIRCUIT (INL, DNL)



\*Assume infinite input impedance

FIGURE 5. POWER SUPPLY SENSITIVITY TEST CIRCUIT (PSS, PSRR)



\*Assume infinite input impedance

FIGURE 6. RESISTOR POSITION NONLINEARITY ERROR TEST CIRCUIT (RHEOSTAT OPERATION: R-INL, R-DNL)

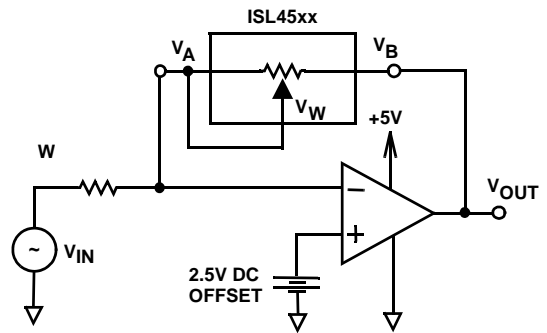
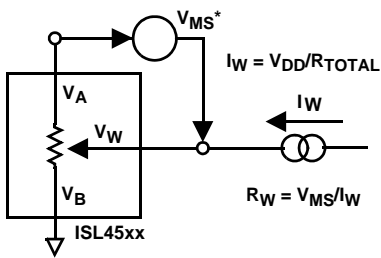


FIGURE 7. CAPACITANCE TEST CIRCUIT



\*Assume infinite input impedance

FIGURE 8. WIPER RESISTANCE TEST CIRCUIT

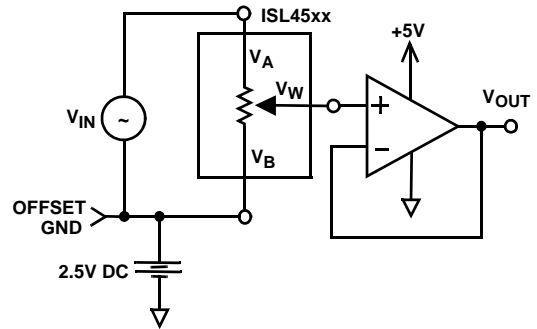
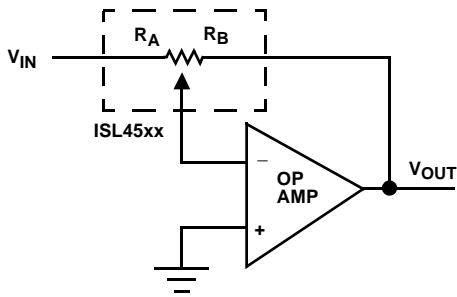


FIGURE 9. GAIN vs FREQUENCY TEST CIRCUIT



Typical Application Circuits

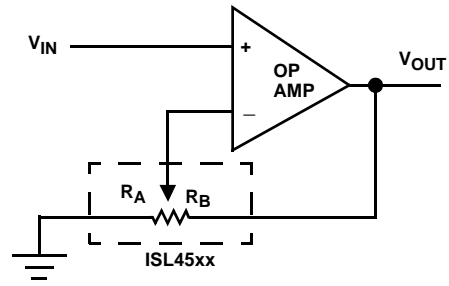


$$V_{OUT} = -V_{IN} \frac{R_B}{R_A}$$

$$R_A = \frac{R_{AB}(64-W)}{64}, R_B = \frac{R_{AB} \cdot W}{64}$$

$R_{AB}$  = Total resistance of potentiometer.  
 $W$  = Wiper setting for ISL45xx

FIGURE 10. PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE ISL45005/ISL45006



$$V_{OUT} = V_{IN} \left( 1 + \frac{R_B}{R_A} \right)$$

$$R_A = \frac{R_{AB}(64-W)}{64}, R_B = \frac{R_{AB} \cdot W}{64}$$

$R_{AB}$  = Total resistance of potentiometer.  
 $W$  = Wiper setting for ISL45xx

FIGURE 11. PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE ISL45005/ISL45006

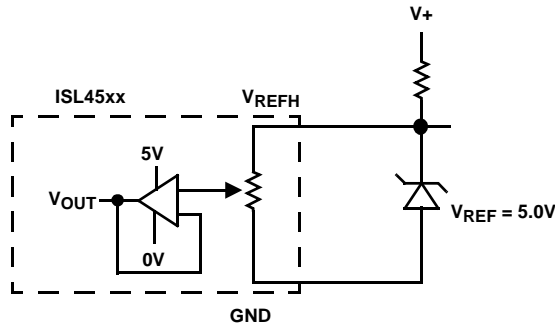


FIGURE 12. ISL45005 TRIMMING VOLTAGE REFERENCE

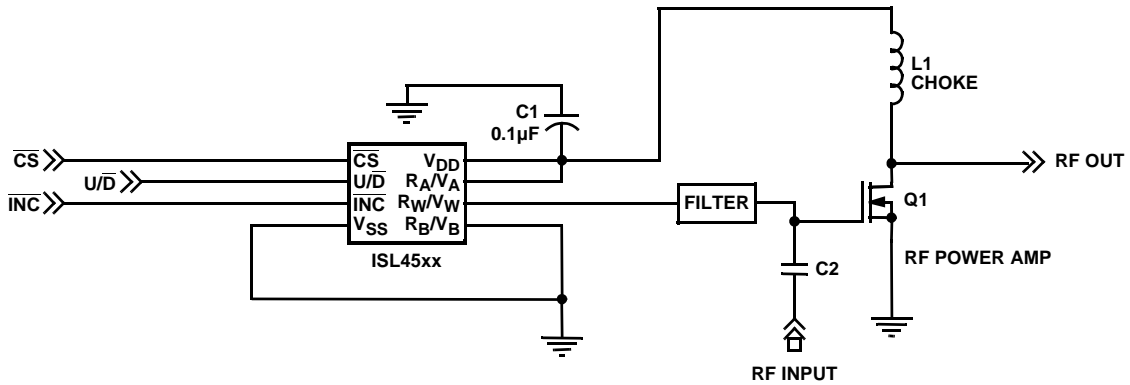


FIGURE 13. ISL45005 RF AMP CONTROL

**Layout Considerations**

Use a 0.1 $\mu$ F bypass capacitor as close as possible to the  $V_{DD}$  pin. This is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the  $V_{DD}$  and  $V_{SS}$  pins. Care should be taken to separate the analog

and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.

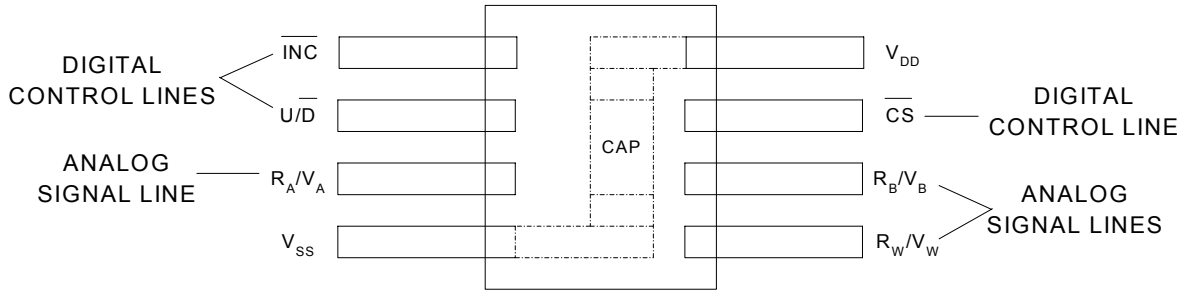
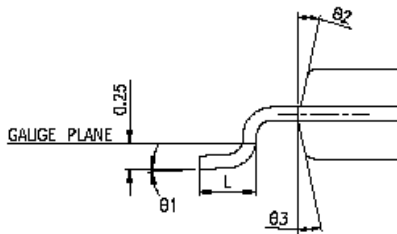
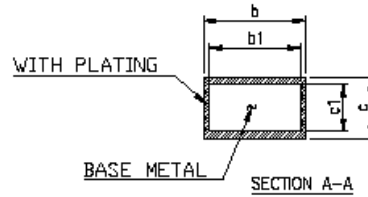
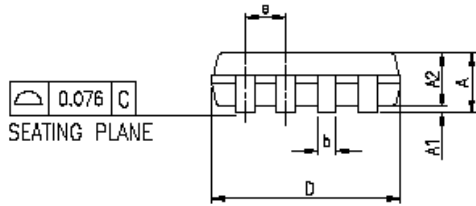
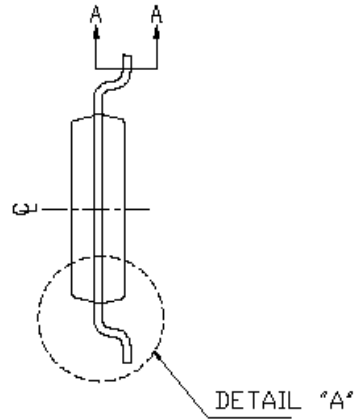
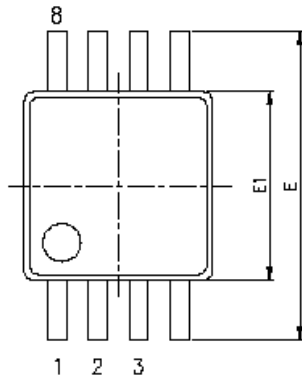


FIGURE 14. ISL45005, ISL45006 LAYOUT

Mini Small Outline Plastic Packages (MSOP)

8 Lead 3mm MSOP



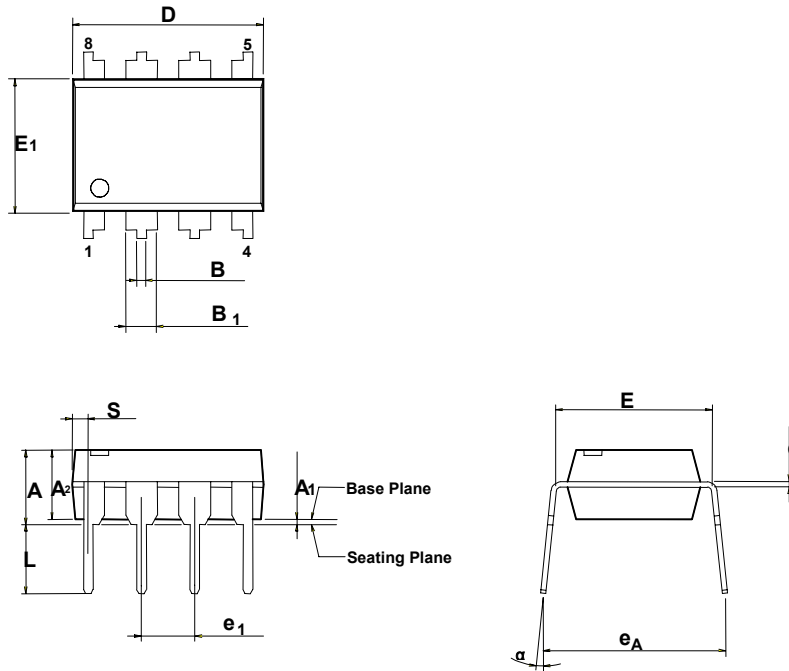
DETAIL "A"  
SCALE 25:1

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.10	---	---	0.043
A1	0.05	---	0.15	0.002	---	0.006
A2	0.81	0.86	0.91	D.032	D.034	0.036
c	0.13	---	0.23	D.005	---	0.009
c1	0.13	0.15	0.18	D.005	D.006	D.007
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.90	3.00	3.10	0.114	0.118	0.122
E	4.90 BSC			0.193 BSC		
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
$\theta 1$	0°		6°	0°		6°

SYMBOL	$\theta L$			1DL		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.25	---	0.40	0.17	---	0.27
b1	0.25	0.30	0.35	0.17	0.20	0.23
e	0.85 BSC			0.50 BSC		
JEDEC	MO-187AA			MO-187		

Dual-In-Line Plastic Packages (PDIP)

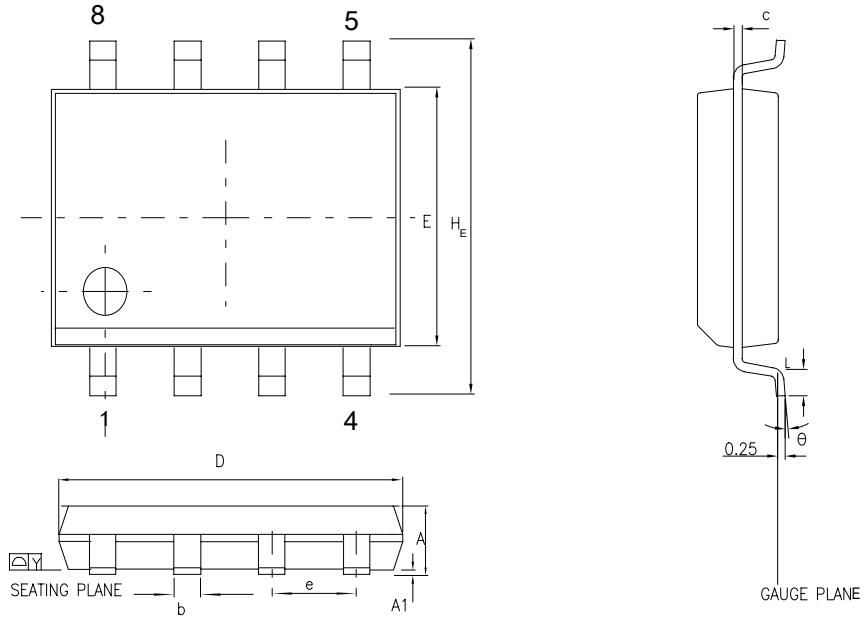
8 Lead 300MIL PDIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A <sub>1</sub>	0.010	—	—	0.25	—	—
A <sub>2</sub>	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B <sub>1</sub>	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.360	0.380	—	9.14	9.65
E	0.290	0.300	0.310	7.37	7.62	7.87
E <sub>1</sub>	0.245	0.250	0.255	6.22	6.35	6.48
e <sub>1</sub>	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
alpha	0	—	15	0	—	15
e <sub>A</sub>	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.045	—	—	1.14

Small Outline Plastic Packages (SOIC)

8 Lead 150MIL SOIC



Control dimensions are in millimeters.

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	4.80	5.00	0.188	0.196
e	1.27 BSC		0.050 BSC	
HE	5.80	6.20	0.228	0.244
Y	0.10		0.004	
L	0.40	1.27	0.016	0.050
theta	0	10	0	10

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