Data Sheet | March 2004 | FN6069.1

256-Tap Dual-Channel Non-Volatile Digital Potentiometer

The iPot™ ISL45022 DCP is a 256-tap, dual-channel non-volatile digital potentiometer available in 10kΩ, 50kΩ and 100kΩ end-to-end resistances. These devices can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications.

The output of each potentiometer is determined by the wiper position, which varies linearly between VA and VB terminal according to the content stored in the volatile Tap Register (TR). The settings of the TR can be provided either directly by the user through the industry standard SPI interface, or by the non-volatile memory (NVMEM0~3) where the previous settings are stored. When changes are made to the TR to establish a new wiper position, the value of the setting can be saved into any non-volatile memory location (NVMEM0~3) by executing a NVMEM save operation. Each channel has its own four non-volatile memory locations (NVMEM0~3) that can be directly written to, and read by, users through the SPI interface. Upon powerup the content of the NVMEM0 is automatically loaded to the Tap Register.

The ISL45022 contains two independent channels in 14-pin PDIP, SOIC and TSSOP packages and can operate over a wide operating voltage range from 2.7V to 5.5V. A selectable output buffer is built-in for each channel for those applications where an output buffer is required.

Features

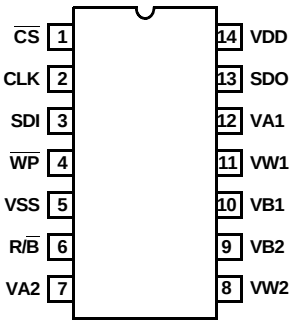
- 256 taps for each potentiometer
- Dual independent, linear-taper channels in one package
- End-to-end resistance available in 10kΩ, 50kΩ and 100kΩ
- Selectable output buffer for each channel
- SPI Serial Interface for data transfer and potentiometer control
- Daisy-chain operation for multiple devices
- Nonvolatile storage of four wiper positions per channel with power-on recall from NVMEM0
- Low standby current (1μA Max. with output buffer inactive)
- Endurance 100K typical stores per bit
- Register Data Retention 100 years
- Industrial temperature range: -40°C ~ 85°C
- Wide operating voltage range: 2.7V ~ 5.5V
- Package option:
  - 14-pin TSSOP, 14-pin SOIC, 14-pin PDIP

Ordering Information

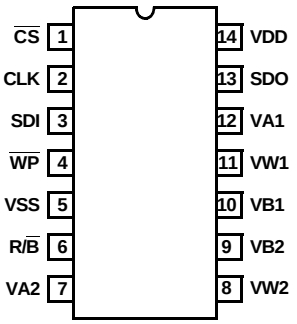
OUTPUT BUFFER	END-TO-END RESISTANCE	TSSOP	SOIC	PDIP	TEMP. RANGE (°C)
Yes	10K	ISL45022IV01	ISL45022IB01	ISL45022IP01	-40 to 85
	50K	ISL45022IV05	ISL45022IB05	ISL45022IP05	-40 to 85
	100K	ISL45022IV10	ISL45022IB10	ISL45022IP10	-40 to 85

Pinouts

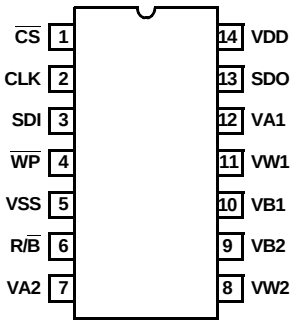
(PDIP)
TOP VIEW



(SOIC)
TOP VIEW



(TSSOP)
TOP VIEW



Pin Description

PIN NAME	PIN NO	I/O	DESCRIPTION
CLK	2	I	**Serial Clock pin.** Data Shifts in one bit at a time on positive clock (CLK) edges
$\overline{CS}$	1	I	**Chip Select pin.** When $\overline{CS}$ is HIGH, ISL45022 is deselected and the SDO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. CS LOW enables ISL45022, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.
SDI	3	I	**Serial Data Input pin.** All opcodes, byte addresses and data to be written to the registers are input on this pin. Data is latched by the rising edge of the serial clock.
SDO	13	O	**Serial Data Output pin with open-drain output.** During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock except for the 1^{st} bit, which is clocked out by the falling edge of $\overline{CS}$. Also can be used to daisy-chain several parts.
R/$\overline{B}$	6	O	Ready signal with active-LOW, open-drain output, and acknowledges the completion of commands 2, 4, 5, 6, and 7.
$\overline{WP}$	4	I	Hardware Write Protect pin. When active LOW $\overline{WP}$ prevents any changes to the present contents except retrieving NVMEM contents.
V_{DD}	14	-	Power Supply
V_{SS}	5	-	Ground pin, logic ground reference
VA1	12	-	A terminal of potentiometer ‘1’, equivalent to the HI terminal connection on a mechanical potentiometer
VB1	10	-	B terminal of potentiometer ‘1’, equivalent to the LO terminal connection on a mechanical potentiometer
VW1	11	O	Wiper terminal of potentiometer ‘1’, equivalent to the wiper terminal of a mechanical potentiometer
VA2	7	-	A terminal of potentiometer ‘2’, equivalent to the HI terminal connection on a mechanical potentiometer.
VB2	9	-	B terminal of potentiometer ‘2’, equivalent to the LO terminal connection on a mechanical potentiometer.
VW2	8	O	Wiper terminal of potentiometer ‘2’, equivalent to the wiper terminal of a mechanical potentiometer.

Block Diagram

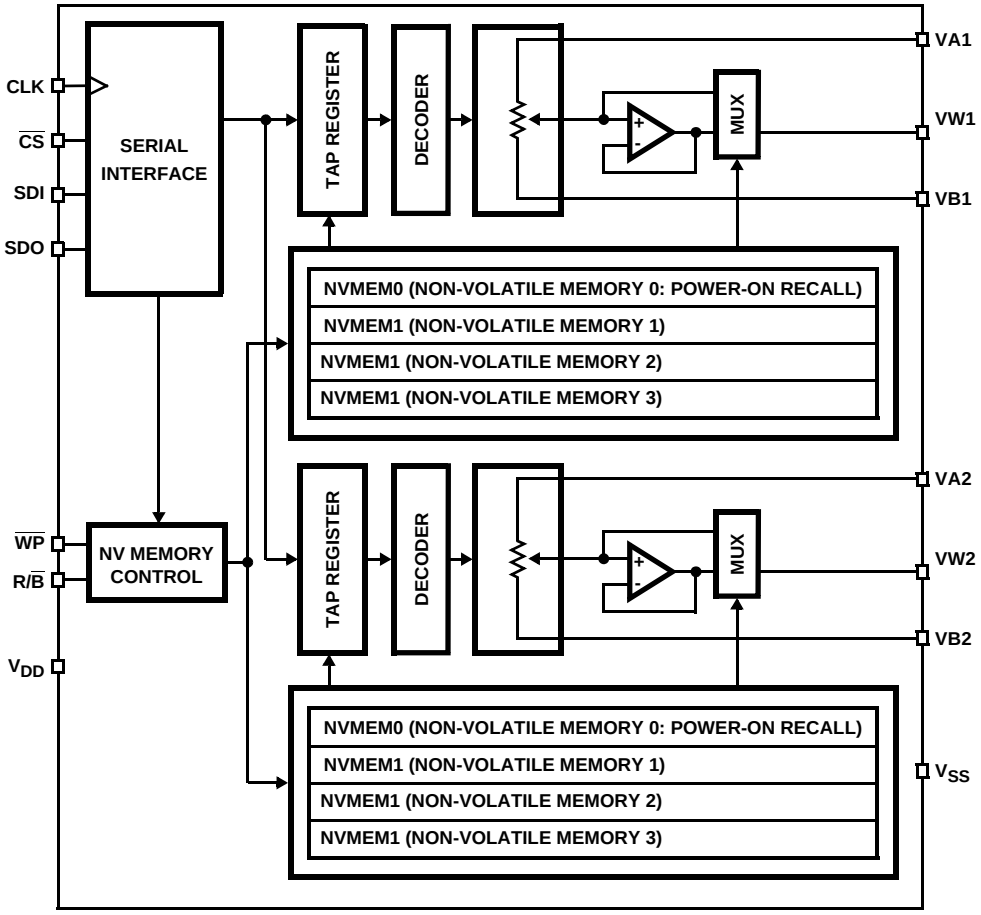


FIGURE 1. ISL45022 BLOCK DIAGRAM

Absolute Maximum Ratings

Voltage Applied to Any Pad . . . . . .(V_{SS} – 0.3V) to (V_{DD} + 0.3V)
V_{DD} – V_{SS} . . . . . -0.3 to 7.0V

Operating Conditions

Industrial Operating Temperature . . . . . .-40°C to +85°C
Supply Voltage (VDD) . . . . . .+2.7V to +5.5V
Ground Voltage (VSS) 0V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (0m/s air velocity)
TSSOP Package	120
PDIP Package	85
SOIC Package	115

Maximum Junction Temperature (Plastic Package) . . . . . .150°C
Maximum Storage Temperature Range . . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .235°C
(SOIC, Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

VDD: 2.7V~5.5V; Temp: –40°C~85°C; Typical values: VDD = 5V and T = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP	MAX.	UNITS
RHEOSTAT MODE						
Nominal Resistance	R	T = 25°C, V_W open	-20		+20	%
Different Non Linearity	DNL		-1	0.3	+1	LSB
Integral Non Linearity	INL		-1	0.5	+1	LSB
Rheostat Tempco (Note 1)	$\Delta R_{AB}/\Delta T$			200		ppm/°C
Wiper Resistance (Note 2)	R_W	V_{DD} = 5V, I = V_{DD}/R_{Total}		50	100	Ω
		V_{DD} = 2.7V, I = V_{DD}/R_{Total}		80	120	Ω
POTENTIOMETER MODE						
Resolution (Note 1)	N		8			Bits
Different Non Linearity (Note 2)	DNL		-1		+1	LSB
Integral Non Linearity (Note 2)	INL		-1		+1	LSB
Potentiometer Tempco (Note 1)	$\Delta V_w/\Delta T$	Code = 80h		+20		ppm/°C
Full Scale Error	V_{FSE}	Code = Full Scale	-1		0	LSB
Zero Scale Error	V_{ZSE}	Code = Zero Scale	0		1	LSB
RESISTOR TERMINAL						
Voltage Range (Note 1)	V_A,V_B,V_W		V_{SS}		V_{DD}	V
Terminal Capacitance (Note 1)	C_A, C_B			30		pF
Wiper Capacitance (Note 1)				30		pF
DYNAMIC CHARACTERISTICS[1]						
	BW_{10K}	V_{DD} = 5V, V_B = V_{SS} Code = Full Scale		1.5		MHz
Bandwidth -3dB	BW_{50K}	Code = 80h		300		kHz
	BW_{100K}	CL = 30pF		200		kHz
Settling Time to 1 LSB	T_S	V_{DD} = 5.5V = V_A, V_B = V_{SS}		80	100	µs
ANALOG OUTPUT (BUFFER ENABLED)						
Amp Output Current (Note 2)	I_{OUT}	V_O = 1/2 scale	3			mA
Amp Output Resistance (Note 2)	Rout			1	10	
Total Harmonic Distortion (Note 1)	THD	V_A = 2.5V, V_{DD} = 5V, f = 1kHz, V_{IN} = $1V_{RMS}$			0.08	%
DIGITAL INPUTS/OUTPUTS						
Input High Voltage	V_{IH}		$0.7V_{DD}$			V
Input Low Voltage	V_{IL}				$0.3V_{DD}$	V

Electrical Specifications VDD: 2.7V~5.5V; Temp: –40°C~85°C; Typical values: VDD = 5V and T = 25°C, Unless Otherwise Specified

Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4	V
Input Leakage Current	I_{LI}	$\overline{CS}$ = V_{DD}, Vin = Vss ~ V_{DD}	-1		+1	µA
Output Leakage Current	I_{Lo}	$\overline{CS}$ = V_{DD}, Vin = V_{SS} ~ V_{DD}	-1		+1	µA
Input Capacitance (Note 1)	C_{IN}	V_{DD} = 5V, fc = 1MHz Code = 80h		25		pF
Output Capacitance (Note 1)	C_{OUT}	V_{DD} = 5V, fc = 1MHz Code = 80h		25		pF
POWER REQUIREMENTS						
Operating Voltage (Note 1)	V_{DD}		2.7		5.5	V
Operating Current	I_{DDR}	All ops except NVMEM program		1	1.8	mA
Operating Current	I_{DDW}	During Non-volatile memory program		1	2	mA
Standby Current	I_{SA}	Buffer is active, no load	0.5		1	mA
	I_{SB} (Note 2)	Buffer is inactive, Power Down, No load		0.1	1	µA
Power Supply Rejection Ratio	PSRR	V_{DD} = 5V ±10%, Code = 80h			1	LSB/V

NOTES:

1. Not subject to production test.
2. Only on Final Test.
3. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, T = 25°C, unless otherwise noted.

Functional Description

The ISL45022 series, a family of 256-tap, nonvolatile digitally programmable potentiometers is designed to operate as both a potentiometer or a variable resistor depending upon the output configuration selected.

The chip can store four 9-bit words in nonvolatile memory (NVMEM0 ~ NVMEM3) and the word stored in the NVMEM0 will be used to set the tap register values when the device is powered up.

The ISL45022 is controlled by a serial SPI interface that allows setting tap register values as well as storing data in the nonvolatile memory.

Potentiometer and Rheostat Modes

The ISL45022 can operate as either a rheostat or as a potentiometer (voltage divider). When in the potentiometer configuration there are two possible modes. One is without the output buffer and the other mode is with the output buffer. Selecting the mode is done by controlling bit D8 of the data register. D8 = 0 sets the output buffer off and D8 = 1 sets it on. Each channel can be independently set to either buffer On or Off.

Note that this bit can only be set by loading the value to the NVMEM with instructions #5 and then loading the TAP register with instruction #6 from NVMEM. This bit cannot be controlled by directly writing the value to the chip when the tap register is set.

RHEOSTAT CONFIGURATION

The ISL45022 acts as a two terminal resistive element in the rheostat configuration where one terminal is either one of the end point pins of the resistor (VA and VB) and the other terminal is the wiper (VW) pin. This configuration controls the resistance between the two terminals and the resistance can be adjusted by sending the corresponding tap register setting commands to the ISL45022 or loading a pre-set tap register value from nonvolatile memory NVMEM0 ~ MVMEM3.

POTENTIOMETER CONFIGURATION

In potentiometer configuration an input voltage is connected to one of the end point pins (VA or VB). The voltage on the wiper pin will be proportional to the voltage difference between VA and VB and the wiper setting. The resistance cannot be directly measured in this configuration.

Programming Modes

Two program modes are available for the ISL45022:

1. **Direct program mode**. The tap register setting can be changed either by loading a predetermined value from an external microcontroller or by using the UP/DOWN commands. The UP and DOWN commands change the tap register setting incrementally i.e., 1 LSB at a time. The UP and DOWN commands will not wrap around at the ends of the scale.

2. **NVMEM restore mode**. One of the previously stored settings can be loaded into the TR register from the non-volatile memory. Four 9-bit non-volatile memories, are available for each channel to store tap register settings. The first register, NVMEM0, stores the favorite or default tap register setting that will be loaded into the tap register at system power up or software power on reset operation.

Non-Volatile Memory (NVMEM)

Each channel has four NVMEM positions available for storing the output buffer operating mode and the potentiometer setting. These NVMEM positions can be directly written through the SPI using a write command (#5) with address and data bytes. Another command (#7) is available that stores the current output buffer operating mode and potentiometer settings into the selected NVMEM position. Bit A3 and A2 in the instruction byte decide which NVMEM position is used. (See Table 5).

All potentiometers are loaded with the value stored in the NVMEM position 0 for their respective channel on power up.

WRITE PROTECT OF NVMEM

Write-protect ($\overline{WP}$) disables any changes of current content in the NVMEM regardless of the commands, except that NVMEM setting can be retrieved using commands 4, 6 of Table 5. Therefore, Write-Protect ($\overline{WP}$) pin provides hardware NVMEM protection feature with $\overline{WP}$ tied to Vss. $\overline{WP}$, which is active at logic LOW, should be tied directly to V_{DD} if it is not being used.

Flow Control

Reading and writing to NVMEM requires an internal access cycle to complete before the next command can be sent. The following commands have additional flow control using the R/$\overline{B}$ pin.

- Read Tap Register (#2)
- Read NVMEM (#4)
- Program NVMEM (#5)
- Load Tap Register (#6)
- Program NVMEM with Tap Register (#7)

The R/$\overline{B}$ bit will be pulled HIGH when $\overline{CS}$ goes LOW, and will stay HIGH indicating the chip is ready to accept another command. After sending one of those commands, the R/$\overline{B}$ pin should be polled to determine when the device is ready to accept the additional data.

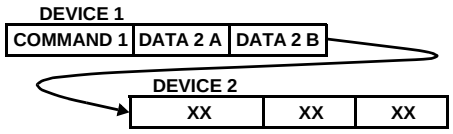
This flow control can be used on all commands without any performance penalty although it is only needed on the commands listed above.

Daisy Chain

Multiple devices can be controlled by the same bus without the need for extra $\overline{CS}$ lines from the microcontroller by daisy chaining the devices with the SDO of the first device connected to SDI of the next device as shown in Figure 3.

A complete command is 24 bits including the instruction and the two data bytes. When shifting 24 bits in to the first device in the chain, the 24 bits of the previous command will be shifted out. So to set up two devices in a daisy chain, a total of 48 bits must be sent where the first 24 bits will be shifted out to the second device and the 24 bits shifted in last will remain in the first device.

1. Command and data for device 2 is shifted into device 1, this will propagate to Device 2 when the next 24 bits are shifted in.



2. Command and data for device 1 is shifted into device 1. Now Device 1 and 2 are correctly set up.

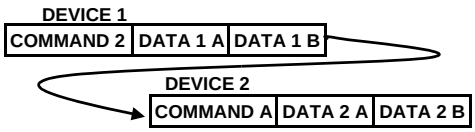


FIGURE 2. DAISY CHAIN COMMAND EXAMPLE

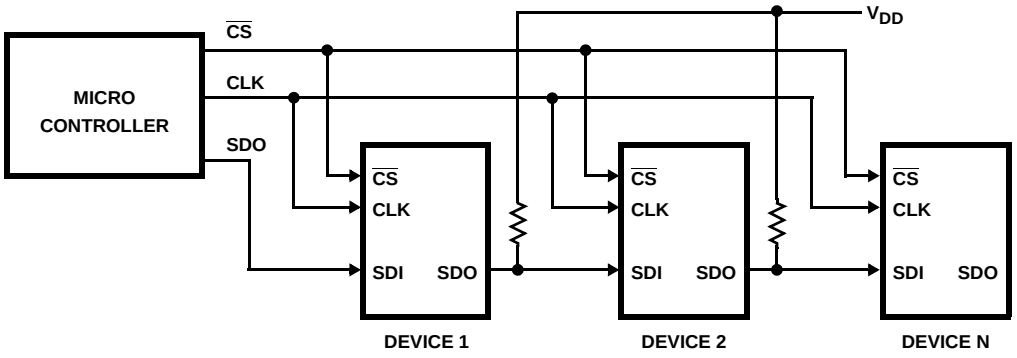


FIGURE 3. DAISY CHAIN CONFIGURATION

Serial Data Interface

The ISL45022 contains a four-wire SPI interface:

- **SDO** (Serial Data Output) Used for reading out the internal register contents and for daisy chaining multiple devices.
- **SDI** (Serial Data Input) Used for clocking in commands and potentiometer settings.
- **CS** (Chip Select) This pin must be pulled LOW before starting to send a command and pulled HIGH to signal the end of the command. This pin can be used to control multiple devices on the bus.
- **CLK** (Clock) The SDI bits are shifted in on the rising edge of the clock and SDO data is shifted out on the falling edge of the clock.

The key features of this interface include:

- Independently programmable Read & Write to all registers
- Direct parallel refresh of all Tap registers from corresponding internal NVMEM registers
- Increment and decrement instruction for each Tap register
- Nonvolatile storage of the present Tap register values into one of the four NVMEM registers available to each channel
- Configurable output buffer amplifier to allow both the functions of a potentiometer and a variable resistor
- Four 9-bit non-volatile registers store four preset wiper positions and the first one will be recalled to set the wiper position during power up.

The serial interface uses an SPI compatible uniform 24-bit word format as shown in Table 3. This format is used for all members of the WMS720x family. The data is sent MSB first.

C3-C0 are the command bits that control the operation of the digital potentiometer according to the command instructions shown in the Instruction Set in Table 5 in the Instruction Set section.

A1 and A0 are the address bits that determine which channel is activated, as shown in the table below. For the ISL45022 only the first two codes are used.

TABLE 1. A1 AND A0 ADDRESS BIT DECODE TABLE

[A1 A0]	[0 0]	[0 1]	[1 0]	[1 1]
Channel	0	1	2	3

A3 and A2 are the address bits that decide which NVMEM memory to be accessed, as shown in the table below.

TABLE 2. A3 AND A2 ADDRESS BIT DECODE TABLE

[A3 A2]	[0 0]	[0 1]	[1 0]	[1 1]
NVMEM	0	1	2	3

D7-D0 are the data values to be loaded into the Tap Register to set the wiper position, while D8 is used to set the output mode. D8 has to be loaded into the NVMEM0~3 first and then the "**Load Tap Register**" command (#6) has be executed to load D8 into the output-selection MUX to set the output mode. D8 = 0 sets the output to Buffer Off mode while D8 = 1 sets to Buffer On mode.

TABLE 3. 24-BIT DATA WORD FORMAT

MSB																							**LSB**
C3	C2	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	X	D8	D7	D6	D5	D4	D3	D2	D1	D0

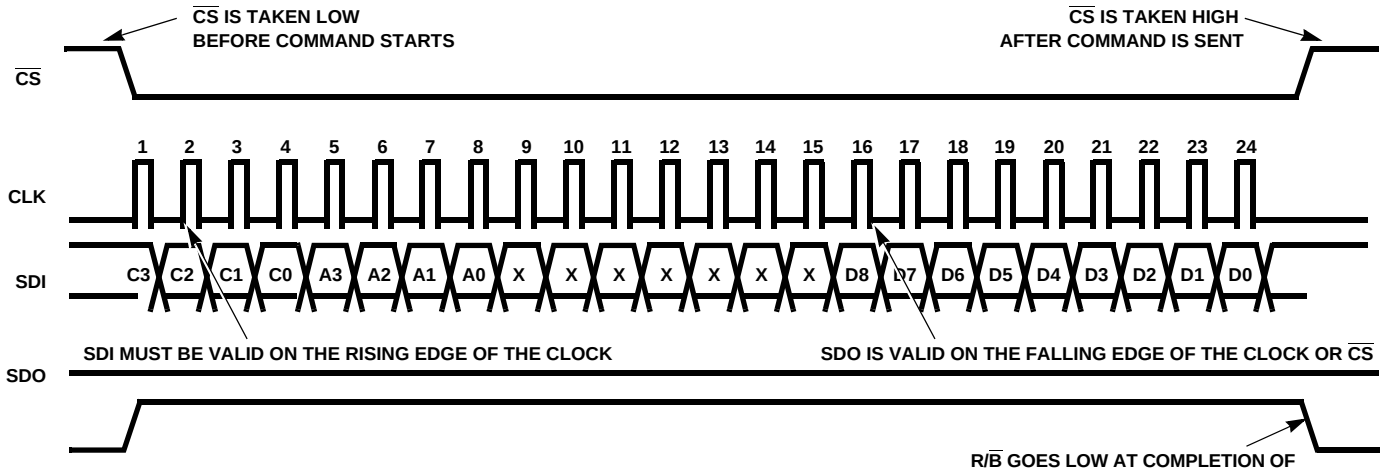


FIGURE 4. SPI COMMAND WAVEFORMS

NOTES:

4. A multiple of 24 bits must always be sent or the command will not be valid.
5. Bits marked "x" are don't care bits.

Instruction Set

TABLE 4. INSTRUCTION SET

INST NO.	INSTRUCTION BYTE C3 C2 C1 C0 A3 A2 A1 A0	DATA BYTE 1 D15 D14 D13 D12 D11 D10 D9 D8	DATA BYTE 2 D7 D6 D5 D4 D3 D2 D1 D0	OPERATION
1	0 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	**No Operation** (NOP). Do nothing
2	1 1 0 0 x x A1 A0	x x x x x x x x	x x x x x x x x	**Read Tap Register** and output selection MUX register
3	0 1 0 0 x x A1 A0	x x x x x x x x	D7 D6 D5 D4 D3 D2 D1 D0	**Write to Tap Register** with D7-D0
4	1 0 1 0 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	**Read NVMEM** pointed to by A3-A0
5	0 0 1 0 A3 A2 A1 A0	x x x x x x x D8	D7 D6 D5 D4 D3 D2 D1 D0	**Program NVMEM** pointed to by A3-A0 with D8-D0
6	1 0 1 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	**Load Tap Register** and output selection MUX register with the contents of NVMEM pointed to by A3-A0
7	0 0 1 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	**Program NVMEM** pointed to by A3-A0 with the contents of Tap Register and output selection MUX register
8	0 1 1 1 x x A1 A0	x x x x x x x x	x x x x x x x x	**Up**: Increment setting of TR by one tap
9	1 1 1 1 x x A1 A0	x x x x x x x x	x x x x x x x x	**Down**: Decrement setting of TR by one tap
10	1 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	**Sleep**: Discontinue clock supply to the logic and memories
11	0 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	**Wake Up**: Clock supply to the logic and memories
12	1 1 0 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	**Byte-erase NVMEM** pointed to by A3-A0
13	1 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	**Power On Reset**: Software reset the part to the power up state

NOTE: C3-C0 are the command op-code; A3, A2 are the NVMEM address; A1, A0 are the channel address.

Basic Operation

This chapter describes the sequences of commands to send to the ISL45022 and how to use the different features.

SENDING A COMMAND

1. Take the chip out of SLEEP mode.
2. Check that the write protect is set correctly if writing to NVMEM.
3. Check that R/$\overline{B}$ is HIGH before issuing command.
4. Pull the $\overline{CS}$ pin LOW before sending data to the device.
5. 24 clock pulses are sent for each command. SDI must be valid on the rising edge of the clock, SDO is valid on the falling edge of the clock or $\overline{CS}$.
6. Take $\overline{CS}$ HIGH after the command has completed.
7. If command 2, 4, 5, 6 or 7 is sent, wait for the R/$\overline{B}$ pin to go HIGH before sending the next command.

WAKE UP/SLEEP/POWER COMMANDS

The chip is in SLEEP mode after:

- V_{DD} is applied
- A Power on Reset command is sent
- A SLEEP command is sent

Before any operations can be performed the WAKE UP command must be sent.

When a SLEEP command is sent, the chip retains its resistor settings as long as the chip is powered up but cannot accept any other commands than a WAKE UP command.

TABLE 5. POWER RELATED COMMANDS

INST. NO.	COMMAND NAME	COMMAND BYTE	DATA BYTE 1	DATA BYTE 2	COMMENT
11	Wake Up	0 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	Wake Up entire chip
10	Sleep	1 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	Send chip into power save mode
13	Power on Reset	1 0 0 1 x x x x	x x x x x x x x	x x x x x x x x	Reset Chip
1	NOP	0 0 0 0 x x x x	x x x x x x x x	x x x x x x x x	Dummy instruction

The commands above control the entire chip. There is no way to independently power on or off individual potentiometers.

WRITE TO TAP REGISTER (TR)

The microcontroller can write a value directly into the tap register or send an increment or decrement command to control the tap register. Alternatively, the contents of an NVMEM location can be written to the tap register. The only way to change the output buffer mode is to write the desired value of bit D8 into an NVMEM location and then load the corresponding NVMEM location into the tap register.

TABLE 6. WRITING TO THE TAP REGISTERS

INST. NO.	COMMAND NAME	COMMAND BYTE	DATA BYTE 1	DATA BYTE 2	COMMENT
3	Write to Tap Register	0 1 0 0 x x A1 A0	x x x x x x x x	D7 D6 D5 D4 D3 D2 D1 D0	Writes a value to the tap register of the selected channel
8	Up	0 1 1 1 x x A1 A0	x x x x x x x x	x x x x x x x x	Increment tap register value by one
9	Down	1 1 1 1 x x A1 A0	x x x x x x x x	x x x x x x x x	Decrement tap register value by one
6	Load Tap Register	1 0 1 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	Load the selected NVMEM location into the tap register

PROGRAMMING NON-VOLATILE MEMORY (NVMEM)

The value stored in the NVMEM location is 9 bits, the 8 bits (D7-D0) of the tap register plus 1 bit (D8) of the output buffer mode. The NVMEM position must be erased before writing to it. There are two ways to program a value into NVMEM.

Write a value directly from the microcontroller

Load the current potentiometer setting into NVMEM.

TABLE 7. PROGRAMMING NVMEM

INST. NO	COMMAND NAME	COMMAND BYTE	DATA BYTE 1	DATA BYTE 2	COMMENT
12	Erase NVMEM	1 1 0 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	Erases the 9 bit word pointed to by A3, A2, A1 and A0.
5	Program NVMEM	0 0 1 0 A3 A2 A1 A0	x x x x x x x D8	D7 D6 D5 D4 D3 D2 D1 D0	Writes a value to the selected NVMEM register of the selected channel
7	Program NVMEM with Tap Register	0 0 1 1 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	Takes the current potentiometer settings and saves in the selected NVMEM location.

For programming NVMEM, the following sequence must be followed:

1. Erase word at NVMEM location
2. Program word at NVMEM location

READING TAP REGISTERS AND NVMEM LOCATIONS

The contents of the tap register for any channel or any NVMEM location can be read back through the SDO pin. When a command is sent, the data is clocked out on the falling edge of the clock. Since daisy-chain operation requires data from one command to be clocked out when the next command arrives, any read command must be followed by another command to get the correct data on the SDO pin.

TABLE 8. READING THE TAP REGISTERS

INST. NO.	COMMAND NAME:	COMMAND BYTE	DATA BYTE 1	DATA BYTE 2	COMMENT
4	Read NVMEM	1 0 1 0 A3 A2 A1 A0	x x x x x x x x	x x x x x x x x	Read the value of the selected NVMEM location
2	Read Tap Register	1 1 0 0 x x A1 A0	x x x x x x x x	x x x x x x x x	Read the value of the selected tap register
1	NOP to Read Register	0 0 0 0 x x x x	x x x x x x x D8	D7 D6 D5 D4 D3 D2 D1 D0	Output data to SDO pin

To read the contents of either the tap register or a NVMEM location, the following sequence must be followed.

1. Send the desired read command (#2 or #4) to select the register to read
2. Send another command such as NOP and read the SDO pin on the falling edge of the clock. The other command could be any command, but to make sure that the chip does not change anything, send either another Read command or a NOP command (#1).

Timing Diagrams

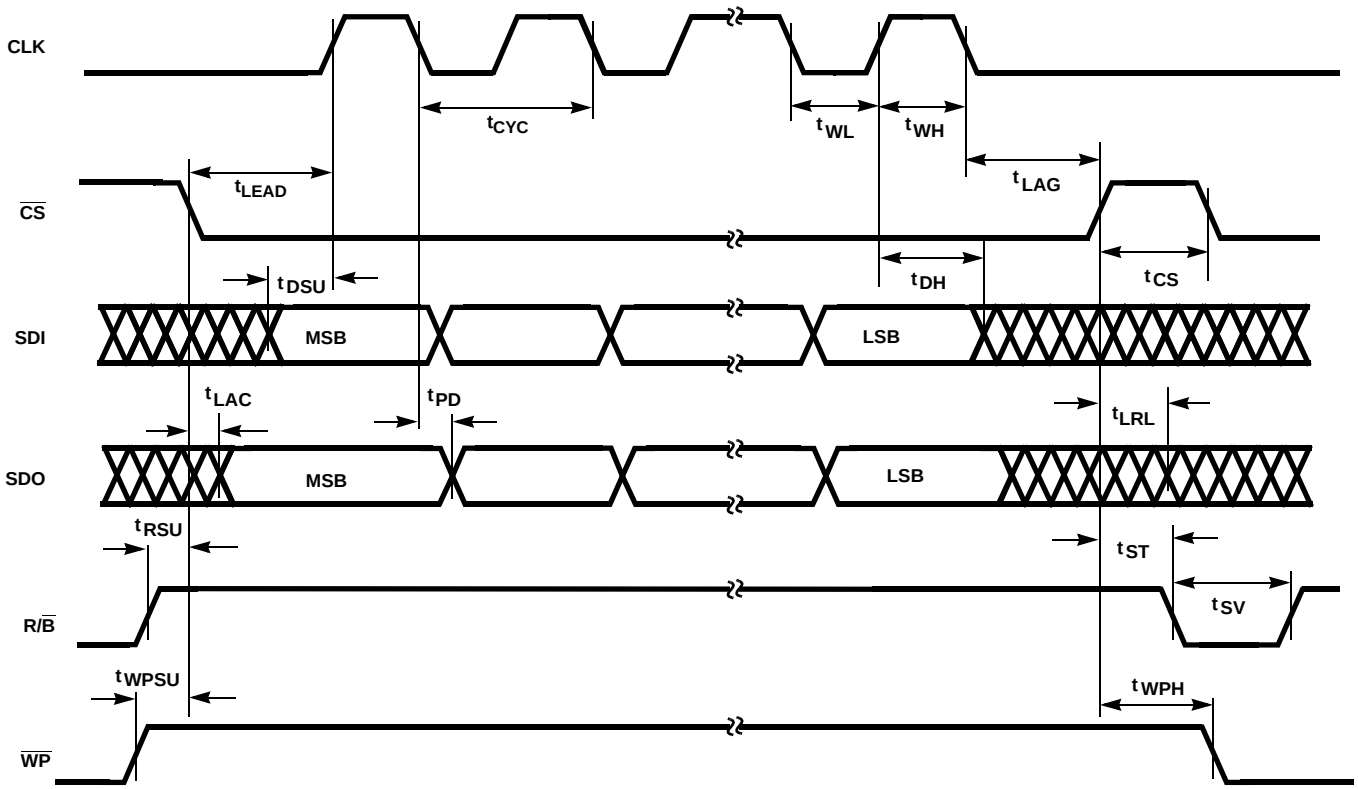


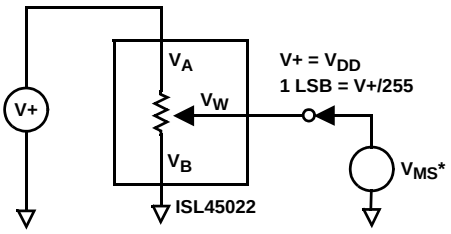
FIGURE 5. ISL45022 TIMING DIAGRAM

TABLE 9. TIMING PARAMETERS

PARAMETER	SYMBOL	MIN	MAX	UNIT
SPI Clock Cycle Time	t_{CYC}	100		ns
SPI Clock HIGH Time	t_{WH}	50		ns
SPI Clock LOW Time	t_{WL}	50		ns
Lead Time	t_{LEAD}	100		ns
Lag Time	t_{LAG}	100		ns
SDI Setup Time	t_{DSU}	20		ns
SDI Hold Time	t_{DH}	20		ns
$\overline{CS}$ to SDO – SPI Line Acquire	t_{LAC}	5		ns
$\overline{CS}$ to SDO – SPI Line Release	t_{LRL}	5		ns
CLK to SDO Propagation Delay	t_{PD}	1		ns
R/B Rise to $\overline{CS}$ Fall	t_{RSU}	500		ns
Store to NVMEM Save Time	t_{SV}		2	ms
$\overline{CS}$ Deselect Time	t_{CS}	600		ns
Startup Time	t_{ST}	0.1		ms
$\overline{WP}$ Setup Time	t_{WPSU}	10		ns
$\overline{WP}$ Hold Time	t_{WPH}	10		ns

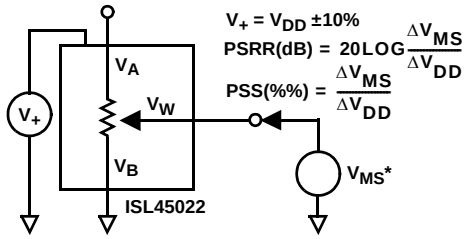
NOTE: The interface timing characteristics apply to all parts but are guaranteed by design and not subject to production test.

Test Circuits



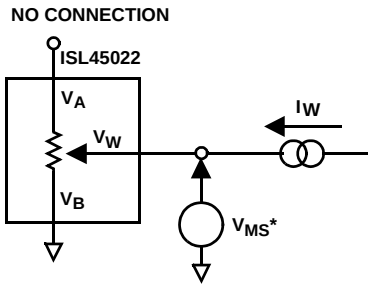
*Assume infinite input impedance

FIGURE 6. POTENTIOMETER DIVIDER NONLINEARITY ERROR TEST CIRCUIT (INL, DNL)



*Assume infinite input impedance

FIGURE 7. POWER SUPPLY SENSITIVITY TEST CIRCUIT (PSS, PSRR)



*Assume infinite input impedance

FIGURE 8. RESISTOR POSITION NONLINEARITY ERROR TEST CIRCUIT (RHEOSTAT OPERATION: R-INL, R-DNL)

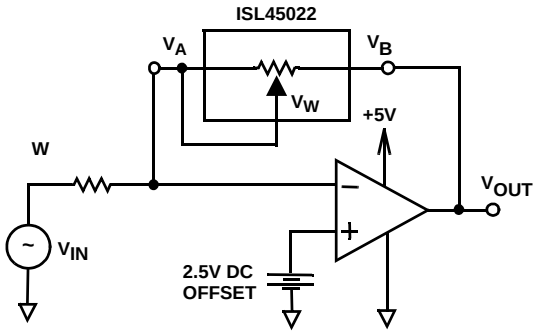
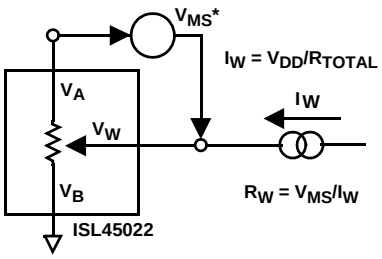


FIGURE 9. CAPACITANCE TEST CIRCUIT



*Assume infinite input impedance

FIGURE 10. WIPER RESISTANCE TEST CIRCUIT

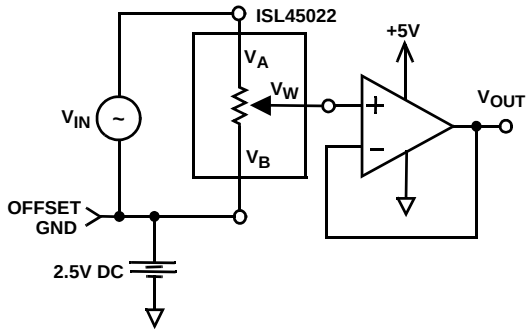
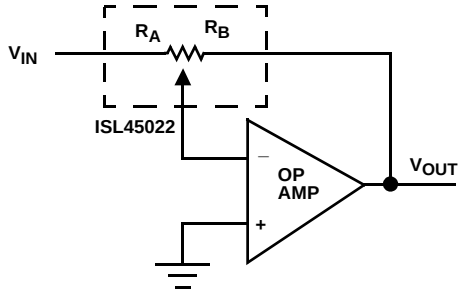


FIGURE 11. GAIN vs FREQUENCY TEST CIRCUIT

Typical Application Circuits

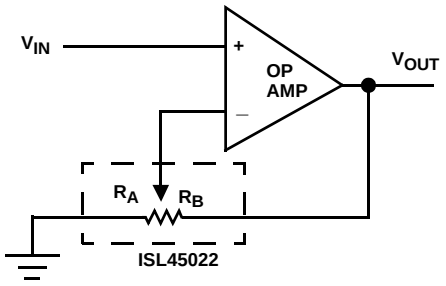


$$V_{OUT} = -V_{IN}f\frac{R_B}{R_A}$$

$$R_A = \frac{R_{AB}(256-D)}{256},\ R_B = \frac{R_{AB} \bullet D}{256}$$

R_{AB} = Total resistance of potentiometer.
W = Wiper setting for ISL45022

FIGURE 12. PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE ISL45022



$$V_{OUT} = V_{IN}\left(1 + \frac{R_B}{R_A}\right)$$

$$R_A = \frac{R_{AB}(256-D)}{256},\ R_B = \frac{R_{AB} \bullet D}{256}$$

R_{AB} = Total resistance of potentiometer.
W = Wiper setting for ISL45022

FIGURE 13. PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE ISL45022

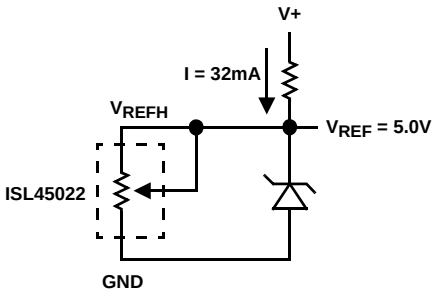


FIGURE 14. ISL45022 TRIMMING VOLTAGE REFERENCE

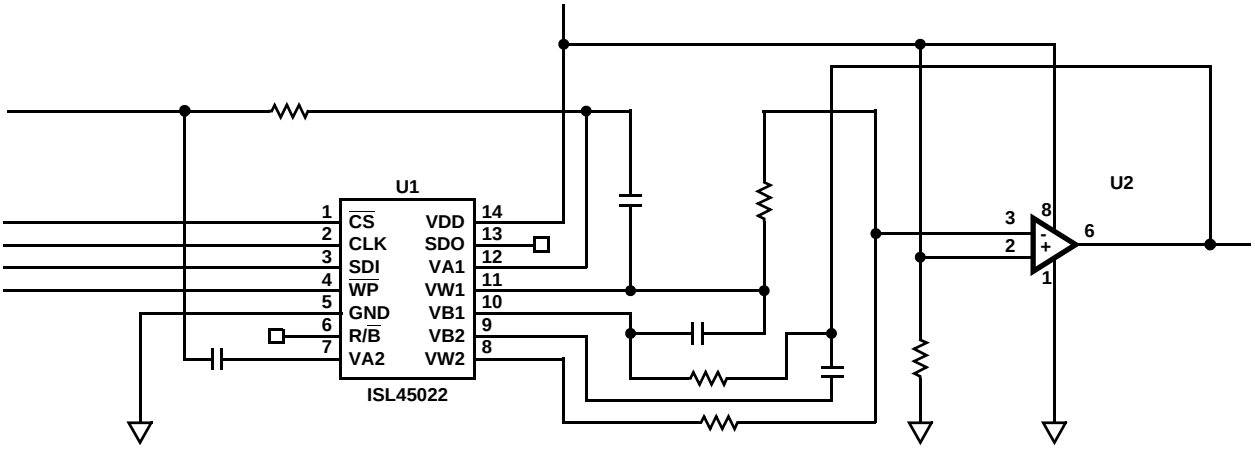


FIGURE 15. ISL45022 AUDIO TONE CONTROL

Typical Application Circuits (Continued)

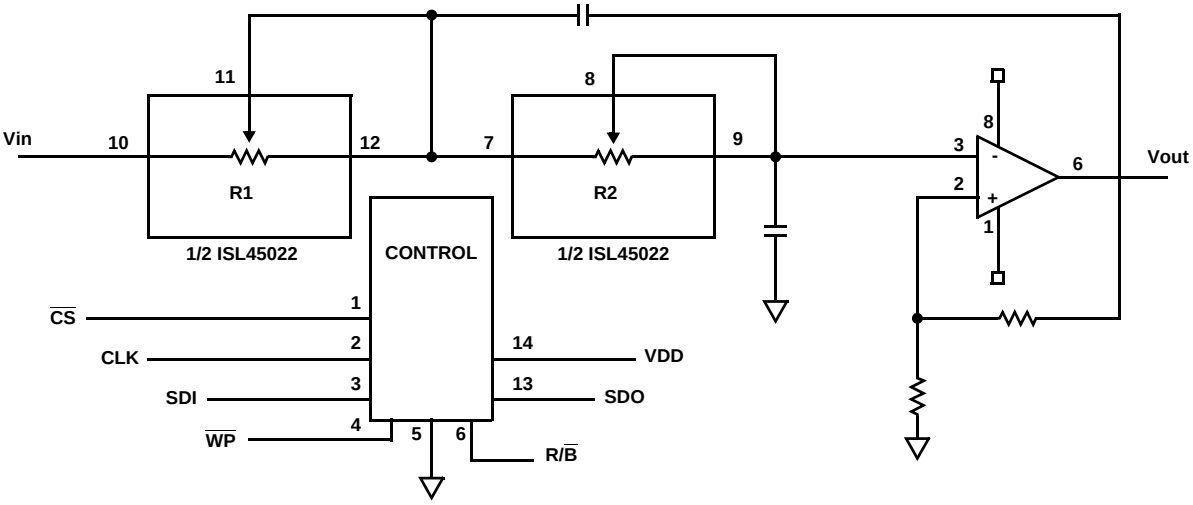


FIGURE 16. PROGRAMMABLE LOW-PASS FILTER

Layout Considerations

A 0.1µF bypass capacitor as close as possible to the V_{DD} pin is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the V_{DD} and V_{SS} pins. Care should be taken to separate the analog and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.

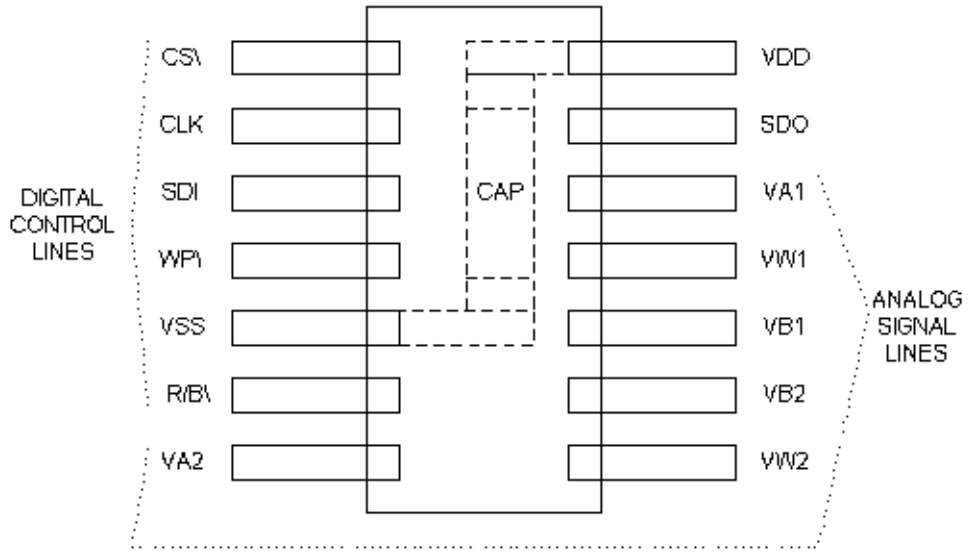
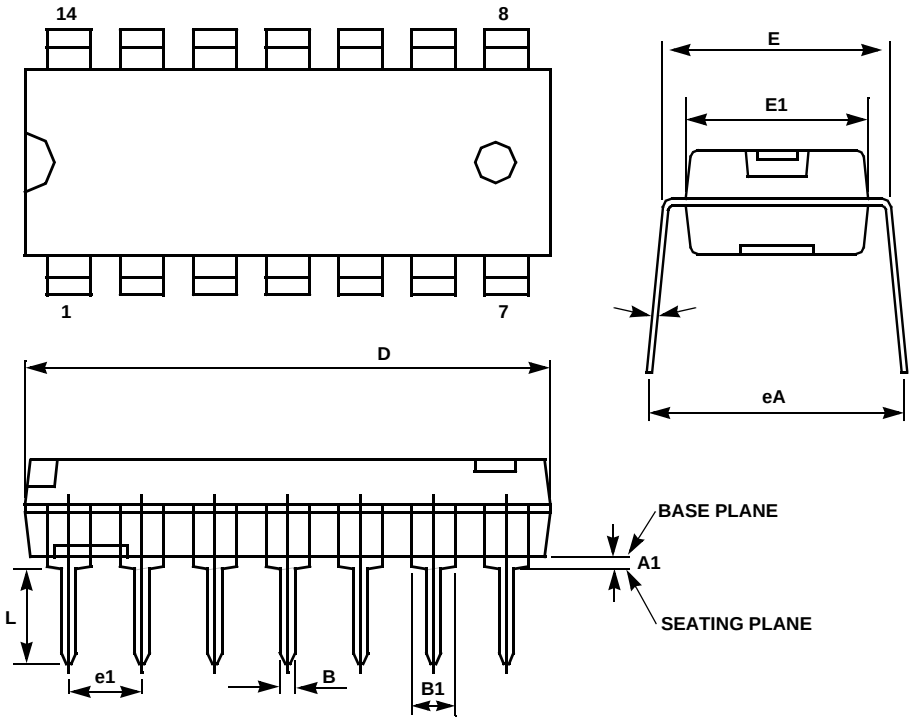


FIGURE 17. ISL45022 LAYOUT

Dual-In-Line Plastic Packages (PDIP)

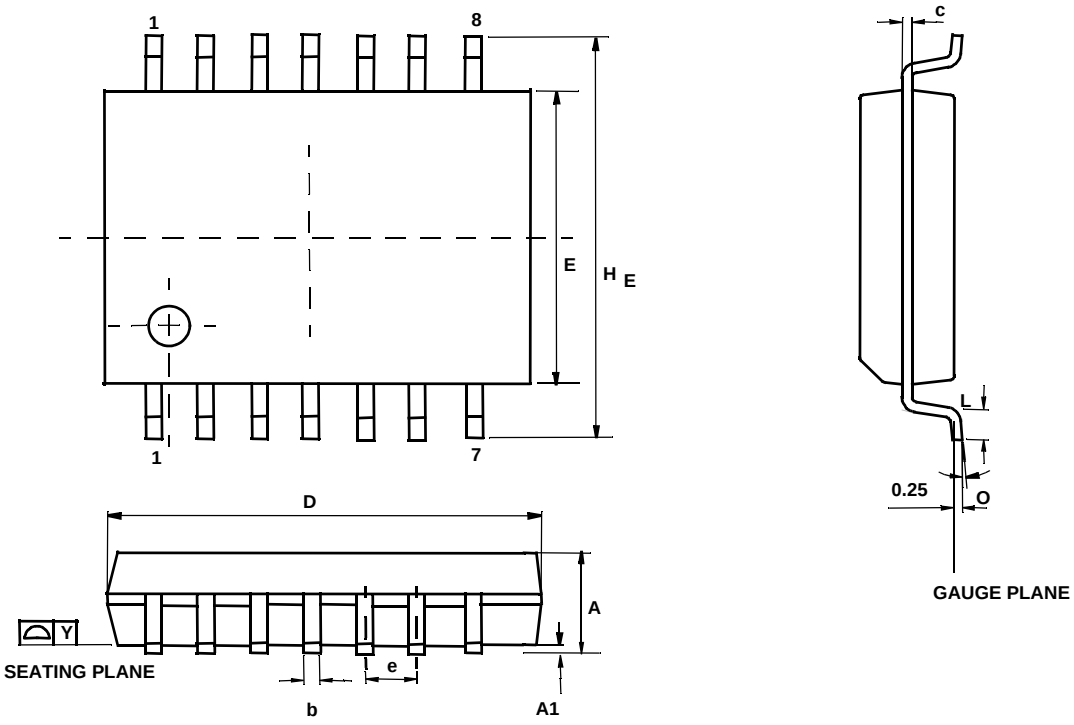
14 Lead 300MIL PDIP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A1	0.381			0.015		
B	0.406	0.457	0.508	0.016	0.018	0.020
B1	1.397	1.524	1.651	0.055	0.060	0.065
c		0.25			0.010	
D	18.80	19.05	19.30	0.740	0.750	0.760
E	7.62	7.925	8.230	0.300	0.312	0.324
E1	6.25	6.35	6.45	0.246	0.250	0.254
e1	2.54 BSC			0.1 BSC		
L	2.2921			0.115		
eA	8.382	8.89	9.398	0.330	0.350	0.370

Small Outline Plastic Packages (SOIC)

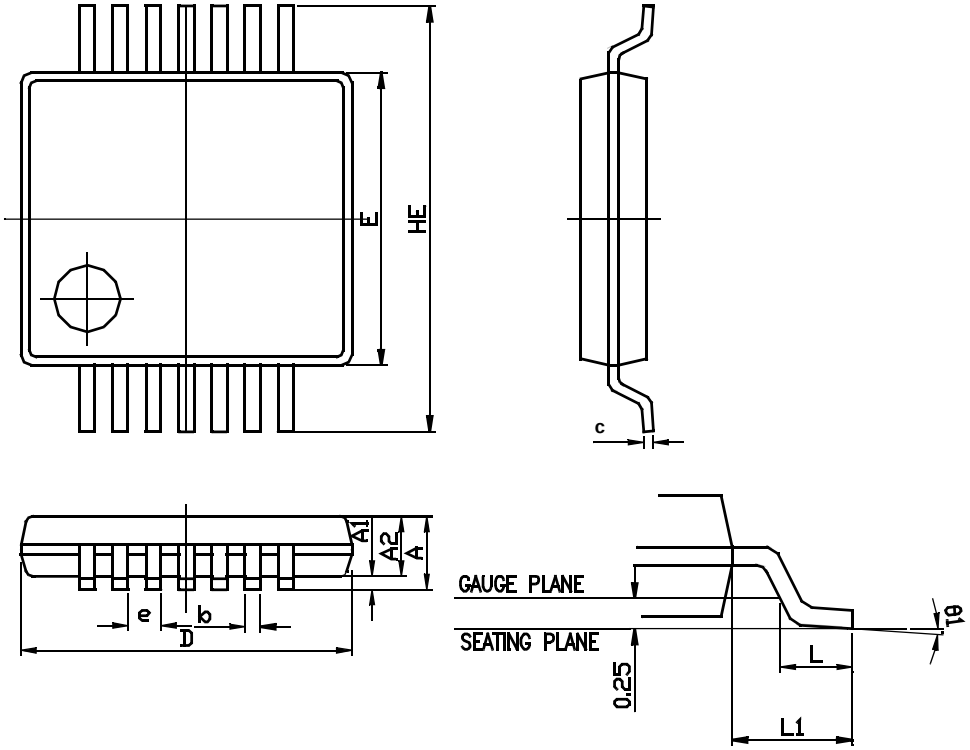
14 Lead 150MIL SOIC



SYMBOL	DIMENSION (MM)		DIMENSION (INCH)	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC.		0.050 BSC.	
H_E	5.80	6.20	0.228	0.244
Y		0.10		0.004
L	0.40	1.27	0.016	0.050
0	0	8	0	8

Thin Shrink Small Outline Plastic Packages (TSSOP)

14 Lead 4.4MM TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM	MAX	MIN	NOM	MAX
A			1.20			0.043
A1	0.05		0.15	0.002		0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.50	0.60	0.75	0.020	0.024	0.030
HE	6.40 BSC			0.252 BSC		
E	4.30	4.40	4.50	0.169	0.173	0.177
D	4.90	5.00	5.10	0.193	0.197	0.201
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
L1	1.0 REF			0.039 REF		
e	0.65 BSC			0.026 BSC		
θ1	0		8	0		8