

500MHz Rail-to-Rail Amplifiers

The 5962-0623501QPC, 5962-0623502QPC are fully DSCC SMD compliant parts and the SMD data sheets are available on the DSCC website

(<http://www.dscclia.mil/programs/specfind/default.asp>).

The 5962-0623501QPC is electrically equivalent to the EL8102 and the 5962-0623502QPC is electrically equivalent to the EL8103, reference these data sheets for additional information. These parts are single rail-to-rail amplifiers with a -3dB bandwidth of 500MHz and slew rate of 600V/μs. Running off a very low 11mA supply current, the 5962-0623501QPC, 5962-0623502QPC also feature inputs that go to 0.15V below the V_{S-} rail.

The 5962-0623501QPC includes a fast-acting disable/power-down circuit. With a 25ns disable and a 200ns enable, the 5962-0623501QPC is ideal for multiplexing applications.

The 5962-0623501QPC, 5962-0623502QPC are designed for a number of general purpose video, communication, instrumentation, and industrial applications. Both parts are available in 8 Ld SBDIP. All are specified for operation over the -55°C to +125°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962-0623501QPC	5962-0623501QPC	-55 to +125	8 Ld SBDIP	D8.3
5962-0623502QPC	5962-0623502QPC	-55 to +125	8 Ld SBDIP	D8.3

Features

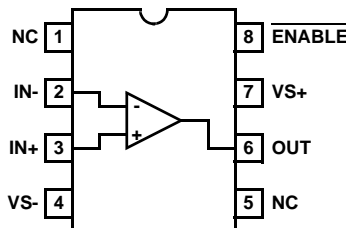
- 500MHz -3dB bandwidth
- 600V/μs slew rate
- Low supply current = 11mA
- Supplies from 3V to 5.0V
- Rail-to-rail output
- Input to 0.15V below V_{S-}
- Fast 25ns disable (5962-0623501QPC only)

Applications

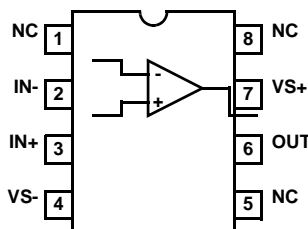
- Video amplifiers
- Portable/hand-held products
- Communications devices

Pinouts

5962-0623501QPC
(8 LD SBDIP)
TOP VIEW



5962-0623502QPC
(8 LD SBDIP)
TOP VIEW



Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

Supply Voltage from V_{S+} to V_{S-} 5.5V
 Input Voltage $V_{S+} + 0.3\text{V}$ to $V_{S-} - 0.3\text{V}$
 Differential Input Voltage2V
 Continuous Output Current 20mA

Thermal Information

Power Dissipation 60.5mW
 Storage Temperature -65°C to $+150^\circ\text{C}$
 Ambient Operating Temperature -55°C to $+125^\circ\text{C}$
 Operating Junction Temperature $+150^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

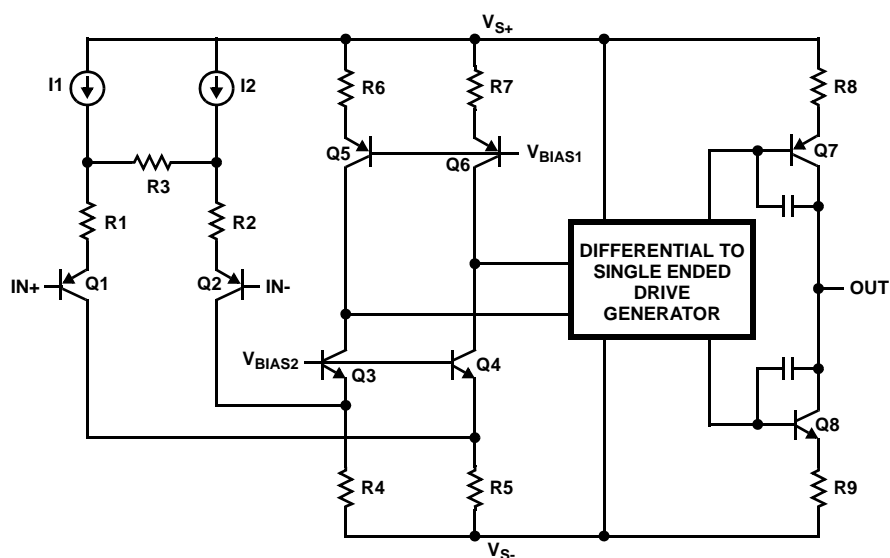
Electrical Specifications $V_{S+} = 5\text{V}$, $V_{S-} = \text{GND}$, $T_A = +25^\circ\text{C}$, $V_{CM} = 2.5\text{V}$, $R_L = 2.5\text{k}\Omega$, $A_V = 1$, Unless Otherwise Specified

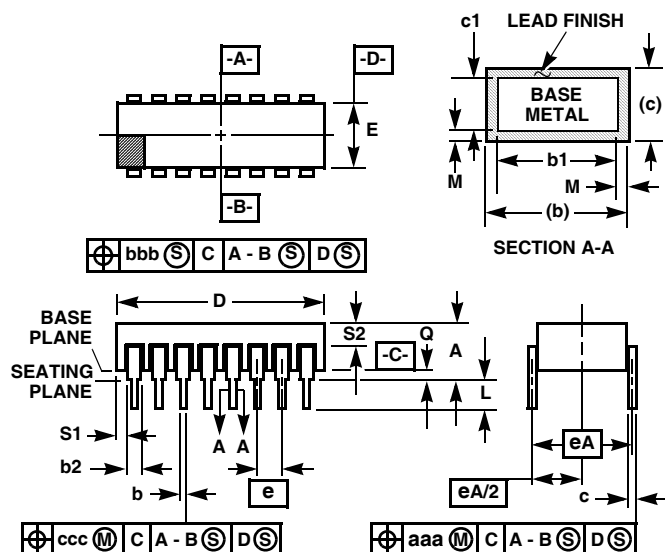
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
R_{IN}	Input Resistance	Common Mode		3.5		$\text{M}\Omega$
C_{IN}	Input Capacitance			0.5		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	$A_V = +1$		30		m Ω
ENABLE (5962-0623501QPC ONLY)						
t_{EN}	Enable Time			200		ns
t_{DS}	Disable Time			25		ns
AC PERFORMANCE						
BW	-3dB Bandwidth	$A_V = +1$, $R_F = 0\Omega$, $C_L = 5\text{pF}$		500		MHz
		$A_V = -1$, $R_F = 1\text{k}\Omega$, $C_L = 5\text{pF}$		140		MHz
		$A_V = +2$, $R_F = 1\text{k}\Omega$, $C_L = 5\text{pF}$		165		MHz
		$A_V = +10$, $R_F = 1\text{k}\Omega$, $C_L = 5\text{pF}$		18		MHz
BW	$\pm 0.1\text{dB}$ Bandwidth	$A_V = +1$, $R_F = 0\Omega$, $C_L = 5\text{pF}$		35		MHz
Peak	Peaking	$A_V = +1$, $R_L = 1\text{k}\Omega$, $C_L = 5\text{pF}$		1		dB
GBWP	Gain Bandwidth Product			200		MHz
PM	Phase Margin	$R_L = 1\text{k}\Omega$, $C_L = 5\text{pF}$		55		$^\circ$
SR	Slew Rate	$A_V = 2$, $R_L = 100\Omega$, $V_{OUT} = 0.5\text{V}$ to 4.5V		600		V/ μs
t_R	Rise Time	$2.5V_{STEP}$, 20% to 80%		4		ns
t_F	Fall Time	$2.5V_{STEP}$, 20% to 80%		2		ns
OS	Overshoot	200mV step		10		%
t_{PD}	Propagation Delay	200mV step		1		ns
t_S	0.1% Settling Time	200mV step		15		ns
dG	Differential Gain	$A_V = +2$, $R_F = 1\text{k}\Omega$, $R_L = 150\Omega$		0.01		%
dP	Differential Phase	$A_V = +2$, $R_F = 1\text{k}\Omega$, $R_L = 150\Omega$		0.01		$^\circ$
e_N	Input Noise Voltage	$f = 10\text{kHz}$		12		nV/ $\sqrt{\text{Hz}}$
i_{N+}	Positive Input Noise Current	$f = 10\text{kHz}$		1.7		pA/ $\sqrt{\text{Hz}}$
i_{N-}	Negative Input Noise Current	$f = 10\text{kHz}$		1.3		pA/ $\sqrt{\text{Hz}}$

Pin Descriptions

PART		PIN NAME	FUNCTION
5962-0623501QPC	5962-0623502QPC		
1, 5	1, 5, 8	NC	Not connected
2	2	IN-	Inverting input
3	3	IN+	Non-inverting input
4	4	VS-	Negative power supply
6	6	OUT	Amplifier output
7	7	VS+	Positive power supply
8		ENABLE	Enable and disable input

Simplified Schematic Diagram



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

**D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Rev. 0 4/94

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com