March 2003 FN4645.3

Triple 8-Bit, 80MSPS A/D Converter with Internal Voltage Reference

The HI5630 is a monolithic, triple 8-bit, 80MSPS analog-to-digital converter fabricated in an advanced CMOS process. It is designed for digitizing RGB graphics from work stations and personal computers. The HI5630 reaches a new level of multi-channel integration. The fully pipeline architecture and an innovative input stage enable the HI5630 to accept a variety of single-ended or fully differential input configurations which present valid data to the output bus with a latency of 5 clock cycles. Only one external clock is necessary to drive all three converters with a clock out signal provided. An internal band-gap voltage reference is also provided allowing the system designer to realize an increased level of system integration resulting in decreased cost and power dissipation.

The HI5630 can be bench tested using a complete ADC evaluation board with clock drivers, ADC, latches and a reconstruct DAC. In addition, complete LCD monitor reference designs are available for immediate volume production (contact factory).

Part Number Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5630/8CN	0 to 70	64 Ld MQFP	Q64.14x14
HI5630EVAL1	25	ADC Evaluation Platform	

Features

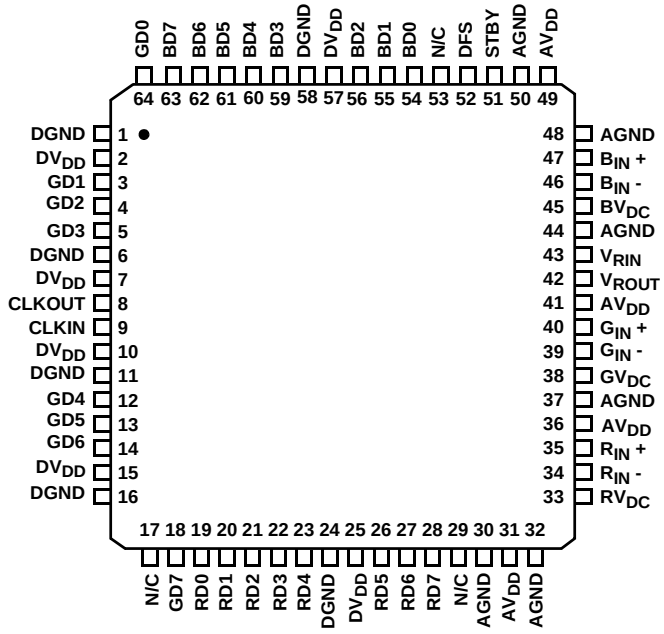
- Triple 8-Bit A/D Converter on a Monolithic Chip
- Sampling Rate 80MSPS
- ENOB (f_{IN} = 1MHz) 7.6
- Wide Full Power Input Bandwidth 300MHz
- Internal Band-Gap Voltage Reference 2.5V
- Excellent Channel-to-Channel Isolation . . . . . >75dB
- Single Supply Voltage Operation . . . . . +5V
- On-Chip Sample and Hold Amplifiers
- Clock Output
- Offset Binary or Two's Complement Output Format
- Stand-By Low Power mode

Applications

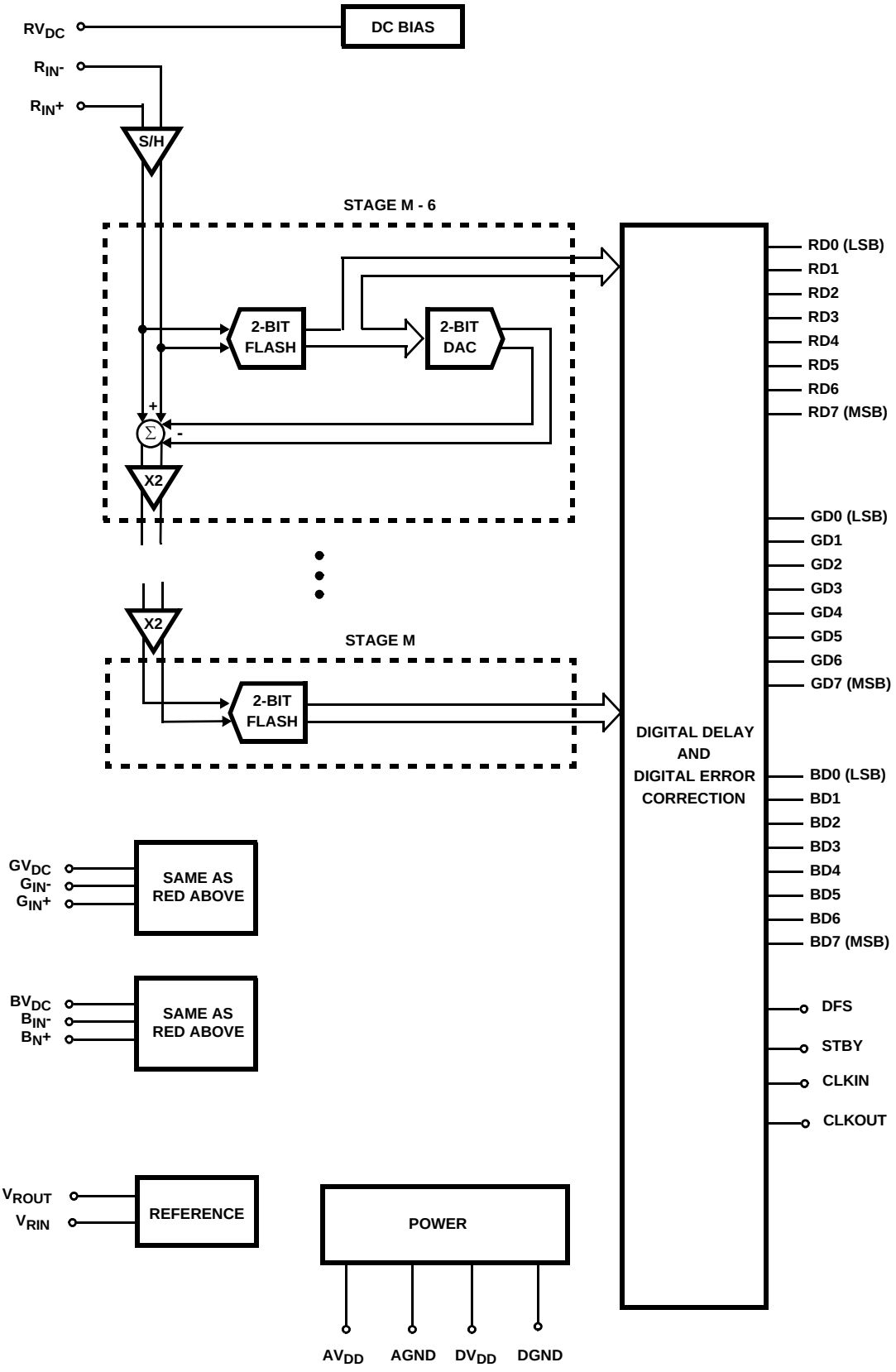
- LCD Monitors, Projectors and Plasma Display Panels
- Video Digitizing (RGB, Composite or Y-C)
- Medical Imaging
- High Speed Multi-Channel Data Acquisition

Pinout

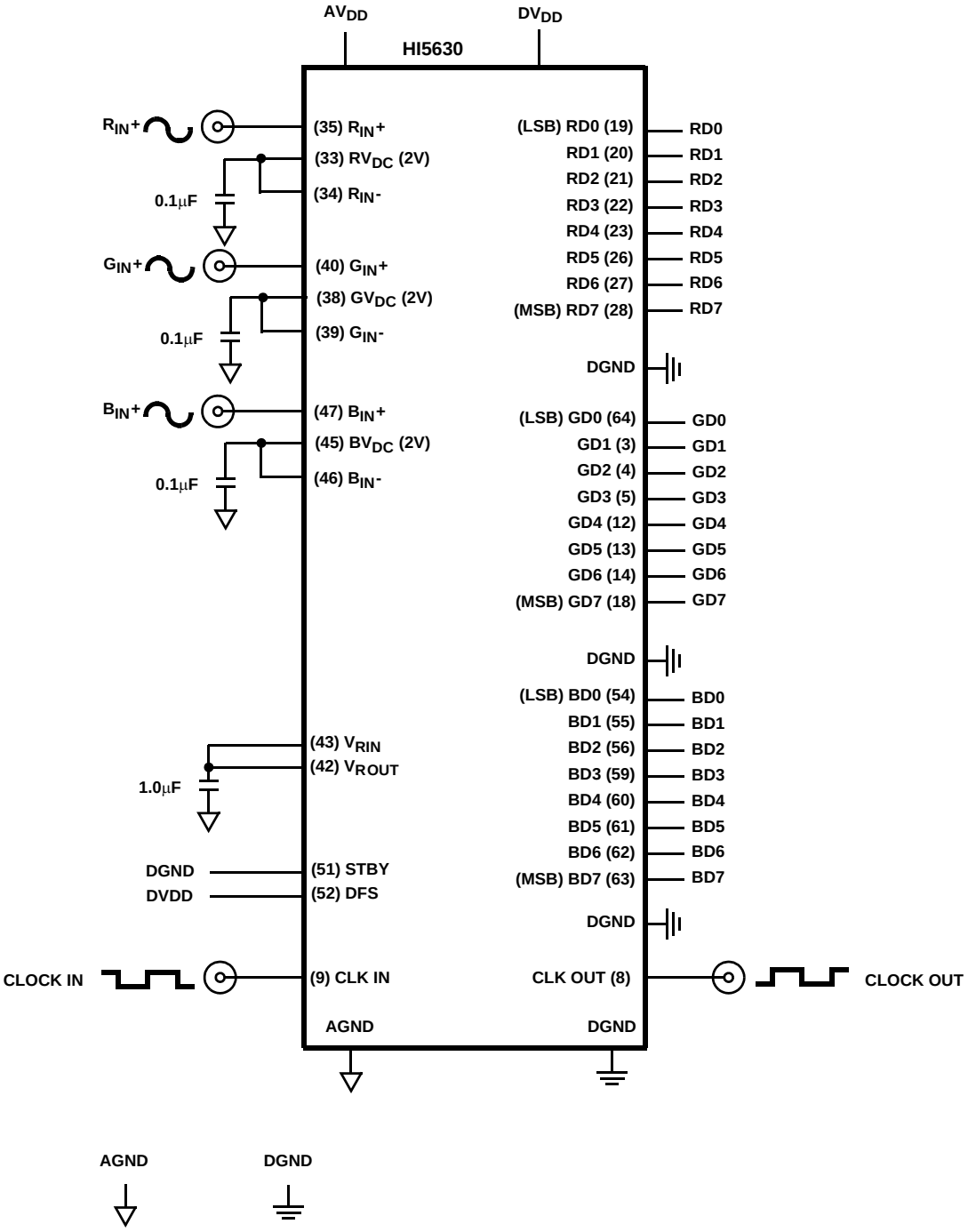
HI5630
(MQFP)
TOP VIEW



Functional Block Diagram



Typical Video Application Schematic



Pin Description

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DV_{DD}	Digital Supply (5.0V)
3	GD1	Green Data Bit 1 Output
4	GD2	Green Data Bit 2 Output
5	GD3	Green Data Bit 3 Output
6	DGND	Digital Ground
7	DV_{DD}	Digital Supply (5.0V)
8	CLK OUT	Sample Clock Output
9	CLK IN	Sample Clock Input
10	DV_{DD}	Digital Supply (5.0V)
11	DGND	Digital Ground
12	GD4	Green Data Bit 4 Output
13	GD5	Green Data Bit 5 Output
14	GD6	Green Data Bit 6 Output
15	DV_{DD}	Digital Supply (5.0V)
16	DGND	Digital Ground
17	NC	No Connection
18	GD7	Green Data Bit 7 Output
19	RD0	Red Data Bit 0 Output
20	RD1	Red Data Bit 1 Output
21	RD2	Red Data Bit 2 Output
22	RD3	Red Data Bit 3 Output
23	RD4	Red Data Bit 4 Output
24	DGND	Digital Ground
25	DV_{DD}	Digital Supply (5.0V)
26	RD5	Red Data Bit 5 Output
27	RD6	Red Data Bit 6 Output
28	RD7	Red Data Bit 7 Output
29	NC	No Connection
30	AGND	Analog Ground
31	AV_{DD}	Analog Supply (5.0V)
32	AGND	Analog Ground

Pin Description (Continued)

PIN NO.	NAME	DESCRIPTION
33	RV_{DC}	Red DC Bias Voltage Output (2.0)
34	R_{IN}-	Red Negative Analog Input
35	R_{IN}+	Red Positive Analog Input
36	AV_{DD}	Analog Supply (5.0V)
37	AGND	Analog Ground
38	GV_{DC}	Green DC Bias Voltage Output
39	G_{IN}-	Green Negative Analog Input
40	G_{IN}+	Green Positive Analog Input
41	AV_{DD}	Analog Supply (5.0V)
42	V_{ROUT}	+2.5V Reference Voltage Output
43	V_{RIN}	+2.5V Reference Voltage Input
44	AGND	Analog Ground
45	BV_{DC}	Blue DC Bias Voltage Output
46	B_{IN}-	Blue Negative Analog Input
47	B_{IN}+	Blue Positive Analog Input
48	AGND	Analog Ground
49	AV_{DD}	Analog Supply (5.0V)
50	AGND	Analog Ground
51	STBY	Stand-By Power Mode
52	DFS	Data Format Select Input
53	NC	No Connection
54	BD0	Blue Data Bit 0 Output
55	BD1	Blue Data Bit 1 Output
56	BD2	Blue Data Bit 2 Output
57	DV_{DD}	Digital Supply (5.0V)
58	DGND	Digital Ground
59	BD3	Blue Data Bit 3 Output
60	BD4	Blue Data Bit 4 Output
61	BD5	Blue Data Bit 5 Output
62	BD6	Blue Data Bit 6 Output
63	BD7	Blue Data Bit 7 Output
64	GD0	Green Data Bit 0 Output

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{DD} or DV_{DD} to AGND or DGND 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{DD}
Analog I/O Pins . . . . . AGND to AV_{DD}

Operating Conditions

Temperature Range
HI5630/8CN . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP	55

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a 1S2P (1 Signal and 2 Power) evaluation PC board in free air.

Electrical Specifications

AV_{DD} = 5V, DV_{DD} = 5V; Single Ended Inputs, V_{RIN} = 2.5V; f_S = 80MSPS at 50% Duty Cycle; C_L = 10pF; $T_A = 25^oC$; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		-	8	-	Bits
Integral Linearity Error, INL	f_{IN} = 1MHz	-	±0.4	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = 1MHz	-	±0.2	±1.0	LSB
Channel Offset Match	f_{IN} = DC	-	1	-	LSB
Channel Full Scale Error Match	f_{IN} = DC	-	0.25	-	LSB
Offset Code, V_{OC}	$V_{IN}+ = V_{IN}-$	-	140	-	CODE
Full Scale Error, FSE	f_{IN} = DC	-	1	-	LSB
Bit Error Rate (BER)		-	-	-	s
ANALOG INPUT					
Analog Input Range	(Note 2)	-	0.95	1	V
Analog Input Resistance	$V_{IN}+ = V_{IN}- = V_{REF}$	-	1	-	MΩ
Analog Input Capacitance		-	10	-	pF
Analog Input Bias Current	$V_{IN}+ = V_{IN}- = V_{REF}$	-10	1.0	10	µA
Full Power Input Bandwidth, FPBW		-	300	-	MHz
INTERNAL VOLTAGE REFERENCE 1µF Decoupling Cap Needed					
Reference Output Voltage, V_{REF}	I_{REF} = 4mA	2.33	2.5	2.67	V
Reference Output Current, I_{ROUT}	V Applied = 2.5V	-	2	4	mA
Reference Temperature Coefficient		-	6	-	$\mu V/^oC$
DC BIAS PINS RV_{DC}, GV_{DC}, BV_{DC} with 0.1µF Decoupling Cap Needed					
VDC Output Voltage (Loaded)		-	1.97	-	V
VDC Output Current, I_{VDC}		-	-	-	mA
VDC Temperature Coefficient		-	60	-	$\mu V/^oC$
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{RIN}	(Note 2)	2.2	2.5	2.8	V
Total Reference Resistance, R_{RIN}	V_{RIN} = 2.5V	-	2.93	-	kΩ
Reference Current, I_{RIN}	V_{RIN} = 2.5V	-	0.95	-	mA
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	1	-	-	MSPS
Maximum Conversion Rate	No Missing Codes	-	-	80	MSPS
Overclocking Conversion Rate	No Missing Codes	-	95	-	MSPS
Transient Response		-	1	-	Cycle

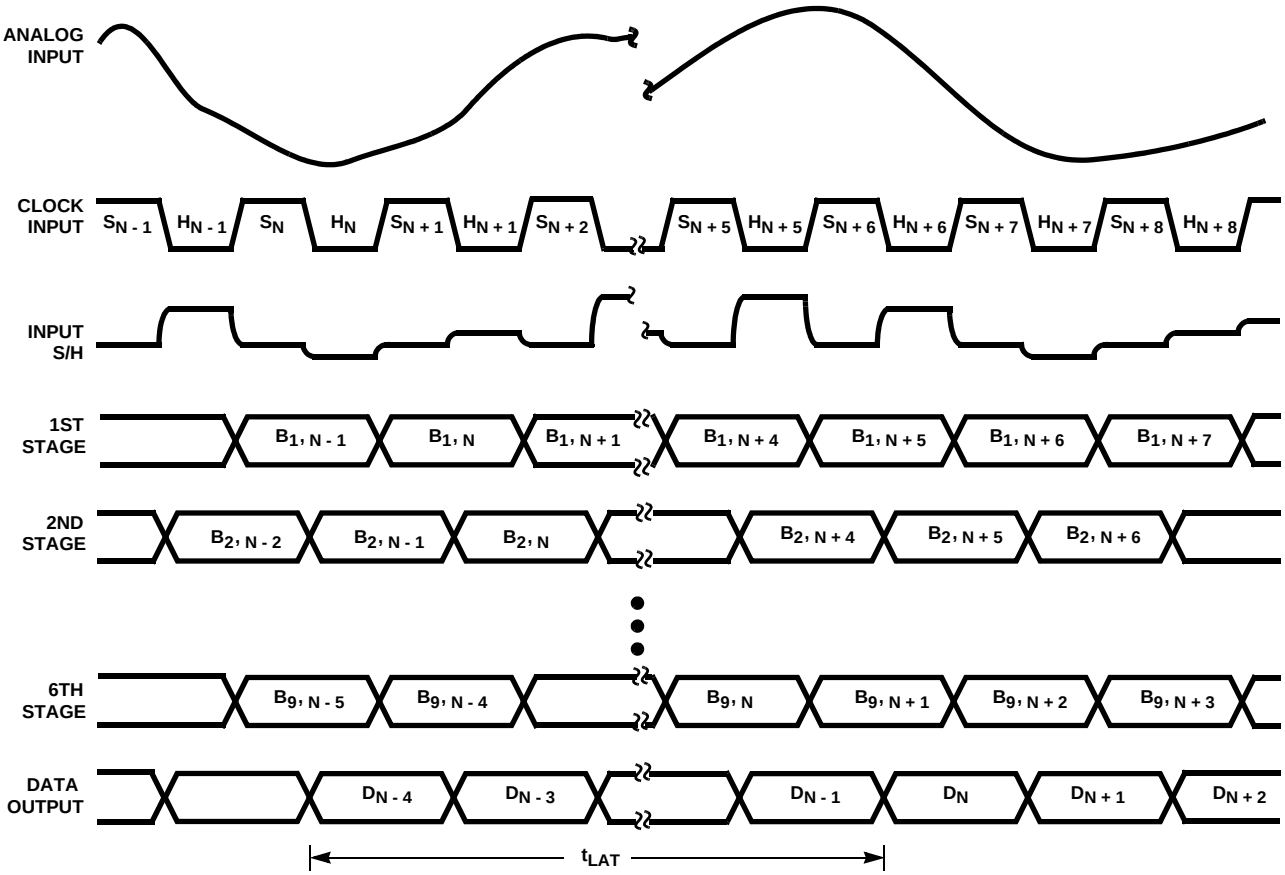
Electrical Specifications AV_{DD} = 5V, DV_{DD} = 5V; Single Ended Inputs, V_{RIN} = 2.5V; f_S = 80MSPS at 50% Duty Cycle; C_L = 10pF; T_A = 25°C; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Recovery	0.2V Overdrive	-	1	-	Cycle
Effective Number of Bits, ENOB	f_{IN} = 1MHz (Figure 11)	-	7.6	-	Bits
Signal to Noise and Distortion Ratio, SINAD	f_{IN} = 1MHz	-	47.8	-	dB
Signal to Noise Ratio, SNR	f_{IN} = 1MHz (Figure 12)	-	47.9	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	- 63	-	dB
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz (Figure 13)	-	- 64	-	dB
Channel Crosstalk		-	75	-	dB
SAMPLING CLOCK INPUT Note 3					
Input Logic High Voltage, V_{IH}	Figure 10	-	4	-	V
Input Logic Low Voltage, V_{IL}	Figure 10	-	0.4	-	V
Input Logic High Current, I_{IH}	V_{IH} = 4.5V	-10.0	-	+10.0	µA
Input Logic Low Current, I_{IL}	V_{IL} = 0V	-10.0	-	+10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
CLOCK OUTPUT C_L = 10pF (Note 3)					
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100µA	-	-	0.8	V
Output Capacitance, C_{COUT}		-	7	-	pF
DIGITAL OUTPUTS C_L = 10pF (Note 3)					
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; DV_{DD} = 5V	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100µA; DV_{DD} = 5V	-	-	0.8	V
Output Capacitance, C_{DOUT}		-	7	-	pF
TIMING CHARACTERISTICS					
Data Latency, t_{LAT}	For a Valid Sample	-	5	-	Cycles
Power-Up Initialization	Data Invalid Time	-	-	20	Cycles
Sample Clock Pulse Width (Low)		-	-	-	ns
Sample Clock Pulse Width (High)		-	-	-	ns
Sample Clock Duty Cycle Variation	Figure 9	-	±5	-	%
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{DD}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{DD}		4.75	5.0	5.25	V
Supply Current, I_{TOTAL}		-	348	-	mA
Analog Current, IAV_{DD}		-	235	265	mA
Digital5 Current, IDV_{DD}		-	113	-	mA
Power Dissipation		-	1.74	-	W
Standby Current		-	8	-	mA
Standby Power		-	40	-	mW
Offset Error PSRR, ΔV_{OS}	AV_{DD} or DV_{DD} = 5V ±5%	-	±0.4	-	LSB
Gain Error PSRR, ΔFSE	AV_{DD} or DV_{DD} = 5V ±5%	-	±0.15	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5630 INTERNAL CIRCUIT TIMING

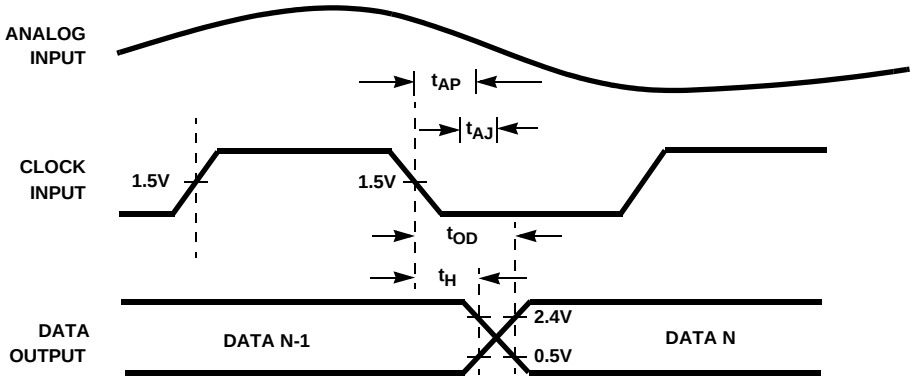


FIGURE 2. HI5630 INPUT-TO OUTPUT TIMING

Detailed Description

Theory of Operation

The HI5630 is a triple 8-Bit fully differential sampling pipeline A/D converter with digital error correction logic. Each of the three channels are identical so this discussion will only cover one channel. Figure 3 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

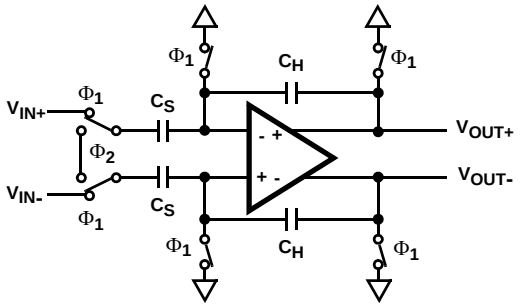


FIGURE 3. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram, identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the last stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the identical two-bit subconverter stages with the corresponding output of the last stage flash converter before applying the results to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 5th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The digital output data is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see Table 1, A/D Code Table).

Internal Reference Voltage Output, V_{ROUT}

The HI5630 is equipped with an internal reference voltage generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage. An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.5V reference voltage used by the converter. A 8:1 array of substrate PNPs generates the "delta-V_{BE}" and a two-stage op amp closes the loop to create an internal +1.25V band-gap reference voltage. This voltage is then amplified by a wide-band uncompensated operational amplifier connected in a gain-of-two configuration. An external, user-supplied, 1µF capacitor connected from the V_{ROUT} output pin to analog ground is used to set the dominant pole and to maintain the stability of the operational amplifier.

Reference Voltage Input, V_{RIN}

The HI5630 is designed to accept a +2.5V reference voltage source at the V_{REFIN} input pin. Typical operation of the converter requires V_{RIN} to be set at +2.5V. The HI5630 is tested with V_{RIN} connected to V_{ROUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external +2.5V reference voltage. As a result of the high input impedance presented at the V_{RIN} input pin, 3.0kΩ typically, the external reference voltage being used is only required to source 1mA of reference input current. In the situation where an external reference voltage will be used an external 1µF capacitor must be connected from the V_{ROUT} output pin to analog ground in order to maintain the stability of the internal operational amplifier.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

DC Voltage Source, V_{DC}

An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.0V DC voltage source to the user to help simplify circuit design. The characteristics of the DC source is equivalent to the internal reference.

Analog Input, Differential Connection

The analog input to the HI5630 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figures 4 and 5) will deliver the best performance from the converter.

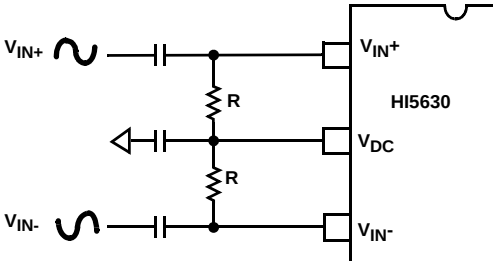


FIGURE 4. AC COUPLED DIFFERENTIAL INPUT

Since the HI5630 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 2.0V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC coupled differential input (Figure 4) and with V_{RIN} connected to V_{ROUT}, full scale is achieved when the V_{IN} and V_{IN}- input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the V_{IN}+ input is at V_{DC} + 0.25V and the V_{IN}- input is at V_{DC} - 0.25V (V_{IN}+ - V_{IN}- = +0.5V). Conversely, the converter will be at negative full scale when the V_{IN}+ input is equal to V_{DC} - 0.25V and V_{IN}- is equal to V_{DC} + 0.25V (V_{IN}+ - V_{IN}- = -0.5V).

The analog input can be DC coupled (Figure 5) as long as the inputs are within the analog input common mode voltage range ($0.25V \leq VDC \leq 4.75V$).

The resistors, R, in Figure 5 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

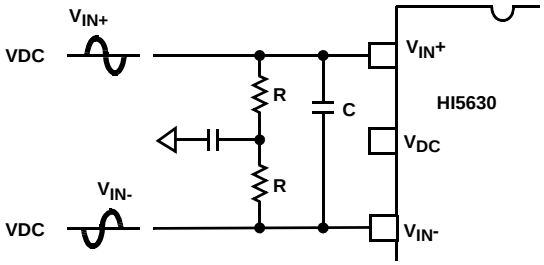


FIGURE 5. DC COUPLED DIFFERENTIAL INPUT

Analog Input, Single-Ended Connection

The configuration shown in Figure 6 may be used with a single ended AC coupled input.

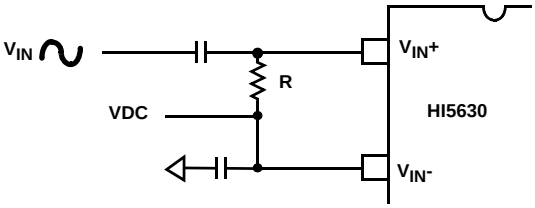


FIGURE 6. AC COUPLED SINGLE ENDED INPUT

Again, with V_{RIN} connected to V_{ROUT}, if V_{IN} is a $1V_{P-P}$ sinewave, then V_{IN}+ is a $1.0V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when V_{IN}+ is at VDC + 0.5V (V_{IN}+ - VIN- = +0.5V) and will be at negative full scale when V_{IN}+ is equal to VDC - 0.5V (V_{IN}+ - V_{IN}- = -0.5V). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, V_{DC}, output of the HI5630.

The single ended analog input can be DC coupled (Figure 1) as long as the input is within the analog input common mode voltage range.

The resistor, R, in Figure 7 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5630.

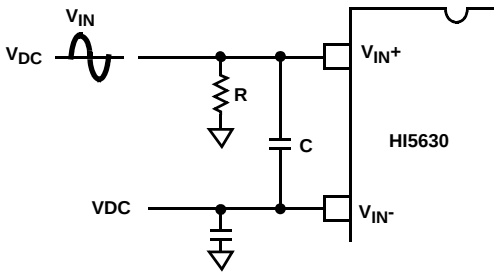


FIGURE 7. DC COUPLED SINGLE ENDED INPUT

Digital Output Control and Clock Requirements

The HI5630 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5630, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5630 will only be guaranteed at conversion rates above 1MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 1 for further information.

Supply and Ground Considerations

The HI5630 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5630 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply should be isolated with a ferrite bead from the digital supply.

Refer to the application note "Using Intersil High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS}) - The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE) - The last code transition should occur for an analog input that is $^3/_4$ LSB below Positive Full Scale (+FS) with the offset error removed. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL) - DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL) - INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity - Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE (V_{IN}+ - V_{IN}-)	OFFSET BINARY OUTPUT CODE (DFS LOW)								TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)							
		MSB							LSB	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^7/_{16}$ LSB	0.498291V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
+FS - $1^7/_{16}$ LSB	0.494385V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
+ $^9/_{16}$ LSB	2.19727mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- $^7/_{16}$ LSB	-1.70898V	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^9/_{16}$ LSB	-0.493896V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
-Full Scale (-FS) + $^9/_{16}$ LSB	-0.497803V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

NOTE:

8. The voltages listed above represent the ideal center of each output code shown with V_{RIN} = +2.5V.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5630. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is typically -0.5dB down from full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

The Effective Number of Bits (ENOB) is calculated from the SINAD data by:
ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,
where: V_{CORR} = 0.5dB (Typical).

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is backed off from full scale.

Signal To Noise and Distortion Ratio (SINAD) - SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR) - SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD) - THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion - This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR) - SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD) - Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), ($2f_1$), ($2f_2$), ($2f_1+f_2$), ($2f_1-f_2$), (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response - Transient response is measured by providing a full-scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 8-bit accuracy.

Over-Voltage Recovery - Over-Voltage Recovery is measured by providing a full-scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 8-bit accuracy.

Full Power Input Bandwidth (FPBW) - Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG) - Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP) - Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP}) - Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ}) - Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H) - Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD}) - Data output delay time is the time from the rising edge of the external sample clock to where the new data (N) is valid.

Data Latency (t_{LAT}) - After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 7 sample clock cycles.

Power-Up Initialization - This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

Typical Performance Curves

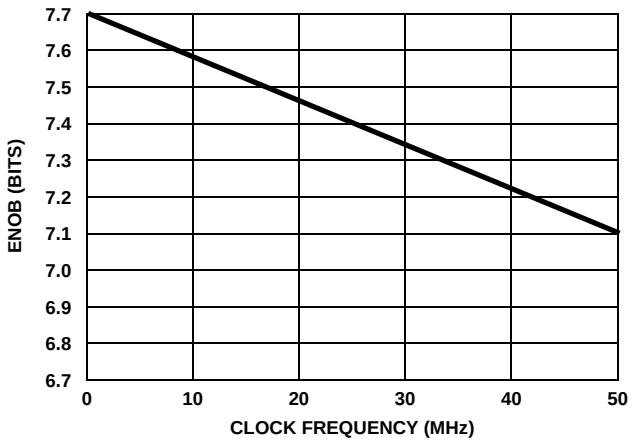


FIGURE 8. ENOB vs INPUT FREQUENCY (f_{CLK} = 80MHz)

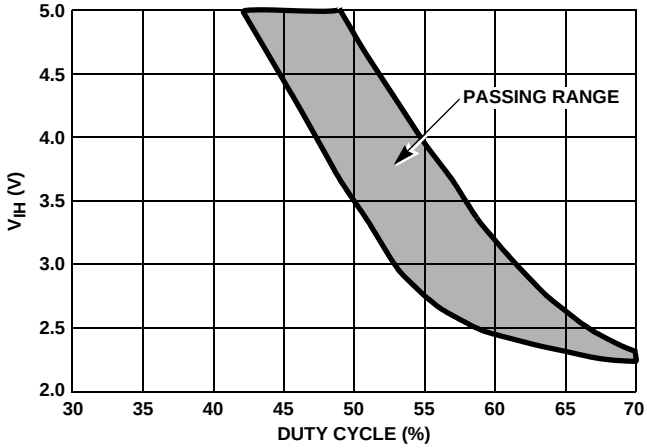


FIGURE 9. DUTY CYCLE vs V_{IH}

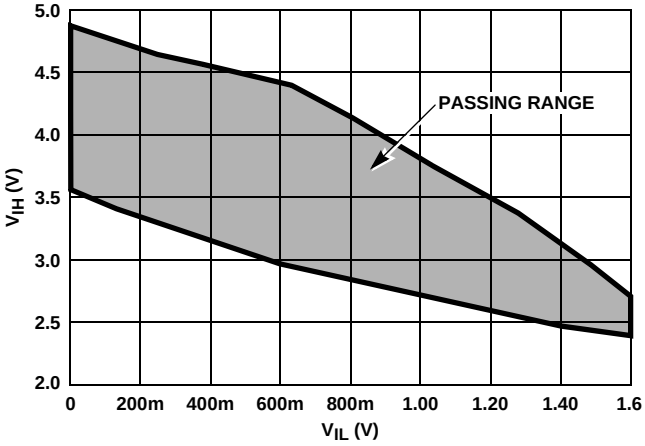


FIGURE 10. V_{IH} vs V_{IL}

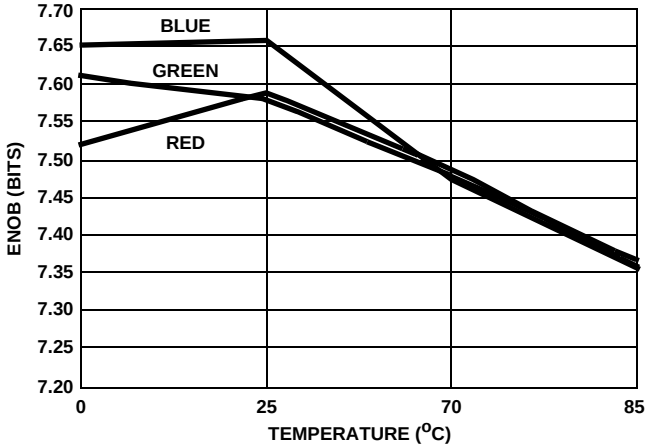


FIGURE 11. ENOB vs TEMPERATURE

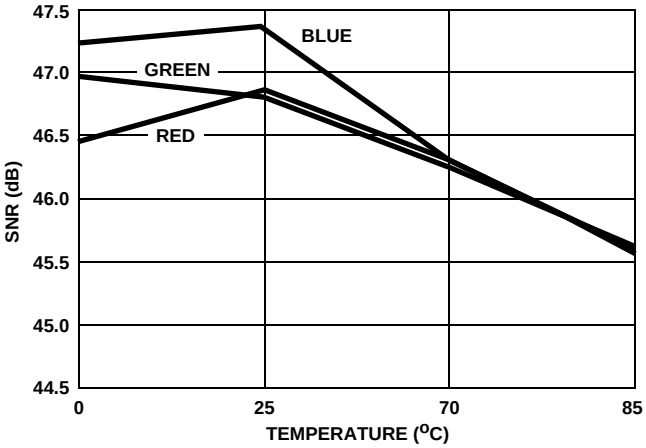


FIGURE 12. SNR vs TEMPERATURE

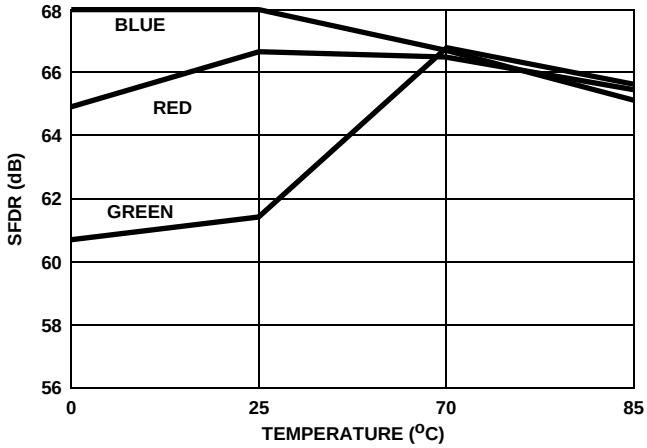


FIGURE 13. SFDR vs TEMPERATURE

Typical Performance Curves (Continued)

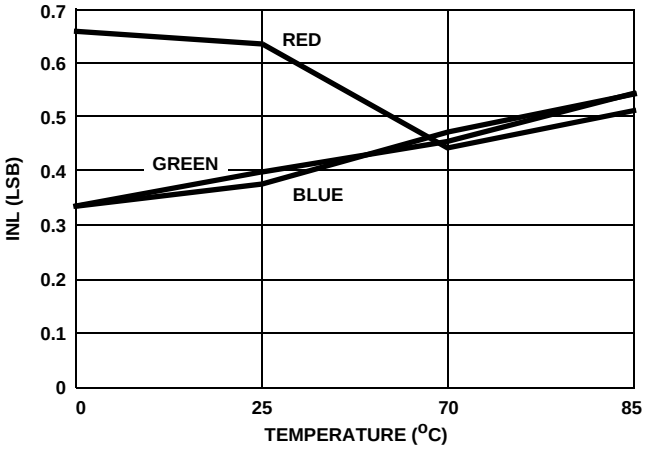


FIGURE 14. INL vs TEMPERATURE

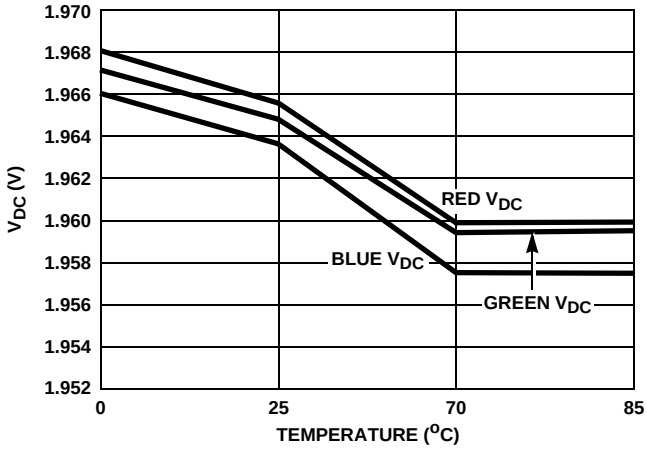


FIGURE 15. V_{DC} vs TEMPERATURE

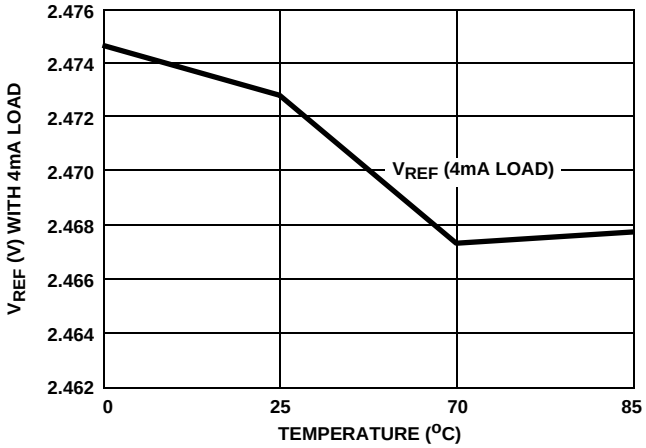


FIGURE 16. V_{REF} vs TEMPERATURE

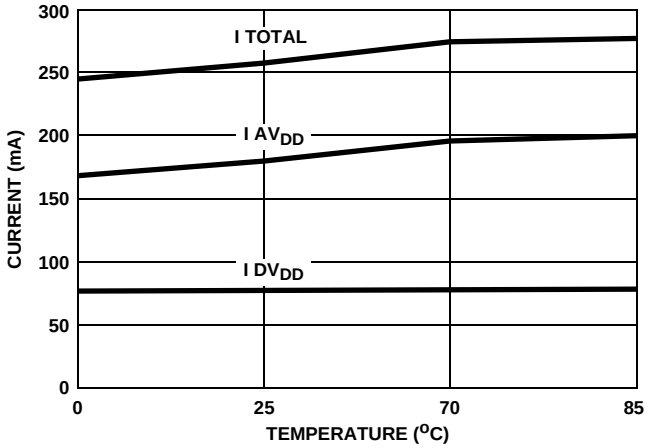


FIGURE 17. SUPPLY CURRENT (mA) vs TEMPERATURE