High Voltage TFT-LCD Logic Driver

The ISL24010 is a high voltage TFT-LCD logic driver with a +40V and -20V (momentary absolute max) output voltage swing capability. It is manufactured using the Intersil's proprietary monolithic high voltage bipolar process and is capable of driving a 3000pF load in 500ns.

The ISL24010 will level shift a digital input signal to an output voltage nearly equal to its output supply voltages. The ISL24010 has 3 supplies. V_{ON1} and V_{ON2} are positive supplies with a voltage range between +10V and +40V (absolute max). V_{OFF} is the negative supply with a voltage range between -5V and -20V (absolute max). Outputs 1 through 6 are connected to V_{ON1} and V_{OFF}. Outputs 7 and 8 are connected to V_{ON2} and V_{OFF}. This configuration enables outputs 1 through 6 to provide slicing to the row drivers to reduce flicker, and outputs 7 and 8 to control possible supply lines. V_{ON2} should remain constant. It is possible to tie V_{ON1} and V_{ON2} supplies together, if independent control as described above is not desired. V_{ON2} is required to be greater than or equal to V_{ON1} at all times.

The ISL24010 is available in TSSOP-20 pin package. It is specified for operation over the -40°C to +85°C industrial temperature range.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL24010IVZ (See Note)	24010IVZ	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ISL24010IVZ-T (See Note)	24010IVZ	-40 to +85	20 Ld TSSOP Tape and Reel (Pb-free)	M20.173

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
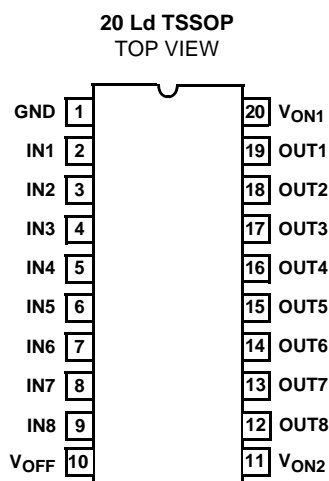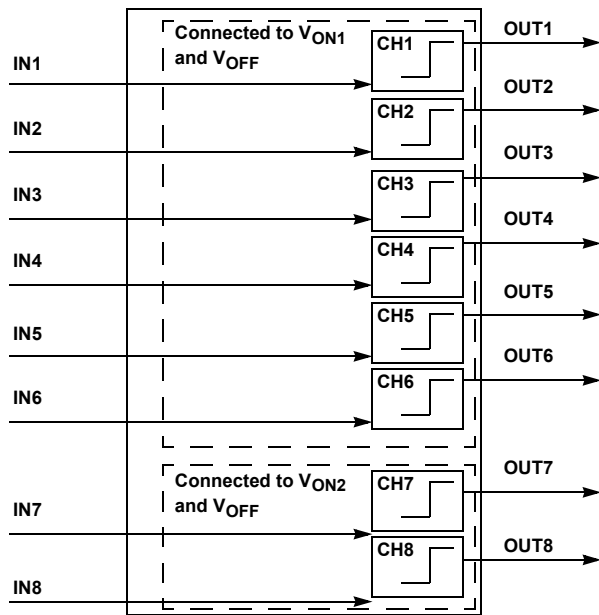
Features

• 0V to 5.5V (absolute max) Input Voltage Range

• +40V and -20V (momentary absolute max) Output Voltage Range

• 10mA Output Continuous Current (all 8 channels)

• 25mA Output Peak Current (all 8 channels)

• Rise/Fall Times 150ns/210ns

• Propagation Delay 250ns

• 50kHz Input Logic Frequency

• 20 Ld TSSOP Pb-Free Plus Anneal (RoHS Compliant)

Applications

• TFT-LCD panels

Pinout

20 Ld TSSOP
TOP VIEW

Pin	Name		Pin	Name
1	GND		20	V_{ON1}
2	IN1		19	OUT1
3	IN2		18	OUT2
4	IN3		17	OUT3
5	IN4		16	OUT4
6	IN5		15	OUT5
7	IN6		14	OUT6
8	IN7		13	OUT7
9	IN8		12	OUT8
10	V_{OFF}		11	V_{ON2}

Functional Diagram

ISL24010

Absolute Maximum Ratings (T$_A$ = 25°C)

Driver Positive Supply Voltage Range, (V$_{ON}$) . . . . +5V to +40V
Power Supply Voltage Range, (V$_{ON}$ to V$_{OFF}$) . . . . . . +10V to +60V
Negative Supply Voltage Range, (V$_{OFF}$). . . . . -20V to -5V
Supply Turn-on Slew Rate 10V/µs
Input Voltage Range, All Inputs . . . . -0.5V to 5.5V
Output Voltage Range, All Outputs . . . . . V$_{OFF}$ -0.5V to V$_{ON}$ +0.5V

Thermal Information

Thermal Resistance (Typical, Note 1)   θ$_{JA}$ (°C/W)
  20 Ld TSSOP Package   140
I$_{OUT}$ (continuous, all 8 channels) 80mA
T$_{AMBIENT}$ ·-40°C to +85°C
T$_{JUNCTION}$ ·-40°C to +150°C
T$_{STORAGE}$· ·-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ$_{JA}$ is measured with the component mounted on a HIGH effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T$_J$ = T$_C$ = T$_A$

Electrical Specifications   V$_{ON}$ = 22V, V$_{OFF}$ = -5V, T$_A$ = -40°C to +85°C Unless Otherwise Specified. Typical values tested at 25°C

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
Power Supplies	Recommended Operating Voltages		-5 (V$_{OFF}$)		22 (V$_{ON}$)	V
I(V$_{ON}$)	Supply Current	All Inputs low or high No load V$_{ON}$ = V$_{ON1}$ + V$_{ON2}$		1.8	4.0	mA
I(V$_{OFF}$)	Supply Current	All Inputs low or high No load	-4.0	-1.8		mA
I$_{IN}$	Input Leakage	Each Input low or high High = 1.8V, Low = 0.8V	-8.0	± 2.0	8.0	µA
VOH	High Level Output Voltage	IOH = -100µA V$_{ON}$ = 22V RL = 100pF in parallel with 5kΩ	(V$_{ON}$ - 1.5V)	21.2		V
VOL	Low Level Output Voltage	IOH = +100µA V$_{OFF}$ = -5V RL = 100pF in parallel with 5kΩ		-4.3	(V$_{OFF}$ + 1.5V)	V
VIH	High Level Input Voltage		1.8			V
VIL	Low Level Input Voltage				0.8	V
tplh	Low to High Prop Delay	50% to 50%, Tested with RL = 100pF in parallel with 5kΩ, f = 50kHz		300	500	ns
tphl	High to Low Prop Delay	Measured at 50% to 50% f = 50kHz RL = 100pF in parallel with 5kΩ,		250	500	ns
ttlh	Rise Time	Measured at 10% to 90% f = 50kHz RL = 100pF in parallel with 5kΩ		150	500	ns
tthl	Fall Time	Measured at 10% to 90% f = 50kHz RL = 100pF in parallel with 5kΩ		210	500	ns

Pin Descriptions

PIN NUMBER TSSOP-20	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	GND	4	Ground pin
2	IN1	1	Level shifter input 1
3	IN2	1	Level shifter input 2
4	IN3	1	Level shifter input 3
5	IN4	1	Level shifter input 4
6	IN5	1	Level shifter input 5
7	IN6	1	Level shifter input 6
8	IN7	1	Level shifter input 7
9	IN8	1	Level shifter input 8
10	VOFF	4	Negative output supply for all channels
11	VON2	4	Positive output supply for channels 7 and 8. V_{ON2} is required to be greater than or equal to V_{ON1}.
12	OUT8	3	Lever shifter output 8
13	OUT7	3	Lever shifter output 7
14	OUT6	2	Lever shifter output 6
15	OUT5	2	Lever shifter output 5
16	OUT4	2	Lever shifter output 4
17	OUT3	2	Lever shifter output 3
18	OUT2	2	Lever shifter output 2
19	OUT1	2	Lever shifter output 1
20	VON1	4	Positive output supply for channels 1 through 6. V_{ON1} is required to be less than or equal to V_{ON2}.
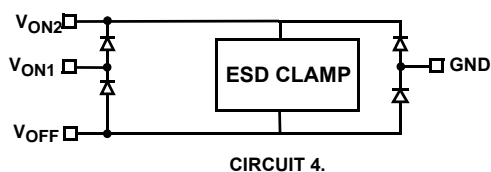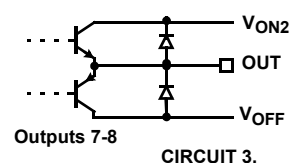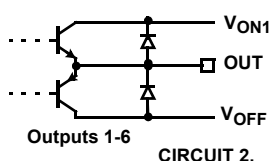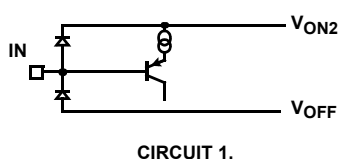
CIRCUIT 1.

Outputs 1-6
CIRCUIT 2.

Outputs 7-8
CIRCUIT 3.

CIRCUIT 4.

ISL24010

Typical Performance Curves T_A = 25°C, Output load parallel RC (RL = 5kΩ, CL = 100pF) unless otherwise specified.
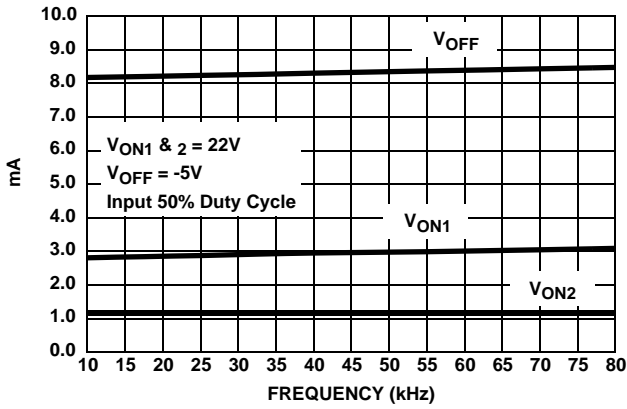
FIGURE 1. SUPPLY CURRENT vs FREQUENCY 1 CHANNEL TOGGELING
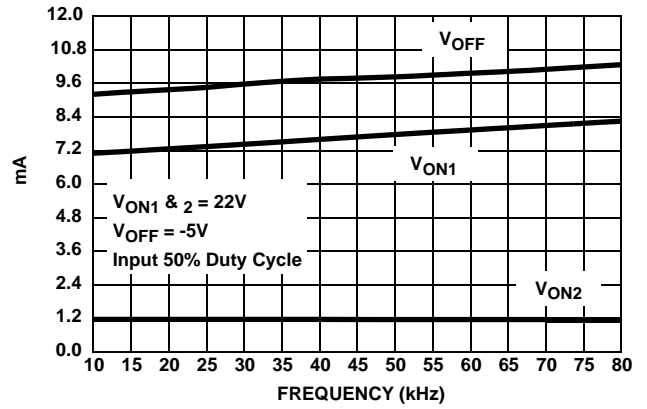
FIGURE 2. SUPPLY CURRENT vs FREQUENCY 4 CHANNELS TOGGELING
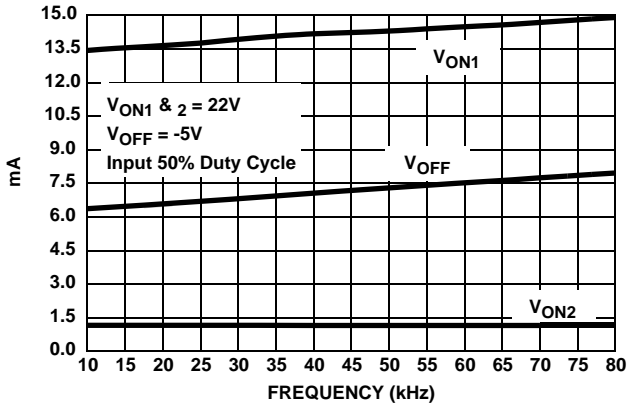
FIGURE 3. SUPPLY CURRENT vs FREQUENCY 6 CHANNELS TOGGLING
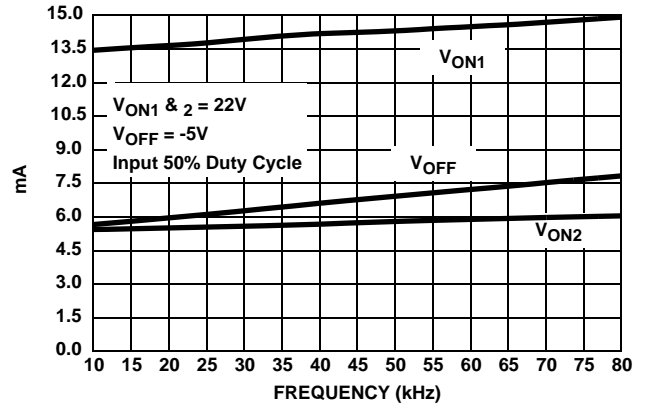
FIGURE 4. SUPPLY CURRENT vs FREQUENCY 8 CHANNELS TOGGLING
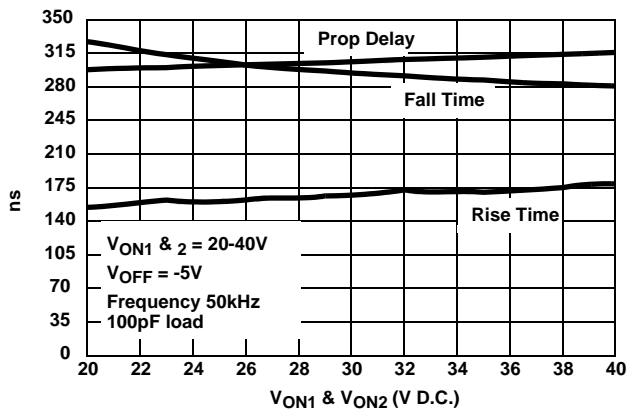
FIGURE 5. RISE TIME, FALL TIME AND PROP DELAY vs V_{ON1} & V_{ON2} VOLTAGE WITH V_{OFF} = -5V
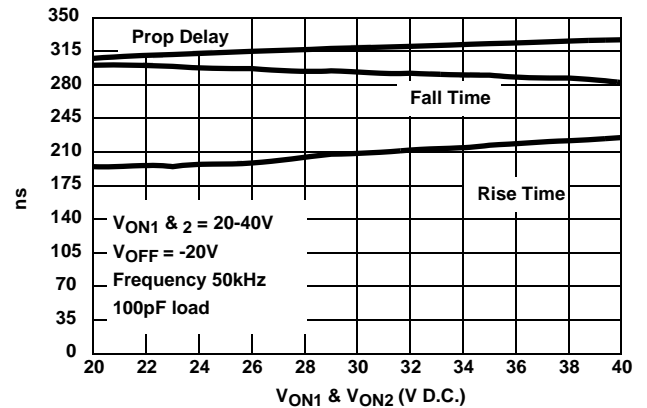
FIGURE 6. RISE TIME, FALL TIME AND PROP DELAY vs V_{ON1} & V_{ON2} VOLTAGE WITH V_{OFF} = -20V

Typical Performance Curves T_A = 25°C, Output load parallel RC (RL = 5kΩ, CL = 100pF) unless otherwise specified. **(Continued)**
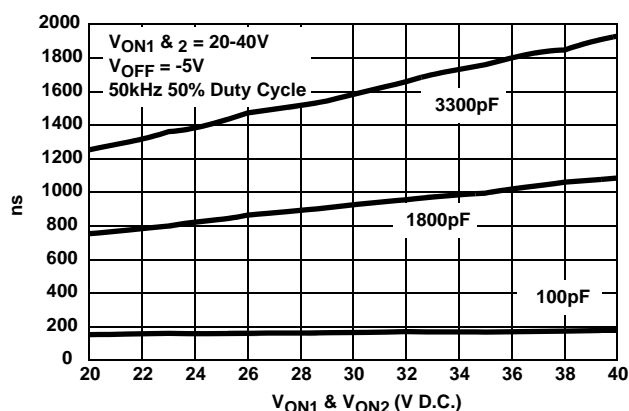
FIGURE 7. RISE TIME vs CAPACITANCE vs SUPPLY
VOLTAGE WITH V_{OFF} = -5V
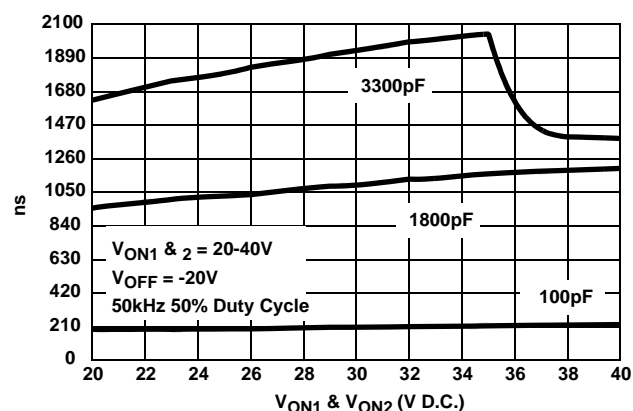
FIGURE 8. RISE TIME vs CAPACITANCE vs SUPPLY
VOLTAGE WITH V_{OFF} = -20V
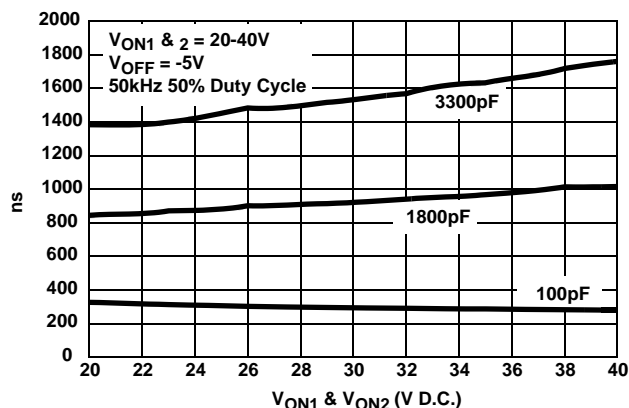
FIGURE 9. FALL TIME vs CAPACITANCE vs SUPPLY
VOLTAGE WITH V_{OFF} = -5V
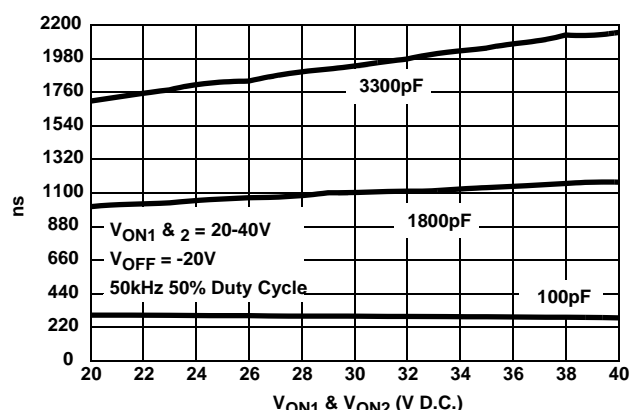
FIGURE 10. FALL TIME vs CAPACITANCE vs SUPPLY
VOLTAGE WITH V_{OFF} = -20V
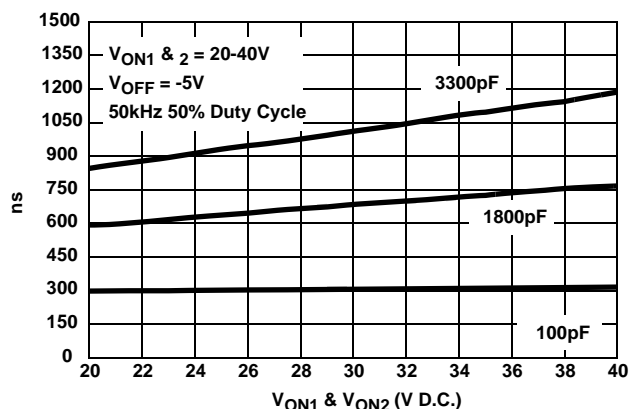
FIGURE 11. PROP DELAY vs CAPACITANCE vs SUPPLY
VOLTAGE WITH V_{OFF} = -5V
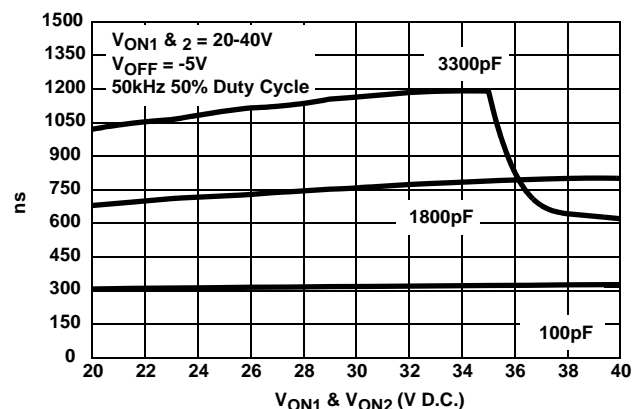
FIGURE 12. PROP DELAY vs CAPACITANCE vs SUPPLY
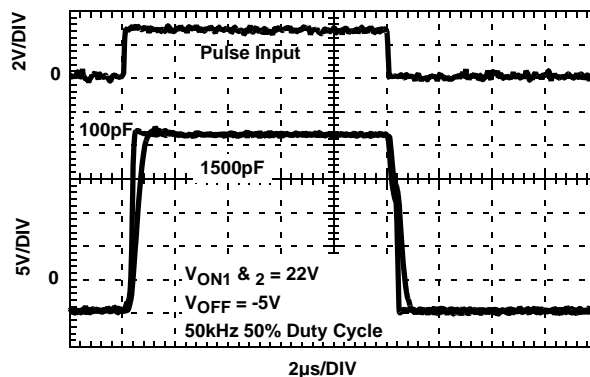VOLTAGE WITH V_{OFF} = -20V

ISL24010

FIGURE 13. TRANSIENT RESPONSE vs LOAD CAPACITANCE

Application Information

General

The ISL24010 is an Octal voltage level shifter. The part was designed to level shifts a digital input signal to +22V and -5V for TFT-LCD displays. The device is capable of level shifting a CMOS logic signal between +40V and -20V.

Power Supply Decoupling

The ISL24010 requires a 0.1μF decoupling capacitor as close to the V_{ON1}, V_{ON2} and V_{OFF} power supply pins for a large load equal to 5kΩ in parallel with 100pF (Figure 16). This will deduce any dv/dt between the different supplies and prevent the internal ESD clamp from turning on and damaging the part.

Power Supply Sequence

The ISL24010 requires that V_{ON2} be greater than or equal to V_{ON1} at all times. Therefore, if V_{ON1} and Von 2 are different supplies, then V_{ON2} needs to be turned on before V_{ON1}. The reason for this requirement is shown in Circuit 4 in the Pin Description Table. The ESD protection diode between V_{ON2} and Von 1 will forward bias if V_{ON1} becomes a diode drop greater than V_{ON2}. Recommended power supply sequence: V_{ON2}, V_{ON1}, V_{OFF} then input logic signals.

The ESD protection scheme is based on diodes from the pins to the V_{ON2} supply and a dV/dt- triggered clamp. This dV/dt triggered clamp imposes a maximum supply turn-on slew rate of 10V/μs. This clamp will trigger if the supply powers up too fast, causing amps of current to flow. Ground and V_{ON1} are treated as I/O pins with this protection scheme. In applications where the dV/dt supply ramp could exceed 10V/μs, such as hot plugging, additional methods should be employed to ensure the rate of rise is not exceeded.

Latch-up Proof

The ISL24010 is manufactured in a high voltage DI process that isolates every transistor in it's own tub making the part latch-up proof.

Input Pin Connections

Unused inputs must be tied to ground. Failure to tie unused input pins to ground will result in a rail to rail oscillations on the respective output pins and higher unwanted power dissipation in the part. Under these conditions, the temperature of the part could get very hot.

Limiting the Output Current

No output short circuit current limit exists on this part. All applications need to limit the output current to less than 80mA. Adequate thermal heat sinking of the parts is also required.
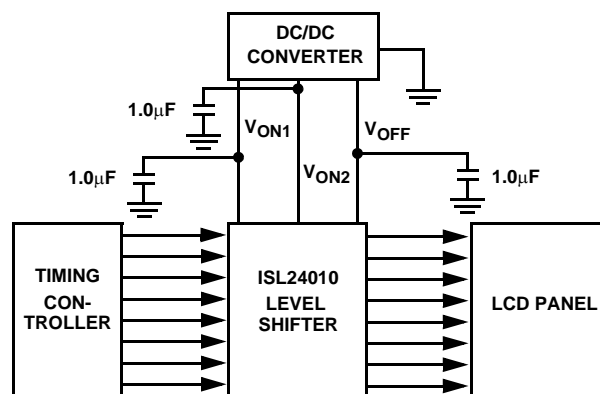
Application Diagram (TV)

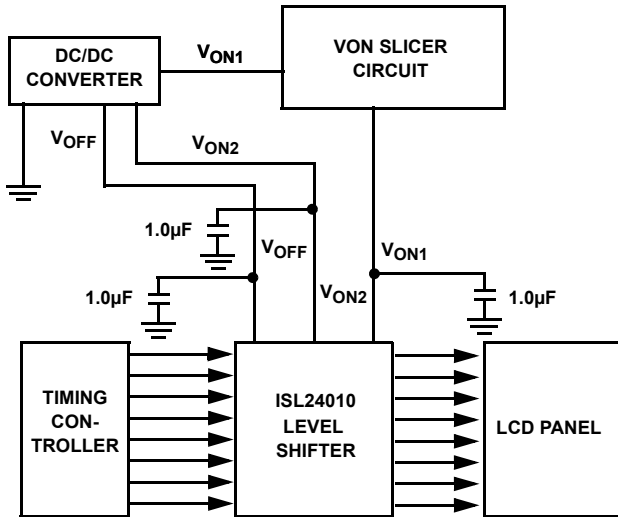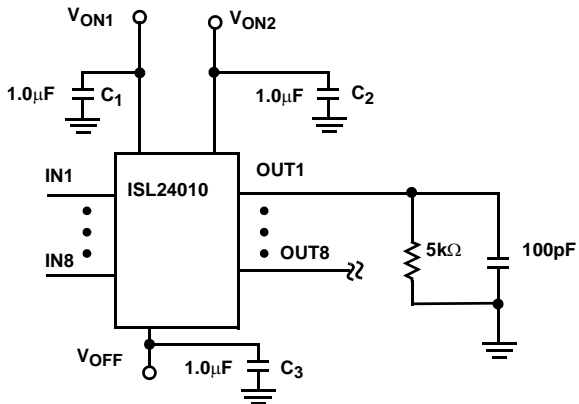**FIGURE 14. TYPICAL TV APPLICATION CIRCUIT**

Application Diagram (Monitor)

FIGURE 15. TYPICAL MONITOR APPLICATION CIRCUIT WITH SLICER TO REDUCE FLICKER

Test Circuit

If the output load is a series 200Ω resistor and a 3300pF then C1, C2 and C3 can be reduced to 0.47pF.
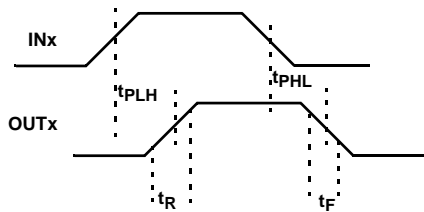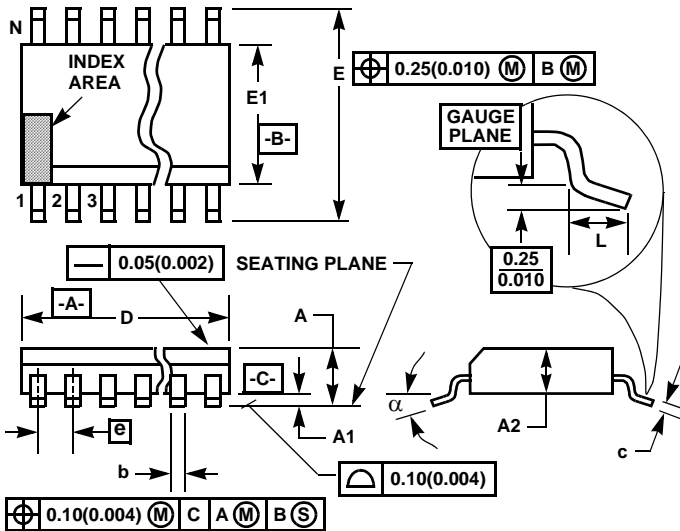

FIGURE 16. TEST LOAD AND TIMING DEFINITIONS

Thin Shrink Small Outline Plastic Packages (TSSOP)

M20.173
20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.252	0.260	6.40	6.60	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 1 6/98

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

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