Data Sheet | April 13, 2007 | FN6156.2

Single and Dual Ultra-Low Noise, Rail-to-Rail, Op Amp

The ISL28191 and ISL28291 are tiny single and dual ultra-low noise, ultra-low distortion operational amplifiers. Fully specified to operated down to +3V single supply. These amplifiers have outputs that swing rail-to-rail, and an input common mode voltage that extends to ground (ground sensing).

The ISL28191 and ISL28291 are unity gain stable with an input referred voltage noise of 1.7nV/√Hz. Both parts feature 2^{nd} and 3^{rd} harmonic distortion of -76dBc and -70dBc, respectively.

The ISL28191 is available in the space-saving 6 Ld µTDFN (1.6mm x 1.6mm) and SOT-23 packages. The ISL28291 is available in the 10 Ld µTQFN (1.8mm x 1.4mm) and MSOP packages. All devices are guaranteed over -40°C to +125°C.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-free)	PKG. DWG. #
ISL28191FHZ-T7	GABJ	3k pcs	6 Ld SOT-23	MDP0038
Coming Soon ISL28191FRUZ-TK		1k pcs	6 Ld µTDFN	L6.1.6x1.6A
ISL28291FUZ	8291Z	50/tube	10 Ld MSOP	MDP0043
ISL28291FUZ-T7	8291Z	1.5k pcs	10 Ld MSOP	MDP0043
Coming Soon ISL28291FRUZ-T7		1k pcs	10 Ld µTQFN	L10.1.8x1.4A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

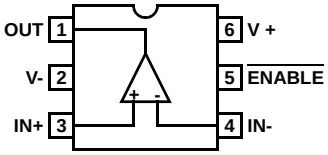
- 1.7nV/√Hz input voltage noise at 1kHz
- Harmonic Distortion -76dBc, -70dBc, f_O = 1MHz
- 61MHz -3dB bandwidth
- 630µV maximum offset voltage
- 3µA input bias current
- 100dB typical CMRR
- 3V to 5.5V single supply voltage range
- Rail-to-rail output
- Ground Sensing
- Enable pin
- Pb-free plus anneal available (RoHS compliant)

Applications

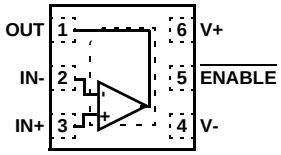
- Low noise signal processing
- Low noise microphones/preamplifiers
- ADC buffers
- DAC output amplifiers
- Digital scales
- Strain gauges/sensor amplifiers
- Radio systems
- Portable equipment
- Infrared detectors

Pinouts

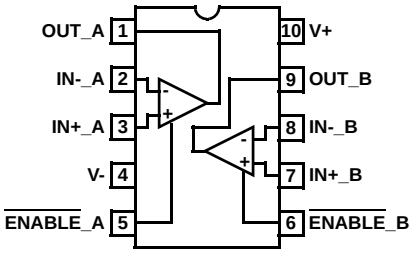
ISL28191
(6 LD SOT-23)
TOP VIEW



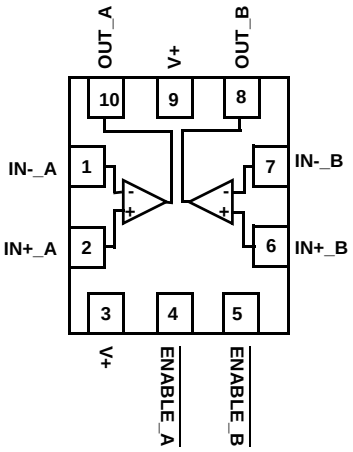
ISL28191
(6 LD 1.6X1.6X0.5 µTDFN)
TOP VIEW



ISL28291
(10 LD MSOP)
TOP VIEW



ISL28291
(10 LD µTQFN**)**
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD tolerance, Human Body Model 3kV
ESD tolerance, Machine Model 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
6 Ld SOT-23 Package	230
6 Ld µTDFN Package	120
10 Ld MSOP Package	115
6 Ld µTQFN Package	143

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+= 5.0V, V_-= GND, R_L = 1kΩ, R_F = 1kΩ, A_V = -1. unless otherwise specified. Parameters are per amplifier. Typical values are at V+= 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C, temperature data guaranteed by characterization**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage			270	630 **840**	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature	Figure 17		3.1		µV/°C
I_{OS}	Input Offset Current			35	500 **900**	nA
I_B	Input Bias Current			3	6 **7**	µA
HD (1MHz)	2nd Harmonic Distortion	$2V_{P-P}$ output voltage, A_V = 1		-76		dBc
	3rd Harmonic Distortion			-70		dBc
V_N	Input Referred Voltage Noise	f_O = 1kHz		1.7		nV/√Hz
IN	Input Referred Current Noise	f_O = 1kHz		1.8		pA/√Hz
CMIR	Common-Mode Input Range		0		3.8	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.8V	78	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 5V	74	80		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4V, R_L = 1kΩ	90 **86**	98		dB
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 1kΩ		20	50 **80**	mV
		Output high, R_L = 1kΩ, V+ = 5V	4.95 **4.92**	4.97		V
SR	Slew Rate		12 **12**	17		V/µs
3dB BW	3dB Bandwidth	C_L = 20pF, A_V = 1, R_L = 10kΩ		61		MHz
$I_{S,ON}$	Supply Current, Enabled			2.6	3.5 **3.9**	mA
$I_{S,OFF}$	Supply Current, Disabled			26	35 **48**	µA
I_O+	Short-Circuit Output Current	R_L = 10Ω	95 **90**	130		mA
I_O-	Short-Circuit Output Current	R_L = 10Ω	95 **90**	130		mA

Electrical Specifications V_+= 5.0V, V_-= GND, R_L = 1kΩ, R_F = 1kΩ, A_V = -1. unless otherwise specified. Parameters are per amplifier. Typical values are at V+= 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C, temperature data guaranteed by characterization**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Supply Operating Range	V_S+ to V_S-	3		5.5	V
V_{INH}	ENABLE Pin High Level		2			V
V_{INL}	ENABLE Pin Low Level				0.8	V
I_{ENH}	ENABLE Pin Input High Current	V_{EN} = V+		0.8	1.1 **1.3**	µA
I_{ENL}	ENABLE Pin Input Low Current	V_{EN} = V-		20	80 **100**	nA

Typical Performance Curves

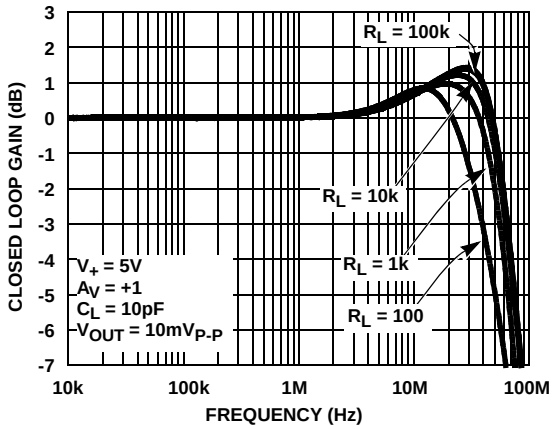


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

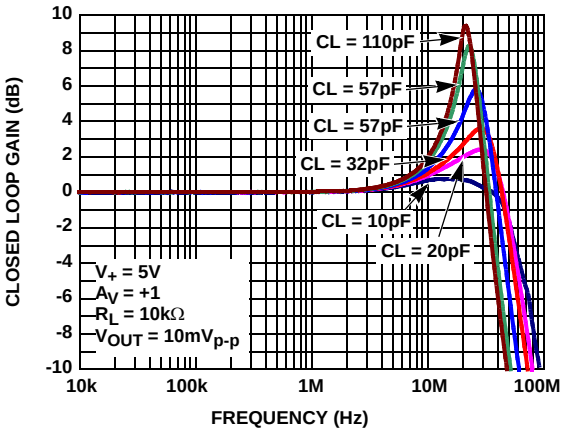


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

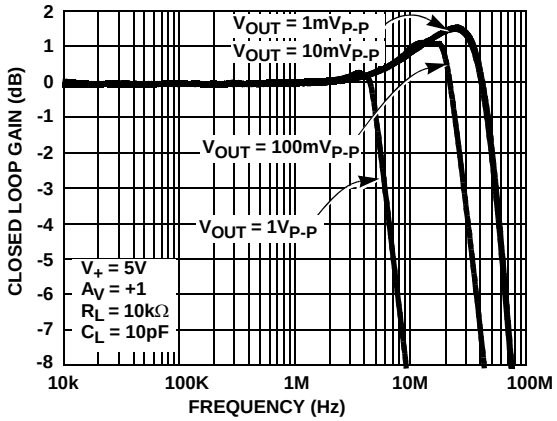


FIGURE 3. -3dB BANDWIDTH vs V_{OUT}

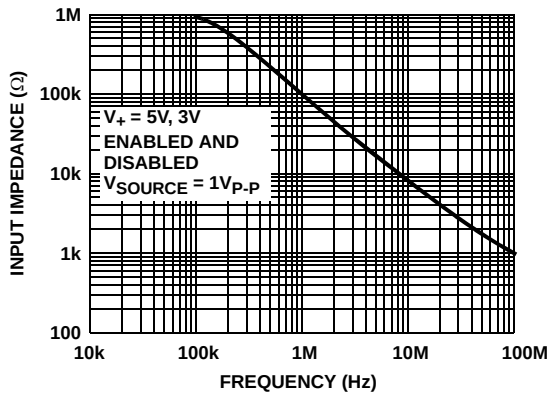


FIGURE 4. INPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

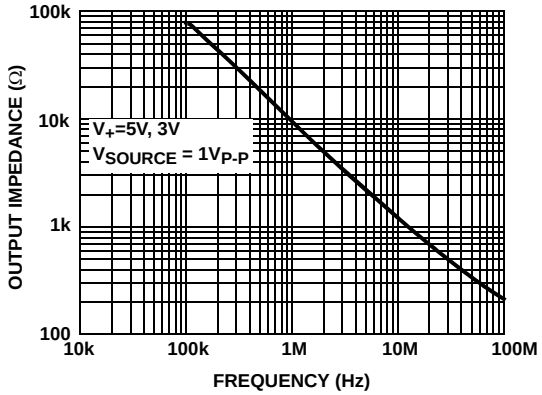


FIGURE 5. DISABLED OUTPUT IMPEDANCE vs FREQUENCY

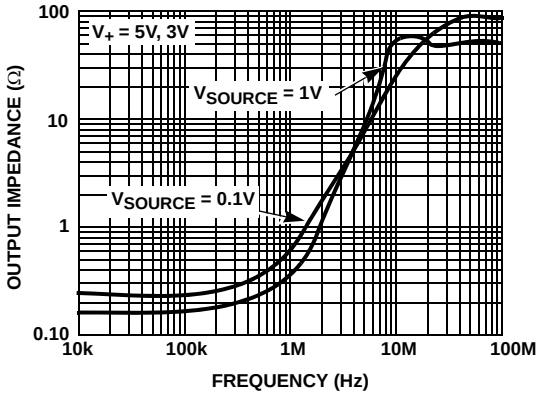


FIGURE 6. ENABLED OUTPUT IMPEDANCE vs FREQUENCY

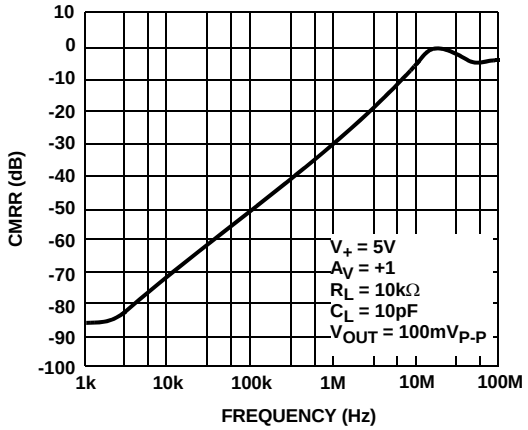


FIGURE 7. CMRR vs FREQUENCY

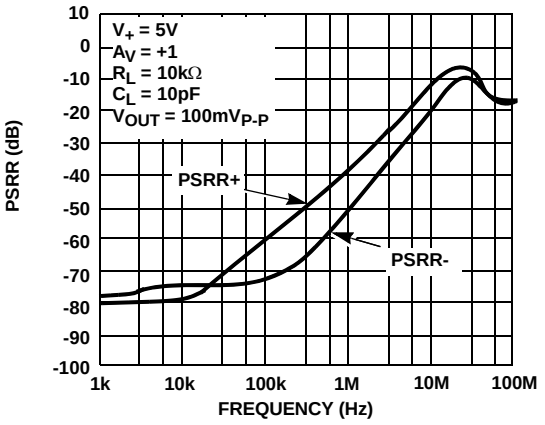


FIGURE 8. PSRR vs FREQUENCY

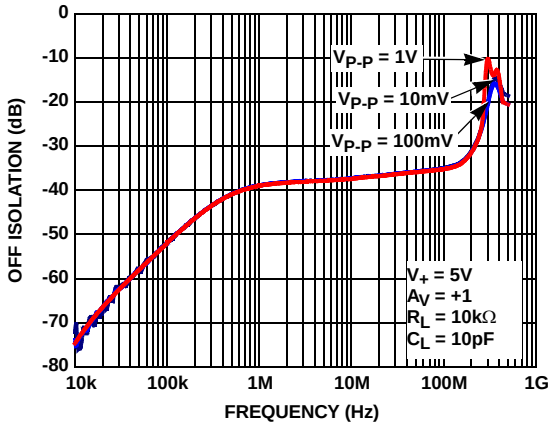


FIGURE 9. OFF ISOLATION vs FREQUENCY

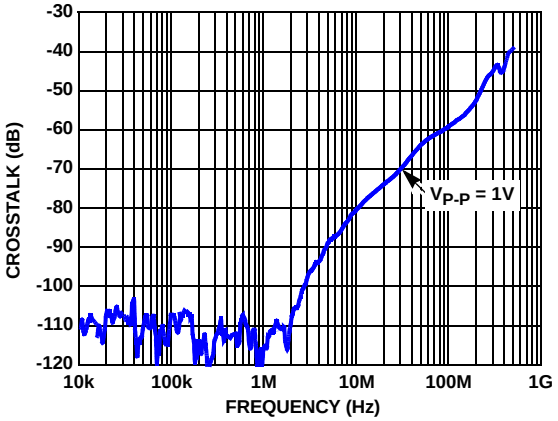


FIGURE 10. CHANNEL TO CHANNEL CROSSTALK vs FREQUENCY

Typical Performance Curves (Continued)

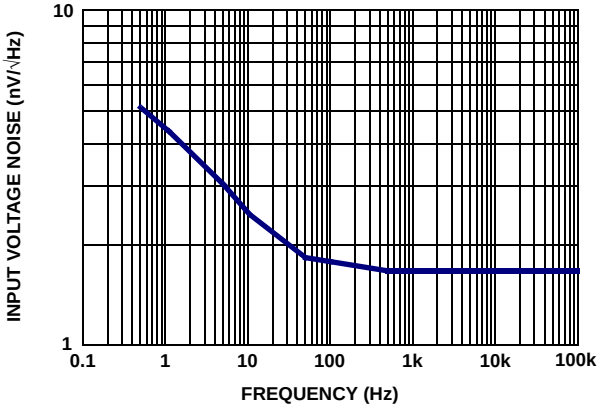


FIGURE 11. INPUT REFERRED NOISE VOLTAGE vs FREQUENCY

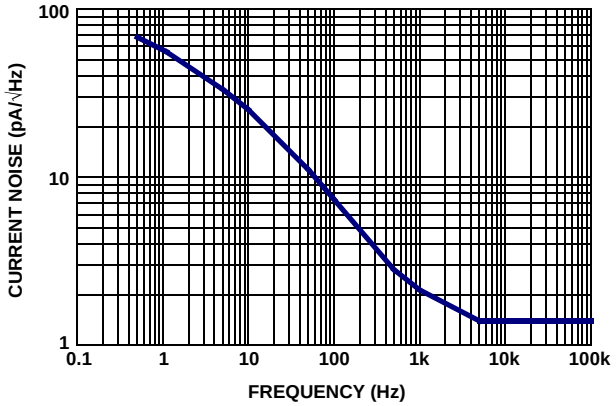


FIGURE 12. INPUT REFERRED NOISE CURRENT vs FREQUENCY

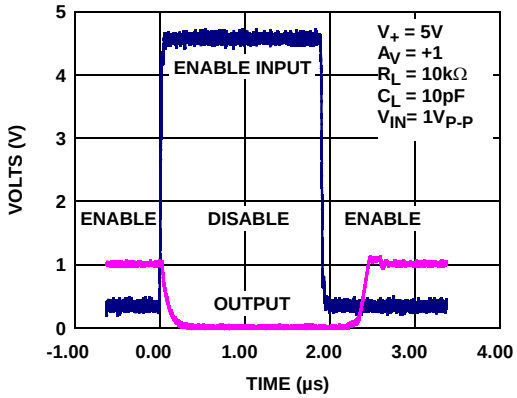


FIGURE 13. ENABLE/DISABLE TIMING

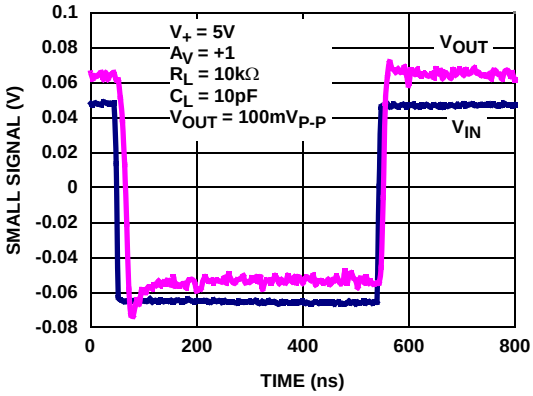


FIGURE 14. SMALL SIGNAL STEP RESPONSE_RISE AND FALL TIME

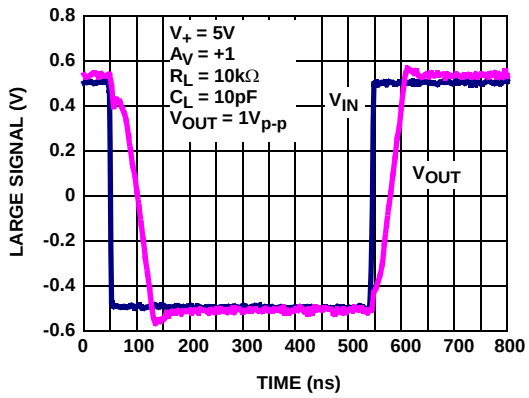


FIGURE 15. LARGE SIGNAL STEP RESPONSE_RISE AND FALL TIME

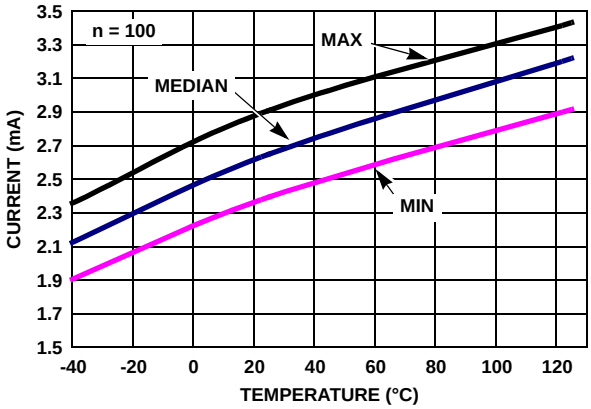


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

Typical Performance Curves (Continued)

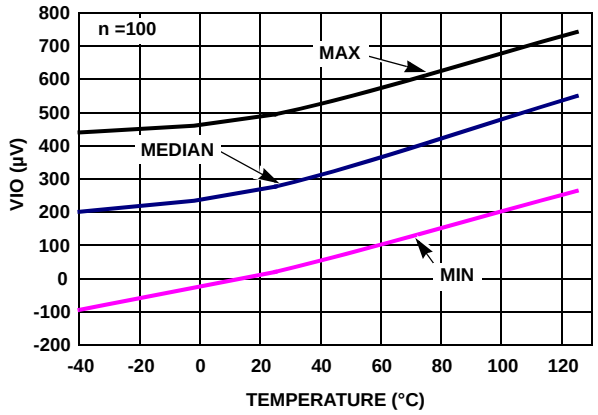


FIGURE 17. VIO vs TEMPERATURE V_S = ±2.5V

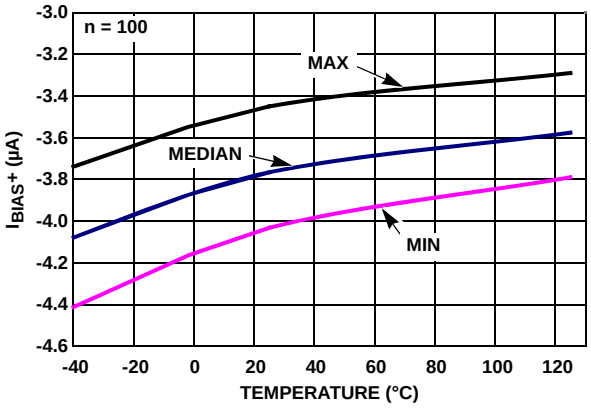


FIGURE 18. I_{BIAS+} vs TEMPERATURE V_S = ±2.5V

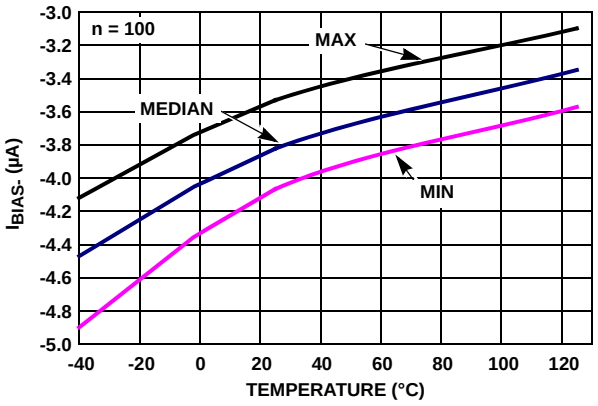


FIGURE 19. I_{BIAS-} vs TEMPERATURE V_S = ±2.5V

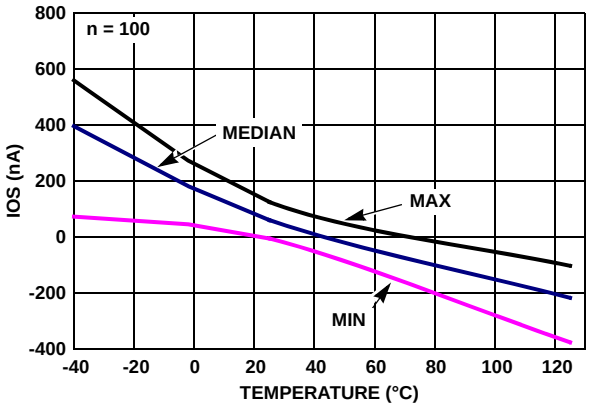


FIGURE 20. IOS vs TEMPERATURE V_S = ±2.5V

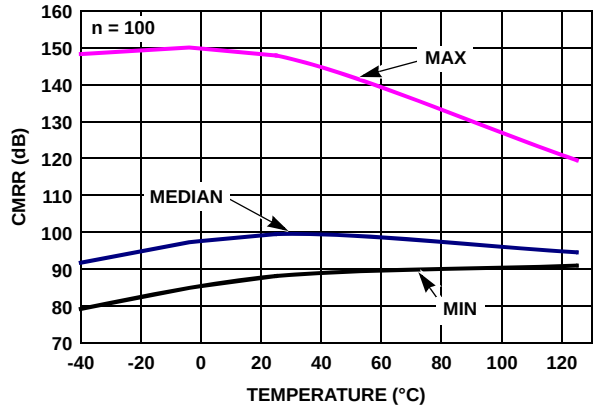


FIGURE 21. CMRR vs TEMPERATURE VCM = 3.8V, V_S = ±2.5V

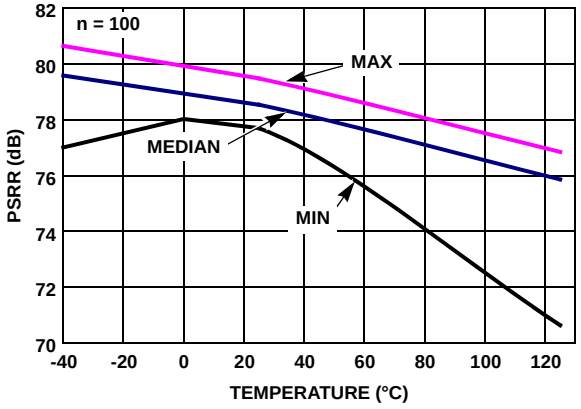


FIGURE 22. PSRR vs TEMPERATURE ±1.5V to ±2.5V

Typical Performance Curves (Continued)

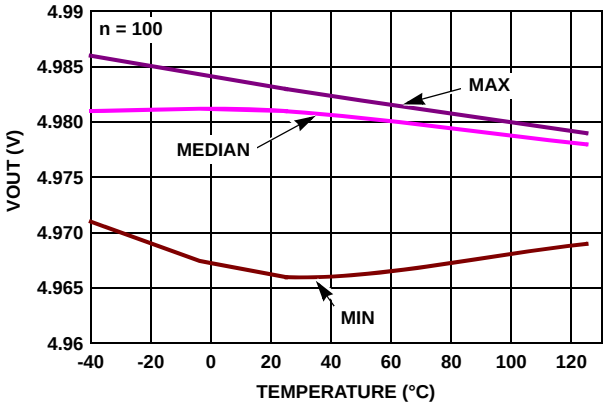


FIGURE 23. POSITIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

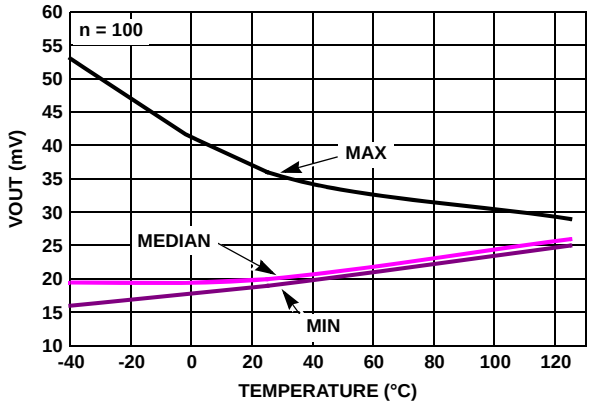
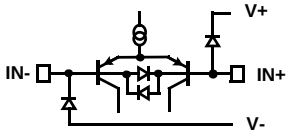
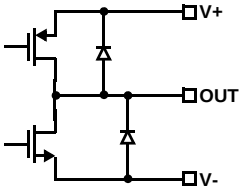
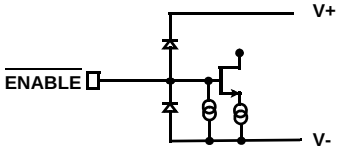


FIGURE 24. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

Pin Descriptions

ISL28191 (6 Ld SOT-23)	ISL28191 (6 Ld μTDFN)	ISL28291 (10 Ld MSOP)	ISL28191 (10 Ld μTDFN)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
4	1	2 (A) 8 (B)	1 (A) 7 (B)	IN-	Inverting input	 Circuit 1
3	3	3 (A) 7 (B)	2 (A) 6 (B)	IN+	Non-inverting input	(See circuit 1)
2	2	4	3	V-	Negative supply	
1	4	1 (A) 9 (B)	10 (A) 8 (B)	OUT	Output	 Circuit 2
6	6	10	9	V+	Positive supply	
5	5	5 (A) 6 (B)	4 (A) 5 (B)	$\overline{\text{ENABLE}}$	Enable BAR pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.	 Circuit 3

Applications Information

Product Description

The ISL28191 and ISL28291 are voltage feedback operational amplifier designed for communication and imaging applications requiring very low voltage and current noise. Both parts feature low distortion while drawing moderately low supply current. The ISL28191 and ISL28291 use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier.

Enable/Power-Down

The ISL28191 and ISL28291 amplifiers are disabled by applying a voltage greater than 2V to the $\overline{\text{ENABLE}}$ pin, with respect to the V- pin. In this condition, the output(s) will be in a high impedance state and the amplifier(s) current will be reduced to 13µA/Amp. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{\text{ENABLE}}$ pin. The $\overline{\text{ENABLE}}$ pin also has an internal pull down. If left open, the $\overline{\text{ENABLE}}$ pin will pull to the negative rail and the device will be enabled by default.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both parts have additional back-to-back diodes across the input terminals (as shown in Figure 25). In pulse applications where the input Slew Rate exceeds the Slew Rate of the amplifier, the possibility exists for the input protection diodes to become forward biased. This can cause excessive input current and distortion at the outputs. If overdriving the inputs is necessary, the external input current must never exceed 5mA. An external series resistor may be used to limit the current as shown in Figure 25.

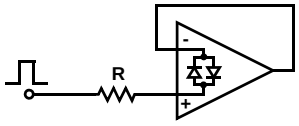


FIGURE 25. LIMITING THE INPUT CURRENT TO LESS THAN 5mA

Using Only One Channel

The ISL28291 is a Dual channel op-amp. If the application only requires one channel when using the ISL28291, the user must configure the unused channel to prevent it from oscillating. Oscillation can occur if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 26).

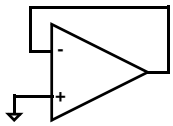


FIGURE 26. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Current Limiting

The ISL28191 and ISL28291 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device. This is why output short circuit current is specified and tested with $R_L = 10\Omega$.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL})$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

where:

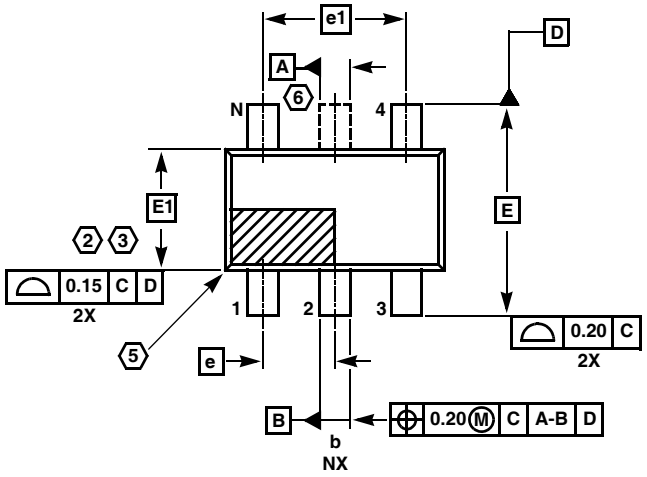
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

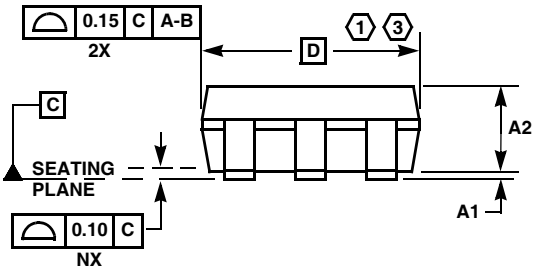
Power Supply Bypassing and Printed Circuit Board Layout

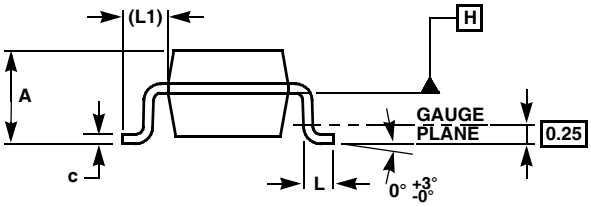
As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the inverting input. When ground plane construction is used, it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of additional series inductance. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in additional peaking and overshoot.

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

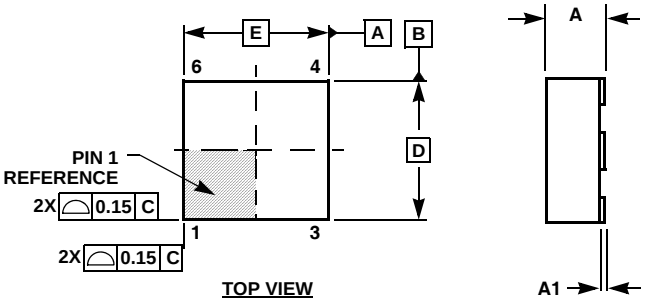
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

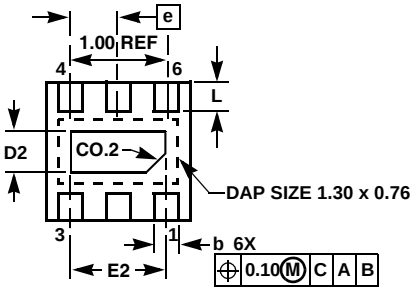
Rev. F 2/07

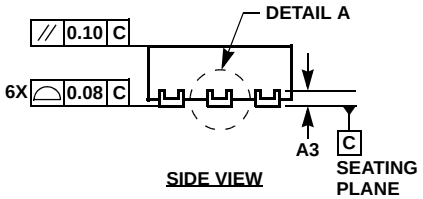
NOTES:

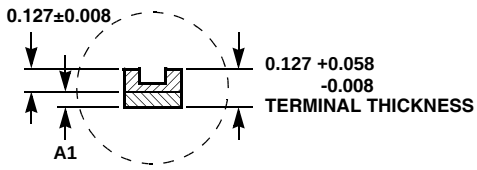
1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

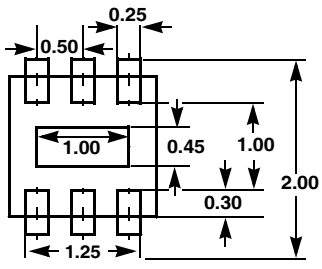
Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)











L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

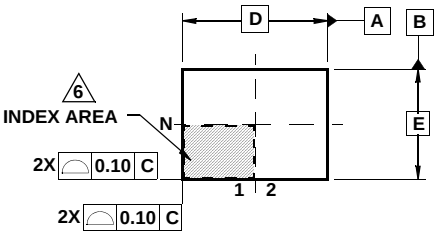
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e		0.50 BSC		-
L	0.25	0.30	0.35	-

Rev. 1 6/06

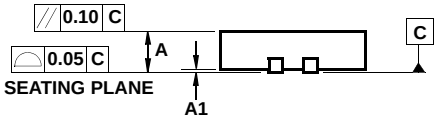
NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

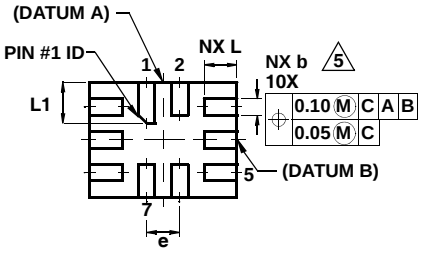
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



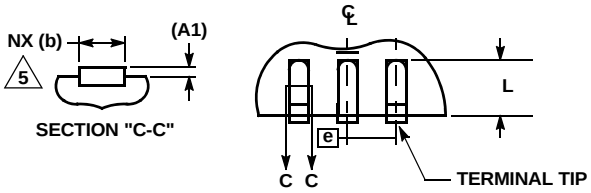
TOP VIEW

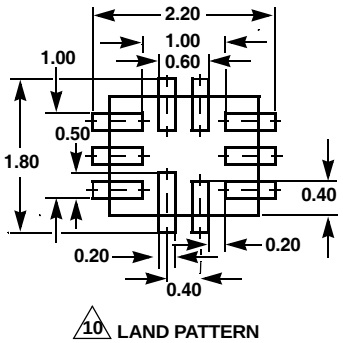


SIDE VIEW



BOTTOM VIEW





L10.1.8x1.4A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

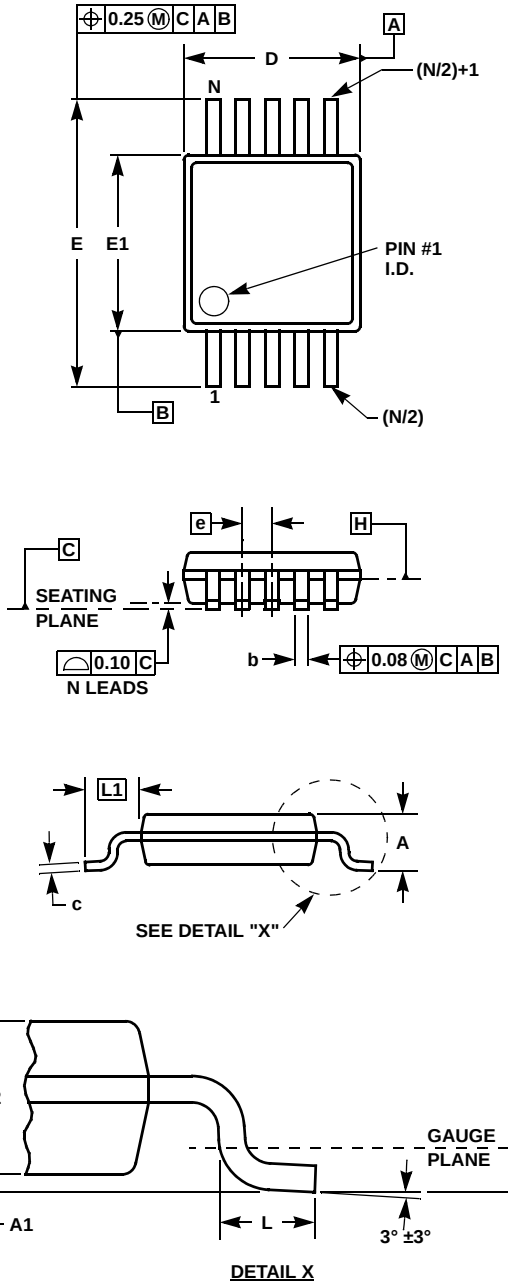
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	1.75	1.80	1.85	-
E	1.35	1.40	1.45	-
e		0.40 BSC		-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N		10		2
Nd		2		3
Ne		3		3
θ	0	-	12	4

Rev. 3 6/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.