Data Sheet August 1999 File Number 3977.2

Radiation Hardened Single 8/Differential 4-Channel CMOS Analog Multiplexers

These radiation hardened monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS. Switches are guaranteed to break-before-make, so that two channels are never shorted together. The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic “1” and maximum 0.8 for logic “0”. This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply. The HS-0508RH is an eight channel single-ended multiplexer, and the HS-0509RH is a four channel differential version. If input overvoltage protection is needed, the HS-0548RH and HS-0549RH multiplexers are recommended.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95692. A “hot-link” is provided on our homepage for downloading.
http://www.intersil.com/spacedefense/space.htm

Features

- Electrically Screened to SMD # 5962-95692
- QML Qualified per MIL-PRF-38535 Requirements
- Gamma Dose . . . . . 1 x 10^4RAD(Si)
- No Latch-Up
- No Channel Interaction During Overvoltage
- Low On Resistance . . . . . <200Ω (Typ)
- 44V Maximum Power Supply
- Break-Before-Make Switch
- Analog Signal Range . . . . . ±15V
- Access Time. . . . . <300ns (Typ)

Applications

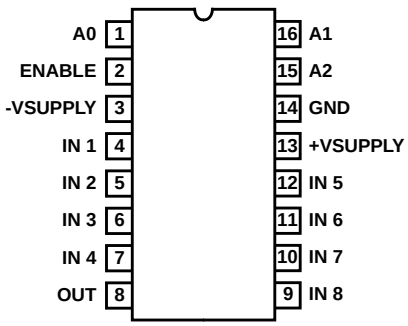
- Data Acquisition Systems
- Control Systems
- Telemetry

Ordering Information

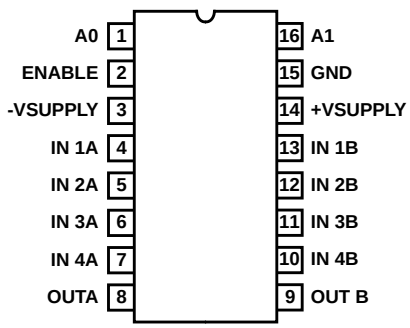
ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962D9569201VEA	HS1-0508RH-Q	-55 to 125
5962D9569201VEC	HS1B-0508RH-Q	-55 to 125
5962D9569202VEA	HS1-0509RH-Q	-55 to 125
5962D9569202VEC	HS1B-0509RH-Q	-55 to 125

Pinouts

HS-0508RH GDIP1-T16 (CERDIP)
OR CDIP2-T16 (SBDIP)
TOP VIEW

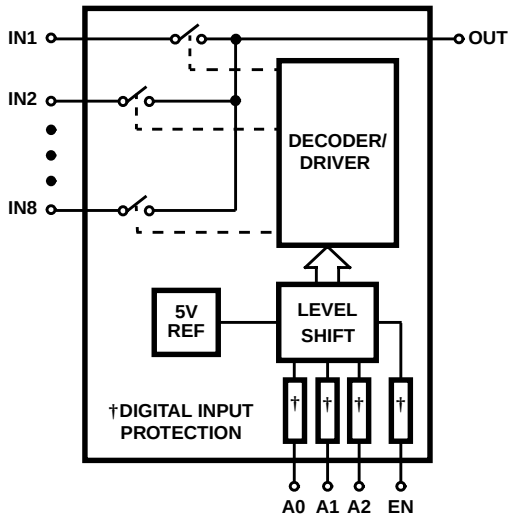


HS-0509RH GDIP1-T16 (CERDIP)
OR CDIP2-T16 (SBDIP)
TOP VIEW

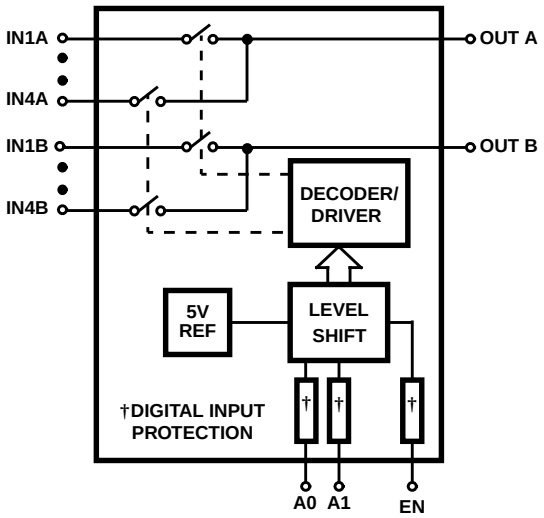


Functional Diagrams

HS-0508RH



HS-0509RH



HS-0508RH TRUTH TABLE

A2	A1	A0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HS-0509RH TRUTH TABLE

A1	A0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Schematic Diagrams

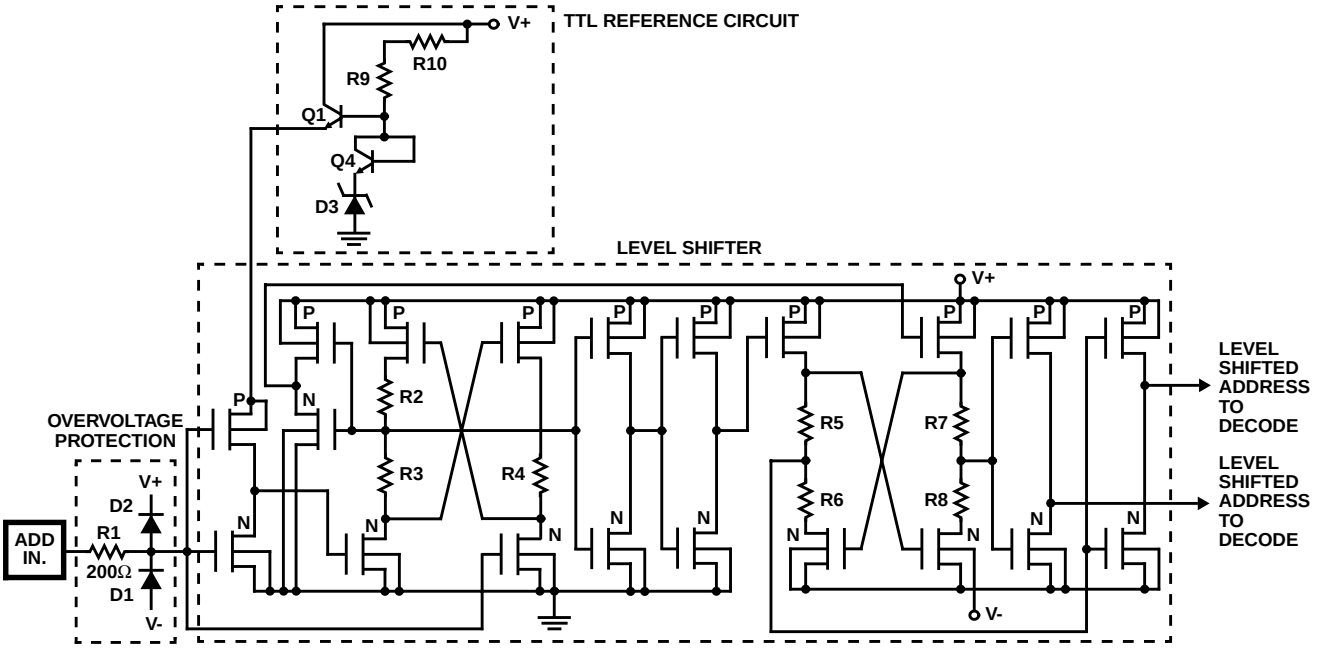


FIGURE 1. ADDRESS INPUT BUFFER AND LEVEL SHIFTER

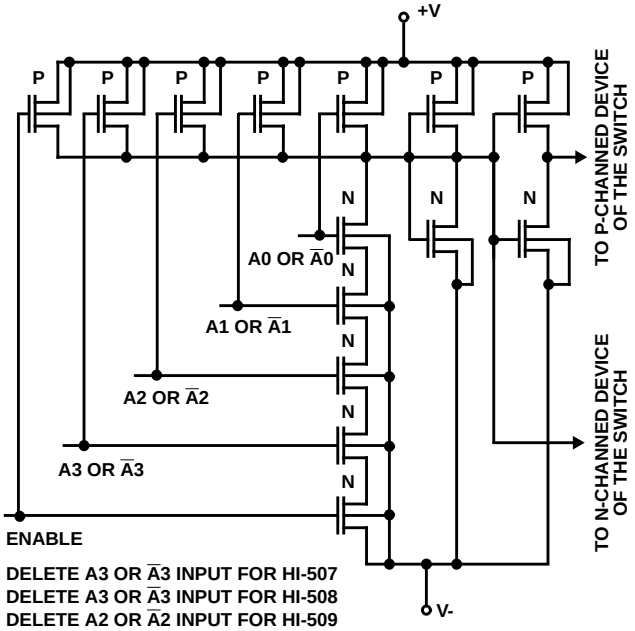


FIGURE 2. ADDRESS DECODER

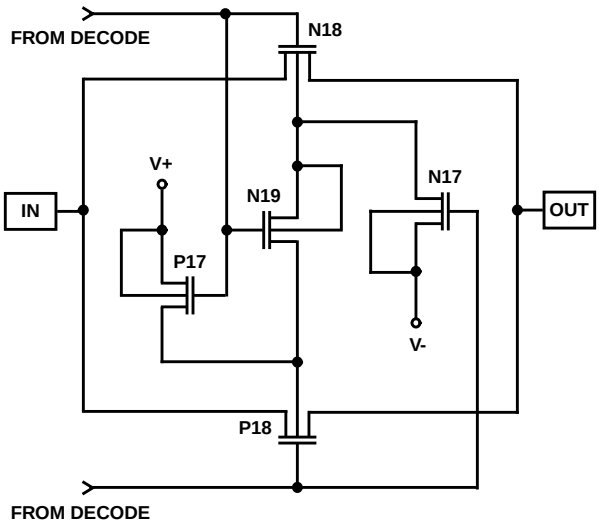
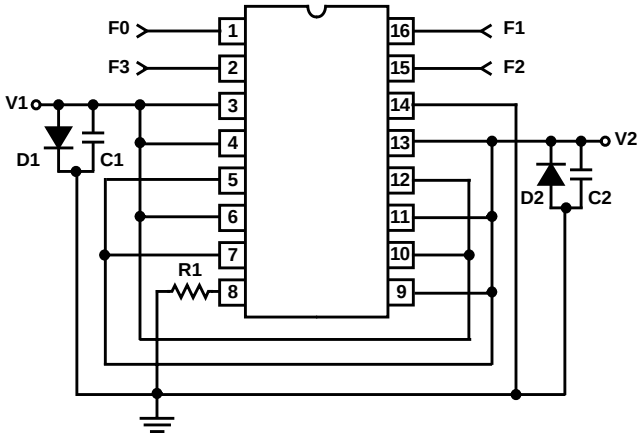


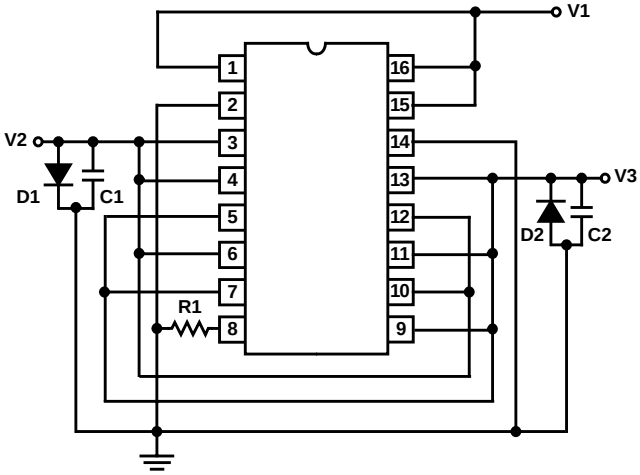
FIGURE 3. MULTIPLEX SWITCH

Burn-In/Life Test Circuits



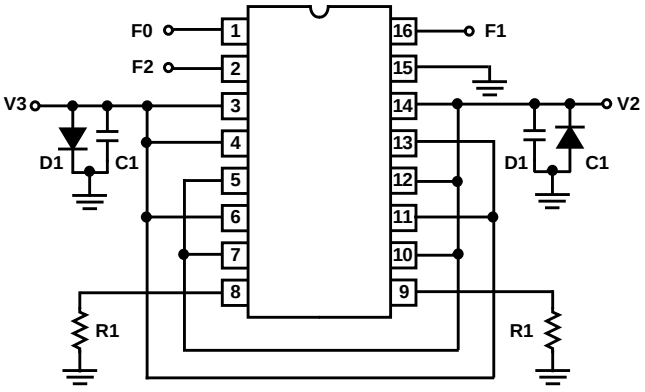
HS-0508RH
DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

V1 = -15V maximum, -16V minimum
V2 = +15V minimum, +16V maximum
R1 = 10kΩ ±5% 1/4W
C1 = C2 = 0.01µF minimum (per socket) or 0.1µF minimum (per row)
D1 = D2 = 1N4002 (or equivalent)
F0 = 100kHz 50% duty cycle; VIL = 0.8V max; VIH = 4.0V min.
F1 = F0/2
F2 = F1/2
F3 = F2/2



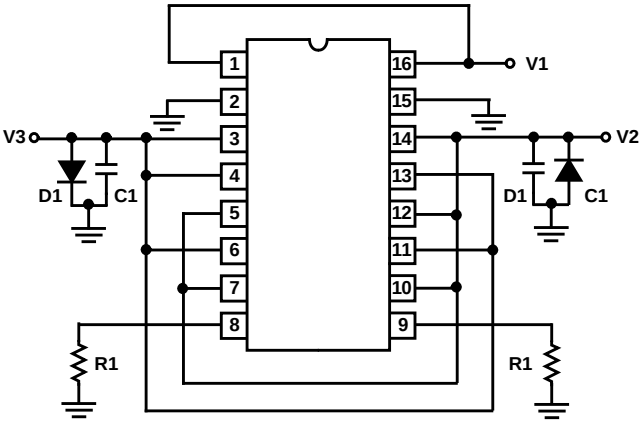
HS-0508RH
STATIC BURN-IN TEST CIRCUIT

V1 = 5V minimum, 6V maximum
V2 = -15V maximum, -16V minimum
V3 = +15V minimum, +16V maximum
R1 = 10kΩ ±5% 1/4W
C1 = C2 = 0.01µF minimum (per socket) or 0.1µF minimum (per row)
D1 = D2 = 1N4002 (or equivalent)



HS-0509RH
DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

V2 = +15.5V, ±.0.5V
V3 = -15.5V, ±0.5V
R1 = 10kΩ, ±5%
C1 = 0.1µF minimum (per socket)
D1 = 1N4002 or equivalent (per board)
F0 = 100kHz, ±10%; F1 = F0/2; F2 = F1/2, 50% duty cycle, VIL = 0.8V max.; VIH = 4.0V min.

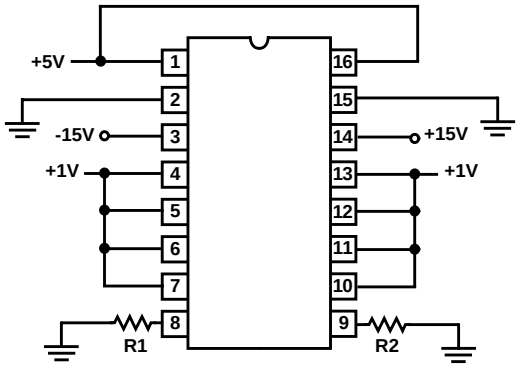


HS-0509RH
STATIC BURN-IN TEST CIRCUIT

V1 = +5.5V, ±0.5V
V2 = +15.5V, ±0.5V
V3 = -15.5V, ±0.5V
R1 = 10kΩ, ±10%
C1 = 0.1µF minimum (per socket)
D1 = 1N4002 or equivalent (per board)

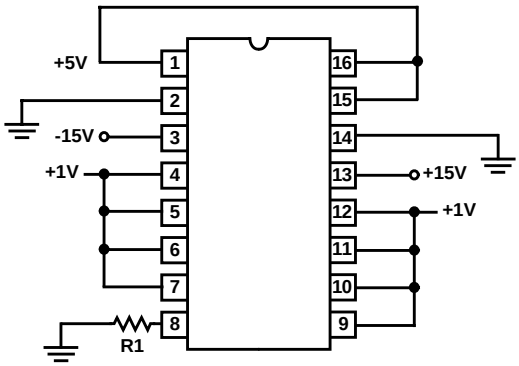
Irradiation Circuits

HS-0509RH



R1 = R2 = 10kΩ ±5%

HS-0508RH



R1 = 10kΩ ±5%

Die Characteristics

DIE DIMENSIONS:

81.9mils x 90.2mils x 19mils

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
Thickness: 7kÅ ±0.7kÅ

Top Metallization:

Type: Al
Thickness: 16kÅ ±2kÅ

Substrate:

CMOS
Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

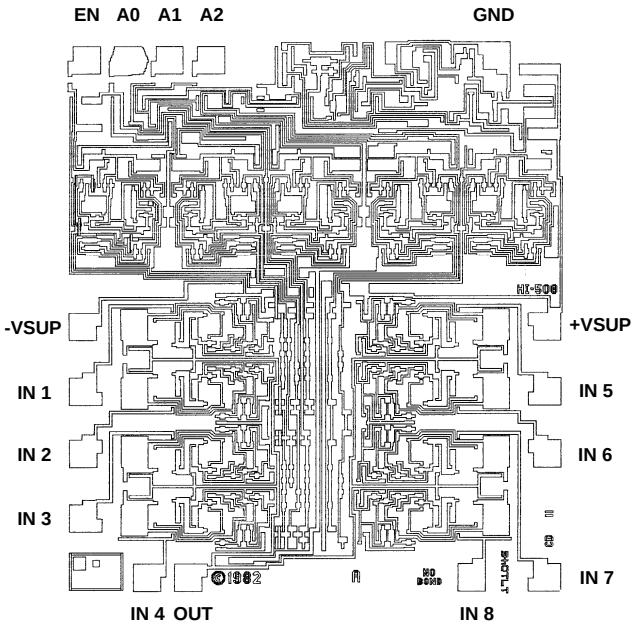
$< 2.0 \times 10^5$ A/cm^2

Transistor Count:

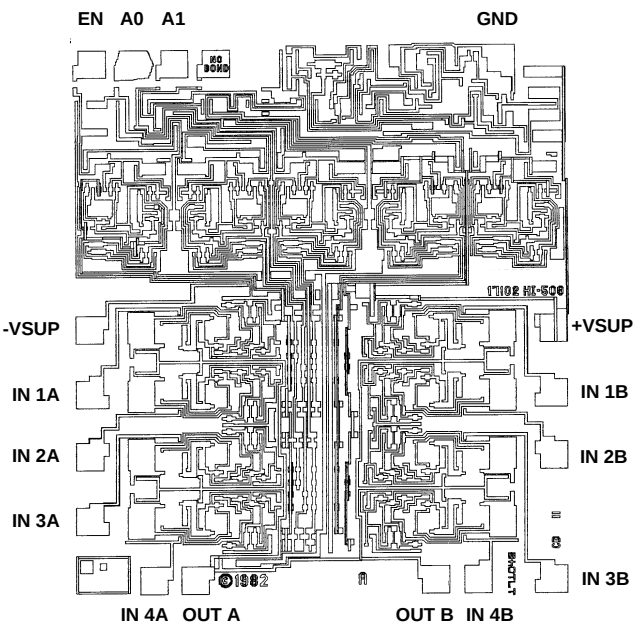
HS-0508RH	243
HS-0509RH	243

Metallization Mask Layout

HS-0508RH



HS-0509RH



NOTE: Pad numbers correspond to DIP pin numbers only.

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