

## CMOS Hex Buffer/Converter

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The CD4049UBT is an Inverting Hex Buffer and features logic level conversion using only one supply (voltage ( $V_{CC}$ )). The input signal high level ( $V_{IH}$ ) can exceed the  $V_{CC}$  supply voltage when this device is used for logic level conversions. This device is intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ( $V_{CC} = 5V$ ,  $V_{OL} \leq 0.4V$ , and  $I_{OL} \geq 3.3mA$ ).

The CD4049UBT is the designated replacement for the CD4009UB. Because the CD4049UBT requires only one power supply, it is preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB in all inverter, current driver, or logic level conversion applications. In these applications the CD4049UBT is pin compatible with the CD4009UB, and can be substituted for this device in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UBT, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

## Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the CD4049UBT are contained in SMD 5962-96636.** A "hot-link" is provided from our website for downloading.

[www.intersil.com/spacedefense/newsafclasst.asp](http://www.intersil.com/spacedefense/newsafclasst.asp)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/quality/manuals.asp](http://www.intersil.com/quality/manuals.asp)

## Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9663601TEC	CD4049UBDTR	-55 to 125
5962R9663601TXC	CD4049UBKTR	-55 to 125

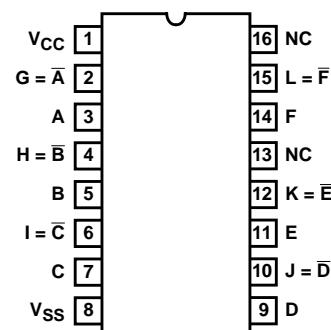
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

## Features

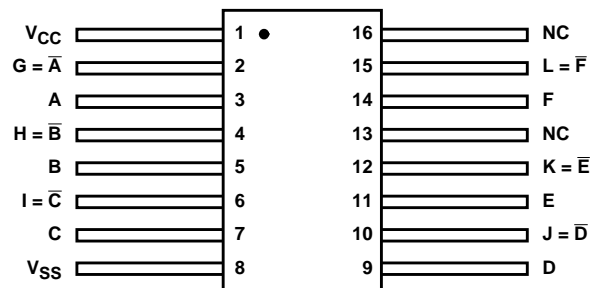
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - SEP Effective LET  $>75$  MEV-gm/cm<sup>2</sup>
- Inverting Type
- High Sink Current for Driving 2 TTL Loads
- High-to-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings

## Pinouts

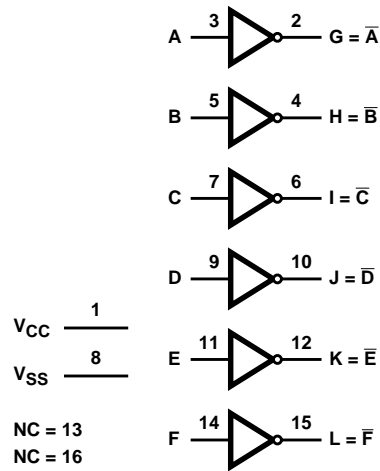
**CD4049BT (SBDIP), CDIP2-T16**  
TOP VIEW



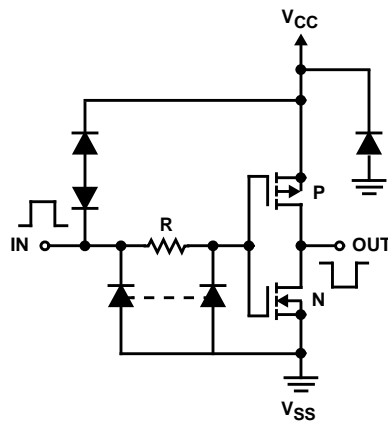
**CD4049BT (FLATPACK), CDFP4-F16**  
TOP VIEW



## Functional Diagram



## Schematic



SCHEMATIC DIAGRAM, 1 OF 6 IDENTICAL UNITS

## Die Characteristics

### DIE DIMENSIONS:

(1448 $\mu$ m x 1880 $\mu$ m x 533 $\mu$ m  $\pm$ 25.4 $\mu$ m)  
57 x 74 x 21mils  $\pm$ 1mil

### METALLIZATION:

Type: Al  
Thickness: 12.5k $\text{\AA}$   $\pm$ 1.5k $\text{\AA}$

### SUBSTRATE POTENTIAL:

Leave Floating or Tie to  $V_{CC}$   
Bond Pad #1 ( $V_{CC}$ ) First

### BACKSIDE FINISH:

Silicon

### PASSIVATION:

Type: Phosphorus Doped Silox ( $\text{SiO}_2$ )  
Thickness: 13.0k $\text{\AA}$   $\pm$ 2.6k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

$< 2.0\text{e}5 \text{ A/cm}^2$

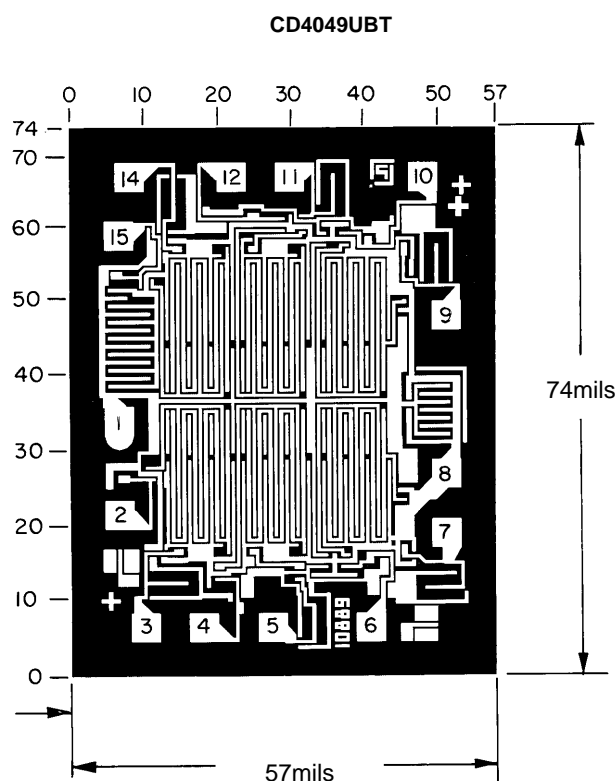
### TRANSISTOR COUNT:

12

### PROCESS:

Bulk CMOS

## Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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