82C83H

March 1997

CMOS Octal Latching Inverting Bus Driver

Features

- **Full 8-Bit Parallel Latching Buffer**
- **Bipolar 8283 Compatible**
- **Three-State Inverting Outputs**
- **Propagation Delay . . . . . 25ns Max**
- **Gated Inputs**
  - **Reduce Operating Power**
  - **Eliminate the Need for Pull-Up Resistors**
- **Single 5V Power Supply**
- **Low Power Operation**
  - **ICCSB 10mA**
- **Operating Temperature Ranges**
  - **C82C83H . . . . . 0^oC to $+70^oC$**
  - **I82C83H . . . . . -40^oC to $+85^oC$**
  - **M82C83H . . . . . -55^oC to $+125^oC$**

Description

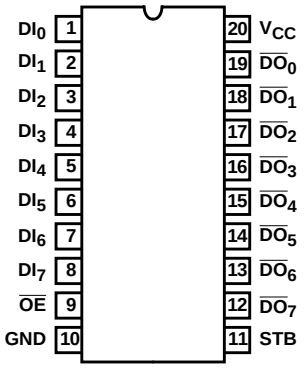
The Intersil 82C83H is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C83H provides an 8-bit parallel latch/buffer in a 20 lead pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable (OE) permits simple interface to microprocessor systems. The 82C83H provides inverted data at the outputs.

Ordering Information

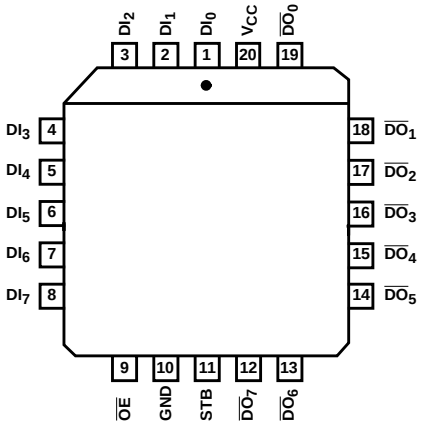
PART NO.	PACKAGE	TEMP RANGE	PKG. NO
CP82C83H	20 Ld PDIP	0^oC to $+70^oC$	E20.3
IP82C83H		-40^oC to $+85^oC$	E20.3
CS82C83H	20 Ld PLCC	0^oC to $+70^oC$	N20.35
IS82C83H		-40^oC to $+85^oC$	N20.35
CD82C83H	20 Ld CERDIP	0^oC to $+70^oC$	F20.3
ID82C83H		-40^oC to $+85^oC$	F20.3
MD82C83H/B		0^oC to $+70^oC$	F20.3
8406702RA	SMD#	-55^oC to $+125^oC$	F20.3
MR82C83H/B	20 Pad CLCC	-55^oC to $+125^oC$	J20.A
84067022A	SMD#	-55^oC to $+125^oC$	J20.A

Pinouts

82C83H (PDIP, CERDIP)
TOP VIEW



82C83H (PLCC, CLCC)
TOP VIEW



TRUTH TABLE

STB	OE	DI	DO
X	H	X	HI-Z
H	L	L	H
H	L	H	L
↓	L	X	†

H = Logic One
L = Logic Zero
X = Don't Care

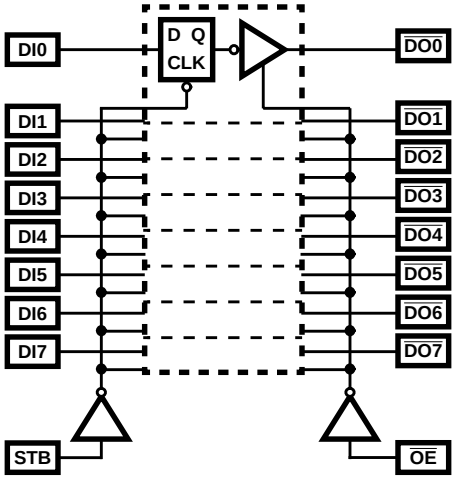
HI-Z = High Impedance
↓ = Negative Transition
† = Latched to Value of Last Data

PIN NAMES

PIN	DESCRIPTION
DI_0 - DI_7	Data Input Pins
DO_0 - DO_7	Data Output Pins
STB	Active High Strobe
OE	Active Low Output Enable

File Number **2971.1**

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance (``float'' condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Intersil 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

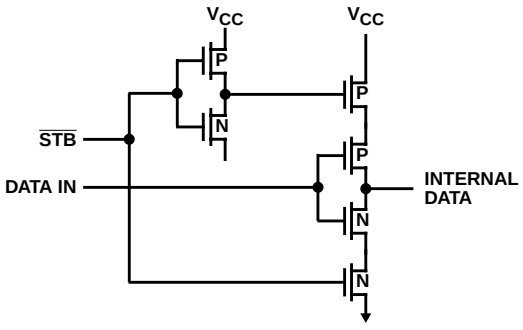


FIGURE 1. 82C82/83H

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10µA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

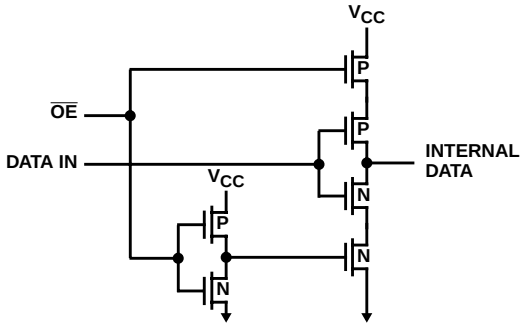


FIGURE 2. 82C86H/87H GATED INPUTS

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C83H data sheet is determined by

$I = C_L (dv/dt)$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(V_{CC} \times 80 \text{ percent})}{t_R / t_F} \quad \text{(EQ. 1)}$$

where t_R = 20ns, V_{CC} = 5.0V, C_L = 300pF on each eight outputs.

$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) = 480mA$

This current spike may cause a large negative voltage spike on V_{CC} which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1µF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

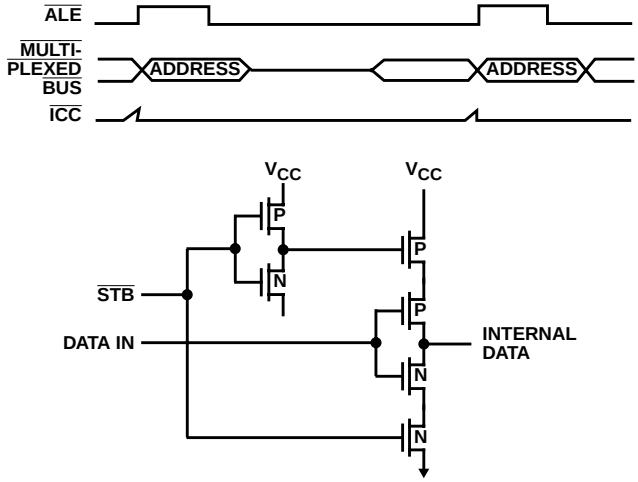


FIGURE 3. SYSTEM EFFECTS OF GATED INPUTS

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND 0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C83H . . . . . 0^oC to $+70^oC$
I82C83H . . . . . -40^oC to $+85^oC$
M82C83H . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
CERDIP Package	70	16
CLCC Package	80	20
PDIP Package	75	N/A
PLCC Package	75	N/A

Storage Temperature Range . . . . . -65^oC to $+150^oC$
Max Junction Temperature Ceramic Package . . . . . $+175^oC$
Max Junction Temperature Plastic Package. . . . . $+150^oC$
Lead Temperature (Soldering 10s) (PLCC - Lead Tips Only) . . $+300^oC$

Die Characteristics

Gate Count . . . . . 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0^oC to $+70^oC$ (C82C83H);
T_A = -40^oC to $+85^oC$ (I82C83H);
T_A = -55^oC to $+125^oC$ (M82C83H)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V	C82C83H, I82C83H, M82C83H, (Note 1)
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical One Output Voltage	3.0 V_{CC} -0.4V	-	V	I_{OH} = -8mA, I_{OH} = -100mA, $\overline{OE}$ = GND
V_{OL}	Logical Zero Output Voltage		0.45	V	I_{OL} = 20mA, $\overline{OE}$ = GND
I_I	Input Leakage Current	-10	10	µA	V_{IN} = GND or V_{CC}, DIP Pins 1-9,11
I_O	Output Leakage Current	-10	10	µA	V_O = GND or $\overline{OE} \geq V_{CC}$ -0.5V DIP Pins 12-19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND V_{CC} = 5.5V Outputs Open
IC COP	Operating Power Supply Current	-	1	mA/ MHz	T_A = $+25^oC$, V_{CC} = 5V, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = V_{IHMIN} to one data Input at a time and checking the corresponding device output for a valid logical 1 - during valid input high time. Control pins (STB, $\overline{CE}$) are tested separately with all device data input pins at V_{CC} -0.4V.
2. Typical ICCOP = 1 mA/MHz of STB cycle time. (Example: 5MHz µP, ALE = 1.25MHz, ICCOP = 1.25mA).

Capacitance

T_A = $+25^oC$

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	13	pF	FREQ = 1MHz, all measure-ments are referenced to device GND
C_{OUT}	Output Capacitance	20	pF	

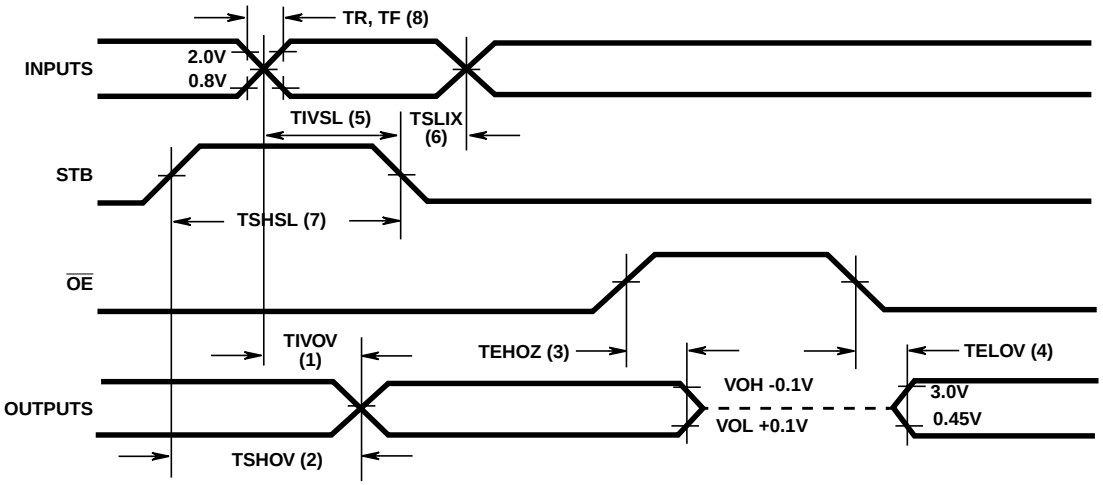
AC Electrical Specifications V_{CC} = 5.0V ±10%; C_L = 300pF (Note 1), FREQ = 1MHz
$T_A = 0^oC$ to $+70^oC$ (C82C83H);
$T_A = -40^oC$ to $+85^oC$ (I82C83H);
$T_A = -55^oC$ to $+125^oC$ (M82C83H)

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
(1) TIVOV	Propagation Delay Input to Output	5	25	ns	See Notes 2, 3
(2) TSHOV	Propagation Delay STB to Output	10	50	ns	See Notes 2, 3
(3) TEHOZ	Output Disable Time	5	22	ns	See Notes 2, 3
(4) TELOV	Output Enable Time	10	45	ns	See Notes 2, 3
(5) TIVSL	Input to STB Set Up Time	0	-	ns	See Notes 2, 3
(6) TSLIX	Input to STB Hold Time	30	-	ns	See Notes 2, 3
(7) TSHSL	STB High Time	15	-	ns	See Notes 2, 3
(8) TR, TF	Input Rise/Fall Times	-	20	ns	See Notes 2, 3

NOTES:

1. Output load capacitance is rated 300pF for both ceramic and plastic packages.
2. All AC Parameters tested as per test load circuits. Input rise and tall times are driven at 1ns/V.
3. Input test signals must switch between V_{IL} -0.4V and V_{IH} +0.4V.

Timing Waveforms



All Timing measurements are made at 1.5V unless otherwise noted.

FIGURE 4. TIMING WAVEFORMS

Test Load Circuits

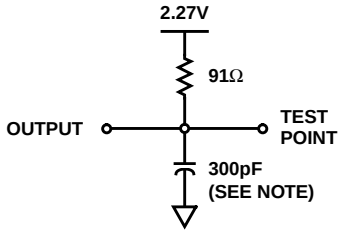


FIGURE 5. TIVOV, TSHOV

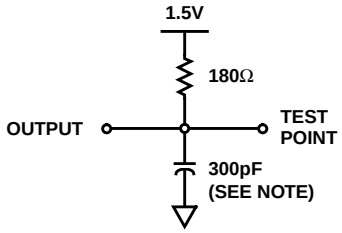
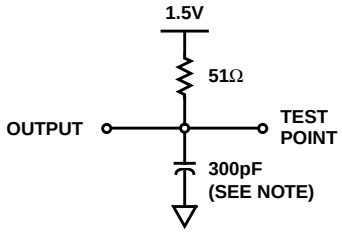


FIGURE 6. TELOV OUTPUT HIGH ENABLE

Test Load Circuits (Continued)



NOTE: Includes jig and stray capacitance.

FIGURE 7. TELOV OUTPUT LOW ENABLE

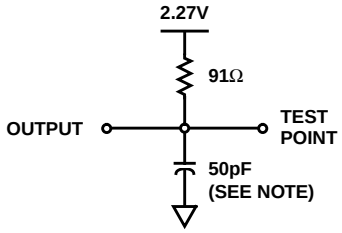


FIGURE 8. TEHOZ OUTPUT LOW/HIGH DISABLE

Burn-In Circuits

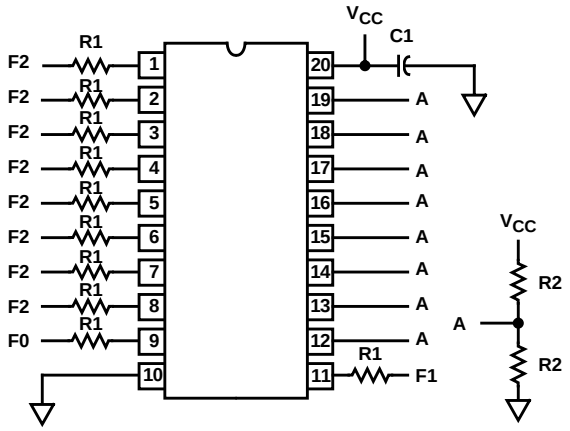


FIGURE 9. MD82C83H CERDIP

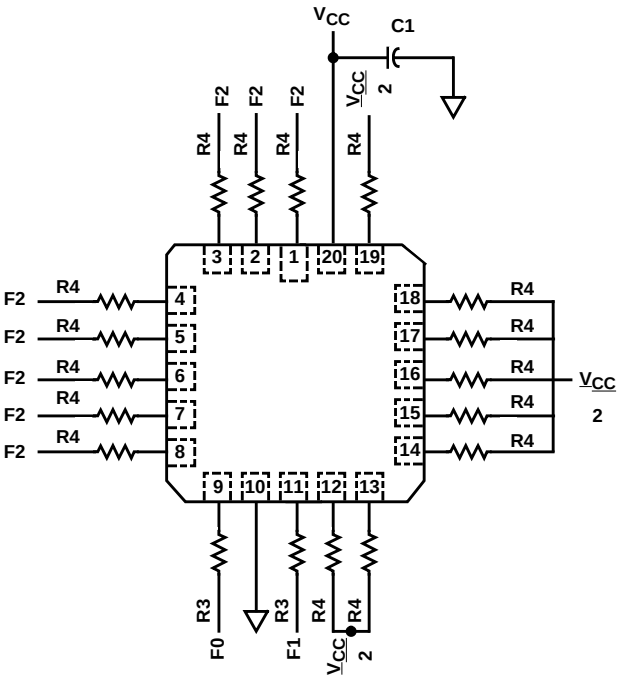


FIGURE 10. MR82C83H CLCC

NOTES:

1. V_{CC} = 5.5V ± 0.5V GND = 0V
2. V_{IH} = 4.5V ± 10%
3. V_{IL} = -0.2 to 0.4V
4. R1 = 47kW ± 5%
5. R2 = 2.0kW ± 5%
6. R3 = 1.0kW ± 5%
7. R4 = 5.0kW ± 5%
8. C1 = 0.01µF Minimum
9. F0 = 100kHz ± 10%
10. F1 = F0/2, F2 = F1/2, F3 = F2/2

Die Characteristics

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1 mils

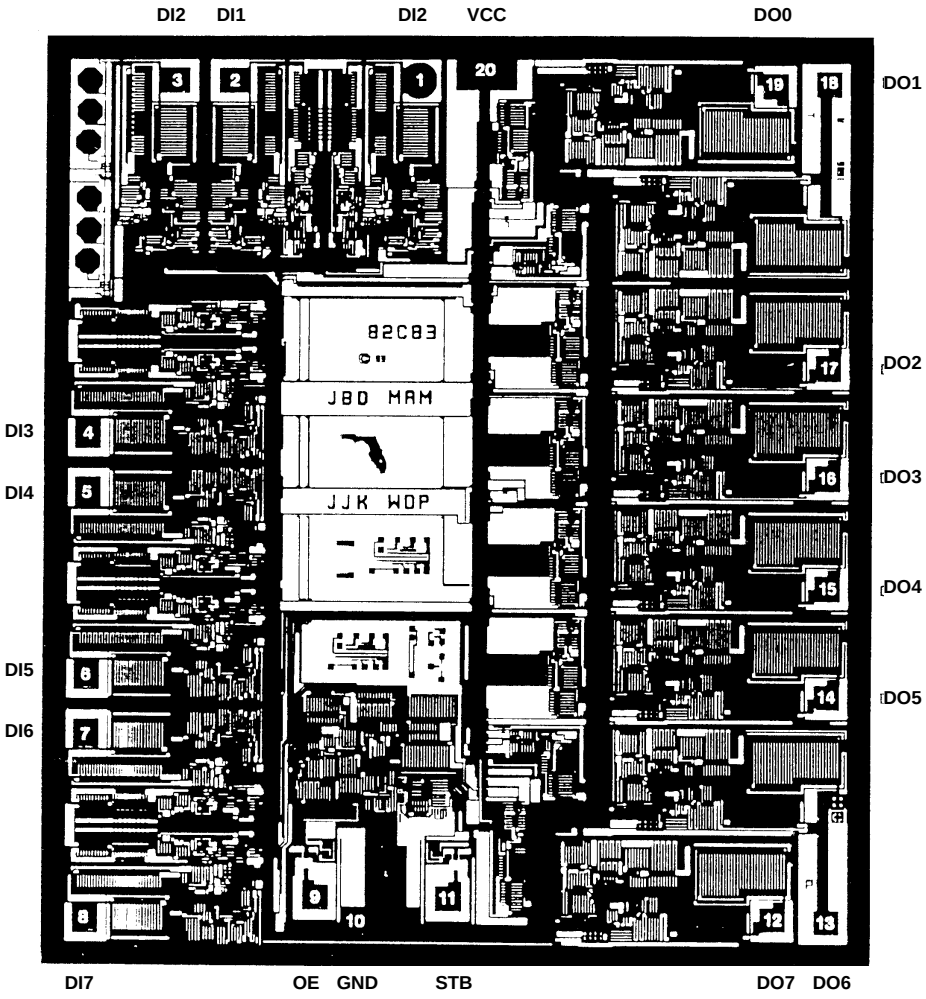
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2

Metallization Mask Layout

82C83H



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