Circuit Considerations In Imaging Applications (HA-2546, HA-5020, HA-5033, HI-5700)

Application Note | November 1996 | AN9313.1

Introduction

Present day image-processing systems perform many functions such as low pass filtering and pattern recognition in the digital domain. However, as shown in the block diagram, the analog input signal must first pass through some signal conditioning and then be digitized by an A/D before it can be manipulated by the Digital Signal Processing (DSP).

It is these front end components that will set the overall dynamic range and resolution of the system and hence the detail that can be resolved in the image. This note will describe the considerations involved in designing and testing the performance of this part of the system.

Video Format

RS-170 is a standard video format for monochrome television. It was later updated to RS-170A by NTSC to cover the requirements for color television broadcasting in the U.S. The FCC has control over broadcast video standards; but, since imaging processing systems are self contained, they do not have to follow a particular standard. For example, color cameras might provide three RGB outputs (component video) or a composite NTSC color signal. System synchronization schemes could also vary greatly.

A typical RS-170 image, or frame, is made up of two interlaced fields. The first field scanned represents the odd numbered lines; the second is the even numbered lines. A total of 525 lines per frame will be scanned in 1/30 of a second with 485 lines being visible. The number of active elements per line, or pixels, varies from system to system depending on the desired resolution.

The RS-170 monochrome composite video signal is shown in Figure 1. System timing is controlled by vertical and horizontal sync pulses. Horizontal sync controls the line by line timing and occurs during the 10.9µs blanking period. Vertical sync controls the field timing and occurs at 1/60 of a second rate. The brightness information for the video image is transmitted during the active line time and will vary from the reference black level (7.5 IRE) to the reference white level (100 IRE).

RS-170 normally has an aspect ratio of 4:3. However, because of frame buffer memory and DSP requirements many image-processing applications will use a 1:1 aspect ratio. Figure 2 depicts the resulting picture and timing requirements for a RS-170 video with a 1:1 aspect ratio. The active line time is 39.44µs centered with 6.575µs of “inactive” time on either side. Notice that for 512 active pixels per line and 485 lines one frame of digitized video information will fit into 248,320 of memory.

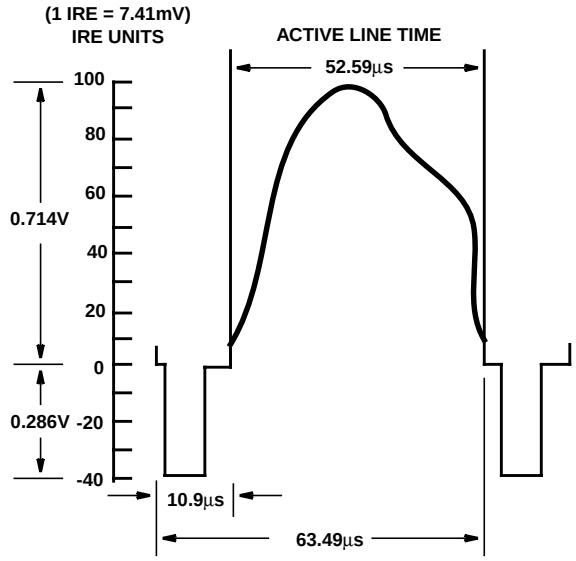
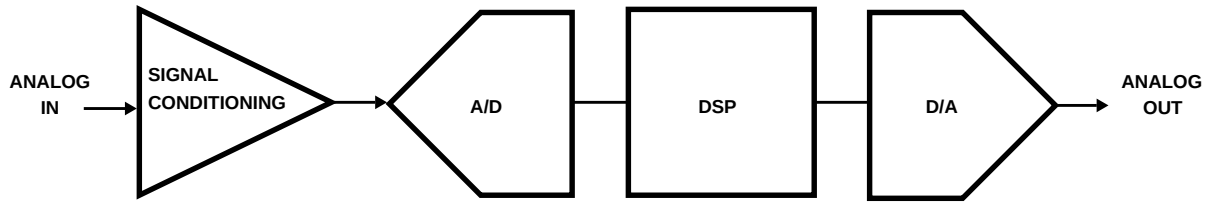


FIGURE 1. STANDARD RS-170 COMPOSITE VIDEO SIGNAL

Imaging System Block Diagram



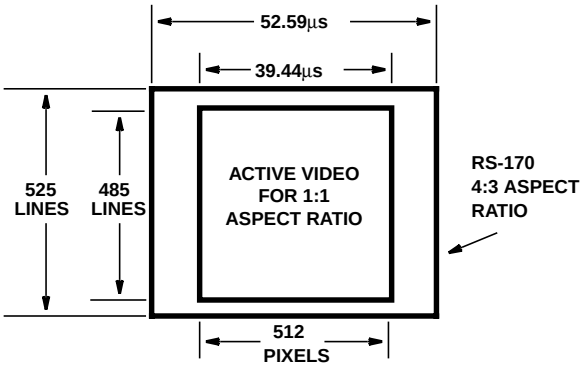


FIGURE 2. MODIFIED RS-170 VIDEO

Circuit Design Considerations

The analog waveforms seen by the signal conditioning front end to an image-processing system can be classified as small signal or large signal. The appropriate analysis should be used in each case. A good rule of thumb is to say any signal of less then a $1V_{P-P}$, like RS-170 video, should be considered as small signal.

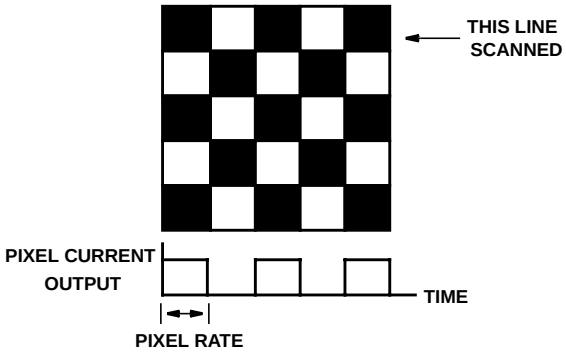


FIGURE 3. VIDEO

Figure 3 is an example of a worst case light pattern that might be seen by a small section of a Charge Coupled Device (CCD) array inside a video camera. Each square represents an individual pixel. The rate at which these pixels are scanned will determine the bandwidth requirements. If it takes 39.44ms to scan the 512 active pixels, then the pixel clock rate would be 12,981,174 elements per second. The video signal is a square-wave with a fundamental at half the pixel rate of 12,981,174/2 or 6.4MHz. To pass this signal undistorted would require a great deal of small signal bandwidth however, a bandwidth of 4MHz has been found to be adequate for video.

Insufficient high frequency response and phase distortion of a video signal will result in blurring of the fine detail in a picture and the overall image will look darker than normal. Therefore, the first requirement for the signal conditioning circuit is that its small signal bandwidth needs to be considerably wider than the bandwidth of the incoming video. This will ensure a constant gain over the frequency band of interest and avoid a loss of dynamic range as the input to the A/D rolls off.

The second requirement is that the system should have zero phase shift over its entire frequency range. Because this is impractical, a realistic goal is a phase shift that is proportional to frequency. That is, the second harmonic should be delayed twice as much as the fundamental, the third three times as much, and so on. When this occurs all the frequency components will end up having the same amount of time delay resulting in a image that is only delayed slightly in time and can easily be adjusted for.

For a single pole system, the attenuation factor and phase shift at a particular frequency relative to the f_{-3dB} can be calculated from:

$$A(f) = \frac{1}{\sqrt{1 + \left(\frac{f}{f_{-3dB}}\right)^2}} \quad \text{(EQ. 1)}$$

and

$$\theta(f) = \operatorname{atan}\left(\frac{f}{f_{-3dB}}\right) \quad \text{(EQ. 2)}$$

Taking these error terms into account, the complete equation for a sinewave including the effects of the system would now be:

$$V(t) = \frac{A}{\sqrt{1 + \left(\frac{f}{f_{-3dB}}\right)^2}} \times \sin\left(\omega t + \operatorname{atan}\left(\frac{f}{f_{-3dB}}\right)\right) \quad \text{(EQ. 3)}$$

In Equation 1, when f equals 4MHz and the attenuation A(f) is one 8-bit LSB (0.4%) the required small signal bandwidth f_{3dB} would be 40MHz. The corresponding phase shift at 4MHz from equation 2 would be 5.7 degrees.

By the time the video has reached the input to the A/D it has been amplified enough so that large signal parameters such as slew rate and full power bandwidth (FPBW) have to be considered. The required slew rate can be found by taking a conservative approach and forcing the video signal to slew through its range in 25% of the pixel clock. Therefore, if the pixel clock is 12.98MHz (pixel time is 77ns) and the reference for the A/D is 4V, then the minimum slew rate required would be:

$$SR_{MIN} = \frac{4V}{0.25 \times 77ns} = 208\frac{V}{\mu s} \quad \text{(EQ. 4)}$$

Now that the slew rate has been determined the minimum required full power bandwidth of the signal conditioning block and the converter can be calculated from:

$$FPBW = \frac{SR_{MIN}}{2 \times \pi \times V} = \frac{208}{2 \times \pi \times 4} = 8.3MHz \quad \text{(EQ. 5)}$$

Trying to relate the above equation for FPBW to the FPBW quoted for a converter should be done with caution by the user and requires a knowledge of the way it has been defined by the A/D manufacturer. One method used will test for the presence of sparkle codes. These are anomalous codes that show up when the input slew rate exceeds a certain value. The term sparkle code comes from the fact they will cause bright pixels in a video display.

Figure 4 is a plot of a sinewave input to a converter that has been digitally reconstructed and shows evidence of sparkle codes. The FPBW is then determined from the maximum fullscale input frequency that has sparkle free performance.

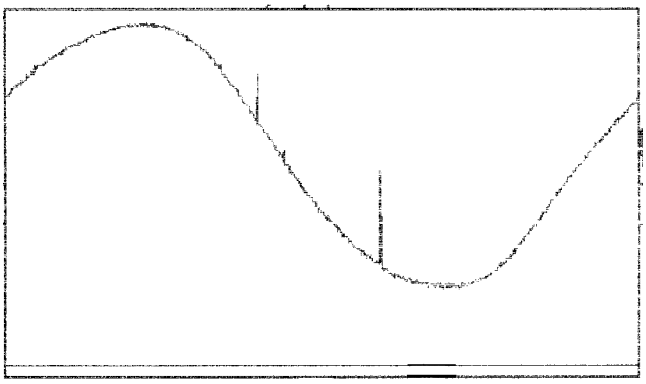


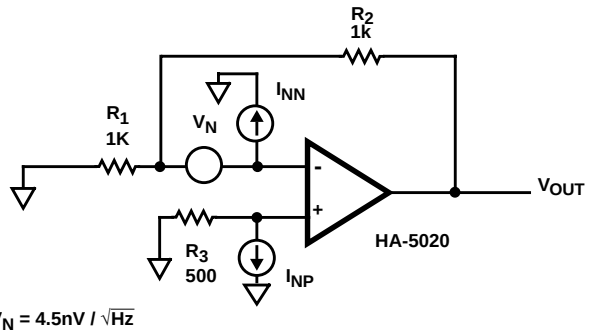
FIGURE 4. RECONSTRUCTED SINEWAVE

Some manufacturers will quote FPBW as the point in the frequency domain where the fundamental is 3dB down from the low frequency value. This method will tend to average out sparkle codes. Other A/Ds will have the FPBW specified as the point where a reconstructed sinewave in the time domain is 3dB down from the low frequency value. The user must determine if the test method used by the manufacturer to determine the quoted FPBW will ensure accurate sparkle free performance at their operating frequencies.

Sparkle codes can also occur if the maximum conversion rate of the A/D is exceeded. For example, the HI-5700 is an 8-bit CMOS flash converter that has datasheet limit for conversion rate of 20MHz. However, as is the case for many flash converters, by skewing the duty cycle of the sampling clock the part can be made to operate at 25MHz and higher.

The theoretical best dynamic range that can be expected from an A/D with n bits of resolution can be calculated from: $DR(dB) = 20 \log (2^n) = 6.02(n)$. An image-processing system would be expected to have a dynamic range of at least 36dB or about 6 bits.

In order to make use of the full dynamic range available from the converter, the overall system noise should be less than the theoretical quantization noise of the converter $q/(\sqrt{12})$ (q is the A/D lsb size). Figure 5 is a typical voltage feedback or current feedback op amp circuit that will be used to illustrate some basic noise calculations. The voltage noise (V_N) and noise current (I_N) sources have been modeled, but the Johnson noise of the resistors will be neglected because of the low resistor values normally used in high-speed circuits.



$V_N = 4.5nV / \sqrt{Hz}$

$I_{NN} = 25pA / \sqrt{Hz}$; $I_{NP} = 2.5pA / \sqrt{Hz}$

FIGURE 5. OP AMP NOISE MODEL

The equation for the total RMS noise over the bandwidth of interest is:

$$V_{TOT} = \sqrt{1.57 \times f_{BW}} \times \quad \text{(EQ. 6)}$$

$$\sqrt{(V_N)^2 \times \left(1 + \frac{R_2}{R_1}\right)^2 + (R_2)^2 \times (I_{NN})^2 + (R_3)^2 \times (I_{NP})^2 \times \left(1 + \frac{R_2}{R_1}\right)^2} \quad \text{(EQ. 7)}$$

Where:

V_{TOT} is the total RMS noise voltage.

R_1 is the feedforward resistor.

R_2 is the feedback resistor.

R_3 is the noninverting input resistor.

V_N is input voltage noise spectral density.

I_{NN} is the inverting input current noise spectral density.

I_{NP} is the noninverting input current noise spectral density.

f_{BW} is the bandwidth over the region of interest.

As is normal for current feedback op amps, the HA-5020 has unequal I_{NN} and I_{NP}.

For the values given in the figure over the 18MHz FPBW specified for the HI-5700 8-bit flash A/D the RMS noise V_{TOT} is found to be equal to 106mV. The peak noise value will be about five times this value or 530mV. This is significantly less than the 4.5mV of quantization noise for an 8-bit ADC with a 4V range.

This example has shown how to model the noise of a opamp. If there are other noise sources present, then the total noise can be found by taking the RMS sum of all the individual noise sources.

A wide dynamic range is usually required of a signal conditioning block to accommodate large incoming signal variations. Automatic Gain Control (AGC) will compensate for these variations and allow the user to design with a lower resolution A/D.

The AGC circuit should be considered a control loop, and its frequency and phase characteristics plotted. A slow AGC loop could compensate for slow offset or gain changes over temperature while a faster AGC loop could compensate for signal overload conditions.

There are a number of opinions on where the AGC should be applied. An easy way to do it is to vary the reference on the A/D depending on signal strength. This will work fine if the converter has been thoroughly characterized over the range of reference voltages it will see. Unfortunately this is usually not the case. Most datasheets will not specify the performance of the converter versus reference voltage. Therefore, the user is taking a significant chance that the part performance will stay the same over the life of the system for various manufacturing lots of the A/D. The second option is to let the AGC vary the gain of the signal conditioning circuitry while leaving the reference to the A/D at the value where the performance is guaranteed by the datasheet. This approach will guarantee the long term success of a circuit. The design section of this note will discuss a technique using a multiplier chip to accomplish this.

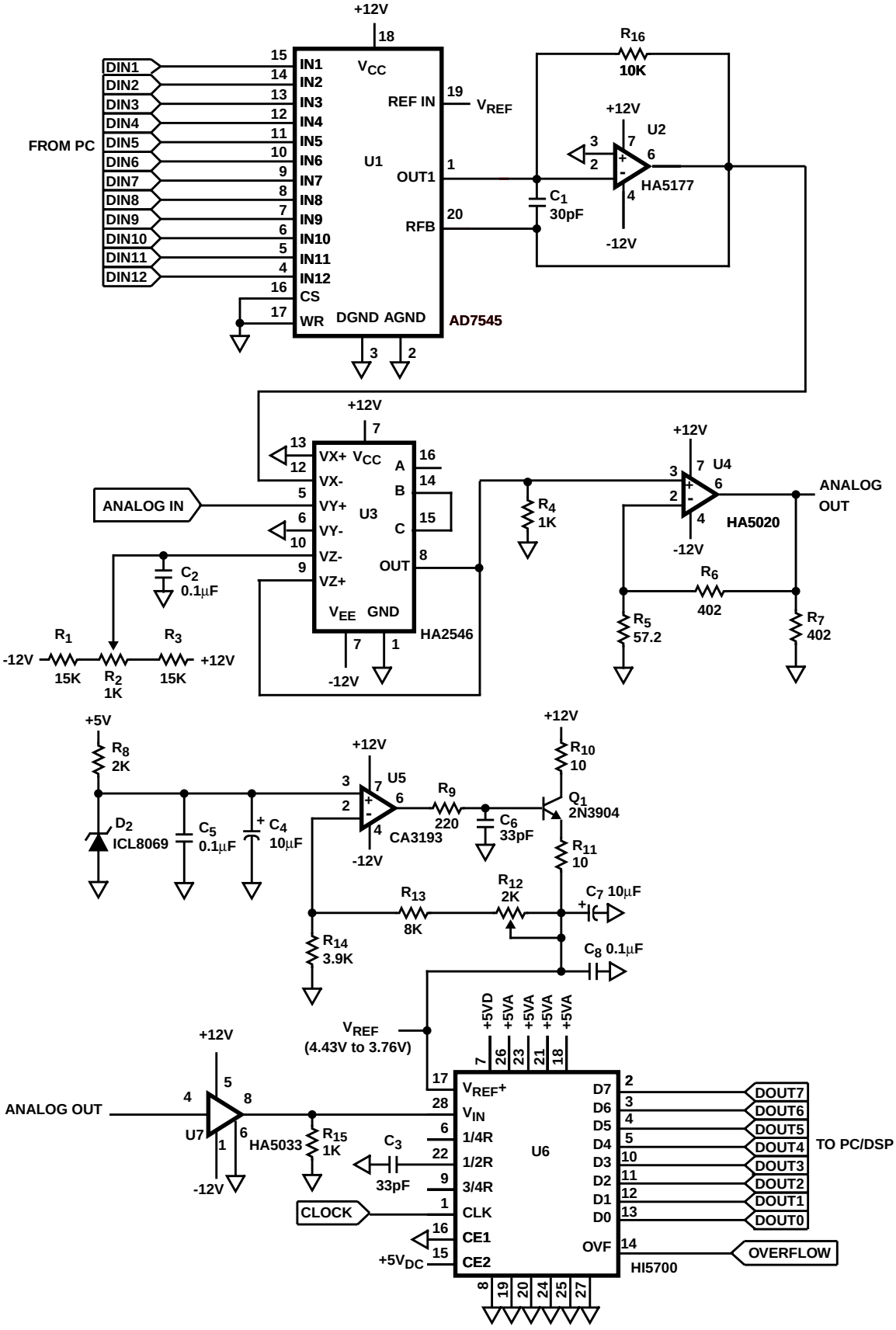


FIGURE 6. DESIGN FOR VIDEO IMAGING FRONT END

System Design

Figure 6 is a design for a signal conditioning and A/D front end to an image-processing system. The video input to the system will be assumed to have a positive picture phase. That is, the blanking and sync pulses will be the most negative portion of the video waveform. When the video is ac coupled, the black reference level has to be reinserted prior to the A/D. If this is not done, then, as the amplitude of the video signal is reduced, due to a reduced contrast image, the blanking level moves more positive. The resulting image will now appear a light shade of gray, rather than the preferred black level. Also, the DSP becomes more sensitive to coupled noise and may for example, during edge detect, show an edge where none exists.

Figure 7 is a simple circuit to DC restore the video. This circuit clamps the most negative point of the signal to -0.7V which can now be offset by the HA-2546 to provide a stable black level during changing contrast. Another 8-bit 20 MSPS converter from Intersil Corporation, the HI1176, has an internal circuit which will clamp the back porch of a video signal to a voltage input on the reference pin.

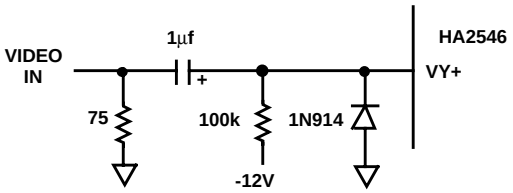


FIGURE 7. DC RESTORE CIRCUIT

The HA-2546 is a wideband two quadrant analog multiplier which makes the implementation of AGC offset and gain correction easy. It is configured in this design to give the transfer function:

$$V_{OUT} = \frac{(V_X \times V_Y)}{2} - V_Z \quad \text{(EQ. 8)}$$

The V_Z pin can be used to correct for system offset as long as it does not exceed ±5V. The initial offset adjustment is set by pot R_2. The V_X pin can be used to adjust system gain.

U5 is part of a reference circuit in Figure 6 that provides the 4V reference required by the A/D and the DAC. It is capable of 8-bit performance over the industrial temperature range. Pot R_{12} will set the initial overall system gain.

For the reasons outlined above, it was decided to leave the reference to the flash at its nominal datasheet value and let the AGC adjust the gain of the signal conditioning components prior to the converter. A AD7545 12-bit DAC is used as part of a slow AGC loop which uses the V_X pin of the HA-2546 to control the gain of the system.

As illustrated in Figure 8, the feedback loop could be closed by a microprocessor using the overflow bit on the HI-5700 and could compensate for light intensity shifts or temperature drift. In order to avoid any glitches the DAC should be updated during the vertical retrace period.

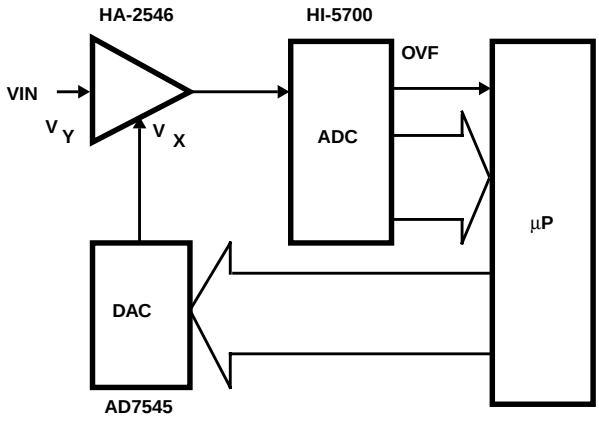


FIGURE 8. SLOW AGC LOOP

The HA-5177 op amp acts as an I/V converter for the DAC. Its feedback is set so that at all ones to the DAC the output voltage will be -2V which is the maximum voltage that is allowed on the V_X pin. At the normal operating point for the system the DAC will be at midscale and the overall system gain will result in a full scale swing to the A/D. Since the DAC is at midscale the system has an equal amount of gain correction range up and down.

The HA-5020 is a high-speed current feedback op amp which provides additional gain so that a nominal $1V_{P-P}$ signal input to the system the HI-5700 flash will see its full 0V to 4V swing. If the sync has been stripped from the video before it is digitized [8], then the gain could be adjusted so that the video reference black to reference white level will span the full range of the converter.

A high-speed unity gain op amp (HA-5033) buffers the input to the HI-5700 and provides the necessary low output impedance over frequency required by flash converters. Although the HA-5020 can drive the HI-5700 directly, the HA-5033 has superior current drive, lower output impedance, and better bandwidth.

The pixel clock of 12.98MHz will usually determine the minimum sampling rate of the A/D. In order to relax the filter requirements on the front end to the system the actual sampling rate used in this note is 15MHz. This will be more than adequate to cover all established sampling rates specified for the various published standards.

Additional timing circuitry might be added to gate the pixel clock so that it is only on during the active line period thereby conserving frame buffer memory size. If the system uses an interlaced video format then the circuitry could also define the even and odd fields of the image frame and update the memory accordingly.

The clock period for the HI-5700 8-bit flash is made up of an autozero time and sample time. It was found that the autozero time can be reduced down to as little as 15ns while the sampling time must remain at 24ns or greater. This timing allows the sparkle free operation of the circuit at pixel rates up to 25MHz.

There are many considerations which have to be taken into account when using high speed converters. These involve board layout, choosing the right op amp to drive the input, and designing a low drift reference. Refer to references 6 and 7 for a complete discussion of these topics and others.

Test Results

The IEEE has various standards which address the type of tests that need to be done on a broadcast video system to verify the performance of a video A/D and D/A combination (codec). Among them are DC linearity, Signal-To-Noise Ratio (SNR), bandwidth, and differential phase and gain. Since this note deals only with RS-170 monochrome video signals, the tests that deal with the color information, such as differential phase and gain, are not applicable. Also, adding a DAC on the output of the converter in order to use the IEEE test methods would tend to cloud its overall performance of the system with the errors of the DAC. Therefore, the system will be evaluated using a set of tests that are similar to those recommended by the IEEE but are done by analyzing the digital data out of the converter. These tests can also be found on a datasheet for a typical flash A/D. Hopefully, as a result of this approach the user will now also be able to more intelligently read and compare converter datasheets.

There is a great deal of information in the low frequency (30Hz) content of video. Historically, the low frequency performance of an A/D has been evaluated by the Differential (DNL) and Integral (INL) NonLinearity specs. DNL is a measure of the deviation of the code widths from the ideal value of one Least Significant Bit (LSB). INL is the deviation of the code edges from the ideal transfer curve of the A/D. Since the A/D in this system is initially calibrated for offset and gain, the line used as a reference will be one drawn through the first and last transition point.

The DNL and INL errors can not be calibrated out and is the best accuracy that can be expected of the system. Therefore, the INL error should ideally not exceed 1/2 LSB so that when it is combined with the inherent 1/2 LSB quantizing error of an A/D the total error would not exceed 1 LSB. A DNL error of more than -1 LSB means a code is missing from the transfer curve. An INL error of 1/2 LSB will ensure a DNL error of at most 1 LSB.

Figure 9 shows a plot for the transfer function of a converter with DNL and INL errors. The reference curve and the ideal transitions are pointed out. Transition point 3 is offset in the negative direction by 1/2 LSB therefore the ILE at this point is -1/2 LSB. The ILE of all the other transitions is zero. The DLE of code 2 is -1/2 LSB and the DLE of code 3 is +1/2 LSB.

The actual linearity test was done using a histogram approach. A triangle wave is input to the system and the number of occurrences of each code is kept track of. DNL error is then calculated in LSBs from:

$$DNL(i) = \frac{(P_m(i))}{(P_i(i))} - 1 \qquad \text{(EQ. 9)}$$

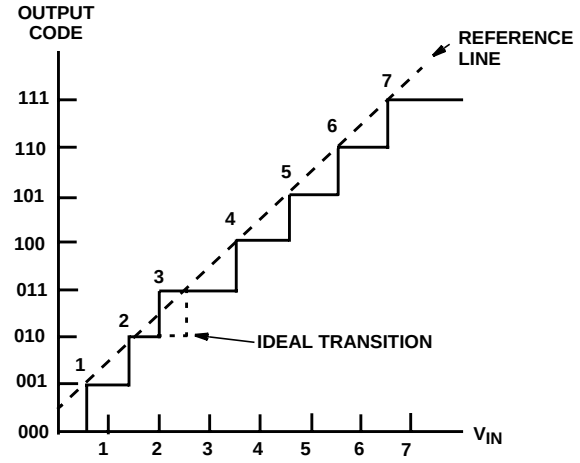


FIGURE 9. A/D TRANSFER FUNCTION

The ideal probability, P_i is a constant and is equal to the average of the number of counts per code divided by the total number of samples. P_m is the measured probability and is equal to the total number of counts for a particular code divided by the total number of samples. Once the DNL error has been determined the INL error is calculated from the sum of the DLE errors.

A histogram was done on the design discussed in this note by inputting a $1V_{P-P}$ 5kHz triangle wave, encoding the HI5700 at 15MHz, and capturing the digital data. Figure 10 and Figure 11 are plots of the DNL and INL error for the total system indicating an accuracy of better than 7 bits with no missing codes.

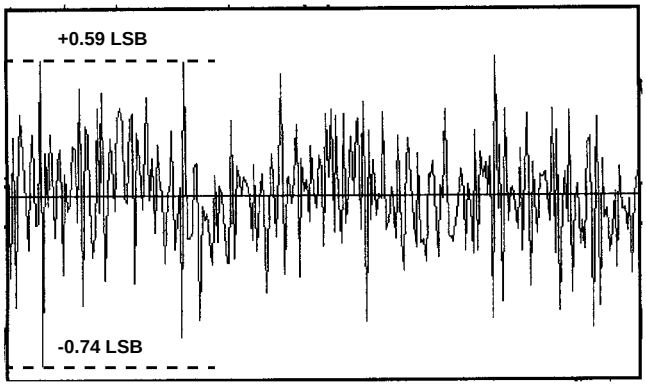


FIGURE 10. DIFFERENTIAL LINEARITY ERROR vs CODE

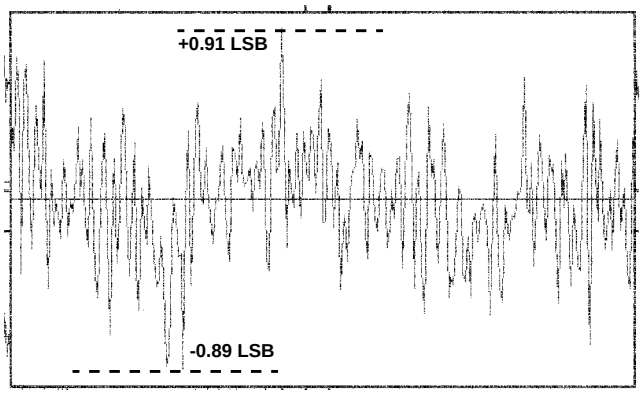


FIGURE 11. INTEGRAL LINEARITY ERROR vs CODE

Due to various dynamic effects such as slew rate limiting and bandwidth rolloff the static DNL and INL will degrade as the input frequency approaches the 4MHz bandwidth requirement of video. DNL will show up as an increase in the quantization noise which will tend to elevate the noise floor of the A/D. INL is a bend in the transfer curve of the converter and will generate harmonics. Both result in a loss of dynamic range of the system.These effects are usually evaluated in the frequency domain by finding the SIgnal-to-Noise-And-Distortion (SINAD) in dB.

The SINAD test requires performing a fourier transform on the data obtained by sampling a continuous time input waveform. The Discrete Fourier Transform (DFT) can be thought of as a frequency selective filter that calculates the RMS voltage at a particular frequency and will work for any number of samples.

The coefficient for a particular frequency can be found from:

$$X_d(k) = \sum_{n=0}^{N-1} x(n) \times e^{-j2\pi k(n/N)} \quad \text{(EQ. 10)}$$

N is the number of samples.

n is the time sample index (n = 0, 1, 2, ... , N-1).

k is the index for the computed frequency components (k=0, 1, 2,...,N-1).

The Fast Fourier Transform (FFT) is an algorithm that will compute all the DFT coefficients at one time; but, unlike the DFT it will only work for sample sizes that are a power of two. The FFT will output the coefficients for N/2 discrete frequency bins that will have a resolution of F_{sample}/N.

Once the FFT has been performed SINAD can be calculated from:

$$SINAD_{dB} = 20 \times \log\left(\frac{RMS_{SIGNAL}}{RMS_{NOISE}}\right) \quad \text{(EQ. 11)}$$

Where RMS_{SIGNAL} is the measured RMS signal in the fundamental bin and RMS_{NOISE} is the sum of all other spectral components below the Nyquist frequency excluding DC. It is important that the distortion components be included in this calculation in order to take into account all the system errors.

The Effective Number Of Bits (ENOB) of the system can be found by:

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} \quad \text{(EQ. 12)}$$

ENOB is a global indication of the accuracy of the system and, along with INL and DNL will degrade as the input frequency is increased. The low DNL and INL errors indicate the excellent low frequency performance of the design. This was again verified by inputting a $1V_{P-P}$ sinewave at 20kHz, encoding the part at 15MHz, and performing an FFT on the data. The SINAD was calculated to be 44.5dB for an ENOB of 7.1 bits. An indication of the overall low noise in the system.

The high frequency performance of the system was evaluated by changing the input frequency to 4MHz and again performing an FFT. Figure 12 is a spectrum plot of the system output. The SINAD for this plot was determined to be 38.2dB for an ENOB of 6.05 bits.

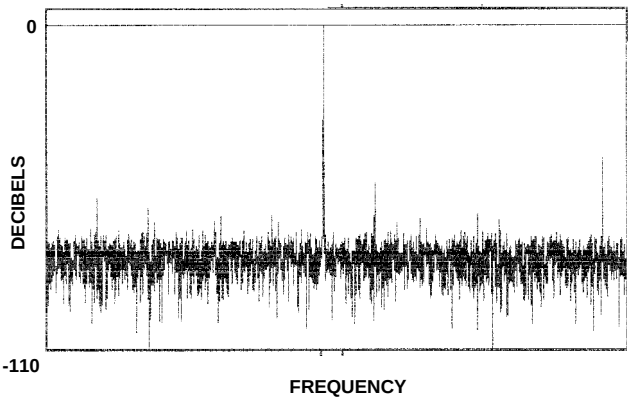


FIGURE 12. HIGH FREQUENCY SPECTRAL PLOT OF SYSTEM (f_I = 4MHz)

The full power bandwidth and slew rate capability of the system was checked by inputting a fullscale sinewave at 8MHz and sampling it at a 15MHz rate. Figure 13 shows the resulting reconstructed waveform. Notice the lack of distortion and sparkle codes.

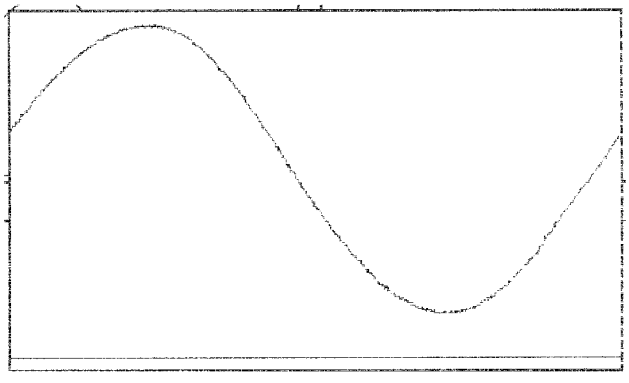


FIGURE 13. RECONSTRUCTED SINEWAVE (f_I = 8MHz)

Time Division Multiplexed Systems

This note is mainly concerned with RS-170 type video signals. However, it is instructive to briefly discuss the factors to consider when dealing with other time division multiplexed signals that might be seen from some types of CCD arrays, a multiplexed input, or an infrared sensor array.

The output of CCD arrays many times will have the signal of interest riding on a large DC offset. Figure 14 is an example of an inverting buffer that can be used to remove large offsets. Notice that since resistor R_3 sees a virtual ground Voffset can take on a value much higher than the supply voltage.

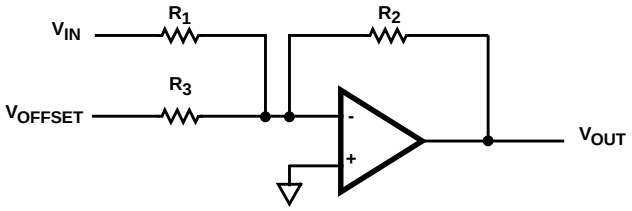


FIGURE 14. INVERTING BUFFER

The circuit gain can be calculated from:

$$V_{OUT} = (-R_2/R_1) \times V_{IN} - (R_2/R_3) \times V_{OFFSET} \quad \text{(EQ. 13)}$$

The circuits that process large signal pulse type waveforms must slew and settle quickly so, as depicted in Figure 15, the A/D can then accurately digitize the pixel information. Given the ever increasing pixel rates this can become quite a challenge.

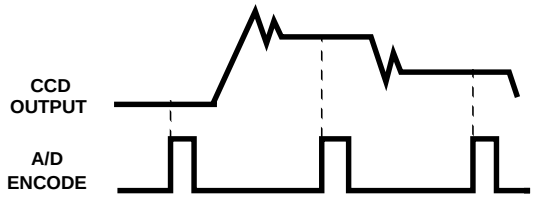


FIGURE 15. TIME DIVISION MULTIPLEXED SIGNAL

The overall system settling time is made up of two parts. Initially the signal must slew until it enters a region where small signal analysis takes over. Similar slew rate requirements as discussed in the design considerations section apply in this case also. For a single pole system, the error will then decay with a time constant determined by the small signal bandwidth of the system. The settling time in an actual system is very much a function of the circuit parasitics and the overall frequency response of the circuit. As such, it is difficult to calculate an accurate number beforehand. Reference 2 has a more thorough discussion of settling time and the calculations involved.

Additional large signal time domain converter specifications such as overvoltage recovery time and transient response time become important in these types of applications. As in the case of full power bandwidth, there are many ways to define these tests so be aware of the method used on the datasheet and how it applies to a particular application.

Once the circuits have settled then the A/D must digitize the level it sees at its input. The accuracy with which this can be done is a function dynamic range of the system and will be determined by the low frequency accuracy of the converter, the noise generated in the signal conditioning circuits, and the noise added by the converter. The INL, DNL, and low frequency SINAD specifications can be used to predict performance of the system with a particular converter.

The HI5800 is a low noise 12-bit 3 MSPS converter that is perfect for the applications which require a higher dynamic range at slower pixel rates. It is a complete sampling converter with on board sample and hold and reference. The low frequency (20kHz input) SINAD of typically 70dB reflects its outstanding low noise performance. The high frequency (1MHz input) SINAD number of 68dB illustrates how the performance is maintained at higher input frequencies.

Conclusion

This note has discussed the various considerations involved in designing the analog front end to an image-processing system. A system design was presented and proved to have accurate sparkle free performance at typical video frequencies.The methodology presented could be used to analyze the system requirements for systems with higher pixel rates.

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