CA3126

May 1999

TV Chroma Processor

Features

- **Phase Locked Subcarrier Regeneration Utilizes Sample-and-Hold Techniques**
- **Automatic Chrominance Control (ACC)/Killer Detector Employs Sample-and-Hold Techniques**
- **Supplementary ACC with an Overload Detector to Prevent Oversaturation of this Picture Tube**
- **Sinusoidal Subcarrier Output**
- **Keyed Chroma Output**
- **Emitter Follower Buffered Outputs for Low Output Impedance**
- **Linear DC Saturation Control**

Applications

- **TV/CATV Receiver Circuits**
- **NTSC Color Decoder/Processor**
- **Computer Graphics Subcarrier Regenerator**
- **Timing Reference for Frame Grabbers**
- **DSP Clock Timing Reference Source**

Description

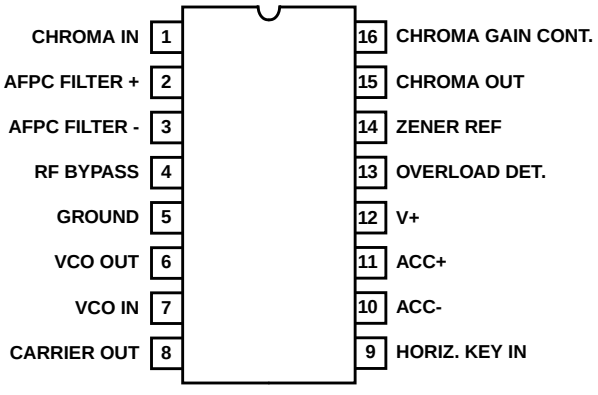
The Harris CA3126 is a monolithic silicon integrated circuit designed for TV chroma processing and is ideally suited for NTSC color graphic applications that require subcarrier regeneration of the color burst signal.

Part Number Information

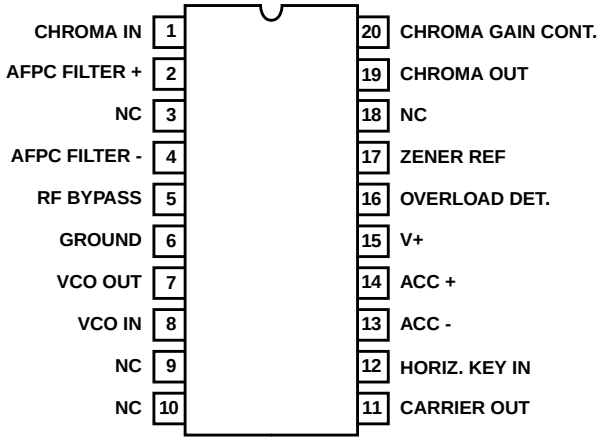
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3126E	-40 to 85	16 Ld PDIP	E16.3
CA3126M1	-40 to 85	20 Ld SOIC	M20.3

Pinouts

CA3126
(PDIP)
TOP VIEW



CA3126
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **860.5**

Absolute Maximum Ratings

DC Supply Voltage (V+ to GND) (Note 1). 13.2V
DC Current:
Into V+ Pin 38mA
Into Zener Reference Pin 20mA
DC Voltage (Horizontal Key In)
Negative Rating . . . . . -5V
Positive Rating 3V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{o}C/W)
PDIP Package 100
SOIC Package 85
Maximum Junction Temperature (Plastic Packages) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

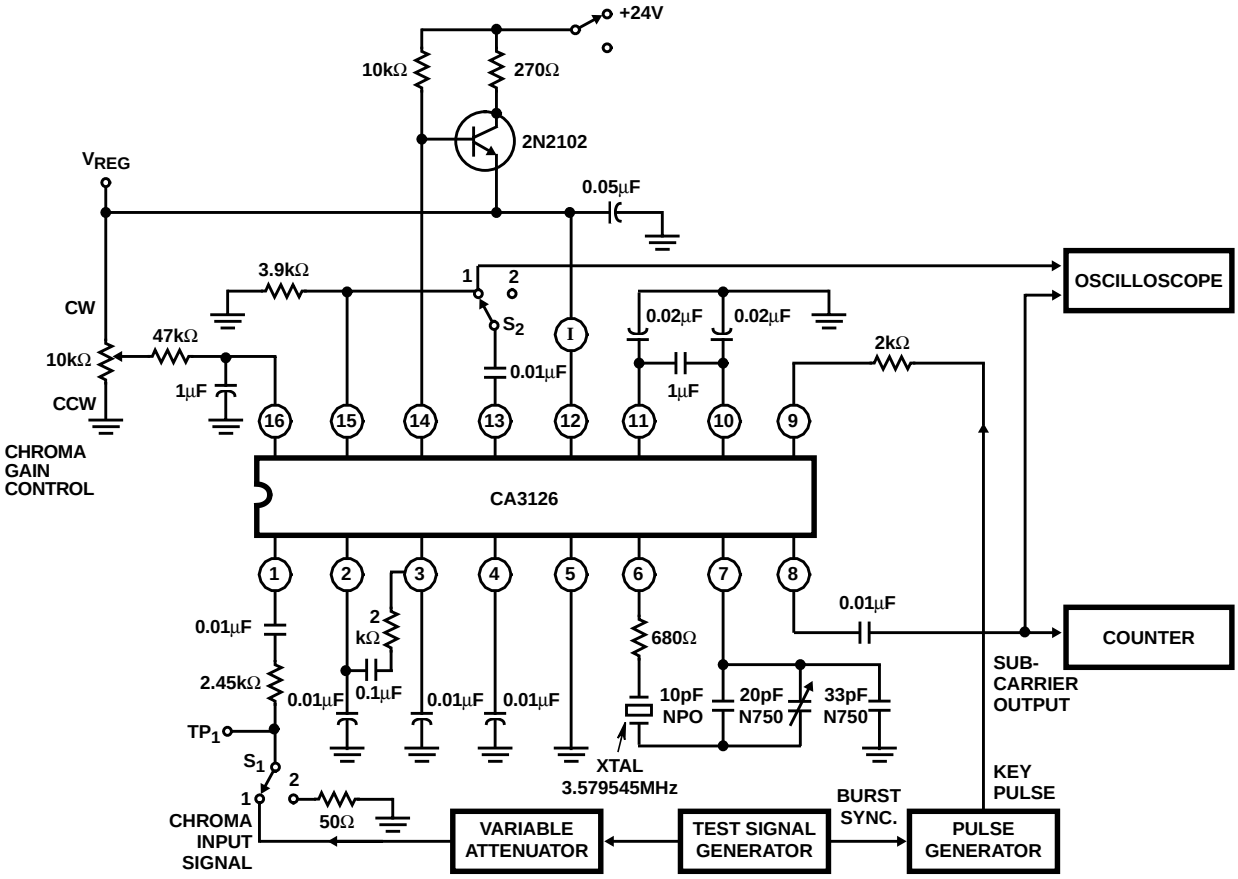
T_A = 25^{o}C, Chroma Gain Control at maximum position for all tests except as noted. Electrical specifications referenced to test circuit.

PARAMETER	TERMINAL, MEASUREMENT AND SYMBOL	SWITCH POS.		V_{CHROMA} INPUT TP_1	MIN	TYP	MAX	UNITS
		S_1	S_2					
DC ELECTRICAL SPECIFICATIONS								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
SWITCHING ELECTRICAL SPECIFICATIONS (Note 3)								
Pull-In Range (Note 4)	V_8	(Note 6)	2	$0.5V_{P-P}$	±250	-	-	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	-	V_{P-P}
100% Chroma Output	V_{15}	1	2	$0.5V_{P-P}$	1.4	2.7	-	V_{P-P}
Overload Detector	V_{15}	1	1	$0.5V_{P-P}$	0.4	-	0.7	V_{P-P}
Minimum Chroma Output (Note 5)	V_{15}	1	2	$0.5V_{P-P}$	-	-	20	mV_{P-P}
200% Chroma Output	V_{15}	1	2	$1V_{P-P}$	70	100	140	% of 100% Reading
20% Chroma Output	V_{15}	1	2	$0.1V_{P-P}$	40	-	105	
Kill Level	V_{TP1}	1	2	Vary	5	-	60	mV_{P-P}

NOTES:

3. Except for pull-in range testing, tune oscillator trimmer capacitor for free running frequency of 3.579545MHz ±10Hz.
4. Set Switch 1 to Position 2, detune oscillator ±250Hz, set Switch 1 to Position 1, and check for oscillator pull-in.
5. Set Chroma Gain Control to minimum position (CCW).

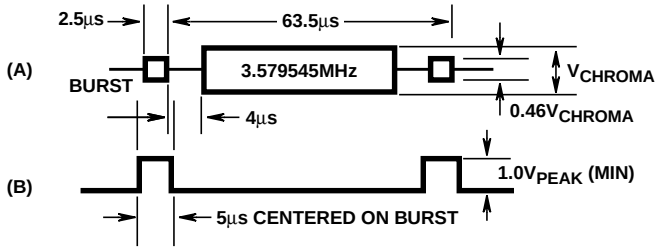
Test Circuit



Pin numbers refer to the PDIP package.

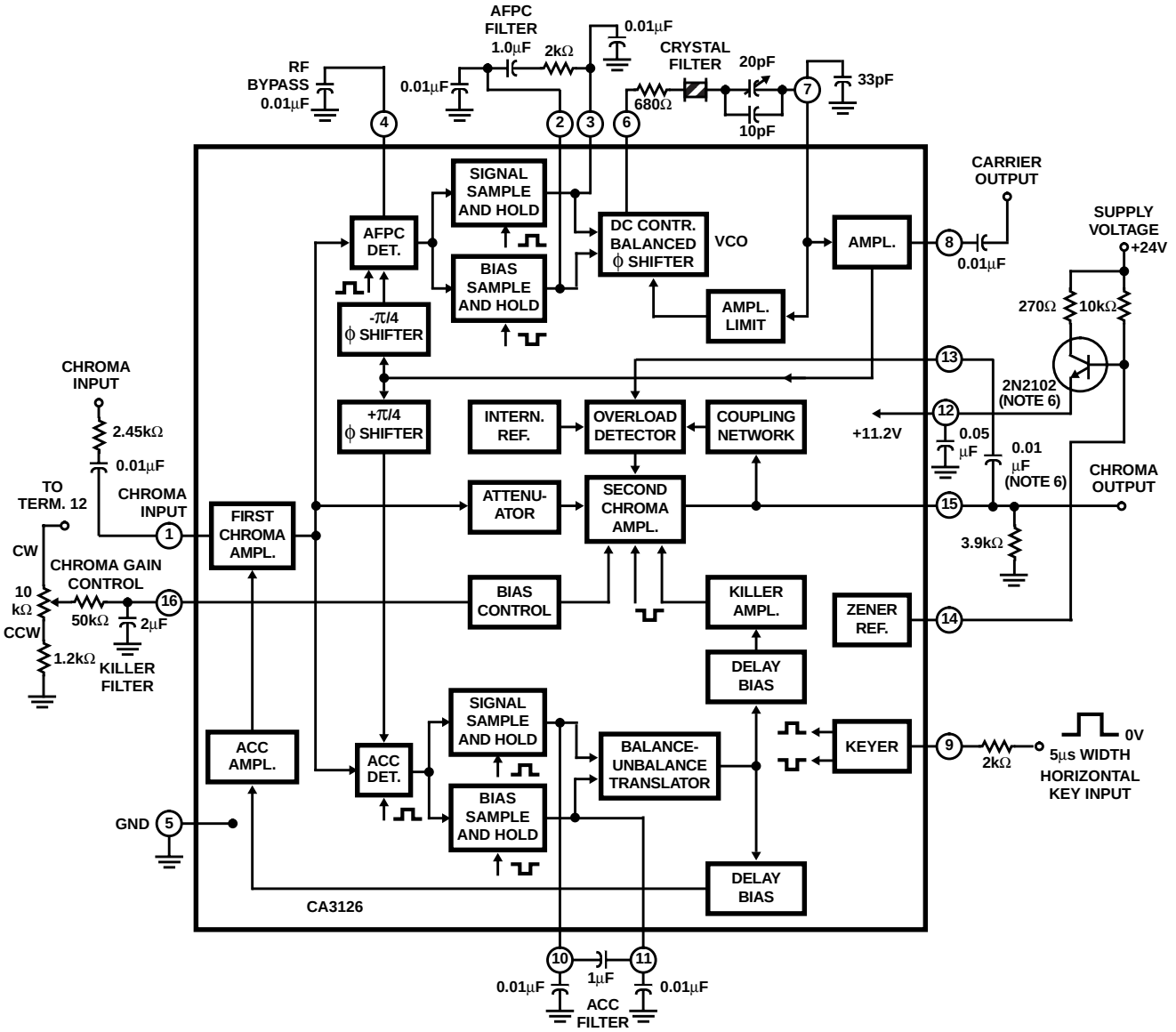
(A) Chroma input signal

(B) Key pulse input signal



Block Diagram

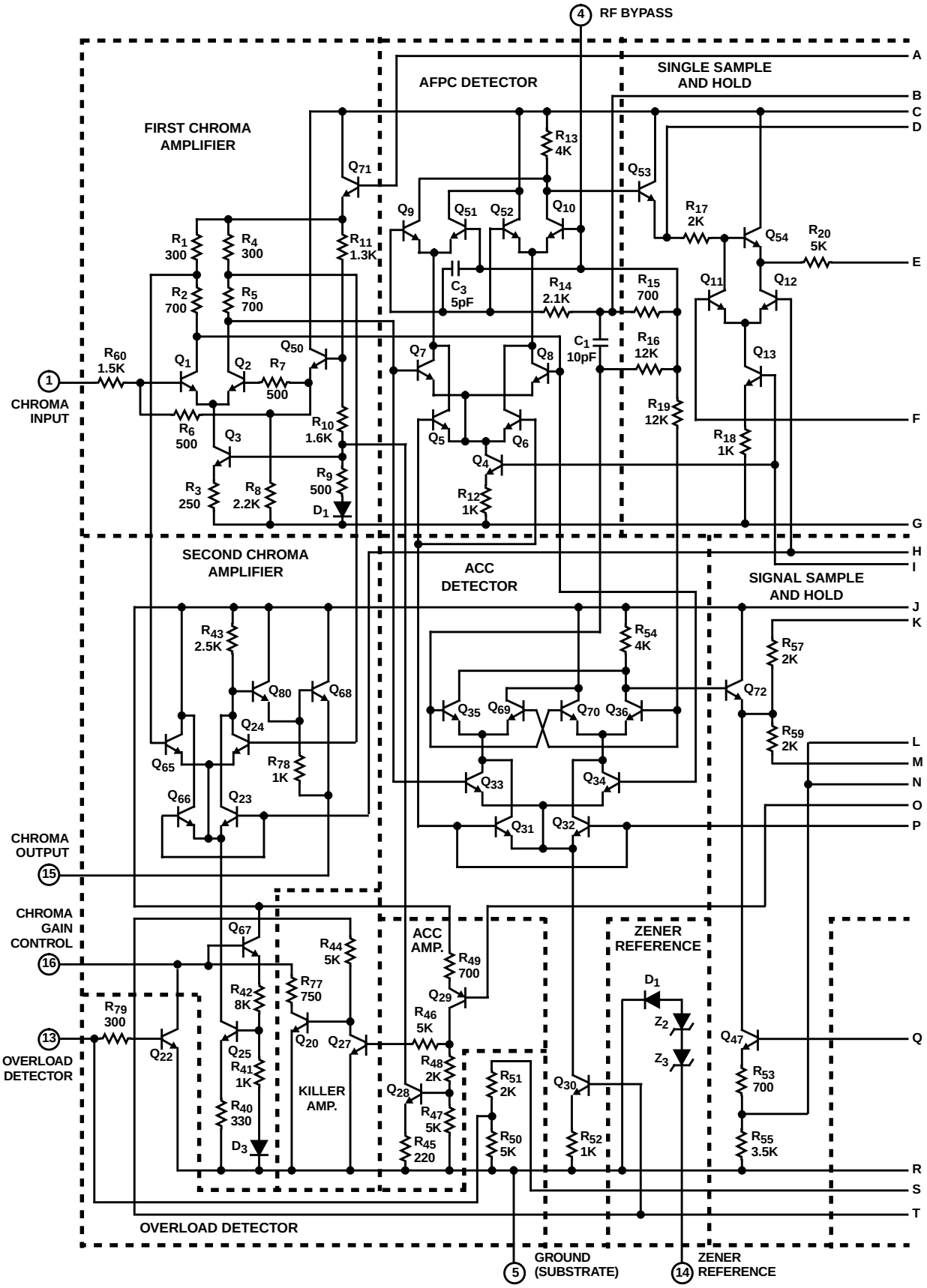
TV CHROMA PROCESSOR



NOTES:

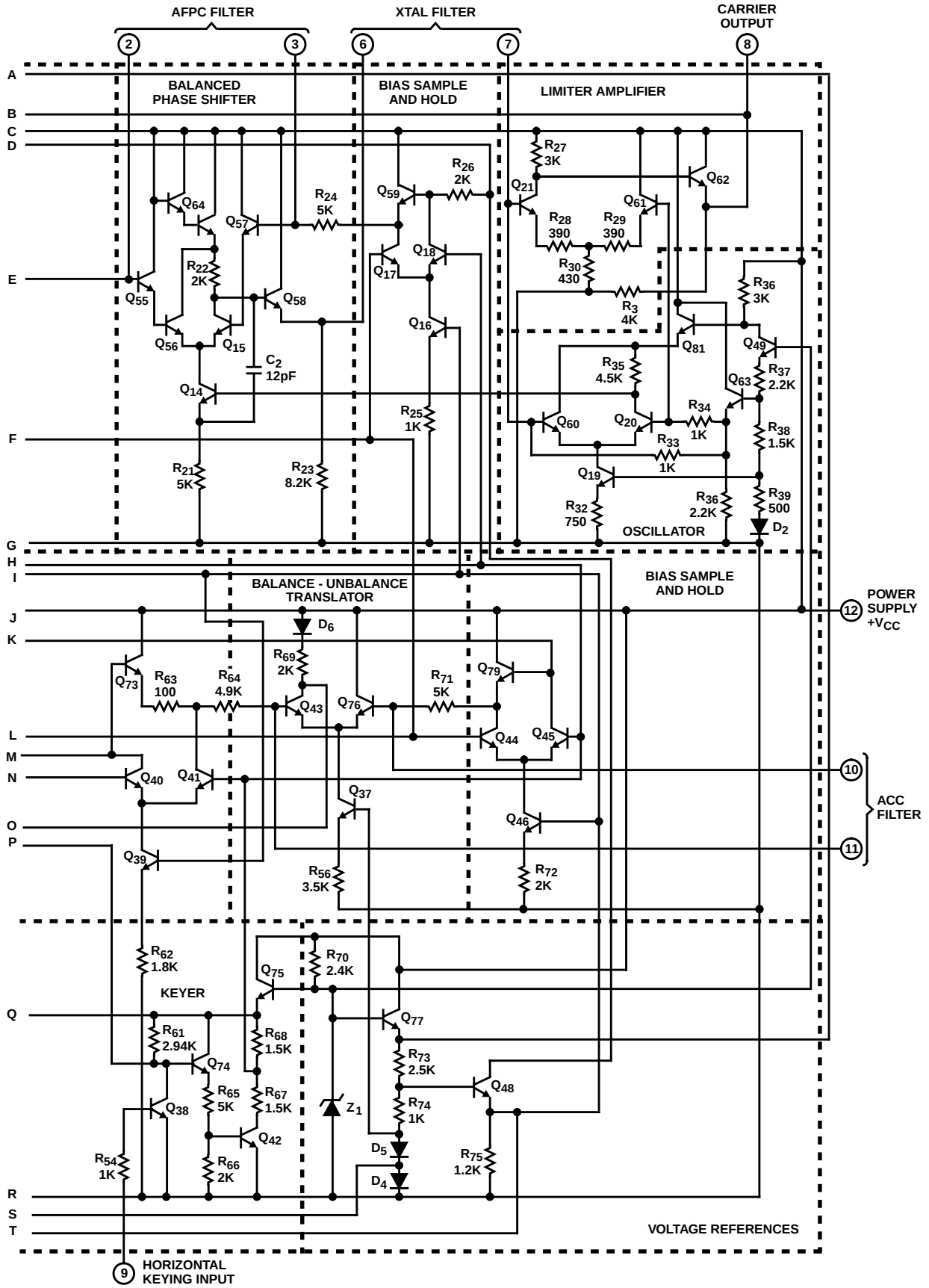
6. Optional design features.
7. Pinout numbers refer to the PDIP package.

Schematic Diagram



NOTE: Pin numbers refer to the PDIP Package. Resistance values are in ohms.

Schematic Diagram (Continued)



Application Information

Circuit Description (Pin numbers refer to the DIP package.)

The following paragraphs briefly describe the circuit operation of the CA3126 (shown in the Block Diagram and Schematic Diagram). A detailed description of the operation of various portions of the CA3126 is given in AN6247, “Application of the CA3126 Chroma-Processing lC Using Sample-and-Hold Techniques”.

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450Ω resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This “compared” voltage controls the phase- shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45 and -45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The “compared” voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

General Considerations

The block diagram shown is typical of the type of circuit used in the practical application of the CA3126. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450Ω (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.
2. When the overload detector is used, a large resistor (nominally 47,000Ω) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is DC shorted during the setting operation because of the DC offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in AN6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than $0.5V_{P-P}$ output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q_{25}. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126 is shown in Figure 1.

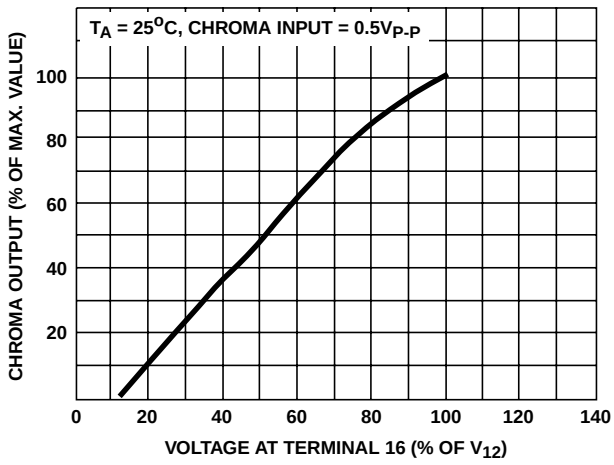


FIGURE 1. CHROMA GAIN CONTROL

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545MHz crystal, a 680Ω resistor, and a 10pF capacitor connected in series across Terminals 6 and 7. A 33pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A

curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Figure 2. It should be noted that the slope of the curve determines the DC gain of the phase-locked loop, i.e., 40Hz per degree.

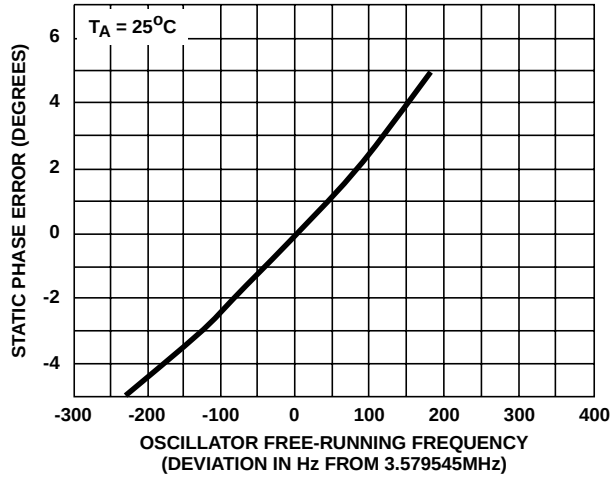


FIGURE 2. STATIC PHASE ERROR

Thermal Considerations

The circuit of the CA3126 is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figures 3 and 4 show the oscillator and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively.

Both the oscillator and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Figure 5. All the temperature plots are characteristic of the test circuit with the indicated component types and values given.

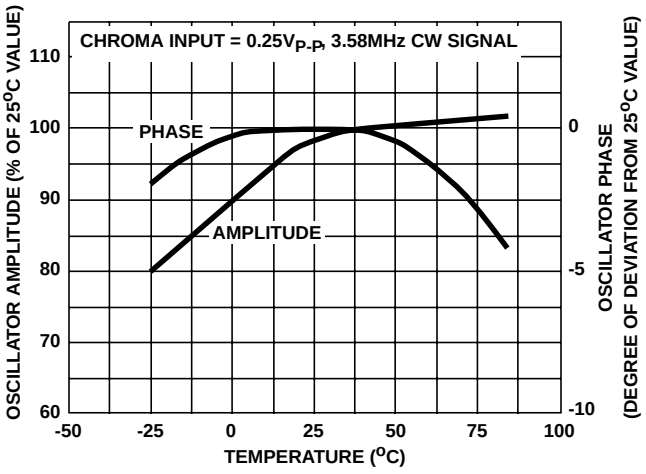


FIGURE 3. AMPLITUDE AND PHASE VARIATIONS OF OSCILLATOR OUTPUT vs TEMPERATURE

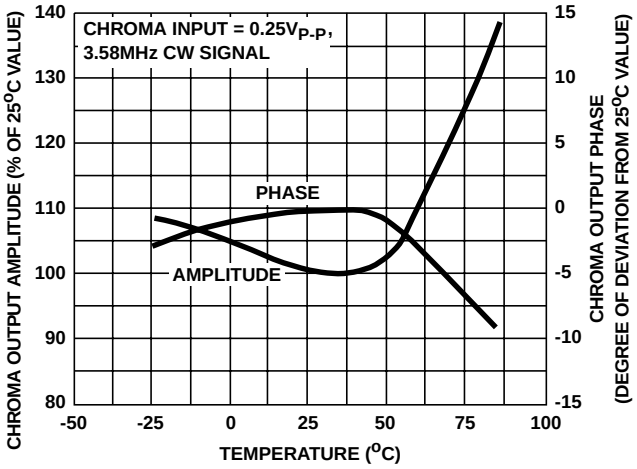


FIGURE 4. AMPLITUDE AND PHASE VARIATIONS OF CHROMA OUTPUT vs TEMPERATURE

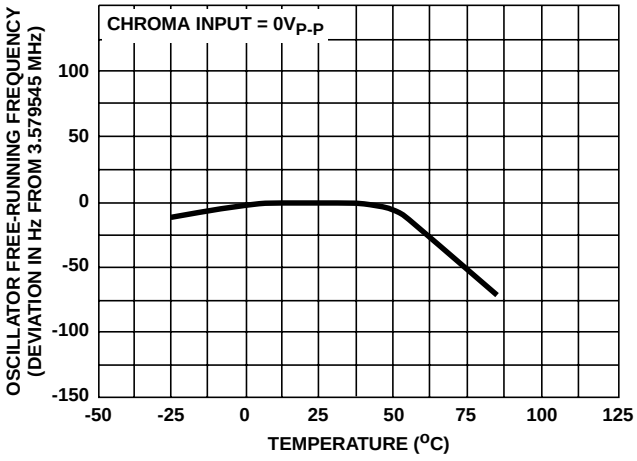
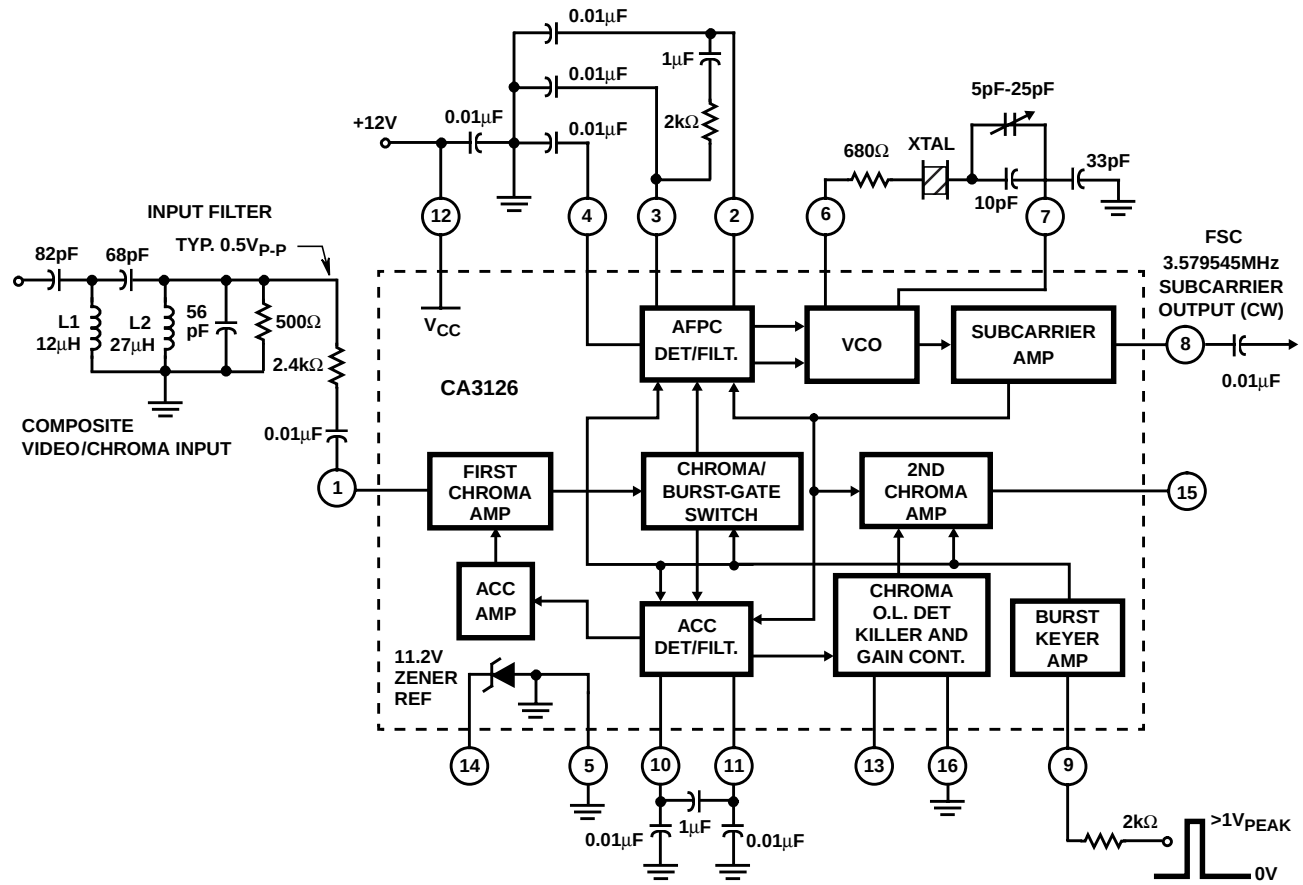


FIGURE 5. VARIATION OF OSCILLATOR FREE RUNNING FREQUENCY vs TEMPERATURE



NOTE: For Subcarrier Regenerator, the second chroma amp is not used; Pins 13,14, and 15 are not connected and pin 16 is grounded.

FIGURE 6. TYPICAL APPLICATION OF THE CA3126 AS A SUBCARRIER REGENERATOR