

January 1999

Features

- 5 Multiplex Video Channels
 - 1 Independent Channel
 - 4 Channels with Enable
- 4 LED Channel Indicator Outputs
- Wideband Video Amplifier 25MHz Unity Gain
- Adjustable Video Amplifier Gain
- High Signal-Drive Capability

Applications

- Video Multiplex Switch
- 75 Ω Video Amplifier/Line Driver
- Video Signal-Level Control
- Monitor Switching Control
- TV/CATV Audio/Video Switch
- Video Signal Adder/Fader Control

Part Number Information

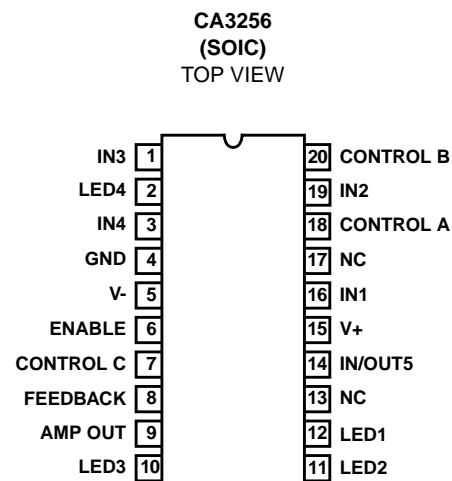
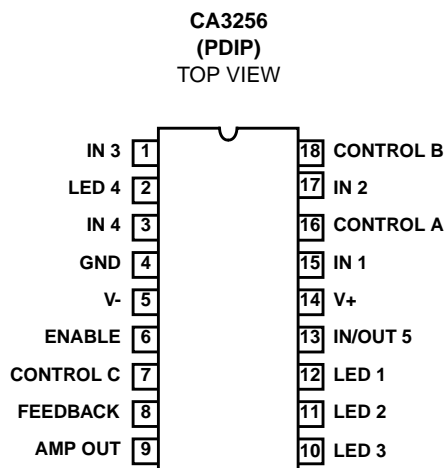
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3256E	-40 to 85	18 Ld PDIP	E18.3
CA3256M	-40 to 85	20 Ld SOIC	M20.3

Description

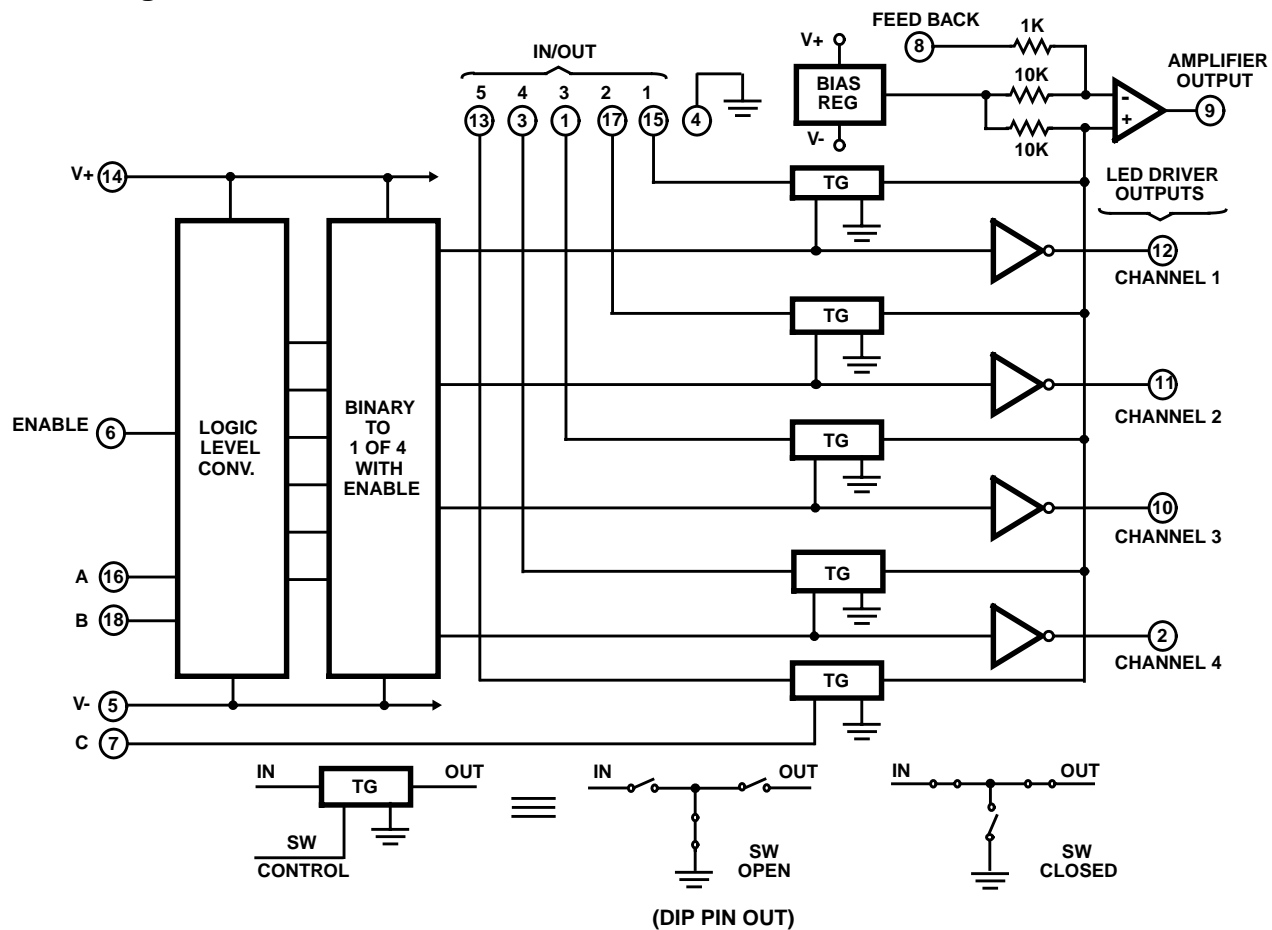
The CA3256 BiMOS analog video switch has five channels of CMOS multiplex switching for general-purpose video-signal control. One of four CMOS channels may be selected in parallel with channel 5. The CMOS switches are inputs to the video amplifier but may be used in bilateral switching between channels 1 to 4 and channel 5. The analog switches of channels 1 to 4 are digitally controlled with logic level conversion and binary decoding to select 1 of 4 channels. The enable function controls channels 1 to 4 but does not affect channel 5. LED output drivers are selected with the channel 1-to-4 switch selection to indicate the ON-channel. Channel 5 may be used as a monitor output for data or signal information on channels 1 to 4. The transmission gate switches shown in the block diagram of the CA3256 are configured in a "T" design to minimize feedthrough. When the switch is off, the shunt or center of the "T" is grounded.

The amplifier has high input impedance to minimize the R_{ON} transmission gate insertion loss. The amplifier output impedance is typically 5 Ω in a complementary symmetry output. The amplifier can directly drive a nominal 75 Ω coaxial cable to provide line-to-line video switching. The gain of the amplifier is programmable by different feedback resistor values between pins 8 and 9. Compensation may also be used between these pins for an optimally flat frequency response. An internal regulated 5V bias reference with temperature compensation permits stable direct-coupled output drive and minimizes DC offset during signal switching.

Pinouts



Block Diagram



Switch Control Logic

Channel Number	C	A	B	Enable
1	0	0	0	1
2	0	0	1	1
3	0	1	0	1
4	0	1	1	1
5 + (1-4) (Note)	1	Channel 1-4		1
5	1	Channel 5 Only		0
None	0	X	X	0

NOTE: For Maximum Video Bandwidth, Use Single Channel Selections

Absolute Maximum Ratings

DC Supply Voltage Range (V+ to V-) 18V
 Control Input Voltage Range, All Inputs V+ to V-
 Signal Input Voltage Range, Channel 1-5 3V_{P-P}
 Amplifier Output Current 30mA
 DC LED Sink Current 30mA

Operating Conditions

Temperature Range -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
 PDIP Package 70
 SOIC Package 75
 Maximum Junction Temperature (Die) 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC - Lead Tips Only)

Electrical Specifications $T_A = 25^\circ\text{C}$, V+ = 12V; V- = GND

PARAMETER	SYMBOL	TYPICAL VALUES		UNITS
Power Supply Voltage V+ to V-		10 to 17		V
Power Supply Current	I_{CC}	20		mA
		SWITCH	AMPLIFIER	
Open Loop Gain	A_{OL}	-	35	dB
Programmable Gain, FB Adjustment Range		-	-0.8 A_{OL}	dB
Full Power Bandwidth		-	10	MHz
Unity Gain Bandwidth, 1k Ω , 7pF Compensation		-	25	MHz
Insertion Loss		-0.8	-	dB
Signal Feedthrough, 5MHz		-66	-	dB
Input Impedance	Z_{IN}	-	10	k Ω
Output Impedance	Z_{OUT}	-	5	Ω
Maximum Input Voltage	$V_{I(MAX)}$	3	2.5	V _{P-P}
Maximum Output Voltage, Clipped	$V_{O(MAX)}$	-	7	V _{P-P}
Reference Bias Output Voltage (V _g - V-)		-	5	V
Differential Gain		-	1	%
Differential Phase		-	1	Degree
Off Isolation, Channel to Channel, $Z_{IN} = 75\Omega$		-66	-	dB
LLC Switch Turn On/Off Time Delay		-	0.5	μs
Maximum LED Sink Current		-	30	mA
Typical Output Source Current		-	16	mA
Channel Control Switch A, B, C and E _N Threshold (Notes 2, 3)	V_{TH}	Approximately (V+ - V-)/2		V

CAUTION: Connect the V- power supply voltage before or during the V+ turn-on.

NOTES:

2. Threshold value is referenced to GND.
3. V_{TH} is restricted by the equation, $V_{TH} < V+ - 1$.

CA3256

Electrical Specifications $T_A = 25^{\circ}\text{C}$, $V_+ = 12\text{V}$, $V_{\text{LED}} = 12\text{V}$, $V_- = \text{GND}$, Pin 4 = GND, Feedback Switch Closed, $V_{\text{HIGH}} = 9\text{V}$, $V_{\text{LOW}} = 3\text{V}$
(See Figure 1), Unless Otherwise Specified

PARAMETERS	INPUTS					CHANNEL SWITCH CONTROL					MIN	TYP	MAX	UNITS
	CH 1	CH 2	CH 3	CH 4	CH 5	A	B	C	ENABLE	NOTE 6 TEST PIN#				
	PIN 15	PIN 17	PIN 1	PIN 3	PIN 13	PIN 16	PIN 18	PIN 7	PIN 6					
Supply Current, V _{LED} = 0V	0V	0V	0V	0V	0V	3V	3V	3V	3V	14	10	16	22	mA
Dual Supply Current V+ = +7V, V- = -5V	0V	0V	0V	0V	0V	0V	0V	0V	7V	14/5	10	20	26	mA
Amplifier Output Voltage, Open Loop V _{LED} = 0V	0V	0V	0V	0V	0V	3V	3V	3V	3V	9	6	8.5	10	V
Amplifier Output Voltage, Closed Loop, V _{LED} = 0V	0V	0V	0V	0V	0V	3V	3V	3V	3V	9	4.8	5.1	5.4	V
I _{OUT} (MAX) (Source) Open Loop	0V	0V	0V	0V	0V	3V	3V	3V	3V	9 Note 4	-	-70	-25	mA
I _{OUT} (MAX) (Sink) Open Loop	0V	0V	0V	0V	0V	3V	3V	3V	3V	9 Note 5	10	16	-	mA
Input Leakage Channel 1-5	3V	3V	3V	3V	3V	3V	3V	3V	3V	1, 3, 15, 17	-15	5	15	nA
Channel Control Input A, B, C, Enable Leakage	0V	0V	0V	0V	0V	Measure at 3V, 9V each; Enable and Channel Switching Control Inputs				6, 7, 16, 18	-20	10	20	nA
LED Off Voltage, V _{OFF}	0V	0V	0V	0V	0V	Select Channel 0-5				2, 10, 11, 12	11.97	11.99	-	V
LED On Voltage, V _{ON}	0V	0V	0V	0V	0V	Select Channel 0-5				2, 10, 11, 12	-	0.1	0.3	V
Switch Resistance, R _{DS}	±100µA Input Each Switch, Channel 1-4 + 5					Select Channel 1-4		9V	9V		0.8	1.1	1.4	kΩ
R _{DS} Match	Calculation: (Max R _{DS} - Min R _{DS})/Min R _{DS}									-	-	3.6	5	%
Amplifier Output Offset, V _O , Feedback Switch Closed V+ = +7V, V- = -5V	0V	0V	0V	0V	0V	0V	0V	0V	7V	9	-100	45	100	mV
Closed Loop Gain	3V	0V	0V	0V	0V	3V	3V	3V	9V	9	-0.5	-0.1	0.5	dB

NOTES:

- $V_{\text{OUT}} = +7\text{V}$.
- $V_{\text{OUT}} = +3\text{V}$.
- DIP Pinout.

Test Circuits

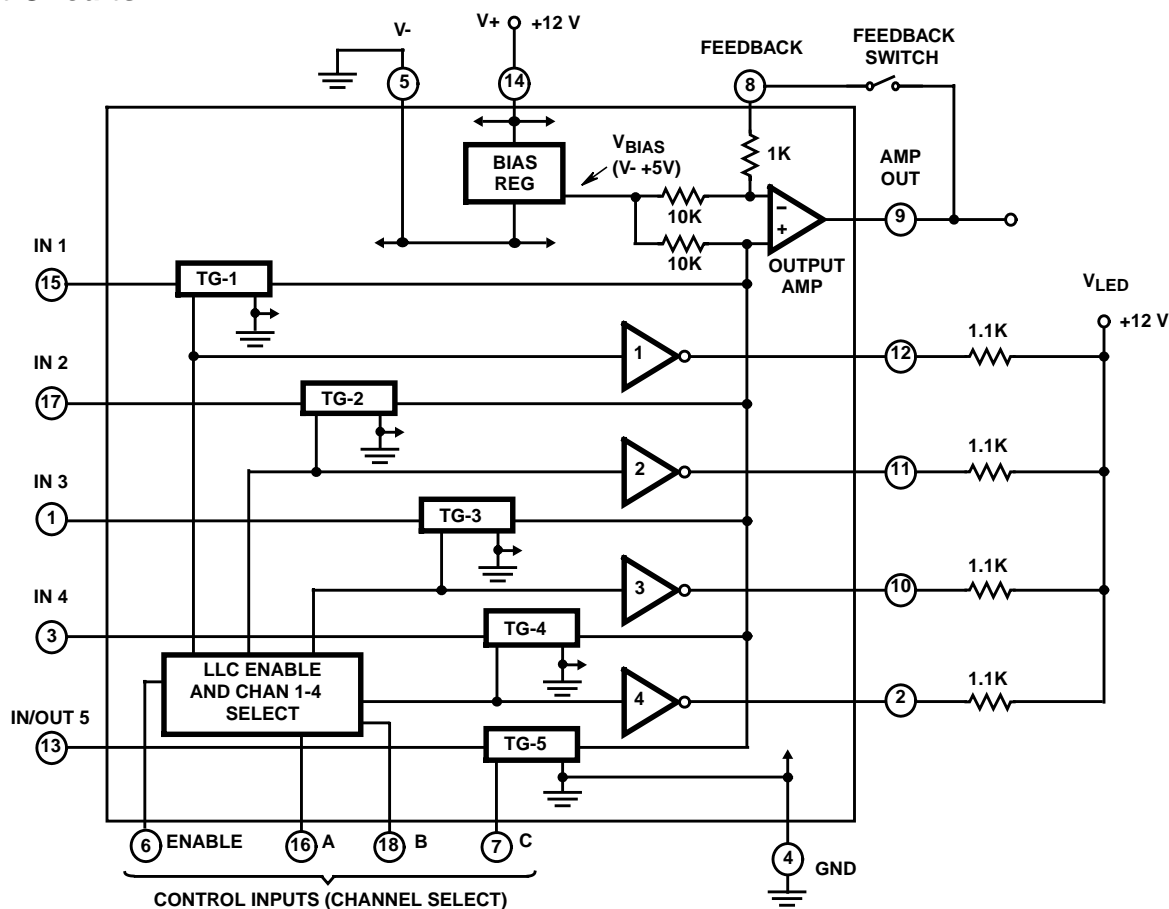


FIGURE 1. CA3256 TEST CIRCUIT (DIP PINOUT)

Application Information

CMOS analog switches are available in a wide variety of forms, and have been known and used for some time. There are a number of advantages to using the CMOS transmission gate as a switch:

- Ideal Suitability to Series Cascade Arrangements
- Simple Multiple Parallel Input Switching Arrangements
- No Bipolar Junctions and, Hence, No Offset
- Very Low Power Consumption
- Wide Signal-Swing Capability
- Fast Multiplexing and Video Switching
- Wide Bandwidth
- Low R_{ON} Channel Resistance
- Bidirectional Signal Handling

An Integrated Video-Switch Amplifier

Commonly, integrated video-switch amplifiers have been fabricated in the bipolar technology using differential amplifiers in a current-switching mode. In this form, two differential pairs are needed for two input-signal sources. The handling of multiple sources is very much more complex. The advantages of the CMOS video-switch amplifier have already been noted. While the bipolar video switch has high output drive and switching

speed as advantages, the price is high in voltage offset and current drain. The integrated device solution that is offered here is in the use of the BiMOS technology, where both the CMOS and bipolar processes complement each other to provide CMOS switching with bipolar amplifiers. The BiMOS process allows several CMOS switches to be coupled to a bipolar drive-amplifier in the same process to exploit the best of two technologies.

Other advantages are gained when the BiMOS process is used for an IC video-switch amplifier design. The BiMOS process calls for a P-substrate and, therefore, isolated N-epitaxial wells can be built for both N and P channel parts. The boats provide for better isolation of the N and P channels. The N and P wells in a transmission-gate cell can be switched between source and rail; therefore, they have a smaller body effect on both N and P devices, which results in better gain linearity. Where desired, oxide capacitors are available for bipolar amplifier compensation.

CA3256 Video-Switch Amplifier

The Block Diagram shows the functional diagram of the CA3256, which consists of five MOS channels, each comprising a three-element T-switch. The output of the five switches is made common and fed into the input of a bipolar

buffer amplifier. The T-switch, together with the input impedance of the buffer, is typically 10k Ω , and has an insertion loss of approximately 0.8dB. The T-switch was designed to handle up to 3V_{P-P} input signal with low distortion. The T-switches of the CA3256 conform to a break-before-make format; hence, shorting to ground is eliminated.

The amplifier is programmable for gain and, typically, can provide a gain of 1 into a 75 Ω load or a gain of 5 into a 1k Ω load. The maximum output signal swing with linearity is greater than 5V_{P-P} for (V₊ to V₋) greater than or equal to 12V, while the maximum output current is approximately 20mA. The amplifier has base-current compensation to reduce offset and a temperature compensated 5V zener referenced bias. Other features include LED-selector indicators for channels 1 through 4. The fifth channel is independently

selectable for use as a separate input or output in parallel with any on channel, and may be used as a monitor, or for pass-through, signal summing, or parallel distribution.

In the application, the user has the option to specify V₋ = -5V for the switch and a ground reference for the amplifier input and output. Alternatively, the CA3256 may be used with a single +12V supply. The logic select for channels 1 through 4 is controlled by the A, B and Inhibit lines with ground to V₊ logic switching. The logic threshold is approximately (V₊ - V₋)/2 referenced to ground. DC coupling may also be used at the output (when V₋ is returned to a -5V supply). For the circuit of Figure 3, AC coupling is used at the output and input. The switching bias arrangement shown provides for stable bias across each switch when in the off position to minimize transients when the input is switched.

Typical Applications

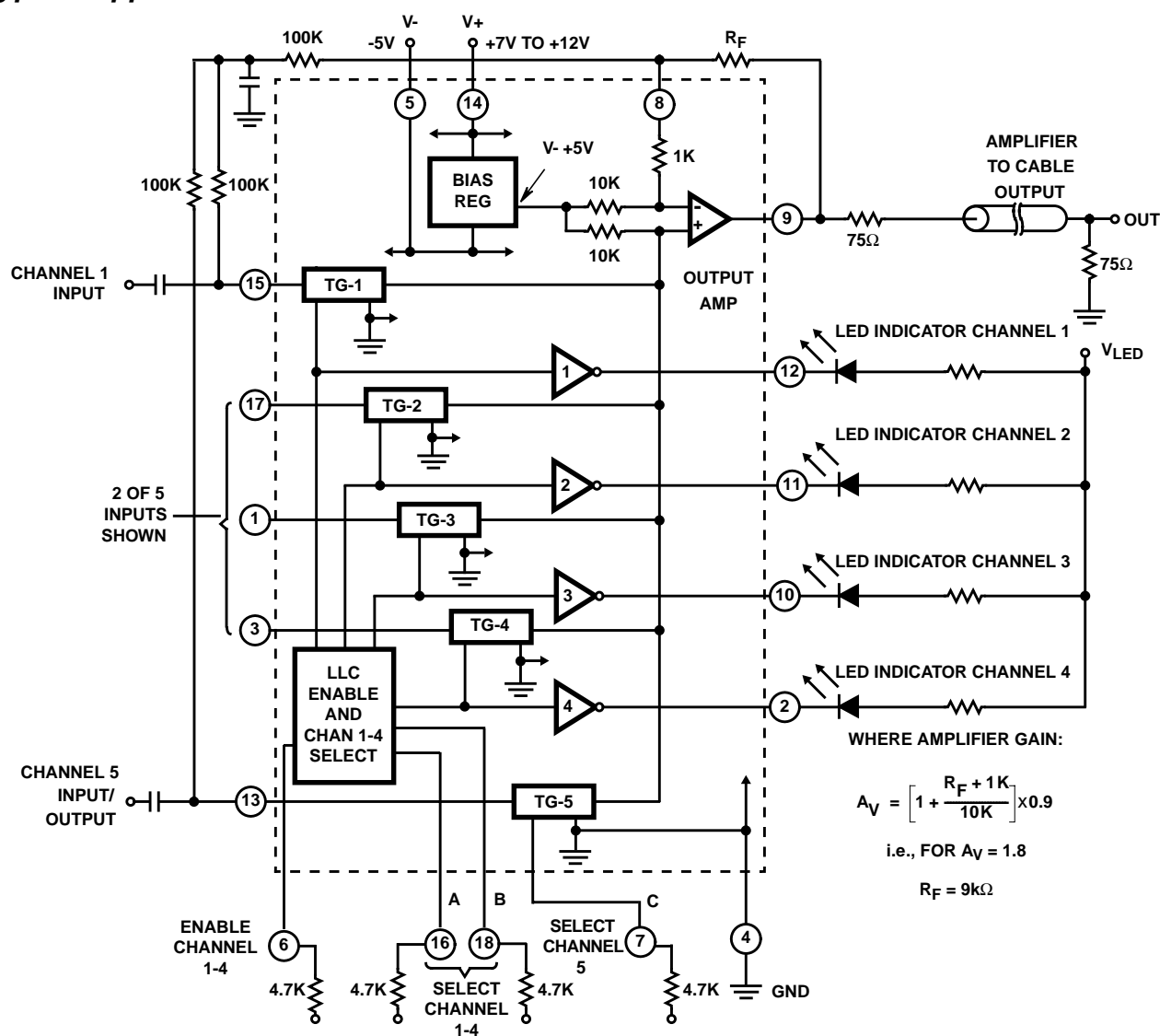
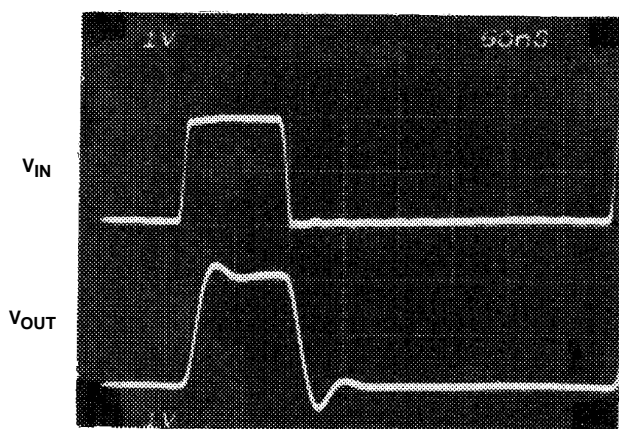
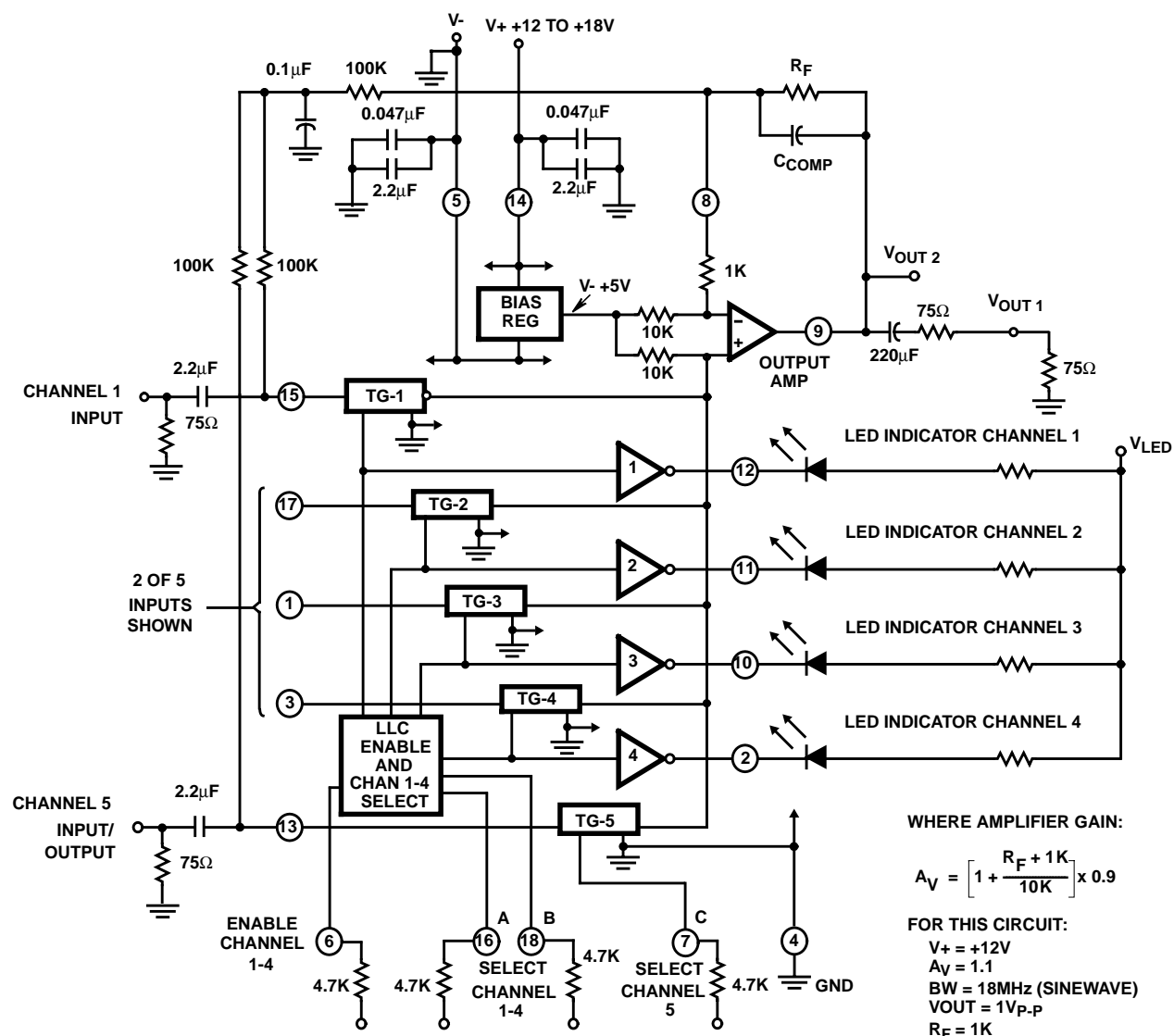


FIGURE 2. TYPICAL APPLICATION WITH DIRECT-COUPLED OUTPUT AND V₋ = -5V (DIP PINOUT)



Pulse Performance = 20ns t_R for 0V to 2V Pulse. See Figure 4 for frequency response.

V+ = +12V, R_F = 1kΩ, C_{COMP} = 6pF.

FIGURE 3. TYPICAL APPLICATION WITH AC-COUPLED INPUT AND OUTPUT, AND V- = GND (DIP PINOUT)

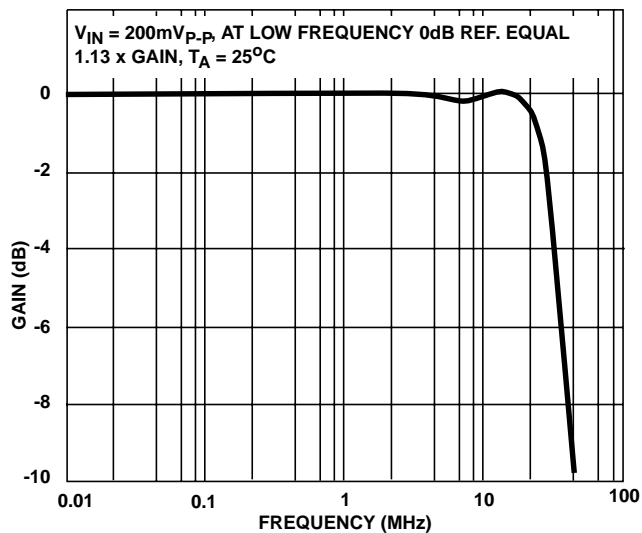


FIGURE 4A. CLOSED LOOP RESPONSE WITH COMPENSATION CAPACITOR, C_{COMP} , AND R_F , SEE FIGURE 4B

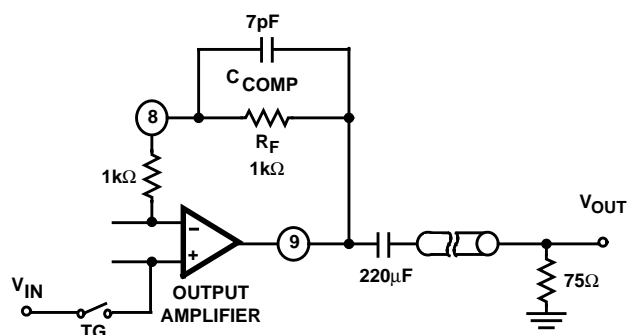


FIGURE 4B. TEST CIRCUIT FOR FIGURE 4A

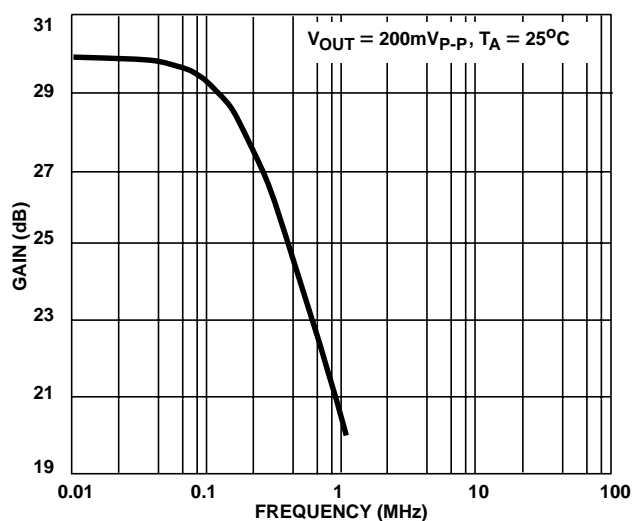


FIGURE 4C. OPEN LOOP RESPONSE WITH NO FEEDBACK, SEE FIGURE 4D

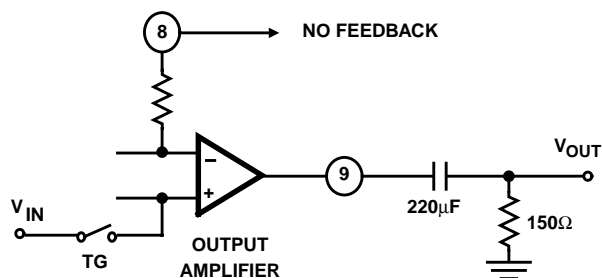


FIGURE 4D. TEST CIRCUIT FOR FIGURE 4C

FIGURE 4. FREQUENCY RESPONSE OF AC COUPLED CIRCUIT OF FIGURE 3

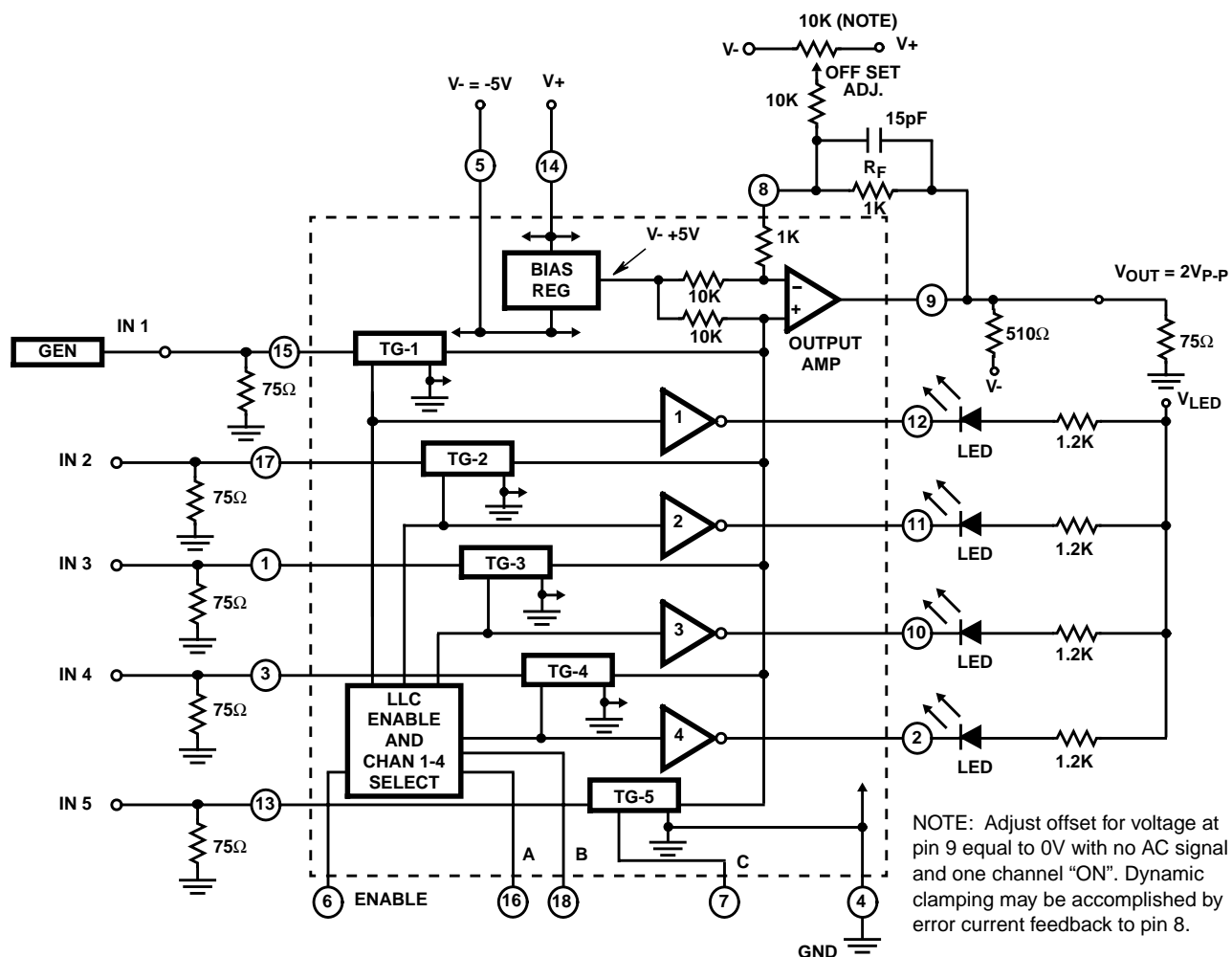


FIGURE 5. TYPICAL APPLICATION WITH DC-COUPLED INPUT AND OUTPUT, AND OFFSET ADJUST. OUTPUT VOLTAGE IS FIXED BY THE V_+ AND V_- RANGE. (DIP PINOUT)

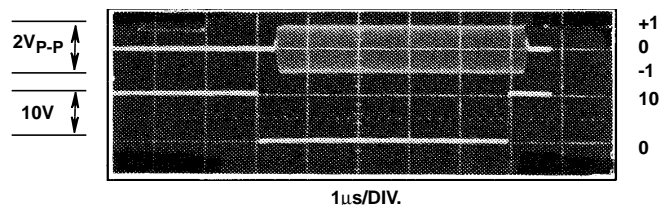


FIGURE 6A. GATED OUTPUT FOR $V_+ = +12V$ ENABLE = HIGH, CONTROL B = C = LOW, CONTROL A = 10V PULSE. THE BURST OUTPUT IS DELAYED $\sim 400ns$ AT t_{ON} , t_{OFF} .

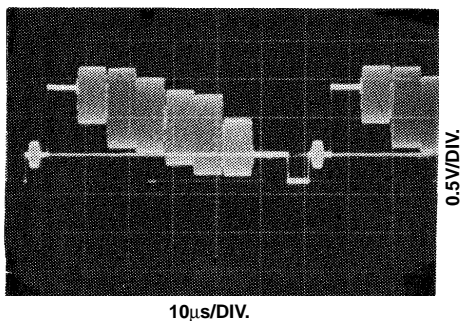


FIGURE 6B. STANDARD NTS COLOR BAR

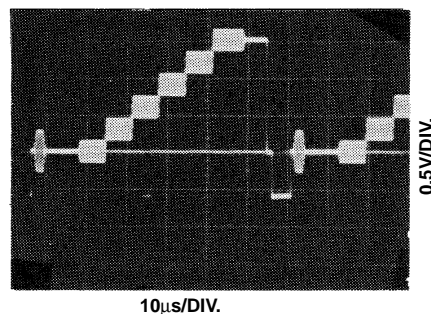


FIGURE 6C. UNIFORM STEP SIGNAL WITH 3.58MHz MODULATION

FIGURE 6. PERFORMANCE OF CIRCUIT IN FIGURE 5

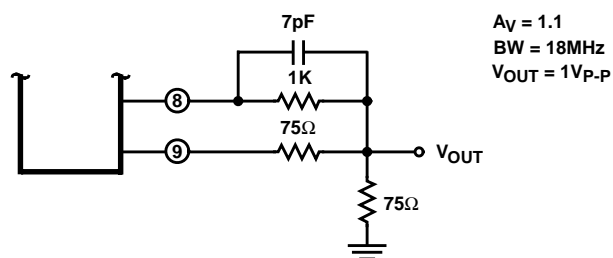
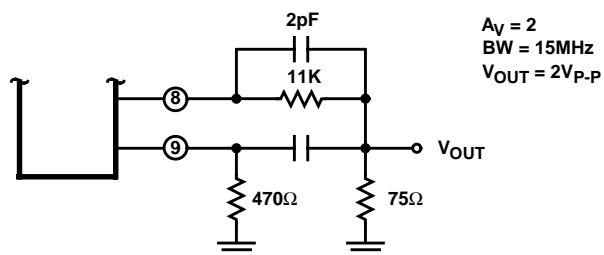


FIGURE 7A.



NOTE: 470Ω added to increase source drive current.

FIGURE 7B.

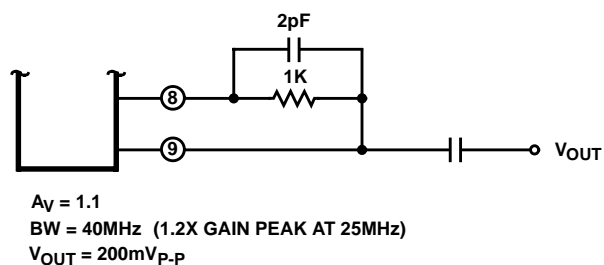


FIGURE 7C.

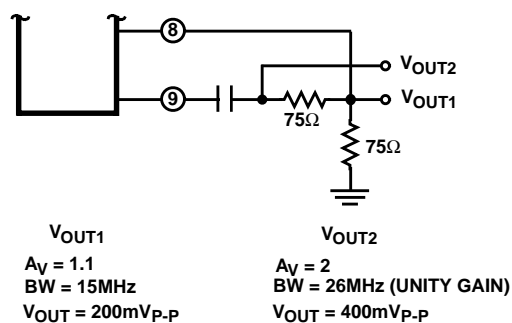


FIGURE 7D.

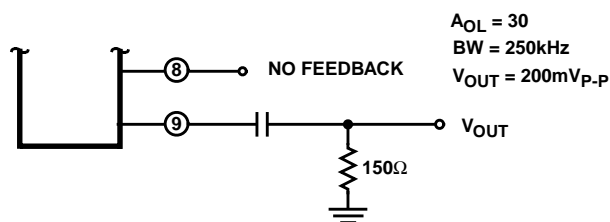


FIGURE 7E.

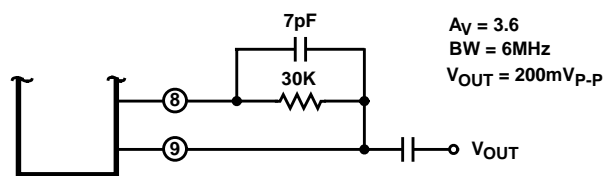


FIGURE 7F.

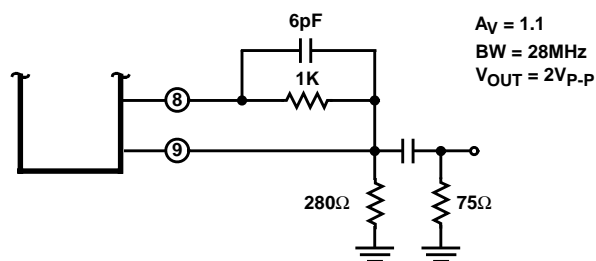


FIGURE 7G.

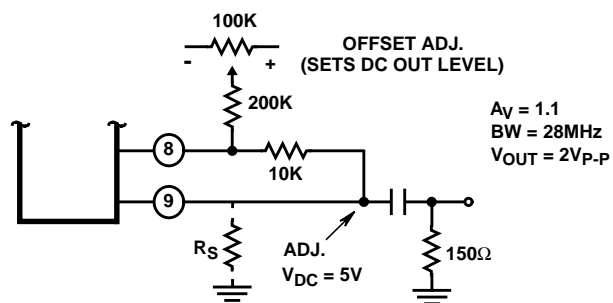
NOTE: Add R_S to reduce high-frequency slewing.

FIGURE 7H.

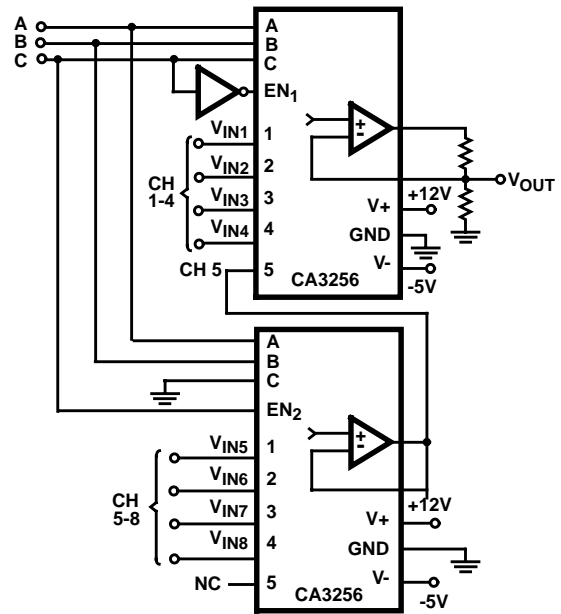
FIGURE 7. OTHER TABULATED RESULTS FOR VARIATIONS OF LOAD AND FEEDBACK ($V_+ = +12\text{V}$)

Any combination of switch input circuits can be configured with multiple, parallel, line-drive outputs. The video switch amplifier circuit of Figure 8 illustrates how the CA3256 may be configured in pairs to provide an 8-to-1 video switch amplifier using a 3-bit address to select the input. It is also possible to use the fifth channel input to tie signals to a common bus line for distribution from the selected amplifier; however, distributed capacitance loading will result in reduced bandwidth. The 4 plus 1 combination of input-signal switching provides for a wide assortment of video switch circuit configurations.

While the BiMOS process does provide some compromises for both the switch and the amplifier, the combined system is capable of the performance needed in most high-quality, switching applications. As an integrated system, many of the problems in PC-board layout are simplified, and there is a reduction in component count. In its simplest form, with +12V and -5V supplies, the CA3256 may be DC connected at the input and output; the LED indicators need not be connected. Under these conditions, the circuit may be as simple as the one in Figure 8.

Summary

While each video-switch amplifier is designed for a specific application and, to that end, is tailored as far as performance to a given set of specifications, the circuit-designer's goal is generally the same in every case: to make the best possible switch for the lowest cost. In this respect, the CA3256 IC switch and amplifier discussed provide an excellent choice for a cost-effective high-performance video-switch amplifier, by taking advantage of the complementary features of both high-speed CMOS and bipolar integrated circuits.



TRUTH TABLE

CH	C	A	B
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

FIGURE 8. AN 8-TO-1 VIDEO SWITCH AMPLIFIER USING TWO CA3256 DEVICES