HARRIS Semiconductor

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
Call Central Applications 1-800-442-7747
or email: centapp@harris.com

CD22354A, CD22357A

CMOS Single-Chip, Full-Feature PCM CODEC

February 1999

Features

- Meets or Exceeds All AT&T D3/D4 Specifications and CCITT Recommendations
- Complete CODEC and Filtering Systems: No External Components for Sample-and-Hold and Auto-Zero Functions. Receive Output Filter with (SIN X)/X Correction and Additional 8kHz Suppression
- Variable Data Clocks - From 64kHz 2.1MHz
- Receiver Includes Power-Up Click Filter
- TTL or CMOS-Compatible Logic
- ESD Protection on All Inputs and Outputs

Applications

- PABX
- Central Office Switching Systems
- Accurate A/D and D/A Conversions
- Digital Telephones
- Cellular Telephone Switching Systems
- Voice Scramblers - Descramblers
- T1 Conference Bridges
- Voice Storage and Retrieval Systems
- Sound Based Security Systems
- Computerized Voice Analysis
- Mobile Radio Telephone Systems
- Microwave Telephone Networks
- Fiber-Optic Telephone Networks

Description

The CD22354A and CD22357A are monolithic silicon-gate, double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22354A provides the AT&T μ-law and the CD22357A provides the CCITT A-law companding characteristic.

The primary applications for the CD22354A and CD22357A are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown below.

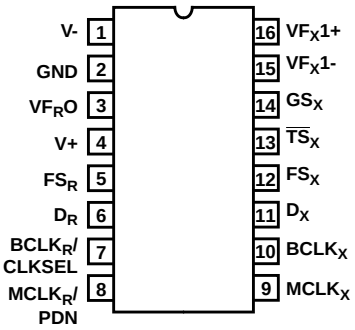
With flexible features, including synchronous and asynchronous operations and variable data rates, the CD22354A and CD22357A are ideally suited for PABX, central office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD22354AE	-40 to 80	16 Ld PDIP	E16.3
CD22357AE	-40 to 80	16 Ld PDIP	E16.3

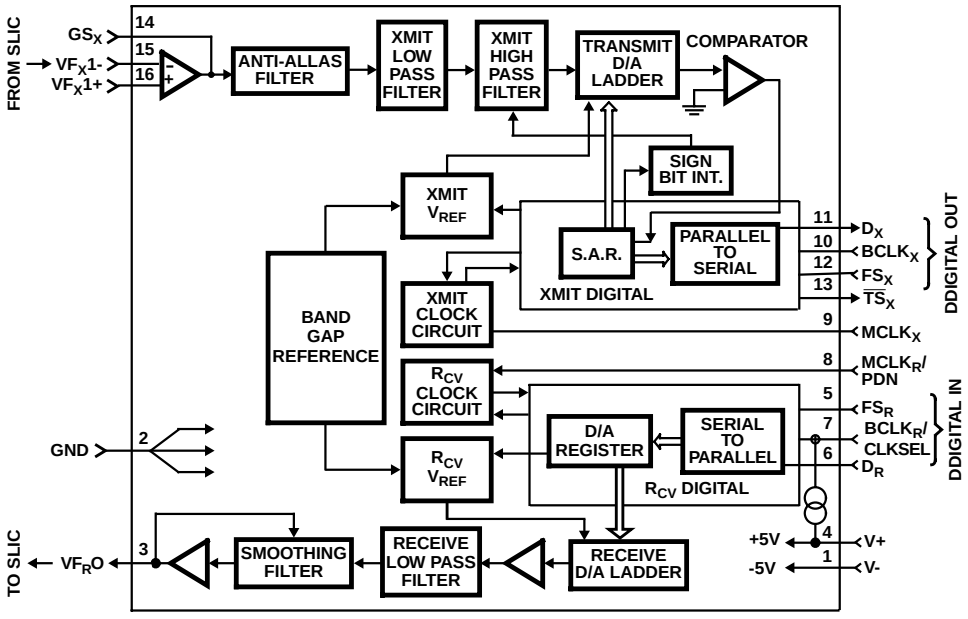
Pinout

CD22354A, CD22357A
(PDIP)
TOP VIEW



Functional Block Diagram

FULL-FEATURE PCM CODEC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1682.4**

Absolute Maximum Ratings

DC Supply-Voltage, (V+) . . . . . -0.5 to 7V
DC Supply-Voltage, (V-) . . . . . 0.5 to -7V
DC Input Diode Current,
I_{IK} (V_I < V- -0.5V or V_I > V+ 0.5V) . . . . . ±20mA
DC Output Diode Current,
I_{OK} (V_I < V- -0.5V or V_O > V+ 0.5V) . . . . . ±20mA
DC Drain Current, Per Output
I_O (V- -0.5V < V_O < V+ 0.5V) . . . . . ±25mA
DC Supply/Ground Current . . . . . ±50mA
Power Dissipation Per Package (P_D):
For T_A = -40°C to 60°C 500mW
For T_A = 60°C to 85°C . . . . . Derate Linearly at 8mW/°C to 300mW

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Operating-Temperature Range (T_A) . . . . . -40°C to 80°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS						
Positive Power Supply	V+		4.75	5	5.25	V
Negative Power Supply	V-		-4.75	-5	-5.25	V
Power Dissipation (Operating)	P_{OPR}	V+ = 5V	-	75	90	mW
Power Dissipation (Standby)	P_{STBY}	V- = -5V	-	9	15	mW

Electrical Specifications At T_A = 0°C to 70°C; V+ = 5V ±5%, V- = -5V ±5%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS						
Analog Input Resistance	R_{INA}		10	-	-	MΩ
Input Capacitance	C_{IN}	All Logic and Analog Inputs	-	5	-	pF
Input Leakage Current, Digital	I_I	V_I = 0V or V+	-10	-	10	µA
Low Level Input Voltage	V_{IL}	I_{IL} = ±10µA (Max)	-	-	0.8	V
High Level Input Voltage	V_{IH}	I_{IH} = ±10µA (Max)	2	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL} = 3.2mA	-	-	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = 1.0mA	2.4	-	-	V
Open State Output Current	I_{OZ}	GND < D_X < V+	-10	-	10	µA
Input Leakage Current, Analog	I_I	-2.5V ≤ VF_X < 2.5V	-200	-	200	nA

Electrical Specifications

V+ = 5V ±5%, V- = -5V ± 5%, $BCLK_R = BCLK_X = MCLK_X$ = 1.544MHz, V_{IN} = 0dBm0, $T_A = 0^oC$ to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT AND RECEIVE FILTER TRANSFER CHARACTERISTICS						
Transmit Gain (Relative to Gain at 1020Hz) Input Amplifier Set to Unity Gain	G_{RX}	f = 16Hz	-	-	-40	dB
		f = 50Hz	-	-	-30	dB
		f = 60Hz	-	-	-26	dB
		f = 200Hz	-1.8	-	-0.1	dB
		f = 300Hz to 3000Hz	-0.15	-	0.15	dB
		f = 3300Hz	-0.35	-	0.05	dB
		f = 3400Hz	-0.7	-	0	dB
		f = 4000Hz	-	-	-14	dB
		f ≥ 4600Hz, Measure 0 - 4kHz Response	-	-	-32	dB
Receive Gain (Relative to Gain at 1020Hz) (Includes (SIN X)/X Compensation)	G_{RR}	f = 0Hz to 3000Hz	-0.15	-	0.15	dB
		f = 3300Hz	-0.35	-	0.05	dB
		f = 3400Hz	-0.9	-	0	dB
		f = 4000Hz	-	-	-14	dB

AC Specifications

Unless otherwise specified, the following conditions apply:

V+ = 5V ±5%, V- = -5V ±5%
GND_A, GND_D = 0V, F_{FX} = 1020Hz at 0dBm0
Transmit input amplifier operating in a unity gain configuration
Temperature . . . . . 0^oC to 70^oC
Receive output is measured single-ended. All output levels are (SIN X)/X corrected.

Definition

AMPLITUDE RESPONSE
Absolute Levels Definition:
V_{REF} = -2.5V
Nominal 0dBm0 level. . . . . 4dBm into 600Ω
$1.2276V_{RMS}$
Maximum Overload Level:
Voltage reference (V_{REF}) of -2.5V . . . . . 2.5V μ-Law
2.49V A-Law

AC Specifications Encoding Format at D_X Output

	CD22354A μ-LAW								CD22357A A-LAW (INCLUDES EVEN BIT INVERSION)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = -Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC DISTORTION						
Signal to Total Distortion Xmit or R_{CV}	STD_X, STD_R	Level = +3dBm0	33	-	-	dBc
		Level = 0 to -30dBm0	36	-	-	dBc
		Level = -40dBm0	30	-	-	dBc
		Level = -55dBm0, XMT	14	-	-	dBc
		Level = -55dBm0, R_{CV}	15	-	-	dBc
Single Frequency Distortion Xmit or R_{CV}	SFD_X, SFD_R		-	-	-46	dBc
Intermodulation (End-to-End Measurement) 2-Tone	IMD	V_{FX} = -4dBm0 to -21dBm0 f1, f2 from 300 to 3400Hz	-	-	-41	dB
Transmit Delay, Absolute	t_{DAX}	f = 1600Hz	-	280	315	µs
Transmit Envelope Delay Relative to t_{DAX}	t_{DEX}	f = 500-600Hz	-	170	220	µs
		f = 600-1000Hz	-	70	145	µs
		f = 1000-2600Hz	-	40	75	µs
		f = 2600-2800Hz	-	90	105	µs
Receive Delay, Absolute	t_{DAR}	f = 1600Hz	-	180	200	µs
Receive Envelope Delay Relative to t_{DAR}	t_{DER}	f = 500-600Hz	-40	-25	-	µs
		f = 600-1000Hz	-40	-25	-	µs
		f = 1000-2600Hz	-	60	90	µs
		f = 2600-2800Hz	-	110	125	µs

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC GAIN TRACKING						
Transmit Gain Tracking Error	GTX	+3 to -40dBm0	-	-	±0.2	dB
		-40 to -50dBm0	-	-	±0.4	dB
		-50 to -55dBm0	-	-	±1.2	dB
Receive Gain Tracking Error	GTR	+3 to -40dBm0	-	-	±0.2	dB
		-40 to -50dBm0	-	-	±0.4	dB
		-50 to -55dBm0	-	-	±1.2	dB
Transmit Input Amplifier Gain, Open Loop	A_{OL}	$R_L \geq 1M\Omega$ at GS_X	68	-	-	dB

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Transmit Input Amplifier Gain, Unity	A_{CL}	Unity Gain Configuration Inverting or Non-Inverting $R_L \geq 10K$, $C_L \leq 50pF$	-0.01	-	0.01	dB
Transmit Gain, Absolute	G_{XA}	$R_L \geq 10K$, $C_L \leq 50pF$	-0.15	-	0.15	dB
Receive Gain, Absolute	G_{RA}	$R_L \geq 600\Omega$, $C_L \leq 500pF$	-0.15	-	0.15	dB

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC NOISE						
Transmit Noise	N_X	VF_XI- = GND	-	12	15	dBrnc0
		VF_XI+ = GND	-	-74	-67	dBrn0p
Receive Noise	N_R	PCM Code Equivalent to 0V	-	7	11	dBrnc0
			-	-83	-79	dBrn0p
V+ Power Supply Rejection Transmit	PSRR	VF_XI+ = 0V V+ = 5V + ($100mV_{RMS}$) f = 0kHz to 50kHz	40	-	-	dBc
V- Power Supply Rejection Transmit	PSRR	VF_XI- = 0V V- = -5V + ($100mV_{RMS}$) f = 0kHz to 50kHz	40	-	-	dBc
V+ Power Supply Rejection Receive	PSRR	PCM Code = All 1 Code V+ = 5V + ($100mV_{RMS}$) f = 0kHz to 4kHz	40	-	-	dBc
		f = 4kHz to 25kHz	37	-	-	dB
		f = 25kHz to 50kHz	36	-	-	dB
V- Power Supply Rejection Receive	PSRR	PCM Code = All 1 Code V- = -5V + ($100mV_{RMS}$) f = 0kHz to 4kHz	40	-	-	dBc
		f = 4kHz to 25kHz	40	-	-	dB
		f = 25kHz to 50kHz	36	-	-	dB
Cross Talk Transmit to Receive	CT_{XR}	VF_XI- = 0dBm0 at 1020Hz	-	-80	-70	dB
Cross Talk Receive to Transmit	CT_{RX}	D_R = 0dBm0 at 1020Hz, VF_XI- = 0V	-	-76	-70	dB

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TIMING						
Frequency of Master Clocks	$1/t_{PM}$	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin	-	1.536	-	MHz
			-	1.544	-	MHz
		$MCLK_X$ and $MCLK_R$	-	2.048	-	MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160	-	-	ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160	-	-	ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$	-	-	50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$	-	-	50	ns
Set-up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First Bit Clock after the Leading Edge of FS_X	100	-	-	ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	V_{IH} = 2.2V	160	-	-	ns
Width of Bit Clock Low	t_{WBL}	V_{IL} = 0.6V	160	-	-	ns
Rise Time of Bit Clock	t_{RB}	t_{PB} = 488ns	-	-	50	ns
Fall Time of Bit Clock	t_{FB}	t_{PB} = 488ns	-	-	50	ns
Hold Time from Bit Clock Low to Frame Sync	t_{HBF}	Long Frame Only	0	-	-	ns
Hold Time from Bit Clock High to Frame Sync	t_{HOLD}	Short Frame Only	0	-	-	ns
Set-up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80	-	-	ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL Loads	0	-	180	ns
Delay Time to $\overline{TS}_X$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL Loads	-	-	140	ns
Delay Time from $BCLK_X$ Low or FS_X Low to Data Output Disabled	t_{DZC}		50	-	165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20	-	165	ns
Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50	-	-	ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50	-	-	ns
Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50	-	-	ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100	-	-	ns

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long Frame Sync Pulse (from 3 to 8-Bit Clock Periods Long)	100	-	-	ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K Bit/s Operating Mode	160	-	-	ns

NOTE:

1. For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

Pin Descriptions

PIN NO.	SYMBOL	DESCRIPTION
1	V-	Negative power supply, V- = -5V ±5%.
2	GND	Analog and digital ground. All signals referenced to this pin.
3	VF_RO	Analog output of RECEIVE FILTER.
4	V+	Positive power supply, V+ = 5V ±5%.
5	FS_R	Receive Frame Sync Pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8kHz PULSE TRAIN.
6	D_R	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLK-SEL	The Receive Bit Clock, which shifts data into D_R after the frame sync leading edge, may vary from 64kHz to 2.048MHz. Alternatively, the leading edge may be a logic input which selects either 1.536MHz/ 1.544MHz or 2.048MHz for Master Clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/PDN	Receive Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but best performance is realized from synchronous operation. When this pin is continuously connected low, $MCLK_X$ is selected for all internal timing. When this pin is continuously connected high, the device is powered down.
9	$MCLK_X$	Transmit Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$, but best performance is realized from synchronous operation.
10	$BCLK_X$	The Bit Clock which shifts out the PCM Data on D_X. May vary from 64kHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The THREE-STATE PCM Data Output which is enabled by FS_X.
12	FS_X	Transmit Frame Sync Pulse input which enables $BCLK_X$ to shift out the data on D_X. FS_X is an 8kHz PULSE TRAIN.
13	$\overline{TS}_X$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Transmit gain adjust.
15	VF_XI-	Inverting input of the transmit input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

Functional Description

Power Supply Sequencing

Do not apply input signal or load on output before powering up V_{CC} supply. Care must be taken to ensure that D_X pin goes on common back plane (with other D_X pins from other chips). D_X pin cannot drive >50mA before Power-Up. This will cause the part to latch up.

Power-Up

When power is first applied, the Power-On reset circuitry initializes the CODEC and places it in a Power-Down mode. When the CODEC returns to an active state from the Power-Down mode, the receive output is muted briefly to minimize turn-on “click”.

To power up the device, there are two methods available.

1. A logical zero at $MCLK_R$/PDN will power up the device, provided FS_X or FS_R pulses are present.
2. Alternatively, a clock ($MCLK_R$) must be applied to $MCLK_R$/PDN and FS_X or FS_R pulses must be present.

Power-Down

Two power-down modes are available.

1. A logical 1 at $MCLK_R$/PDN, after approximately 0.5ms, will power down the device.
2. Alternatively, hold both FS_X and FS_R continuously low, the device will power down approximately 0.5ms after the last FS_X or FS_R pulse.

Synchronous Operation (Transmit and Receive Sections use the Same Master Clock)

The same master clock and bit-clock should be used for the receive and transmit sections. $MCLK_X$ (pin 9) is used to provide the master clock for the transmit section; the receive section will use the same master clock if the $MCLK_R$/PDN (pin 8) is grounded (synchronous operation), or at V+ (power-down mode). $MCLK_R$/PDN may be clocked only if a clock is provided at $BCLK_R$/CLKSEL (pin 7) as in asynchronous operation.

The $BCLK_X$ (pin 10) is used to provide the bit clock to the transmit section. In synchronous operation, this bit clock is also used for the receive section if $MCLK_R$/PDN (pin 8) is grounded. $BCLK_R$/CLKSEL (pin 7) is then used to select the proper internal frequency division for 1.544MHz, 1.536MHz or 2.048MHz operation (see Table below). For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the leading edge of $BCLK_X$. After 8 bit-clock periods, the tristate D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of the $BCLK_X$. FS_X and FS_R must be synchronous with $MCLK_X$.

CLOCKING OPTIONS

MODE	$BCLK_R$/CLKSEL (PIN 7)	MASTER CLOCK FREQUENCY SELECTED	
		CD22354A (μ)	CD22357A (A)
Asynchronous or Synchronous	Clocked	1.536MHz or 1.544MHz	2.048MHz
Synchronous	0	2.048MHz	1.536MHz or 1.544MHz
Synchronous	1(or open circuit)	1.536MHz or 1.544MHz	2.048MHz

Asynchronous Operation (Transmit and Receive Sections use Separate Master Clocks)

For the CD22357A, the $MCLK_X$ and $MCLK_R$ must be 2.048MHz and for the CD22354A must be 1.536MHz or 1.544MHz. These clocks need not be synchronous. However, for best transmission performance, it is recommended that $MCLK_X$ and $MCLK_R$ be synchronous.

For 1.544MHz operation the device automatically compensates for the 193rd clock pulse each frame. FS_X starts the encoding operation and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts the decoding operation and must be synchronous with $BCLK_R$. $BCLK_R$ must be clocked in asynchronous operation. $BCLK_X$ and $BCLK_R$ may be between 64kHz - 2.04MHz.

Short-Frame Sync Mode

When the power is first applied, the power initialization circuitry places the CODEC in a short-frame sync mode. In this mode both frame sync pulses must be 1 bit-clock period long, with the timing relationship shown in Figure 1.

With FS_X high during the falling edge of the $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X tristate output buffer, which will output the sign bit. The following rising seven edges clock out the remaining seven bits upon which the next falling edge will disable the D_X output.

With FS_R high during the falling edge of the $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven edges latch in the seven remaining bits.

Long-Frame Sync Mode

In this mode of operation, both of the frame sync pulses must be three or more bit-clock periods long with the timing relationship shown in Figure 2.

Based on the transmit frame sync FS_X, the CODEC will sense whether short or long-frame sync pulses are being used.

For 64kHz operation the frame sync pulse must be kept low for a minimum of 160ns.

The D_X tristate output buffer is enabled with the rising edge of FS_X or the rising edge of the $BCLK_X$, whichever comes later and the first bit clocked out is the sign bit. The following seven rising edges of the $BCLK_X$ clock out the remaining seven bits. The D_X output is disabled by the next falling edge of the $BCLK_X$ following the 8th rising edge or by FS_X going low whichever comes later.

A rising edge on the receive frame sync, FS_R, will cause the PCM data at D_R to be latched in on the next falling edge of the $BCLK_R$. The remaining seven bits are latched on the successive seven falling edges of the bit-clock ($BCLK_X$ in synchronous mode).

Transmit Section

The transmit section consists of a gain-adjustable input op-amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input op-amp drives a RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30dB attenuation (Min) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128kHz, followed by a 3rd order high-pass filter clock at 32kHz. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8kHz sampling rate. A precision voltage reference is trimmed in manufacturing to provide an input overload of nominally $2.5V_{PEAK}$. Transmit frame sync pulse FS_X controls the process. The 8-bit PCM data is clocked out at D_X by the $BCLK_X$. $BCLK_X$ can be varied from 64kHz to 2.048MHz.

Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at D_R upon the occurrence of FS_R, Receive Frame sync pulse. $BCLK_R$, Receive Data Clock, which can range from 64kHz to 2.048MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clocked at 128kHz to smooth the sample-and-hold signal as well as to compensate for the (SIN X)/X distortion.

The filter is then followed by a second order Sallen and Key active filter capable of driving a 600Ω load to a level of 7.2dBm.

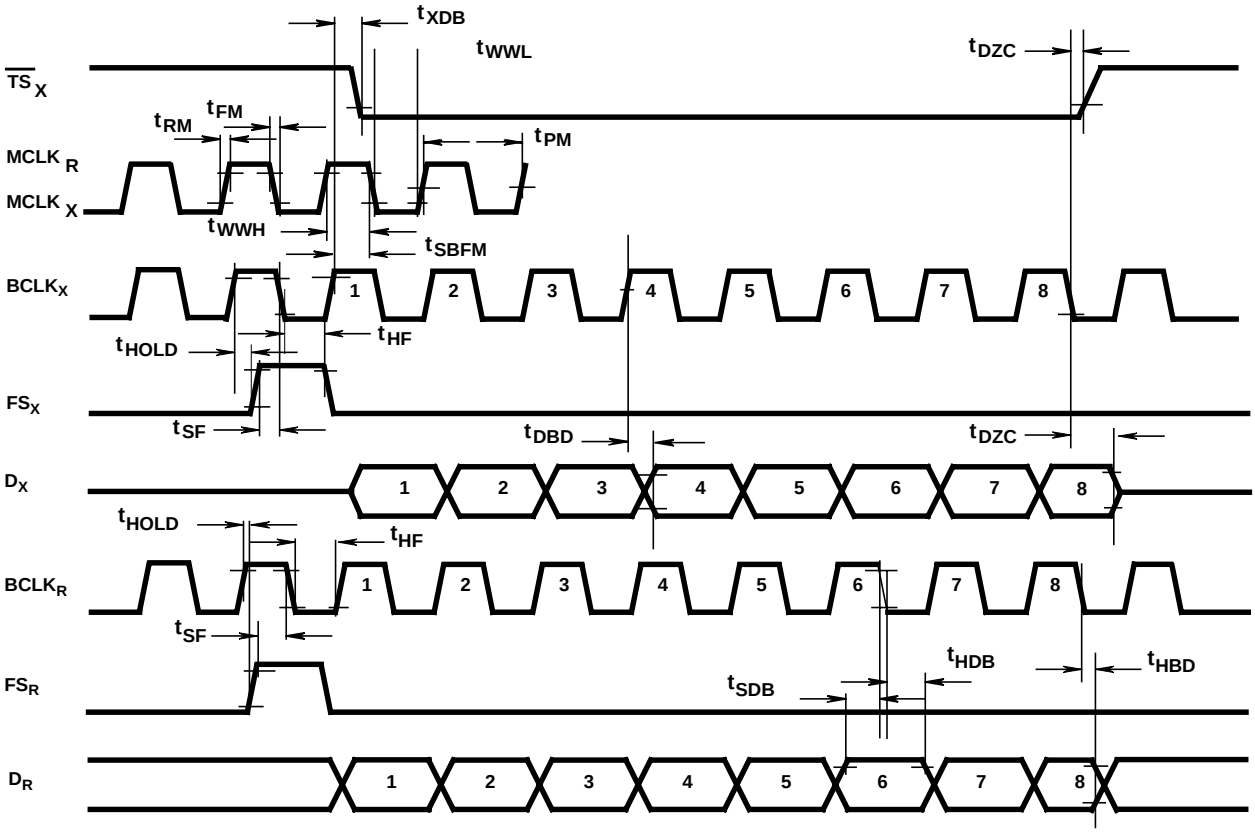


FIGURE 1. SHORT FRAME-SYNC TIMING

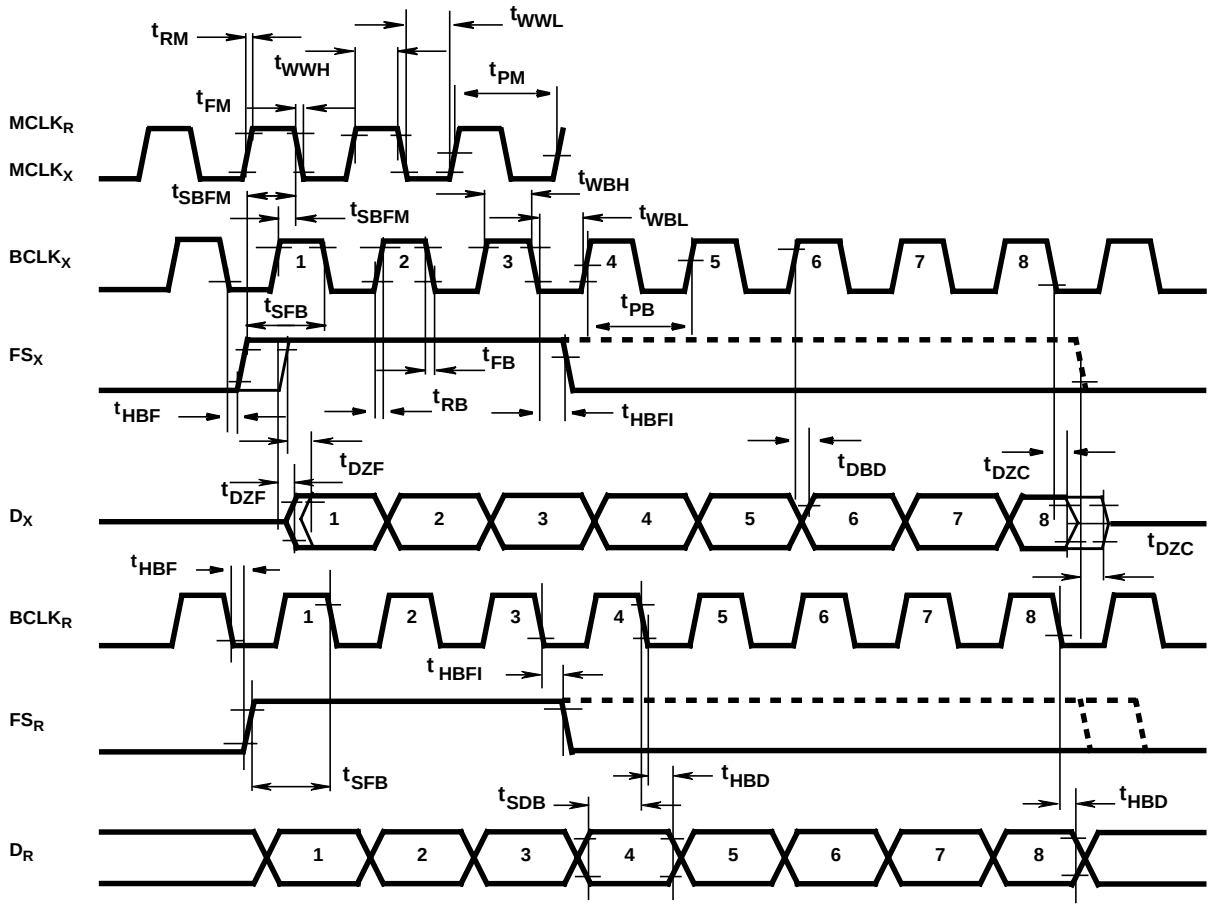


FIGURE 2. LONG FRAME-SYNC TIMING