

April 1999

**OBSOLETE PRODUCT  
FOR A POSSIBLE SUBSTITUTE PRODUCT  
call Central Applications 1-800-442-7747  
or email: centapp@harris.com**

### Features

- Direct RESET
- TTL and CMOS Compatible Address and Enable Inputs
- Maximum Power Supply Rating ..... 44V
- Break-Before-Make Switching
- Alternate Source

### Applications

- Data Acquisition Systems
- Communication Systems
- Automatic Test Equipment
- Microprocessor Controlled Systemd

### Description

The DG526, DG527, DG528, and DG529 are CMOS Monolithic 16-Channel/Dual 4-Channel Analog Multiplexers. Each device has on-chip address and control latches to simplify design in microprocessor based applications. The DG526 uses 4 address lines to control its 16 channels; the DG527, DG528 both use 3 address lines to control their 8 channels; and the DG529 uses 2 address lines to control its 4 channels. The enable pin is used to enable the address latches during the  $\overline{WR}$  pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The  $\overline{RS}$  pin is used to clear all latches regardless of the state of any other latch or control line. The  $\overline{WR}$  pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low.

A channel in the ON state conducts signals equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs,  $\overline{WR}$ ,  $\overline{RS}$  and the enable input are TTL and CMOS compatible over the full specified operation temperature range.

### Part Number Information

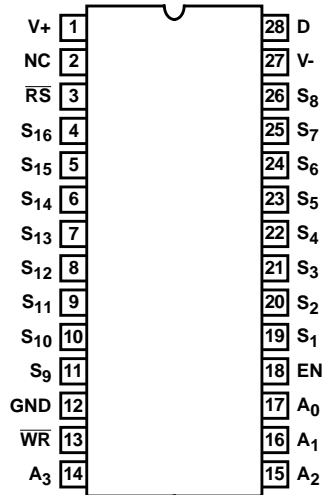
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG526AK	-55 to 125	28 Ld CERDIP	F28.6
DG526AK/883B	-55 to 125	28 Ld CERDIP	F28.6
DG526BK	-25 to 85	28 Ld CERDIP	F28.6
DG526BY	-25 to 85	28 Ld SOIC	M28.3
DG526CJ	0 to 70	28 Ld PDIP	E28.6
DG526CK	0 to 70	28 Ld CERDIP	F28.6
DG526CY	0 to 70	28 Ld SOIC	M28.3
DG527AK	-55 to 125	28 Ld CERDIP	F28.6
DG527AK/883B	-55 to 125	28 Ld CERDIP	F28.6
DG527BK	-25 to 85	28 Ld CERDIP	F28.6
DG527BY	-25 to 85	28 Ld SOIC	M28.3
DG527CJ	0 to 70	28 Ld PDIP	E28.6
DG527CK	0 to 70	28 Ld CERDIP	F28.6
DG527CY	0 to 70	28 Ld SOIC	M28.3

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG528AK	-55 to 125	18 Ld CERDIP	F18.3
DG528AK/883B	-55 to 125	18 Ld CERDIP	F18.3
DG528BK	-25 to 85	18 Ld CERDIP	F18.3
DG528BY	-25 to 85	18 Ld SOIC	M18.3
DG528CJ	0 to 70	18 Ld PDIP	E18.3
DG528CK	0 to 70	18 Ld CERDIP	F18.3
DG528CY	0 to 70	18 Ld SOIC	M18.3
DG529AK	-55 to 125	18 Ld CERDIP	F18.3
DG529AK/883B	-55 to 125	18 Ld CERDIP	F18.3
DG529BK	-25 to 85	18 Ld CERDIP	F18.3
DG529BY	-25 to 85	18 Ld SOIC	M18.3
DG529CJ	0 to 70	18 Ld PDIP	E18.3
DG529CK	0 to 70	18 Ld CERDIP	F18.3
DG529CY	0 to 70	18 Ld SOIC	M18.3

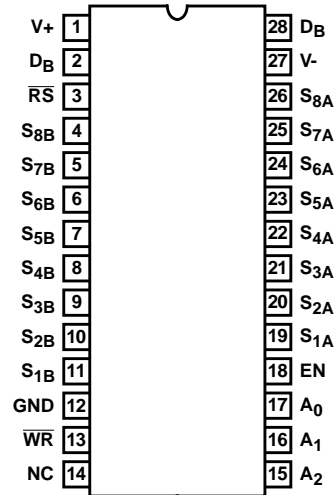
# DG526, DG527, DG528, DG529

## Pinouts

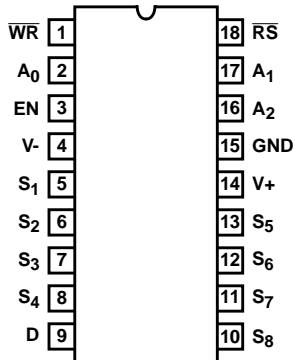
**DG526**  
(PDIP, CERDIP, SOIC)  
TOP VIEW



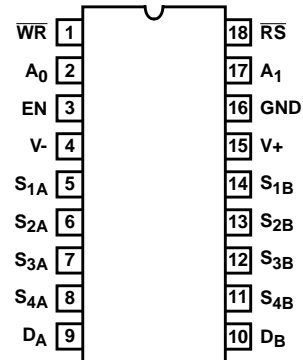
**DG527**  
(PDIP, CERDIP, SOIC)  
TOP VIEW



**DG528**  
(PDIP, CERDIP, SOIC)  
TOP VIEW

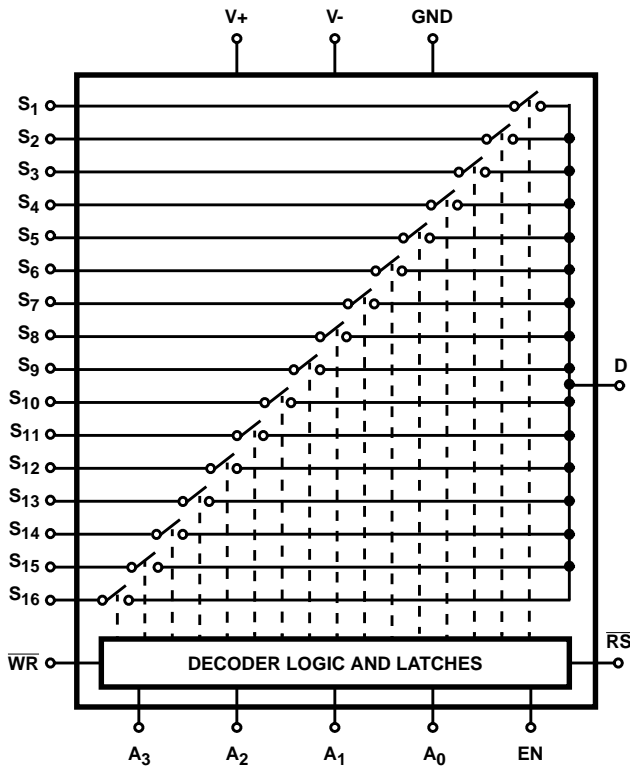


**DG529**  
(PDIP, CERDIP, SOIC)  
TOP VIEW

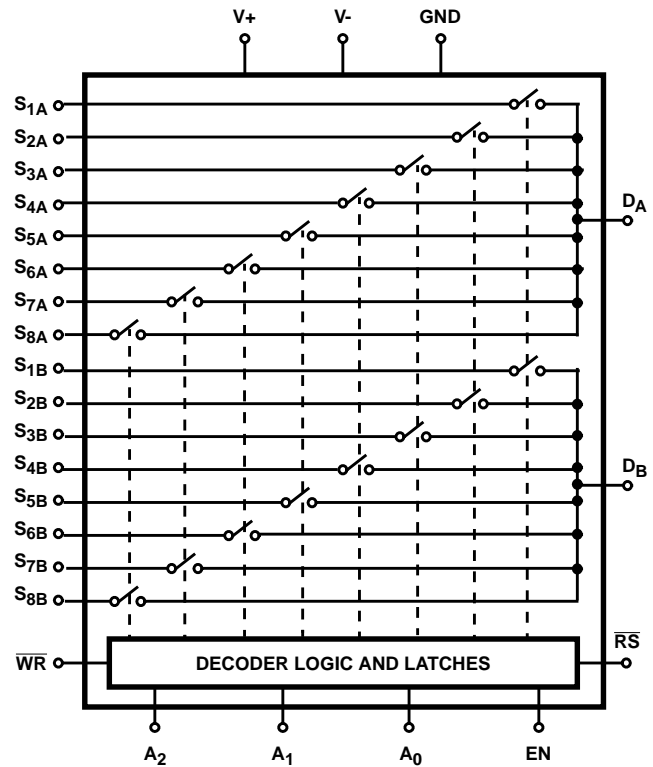


Functional Diagrams

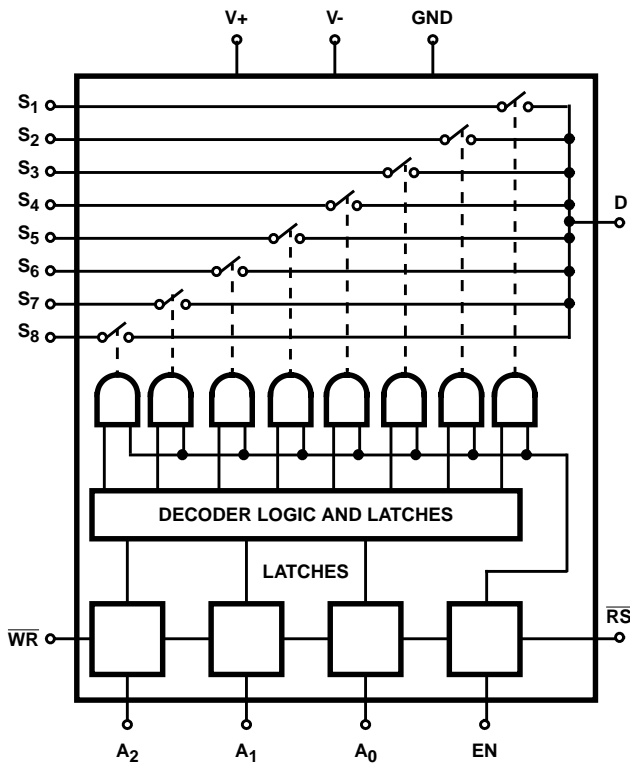
DG526  
16-CHANNEL SINGLE ENDED MULTIPLEXER



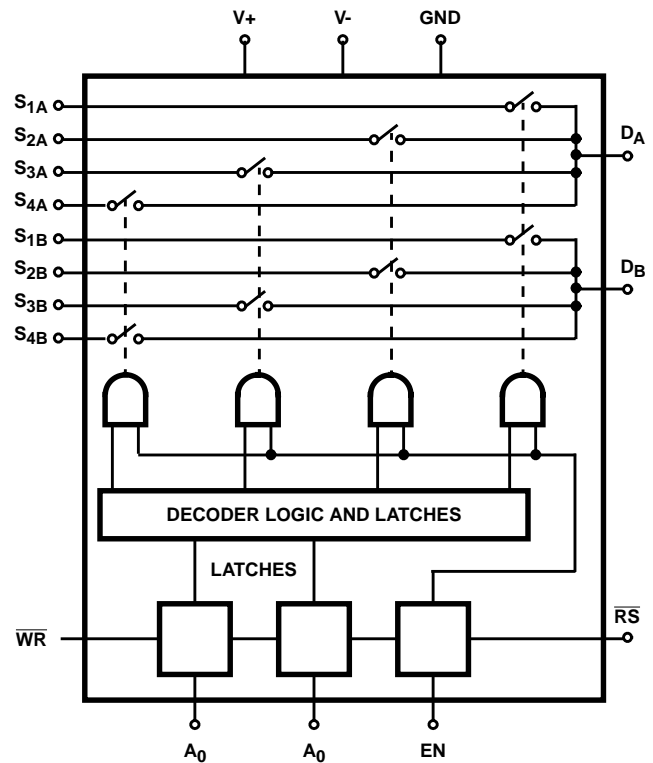
DG527  
DIFFERENTIAL 8-CHANNEL MULTIPLEXER



DG528  
8-CHANNEL SINGLE ENDED MULTIPLEXER

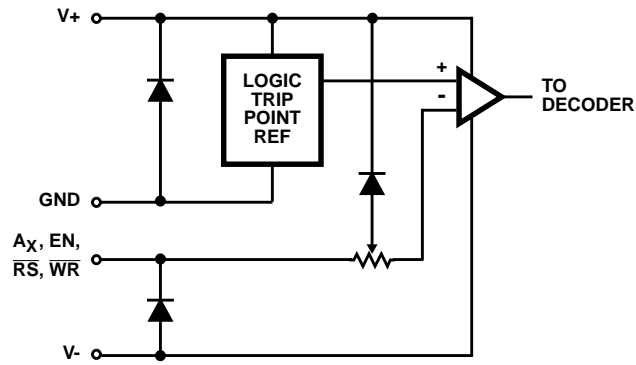


DG529  
DUAL 4-CHANNEL MULTIPLEXER

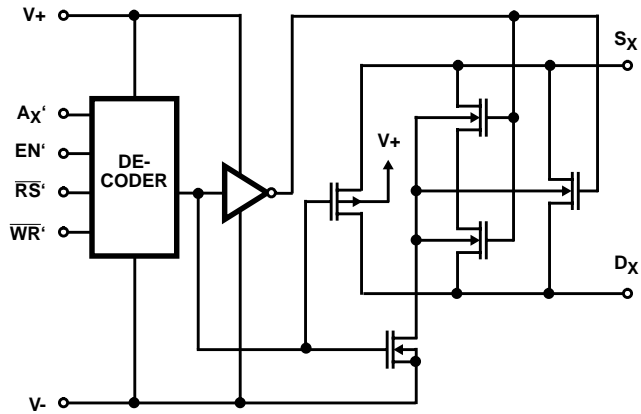


Schematic Diagrams

LOGIC INTERFACE AND LEVEL SHIFTER



DECODER AND SWITCH



# DG526, DG527, DG528, DG529

## Absolute Maximum Ratings

V+ to V-	+44V
V- to Ground	-25V
V <sub>IN</sub> to Ground (Note 1)	(V- - 2V), (V+ + 2V)
V <sub>S</sub> or V <sub>D</sub> to V+ (Note 1)	+2V, (V- - 2V)
V <sub>S</sub> or V <sub>D</sub> to V- (Note 1)	-2V, (V+ + 2V)
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max)	40mA

## Operating Conditions

Operating Temperature	
C Suffix	0°C to 70°C
B Suffix	-25°C to 85°C
A Suffix	-55°C to 125°C

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
18 Ld PDIP Package	90	N/A
18 Ld CERDIP Package	75	22
18 Ld SOIC Package	95	N/A
28 Ld PDIP Package	60	N/A
28 Ld CERDIP Package	55	18
28 Ld SOIC Package	70	N/A
Maximum Junction Temperature		
Ceramic Packages	175°C	
Plastic Packages	150°C	
Maximum Storage Temperature Range		
C Suffix	-65°C to 125°C	
A and B Suffix	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications (Note 3) V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, T<sub>A</sub> = 25°C, Unless Otherwise Specified

PARAMETER	(NOTE 6) TEST CONDITIONS	A SUFFIX			B AND C SUFFIX			UNITS		
		MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX			
<b>DYNAMIC</b>										
Switching Time of Multiplexer, $t_{\text{TRANSITION}}$	DG526, DG527	See Figure 3 (Note 7)		-	0.65	1	-	0.65	-	$\mu\text{s}$
	DG528, DG529	See Figure 3		-	0.6	1	-	0.6	-	$\mu\text{s}$
Break-Before-Make Interval, $t_{\text{OPEN}}$	DG526, DG527	See Figure 4		-	0.2	-	-	0.2	-	$\mu\text{s}$
	DG528, DG529			-	0.2	-	-	0.2	-	$\mu\text{s}$
Enable and Write Turn-ON Time, $t_{\text{ON}}(\text{EN}, \overline{\text{WR}})$	DG526, DG527	See Figures 1, 6 (Note 7)		-	0.7	1.5	-	0.7	-	$\mu\text{s}$
	DG528, DG529	See Figures 5, 6 (Note 7)		-	1	1.5	-	1	-	$\mu\text{s}$
Enable and Reset Turn OFF Time, $t_{\text{OFF}}(\text{EN}, \overline{\text{RS}})$	DG526, DG527	See Figures 2, 7 (Note 7)		-	0.4	1	-	0.4	-	$\mu\text{s}$
	DG528, DG529	See Figures 5, 6 (Note 7)		-	0.4	1	-	0.4	-	$\mu\text{s}$
Off Isolation, OIRR	DG526, DG527	$V_{\text{EN}} = 0\text{V}$ , $R = 1\text{k}\Omega$ , $C_{\text{L}} = 15\text{pF}$ , $V_{\text{S}} = 7V_{\text{RMS}}$ , $f = 500\text{kHz}$ (Note 4)		-	55	-	-	55	-	dB
	DG528, DG529			-	68	-	-	68	-	dB
Logic Input Capacitance, $C_{\text{IN}}$	DG526, DG527	$f = 1\text{MHz}$		-	6	-	-	6	-	pF
	DG528, DG529			-	2.5	-	-	2.5	-	pF
Source OFF Capacitance, $C_{\text{S(OFF)}}$	DG526, DG527	$V_{\text{S}} = 0\text{V}$	$V_{\text{EN}} = 0\text{V}$ , $f = 140\text{kHz}$	-	10	-	-	10	-	pF
	DG528, DG529			-	5	-	-	5	-	pF

**DG526, DG527, DG528, DG529**

**Electrical Specifications** (Note 3)  $V_+ = +15V$ ,  $V_- = -15V$ ,  $GND = 0V$ ,  $WR = 0V$ ,  $RS = 2.4V$ ,  $EN = 2.4V$ ,  $T_A = 25^\circ C$ ,  
Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX			B AND C SUFFIX			UNITS
				MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
Drain OFF Capacitance, $C_{D(OFF)T}$	DG526	$V_D = 0V$	$V_{EN} = 0V$ , $f = 140kHz$	-	65	-	-	65	-	pF
	DG527			-	35	-	-	35	-	pF
	DG528			-	25	-	-	25	-	pF
	DG529			-	12	-	-	12	-	pF
Charge Injection, Q	DG526, DG527	See Figure 8		-	6	-	-	6	-	pC
	DG528, DG529			-	4	-	-	4	-	pC
<b>INPUT</b>										
Address Input Current, Input Voltage High, $I_{AH}$	DG526, DG527	$V_A = 2.4V$		-10	0.02	-	-10	0.02	-	$\mu A$
		$V_A = 15V$		-	0.02	10	-	0.02	10	$\mu A$
	DG528, DG529	$V_A = 2.4V$		-10	-0.002	-	-10	-0.002	-	$\mu A$
		$V_A = 15V$		-	0.006	10	-	0.006	10	$\mu A$
Address Input Current, Input Voltage Low, $I_{AL}$	DG526, DG527	$V_{EN} = 2.4V$	All $V_A = 0V$ , $\overline{RS} = 0V$ , $\overline{WR} = 0V$	-10	0.01	-	-10	0.01	-	$\mu A$
		$V_{EN} = 0V$		-10	0.01	-	-10	0.01	-	$\mu A$
	DG528, DG529	$V_{EN} = 2.4V$		-10	-0.002	-	-10	-0.002	-	$\mu A$
		$V_{EN} = 0V$		-10	-0.002	-	-10	-0.002	-	$\mu A$
<b>SWITCH</b>										
Analog Signal Range, $V_{ANALOG}$	(Note 7)			-15	-	+15	-15	-	+15	V
Drain Source ON Resistance, $r_{DS(ON)}$	$V_D = \pm 10V$ , $V_{AL} = 0.8V$ , $V_{AH} = 2.4V$ , $I_L = -200\mu A$ Sequence Each Switch ON			-	270	400	-	270	450	$\Omega$
Greatest Change in Drain Source ON Resistance Between Channels, $\Delta r_{DS(ON)}$	$-10V \leq V_S \leq 10V$ $Dr_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG.}}$			-	6	-	-	6	-	%
Source OFF Leakage Current, $I_{S(OFF)}$	DG526, DG527	$V_{EN} = 0V$	$V_S = \pm 10V$ , $V_D = +10V$	-1	0.02	1	-	0.02	-	nA
	DG528, DG529		$V_S = \pm 10V$ , $V_D = +10V$	-1	-0.005	1	-5	-0.005	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	DG526	$V_{EN} = 0V$	$V_S = \pm 10V$ , $V_D = +10V$	-10	0.2	10	-	0.2	-	nA
	DG527		$V_S = \pm 10V$ , $V_D = +10V$	-5	0.2	5	-	0.2	-	nA
	DG528		$V_S = \pm 10V$ , $V_D = +10V$	-10	-0.015	10	-20	0.015	20	nA
	DG529		$V_S = \pm 10V$ , $V_D = +10V$	-10	-0.008	10	-20	0.008	20	nA
Drain ON Leakage Current, $I_{D(ON)}$	DG526	Sequence Each Switch On $V_{AL} = 0.8V$ and $V_{AH} = 2.4V$ (Note 5)	$V_D = V_S(ALL) = \pm 10V$	-10	0.2	10	-	0.2	-	nA
	DG527		$V_D = V_S(ALL) = \pm 10V$	-5	0.2	5	-	0.2	-	nA

**DG526, DG527, DG528, DG529**

**Electrical Specifications** (Note 3)  $V_+ = +15V$ ,  $V_- = -15V$ , GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V,  $T_A = 25^\circ C$ , Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 6) TEST CONDITIONS	A SUFFIX			B AND C SUFFIX			UNITS	
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX		
Drain ON Leakage Current, $I_{D(ON)}$ (Continued)	DG528	Sequence Each Switch On $V_{AL} = 0.8V$ and $V_{AH} = 2.4V$ (Note 5)	$V_D = V_{S(ALL)} = \pm 10V$	-10	-0.03	10	-20	-0.03	20	nA
	DG529		$V_D = V_{S(ALL)} = \pm 10V$	-10	-0.015	10	-20	-0.015	20	nA
<b>SUPPLY</b>										
Positive Supply Current, $I_+$	DG526, DG527	$V_{EN} = 0V$	All $V_A = 0V$	-	2.0	3.0	-	2.0	-	mA
	DG528, DG529			-	-	2.5	-	-	-2.5	mA
Positive Supply Current, $I_-$	DG526, DG527	$V_{EN} = 0V$	All $V_A = 0V$	-2.0	-1.2	-	-	-1.2	-	mA
	DG528, DG529			-1.5	-	-	-1.5	-	-	mA

**Electrical Specifications**  $T_A =$  Over Operating Temperature Range,  $V_+ = +15V$ ,  $V_- = -15V$ , GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V Unless Otherwise Specified

PARAMETER		(NOTE 6) TEST CONDITIONS	A SUFFIX			B AND C SUFFIX			UNITS		
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX			
<b>INPUT</b>											
Address Input Current Input Voltage High, $I_{AH}$		$V_A = 2.4V$		-30	-	-	-30	-	-	$\mu A$	
		$V_A = 15V$		-	-	30	-	-	30	$\mu A$	
Address Input Current, Input Voltage Low, $I_{AL}$	DG526, DG527	$V_A = 2.4V$	$V_{A(ALL)} = 0V,$	-10	-	-	-	-	-	$\mu A$	
		$V_A = 0V$	$\overline{RS} = 0V,$	-10	-	-	-	-	-	$\mu A$	
	DG528, DG529		$WR = 0V$		-30	-	-	-30	-	-	$\mu A$
		$V_A = 0V$			-30	-	-	-30	-	-	$\mu A$
<b>SWITCH</b>											
Analog Signal Range, $V_{ANALOG}$		Note 7		-15	-	+15	-	-	-	%	
Drain Source ON Resistance, $r_{DS(ON)}$		$V_D = \pm 10V, V_{AL} = 0.8V, V_{AH} = 2.4V, I_S = -200\mu A,$ Sequence Each Switch ON		-	-	500	-	-	500	$\Omega$	
Source Off Leakage Current, $I_{S(OFF)}$		$V_{EN} = 0V$	$V_S = \pm 10V, V_D = \mp 10V$	-50	-	50	-	-	-	nA	
Drain OFF Leakage Current, $I_{D(OFF)}$	DG526	$V_{EN} = 0V$	$V_S = \pm 10V, V_D = \mp 10V$	-300	-	300	-300	-	300	nA	
	DG527			-200	-	200	-200	-	200	nA	
	DG528		$V_S = \mp 10V, V_D = \pm 10V$	-200	-	200	-200	-	200	nA	
	DG529			-100	-	100	-100	-	100	nA	
Drain ON Leakage Current, $I_{D(ON)}$	DG526	Sequence Each Switch On, $V_{AL} = 0.8V, V_{AH} = 2.4V$ (Note 5)	$V_D = V_{S(ALL)} = \pm 10V$	-300	-	300	-300	-	300	nA	
	DG527			-200	-	200	-200	-	200	nA	
	DG528			-200	-	200	-200	-	200	nA	
	DG529			-100	-	100	-100	-	100	nA	

# DG526, DG527, DG528, DG529

## Minimum Input Timing Requirements Over Full Temperature Range

PARAMETER	MEASURED TERMINAL	MIN	UNITS
WRITE Pulse Width, $t_{WW}$	$\overline{WR}$ , See Figure 1	300	ns
A, EN Data Valid After WRITE (Stabilization Time), $t_{DW}$	$A_0, A_1, (A_2), EN, \overline{WR}$ ; See Figure 1	180	ns
A, EN Data Valid After WRITE (Hold Time), $t_{WD}$	$A_0, A_1, (A_2), EN, \overline{WR}$ ; See Figure 1	30	ns
RESET Pulse Width, $t_{RS}$	$\overline{RS}$ , (Note 6), $V_S = 5V$ , See Figure 2	500	ns

**NOTES:**

1. Signals on  $V_S, V_D$  or  $V_{IN}$  exceeding  $V+$  or  $V-$  will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and most positive value is a maximum, is used in this datasheet.
4. OFF Isolation =  $20 \frac{|V_S|}{|V_D|}$ , where  $V_S$  = input to OFF switch, and  $V_D$  = output due to  $V_S$ .
5.  $I_{D(ON)}$  is leakage from driver into "ON" switch.
6. Period of Reset ( $\overline{RS}$ ) pulse must be at least 50 $\mu$ s during or after power ON.
7. Parameter not tested. Parameter guaranteed by design or characterization.

## Test Circuits and Waveforms

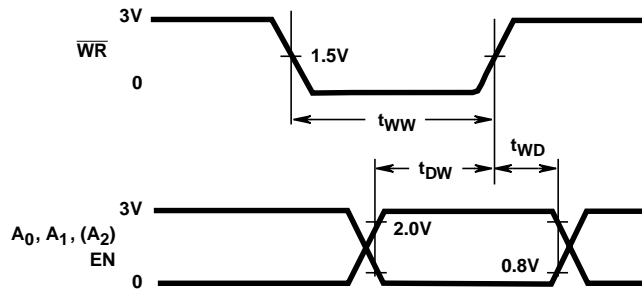


FIGURE 1.  $\overline{WR}$  TIMING WAVEFORMS

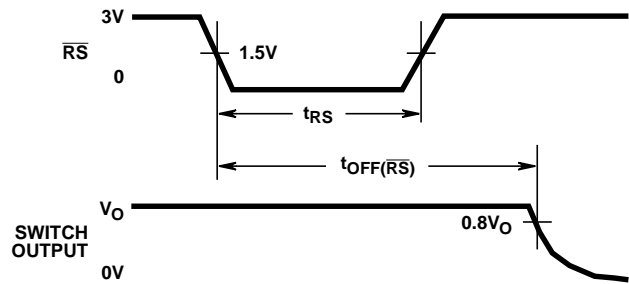


FIGURE 2.  $\overline{RS}$  TIMING WAVEFORMS

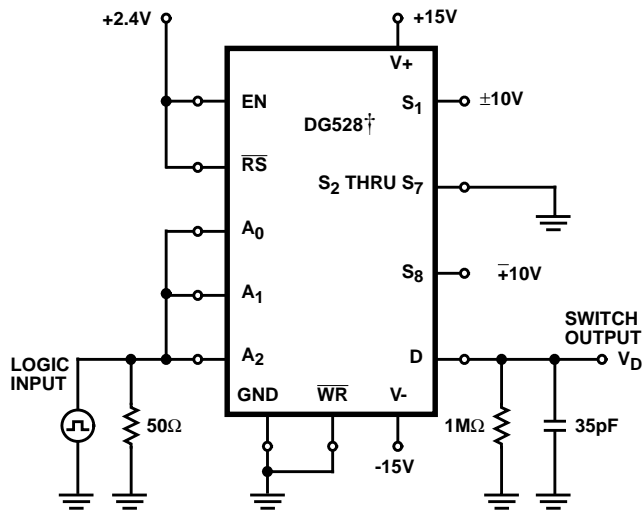


FIGURE 3A.  $t_{TRANSITION}$  SWITCHING TIME TEST CIRCUIT

† Similar connections for DG526

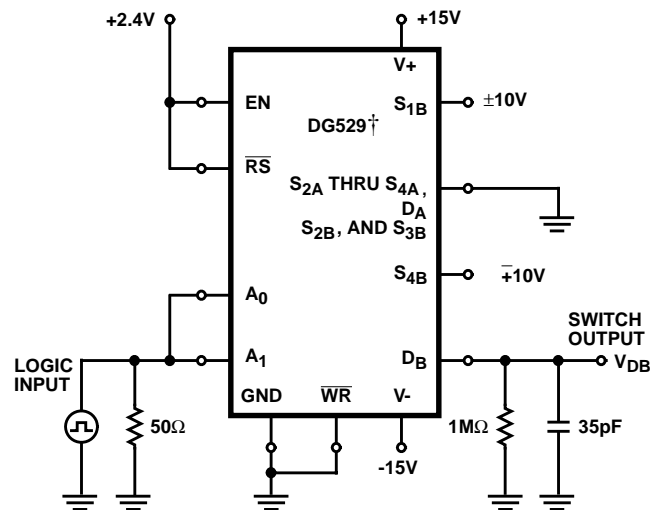


FIGURE 3B.  $t_{TRANSITION}$  SWITCHING TIME TEST CIRCUIT

† Similar connections for DG527



Test Circuits and Waveforms (Continued)

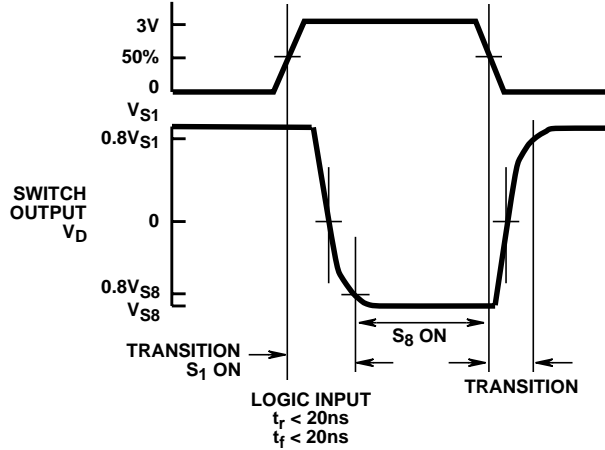


FIGURE 3C.  $t_{\text{TRANSITION}}$  SWITCHING TIME WAVEFORM

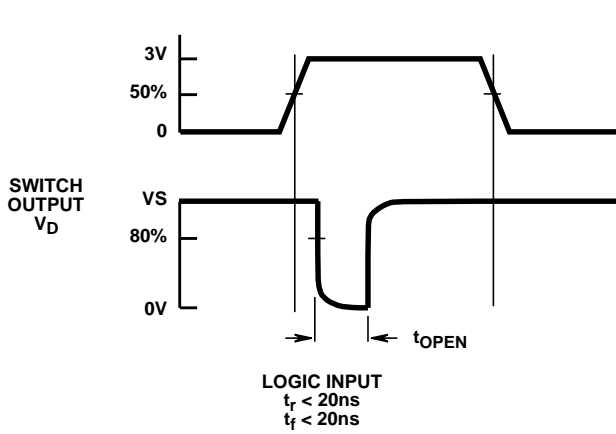


FIGURE 4A.  $t_{\text{OPEN}}$  (BREAK-BEFORE-MAKE) SWITCHING TIME WAVEFORM

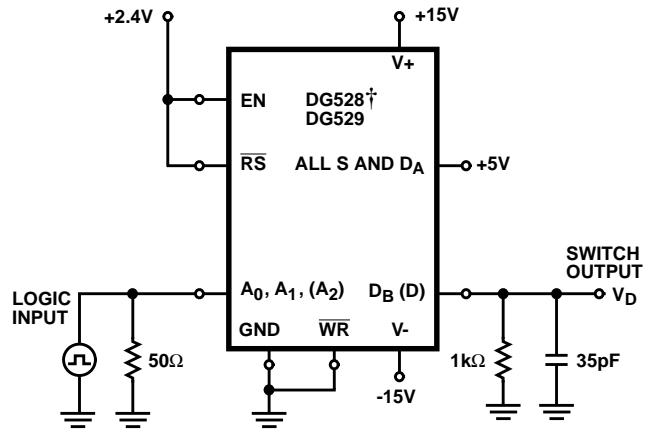


FIGURE 4B.  $t_{\text{OPEN}}$  (BREAK-BEFORE-MAKE) SWITCHING TIME TEST CIRCUIT

† Similar connections for DG526, DG527

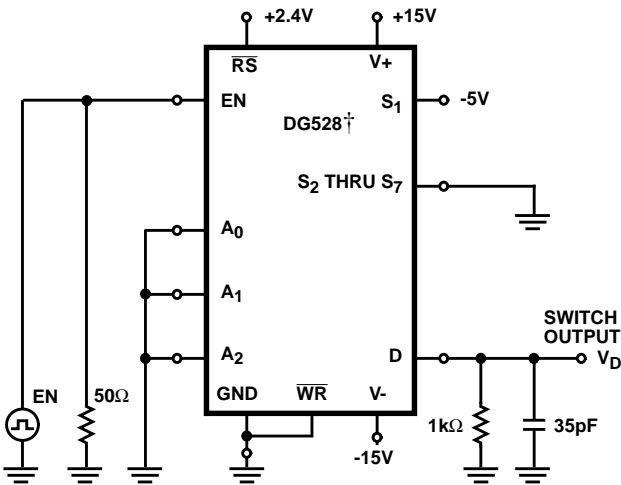


FIGURE 5A. ENABLE  $t_{\text{ON}}$  AND  $t_{\text{OFF}}$  SWITCHING TIME TEST CIRCUIT

† Similar connections for DG526

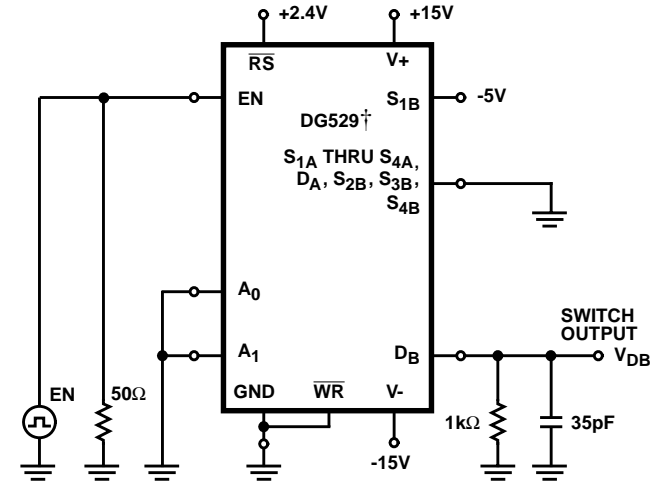


FIGURE 5B. ENABLE  $t_{\text{ON}}$  AND  $t_{\text{OFF}}$  SWITCHING TIME TEST CIRCUIT

† Similar connections for DG527

Test Circuits and Waveforms (Continued)

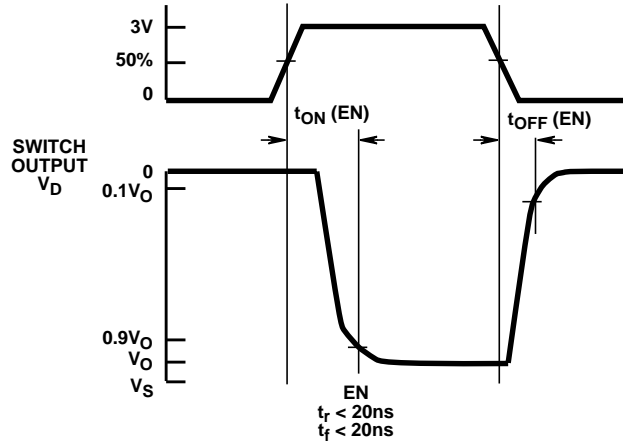


FIGURE 5C. ENABLE  $t_{ON}$  AND  $t_{OFF}$  SWITCHING TIME WAVEFORMS

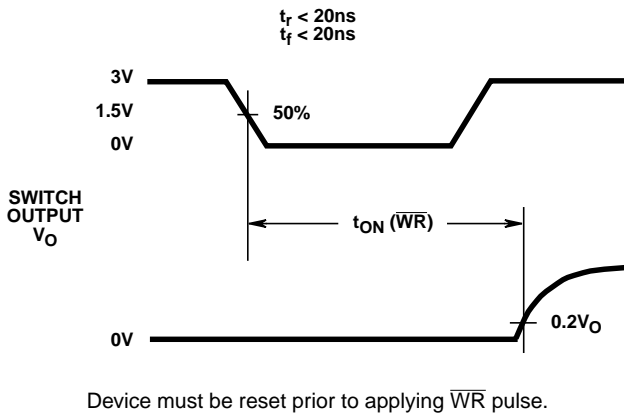


FIGURE 6A. WRITE  $t_{ON}$  SWITCHING TIME WAVEFORMS

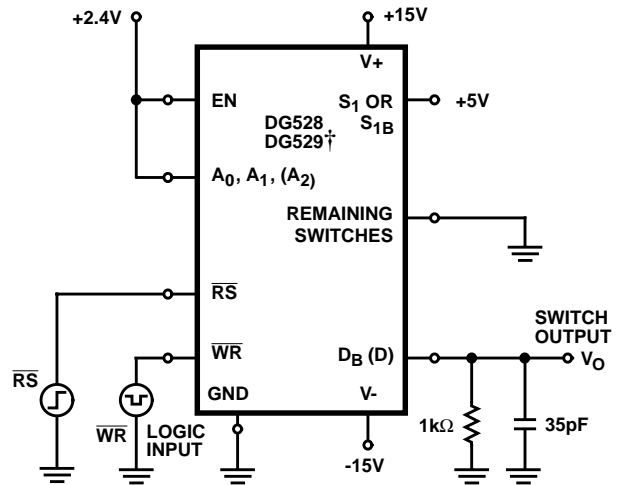


FIGURE 6B. WRITE  $t_{ON}$  SWITCHING TIME TEST CIRCUIT  
† Similar connections for DG526, DG527

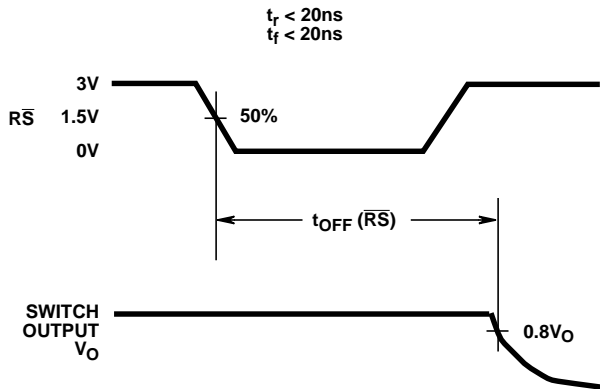


FIGURE 7A. RESET  $t_{OFF}$  SWITCHING TIME WAVEFORMS

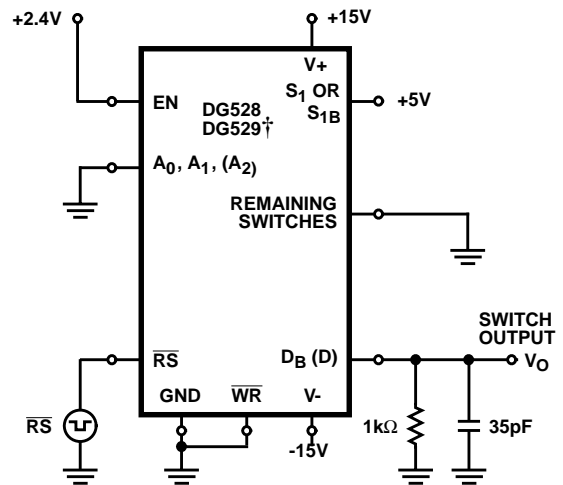
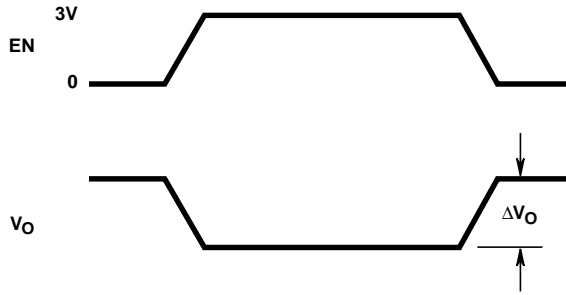


FIGURE 7B. RESET  $t_{OFF}$  SWITCHING TIME TEST CIRCUIT  
† Similar connections for DG526, DG527

Test Circuits and Waveforms (Continued)



$\Delta V_O$  is the measured voltage error due to charge injection. The error voltage in Coulombs is  $Q = C_L \times \Delta V_O$ .

FIGURE 8A. CHARGE INJECTION WAVEFORMS

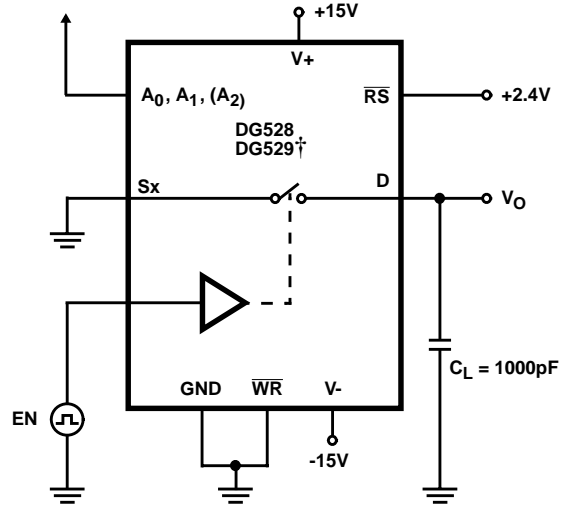


FIGURE 8B. CHARGE INJECTION TEST CIRCUIT

† Similar connections for DG526, DG527

Typical Performance Curves

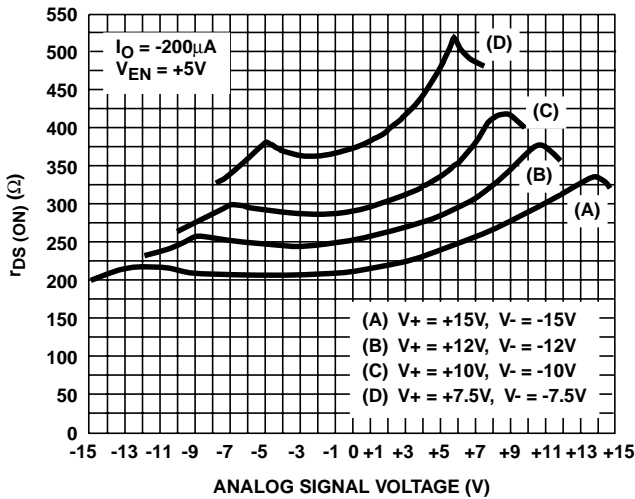


FIGURE 9.  $r_{DS(ON)}$  vs ANALOG SIGNAL VOLTAGE vs SUPPLY VOLTAGE

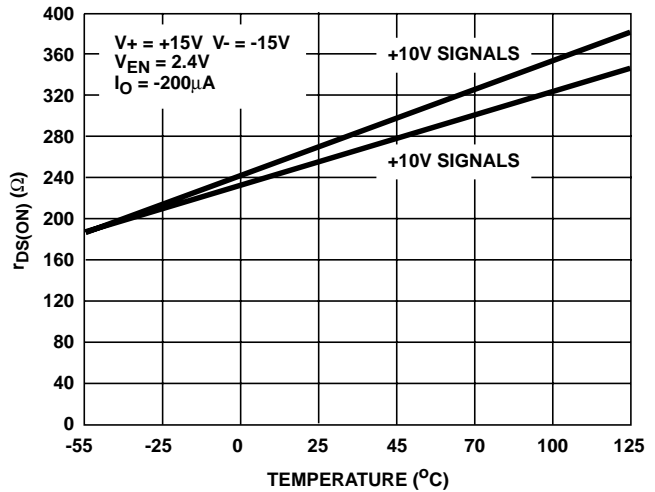


FIGURE 10. TYPICAL  $r_{DS(ON)}$  VARIATION WITH TEMPERATURE

DG526, DG527, DG528, DG529

Truth Tables

DG526

	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching	X	X	X	X	X		1	Maintains Previous Switch State
Reset	X	X	X	X	X	X	0	None (Latches Cleared)
Trans-parent Operation	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
	0	1	1	1	1	0	1	8
	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16	

Logic "0" = V<sub>AL</sub>, V<sub>ENL</sub> ≤ 0.8V

DG527

	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching	X	X	X	X		1	Maintains Previous Switch State
Reset	X	X	X	X	X	0	None (Latches Cleared)
Trans-parent Operation	X	X	X	0	0	1	None
	0	0	0	1	0	1	1
	0	0	1	1	0	1	2
	0	1	0	1	0	1	3
	0	1	1	1	0	1	4
	1	0	0	1	0	1	5
	1	0	1	1	0	1	6
	1	1	0	1	0	1	7
	1	1	1	1	0	1	8

Logic "1" = V<sub>AH</sub>, V<sub>ENH</sub> ≥ 2.4V

DG528

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X		1	Maintains Previous Switch Condition
X	X	X	X	X	0	None (Latches Cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X		1	Maintains Previous Switch Condition
X	X	X	X	0	None (Latches Cleared)
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": V<sub>AH</sub> ≥ 2.4V  
 Logic "0": V<sub>AL</sub> ≤ 0.8V

**Die Characteristics**

**DIE DIMENSIONS:**

3810 $\mu$ m x 2769 $\mu$ m

**METALLIZATION:**

Type: Al

Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

**PASSIVATION:**

Type: PSG Over Nitride

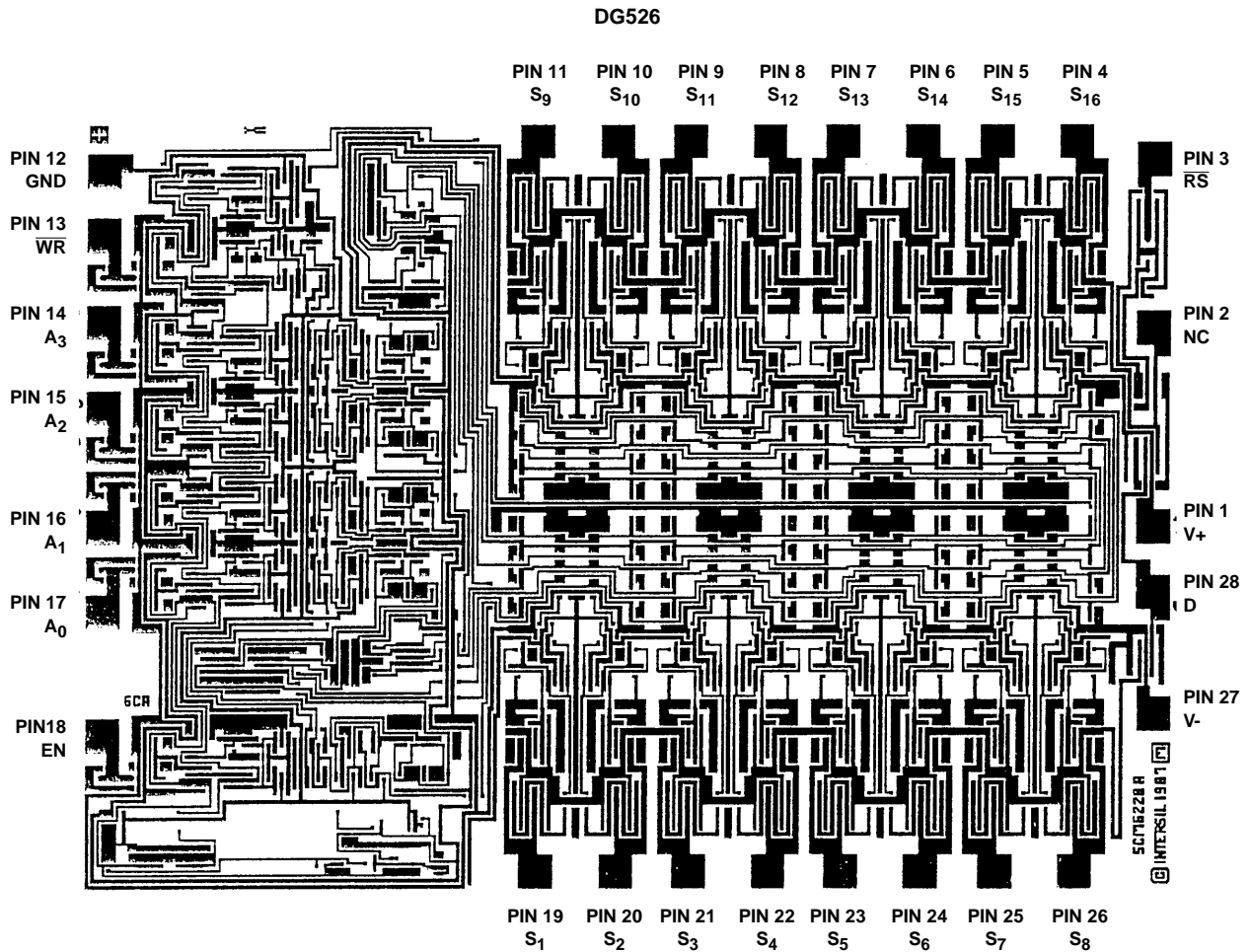
PSG Thickness: 7k $\text{\AA}$   $\pm$  1.4k $\text{\AA}$

Nitride Thickness: 8k $\text{\AA}$   $\pm$  1.2k $\text{\AA}$

**WORST CASE CURRENT DENSITY:**

9.1 x 10<sup>4</sup> A/cm<sup>2</sup>

**Metallization Mask Layout**



**Die Characteristics**

**DIE DIMENSIONS:**

3810 $\mu$ m x 2769 $\mu$ m

**METALLIZATION:**

Type: Al

Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

**PASSIVATION:**

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$   $\pm$  1.4k $\text{\AA}$

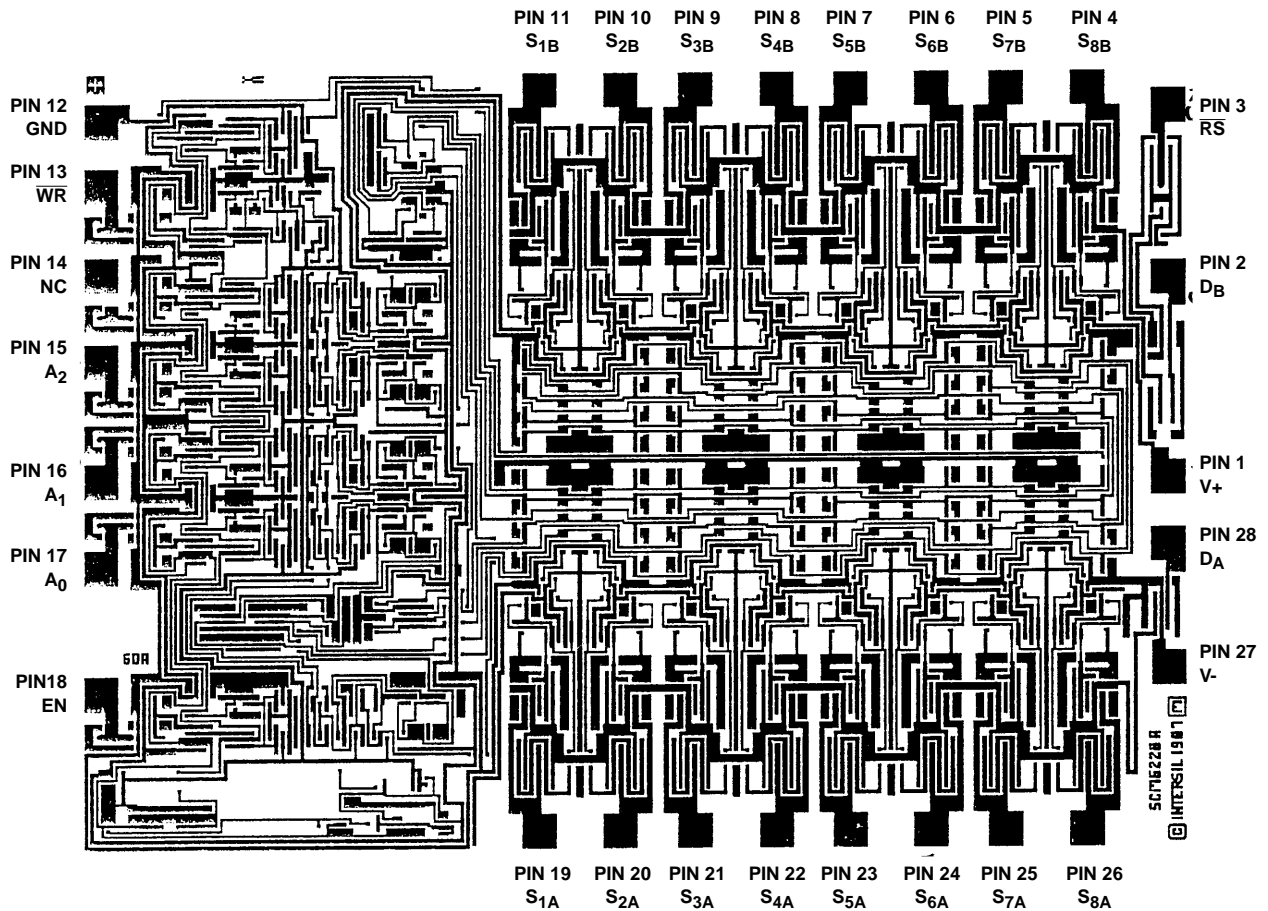
Nitride Thickness: 8k $\text{\AA}$   $\pm$  1.2k $\text{\AA}$

**WORST CASE CURRENT DENSITY:**

9.1 x 10<sup>4</sup> A/cm<sup>2</sup>

**Metallization Mask Layout**

DG527



# DG526, DG527, DG528, DG529

## Die Characteristics

### DIE DIMENSIONS:

3100 $\mu$ m x 2083 $\mu$ m

### METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

### PASSIVATION:

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$   $\pm$  1.4k $\text{\AA}$

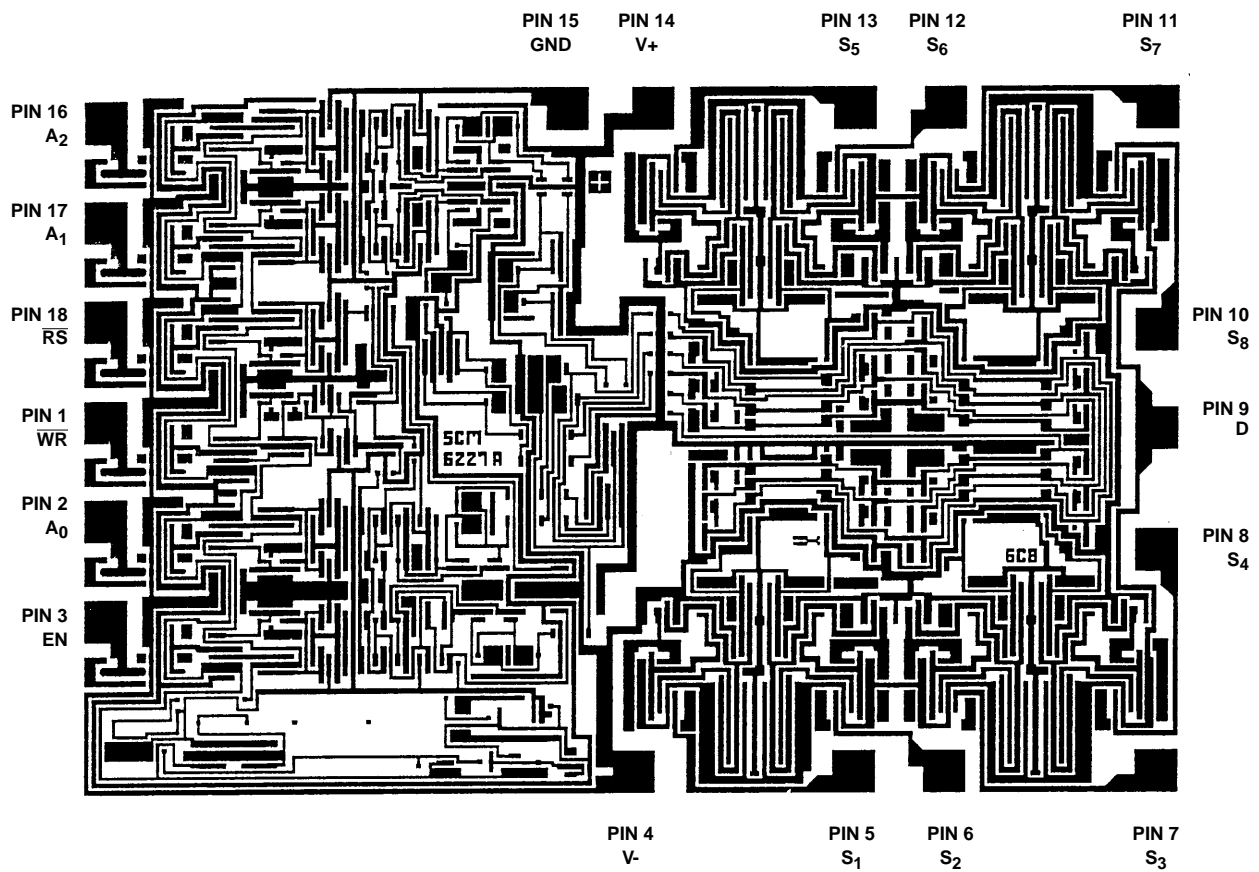
Nitride Thickness: 8k $\text{\AA}$   $\pm$  1.2k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

9.1 x 10<sup>4</sup> A/cm<sup>2</sup>

## Metallization Mask Layout

DG528



# DG526, DG527, DG528, DG529

## Die Characteristics

### DIE DIMENSIONS:

3100 $\mu$ m x 2083 $\mu$ m

### METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

### PASSIVATION:

Type: PSG Over Nitride

PSG Thickness: 7k $\text{\AA}$   $\pm$  1.4k $\text{\AA}$

Nitride Thickness: 8k $\text{\AA}$   $\pm$  1.2k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

9.1 x 10<sup>4</sup> A/cm<sup>2</sup>

## Metallization Mask Layout

DG529

