OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HFA1100, HFA1109

January 1999 File Number 3597.4

600MHz Current Feedback Amplifier with Compensation Pin

Description

The HFA1102 is a high speed wideband current feedback amplifier featuring a compensation pin for bandwidth limiting. Built with Harris' proprietary complementary bipolar UHF-1 process, it has excellent AC performance and low distortion.

Because the HFA1102 is already unity gain stable, the primary purpose for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. The bandwidth of the HFA1102 may be limited by connecting a capacitor and series damping resistor from pin 8 to ground. Typical bandwidths for various values of compensation capacitors are shown in the Electrical Specifications section of this datasheet.

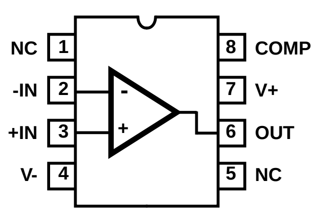
A variety of packages and temperature grades are available. See the ordering information below for details.

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1102IB (H1102I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Pinout

HFA1102
(SOIC)
TOP VIEW



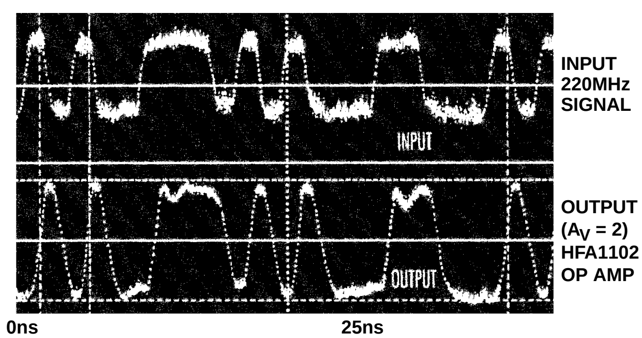
Features

- Compensation Pin for Bandwidth Limiting
- Low Distortion (HD2 at 30MHz) . . . . -56dBc
- -3dB Bandwidth 600MHz
- Very Fast Slew Rate 2000V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) . . . . ±0.05dB
  - (50MHz) . . . . ±0.02dB
  - (30MHz) . . . . ±0.01dB
- High Output Current 60mA
- Overdrive Recovery . . . . <10ns

Applications

- Low Noise Amplifiers
- Video Switching and Routing
- Pulse and Video Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

The Op Amps with Fastest Edges



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^oC/W)	θ_{JC} (^oC/W)
SOIC Package	170	N/A

Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, C_{COMP} = 0pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage		25	-	2	6	mV
		Full	-	-	10	mV
Input Offset Voltage Drift		Full	-	10	-	μV/^oC
V_{IO} CMRR	ΔV_{CM} = ±2V	25	40	46	-	dB
		Full	38	-	-	dB
V_{IO} PSRR	ΔV_S = ±1.25V	25	45	50	-	dB
		Full	42	-	-	dB
Non-Inv. Input Bias Current	+IN = 0V	25	-	25	40	μA
		Full	-	-	65	μA
$+I_{BIAS}$ Drift		Full	-	40	-	nA/^oC
$+I_{BIAS}$ CMS	ΔV_{CM} = ±2V	25	-	20	40	μA/V
		Full	-	-	50	μA/V
Inv. Input Bias Current	-IN = 0V	25	-	12	50	μA
		Full	-	-	60	μA
$-I_{BIAS}$ Drift		Full	-	40	-	nA/^oC
$-I_{BIAS}$ CMS	ΔV_{CM} = ±2V	25	-	1	7	μA/V
		Full	-	-	10	μA/V
$-I_{BIAS}$ PSS	ΔV_S = ±1.25V	25	-	6	15	μA/V
		Full	-	-	27	μA/V
Non-Inv. Input Resistance		25	25	50	-	kΩ
Inv. Input Resistance		25	-	16	30	Ω
Input Capacitance	Either Input	25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±3.0	-	V
Input Noise Voltage	100kHz	25	-	4	-	nV/√Hz
+Input Noise Current	100kHz	25	-	18	-	pA/√Hz
-Input Noise Current	100kHz	25	-	21	-	pA/√Hz
TRANSFER CHARACTERISTICS A_V = +1, R_F = 150Ω, R_{DAMP} = 120Ω, Unless Otherwise Specified						
Open Loop Transimpedance		25	-	500	-	kΩ

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, $C_{COMP} = 0pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Linear Phase Deviation	DC to 100MHz	25	-	0.6	-	Degrees
Differential Gain	NTSC, $R_L = 75\Omega$	25	-	0.03	-	%
Differential Phase	NTSC, $R_L = 75\Omega$	25	-	0.03	-	Degrees
Minimum Stable Gain		Full	1	-	-	V/V
Bandwidth Limiting Characteristics -3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, $A_V = +1$)	$C_{COMP} = 0pF$	25	-	600	-	MHz
	$C_{COMP} = 1pF$	25	-	350	-	MHz
	$C_{COMP} = 3pF$	25	-	190	-	MHz
	$C_{COMP} = 7pF$	25	-	55	-	MHz
Gain Flatness (To 30MHz)	$C_{COMP} = 0pF$	25	-	±0.01	-	dB
	$C_{COMP} = 1pF$	25	-	±0.05	-	dB
	$C_{COMP} = 3pF$	25	-	±0.10	-	dB
Gain Flatness	To 100MHz	25	-	±0.05	-	dB
Gain Flatness	To 50MHz	25	-	±0.02	-	dB
OUTPUT CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified						
Output Voltage	$A_V = -1$	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current	$R_L = 50\Omega$, $A_V = -1$	25	50	65	-	mA
		Full	40	60	-	mA
Closed Loop Output Impedance	DC	25	-	0.1	-	Ω
2nd Harmonic Distortion	30MHz, $V_{OUT} = 2V_{P-P}$	25	-	-56	-	dBc
3rd Harmonic Distortion	30MHz, $V_{OUT} = 2V_{P-P}$	25	-	-80	-	dBc
3rd Order Intercept	100MHz	25	-	30	-	dBm
1dB Compression	100MHz	25	-	20	-	dBm
TRANSIENT RESPONSE $A_V = +1$, $R_F = 150\Omega$, $R_{DAMP} = 120\Omega$, Unless Otherwise Specified						
Rise Time	$V_{OUT} = 2.0V$ Step	25	-	600	-	ps
Overshoot	$V_{OUT} = 2.0V$ Step	25	-	10	-	%
Slew Rate	$A_V = +1$, $V_{OUT} = 5V_{P-P}$	25	-	1200	-	V/µs
	$A_V = +2$, $V_{OUT} = 5V_{P-P}$	25	-	2000	-	V/µs
0.1% Settling Time	$V_{OUT} = 2V$ to 0V	25	-	11	-	ns
0.2% Settling Time	$V_{OUT} = 2V$ to 0V	25	-	7	-	ns
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current		25	-	21	26	mA
		Full	-	-	33	mA

Application Information

Optimum Feedback Resistor (R_F)

All current feedback amplifiers require a feedback resistor, even for unity gain applications. The R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1102 design is optimized for a 150Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, leading to excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

Bandwidth Limiting

The bandwidth of the HFA1102 may be limited by connecting a resistor (R_{DAMP}) and capacitor in series from pin 8 to GND. The series resister is required to damp the interaction between the package parasitics and C_{COMP}. Typical bandwidths for various values of compensation capacitor are shown in the specification tables. Because the HFA1102 is already unity gain stable, the main reason for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. Additionally, compensating the HFA1102 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} offsets the bandwidth increase from the lower R_F, keeping the amplifier stable. Reducing R_F provides the double benefits of reduced DC errors ($-I_B \times R_F$) and reduced total noise ($I_{NI} \times R_F$ and $4KTR_F$).

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown.

Evaluation Board

The HFA1102 may be evaluated using the HFA11XX Evaluation Board which is available from your local sales office (part number HFA11XXEVAL). R_{DAMP} and C_{COMP} should be connected in series from the socket pin to the GND plane. The trace from pin 8 to the V_H connector should be cut near the socket to remove this parallel capacitance.The layout and schematic of the board are shown below:

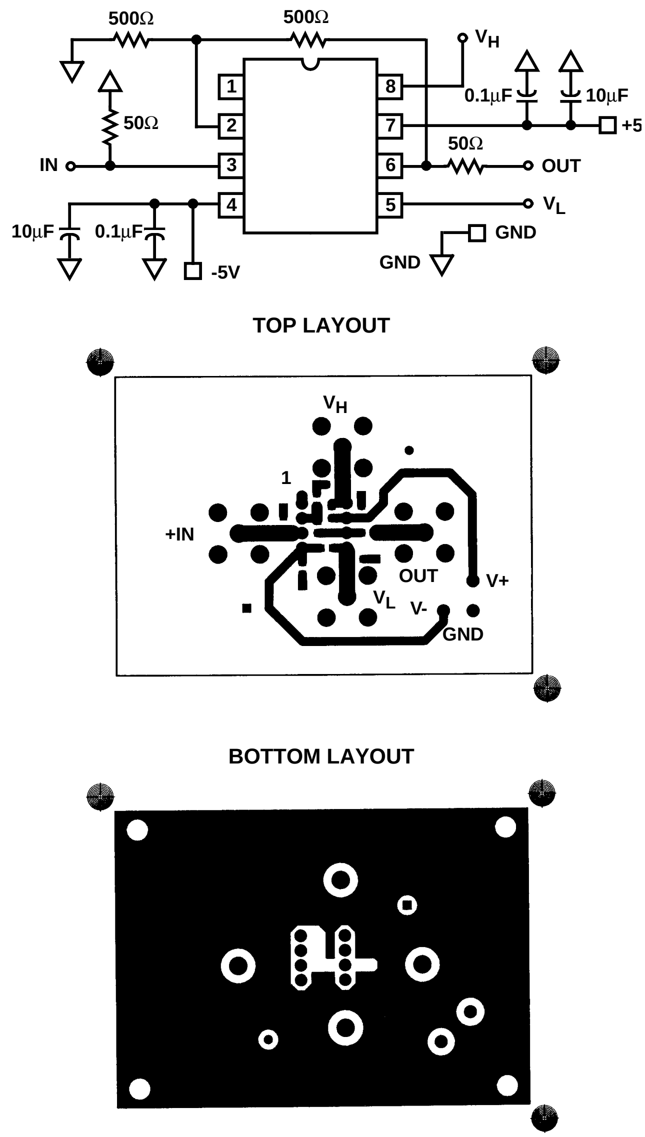

FIGURE 1. EVALUATION BOARD SCHEMATIC AND LAYOUT

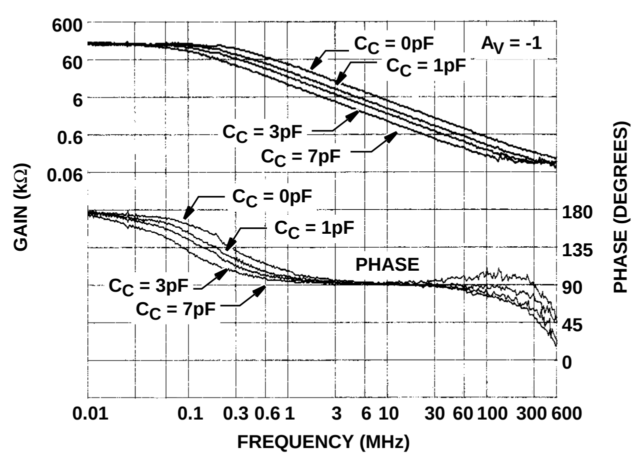

FIGURE 2. OPEN LOOP TRANSIMPEDANCE FOR VARIOUS COMPENSATION CAPACITORS