Data Sheet | November 1998 | File Number 4488.2

Direct Sequence Spread Spectrum Baseband

The Intersil HFA3860A Direct Sequence Spread Spectrum (DSSS) baseband processor is part of the PRISM™ 2.4GHz radio chipset, and contains all the functions necessary for a full or half duplex packet baseband transceiver.

The HFA3860A has on-board A/Ds for analog I and Q inputs, for which the HFA3724/6 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with M-Ary Bi-Orthogonal Keying to provide a variety of data rates. Built-in flexibility allows the HFA3860A to be configured through a general purpose control bus, for a range of applications. A Receive Signal Strength Indicator (RSSI) monitoring function with on-board 6-bit A/D provides Clear Channel Assessment (CCA) to avoid data collisions and optimize network throughput. The HFA3860A is housed in a thin plastic quad flat package (TQFP) suitable for PCMCIA board applications.

Ordering Information

PART NO.	TEMP. RANGE (^oC)	PKG. TYPE	PKG. NO.
HFA3860AIV	-40 to 85	48 Ld TQFP	Q48.7x7
HFA3860AIV96	-40 to 85	Tape and Reel	

Features

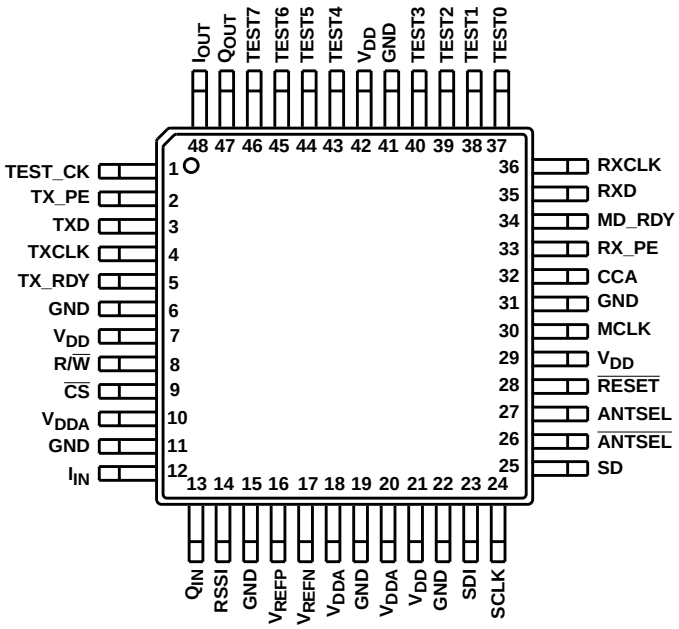
- Complete DSSS Baseband Processor
- Processing Gain . . . . . ≥10.4dB
- Programmable Data Rate . . . . . .1, 2, 5.5, and 11MBPS
- Ultra Small Package . . . . . 7 x 7 x 1mm
- Single Supply Operation (44MHz Max) . . . . . 2.7V to 3.6V
- Modulation Methods . . . . . .DBPSK, DQPSK, and MBOK
- Supports Full or Half Duplex Operations
- On-Chip A/D Converters for I/Q Data (3-Bit, 22MSPS) and RSSI (6-Bit)
- Backwards Compatible with HFA3860
- Supports Antenna Diversity

Applications

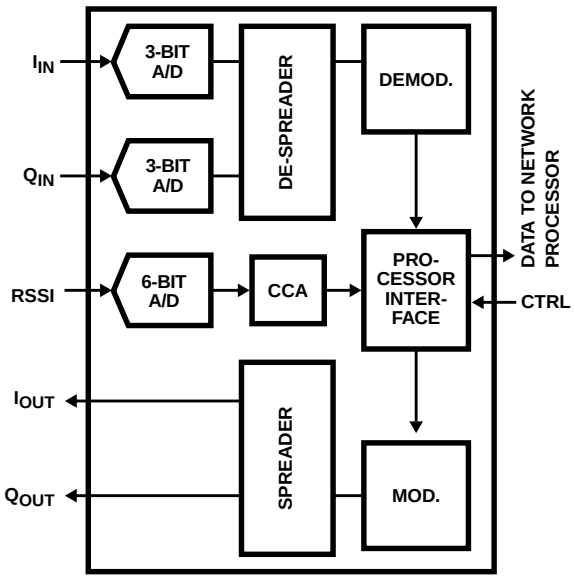
- Enterprise WLAN Systems
- Systems Targeting Ethernet Data Rates
- DSSS PCMCIA Wireless Transceiver
- Spread Spectrum WLAN RF Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable Bar Code Scanners/POS Terminal
- Portable PDA/Notebook Computer
- Wireless Digital Audio
- Wireless Digital Video
- PCN/Wireless PBX

Pinout

HFA3860A (TQFP)



SIMPLIFIED BLOCK DIAGRAM



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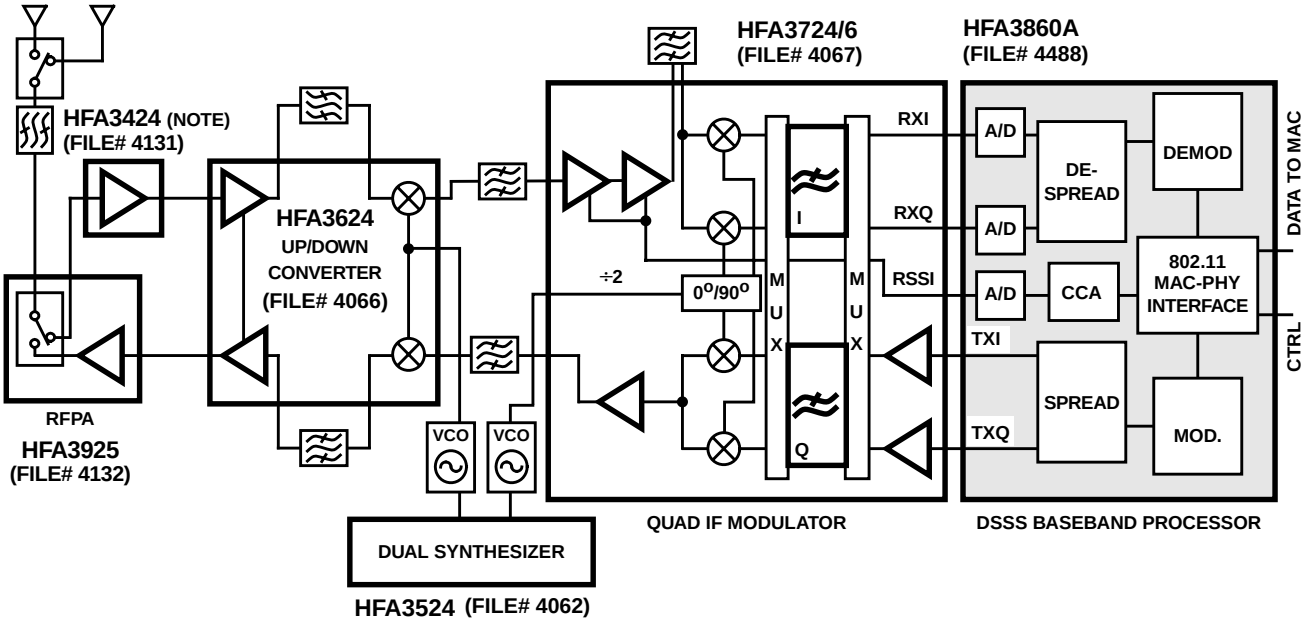
Typical Application Diagram



TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HFA3860A

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Intersil' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the data sheets you wish to receive.

The four-digit file numbers are shown in the Typical Application Diagram, and correspond to the appropriate circuit.

Pin Descriptions

NAME	PIN	TYPE I/O	DESCRIPTION
V_{DDA} (Analog)	10, 18, 20	Power	DC power supply 2.7V - 3.6V (Not Hardwired Together On Chip).
V_{DD} (Digital)	7, 21, 29, 42	Power	DC power supply 2.7 - 3.6V
GND (Analog)	11, 15, 19	Ground	DC power supply 2.7 - 3.6V, ground (Not Hardwired Together On Chip).
GND (Digital)	6, 22, 31, 41	Ground	DC power supply 2.7 - 3.6V, ground.
V_{REFN}	17	I	"Negative" voltage reference for A/D's (I and Q) [Relative to V_{REFP}]
V_{REFP}	16	I	"Positive" voltage reference for A/D's (I, Q and RSSI)
I_{IN}	12	I	Analog input to the internal 3-bit A/D of the In-phase received data.
Q_{IN}	13	I	Analog input to the internal 3-bit A/D of the Quadrature received data.
$\overline{\text{ANTSEL}}$	26	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL (pin 27) for differential drive of antenna switches.
ANTSEL	27	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for $\overline{\text{ANTSEL}}$ (pin 26) for differential drive of antenna switches.
RSSI	14	I	Receive Signal Strength Indicator Analog input.
TX_PE	2	I	When active, the transmitter is configured to be operational, otherwise the transmitter is in standby mode. TX_PE is an input from the external Media Access Controller (MAC) or network processor to the HFA3860A. The rising edge of TX_PE will start the internal transmit state machine and the falling edge will initiate shut down of the state machine. TX_PE envelopes the transmit data except for the last bit. The transmitter will continue to run for 3 symbols after TX_PE goes inactive to allow the PA to shut down gracefully.

Pin Descriptions (Continued)

NAME	PIN	TYPE I/O	DESCRIPTION
TXD	3	I	TXD is an input, used to transfer MAC Payload Data Unit (MPDU) data from the MAC or network processor to the HFA3860A. The data is received serially with the LSB first. The data is clocked in the HFA3860A at the rising edge of TXCLK.
TXCLK	4	O	TXCLK is a clock output used to receive the data on the TXD from the MAC or network processor to the HFA3860A, synchronously. Transmit data on the TXD bus is clocked into the HFA3860A on the rising edge. The clocking edge is also programmable to be on either phase of the clock. The rate of the clock will be dependent upon the data rate that is programmed in the signalling field of the header.
TX_RDY	5	O	TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HFA3860A is ready to receive the data packet from the network processor over the TXD serial bus. The TX_RDY returns to the inactive state when the last chip of the last symbol has been output.
CCA	32	O	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm makes its decision as a function of RSSI, Energy detect (ED), and Carrier Sense (CRS). The CCA algorithm and its features are described elsewhere in the data sheet. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). This polarity is programmable and can be inverted.
RXD	35	O	RXD is an output to the external network processor transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD_RDY.
RXCLK	36	O	RXCLK is the bit clock output. This clock is used to transfer Header information and payload data through the RXD serial bus to the network processor. This clock reflects the bit rate in use. RXCLK is held to a logic “0” state during the CRC16 reception. RXCLK becomes active after the SFD has been detected. Data should be sampled on the rising edge. This polarity is programmable and can be inverted.
MD_RDY	34	O	MD_RDY is an output signal to the network processor, indicating header data and a data packet are ready to be transferred to the processor. MD_RDY is an active high signal and it envelopes the data transfer over the RXD serial bus. MD_RDY goes active when the SFD is detected and returns to its inactive state when RX_PE goes inactive or an error is detected in the header.
RX_PE	33	I	When active, the receiver is configured to be operational, otherwise the receiver is in standby mode. This is an active high input signal. In standby, RX_PE inactive, all A/D converters are disabled.
SD	25	I/O	SD is a serial bidirectional data bus which is used to transfer address and data to/from the internal registers. The bit ordering of an 8-bit word is MSB first. The first 8 bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read at that register.
SCLK	24	I	SCLK is the clock for the SD serial bus. The data on SD is clocked at the rising edge. SCLK is an input clock and it is asynchronous to the internal master clock (MCLK). The maximum rate of this clock is 11MHz or one half the master clock frequency, whichever is lower.
SDI	23	I	Serial Data Input in 3 wire mode described in Tech Brief 362. This pin is not used in the 4 wire interface described in this data sheet. It should not be left floating.
R/$\overline{W}$	8	I	R/$\overline{W}$ is an input to the HFA3860A used to change the direction of the SD bus when reading or writing data on the SD bus. R/$\overline{W}$ also enables the serial shift register used in a read cycle. R/$\overline{W}$ must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
$\overline{CS}$	9	I	$\overline{CS}$ is a Chip Select for the device to activate the serial control port. The $\overline{CS}$ doesn’t impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, and R/$\overline{W}$ become “don’t care” signals.
TEST 7:0	37, 38, 39, 40, 43, 44, 45, 46	O	This is a data port that can be programmed to bring out internal signals or data for monitoring. These bits are primarily reserved by the manufacturer for testing. A further description of the test port is given at the appropriate section of this data sheet.
TEST_CK	1	O	This is the clock that is used in conjunction with the data that is being output from the test bus (TEST 0-7).
$\overline{RESET}$	28	I	Master reset for device. When active TX and RX functions are disabled. If $\overline{RESET}$ is kept low the HFA3860A goes into the power standby mode. $\overline{RESET}$ does not alter any of the configuration register values nor does it preset any of the registers into default values. Device requires programming upon power-up.
MCLK	30	I	Master Clock for device. The nominal frequency of this clock is 44MHz. This is used internally to generate all other internal necessary clocks and is divided by 2 or 4 for the transceiver clocks.
I_{OUT}	48	O	TX Spread baseband I digital output data. Data is output at the chip rate.
Q_{OUT}	47	O	TX Spread baseband Q digital output data. Data is output at the chip rate.

NOTE: Total of 48 pins; ALL pins are used.

External Interfaces

There are three primary digital interface ports for the HFA3860A that are used for configuration and during normal operation of the device as shown in Figure 1. These ports are:

- The **Control Port**, which is used to configure, write and/or read the status of the internal HFA3860A registers.
- The **TX Port**, which is used to accept the data that needs to be transmitted from the network processor.
- The **RX Port**, which is used to output the received demodulated data to the network processor.

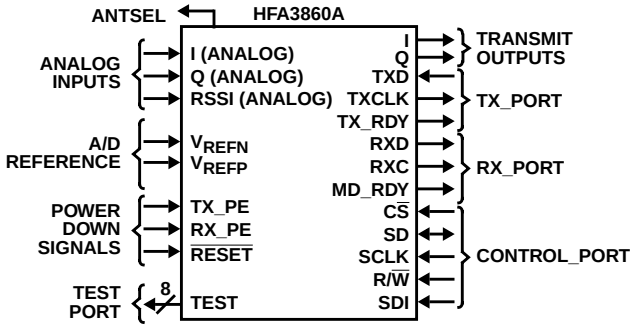


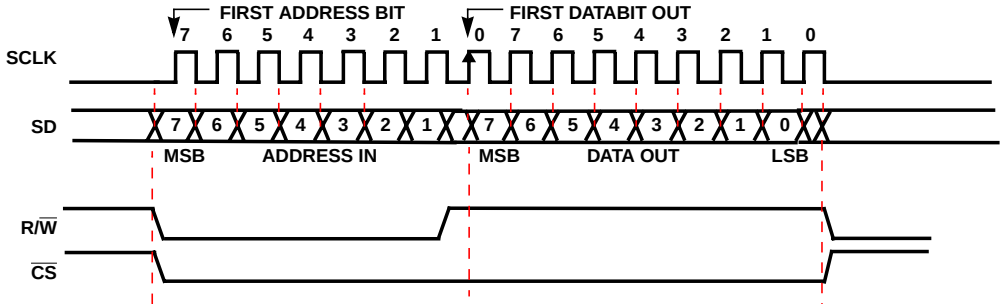
FIGURE 1. EXTERNAL INTERFACE

In addition to these primary digital interfaces the device includes a byte wide parallel **Test Port** which can be configured to output various internal signals and/or data. The device can also be set into various power consumption modes by external control. The HFA3860A contains three Analog to Digital (A/D) converters. The analog interfaces to the HFA3860A include the In phase (I) and quadrature (Q) data component inputs, and the RF signal strength indicator input. A reference voltage divider is also required external to the device.

Control Port (4 Wire)

The serial control port is used to serially write and read data to/from the device. This serial port can operate up to a 11MHz rate or 1/2 the maximum master clock rate of the device, MCLK (whichever is lower). MCLK must be running during programming. This port is used to program and to read all internal registers. The first 8 bits always represent the address followed immediately by the 8 data bits for that register. The two LSBs of address are don't care, but reserved for future expansion. The serial transfers are accomplished through the serial data pin (SD). SD is a bidirectional serial data bus. Chip Select ($\overline{CS}$), and Read/$\overline{Write}$ (R/$\overline{W}$) are also required as handshake signals for this port. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided by the external source and it is an input to the HFA3860A. The timing relationships of these signals are illustrated in Figures 2 and 3. R/$\overline{W}$ is high when data is to be read, and low when it is to be written. $\overline{CS}$ is an asynchronous reset to the state machine. $\overline{CS}$ must be active (low) during the entire data transfer cycle. $\overline{CS}$ selects the serial control port device only. The serial control port operates asynchronously from the TX and RX ports and it can accomplish data transfers independent of the activity at the other digital or analog ports.

The HFA3860A has 31 internal registers that can be configured through the control port. These registers are listed in the Configuration and Control Internal Register table. Table 1 lists the configuration register number, a brief name describing the register, and the HEX address to access each of the registers. The type indicates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high and low bytes).



NOTES:

1. The HFA3860A always uses the rising edge of SCLK. SD, R/W and CS hold times allow the controller to use either the rising or falling edge.
2. This port operates essentially the same as the HFA3824 with the exception that the AS signal of the 3824 is not required.

FIGURE 2. CONTROL PORT READ TIMING

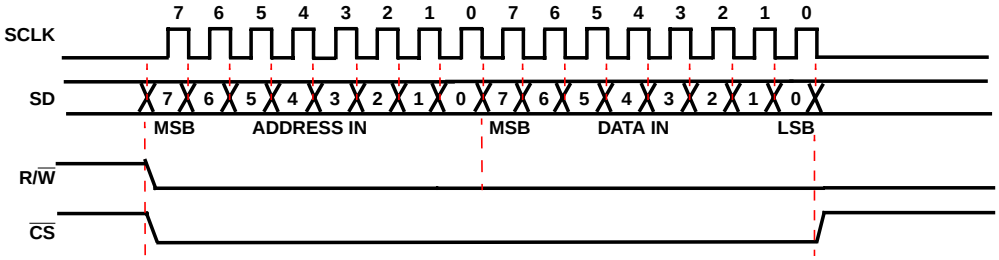


FIGURE 3. CONTROL PORT WRITE TIMING

TABLE 1. CONFIGURATION AND CONTROL INTERNAL REGISTER LIST

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX
CR0	Part/Version Code	R	00
CR1	I/O Polarity	R/W	04
CR2	TX and RX Control	R/W	08
CR3	A/D_CAL_POS Register	R/W	0C
CR4	A/D_CAL_NEG Register	R/W	10
CR5	CCA Antenna Control	R/W	14
CR6	Preamble Length	R/W	18
CR7	Scramble_Tap (RX and TX)	R/W	1C
CR8	RX_SQ1_ ACQ (High) Threshold	R/W	20
CR9	RX-SQ1_ ACQ (Low) Threshold	R/W	24
CR10	RX_SQ2_ ACQ (High) Threshold	R/W	28
CR11	RX-SQ2_ ACQ (Low) Threshold	R/W	2C
CR12	SQ1 CCA Thresh (High)	R/W	30
CR13	SQ1 CCA Thresh (Low)	R/W	34
CR14	ED or RSSI Thresh	R/W	38
CR15	SFD Timer	R/W	3C
CR16	Signal Field (BPSK - 11 Chip Sequence)	R/W	40
CR17	Signal Field (QPSK - 11 Chip Sequence)	R/W	44
CR18	Signal Field (BPSK - Mod. Walsh Sequence)	R/W	48
CR19	Signal Field (QPSK - Mod. Walsh Sequence)	R/W	4C
CR20	TX Signal Field	R/W	50
CR21	TX Service Field	R/W	54
CR22	TX Length Field (High)	R/W	58
CR23	TX Length Field (Low)	R/W	5C
CR24	RX Status	R	60
CR25	RX Service Field Status	R	64
CR26	RX Length Field Status (High)	R	68
CR27	RX Length Field Status (Low)	R	6C
CR28	Test Bus Address	R/W	70
CR29	Test Bus Monitor	R	74
CR30	Test Register 1, Must Load 00H	R/W	78
CR31	RX Control	R/W	7C

TX Port

The transmit data port accepts the data that needs to be transmitted serially from an external data source. The data is modulated and transmitted as soon as it is received from the external data source. The serial data is input to the HFA3860A through TXD using the next rising edge of TXCLK to clock it in the HFA3860A. TXCLK is an output from the HFA3860A. A timing scenario of the transmit signal handshakes and sequence is shown on timing diagram Figure 4.

The external processor initiates the transmit sequence by asserting TX_PE. TX_PE envelopes the transmit data packet on TXD. The HFA3860A responds by generating a Preamble and Header. Before the last bit of the Header is sent, the HFA3860A begins generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE goes back to its inactive state indicating the end of the data packet. The user needs to hold TX_PE high for as many clocks as there bits to transmit. For the higher data rates, this will be in multiples of the number of bits per symbol. The HFA3860A will continue to output modulated signal for 2µs after the last data bit is output, to supply bits to flush the modulation path. TX_PE must be held until the last data bit is output from the MAC/FIFO. The minimum TX_PE inactive pulse required to restart the preamble and header generation is 2.22µs and to reset the modulator is 4.22µs.

The HFA3860A internally generates the preamble and header information from information supplied via the control registers. The external source needs to provide only the data portion of the packet and set the control registers. The timing diagram of this process is illustrated on Figure 4. Assertion of TX_PE will initialize the generation of the preamble and header. TX_RDY, which is an output from the HFA3860A, is used to indicate to the external processor that the preamble has been generated and the device is ready to receive the data packet (MPDU) to be transmitted from the external processor. Signals TX_RDY, TX_PE and TXCLK can be set individually, by programming Configuration Register (CR) 1, as either active high or active low signals.

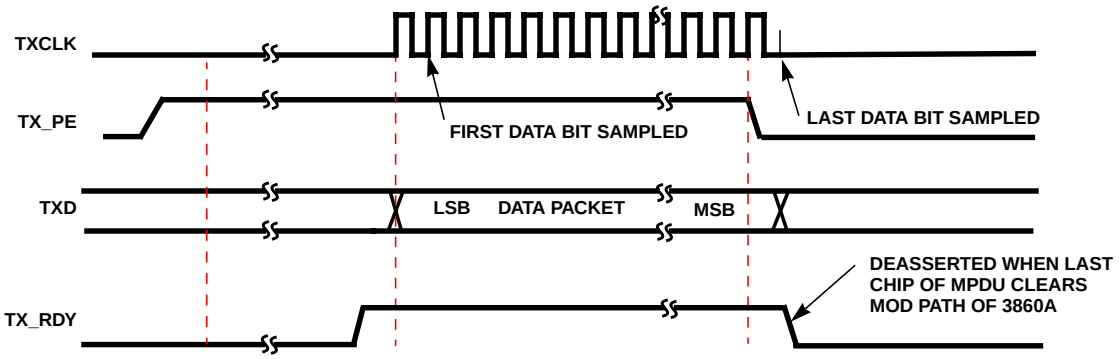
The transmit port is completely independent from the operation of the other interface ports including the RX port, therefore supporting a full duplex mode.

RX Port

The timing diagram Figure 5 illustrates the relationships between the various signals of the RX port. The receive data port serially outputs the demodulated data from RXD. The data is output as soon as it is demodulated by the HFA3860A. RX_PE must be at its active state throughout the receive operation. When RX_PE is inactive the device's receive functions, including acquisition, will be in a stand by mode.

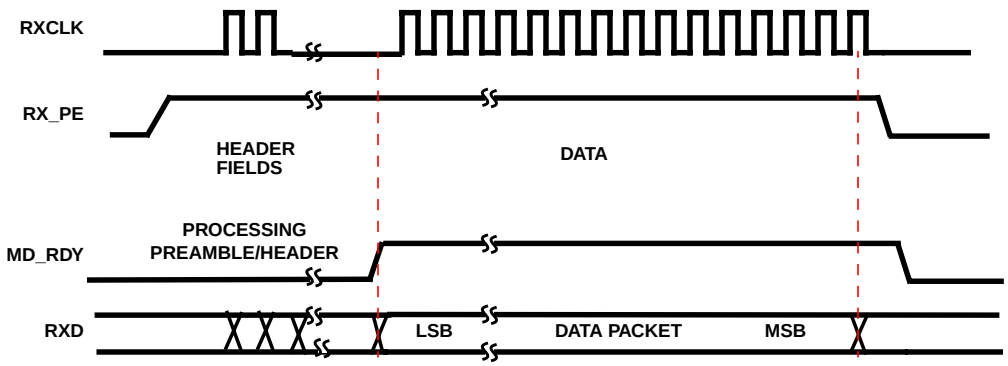
RXCLK is an output from the HFA3860A and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the HFA3860A and it may be set to go active after SFD or CRC fields. Note that RXCLK becomes active after the Start Frame Delimiter (SFD) to clock out the Signal, Service, and Length fields, then goes inactive during the header CRC field. RXCLK becomes active again for the data. MD_RDY returns to its inactive state after RX_PE is deactivated by the external controller, or if a header error is detected. A header error is either a failure of the CRC check, or the failure of the received signal field to match one of the 4 programmed signal fields. For either type of header error, the HFA3860A will reset itself after reception of the CRC field. If MD_RDY had been set to go active after CRC, it will remain low.

MD_RDY and RXCLK can be configured through CR 1, bit 6-7 to be active low, or active high. The receive port is completely independent from the operation of the other interface ports including the TX port, supporting therefore a full duplex mode.



NOTE: Preamble/Header and Data is transmitted LSB first. TXD shown generated from rising edge of TXCLK.

FIGURE 4. TX PORT TIMING



NOTE: MD_RDY active after CRC16. See detailed timing diagrams (see Figures 22, 23, 24).

FIGURE 5. RX PORT TIMING

I/Q A/D Interface

The PRISM baseband processor chip (HFA3860A) includes two 3-bit Analog to Digital converters (A/Ds) that sample the analog input from the IF down converter. The I/Q A/D clock, samples at twice the chip rate. The nominal sampling rate is 22MHz.

The interface specifications for the I and Q A/Ds are listed in Table 2.

TABLE 2. I, Q, A/D SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0
Input Bandwidth (-0.5dB)	-	20MHz	-
Input Capacitance (pF)	-	5	-
Input Impedance (DC)	5kΩ	-	-
FS (Sampling Frequency)	-	22MHz	-

The voltages applied to pin 16, V_{REFP} and pin 17, V_{REFN} set the references for the internal I and Q A/D converters. In addition, V_{REFP} is also used to set the RSSI A/D converter reference. For a nominal I/Q input of 500mV_{P-P}, the suggested V_{REFP} voltage is 1.75V, and the suggested V_{REFN} is 0.86V. V_{REFN} should never be less than 0.25V.

Figure 6 illustrates the suggested interface configuration for the A/Ds and the reference circuits.

Since these A/Ds are intended to sample AC voltages, their inputs are biased internally and they should be capacitively coupled. The HPF corner frequency in the baseband receive path should be less than 1kHz.

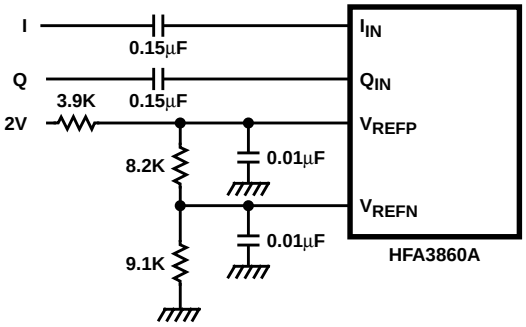


FIGURE 6. INTERFACES

The A/D section includes a compensation (calibration) circuit that automatically adjusts for temperature and component variations of the RF and IF strips. The variations in gain of limiters, AGC circuits, filters etc. can be compensated for up to ±4dB. Without the compensation circuit, the A/Ds could see a loss of up to 1.5 bits of the 3 bits of quantization. The A/D calibration circuit adjusts the A/D reference voltages to maintain optimum quantization of the IF input over this variation range. It works on the principle of setting the reference to insure that the signal is at full scale (saturation) a certain percentage of the time. Note that this is not an AGC and it will compensate only for slow variations in signal levels (several seconds).

The procedure for setting the A/D references to accommodate various input signal voltage levels is to set the reference voltages so that the A/D calibration circuit is operating at half scale with the nominal input. This leaves the maximum amount of adjustment room for circuit tolerances.

A/D Calibration Circuit and Registers

The A/D compensation or calibration circuit is designed to optimize A/D performance for the I and Q inputs by maintaining the full 3-bit resolution of the outputs. There are two registers (CR 3 AD_CAL_POS and CR 4 AD_CAL_NEG) that set the parameters for the internal I and Q A/D calibration circuit.

Both I and Q A/D outputs are monitored by the A/D calibration circuit as shown in Figure 7 and if either has a full scale value, a 24-bit accumulator is incremented as defined by parameter AD_CAL_POS. If neither has a full scale value, the accumulator is decremented as defined by parameter AD_CAL_NEG. The output of this accumulator is used to drive D/A converters that adjust the A/D's references. Loop gain reduction is accomplished by using only the 5 MSBs out of the 24 bits. The compensation adjustment is updated at a 1kHz rate. The A/D calibration circuit is only intended to remove slow component variations.

For best performance, the optimum probability that either the I or Q A/D converter is at the saturation level was determined to be 50%. The probability P is set by the formula:

P(AD_CAL_POS)+(1-P)(AD_CAL_NEG) = 0.

One solution to this formula for P = 1/2 is:

AD_CAL_POS = 1

AD_CAL_NEG = -1

This also sets the levels so that operation with either NOISE or SIGNAL is approximately the same. It is assumed that the RF and IF sections of the receiver have enough gain to cause limiting on thermal noise. This will keep the levels at the A/D approximately the same regardless of whether signal is present or not. The A/D calibration is normally set to work only while the receiver is tracking, but it can be set to operate all the time the receiver is on or it can be turned off and held at mid scale.

The A/D calibration circuit operation can be defined through CR 2, bits 3 and 4. Table 3 illustrates the possible configurations. The A/D Cal function should initially be programmed for mid scale operation to preset it, then programmed for either tracking mode. This initializes the part for most rapid settling on the appropriate values.

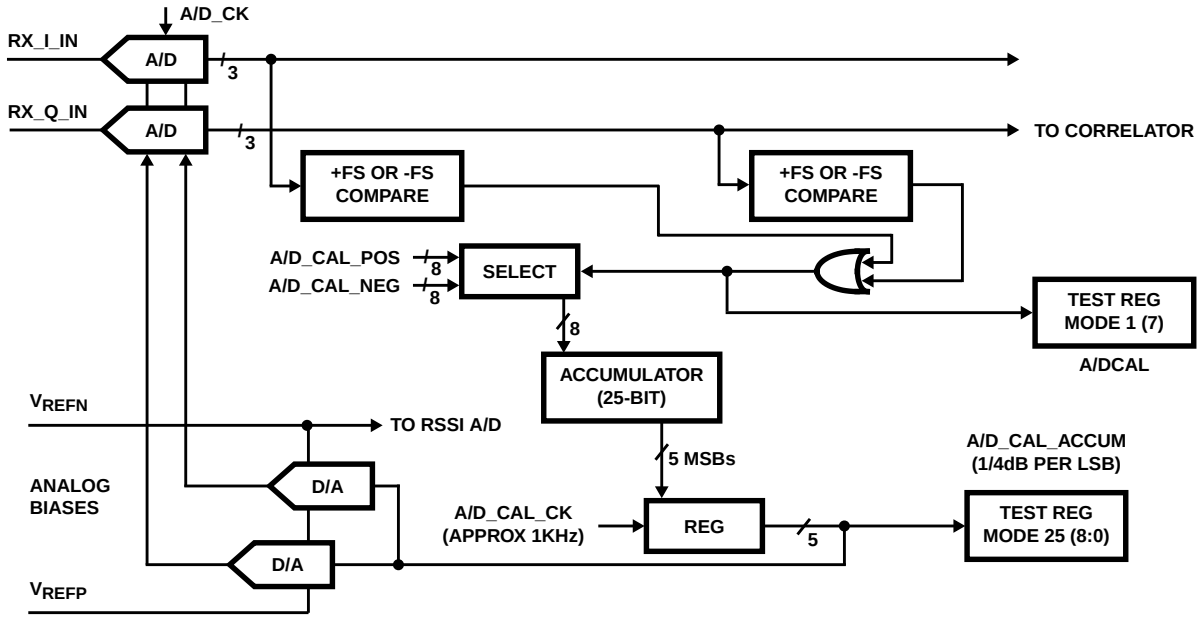


FIGURE 7. A/D CAL CIRCUIT

TABLE 3. A/D CALIBRATION

CR 2 BIT 4	CR 2 BIT 3	A/D CALIBRATION CIRCUIT CONFIGURATION
0	0	OFF, Reference set at mid scale.
0	1	OFF, Reference set at mid scale.
1	0	A/D_Cal while tracking only.
1	1	A/D_Cal while RX_PE active.

RSSI A/D Interface

The Receive Signal Strength Indication (RSSI) analog signal is input to a 6-bit A/D, indicating 64 discrete levels of received signal strength. This A/D measures a DC voltage, so its input must be DC coupled. Pin 16 (V_{REFP}) sets the reference for the RSSI A/D converter. V_{REFP} is common for the I and Q and RSSI A/Ds. The RSSI signal is used as an input to the Clear Channel Assessment (CCA) algorithm of the HFA3860A. The RSSI A/D output is stored in an 6-bit register available via the TEST Bus and the TEST Bus monitor register. CCA is further described on page 14.

The interface specifications for the RSSI A/D are listed in Table 4 below (V_{REFP} = 1.75V).

TABLE 4. RSSI A/D SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage	-	-	1.15
Input Bandwidth (0.5dB)	1MHz	-	-
Input Capacitance	-	7pF	-
Input Impedance (DC)	1M	-	-

Test Port

The HFA3860A provides the capability to access a number of internal signals and/or data through the Test port, pins TEST 7:0. In addition pin 1 (TEST_CK) is an output that can be used in conjunction with the data coming from the test port outputs. The test port is programmable through configuration register (CR28). Any signal on the test port can also be read from configuration register (CR29) via the serial control port.

There are 32 modes assigned to the PRISM test port. Some are only applicable to factory test.

TABLE 5. TEST MODES

MODE	DESCRIPTION	TEST_CLK	TEST (7:0)
0	Quiet Test Bus	0	00
1	RX Acquisition Monitor	Initial Detect	A/DCal, CRS, ED, Track, SFD Detect, Signal Field Ready, Length Field Ready, Header CRC Valid
2	TX Field Monitor	IQMARK	A/DCal, TXPE Internal, Preamble Start, SFD Start, Signal Field Start, Length Field Start, CRC Start, MPDU Start
3	RSSI Monitor	RSSI Pulse	CSE Latched, CSE, RSSI Out (5:0)
4	SQ1 Monitor	Pulse after SQ is valid	SQ1 (7:0)
5	SQ2 Monitor	Pulse after SQ is valid	SQ2 (7:0)
6	Correlator Lo Rate	Sample CLK	Correlator Magnitude (7:0)
7	Freq Test Lo Rate	Subsample CLK	Frequency Register (18:11)
8	Phase Test Lo Rate	Subsample CLK	Phase Register (7:3) Shift <2:0>
9	NCO Test Lo Rate	Subsample CLK	NCO Register (15:8)
10 (0Ah)	Bit Sync Accum Lo Rate	Enable	Bit Sync Accum (7:3) Shift (2:0)
11	Reserved	Reserved	Factory Test Only
12	A/D Cal Test Mode	A/D Cal CLK	A/DCal, ED, A/DCal Disable, ADCal (4:0)
13	Correlator I High Rate	Sample CLK	Correlator I (8:1)
14	Correlator Q High Rate	Sample CLK	Correlator Q (8:1)
15	Chip Error Accumulator	0	Chip Error Accum (14:7)
16	NCO Test Hi Rate	Sample CLK	NCO Accum (19:12)
17	Freq Test Hi Rate	Sample CLK	Lag Accum (18:11)
18	Carrier Phase Error Hi Rate	Sample CLK	Carrier Phase Error (6,6:0)
19	Reserved	Sample CLK	Factory Test Only
20	Reserved	Sample CLK	Factory Test Only
21	I_A/D, Q_A/D	Sample CLK	0,0,I_A/D (2:0),Q_A/D (2:0)
22	Reserved	Reserved	Factory Test Only
23	Reserved	Reserved	Factory Test Only
24	Reserved	Reserved	Factory Test Only
25	A/D Cal Accum Lo	A/D Cal Accum (8)	A/D Cal Accum (7:0)
26	A/D Cal Accum Hi	A/D Cal Accum (17)	A/D Cal Accum (16:9)
27	Freq Accum Lo	Freq Accum (15)	Freq Accum (14:7)
28	Reserved	Reserved	Factory Test Only
29	SQ2 Monitor Hi	Pulse After SQ Valid	SQ2 (15:8)
30-31	Reserved	Reserved	Factory Test Only

Definitions

ED. Energy Detect, indicates that the RSSI value exceeds its programmed threshold.

CRS. Carrier Sense, indicates that a signal has been acquired (PN acquisition).

TXCLK. Transmit clock.

Track. Indicates start of tracking and start of SFD time-out.

SFD Detect. Variable time after track starts.

Signal Field Ready. ~ 8µs after SFD detect.

Length Field Ready. ~ 32µs after SFD detect.

Header CRC Valid. ~ 48µs after SFD detect.

DCLK. Data bit clock.

FrqReg. Contents of the NCO frequency register.

PhaseReg. phase of signal after carrier loop correction.

NCO PhaseAccumReg. Contents of the NCO phase accumulation register.

SQ1. Signal Quality measure #1. Contents of the bit sync accumulator. Eight MSBs of most recent 16-bit stored value.

SQ2. Signal Quality measure #2. Signal phase variance after removal of data, Eight MSBs of most recent 16-bit stored value.

Sample CLK. Receive clock (RX sample clock). Nominally 22MHz.

Subsample CLK. LO rate symbol clock. Nominally 1MHz.

BitSyncAccum. Real time monitor of the bit synchronization accumulator contents, mantissa only.

A/D_Cal_ck. Clock for applying A/D calibration corrections.

A/DCal. 5-bit value that drives the D/A adjusting the A/D reference.

TABLE 6. POWER DOWN MODES

MODE	RX_PE	TX_PE	RESET	AT 44MHz	DEVICE STATE
SLEEP	Inactive	Inactive	Active	4mA	Both transmit and receive functions disabled. Device in sleep mode. Control Interface is still active. Register values are maintained. Device will return to its active state within 10µs plus settling time of AC coupling capacitors (about 5µs).
STANDBY	Inactive	Inactive	Inactive	11mA	Both transmit and receive operations disabled. Device will resume its operational state within 1µs of RX_PE or TX_PE going active.
TX	Inactive	Active	Inactive	15mA	Receiver operations disabled. Receiver will return in its operational state within 1µs of RX_PE going active.
RX	Active	Inactive	Inactive	24mA	Transmitter operations disabled. Transmitter will return to its operational state within 2 MCLKs of TX_PE going active.
NO CLOCK	I_{CC} Standby		Active	300µA	All inputs at V_{CC} or GND.

Power Down Modes

The power consumption modes of the HFA3860A are controlled by the following control signals.

Receiver Power Enable (RX_PE, pin 33), which disables the receiver when inactive.

Transmitter Power Enable (TX_PE, pin 2), which disables the transmitter when inactive.

Reset ($\overline{\text{RESET}}$, pin 28), which puts the receiver in a sleep mode. The power down mode where, both $\overline{\text{RESET}}$ and RX_PE are used is the lowest possible power consumption mode for the receiver. Exiting this mode requires a maximum of 10µs before the device is back at its operational mode for transmitters. Add 5µs more to be operational for receive mode. It also requires that RX_PE be activated briefly to clock in the change of state.

The contents of the Configuration Registers are not effected by any of the power down modes. The external processor does have access and can modify any of the CRs during the power down modes. No reconfiguration is required when returning to operational modes.

Table 6 describes the power down modes available for the HFA3860A (V_{CC} = 3.3V). The table values assume that all other inputs to the part (MCLK, SCLK, etc.) continue to run except as noted.

Transmitter Description

The HFA3860A transmitter is designed as a Direct Sequence Spread Spectrum Phase Shift Keying (DSSS PSK) modulator. It can handle data rates of up to 11MBPS (refer to AC and DC specifications). The various modes of the modulator are Differential Binary Phase Shift Keying (DBPSK), Differential Quaternary Phase Shift Keying (DQPSK), Binary M-ary Bi-Orthogonal Keying (BMBOK), and Quaternary M-ary Bi-Orthogonal Keying (QMBOK). These implement data rates of 1, 2, 5.5 and 11MBPS as shown in Table 7. The major functional blocks of the transmitter include a network processor interface, DPSK modulator, high rate modulator, a data scrambler and a spreader, as shown on Figure 8. A description of (M-ARY) Bi-Orthogonal Keying can be found in Chapter 5 of: “Telecommunications System Engineering”, by Lindsey and Simon, Prentis Hall publishing.

The preamble and header are always transmitted as DBPSK waveforms while the data packets can be configured to be either DBPSK, DQPSK, BMBOK, or QMBOK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and knows when to make the DBPSK to DQPSK or B/QMBOK switchover, as required.

For the PSK modes, the transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK, and mixes it with the BPSK PN spreading. The baseband digital signals are then output to the external IF modulator.

For the MBOK modes, the transmitter inputs the data and forms it into nibbles (4 bits). At 5.5MBPS, it selects one of 8 spread sequences from a table of sequences with 3 of those bits and then picks the true or inverted version of that sequence with the remaining bit. Thus, there are 16 possible spread sequences to send, but only one is sent. This sequence is then modulated on both the I and Q outputs. The phase of the last bit of the header is used as an

absolute phase reference for the data portion of the packet. At 11MBPS, two nibbles are used, and each one is used as above independently. One of the resulting sequences is modulated on the I Channel and the other on the Q Channel output. With 16 possible sequences on I and another 16 independently on Q, the total possible number of combinations is 256. Of these only one is sent.

The bit rate Table 7 shows examples of the bit rates and the symbol rates and Figure 8 shows the modulation schemes.

The modulator is completely independent from the demodulator, allowing the PRISM baseband processor to be used in full duplex operation.

TABLE 7. BIT RATE TABLE EXAMPLES FOR MCLK = 44MHz

DATA MODULATION	A/D SAMPLE CLOCK (MHZ)	TX SETUP CR 20 BITS 1, 0	RX STATUS CR 24 BITS 7, 6	DATA RATE (MBPS)	SYMBOL RATE (MSPS)
DBPSK	22	00	00	1	1
DQPSK	22	01	01	2	1
BMBOK	22	10	10	5.5	1.375
QMBOK	22	11	11	11	1.375

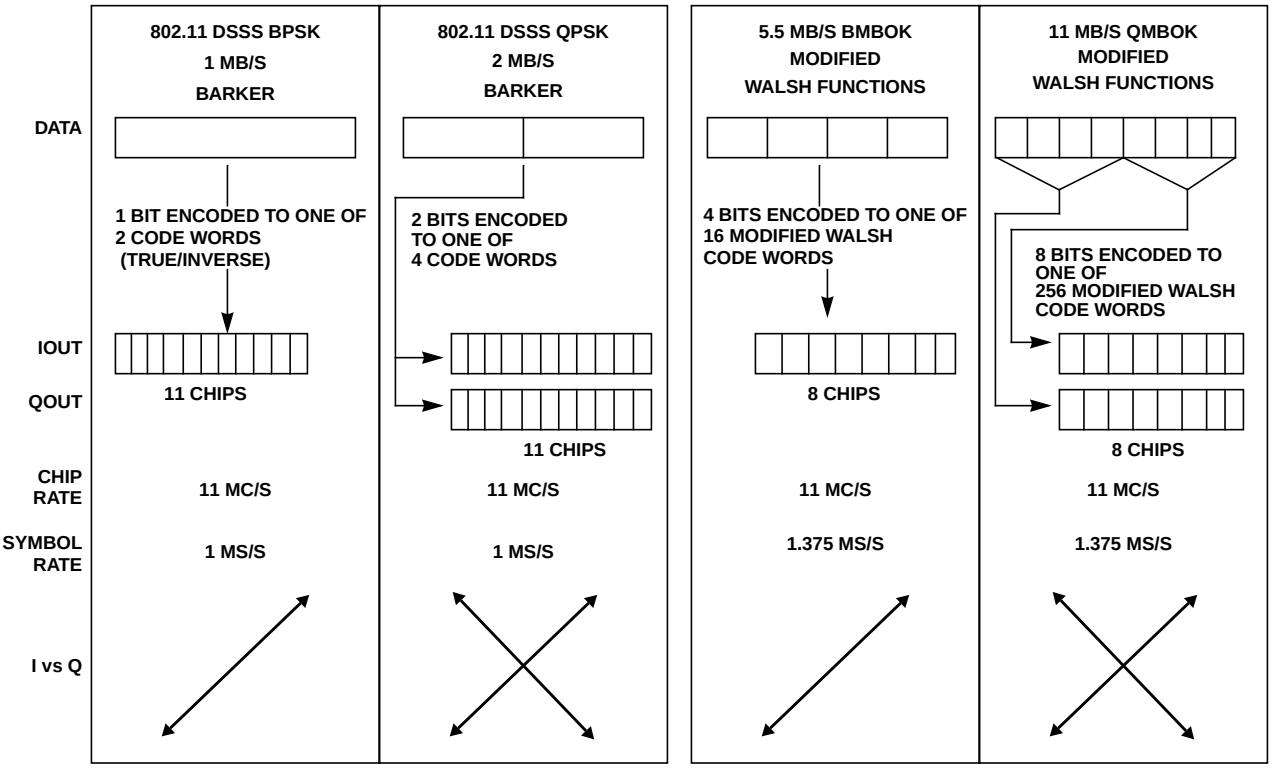


FIGURE 8. MODULATION MODES

Header/Packet Description

The HFA3860A is designed to handle continuous or packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HFA3860A generates its own preamble and header information.

The device uses a synchronization preamble of up to 256 symbols, and a header that includes four fields. The preamble is all 1's plus a start frame delimiter (before entering the scrambler). The actual transmitted pattern of the preamble will be randomized by the scrambler. The preamble is always transmitted as a DBPSK waveform.

Start Frame Delimiter (SFD) Field (16 Bits)

This carries the synchronization to establish the link frame timing. The HFA3860A will not declare a valid data packet, even if it PN acquires, unless it detects the SFD. The HFA3860A receiver is programmed to time out searching for the SFD via CR15. The timer starts counting the moment that initial PN synchronization has been established from the preamble.

The four fields for the header shown in Figure 9 are:

Signal Field (8 Bits). This field indicates what data rate the data packet that follows the header will be. The HFA3860A receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK or B/QMBOK demodulation at the end of the always DBPSK preamble and header fields.

Service Field (8 Bits) - This field is currently unassigned and can be utilized as required by the user. Set to 00h for compliance with IEEE 802.11.

Length Field (16 Bits). This field indicates the number of microseconds it will take to transmit the payload data (MPDU). The external controller will check the length field in determining when it needs to de-assert the RX_PE.

CCITT - CRC 16 Field (16 Bits) - This field includes the 16-bit CCITT - CRC 16 calculation of the three header fields. This value is compared with the CCITT - CRC 16 code calculated at the receiver. The HFA3860A receiver will indicate a CCITT - CRC 16 error via CR24 bit 2 and will lower MD_RDY if there is an error.

FIGURE 9. 802.11 PREAMBLE/HEADER

The CRC or cyclic Redundancy Check is a CCITT CRC-16 FCS (frame check sequence). It is the ones compliment of the remainder generated by the modulo 2 division of the protected bits by the polynomial:

$x^{16} + x^{12} + x^5 + 1$

The protected bits are processed in transmit order. All CRC calculations are made prior to data scrambling. A shift register with two taps is used for the calculation. It is preset to all ones and then the protected fields are shifted through the register. The output is then complemented and the residual shifted out MSB first.

The following Configuration Registers (CR) are used to program the preamble/header functions, more programming details about these registers can be found in the Control Registers section of this document:

CR 6 . Defines the preamble length minus the SFD in symbols. The 802.11 protocol requires a setting of 128d = 80h.

CR 15. Defines the length of time that the demodulator searches for the SFD before returning to acquisition.

CR 16. The contents of this register define DBPSK modulation. If CR 20 bits 1 and 0 are set to indicate DBPSK modulation then the contents of this register are transmitted in the signal field of the header.

CR 17. The contents of this register define DQPSK modulation. If CR 20 bits 1 and 0 are set to indicate DQPSK modulation then the contents of this register are transmitted in the signal field of the header.

CR 18. The contents of this register define BMBOK modulation. If CR 20 bits 1 and 0 are set to indicate BMBOK modulation then the contents of this register are transmitted in the signal field of the header.

CR 19. The contents of this register define QMBOK modulation. If CR 20 bits 1 and 0 are set to indicate QMBOK modulation then the contents of this register are transmitted in the signal field of the header.

CR 20. The last two bits of the register indicate what modulation is to be used for the data portion of the packet.

CR 21. The value to be used in the Service field.

CR 22, 23. Defines the value of the transmit data length field. This value includes all symbols following the last header field symbol and is in microseconds required to transmit the data at the chosen data rate.

The packet consists of the preamble, header and MAC protocol data unit (MPDU). The data is transmitted exactly as received from the control processor. Some dummy bits will be appended to the end of the packet to insure an orderly shutdown of the transmitter. This prevents spectrum splatter. At the end of a packet, the external controller is expected to de-assert the TX_PE line to shut the transmitter down.

Scrambler and Data Encoder Description

The modulator has a data scrambler that implements the scrambling algorithm specified in the IEEE 802.11 standard. This scrambler is used for the preamble, header, and data in all modes. The data scrambler is a self synchronizing circuit. It consist of a 7-bit shift register with feedback from specified taps of the register, as programmed through configuration register CR 7. Both transmitter and receiver use the same scrambling algorithm. The scrambler can be disabled by setting the taps to 0.

NOTE: The IEEE 802.11 compliant scrambler in the HFA3860A has the property that it can lock up (stop scrambling) on random data followed by repetitive bit patterns. The probability of this happening is 1/128. The patterns that have been identified are all zeros, all ones, repeated 10s, repeated 1100s, and repeated 111000s. Any break in the repetitive pattern will restart the scrambler. If an all zeros pattern following random data causes the scrambler to lock up and this state lasts for more than 200 microseconds in the 5.5 and 11MBps data modes, the demodulator may lose carrier tracking and corrupt the packet. This is caused by a buildup of a DC bias in the AC coupling between the HFA3724 and the HFA3860A.

Scrambling is done by a polynomial division using a prescribed polynomial as shown in Figure 10. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The taps are programmable. The transmit scrambler seed is Hex 6C and the taps are set with CR 7.

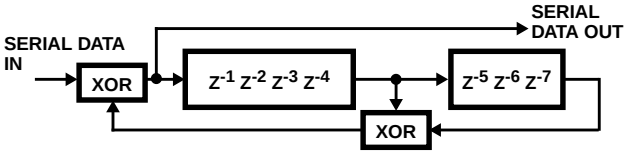


FIGURE 10. SCRAMBLING PROCESS

For the 1MBPS DBPSK data rates and for the header in all rates, the data coder implements the desired DBPSK coding by differential encoding the serial data from the scrambler and driving both the I and Q output channels together. For the 2MBPS DQPSK data rate, the data coder implements the desired coding as shown in the DQPSK Data Encoder table. This coding scheme results from differential coding of dibits (2 bits). Vector rotation is counterclockwise although bits 5 and 6 of configuration register CR2 can be used to reverse the rotation sense of the TX or RX signal if needed.

TABLE 8. DQPSK DATA ENCODER

PHASE SHIFT	DIBIT PATTERN (D0, D1) D0 IS FIRST IN TIME
0	00
+90	01
+180	11
-90	10

For data modulation in the MBOK modes, the data is formed into nibbles (4 bits). For Binary MBOK modulation (5.5MBPS) one nibble is used per symbol and for Quaternary MBOK (11MBPS), two are used. The data is not differentially encoded, just scrambled, in these modes.

Spread Spectrum Modulator Description

The modulator is designed to generate DBPSK, DQPSK, BMBOK, and QMBOK spread spectrum signals. The modulator is capable of automatically switching its rate where the preamble and header are DBPSK modulated, and the data is differently modulated. The modulator can support date rates of 1, 2, 5.5 and 11MBPS. The programming details to set up the modulator are given at the introductory paragraph of this section. The HFA3860A utilizes Quadraphase (I/Q) modulation at baseband for all modulation modes.

In the 1MBPS DBPSK mode, the I and Q Channels are connected together and driven with the output of the scrambler and differential encoder. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. The I and Q signals go to the Quadrature upconverter (HFA3724) to be modulated onto a carrier. Thus, the spreading and data modulation are BPSK modulated onto the carrier.

For the 2MBPS DQPSK mode, the serial data is formed into dibits or bit pairs in the differential encoder as detailed above. One of the bits in a dibit goes to the I Channel and the other to the Q Channel. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. This forms QPSK modulation at the symbol rate with BPSK modulation at the spread rate.

For the 5.5MBPS Binary M-Ary Bi-Orthogonal Keying (BMBOK) mode, the output of the scrambler is partitioned into nibbles of sign-magnitude (4 bits LSB first). The magnitude bits are used to select 1 of 8 eight bit modified Walsh functions. The Walsh functions are modified by adding hex 03 to all members of a Walsh function set to insure that there is no all 0 member as shown in table WAL. The selected function is then XOR'ed with the sign bit and connected to both I and Q outputs. The modified Walsh functions are clocked out at the spread rate (nominally 11MCPS). The symbol rate is 1/8th of this rate. The Differential Encoder output of the last bit of the header CRC is the phase reference for the high rate data. This reference is XOR'ed with the I and Q data before the output. This allows the demodulator to compensate for phase ambiguity without differential encoding the high rate data.

TABLE 9. MODIFIED WALSH FUNCTIONS

MAG	mWAL	DATA PATTERN LSB.....MSB
0	03	11000000
1	0C	00110000
2	30	00001100
3	3F	11111100
4	56	01101010
5	59	10011010
6	65	10100110
7	6A	01010110

For the 11MBPS QMBOK mode, the output of the scrambler is partitioned into two nibbles. Each nibble is used as above to select a modified Walsh function and set its sign. The first of these modified Walsh spreading functions goes to the Q Channel and the second to the I Channel. They are then both XOR'ed with the phase reference developed from the last bit of the header CRC from the differential encoder.

Clear Channel Assessment (CCA) and Energy Detect (ED) Description

The clear channel assessment (CCA) circuit implements the carrier sense portion of a carrier sense multiple access (CSMA) networking scheme. The Clear Channel Assessment (CCA) monitors the environment to determine when it is feasible to transmit. The result of the CCA algorithm is available 16µs after RX_PE goes high through output pin 32 of the device. The CCA circuit in the HFA3860A can be programmed to be a function of RSSI (energy detected on the channel), carrier detection, or both. The CCA output can be ignored, allowing transmissions independent of any channel

conditions. The CCA in combination with the visibility of the various internal parameters (i.e., Energy Detection measurement results), can assist an external processor in executing algorithms that can adapt to the environment. These algorithms can increase network throughput by minimizing collisions and reducing transmissions liable to errors.

There are two measures that are used in the CCA assessment. The receive signal strength (RSSI) which measures the energy at the antenna and carrier sense early (CSE). Both indicators are normally used since interference can trigger the signal strength indication, but it might not trigger the carrier sense. The carrier sense, however, becomes active only when a spread signal with the proper PN code has been detected, so it may not be adequate in itself. The CCA compares these measures to thresholds at the end of the first antenna dwell following RX_PE going active. “The state of CCA is not guaranteed from the time RX_PE goes high until the CCA assessment is made. At the end of a packet, after RX_PE has been deasserted, the state of CCA is also not guaranteed.” CCA should be sampled 16µs after raising RX_PE.

The receive signal strength indication (RSSI) measurement is an analog input to the HFA3860A from the successive IF stage of the radio. The RSSI A/D converts it within the baseband processor and it compares it to a programmable threshold. This threshold is normally set to between -70 and -80dBm. A MAC controlled calibration procedure can be used to optimize this threshold.

The CSE (Carrier Sense Early) is a signal that goes active when SQ1 (after an antenna dwell) has been satisfied. It is called early, since it is indicated before the carrier sense used for acquisition. It is calculated on the basis of the integrated energy in the correlator output over a block of 15 symbols. Thus, the CCA is valid after 16µs has transpired from the time RX_PE was raised.

The Configuration registers effecting the CCA algorithm operation are summarized below (more programming details on these registers can be found under the Control Registers section of this document).

The CCA output from pin 32 of the device can be defined as active high or active low through CR 1 (bit 5). The RSSI threshold is set through CR14. If the actual RSSI value from the A/D exceeds this threshold then ED becomes active.

The instantaneous RSSI value can be monitored by the external network processor by reading the test bus in mode 3. It measures the signal 16µs after the start of each antenna or data dwell. RSSI value is invalid after MD_RDY goes active if CR31 bit 1 is set to a “1”. Value is valid until MD_RDY drops if bit is set to a “0”. The programmable threshold on the CSE measurement is set through CR12 and CR13. More details on SQ1 are included in the receiver section of this document.

In a typical single antenna system CCA will be monitored to determine when the channel is clear. Once the channel is detected busy, CCA should be checked periodically to determine if the channel becomes clear. CCA is stable to allow asynchronous sampling or even falling edge detection of CCA. Once MD_RDY goes active, CCA is then ignored for the remainder of the message. Failure to monitor CCA until MD_RDY goes active (or use of a time-out circuit) could result in a stalled system as it is possible for the channel to be busy and then become clear without an MD_RDY occurring.

A Dual antenna system has the added complexity that CCA will potentially toggle between active and inactive as each antenna is checked. The user must avoid mistaking the inactive CCA signal as an indication the channel is clear. A time-out circuit that begins with the first busy channel indication could be used. Alternatively CCA could be monitored, a clear channel indication for 2 successive antenna dwells would show the channel clear on both antennas. Time alignment of CCA monitoring with the receivers 16µs antenna dwells would be required. Once the receiver has acquired, CCA should be monitored for loss of signal until MD_RDY goes active.

An optional CCA mode is set by CR31 bit 0. When set to a zero, the HFA3860A will perform the CCA monitoring for successive antenna dwells when dual antenna mode is selected. The external CCA signal will go active when a busy channel is detected, CCA will stay active until the channel shows clear for two successive antenna dwells. This allows the same simple algorithm to be used in both signal and dual antenna, namely, continuous monitoring of CCA for a clear channel until MD_RDY goes active.

CR5 selects the starting antenna used when RXPE is brought active.

CSE is updated at the end of each antenna dwell. After acquisition, CSE is updated every 64 symbols. In the event of signal loss after acquisition, CSE may go inactive. But because the accumulation is over 63 symbols instead of 15, it is more likely the SQ1 value will exceed the CSE threshold and CSE will remain active.

Demodulator Description

The receiver portion of the baseband processor, performs A/D conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DBPSK, DQPSK, BMBOK, or QMBOK symbols. The demodulator includes a frequency tracking loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes (where appropriate) and descrambles the data. The data is output through the RX Port to the external processor.

The PRISM baseband processor, HFA3860A uses differential demodulation for the initial acquisition portion of the message processing and then switches to coherent demodulation for the rest of the acquisition and data demodulation. The HFA3860A is designed to achieve rapid settling of the carrier tracking loop during acquisition. Rapid phase fluctuations are

handled with a relatively wide loop bandwidth. Coherent processing improves the BER performance margin as opposed to differentially coherent processing and is necessary for processing the two higher data rates.

The baseband processor uses time invariant correlation to strip the PN spreading and phase processing to demodulate the resulting signals in the header and DBPSK/DQPSK demodulation modes. These operations are illustrated in Figure 15 which is an overall block diagram of the receiver processor.

In processing the DBPSK header, input samples from the I and Q A/D converters are correlated to remove the spreading sequence. The peak position of the correlation pulse is used to determine the symbol timing. The sample stream is decimated to the symbol rate and the phase is corrected for frequency offset prior to PSK demodulation. Phase errors from the demodulator are fed to the NCO through a lead/lag filter to maintain phase lock. The variance of the phase error is used to determine signal quality for acquisition and lock detection. The demodulated data is differentially decoded and descrambled before being sent to the header detection section.

In the 1MBPS DBPSK mode, data demodulation is performed the same as in header processing. In the 2MBPS DQPSK mode, the demodulator demodulates two bits per symbol and differentially decodes these bit pairs. The bits are then serialized and descrambled prior to being sent to the output.

In the MBOK modes, the receiver uses a complex multiplier to remove carrier frequency offsets and a bank of serial correlators to detect the modulation. A biggest picker finds the largest correlation in the I and Q Channels and determines the sign of those correlations. For this to happen, the demodulator must know absolute phase which is determined by referencing the data to the last bit of the header. Each symbol demodulated determines 1 or 2 nibbles of data. This is then serialized and descrambled before passing on to the output.

Chip tracking in the MBOK modes is chip decision directed. Carrier tracking is via a lead/lag filter using a digital Costas phase detector.

Acquisition Description

The PRISM baseband processor uses either a dual antenna mode of operation for compensation against multipath interference losses or a single antenna mode of operation with faster acquisition times.

Two Antenna Acquisition (Recommended for Indoor Use)

During the 2 antenna (diversity) mode the two antennas are scanned in order to find the one with the best representation of the signal. This scanning is stopped once a suitable signal is found and the best antenna is selected.

A projected worst case time line for the acquisition of a signal in the two antenna case is shown in Figure 12. The synchronization part of the preamble is 128 symbols long followed by a 16-bit SFD. The receiver must scan the two antennas to determine if a signal is present on either one and, if so, which has the better signal. The timeline is broken into 16 symbol blocks (dwells) for the scanning process. This length of time is necessary to allow enough integration of the signal to make a good acquisition decision. This worst case time line example assumes that the signal is present on antenna A1 only (A2 is blocked). It further assumes that the signal arrives part way into the first A1 dwell such as to just barely miss detection. The signal and the scanning process are asynchronous and the signal could start anywhere. In this timeline, it is assumed that all 16 symbols are present, but they were missed due to power amplifier ramp up. Since A2 has insufficient signal, the first A2 dwell after the start of the preamble also fails detection. The second A1 dwell after signal start is successful and a symbol timing measurement is achieved.

Meanwhile signal quality and signal frequency measurements are made simultaneous with symbol timing measurements. When the bit sync level, SQ1, and Phase variance SQ2 are above their user programmable thresholds, the signal is declared present for that antenna. More details on the Signal Quality estimates and their programmability are given in the Acquisition Signal Quality Parameters section of this document.

At the end of each dwell, a decision is made based on the relative values of the signal qualities of the signals on the two antennas. In the example, antenna A1 is the one selected, so the recorded symbol timing and carrier frequency for A1 are used thereafter for the symbol timing and the PLL of the NCO to begin carrier de-rotation and demodulation.

Prior to initial acquisition the NCO was inactive and DPSK demodulation processing was used. Carrier phase measurement are done on a symbol by symbol basis afterward and coherent DPSK demodulation is in effect. After a brief setup time as illustrated on the timeline of Figure 12, the signal begins to emerge from the demodulator.

It takes 7 more symbols to seed the descrambler before valid data is available. This occurs in time for the SFD to be received. At this time the demodulator is tracking and in the coherent PSK demodulation mode it will no longer scan antennas.

One Antenna Acquisition (Only Recommended if Multi-path is Not Significant)

When only one antenna is being used, the user can delete the antenna switch and shorten the acquisition sequence. Figure 13 shows the single antenna acquisition timeline with an 80 symbol preamble. This scheme deletes the second antenna dwells but performs the same otherwise. It verifies the signal after initial detection for lower false alarm probability.

Acquisition Signal Quality Parameters

Two measures of signal quality are used to determine acquisition. The first method of determining signal presence is to measure the correlator output (or bit sync) amplitude. This measure, however, flattens out in the range of high BER and is sensitive to signal amplitude. The second measure is phase noise and in most BER scenarios it is a better indication of good signals plus it is insensitive to signal amplitude.

The metric for choosing the best antenna is determined by CR5 bit 3. When set to a zero the antenna with the smallest phase variance (SQ2) is chosen. This metric has shown to have a poor measure of multipath effects and is best suited for 1MBPS and 2MBPS operations. When set to a one, the six sidelobes (3 on either side of the 3 centered on the bit sync peak) are summed and compared. The antenna with the smallest sum (SQ3) is selected. This metric is optimal for improving 5.5 and 11MBPS operation in the presence of multipath.

CR5 bit 4 is to select the bit sync accumulation duration used during antenna dwells. When set to a zero the accumulation is over 15 symbols (consistent with HSP3824, HFA3824A, HFA3860). This setting allows the user to set the CSE and SQ1 thresholds as before and retain consistent CSE and acquisition performance. When set to a one, the bit sync accumulates on the last 13 symbols instead of the last 15. The SQ1 value will be numerically smaller, so CSE and SQ1 acquisition thresholds may need adjustment. The benefit of setting this bit is the elimination of transients (due to antenna switching and A/D timing adjustments) in the bit sync accumulation. This provides the best possible data for SQ3 based antenna diversity.

The bit sync amplitude and phase noise are integrated over each block of 16 symbols used in acquisition or over blocks of 64 symbols in the data demodulation mode. The bit sync amplitude measurement represents the peak of the correlation out of the PN correlator. Figure 14 shows the correlation process. The signal is sampled at twice the chip rate (i.e., 22MSPS). The one sample that falls closest to the peak is used for a bit sync amplitude sample for each symbol. This sample is called the on-time sample. High bit sync amplitude means a good signal. The early and late samples are the two adjacent samples and are used for tracking.

The other signal quality measurement is based on phase noise and that is taken by sampling the correlator output at the correlator peaks. The phase changes due to scrambling are removed by differential demodulation during initial acquisition. Then the phase, the phase rate and the phase variance are measured and integrated for 16 symbols. The phase variance is used for the phase noise signal quality measure (SQ2). Low phase noise means a stronger received signal.

Procedure to Set Acq. Signal Quality Parameters

Example: There are four registers that set the acquisition signal quality thresholds, they are: CR 8, 9, 10, and 11 (RX_SQX_IN_ACQ). Each threshold consists of two bytes, high and low that hold a 16-bit number.

These two thresholds, bit sync amplitude CR (8 and 9) and phase error CR (10 and 11) are used to determine if the desired signal is present. If the thresholds are set too “low”, that increases the probability of missing a high signal to noise detection due to being busy processing a false alarm. If they are set too “high”, that increases the probability of missing a low signal to noise detection. For the bit sync amplitude, “high” actually means high amplitude while for phase noise “high” means low noise or high SNR.

A recommended procedure is to set these thresholds individually optimizing each one of them to the same false alarm rate with no desired signal present. Only the background environment should be present, usually additive gaussian white noise (AGWN). When programming each threshold, the other threshold is set so that it always indicates that the signal is present. Set register CR8 to 00h while trying to determine the value of the phase error signal quality threshold for registers CR 10 and 11. Set register CR10 to FFh while trying to determine the value of the Bit sync amplitude signal quality threshold for registers 8 and 9. Monitor the Carrier Sense (CRS) output (TEST 6, pin 45) in test mode 1 and adjust the threshold to produce the desired rate of false detections. CRS indicates valid initial PN acquisition. After both thresholds are programmed in the device the CRS rate is a logic “and” of both signal qualities rate of occurrence over their respective thresholds and will therefore be much lower than either.

PN Correlators Description

There are two types of correlators in the HFA3860A baseband processor. The first is a parallel matched correlator that correlates for the Barker sequence used in preamble, header, and PSK data modes. This PN correlator is designed to handle BPSK spreading with carrier offsets up to ±50ppm and 11 chips per symbol. Since the spreading is BPSK, the correlator is implemented with two real correlators, one for the I and one for the Q Channel. The same Barker sequence is always used for both I and Q correlators.

These correlators are time invariant matched filters otherwise known as parallel correlators. They use one sample per chip for correlation although two samples per chip are processed. The correlator despreads the samples from the chip rate back to the original data rate giving 10.4dB processing gain for 11 chips per bit. While despreading the desired signal, the correlator spreads the energy of any non correlating interfering signal.

The second form of correlator is the serial correlator bank used for detection of the MBOK modulation. There is a bank of eight 8 chip correlators for the I Channel and another 8 for the Q Channel. These correlators integrate over the symbol and are

sampled at the symbol rate of 1.375MSPS. Each bank of correlators is connected to a biggest picker that finds the correlator output with the largest magnitude output. This finding of 1 out of 8 process determines 3 signal bits per correlator bank. The sign of the correlator output determines 1 more bit per bank. Thus, each bank of correlators can determine 4 bits at 1.375MSPS. This is a rate of 5.5MBPS. Only the I correlator bank is used for BMBOK. When both correlator banks are used, this becomes twice that rate or 11MBPS.

Data Demodulation and Tracking Description (DBPSK and DQPSK Modes)

The signal is demodulated from the correlation peaks tracked by the symbol timing loop (bit sync) as shown in Figure 14. The frequency and phase of the signal is corrected from the NCO that is driven by the phase locked loop. Demodulation of the DPSK data in the early stages of acquisition is done by delay and subtraction of the phase samples. Once phase locked loop tracking of the carrier is established, coherent demodulation is enabled for better performance. Averaging the phase errors over 16 symbols gives the necessary frequency information for proper NCO operation. The signal quality known as SQ2 is the variance in this estimate.

Configuration Register 15 sets the search timer for the SFD. This register sets this time-out length in symbols for the receiver. If the time out is reached, and no SFD is found, the receiver resets to the acquisition mode. The suggested value is # preamble symbols + 16. If several transmit preamble lengths are used by various transmitters in a network, the longest value should be used for the receiver settings.

Data Decoder and Descrambler Description

The data decoder that implements the desired DQPSK coding/decoding as shown in Table 10. The data is formed into pairs of bits called dibits. The left bit of the pair is the first in time. This coding scheme results from differential coding of the dibits. Vector rotation is counterclockwise for a positive phase shift, but can be reversed with bit 5 or 6 of CR2.

For DBPSK, the decoding is simple differential decoding.

TABLE 10. DQPSK DATA DECODER

PHASE SHIFT	DIBIT PATTERN (D0, D1) D0 IS FIRST IN TIME
0	00
+90	01
+180	11
-90	10

The data scrambler and descrambler are self synchronizing circuits. They consist of a 7-bit shift register with feedback of some of the taps of the register. The scrambler is designed to insure smearing of the discrete spectrum lines produced by the PN code.

One thing to keep in mind is that both the differential decoding and the descrambling cause error extension. This causes the errors to occur in groups of 4 and 6. This is due to two properties of the processing. First, the differential decoding process causes errors to occur in pairs. When a symbol error is made, it is usually a single bit error even in QPSK mode. When a symbol is in error, the next symbol will also be decoded wrong since the data is encoded in the change from one symbol to the next. Thus, two errors are made on two successive symbols. In QPSK mode, these may be next to one another or separated by up to 2 bits. Secondly, when the bits are processed by the descrambler, these errors are further extended. The descrambler is a 7-bit shift register with one or more taps exclusive or'ed with the bit stream. If for example the scrambler polynomial uses 2 taps that are summed with the data, then each error is extended by a factor of three. DQPSK errors can be spaced the same as the tap spacing, so they can be canceled in the descrambler. In this case, two wrongs do make a right, so the observed errors can be in groups of 4 instead of 6. If a single error is made the whole packet is discarded, so the error extension property has no effect on the packet error rate.

Descrambling is self synchronizing and is done by a polynomial division using a prescribed polynomial. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The transmit scrambler taps are programmed by CR 7.

Data Demodulation and Tracking Description (BMBOK and QMBOK Modes)

This demodulator handles the M-ary Bi-Orthogonal Keying (MBOK) modulation used for the two highest data rates. It is slaved to the low rate processor which it depends on for initial timing and phase tracking information. The high rate section coherently processes the signal, so it needs to have the I and Q Channels properly oriented and phased. The low rate section acquires the signal, locks up symbol and carrier tracking loops, and determines the data rate to be used for the MPDU data.

The demodulator for the MBOK modes takes over when the preamble and header have been acquired and processed. On the last bit of the header, the absolute phase of the signal is captured and used as a phase reference for the high rate demodulator as shown in Figure 15. The phase and frequency information from the carrier tracking loop in the low rate section is passed to the loop of the high rate section and control of the demodulator is passed to the high rate section.

The signal from the A/D converters is carrier frequency and phase corrected by a complex multiplier (mixer) that multiplies the received signal with the output of the Numerically Controlled Oscillator (NCO) and SIN/COS look up table. This removes the frequency offset and aligns the I and Q Channels properly for the correlators. The sample rate is decimated to 11MSPS for the correlators after the complex multiplier since the data is now synchronous in time.

The Walsh correlation section consists of a bank of 8 serial correlators on I and 8 on Q. Each of these correlators is programmed to correlate for its assigned spread function or its inverse. The demodulator knows the symbol timing, so the correlation is integrated over each symbol and sampled and dumped at the end of the symbol. The sampled correlation outputs from each bank are compared to each other in a biggest picker and the chosen one determines 4 bits of the symbol. Three bits come from which of the 8 correlators had the largest output and the fourth is determined from the sign of that output. In the 5.5MBPS or binary mode, only the I Channel is operated. This demodulates 4 bits per symbol. In the 11MBPS mode, both I and Q Channels are used and this detects 8 bits per symbol. The outputs are corrected for absolute phase and then serialized for the descrambler.

Chip tracking is performed on the de-rotated signal samples from the complex multiplier. These are alternately routed into two streams. The END chip samples are the same as those used for the correlators. The MID chip samples should lie on the chip transitions when the tracking is perfect. A chip phase error is generated if the END sign bits bracketing the MID samples are different. The sign of the error is determined by the sign of the END sample after the MID sample.

Tracking is only measured when there is a chip transition. Note that this tracking is mainly effective since there is a positive SNR in the chip rate bandwidth.

The symbol clock is generated by selecting one 44 MHz clock pulse out of every 32 pulses of the sample clock. Chip tracking adjusts the sampling in 1/8th chip increments by selecting which edge of the 44 MHz clock to use and which pulse. Timing adjustments can be made every 32 symbols as needed.

Carrier tracking is performed in a four phase Costas loop. The initial conditions are copied into the loop from the carrier loop in the low rate section. The END samples from above are used for the phase detection. The phase error for the 11MBps case is derived from Isign*Q-Qsign*I whereas in binary mode, it is simply Isign*Q. This forms the error term that is integrated in the lead/lag filter for the NCO, closing the loop.

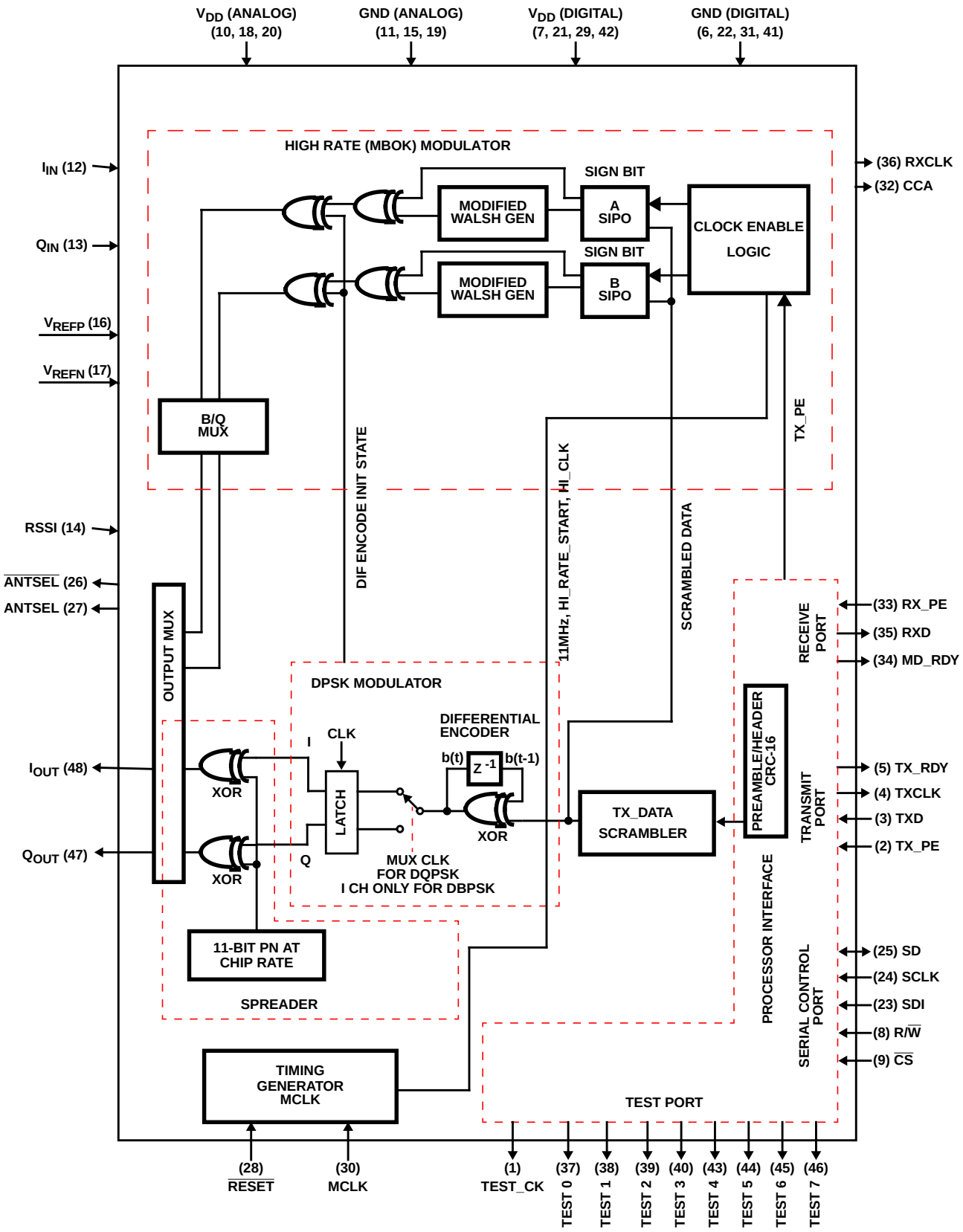
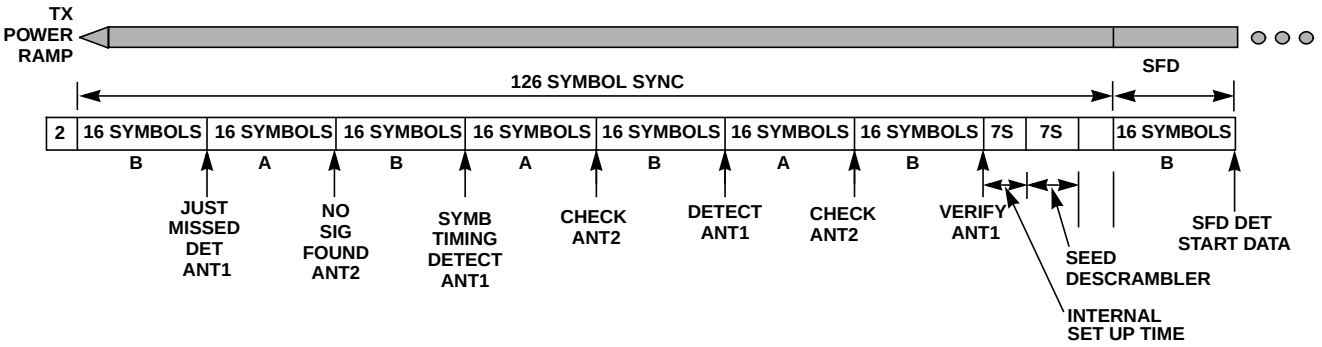


FIGURE 11. DSSS BASEBAND PROCESSOR, TRANSMIT SECTION



NOTES:

3. Worst Case Timing; antenna dwell starts before signal is full strength.
4. Time line shown assumes that antenna 2 gets insufficient signal.

FIGURE 12. DUAL ANTENNA ACQUISITION TIMELINE

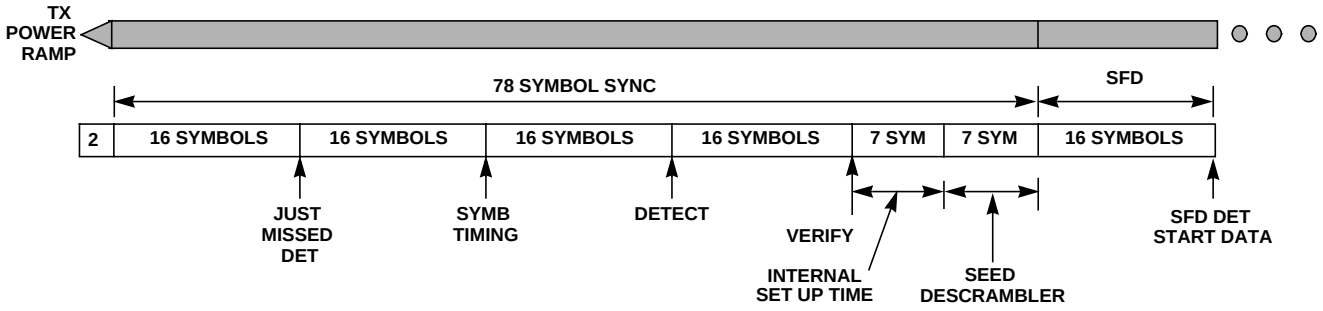


FIGURE 13. SINGLE ANTENNA ACQUISITION TIMELINE

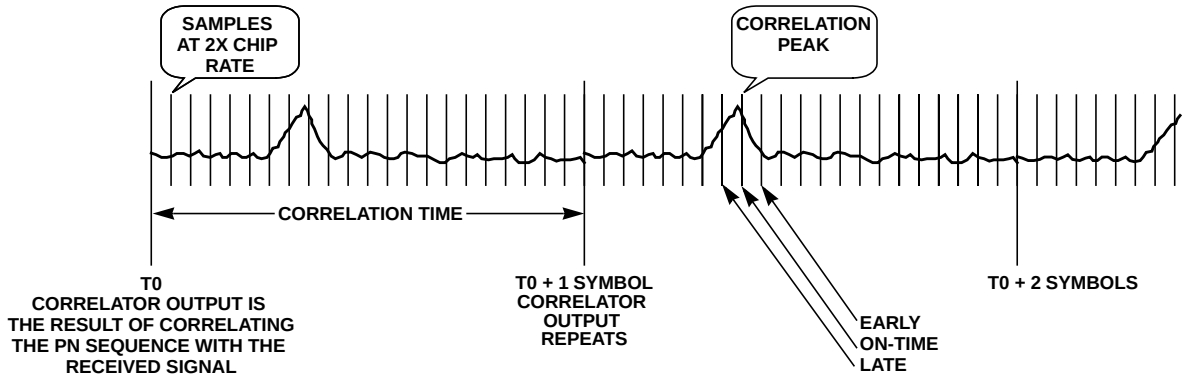


FIGURE 14. CORRELATION PROCESS

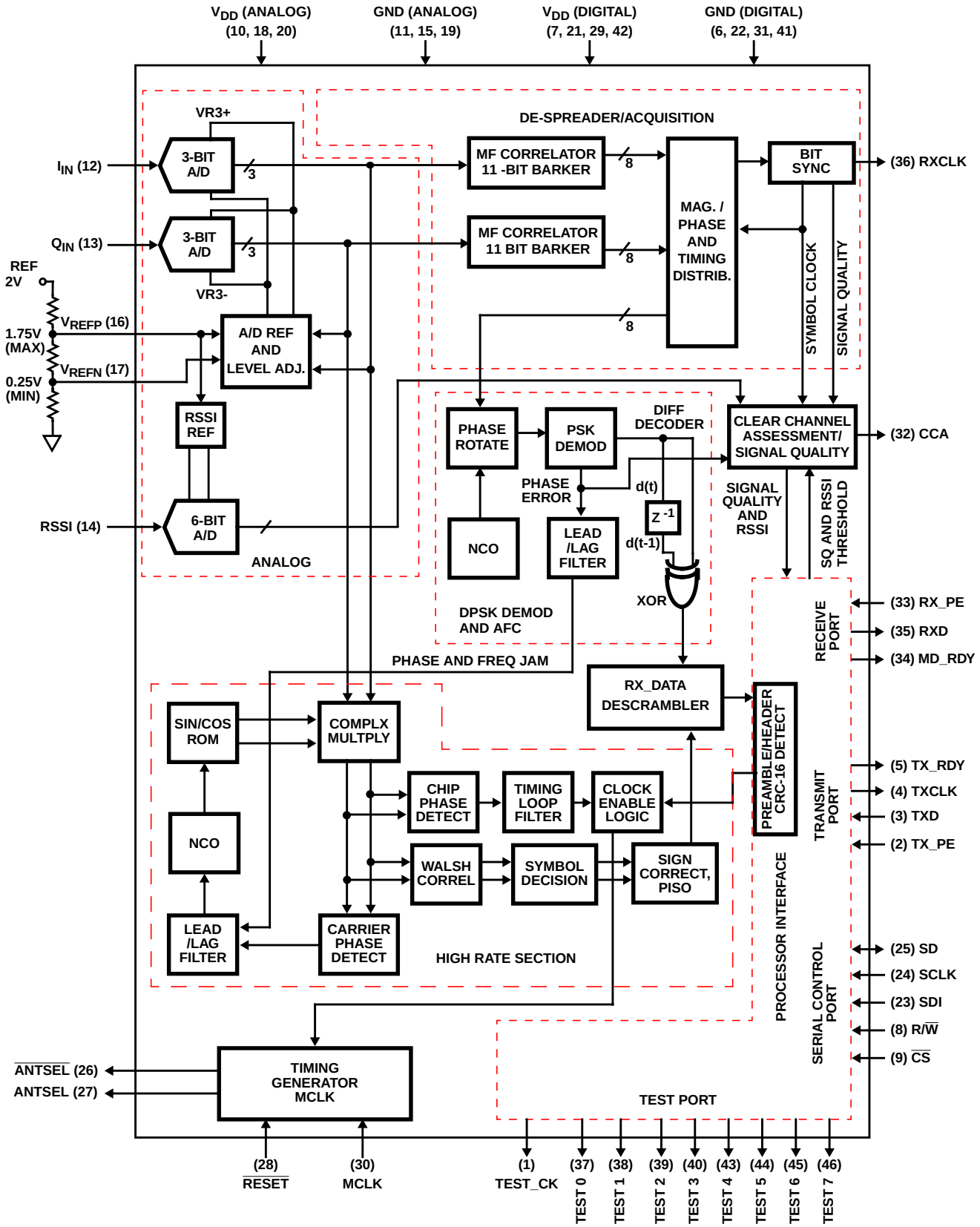


FIGURE 15. DSSS BASEBAND PROCESSOR, RECEIVE SECTION

Demodulator Performance

This section indicates the typical performance measures for a radio design. The performance data below should be used as a guide. In general, the actual performance depends on the application, interference environment, RF/IF implementation and radio component selection.

Overall Eb/N0 Versus BER Performance

The PRISM chip set has been designed to be robust and energy efficient in packet mode communications. The demodulator uses coherent processing for data demodulation. The figures below show the performance of the baseband processor when used in conjunction with the HSP3724 IF limiter and the PRISM recommended IF filters. Off the shelf test equipment are used for the RF processing. The curves should be used as a guide to assess performance in a complete implementation.

Factors for carrier phase noise, multipath, and other degradations will need to be considered on an implementation by implementation basis in order to predict the overall performance of each individual system.

Figure 16 shows the curves for theoretical DBPSK/DQPSK demodulation with coherent demodulation and descrambling as well as the PRISM performance measured for DBPSK and DQPSK. The theoretical performance for DBPSK and DQPSK are the same as shown on the diagram. Figure 17 shows the theoretical and actual performance of the MBOK modes. The losses in both figures include RF and IF radio losses; they do not reflect the HFA3860A losses alone. The HFA3860A baseband processing losses from theoretical are, by themselves, a small percentage of the overall loss.

The PRISM demodulator performs with an implementation loss of less than 3dB from theoretical in a AWGN environment with low phase noise local oscillators. For the 1 and 2MBps modes, the observed errors occurred in groups of 4 and 6 errors. This is because of the error extension properties of differential decoding and descrambling. For the 5.5MBps and 11MBps modes, the errors occur in symbols of 4 or 8 bits each and are further extended by the descrambling. Therefore the error patterns are less well defined.

Clock Offset Tracking Performance

The PRISM baseband processor is designed to accept data clock offsets of up to ±25ppm for each end of the link (TX and RX). This effects both the acquisition and the tracking performance of the demodulator. The budget for clock offset error is 0.75dB at ±50ppm and the performance is shown in Figure 18. This figure shows that the baseband processor in the high rate modes is better than at low rates in tracking clock offsets. The data for this figure and the next one was taken with the SNR into the receiver set to achieve $1E^{-5}$ BER with no offset. Then the offset was varied to determine the change in performance.

Carrier Offset Frequency Performance

The correlators used for acquisition for all modes and for demodulation in the 1MBps and 2MBps modes are time invariant matched filter correlators otherwise known as parallel correlators. They use two samples per chip and are tapped at every other shift register stage. Their performance with carrier frequency offsets is determined by the phase roll rate due to the offset. For an offset of +50ppm (combined for both TX and RX) will cause the carrier to phase roll 22.5 degrees over the length of the correlator. This causes a loss of 0.22dB in correlation magnitude which translates directly to Eb/N0 performance loss. In the PRISM chip design, the correlator is not included in the carrier phase locked loop correction, so this loss occurs for both acquisition and data. In the high rate modes, the data demodulation is done with a set of correlators that are included in the carrier tracking loop, so the loss is less. Figure 19 shows the loss versus carrier offset taken out to +75ppm (120kHz is 50ppm at 2.4GHz).

A Default Register Configuration

The registers in the HFA3860A are addressed with 6-bit numbers where the lower 2 bits of an 8-bit hexadecimal address are left as unused. This results in the addresses being in increments of 4 as shown in table 11.

Table 11 shows the register values for a default 802.11 configuration with dual antennas and various rate configurations. The data is transmitted as either DBPSK, DQPSK, BMBOK, or QMBOK depending on the configuration chosen. It is recommended that you start with the simplest configuration (DBPSK) for initial test and verification of the device and/or the radio design. The user can later modify the CR contents to reflect the system and the required performance of each specific application.

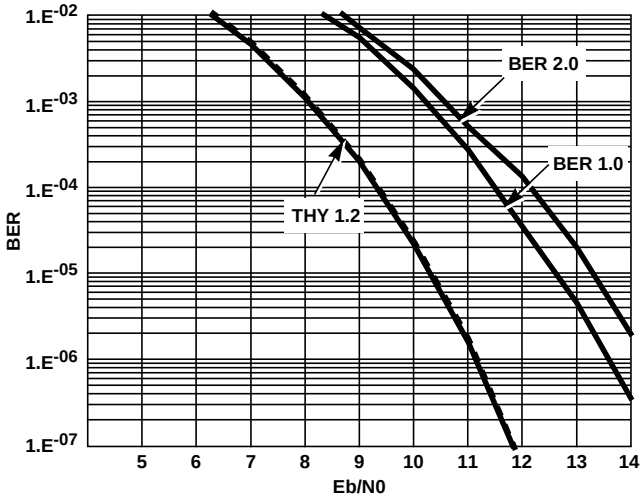


FIGURE 16. BER vs EB/N0 PERFORMANCE FOR PSK MODES

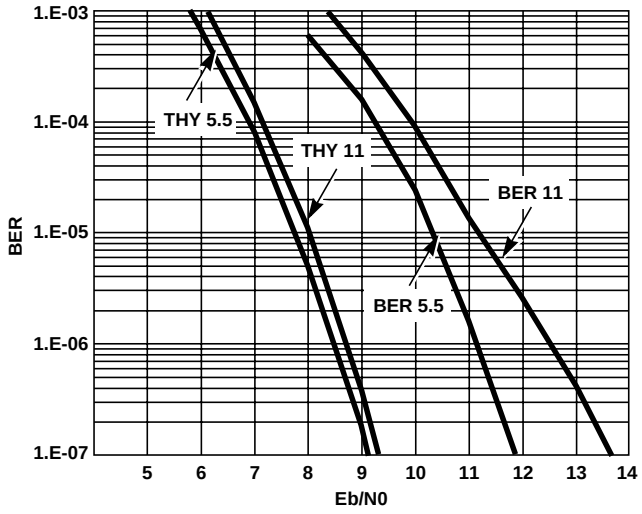


FIGURE 17. BER vs EB/N0 PERFORMANCE FOR MBOK MODES

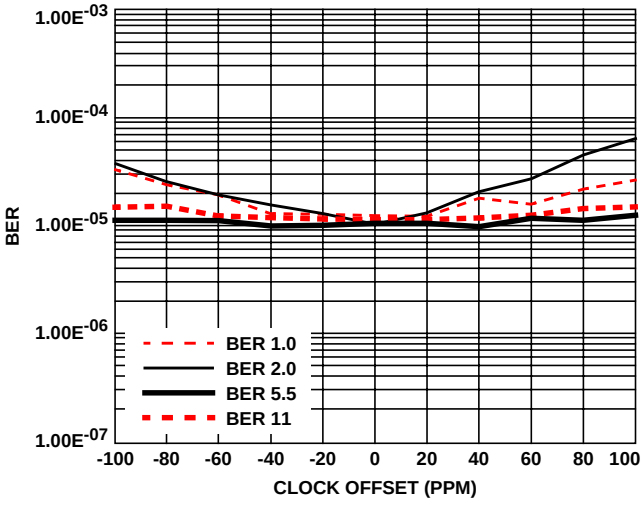


FIGURE 18. BER vs CLOCK OFFSET

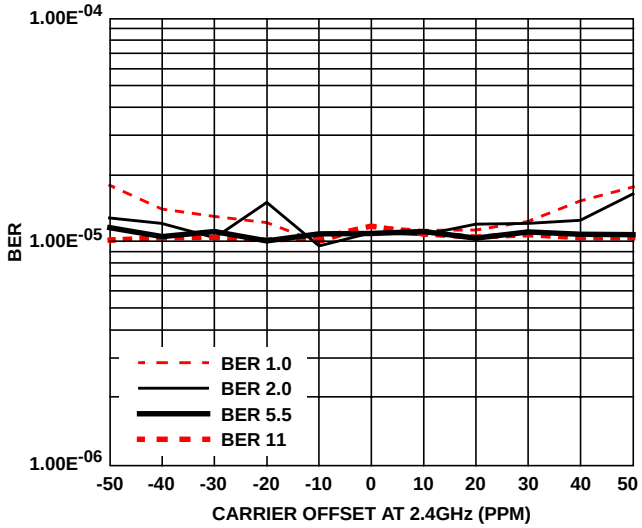


FIGURE 19. BER vs CARRIER OFFSET

TABLE 11. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	1/2/5.5/11MBps
CR0	Part / Version Code	R	00	01
CR1	I/O polarity	R/W	04	00
CR2	TX & RX Control	R/W	08	14
CR3	A/D_CAL_POS Register	R/W	0C	01
CR4	A/D_CAL_NEG Register	R/W	10	FF
CR5	CCA antenna control	R/W	14	2C
CR6	Preamble Length	R/W	18	80
CR7	Scramble_Tap (RX and TX)	R/W	1C	48
CR8	RX_SQ1_ ACQ (High) Threshold	R/W	20	01
CR9	RX-SQ1_ ACQ (Low) Threshold	R/W	24	88
CR10	RX_SQ2_ ACQ (High) Threshold	R/W	28	00
CR11	RX-SQ2_ ACQ (Low) Threshold	R/W	2C	98

TABLE 11. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	1/2/5.5/11MBps
CR12	SQ1 CCA Thresh (high)	R/W	30	01
CR13	SQ1 CCA Thresh (low)	R/W	34	98
CR14	ED or RSSI Thresh	R/W	38	20
CR15	SFD Timer	R/W	3C	90
CR16	Signal Field (BPSK - 11 Chip Barker sequence)	R/W	40	0A
CR17	Signal Field (QPSK - 11 Chip Barker sequence)	R/W	44	14
CR18	Signal Field (BPSK - Mod Walsh sequence)	R/W	48	37
CR19	Signal Field (QPSK - Mod Walsh sequence)	R/W	4C	6E
CR20	TX Signal Field	R/W	50	00/01/02/03
CR21	TX Service Field	R/W	54	00
CR22	TX Length Field (high)	R/W	58	FF
CR23	TX Length Field (low)	R/W	5C	FF
CR24	RX Status	R	60	X
CR25	RX service Field Status	R	64	X
CR26	RX Length Field status (high)	R	68	X
CR27	RX Length Field status (low)	R	6C	X
CR28	Test Bus Address	R/W	70	00
CR29	Test Bus Monitor	R	74	X
CR30	Test Register 1	R/W	78	00
CR31	RX Control	R/W	7C	01

Control Registers

The following tables describe the function of each control register along with the associated bits in each control register.

CONFIGURATION REGISTER 0 ADDRESS (0h) PART/VERSION CODE

Bit 7:4	Part Code 0 = HFA3860A
Bit 3:0	Version Code 2 = Second Version

CONFIGURATION REGISTER 1 ADDRESS (04h) I/O POLARITY

	This register is used to define the phase of clocks and other interface signals. 00h is normal setting.
Bit 7	This controls the phase of the RX_CLK output Logic 1 = Invert Clk Logic 0 = Non-Inverted Clk
Bit 6	This control bit selects the active level of the MD_RDY output pin 34. Logic 1 = MD_RDY is Active 0 Logic 0 = MD_RDY is Active 1
Bit 5	This control bit selects the active level of the Clear Channel Assessment (CCA) output pin 32. Logic 1 = CCA Active 1 Logic 0 = CCA Active 0
Bit 4	This control bit selects the active level of the Energy Detect (ED) output which is an output pin at the test port, pin 44. Logic 1 = ED Active 0 Logic 0 = ED Active 1

CONFIGURATION REGISTER 1 ADDRESS (04h) I/O POLARITY

Bit 3	This control bit selects the active level of the Carrier Sense (CRS) output pin which is an output pin at the test port, pin 45. Logic 1 = CRS Active 0 Logic 0 = CRS Active 1
Bit 2	This control bit selects the active level of the transmit enable (TX_PE) input pin 2. Logic 1 = TX_PE Active 0 Logic 0 = TX_PE Active 1
Bit 1	This control bit selects the phase of the transmit output clock (TXCLK) pin 4. Logic 1 = Inverted TXCLK Logic 0 = NON-Inverted TXCLK
Bit 0	Must be set to “0”

CONFIGURATION REGISTER 2 ADDRESS (08h) TX AND RX CONTROL

Write to control, Read to verify control, setup while TX_PE and RX_PE are low

Bit 7	MCLK control. 0 = 44MHz All signal modes supported. 1 = 22MHz 1MBPS and 2MBPS, B/QPSK 11 Chip sequence mode only. Reduced power mode.
Bit 6	TX Rotation 0 = Normal 1 = Invert Q Out
Bit 5	RX Rotation 0 = Normal 1 = Invert Q IN
Bit 4	A/D Calibration 0 = A/D_CAL Off 1 = A/D_CAL On
Bit 3	A/D Calibration control (only valid if A/D Calibration is on). 0 = A/D Calibration only while in receive tracking mode (A/D Calibration set on signals only). 1 = A/D Calibration while receive RX_PE is active (in this mode, the A/D Calibration will be set primarily on noise).
Bit 2	This bit enables/disables energy detect (ED) for the CCA function. 0 = ED Off 1 = ED On
Bit 1	MD_RDY Start. Sets where MD_RDY will become active. 0 = After SFD detect (normal). This allows the header fields to be enveloped by MD_RDY. 1 = After Header CRC verify and start of MPDU. Header data can be read from Configuration Registers.
Bit 0	TX and RX Clock 0 = Enable Gated clocks (normal). RX clock will come on to clock out header fields, go off during CRC and come back on for MPDU data. Header rate is 1MHz, data rate is variable. TXCLK comes on after TXRDY active. 1 = Clocks start as soon as modem starts tracking and remain on until either header checks fail or until RX_ PE goes back low. This is only usable in the 1MBPS and 2MBPS modes. TXCLK comes on after TX_PE active.

CONFIGURATION REGISTER 3 ADDRESS (0Ch) A/D CAL POS

Bits 0 - 7	This 8-bit control register contains a binary value used for positive increment for the level adjusting circuit of the A/D reference. The larger the step the faster the A/D Calibration settles.

CONFIGURATION REGISTER 4 ADDRESS (10h) A/D CAL NEG

Bits 0 - 7	This 8-bit control register contains a binary value used for the negative increment for the level adjusting circuit of the A/D reference. The number is programmed as 256 - the value wanted since it is a negative number.

CONFIGURATION REGISTER 5 ADDRESS (14h) CCA ANTENNA CONTROL

Bits 7:6	R/W, But Not Used Internally
Bit 5	0 = Normal 1 = A/D timing adjustment during acquisition, deassertion of RXPE required to activate.

CONFIGURATION REGISTER 5 ADDRESS (14h) CCA ANTENNA CONTROL (Continued)

Bit 4	0 = Normal 1 = Delayed bit sync accumulation
Bit 3	0 = Normal 1 = Use multipath antenna selection (SQ3)
Bit 2	RX Diversity 0 = Off Single antenna, can use A or B (see bits 1:0). 1 = On Antenna switches during acquisition every 16 us. Starts cycle on antenna defined by bits 1:0.
Bits 1:0	CCA Antenna mode. Defines the antenna to be used at the start of acquisition for CCA checking and for subsequent transmission. TX antenna is always the same as used to check CCA. Controls antenna selection via the ANT_SEL pin. 00 = Use last Receive antenna for CCA checking and TX. Acquisition starts on the antenna which had a valid header on last reception. 01 = Illegal State - Unknown Behavior 10 = Use antenna B for CCA and TX (single antenna). AntSel = 0 11 = Use antenna A for CCA and TX (single antenna). AntSel = 1

CONFIGURATION REGISTER 6 ADDRESS (18h) PREAMBLE LENGTH

Bits 0 - 7	This register contains the count for the Preamble length counter. Setup while TX_PE is low. For IEEE 802.11 use 80h. For other than IEEE 802.11 applications, in general increasing the preamble length will improve low signal to noise acquisition performance at the cost of greater link overhead. For dual receive antenna operation, the minimum suggested value is 128d = 80h. For single receive antenna operation, the minimum suggested value is 80d = 50h. These suggested values include a 2 symbol TX power amplifier ramp up. If you program 128 you get 130.

CONFIGURATION REGISTER 7 ADDRESS (1Ch) SCRAMBLER TAPS

Bit 7	0 = Normal, RX_PE Enables/Disables the internal receive clock. I = Internal receive clock is always enabled.
Bits 6:0	This register is used to configure the transmit scrambler with a 7-bit polynomial tap configuration. The transmit scrambler is a 7-bit shift register, with 7 configurable taps. A logic 1 is the respective bit position enables that particular tap. The example below illustrates the register configuration for the polynomial $F(x) = 1 + X^{-4}+X^{-7}$. Each clock is a shift left.

		LSB
Bits (6:0)		6 5 4 3 2 1 0
Term		$X^{-7}X^{-6}X^{-5}X^{-4}X^{-3}X^{-2}X^{-1}$
Scrambler Taps	$F(x) = 1 + X^{-4}+X^{-7}$	1 0 0 1 0 0 0

CONFIGURATION REGISTER 8 ADDRESS (20h) SQ1 ACQ THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements made during acquisition at each antenna dwell. This threshold comparison is added with the SQ2 threshold in registers 10 and 11 for acquisition. A lower value on this threshold will increase the probability of detection and the probability of false alarm.

CONFIGURATION REGISTER 9 ADDRESS (24h) SQ1 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition at each antenna dwell.

CONFIGURATION REGISTER 10 ADDRESS (28h) SQ2 ACQ THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8-15) of the carrier phase variance threshold used for acquisition. This register combined with the lower byte represents a 16-bit threshold value for carrier phase variance measurement made during acquisition at each antenna dwell and is based on the choice of the best antenna. This threshold is used with the bit sync threshold in registers 8 and 9 to declare acquisition. A higher value in this threshold will increase the probability of acquisition and false alarm.

CONFIGURATION REGISTER 11 ADDRESS (2Ch) SQ2 ACQ THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0-7) of the carrier phase variance threshold used for acquisition.

CONFIGURATION REGISTER 12 ADDRESS (30h) SQ1 CCA THRESHOLD (HIGH)

Bits 0 - 7	This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for CCA estimation. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition on CCA antenna dwell. A lower value on this threshold will increase the probability of detection and the probability of false alarm. Set the threshold according to instructions in the text.

CONFIGURATION REGISTER 13 ADDRESS (34h) SQ1 CCA THRESHOLD (LOW)

Bits 0 - 7	This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for CCA. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition on CCA antenna dwell.

CONFIGURATION REGISTER 14 ADDRESS (38h) ED OR RSSI THRESHOLD

Bit 7:6	R/W, But Not Used Internally
Bits 5:0	This register contains the value for the RSSI threshold for measuring and generating energy detect (ED). When the RSSI exceeds the threshold ED is declared. ED indicates the presence of energy in the channel.

	MSB LSB	
Bits (0:5)	5 4 3 2 1 0	
	0 0 0 0 0 0	00h (Min)
RSSI_STAT	1 1 1 1 1 1	3Fh (Max)

To disable the ED signal so that it has no affect on the CCA logic, the threshold must be set to a 3Fh (all ones).

CONFIGURATION REGISTER 15 ADDRESS (3Ch) SFD TIMER

Bits 7:0	This register is programmed with an 8-bit value which represents the length of time for the demodulator to search for a SFD in a receive Header. Each bit increment represents 1 symbol period. Failure to find the SFD will result in a return to acquisition mode.

CONFIGURATION REGISTER 16 ADDRESS (40h) SIGNAL FIELD DBPSK

Bits 7:0	This register contains an 8-bit value defining the data packet modulation as DBPSK. This value will be a 0Ah for 802.11, and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received Header.

CONFIGURATION REGISTER 17 ADDRESS (44h) SIGNAL FIELD DQPSK

Bits 7:0	This register contains the 8-bit value defining the data packet modulation as DQPSK. This value will be a 14h for full protocol operation at a data rate of 2MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header.

CONFIGURATION REGISTER 18 ADDRESS (48h) SIGNAL FIELD BMBOK

Bits 7:0	This register contains the 8-bit value defining the data packet modulation as BMBOK. This value will be a 37h for operation at a data rate of 5.5MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header.

CONFIGURATION REGISTER 19 ADDRESS (4Ch) SIGNAL FIELD QMBOK

Bits 7:0	This register contains the 8-bit value defining the data packet modulation as QMBOK. This value will be a 6Eh for operation at a data rate of 11MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header.

CONFIGURATION REGISTER 20 ADDRESS (50h) TX SIGNAL FIELD

Bits 7:3	R/W, But Not Used Internally
Bit 2	0 = Normal 1 = Transmit QPSK (2MBPS) with no header, bits 1:0 must be 00 (see Tech Brief 365)
Bits 1:0	TX data Rate. Must be set at least 2µs before needed in TX frame. This selects TX signal field code from the registers above. 00 = DBPSK - 11 chip sequence (1MBPS) 01 = DQPSK - 11 chip sequence (2MBPS) 10 = BMBOK - modified 8 chip Walsh sequence (5.5MBPS) 11 = QMBOK - modified 8 chip Walsh sequence (11MBPS)

CONFIGURATION REGISTER 21 ADDRESS (54h) TX SERVICE FIELD

Bits 7:0	This 8-bit register is programmed with the 8-bit value of the Service field to be transmitted in the Header. This field is reserved for future use and should always be set to 00h.

CONFIGURATION REGISTER 22 ADDRESS (58h) TX LENGTH FIELD (HIGH)

Bits 7:0	This 8-bit register contains the higher byte (bits 8-15) of the transmit Length Field described in the Header. This byte combined with the lower byte indicates the number of microseconds the data packet will take.

CONFIGURATION REGISTER 23 ADDRESS (5Ch) TX LENGTH FIELD (LOW)

Bits 7:0	This 8-bit register contains the lower byte (bits 0-7) of the transmit Length Field described in the Header. This byte combined with the higher byte indicates the number of microseconds the data packet will take.

CONFIGURATION REGISTER 24 ADDRESS (60h) RX STATUS

This read only register is provided for MACs that can't process the header fields from the RXD port.

Bits 7:6	RX signal field detected 00 = DBPSK - 11 Chip Sequence (1MBPS) 01 = DQPSK - 11 Chip Sequence (2MBPS) 10 = BMBOK - modified 8 chip Walsh sequence (5.5MBPS) 11 = QMBOK - modified 8 chip Walsh sequence (11MBPS)
Bit 5	Search/Acquisition Status (set to 0 when RX_PE is inactive) 0 = Searching 1 = Carrier Acquired
Bit 4	SFD search status (set to 0 when RX_PE is inactive) 0 = Searching 1 = SFD Found
Bit 3	Signal Field Valid (set to 0 when RX_PE is inactive) signal field must be one of the 4 field values in CR 16 to CR19 0 = Not Valid 1 = Valid
Bit 2	Valid header CRC (set to 0 when RX_PE is inactive) 0 = Not Valid 1 = Valid
Bit 1	Antenna received on. Indicates antenna the receiver was on when last valid CRC check occurred. 0 = Antenna B 1 = Antenna A
Bit 0	Always 0

CONFIGURATION REGISTER 25 ADDRESS (64h) RX SERVICE FIELD STATUS

Bits 7:0	This register contains the detected received 8-bit value of the Service Field for the Header. This field is reserved for future use. It should be the value programmed into register 21 of the transmitter.

CONFIGURATION REGISTER 26 ADDRESS (68h) RX LENGTH FIELD STATUS (HIGH)

Bits 7:0	This register contains the detected higher byte (bits 8-15) of the received Length Field contained in the Header. This byte combined with the lower byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER ADDRESS 27 (6Ch) RX LENGTH FIELD STATUS (LOW)

Bits 7:0	This register contains the detected lower byte of the received Length Field contained in the Header. This byte combined with the upper byte indicates the number of transmitted bits in the data packet.

CONFIGURATION REGISTER 28 ADDRESS (70h) TEST BUS ADDRESS

Supplies address for test pin outputs and Test Bus Monitor Register

Bits 7:0	**Test Bus Address = 00h** **Quiet Test Bus** Test 7:0 = 00 TEST_CLK = 0
Bits 7:0	**Test Bus Address = 01h** **RX Acquisition Monitor** These bits sequentially go high as the signal is input. Transitions are aligned to chip boundaries. Bits are reset after last chip of message. Test 7 = A/DCal (Full Scale) Test 6 = CRS, Carrier Sense Test 5 = ED, energy detect comparator output Test 4 = Track, indicates start of tracking and start of SFD time-out Test 3 = SFD Detect, variable time after track start Test 2 = Signal Field Ready, ~ 8µs after SFD Detect Test 1 = Length Field Ready, ~ 32µs after SFD Detect Test 0 = Header CRC Valid, ~ 48µs after SFD Detect TEST_CLK = Initial Detect
Bits 7:0	**Test Bus Address = 02h** **TX Field Monitor.** These bits sequentially go high as the signal is output. Transitions are aligned to chip boundaries. Bits are reset after last chip of valid message. Test 7 = A/DCal (Full Scale) Test 6 = TXPE Internal, Inactive edge of pad TXPE delayed Test 5 = Preamble Start Test 4 = SFD Start Test 3 = Signal Field Start Test 2 = Length Field Start Test 1 = Header CRC Start Test 0 = MPDU Start TEST_CLK = IQMARK, identifies symbol boundaries on IOUT and QOUT
Bits 7:0	**Test Bus Address = 03h** **RSSI Monitor** Test 7 = CSE Enhanced. Used in enhanced CCA dual antenna mode. Test 6 = CSE, Carrier Sense Early (SQI CCA Only) Test 5:0 = RSSI(5:), bit 5 is MSB, straight binary (000000 = Min, 11111 = Max) TEST_CLK = RSSI A/D CLK, Sample RSSI(5:0) on last rising edge 
Bits 7:0	**Test Bus Address = 04h** **SQ1 Monitor** Test 7:0 = SQ1 (7:0) TEST_CLK = pulse after SQ is valid
Bits 7:0	**Test Bus Address = 05h** **SQ2 Monitor** - SQ3 output if SQ3 used for antenna diversity. Test 7:0 = SQ2 (7:0) TEST_CLK = pulse after SQ is valid
Bits 7:0	**Test Bus Address = 06h** **Correlator Lo Rate** Test 7:0 = Correlator Magnitude Lo Rate Only TEST_CLK = Sample CLK

CONFIGURATION REGISTER 28 ADDRESS (70h) TEST BUS ADDRESS (Continued)

Supplies address for test pin outputs and Test Bus Monitor Register

Bits 7:0	**Test Bus Address = 07h** **Freq Test Lo Rate** Test 7:0 = Freq Reg Lo Rate (18:11) TEST_CLK = SUBSAMPLECLK (Symbol Clock)
Bits 7:0	**Test Bus Address = 08h** **Phase Test Lo Rate** Test 7:0 = Phase Reg Lo Rate (7:0) TEST_CLK = SUBSAMPLECLK (Symbol Clock)
Bits 7:0	**Test Bus Address = 09h** **NCO Test Lo Rate** Test 7:0 = NCO Reg Lo Rate (15:8) TEST_CLK = SUBSAMPLECLK (Symbol Clock)
Bits 7:0	**Test Bus Address = 0Ah** **Bit Sync Accum Lo Rate** Test 7:0 = Bit Sync Accumulator (7:3), exponent (2:0) TEST_CLK = Last symbol indicator
Bits 7:0	**Test Bus Address = 0Bh** **Test PN Gen.,** Factory Test Only Test 7:0 +TEST_CLK = Top 9 bits of PN generator used for fault tests.
Bits 7:0	**Test Bus Address = 0Ch** **A/D Cal Test Mode** Test 7 = A/D CAL (Full Scale) Test 6 = ED, Energy Detect Comparator Output Test 5 = A/D_CAL Disable Test(4:0) = A/D_Cal(4:0) TEST_CLK = A/D_Cal CLK
Bits 7:0	**Test Bus Address = 0Dh** **Correlator I High Rate,** tests the MBOK I correlator output. Test 7:0 = Correlator I Hi Rate (8:1) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 0Eh** **Correlator Q High Rate,** tests the MBOK Q correlator output. Test 7:0 = Correlator Q Hi Rate (8:1) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 0Fh** **Chip Error Accumulator,** Test 7:0 = Chip Error Accumulator (14:7) TEST_CLK = 0
Bits 7:0	**Test Bus Address = 10h** **NCO Test Hi Rate,** tests the NCO in the high rate tracking section. Test 7:0 = NCO Accum (19:12) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 11h** **FREQ Test Hi Rate,** tests the NCO lag accumulator in the high rate tracking section. Test 7:0 = Lag Accum (18:11) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 12h** **Carrier Phase Error Hi Rate** Test 7:0 = Carrier Phase Error (6,6:0) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 13h** **I_ROT Hi Rate,** tests the I Channel phase rotation error signal. Test 7:0 = I_ROT (5,5,5:0) TEST_CLK = Sample CLK

CONFIGURATION REGISTER 28 ADDRESS (70h) TEST BUS ADDRESS (Continued)

Supplies address for test pin outputs and Test Bus Monitor Register

Bits 7:0	**Test Bus Address = 14h** **Q_ROT Hi Rate** Test 7:0 = Q_ROT (5,5,5:0) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 15h** **I_A/D, Q_A/D,** tests the I and Q Channel 3-bit A/D Converters. Test 7:6 = 0 Test 5:3 = I_A/D (2:0) Test 2:0 = Q_A/D (2:0) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 16h** **XOR Hi Rate,** Factory Test Only Test 7:0 + TEST_CLK = 9 bits of registered XOR test data from the high rate logic.
Bits 7:0	**Test Bus Address = 17h** **XOR Fast,** Factory Test Only Test 7:0 + TEST_CLK = 9 bits of registered XOR test data from the low rate logic.
Bits 7:0	**Test Bus Address = 18h** **Timing Test,** tests the receiver timing. Test 7 = JMPCLK Test 6 = JMPCNT Test 5 = SUBSAMPLECLK Test 4:0 = MASTERTIM(4:0) TEST_CLK = Sample CLK
Bits 7:0	**Test Bus Address = 19h** **A/D Cal Accum Lo,** tests the lo bits of the A/D cal accumulator. Test 7:0+TestCLK = A/D Cal Accum (8:0)
Bits 7:0	**Test Bus Address = 1Ah** **A/D Cal Accum Hi,** tests the hi bits of the A/D cal accumulator. Test 7:0+TestCLK = A/D Cal Accum (17:9)
Bits 7:0	**Test Bus Address = 1Bh** **Freq Accum Lo,** tests the frequency accumulator of the low rate section. Test 7:0+TestCLK = Freq Accum (15:7)
Bits 7:0	**Test Bus Address = 1Ch** **Slow XOR,** Factory Test Test 7:0 = 8 bits of registered XOR test data from the low rate logic TEST_CLK = SUBSAMPLECLK
Bits 7:0	**Test Bus Address = 1Dh** **SQ2 Monitor Hi** - SQ3 if SQ3 used for antenna diversity Test 7:0 = SQ2 (15:8) TEST_CLK = pulse after SQ is valid
Bits 7:0	**Test Bus Address = 1Eh to 1Fh** **Reserved** Test 7:0 + TestCLK = 0

CONFIGURATION REGISTER 29 ADDRESS (74h) TEST BUS MONITOR

Bits 7:0	Maps test bus pins 7:0 to read only value 7:0 when test bus address is supplied by CR 28

CONFIGURATION REGISTER 30 ADDRESS (78h) TEST REGISTER 1

Bits 7	PN Generator for Fault Test 0 = Normal 1 = Enabled
Bit 6	HR Jumpclock control 0 = Normal Enable HR Jumpclock 1 = Disabled

CONFIGURATION REGISTER 30 ADDRESS (78h) TEST REGISTER 1 (Continued)

Bit 5	HR Demod XOR to Test Bus Enable 0 = Normal 1 = Enabled
Bit 4	Random Address to Test Bus 0 = Normal 1 = Enabled
Bit 3	Faster Cal 0 = Normal 1 = Enabled When enabled, the 1kHz clock used to update the A/D cal bits is increased to 22kHz.
Bit 2	A/D Cal Test Mode 0 = Normal 1 = Enabled When enabled, the 5 A/D cal bits come from CR3<4:0> to allow direct control.
Bit 1	A/D Test Mode 0 = Normal 1 = Enabled When enabled, this bit causes all 12 bits of A/D outputs (6 RSSI, 3 I, 3 Q) to be directly output on pins of the HFA3860A. Modem is nonfunctional.
Bit 0	Loop Back 0 = Normal 1 = Enabled When enabled, this bit routes the I and Q outputs to the I and Q inputs of the modem. The 3-bit I&Q A/Ds are bypassed.

CONFIGURATION REGISTER 31 ADDRESS (7Ch) RX CONTROL

Bits 7:3	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 2	RX QPSK Acquire 0 = Normal 1 = Acquire on QPSK (2MBPS) see Tech Brief 365.
Bit 1	Disable Control 0 = ED disabled after MD_RDY active 1 = ED runs continuously
Bit 0	CCA Type Select 1 = RAW CCA, updates every ANT Dwell 0 = Enhanced CCA

Absolute Maximum Ratings

Supply Voltage 7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +2.70V to +3.60V
Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} ($^oC/W$)
TQFP Package 80
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Die Characteristics

Gate Count . . . . . 33,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 3.0V to 3.3V ±10%, T_A = -40^oC to 85^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.6V, CLK Frequency 44MHz (Notes 6, 7)	-	30	40	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	0.5	1	mA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min	0.7 V_{CC}	-	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max	-	-	$V_{CC}/3$	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min	V_{CC}-0.2	-	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	.2	0.2	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25^oC, Note 7	-	5	10	pF
Output Capacitance	C_{OUT}		-	5	10	pF

NOTES:

6. Output load 30pF.
7. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

V_{CC} = 3.0V to 3.3V ±10%, T_A = -40^oC to 85^oC (Note 8)

PARAMETER	SYMBOL	MCLK = 44MHz		UNITS
		MIN	MAX	
MCLK Period	t_{CP}	22	-	ns
MCLK Duty Cycle		43/57	57/43	%
Rise/Fall (All Outputs)		-	10	ns (Notes 9, 10)
TX_PE to Iout/Qout (1st Valid Chip)	t_{D1}	2.18	2.3	µs (Notes 9, 11)
TX_PE Inactive Width	t_{TLP}	2.22	-	µs (Notes 9, 12)
TX_CLK Width Hi or Low	t_{TCD}	40	-	ns
TX_RDY Active to 1st TX_CLK Hi	t_{RC}	260	-	ns
Setup TXD to TX_CLK Hi	t_{TDS}	30	-	ns
Hold TXD to TX_CLK Hi	t_{TDH}	0	-	ns
TX_CLK to TX_PE Inactive (1MBps)	t_{PEH}	0	965	ns (Notes 9, 22)
TX_CLK to TX_PE Inactive (2MBps)	t_{PEH}	0	420	ns (Notes 9, 22)
TX_CLK to TX_PE Inactive (5.5MBps)	t_{PEH}	0	160	ns (Notes 9, 22)
TX_CLK to TX_PE Inactive (11MBps)	t_{PEH}	0	65	ns (Notes 9, 22)
TX_RDY Inactive To Last Chip of MPDU Out	t_{RI}	-20	20	ns
TXD Modulation Extension	t_{ME}	2	-	µs (Notes 9, 13)

AC Electrical Specifications V_{CC} = 3.0V to 3.3V ±10%, T_A = -40°C to 85°C (Note 8) **(Continued)**

PARAMETER	SYMBOL	MCLK = 44MHz		UNITS
		MIN	MAX	
RX_PE Inactive Width	t_{RLP}	70	-	ns (Notes 9, 14)
RX_CLK Period (1MBps Mode)	t_{RCP}	77	-	ns
RX_CLK Width Hi or Low (11MBps Mode)	t_{RCD}	31	-	ns
RX_CLK to RXD	t_{RDD}	25	60	ns
MD_RDY to 1st RX_CLK	t_{RD1}	940	-	ns (Notes 9, 17)
RXD to 1st RX_CLK	t_{RD1}	940	-	ns
Setup RXD to RX_CLK	t_{RDS}	31	-	ns
RX_CLK to RX_PE Inactive (1MBps)	t_{REH}	0	925	ns (Notes 9, 15)
RX_CLK to RX_PE Inactive (2MBps)	t_{REH}	0	380	ns (Notes 9, 15)
RX_CLK to RX_PE Inactive (5.5MBps)	t_{REH}	0	140	ns (Notes 9, 15)
RX_CLK to RX_PE Inactive (11MBps)	t_{REH}	0	50	ns (Notes 9, 15)
RX_PE inactive to MD_RDY Inactive	t_{RD2}	5	30	ns (Note 16)
Last Chip of SFD in to MD_RDY Active	t_{RD3}	2.77	2.86	µs (Notes 9, 17)
RX Delay		2.77	2.86	µs (Notes 9, 18)
RESET Width Active	t_{RPW}	50	-	ns (Notes 9, 19)
RX_PE to CCA Valid	t_{CCA}	-	16	µs (Notes 9, 20)
RX_PE to RSSI Valid	t_{CCA}	-	16	µs (Notes 9, 20)
ANTSEL Lead Time		820	-	ns (Notes 9, 21)
SCLK Clock Period	t_{SCP}	90	-	ns
SCLK Width Hi or Low	t_{SCW}	20	-	ns
Setup to SCLK + Edge (SD, SDI, R/W, CS)	t_{SCS}	30	-	ns
Hold Time from SCLK + Edge (SD, SDI, R/W, CS)	t_{SCH}	0	-	ns
SD Out Delay from SCLK + Edge	t_{SCD}	-	30	ns
SD Out Enable/Disable from R/W	t_{SCED}	-	15	ns (Note 9)
TEST 0-7, CCA, ANTSEL, TEST_CK from MCLK	t_{D2}	-	40	ns

NOTES:

8. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -1mA. Input reference level all inputs 1.5V. Test $V_{IH} = V_{CC}$, V_{IL} = 0V; $V_{OH} = V_{OL} = V_{CC}/2$.
9. Not tested, but characterized at initial design and at major process/design changes, or guaranteed by design.
10. Measured from V_{IL} to V_{IH}.
11. Iout/Qout are modulated before first valid chip of preamble is output to provide ramp up time for RF/IF circuits.
12. TX_PE must be inactive before going active to generate a new packet.
13. Iout/Qout are modulated after last chip of valid data to provide ramp down time for RF/IF circuits.
14. RX_PE must be inactive at least 3 MCLKs before going active to start a new CCA or acquisition.
15. RX_PE active to inactive delay to prevent next RX_CLK.
16. Assumes RX_PE inactive after last RX_CLK.
17. MD_RDY programmed to go active after SFD detect (measured from I_{IN}, Q_{IN}).
18. MD_RDY programmed to go active at MPDU start. Measured from first chip of first MPDU symbol at I_{IN}, Q_{IN} to MD_RDY active.
19. Minimum time to insure Reset. RESET must be followed by an RX_PE pulse to insure proper operation. This pulse should not be used for first receive or acquisition.
20. CCA and RSSI are measured once during the first 16 us interval following RX_PE going active. RX_PE must be pulsed to initiate a new measurement. RSSI may be read via serial port or from Test Bus.
21. ANTSEL is switched in diversity mode before acquisition cycle to compensate for delays in IF circuits. The correlators will be 100X(820ns - TdRFns)/990 ns% full of new data at the beginning of bit sync accumulation. TdRFns is the settling time of the RF circuits after ANTSEL switches.
22. Delay from TXCLK to inactive edge of TXPE to prevent next TXCLK. Because TXPE asynchronously stops TXCLK, TXPE going inactive within 40ns of TXCLK will cause TXCLK minimum hi time to be less than 40ns.

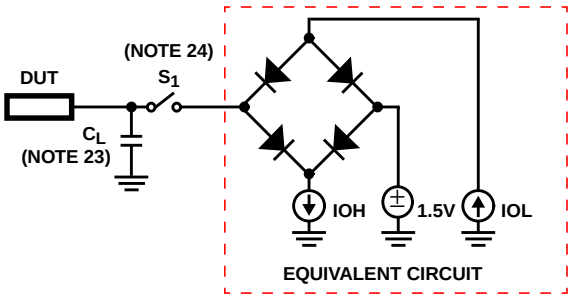
I and Q A/D AC Electrical Specifications (Note 9)

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0	V
Input Bandwidth (-0.5dB)	-	20	-	MHz
Input Capacitance	-	5	-	pF
Input Impedance (DC)	5	-	-	kΩ
FS (Sampling Frequency)	-	-	22	MHz

RSSI A/D Electrical Specifications (Note 9)

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	-	-	1.15	V
Input Bandwidth (0.5dB)	1MHz	-	-	MHz
Input Capacitance (DC)	-	7pF	-	pF
Input Impedance	1M	-	-	MΩ

Test Circuit



NOTES:

23. Includes Stray and JIG Capacitance.

24. Switch S1 Open for I_{CCSB} and I_{CCOP}.

FIGURE 20. TEST LOAD CIRCUIT

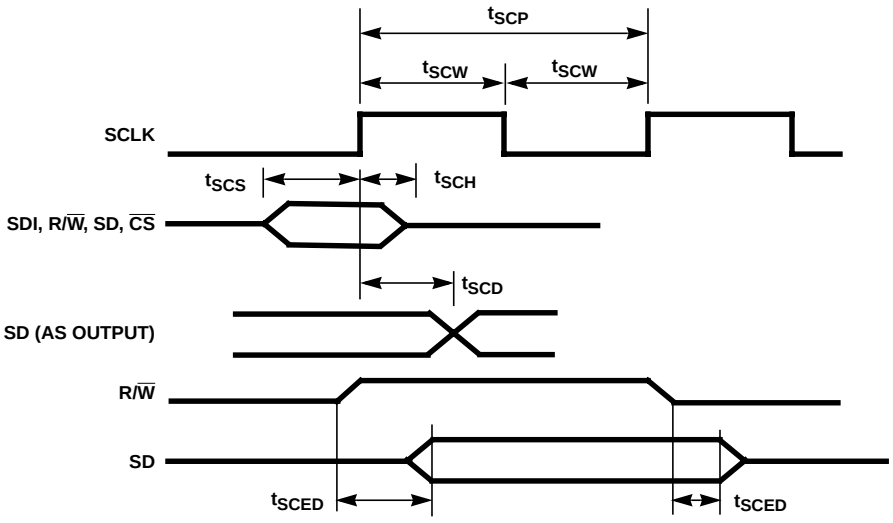


FIGURE 21. SERIAL CONTROL PORT SIGNAL TIMING

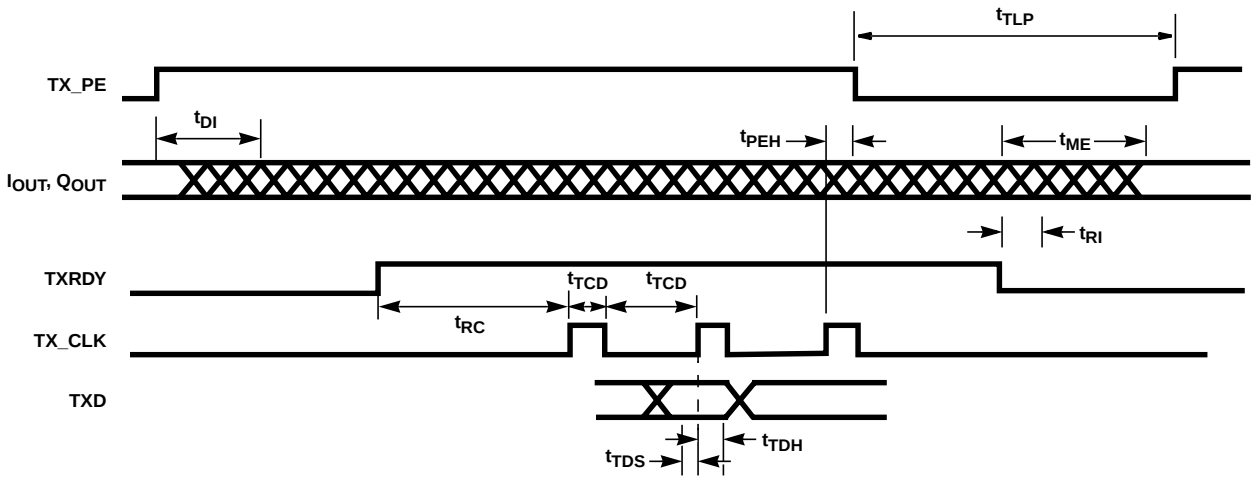
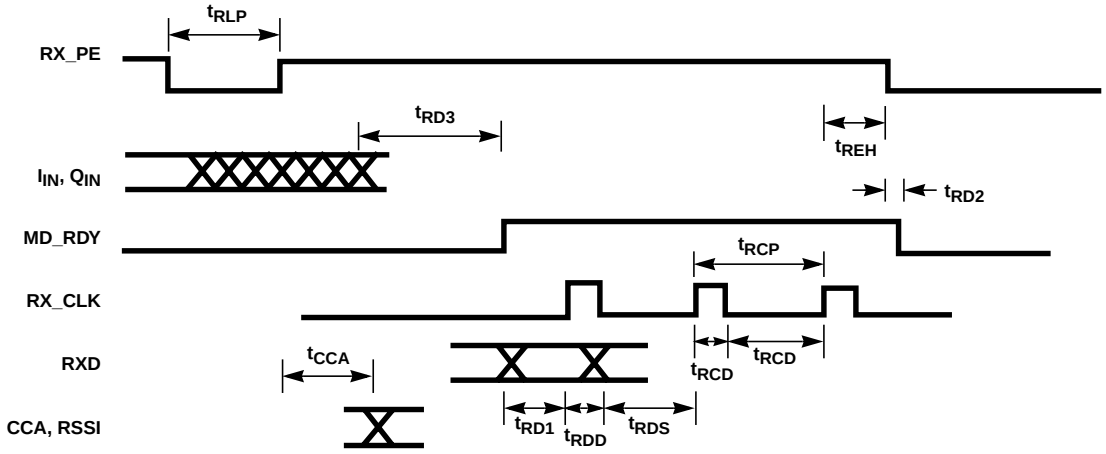


FIGURE 22. TX PORT SIGNAL TIMING



NOTE: RXD, MD_RDY is output two MCLK after RXCLK rising to provide hold time. RSSI Output on TEST (5:0).

FIGURE 23. RX PORT SIGNAL TIMING

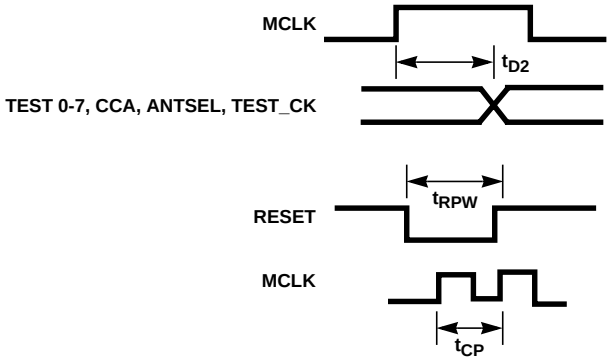


FIGURE 24. MISCELLANEOUS SIGNAL TIMING

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

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