PRELIMINARY | Data Sheet | May 1999 | File Number 4745

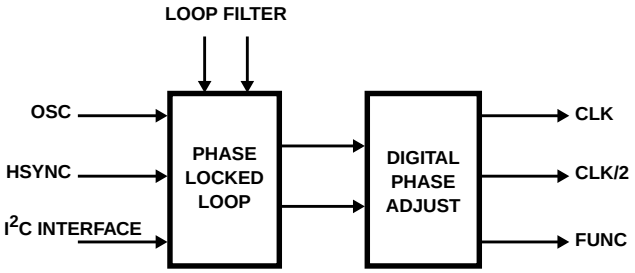
High Performance Programmable Phase-Locked Loop for LCD Applications

The HI5634 is a low cost but very high-performance frequency generator for line-locked and genlocked high resolution video applications. Utilizing an advanced low voltage CMOS mixed signal technology, the HI5634 is an effective clock solution for video projectors and displays at resolutions from VGA to beyond UXGA

The HI5634 offers pixel clock outputs in both differential (to 250MHz) and single-ended (to 150MHz) formats. Digital phase adjustment circuitry allows user control of the pixel clock phase relative to the recovered sync signal. A second differential output at half the pixel clock rate enables deMUXing of multiplexed A/D converters. The FUNC pin provides either the regenerated input from the phase-locked loop (PLL) divider chain output or a re-synchronized and sharpened input HSYNC.

The advanced PLL utilizes either its internal programmable feedback divider or an external divider. The device is programmed by a standard I^2C-bus® serial interface.

Simplified Block Diagram



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5634CB	0 to 70	24 Ld SOIC	M24.3

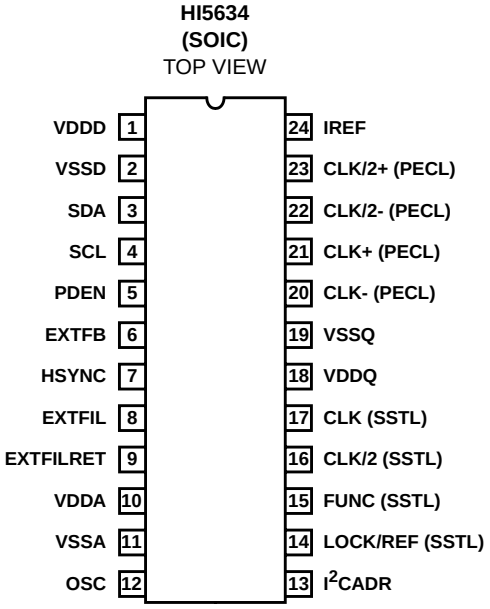
Features

- Pixel Clock Frequencies up to 250MHz
- Very Low Jitter
- Digital Phase Adjustment (DPA) for Clock Outputs
- Balanced PECL Differential Outputs
- Single-Ended SSTL_3 Clock Outputs
- Double-Buffered PLL/DPA Control Registers
- Independent Software Reset for PLL/DPA
- External or Internal Loop Filter Selection
- Uses 3.3V Supply. Inputs are 5V Tolerant.
- I^2C-bus Serial Interface can Run at Either Low Speed (100kHz) or High Speed (400kHz)
- Lock Detection

Applications

- LCD Monitors and Video Projectors
- Genlocking Multiple Video Subsystems
- Frequency Synthesis

Pinout



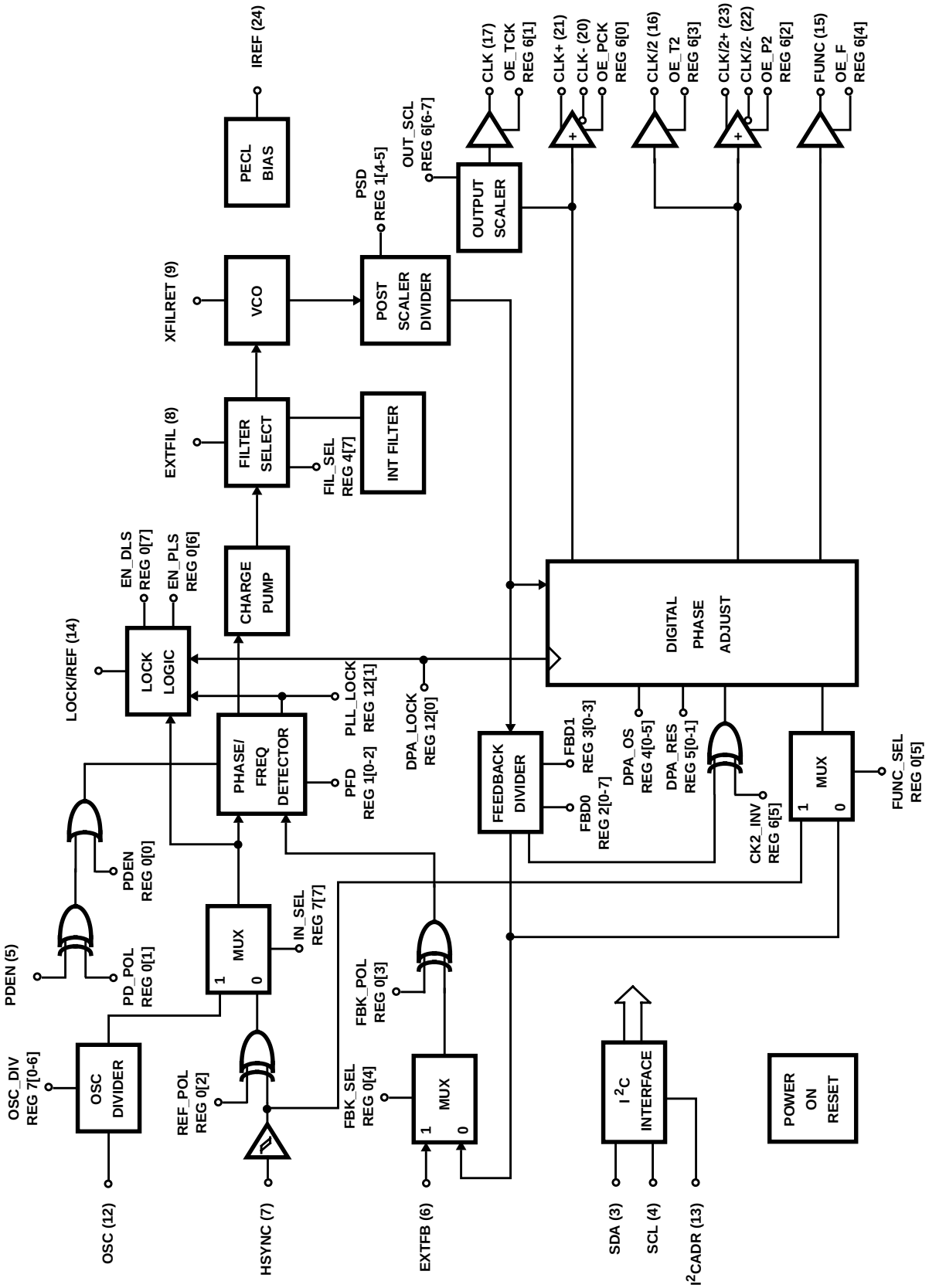
Pin Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION	COMMENTS
1	VDDD	PWR	Digital Supply	3.3V to Digital Sections
2	VSSD	PWR	Digital Ground	
3	SDA	IN/OUT	Serial Data	I^2C-Bus (Note 1)
4	SCL	IN	Serial Clock	I^2C-Bus (Note 1)
5	PDEN	IN	PFD Enable	Suspends Charge Pump (Note1)
6	EXTFB	IN	External Feedback In	External Divider Input to PFD (Note1)
7	HSYNC	IN	Horizontal Sync	Clock Input to PLL (Note1)
8	EXTFIL	IN	External Filter	External PLL Loop Filter
9	EXTFILRET	IN	External Filter Return	External PLL Loop Filter Return
10	VDDA	PWR	Analog Supply	3.3V for Analog Circuitry
11	VSSA	PWR	Analog Ground	Ground for Analog Circuitry
12	OSC	IN	Oscillator	Input From Crystal Oscillator Package (Notes 1, 2)
13	I^2CADR	IN	I^2C Address	Chip I^2C Address Select Low = 4Dh Read, 4Ch Write High = 4Fh Read, 4Eh Write
14	LOCK/REF (SSTL)	OUT	Lock Indicator/Reference	Displays PLL or DPA Lock or REF Input
15	FUNC (SSTL)	OUT	Function Output	SSTL_3 Selectable HSYNC Output
16	CLK/2 (SSTL)	OUT	Pixel Clock/2 Out	SSTL_3 Driver to ADC DeMUX Input
17	CLK (SSTL)	OUT	Pixel Clock Out	SSTL_3 Driver to ADC
18	VDDQ	PWR	Output Driver Supply	3.3V to Output Drivers
19	VSSQ	PWR	Output Driver Ground	Ground for Output Drivers
20	CLK- (PECL)	OUT	Pixel Clock Out	Inverted PECL Driver to ADC. Open Drain Output.
21	CLK+ (PECL)	OUT	Pixel Clock Out	PECL Driver to ADC. Open Drain Output.
22	CLK/2- (PECL)	OUT	Pixel Clock/2 Out	Inverted PECL Driver to ADC DeMUX Input. Open Drain Output.
23	CLK/2+ (PECL)	OUT	Pixel Clock/2 Out	PECL Driver to ADC DeMUX Input. Open Drain Output.
24	IREF	IN	Reference Current	Reference Current for PECL Outputs

NOTES:

1. These LVTTL inputs are 5V tolerant.
2. Connect to ground if unused.

Block Diagram



Absolute Maximum Ratings

VDDA, VDDD, VDDQ (Measured to VSS) 4.3V
Digital Inputs . . . . . VSSD -0.3V to +5.5V
Analog Outputs . . . . . VSSA -0.3V to VDDA +0.3V
Digital Pouts . . . . . VSSQ -0.3V to VDDQ +0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . >2kV

Operating Conditions

Temperature Range . . . . . 0^oC to 70^oC
Voltage Range (VDDA, VDDD, VDDQ to VSS) . . . . . 3.0V to 3.6V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} ($^oC/W$)
SOIC Package 80
Maximum Junction Temperature (Plastic Package) . . . . . .150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 260^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Per Operating Conditions Listed Above, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY CURRENT						
Supply Current, Digital	IDDD	VDDD = 3.6V	-	-	25	mA
Supply Current, Output Drivers	IDDQ	VDDQ = 3.6V, No Output Drivers Enabled	-	-	6	mA
Supply Current, Analog	IDDA	VDDA = 3.6V	-	-	5	mA
DIGITAL INPUTS (SDA, SCL, PDEN, EXTFB, HSYNC, OSC, I^2CADR)						
Input High Voltage	V_{IH}		2	-	5.5	V
Input Low Voltage	V_{IL}		VSS-0.3	-	0.8	V
Input Hysteresis			0.2	-	0.6	V
Input High Current	I_{IH}	V_{IH} = VDD	-	-	±10	µA
Input Low Current	I_{IL}	V_{IL} = 0	-	-	±200	µA
Input Capacitance	C_{IN}		-	-	10	pF
SDA (IN OUTPUT MODE: SDA IS BIDIRECTIONAL)						
Output Low Voltage	V_{OL}	I_{OUT} = 3mA. V_{OH} = 6.0V Maximum, as Determined by the External Pull-up Resistor.	-	-	0.4	V
PECL OUTPUTS (CLK+, CLK-, CLK/2+, CLK/2-)						
Output High Voltage	V_{OH}	I_{OUT} = 0	-	-	VDD	V
Output Low Voltage (Note 4)	V_{OL}	I_{OUT} = Programmed Value	1.0	-	-	V
SSTL_3 OUTPUTS (CLK, CLK/2, FUNC, LOCK/REF)						
Output Resistance	R_O	$1 < V_O < 2V$	-	-	80	Ω
AC INPUT CHARACTERISTICS						
HSYNC Input Frequency	f_{HSYNC}	Reg 7[7] = 0	0.008	-	10	MHz
OSC Input Frequency	f_{OSC}	Reg 7[7] = 1	0.02	-	100	MHz
TIMING CHARACTERISTICS (Note 5)						
REF Output Transition Times	t_r	Rise Time/Fall Time	-	2.8/1.8	-	ns
PECL CLK Output Transition Times	t_P	Rise Time/Fall Time	-	1.0/1.2	-	ns
SSTL CLK Output Transition Times	t_S	Rise Time/Fall Time	-	1.6/0.7	-	ns
FUNC Output Transition Times	t_F	Rise Time/Fall Time	-	1.2/1.0	-	ns
HSYNC to REF Delay	t_0		11.3	11.5	12	ns
REF to PECL Clock Delay	t_1		-1.0	0.8	2.2	ns

Electrical Specifications Per Operating Conditions Listed Above, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PECL Clock Duty Cycle	t_2, t_3		45	50	55	%
PECL Clock to SSTL Clock Delay	t_4		0.2	0.75	1.2	ns
PECL Clock to FUNC Delay	t_5		1.5	1.9	2.3	ns
PECL Clock to PECL Clock/2 Delay	t_6		1.0	1.3	1.5	ns
PECL Clock to SSTL Clock/2 Delay	t_7		1.1	1.4	1.8	ns
SSTL Clock Duty Cycle	t_8, t_9		45	50	55	%

NOTES:

4. V_{OL} must not fall below the minimum specified level or the I_{OUT} value may not be maintained.
5. Measured at 3.6V 0^oC, 135MHz output frequency, PECL Clock lines to 75Ω termination, SSTL Clock lines unterminated, 20pF load. Transition times vary based on termination. See the “Output Timing Diagram” for details.

Application Information

Overview

The HI5634 addresses stringent graphics system line locked and genlocked applications and provides the clock signals required by high-performance video A/D converters. Included are a phase locked loop (PLL) with a 500MHz voltage controlled oscillator (VCO), a digital phase adjustment to provide a user programmed pixel clock delay, the means for deMUXing multiplexed A/D Converters, and both balanced programmable (PECL) and single-ended (SSTL_3) high-speed clock outputs.

Phase-Locked Loop

The phase-locked loop is optimized for line-locked applications, for which the inputs are horizontal sync signals. A high-performance Schmitt trigger preconditions the HSYNC input, whose pulses can be degraded if they are from a remote source. This preconditioned HSYNC signal is provided as a clean reference signal with a short transition time (in contrast, the signal that a typical PC graphics card provides has a transition time of tens of nanoseconds).

A second high frequency input such as a crystal oscillator and a 7-bit programmable divider can be selected. This selection allows the loop to operate from a local source and is also useful for evaluating intrinsic jitter.

A 12-bit programmable feedback divider completes the loop. Designers can substitute an external divider.

Either the conditioned HSYNC input or the loop output (recovered HSYNC) is available at the FUNC pin, aligned to the edge of the pixel clock.

Automatic Power-On-Reset Detection

The HI5634 has automatic power-on-reset detection circuitry and it resets itself if the supply voltage drops below threshold values. No external connection to a reset signal is required.

Digital Phase Adjustment

The digital phase adjustment allows addition of a programmable delay to the pixel clock output, relative to the recovered HSYNC signal. The ability to add delays is particularly useful when multiple video sources must be synchronized. A delay of up to one pixel clock period is selectable in the following increments:

1/64 period for pixel clock rates to 40MHz
1/32 period for pixel clock rates to 80MHz
1/16 period for pixel clock rates to 160MHz

Output Drivers and Logic Inputs

The HI5634 utilizes low voltage TTL (LVTTL) inputs as well as SSTL_3 (EIA/JESD8-8) and low voltage PECL (pseudo-ECL) outputs, operating at 3.3V supply voltage. The LVTTL inputs are 5V tolerant. The SSTL_3 and differential PECL output drivers drive resistive terminations or transmission lines. At lower clock frequencies, the SSTL_3 outputs can be operated unterminated.

I^2C-bus Serial Interface

The HI5634 utilizes the industry standard I^2C-bus serial interface. The interface uses 12 registers: one write-only, eight read/write, and three read-only. Two HI5634 devices can be addressed, according to the state of the I^2 CADR pin. When the pin is low, the read address is 4Dh, and the write address is 4Ch. When the pin is high, the read address is 4Fh, and the write address is 4Eh. The I^2C-bus serial interface can run at either low speed (100kHz) or high speed (400kHz) and provides 5V tolerant input.

PC Board Layout

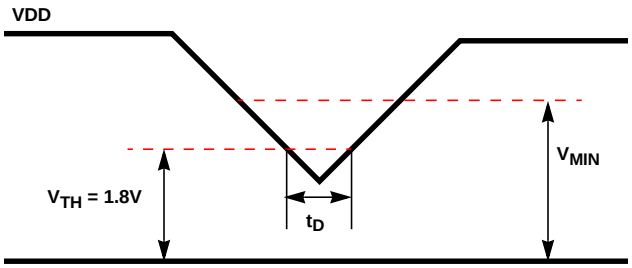
Use a PC board with at least four layers: one power, one ground, and two signal. No special cutouts are required for power and ground planes. All supply voltages must be supplied from a common source and must ramp up together. Flux and other board surface debris can degrade the performance of the external loop filter. Ensure that the HI5634 area of the board is free of contaminants.

Specific Layout Guidelines

1. **Digital Supply (VDDD)** - Bypass pin 1 (VDDD) to pin 2 (VSSD) with 4.7µF and 0.1µF capacitors, located as close as possible to the pins. Traces must be maximally wide and include multiple surface-etched vias to the appropriate plane.
2. **External Loop Filter** - **The use of an external loop filter is strongly recommended in all designs.** Locate loop filter components as close to pins 8 and 9 (EXTFIL and EXTFILRET) as possible. Typical loop filter values are 6.8kΩ for the series resistor, 3300pF RF-type capacitor for the series capacitor, and 150pF for the shunt capacitor.
3. **Analog PLL Supply (VDDA)** - Decouple pin 10 (VDDA) with a series ferrite bead. Bypass the supply end of the bead with 4.7µF and 0.1µF capacitors. Bypass pin 10 to pin 11 (VSSA) with a 0.1µF capacitor. Locate these components as close as possible to the pins. Traces must be maximally wide and have multiple surface-etched vias to the power or ground planes.
4. **PECL Current Set Resistor** - Locate PECL current set resistor as close as possible to pin 24 (IREF). Bypass pin 24 to ground with a 0.1µF capacitor.
5. **PECL Outputs** - Implement these outputs as microstrip transmission lines. The trace widths shown are for 75Ω characteristic impedance, presuming 0.067 in. between layers. Locate the optional series “snubbing” resistors as close as possible to the pins. If the termination resistors are included on-board, locate them as close as possible to the load and connect directly to the power and ground planes (these termination resistors are omitted if the load device implements them internally).
6. **Output Driver Supply (VDDQ)** - Bypass pin 18 (VDDQ) to pin 19 (VSSQ) with 4.7µF and 0.1µF capacitors, located as close as possible to the pins. Traces must be maximally wide and include multiple surface-etched vias to the appropriate plane.
7. **SSTL_3 Outputs** - SSTL_3 outputs can be used like conventional CMOS rail-to-rail logic or as a terminated transmission line system at higher-output frequencies. With terminated outputs, the considerations of item 5, “PECL Outputs” apply. See JEDEC documents JESD8-A and JESD8-8.

Power Supply Considerations

The HI5634 incorporates special internal power-on-reset circuitry that requires no external reset signal connection. The supply voltage (VDD) must remain within the recommended operating conditions during normal operation. To reset the HI5634, the supply voltage at the part must be reduced below the threshold voltage (V_{TH}) of the power-on-reset circuit. The supply voltage must remain below that threshold voltage such that board power conditioning capacitors are drained and the proper reset state is latched. The amount of time (t_D) to hold the voltage in a reset state varies with the design. However, a typical value of 10ms should be sufficient.



SSTL_3 Outputs

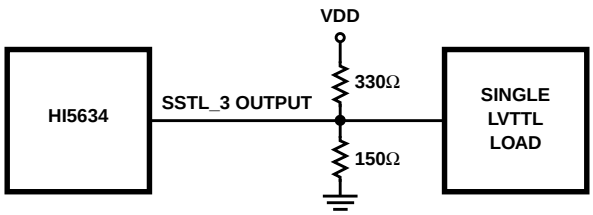
Unterminated Outputs

In the HI5634, unterminated SSTL output pins display exponential transitions similar to those of rectangular pulses presented to RC loads. The 10-90% rise time is typically 1.6ns, and the corresponding fall time is typically 700ps. In turn, this asymmetry contributes to duty cycle asymmetry at higher output frequencies. In the absence of significant load capacitance (which can further increase rise and fall time), this asymmetry is the dominant factor determining high frequency performance of these single-ended outputs. Typically, no termination is required for the LOCK/REF, FUNC, and CLK/2 outputs nor for CLK outputs up to approximately 135MHz.

Terminated Outputs

SSTL_3 outputs are intended to terminate in low impedances to reduce the effect of external circuit capacitance. Use of transmission line techniques enables use of longer traces between source and driver without increasing ringing due to reflections. Where external capacitance is minimal and substantial voltage swing is required to meet LVTTL V_{IH} and V_{IL} requirements, the intrinsic rise and fall times of HI5634 SSTL outputs are only slightly improved by termination in a low impedance.

The HI5634 SSTL output source impedance is typically less than 60Ω. Termination impedance of 100Ω reduces output swing by less than 30% which is more than enough to drive a single load of LVTTL inputs.

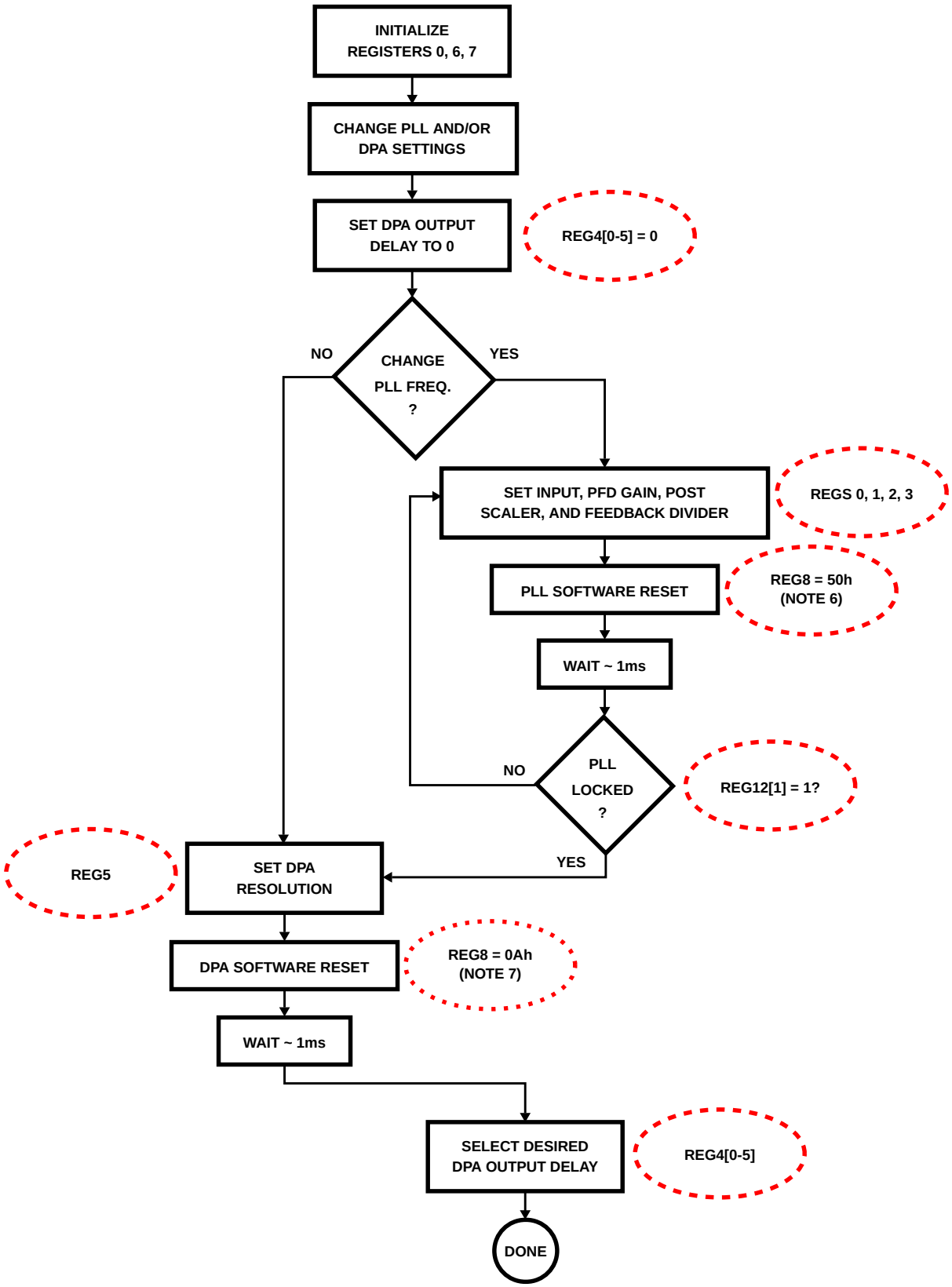


I²C Register Map Summary

REGISTER NUMBER	NAME	ACCESS	BIT NAME	BIT #	RESET VALUE	DESCRIPTION
0h	Input Control	R / W	PDEN	0	1	Phase Detector Enable (0 = External Enable, 1 = Always Enabled)
			PD_POL	1	0	Phase Detector Enable Polarity (0 = Not Inverted, 1 = Inverted)
			REF_POL	2	0	External Reference Polarity (0 = Positive Edge, 1 = Negative Edge)
			FBK_POL	3	0	External Feedback Polarity (0 = Positive Edge, 1 = Negative Edge)
			FBK_SEL	4	0	External Feedback Select (0 = Internal Feedback, 1 = External)
			FUNC_SEL	5	0	Function Out Select (0 = Recovered HSYNC, 1 = Input HSYNC)
			EN_PLS	6	1	Enable PLL Lock/Ref Status Output (0 = Disable, 1 = Enable)
			EN_DLS	7	0	Enable DPA Lock/Ref Status Output (0 = Disable, 1 = Enable)
1h	Loop Control	R / W †	PFD0-2	0-2	0	Phase Detector Gain
			Reserved	3	0	Reserved
			PSD0-1	4-5	0	Post Scaler Divider (0 = ÷2, 1 = ÷4, 2 = ÷8, 3 = ÷16)
			Reserved	6-7	0	Reserved
2h	FDBK Div 0	R / W †	FDB0-7	0-7	FF	PLL Feedback Divider LSBs (Bits 0-7)
3h	FDBK Div 1	R / W †	FDB8-11	0-3	F	PLL Feedback Divider MSBs (Bits 8-11)
			Reserved	4-7	0	Reserved
4h	DPA Offset	R / W	DPA_OS0-5	0-5	0	Digital Phase Adjustment Offset
			Reserved	6	0	Reserved
			FIL_SEL	7	0	Loop Filter Select (0 = External, 1 = Internal)
5h	DPA Control	R / W ††	DPA_RES0-1	0-1	3	DPA Resolution (0 = 16 Delay Elements, 1 = 32, 2 = Reserved, 3 = 64)
			METAL_REV	2-7	0	Metal Mask Revision Number
6h	Output Enables	R / W	OE_PCK	0	0	Output Enable for PECL PCLK Outputs (0 = High Z, 1 = Enabled)
			OE_TCK	1	0	Output Enable for STTL_3 CLK Output (0 = High Z, 1 = Enabled)
			OE_P2	2	0	Output Enable for PECL CLK/2 Outputs (0 = High Z, 1 = Enabled)
			OE_T2	3	0	Output Enable for STTL_3 CLK/2 Output (0 = High Z, 1 = Enabled)
			OE_F	4	0	Output Enable for STTL_3 FUNC Output (0 = High Z, 1 = Enabled)
			CK2_INV	5	0	CLK/2 Invert (0 = Not Inverted, 1 = Inverted)
			OUT_SCL	6-7	0	SSTL Clock Scaler (0 = ÷1, 1 = ÷2, 2 = ÷4, 3 = ÷8)
7h	OSC_DIV	R / W	OSC_DIV 0-6	0-6	0	Osc Divider Modulus
			IN_SEL	7	1	Input Select (0 = HSYNC Input, 1 = Osc Divider)
8h	Reset	Write	DPA	0-3	x	Writing xAh Resets DPA and Loads Working Register 5
			PLL	4-7	x	Writing 5xh Resets PLL and Loads Working Registers 1-3
10h	Chip Ver	Read	CHIP VER	0-7	17	Chip Version 23 Decimal (17 Hex)
11h	Chip Rev	Read	CHIP REV	0-7	01	Initial Value 01h. Value Increments With Each All Layer Change.
12h	RD_REG	Read	DPA_LOCK	0	N/A	DPA Lock Status (0 = Unlocked, 1 = Locked)
			PLL_LOCK	1	N/A	PLL Lock Status (0 = Unlocked, 1 = Locked)
			Reserved	2-7	0	Reserved

† Identifies Double Buffered Registers. Working Registers are Loaded During Software PLL Reset.
†† Identifies Double Buffered Registers. Working Registers are Loaded During Software DPA Reset.

Software Programming Flow



NOTES:

6. Updates working Registers 1-3.
7. Updates working Resister 5.

Detailed Register Description

Register: 0h **Name: Input Control** **Access: Read/Write**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
PDEN	0	1	Phase/Frequency Detector Enable - 0 = External Enable (Phase/Frequency Detector controlled by PDEN (pin 5) only), 1 = Always Enabled (default).
PD_POL	1	0	Phase/Frequency Detector Enable Polarity - Used only when (Reg0 [0]=0). 0 = Not inverted (default, PDEN input (pin 5) is active high),1 = Inverted (PDEN input (pin 5) is active low).
REF_POL	2	0	Phase/Frequency Detector External Reference Polarity - Edge of input signal on which Phase Detector triggers. 0 = Rising Edge (default), 1 = Falling Edge.
FBK_POL	3	0	External Feedback Polarity - Edge of EXTFB (pin 6) signal on which Phase/Frequency Detector triggers when external feedback is used (Reg0 [4]=1). 0 = Positive Edge (default), 1 = Negative Edge.
FBK_SEL	4	0	External Feedback Select - 0 = Internal Feedback (default), 1 = External Feedback.
FUNC_SEL	5	0	Function Output Select - Selects re-clocked output to FUNC (pin 15). 0 = Recovered HSYNC (default, regenerated HSYNC output), 1 = External HSYNC (Schmitt-trigger conditioned input from HSYNC (pin 7)).

				EN_PLS	EN_DLS	IN_SEL	LOCK/REF (14)
EN_PLS	6	1	Outputs PLL Lock Status (Reg12[1]) on LOCK/REF pin.	0	0	N/A	0
EN_DLS	7	0	Outputs DPA Lock Status (Reg12[0]) on LOCK/REF pin. Bits 6, 7 enable multiple functions at LOCK/REF output (pin 14), as shown in table at right.	0	1	N/A	1 if DPA Locked, 0 Otherwise
				1	0	N/A	1 if PLL Locked, 0 Otherwise
				1	1	0	Post Schmitt Trigger HSYNC(7) XOR REF_POL
				1	1	1	$F_{OSC} \div$ OSC_DIV

Register: 1h **Name: Loop Control Register** **Access: Read/Write** **(Note 8)**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
PFD0-2	0-2	0	Phase/Frequency Detector Gain.
Reserved	3	0	Reserved
PSD0-1	4-5	0	Post-Scaler Divider - Divides the output of the VCO prior to the DPA and Feedback Divider.
Reserved	6-7	0	Reserved

BIT 2	BIT 1	BIT 0	PFD GAIN (μA/2π RAD)
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

BIT 5	BIT 4	PSD DIVIDER
0	0	2 (Default)
0	1	4
1	0	8
1	1	16

Register: 2h, 3h Name: Feedback Divider Registers Access: Read/Write (Note 8, 9)

REG #	BIT NAME	BIT #	RESET VALUE	DESCRIPTION
2h	FBD0-7	0-7	FF	PLL Feedback Divider LSBs (0-7). When Bit 0 = 0, the total number of pixels is even. When Bit 0 = 1, the total number of pixels is odd.
3h	FBD8-11	0-3	F	PLL Feedback Divider MSBs (8-11).
3h	Reserved	4-7		Reserved

Feedback Divider Modulus =

REG 3				REG 2								
3	2	1	0	7	6	5	4	3	2	1	0	
												+8

12 ≤ Feedback Divider Modulus ≤ 4103

Register: 4h Name: DPA Offset Register Access: Read/Write

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
DPA_OS0-5	0-5	0	Digital Phase Adjustment Offset - Selects clock edge offset in discrete steps from zero to one clock period minus one step. Resolution (number of delay elements per clock cycle) is selected by DPA_RES0-1 (Reg 5[0-1]). Note: Offsets equal to or greater than one clock period are neither recommended nor supported. Example: For DPA_RES0-1=01h, the clock can be delayed from 0 to 31 steps.
Reserved	6	0	Reserved
FIL_SEL	7	0	Selects external loop filter (0) or internal loop filter (1). The use of an external loop filter is strongly recommended for all designs.

Register: 5h Name: DPA Control Register Access: Read/Write (Note 10)

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
DPA_RES0-1	0-1	3	Digital Phase Adjustment (DPA) Resolution Select. Use of the DPA above 160MHz is not recommended.
METAL_REV	2-7	0	Metal Mask Revision Number - After power-up, register bits 2-7 must be written with 111111. After this write, a read indicates the metal mask revision, as shown in the table at right.

BIT 1	BIT 0	DELAY ELEMENTS	CLK RANGE (MHz)
0	0	16	48 ▬ 160
0	1	32	24 ▬ 80
1	0	Reserved	
1	1	64	12 ▬ 40

REVISION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2
A	1	1	1	1	1	1
B	0	1	1	1	1	1
C1	1	0	1	1	1	1
C2	0	0	1	1	1	1
D	1	1	0	1	1	1
E	1	1	1	0	1	1
F	1	1	1	1	0	1
G	1	1	1	1	1	0

NOTES:

8. Double buffered registers. Actual working registers are loaded during software PLL reset. See Register 8h for details.
9. The value that is programmed into these two registers, plus a value of 8, defines the total number of clock periods that the HI5634 generates between HSYNCs. Program these registers with the total number of horizontal pixels per line minus 8.
10. Double buffered register. Actual working registers are loaded during software DPA reset. See Register 8h for details.

Register: 6h **Name: Output Enable Register** **Access: Read/Write**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
OE_PCK	0	0	Output Enable for CLK Outputs (PECL) - 0 = High Z (default), 1 = Enabled.
OE_TCK	1	0	Output Enable for CLK Output (SSTL_3) - 0 = High Z (default), 1 = Enabled.
OE_P2	2	0	Output Enable for CLK/2 Outputs (PECL) - 0 = High Z (default), 1 = Enabled.
OE_T2	3	0	Output Enable for CLK/2 Output (SSTL_3) - 0 = High Z (default), 1 = Enabled.
OE_F	4	0	Output Enable for FUNC Output (SSTL_3) - 0 = High Z (default), 1 = Enabled.
CK2_INV	5	0	CLK/2 Invert - 0 = Not Inverted (default), 1 = Inverted.
OUT_SCL	6-7	0	Clock (CLK) Scaler.

BIT 7	BIT 6	CLK DIVIDER
0	0	1
0	1	2
1	0	4
1	1	8

Register: 7h **Name: Oscillator Divider Register** **Access: Read/Write**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
OSC_DIV0- 6	0-6	0	Oscillator Divider Modulus - Divides the input from OSC (pin 12) by the set modulus. The modulus equals the programmed value, plus 2. Therefore, the modulus range is from 3 to 129.
IN_SEL	7	1	Input Select - Selects the input to the Phase/Frequency Detector 0 = HSYNC, 1 = Osc Divider (default).

Register: 8h **Name: Reset Register** **Access: Write Only**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
DPA Reset	0-3	X	Writing XAh to this register resets DPA working Register 5.
PLL Reset	4-7	X	Writing 5Xh to this register resets PLL working Registers 1-3.

VALUE	RESETS
XA	DPA
5X	PLL
5A	DPA and PLL

Register: 10h **Name: Chip Version Register** **Access: Read Only**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
CHIP VER	0-7	17	Chip Version 23 (17h).

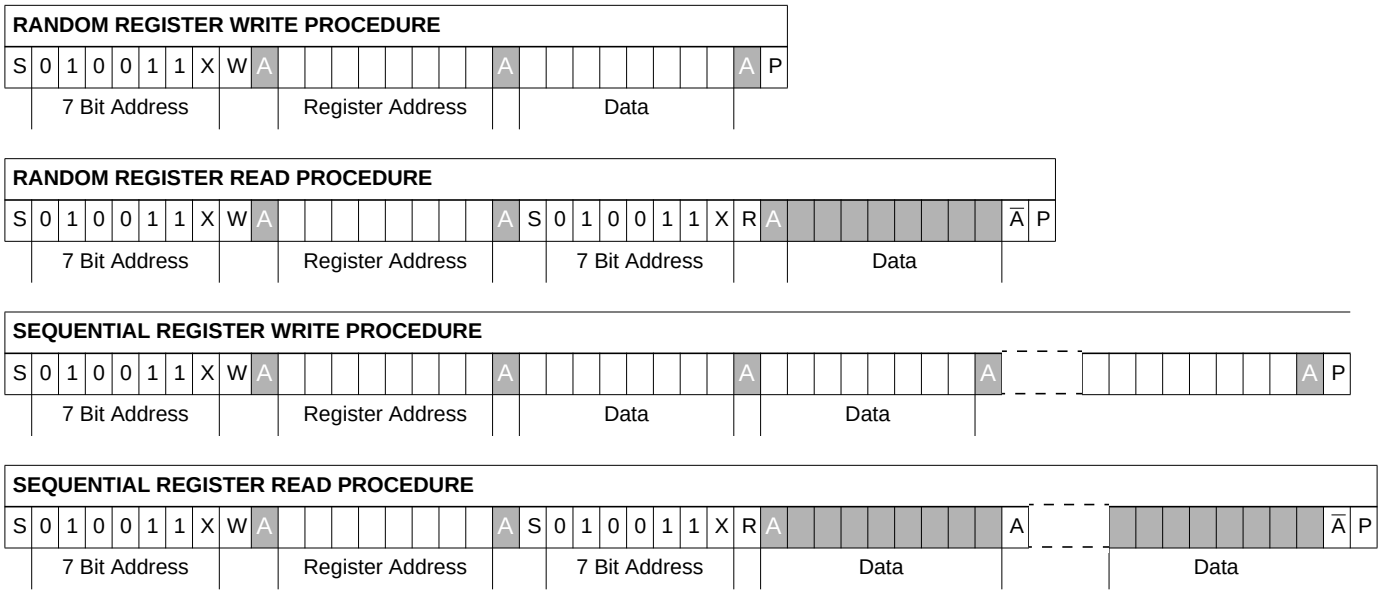
Register: 11h **Name: Chip Revision Register** **Access: Read Only**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
CHIP REV	0-7	01+	Initial value 01h. +Value increments with each all-layer change.

Register: 12h **Name: Status Register** **Access: Read Only**

BIT NAME	BIT #	RESET VALUE	DESCRIPTION
DPA_LOCK	0	N/A	DPA Lock Status (Refer to Register 0h, bits 6 and 7). 0 = Unlocked, 1 = Locked.
PLL_LOCK	1	N/A	PLL Lock Status (Refer to Register 0h, bits 6 and 7). 0 = Unlocked, 1 = Locked.
Reserved	2-7	0	Reserved

I²C Data Format (Notes 11-14)

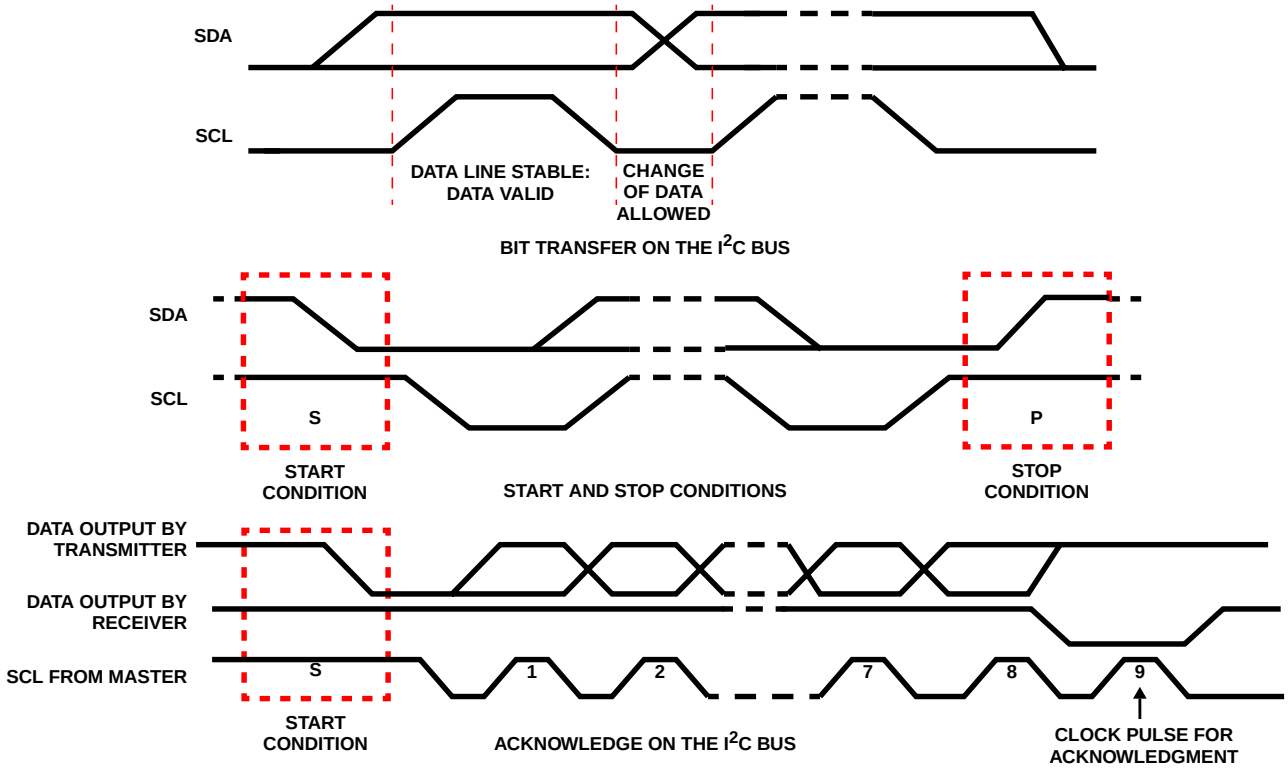


Direction: ☐ = Bus Host to Device ■ = Device to Bus Host

NOTES:

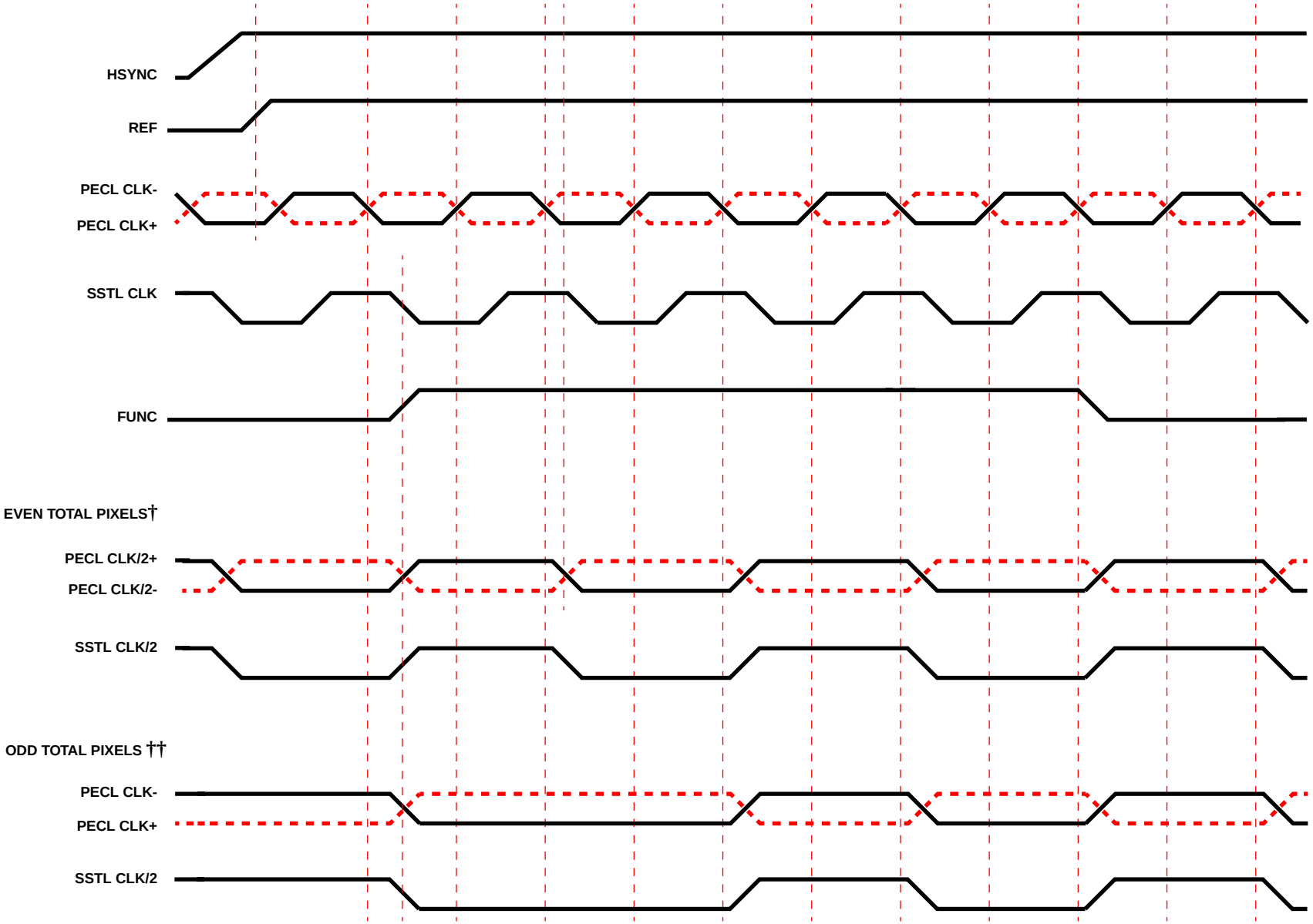
11. All values are transmitted with the most significant bit first and the least significant bit last.
12. The value of the X-bit equals the logic state of pin 13 (I^2CADR).
13. R = Read Command = 1, W = Write Command = 0.
14. S = Start Condition, A = Acknowledge, $\overline{A}$ = No Acknowledge, P = Stop Condition. See "I^2C Data Characteristics" for description.

I²C Data Characteristics



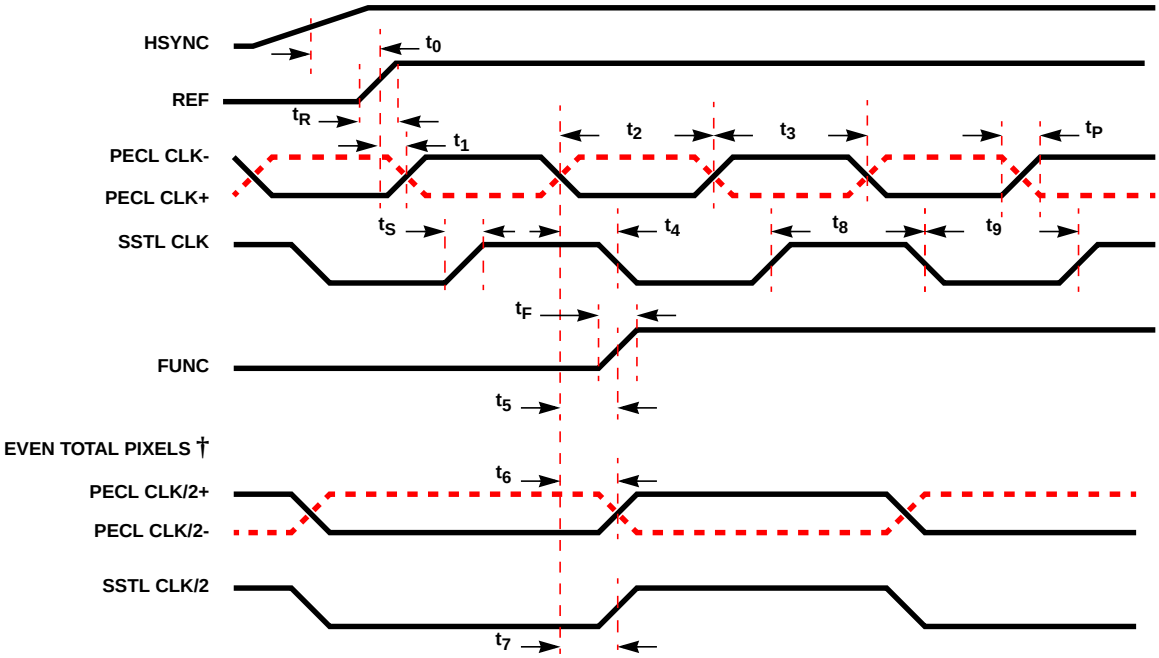
NOTE: These waveforms are from "The I^2C bus and how to use it," published by Philips Semiconductor. The document can be obtained from: http://www-us2.semiconductors.philips.com/acrobat/various/i2c_bus_specification_1995.pdf.

AC Timing Characteristics Overview



† Timing when Register 2[0] = 0 (Total Number of Pixels is Even).
†† Timing when Register 2[0] = 1 (Total Number of Pixels is Odd).

Output Timing Diagram



†Timing when Register 2[0] = 0 (Total Number of Pixels is Even).

Typical Performance Curves

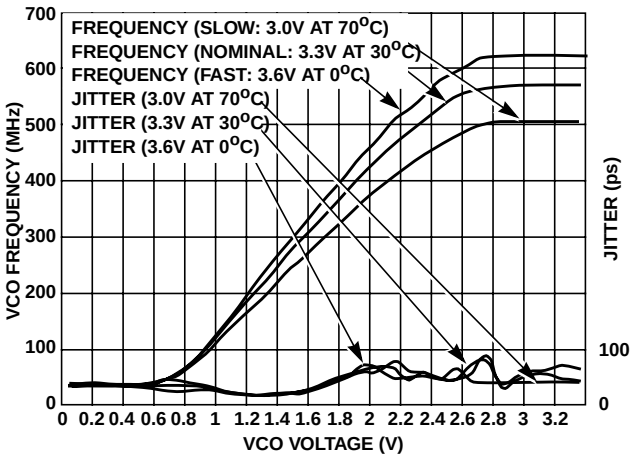


FIGURE 1. VCO FREQUENCY AND JITTER vs VCO VOLTAGE

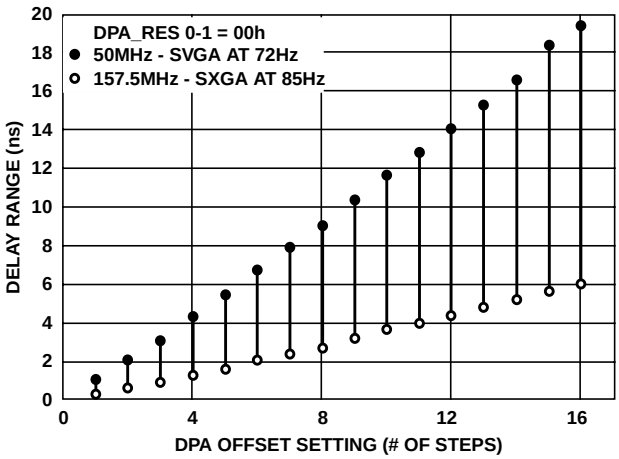


FIGURE 2. DPA DELAY vs OFFSET SETTING (16 ELEMENTS)

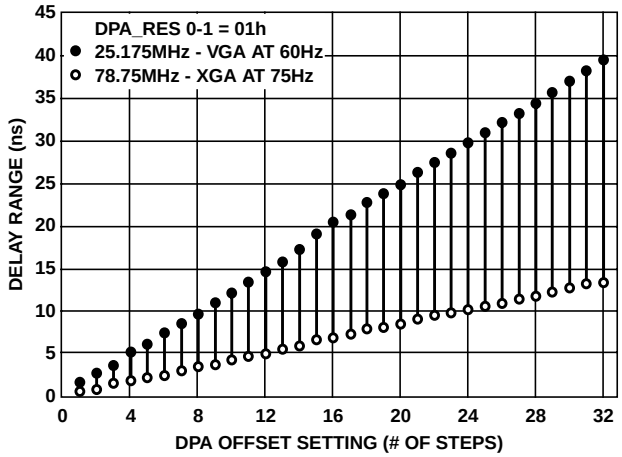


FIGURE 3. DPA DELAY vs OFFSET SETTING (32 ELEMENTS)

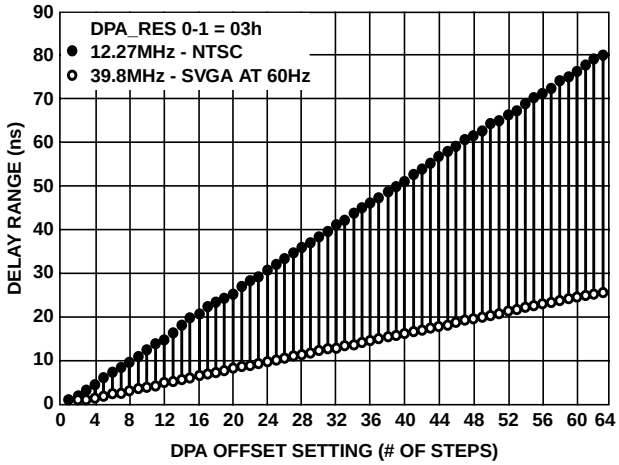
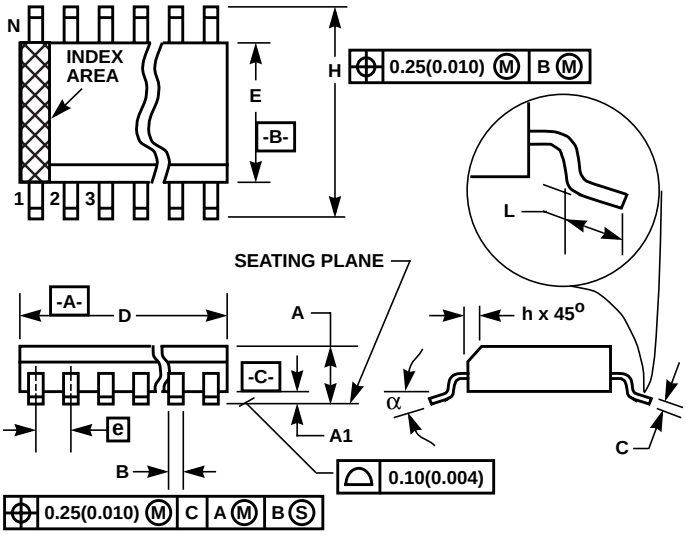


FIGURE 4. DPA DELAY vs OFFSET SETTING (64 ELEMENTS)

Small Outline Plastic Packages (SOIC)



M24.3 **(JEDEC MS-013-AD ISSUE C)**
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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