NOT RECOMMENDED FOR NEW DESIGNS
SEE ISL6414

November 2003 FN9081.2

Triple Output, Low-Noise LDO Regulator with Integrated Reset Circuit

The ISL6411 is an ultra low noise triple output LDO regulator with microprocessor reset circuit and is optimized for powering wireless chip sets. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (LDO1), 2.84V (LDO2), and another ultra clean 2.84V (LDO3). On chip logic provides sequencing between LDO1 and LDO2 for BBP/MAC and I/O supply voltage outputs. LDO3 features ultra low noise that does not typically exceed 30µV RMS to aid VCO stability. High integration and the thin Quad Flat No-lead (QFN) package makes ISL6411 an ideal choice to power many of today's small form factor industry standard wireless cards, such as PCMCIA, mini-PCI and Cardbus-32.

The ISL6411 uses an internal PMOS transistor as the pass device. The SHDN pin controls LDO1 and LDO2 outputs whereas SHDN3 controls LDO3 output. Internal voltage sequencing insures that LDO1 output (1.8V supply) is always stabilized before LDO2 is turned on. When powering down, power to the LDO2 is removed before the LDO1 output goes off. The ISL6411 also integrates RESET function, which eliminates the need for additional RESET IC required in WLAN applications. The IC asserts a RESET signal whenever the VIN supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after Vin has risen above the reset threshold. An output fault detection circuit indicates loss of regulation on any of the three outputs. Other features include an over current protection, thermal shutdown and reverse battery protection.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL6411IR	-40 to +85	16 Ld QFN	L16.4x4
ISL6411IRZ (Note)	-40 to +85	16 Ld QFN	L16.4x4

NOTE: " Z " Suffix: Intersil Lead Free products employ special lead free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and lead free soldering operations. Intersil Lead Free products are MSL classified at lead free peak reflow temperatures that meet or exceed the lead free requirements of IPC/JEDEC J Std-020B. Tape and Reel available. Add "-T" suffix for tape and reel packing option (e.g., ISL6411RZ-T for lead free tape and reel).

Features

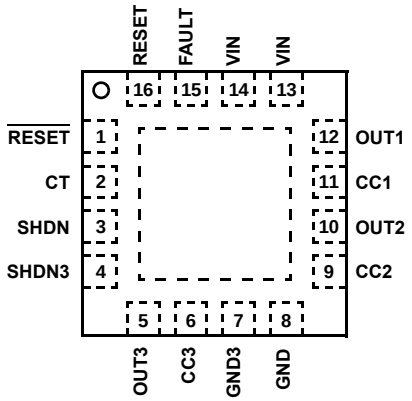
- Small DC-DC Converter Size
  - Three LDOs and RESET Circuitry in a Low-Profile 4x4mm QFN Package
- High Output Current
  - LDO1, 1.8V 500mA
  - LDO2, 2.84V 300mA
  - LDO3, 2.84V 200mA
- Ultra-Low Dropout Voltage
  - LDO2, 2.84V . . . . . 125mV (typ.) at 300mA
  - LDO3, 2.84V . . . . . 100mV (typ.) at 200mA
- Ultra-Low Output Voltage Noise
  - <30µV_{RMS} (typ.) for LDO3 (VCO Supply)
- Stable with Smaller Ceramic Output Capacitors
- Voltage Sequencing for BBP/MAC and Analog Supplies
- Extensive Protection and Monitoring Features
  - Over current protection
  - Short circuit protection
  - Thermal shutdown
  - Reverse battery protection
  - FAULT indicator
- Logic-Controlled Dual Shutdown Pins
- Integrated Microprocessor Reset Circuit
  - Programmable Reset Delay
  - Complimentary Reset Outputs
- Proven Reference Design for Total WLAN System Solution
- QFN Package Option
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint Improves PCB Efficiency and Is Thinner in Profile
  - Lead-Free Package Option Available ("Z" suffix)

Applications

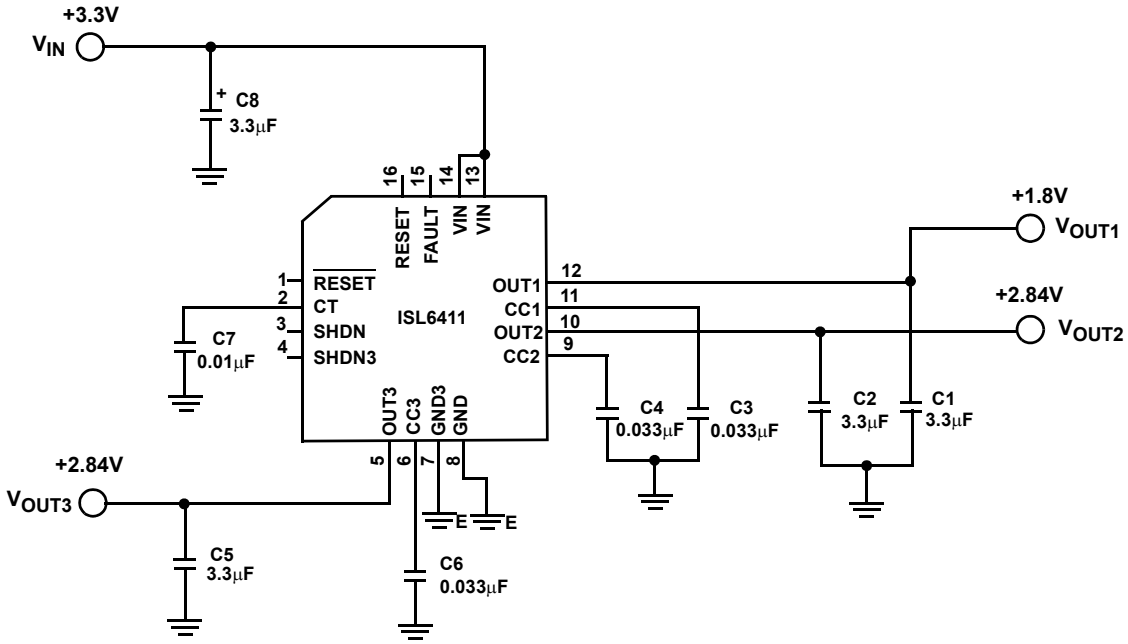
- PRISM® 3, PRISM GT™, and PRISM WWR Chipsets
- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Hand-Held Instruments

Pinout

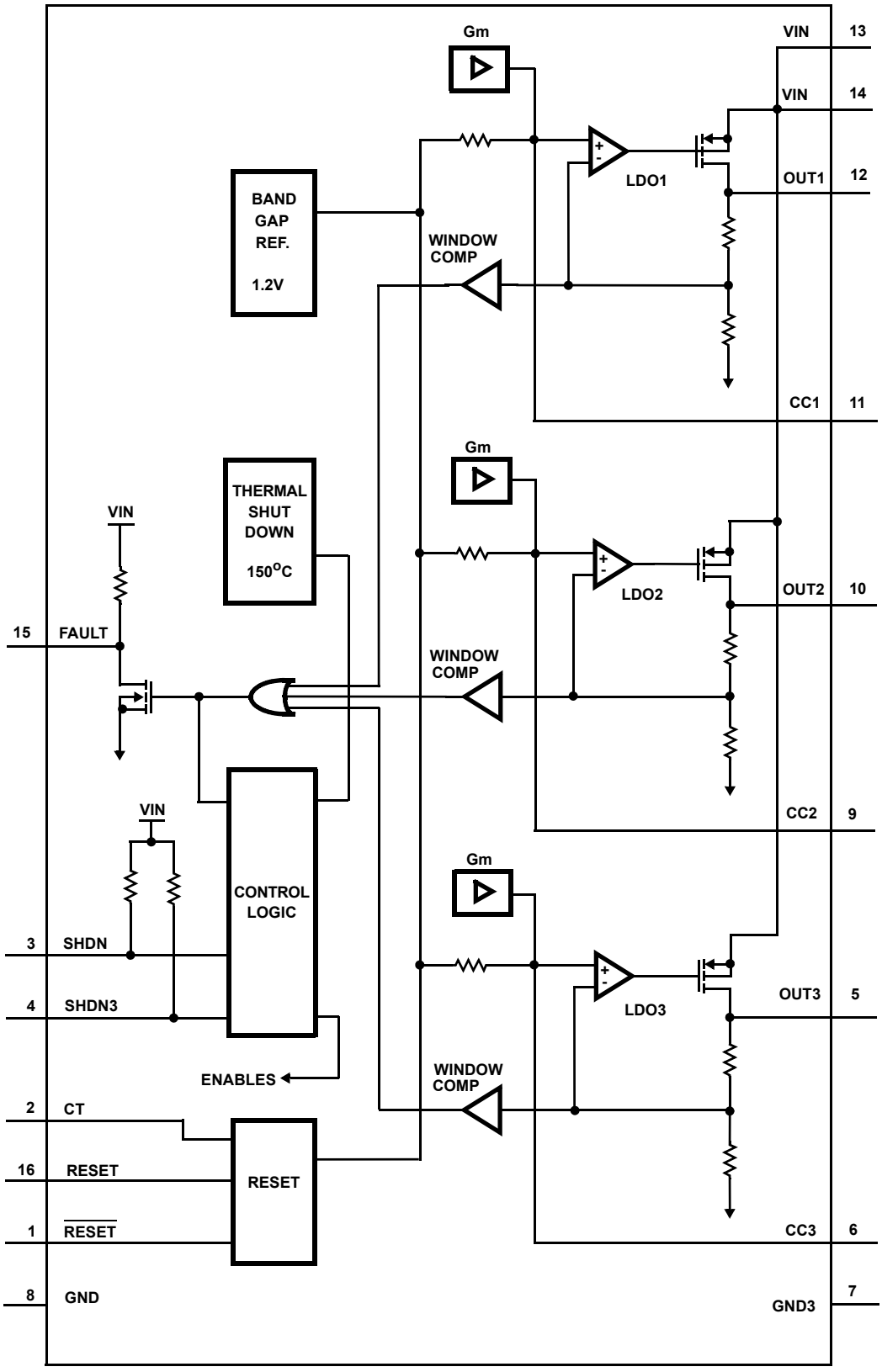
ISL6411 (QFN)
TOP VIEW



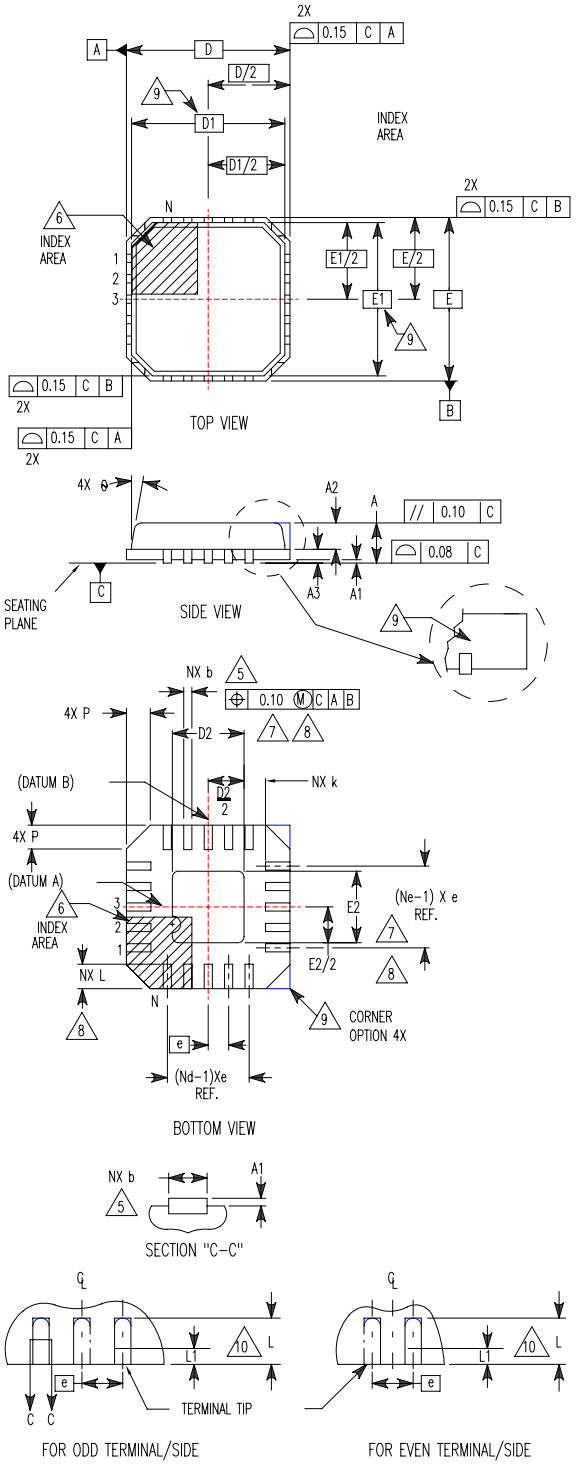
Typical Application Schematic



Functional Block Diagram



Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 4 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.