Data Sheet | December 2003 | FN9077.2

80V/1.25A Peak, Medium Frequency, Low Cost, Half-Bridge Driver

The ISL6700 is an 80V/1.25A peak, medium frequency, low cost, half-bridge driver IC available in 8-lead SOIC and 12-lead QFN plastic packages. The low-side and high-side gate drivers are independently controlled and matched to 25ns. This gives the user maximum flexibility in dead-time selection and driver protocol. Undervoltage protection on both the low-side and high-side supplies force the outputs low. Non-latching, level-shift translation is used to control the upper drive circuit. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL6700IB	-40^{o}C to 125^{o}C	8 Ld SOIC	M8.15
ISL6700IR	-40^{o}C to 125^{o}C	12 Ld 4x4 QFN	L12.4x4

Features

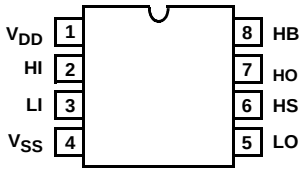
- Drives 2 N-Channel MOSFETs in Half-Bridge Configuration
- Space Saving SO8 and Low R_{C-S} QFN Packages
- Phase Supply Max Voltage to 80VDC
- Bootstrap Supply Max Voltage to 96VDC
- Drives 1000pF Load with Rise and Fall Times Typ. 15ns
- TTL/CMOS Compatible Input Thresholds
- Independent Inputs for Non-Half-Bridge Topologies
- No Start-Up Problems
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN
  - Quad Flat No Leads - Package Outline

Applications

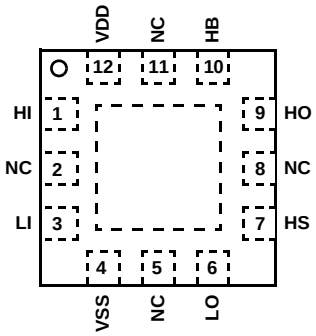
- Telecom/Datacom Power Supplies
- Half-Bridge Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

Pinouts

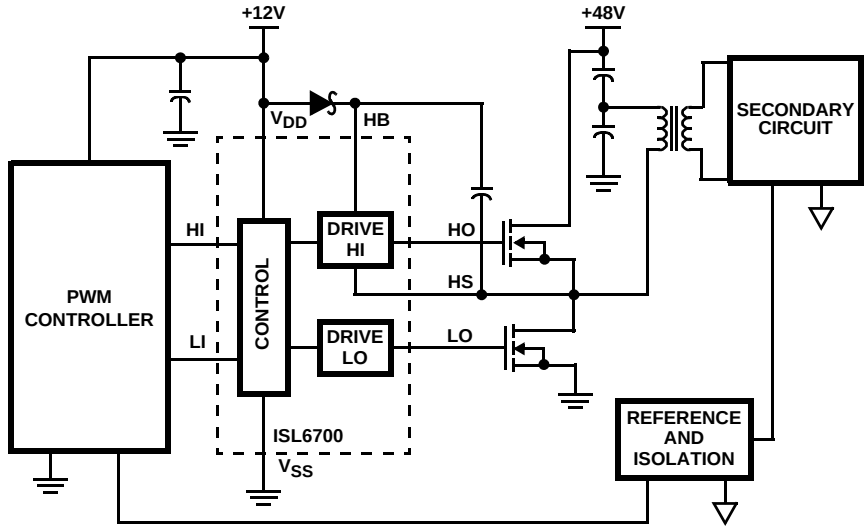
ISL6700IB (SOIC)
TOP VIEW



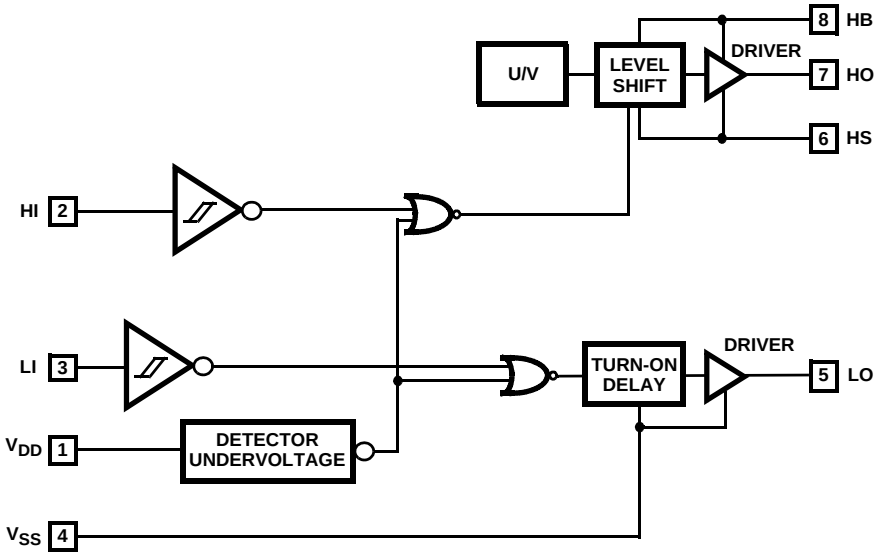
ISL6700IR (QFN)
TOP VIEW



Application Block Diagram



Functional Block Diagram



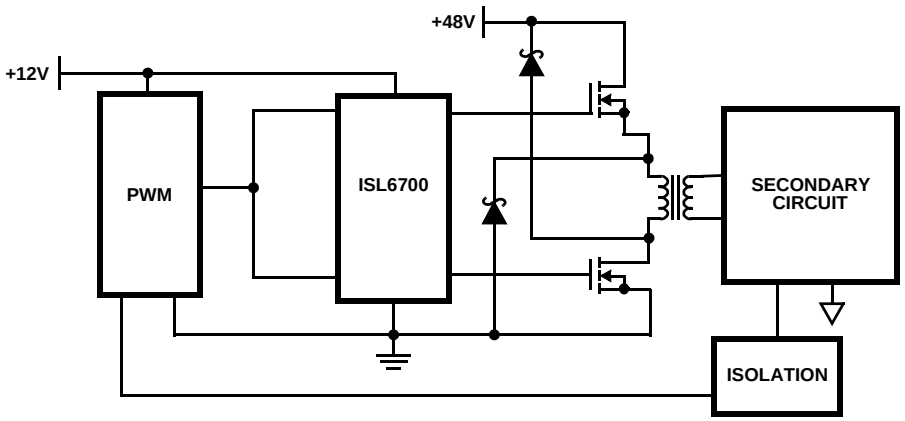


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

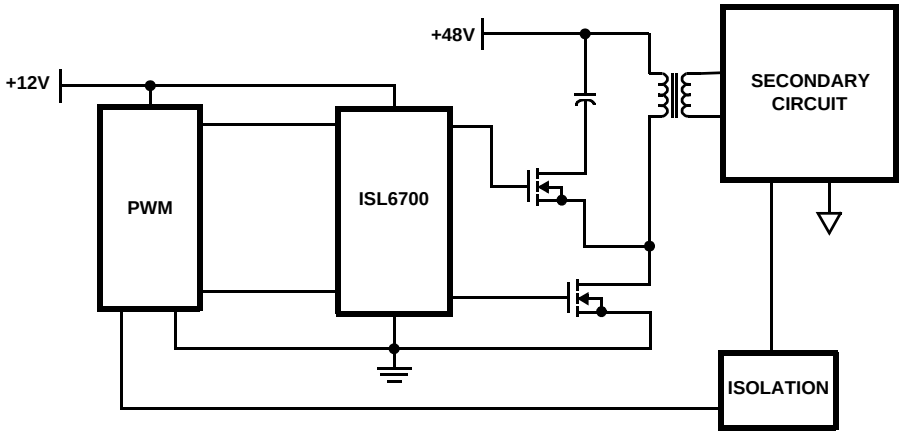


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP

Absolute Maximum Ratings

Supply Voltage, V_{DD} (Note 1) . . . . . -0.3V to 16V
LI and HI Voltages (Note 1) . . . . . -0.3V to V_{DD} +0.3V
Voltage on HS (Note 1) . . . . . -1V to 80V
Voltage on HB (Note 1) . . . . . V_{HS}-0.3V to V_{HS}+V_{DD}
Voltage on LO (Note 1) . . . . . V_{SS}-0.3 to V_{DD}+0.3V
Voltage on HO (Note 1) . . . . . V_{HS}-0.3V to V_{HB}+0.3V
Phase Slew Rate 20V/ns

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . 9V to 15.0VDC
Voltage on HS . . . . . 0V to 75V
Voltage on HS. . . . . (Repetitive Transient) -1V to 80V
Voltage on HB . . . . . V_{HS}+7.5V to V_{HS}+V_{DD}

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{O}C/W)	θ_{JC} (^{O}C/W)
SOIC (Note 2)	95	N/A
QFN (Note 3)	49	7

Max Power Dissipation at 25^{O}C in Free Air (SOIC, Note 2) . . . 1.316W
Max Power Dissipation at 25^{O}C in Free Air (QFN, Note 3) 2.976W
Maximum Storage Temperature Range. . . . . -65^{O}C to +150^{O}C
Maximum Junction Temperature Range . . . . . -40^{O}C to +150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . +300^{O}C
(SOIC - Lead Tips Only)
For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

NOTES:

1. All Voltages Referenced to Pin 4, V_{SS} Unless Otherwise Specified.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. $\theta_{JC,}$ the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = 25^{O}C			T_J = -40^{O}C TO 125^{O}C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS & UNDER VOLTAGE PROTECTION								
V_{DD} Quiescent Current	I_{DD}	LI = 0 or V_{DD}	-	1.9	2.2	-	2.4	mA
V_{DD} Operating Current	I_{DDO}	f = 50kHz	-	2.0	2.2	-	2.5	mA
V_{DD} Operating Current	I_{DDO}	f = 500kHz	-	2.5	3.0	-	4.0	mA
HB Off Quiescent Current	I_{HBL}	HI = 0	-	1.25	1.5	-	1.8	mA
HB On Quiescent Current	I_{HBH}	HI = VDD	-	170	240	-	250	µA
HB Operating Current	I_{HBO}	f = 50kHz, C_L = 1000pF	-	1.45	1.8	-	2.0	mA
HB Operating Current	I_{HBO}	f = 500kHz, C_L = 1000pF	-	2.4	2.8	-	3.0	mA
HS Leakage Current	I_{HLK}	V_{HS} = 80V V_{HB} = 96V	-	-	1	-	1	µA
V_{DD} Rising Undervoltage Threshold	V_{DDUV+}		6.8	7.6	8.25	6.5	8.5	V
V_{DD} Falling Undervoltage Threshold	V_{DDUV-}		6.5	7.1	7.8	6.25	8.1	V
Undervoltage Hysteresis	UVHYS		0.17	0.45	0.75	0.15	0.90	V
HB Undervoltage Threshold	VHBUV	Referenced to HS	5.0	5.3	6.5	4.0	7.5	V
INPUT PINS: LI and HI								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	0.8	1.6	-	0.8	-	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	-	1.7	2.2	-	2.2	V
Input Voltage Hysteresis			-	100	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-70	-60	-30	-80	-30	µA
High Level Input Current	I_{IH}	VIN = 5V, Full Operating Conditions	30	115	130	30	145	µA

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 125^oC		UNITS
			MIN	TYP	MAX	MIN	MAX	
GATE DRIVER OUTPUT PINS: LO & HO								
Low Level Output Voltage	V_{OL}	$I_{OUT} = 0A$	-	-	.1	-	.1	V
High Level Output Voltage	$V_{DD}-V_{OH}$	$I_{OUT} = 0A$	-	-	.1	-	.1	V
Peak Pullup Current	I_O+	$V_{OUT} = 0V$	-	1.4	-	-	-	A
Peak Pulldown Current	I_O-	$V_{OUT} = 12V$	-	1.3	-	-	-	A

Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 125^oC		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (LI-LO,)	T_{LPHL}		-	45	50	-	65	ns
Upper Turn-off Propagation Delay (HI-HO,)	T_{HPHL}		-	60	75	-	90	ns
Lower Turn-on Propagation Delay (LI-LO)	T_{LPLH}		-	75	82	-	95	ns
Upper Turn-on Propagation Delay (HI-HO)	T_{HPLH}		-	70	75	-	95	ns
Deadtime, (T_{HPLH} - T_{LPHL})	DHTon	LI, HI switched simultaneously	0	24	-	0	-	ns
Deadtime, (T_{LPLH} - T_{HPHL})	DLTon		0	17	-	0	-	ns
Rise Time	T_R		-	5	20	-	25	ns
Fall Time	T_F		-	5	20	-	25	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	MT		-	8	20	-	25	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	MT		-	-15	25	-	30	ns

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply to control logic and lower gate drivers. De-couple this pin to V_{SS} (Pin 4). Connect anode of bootstrap diode to this pin.
2	HI	Logic level input that controls the HO output.
3	LI	Logic level input that controls the LO output.
4	V_{SS}	Chip negative supply, generally will be ground.
5	LO	Low-side output. Connect to gate of low-side power MOSFET.
6	HS	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
7	HO	High-side output. Connect to gate of high-side power MOSFET.
8	HB	High-side bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.

Timing Diagrams

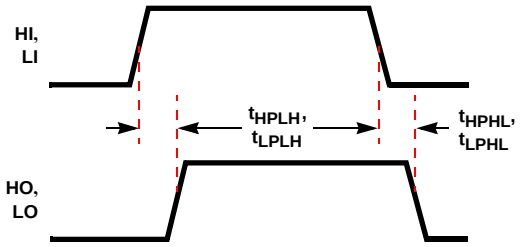


FIGURE 3.

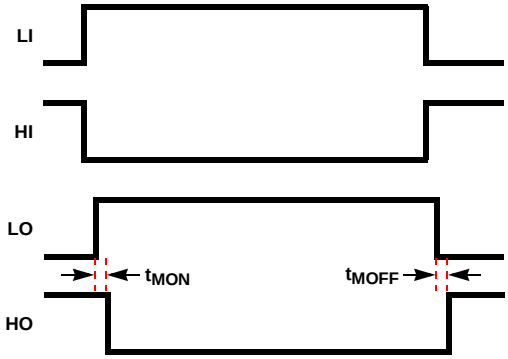
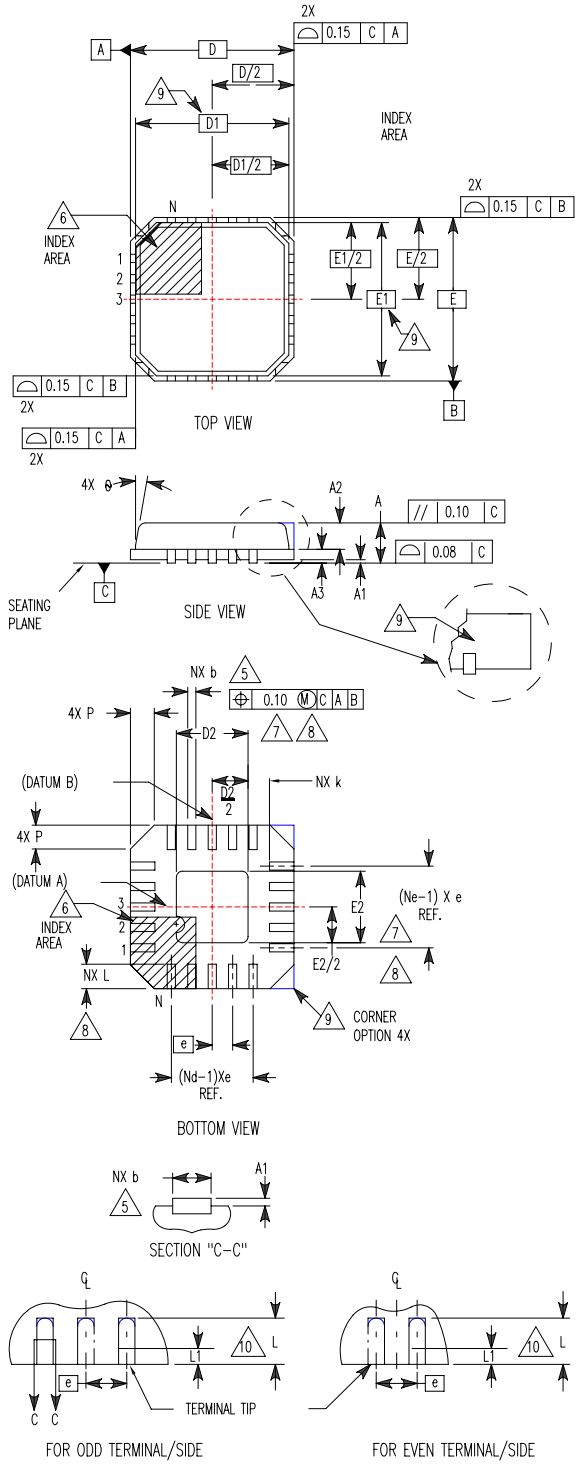


FIGURE 4.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L12.4x4

12 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

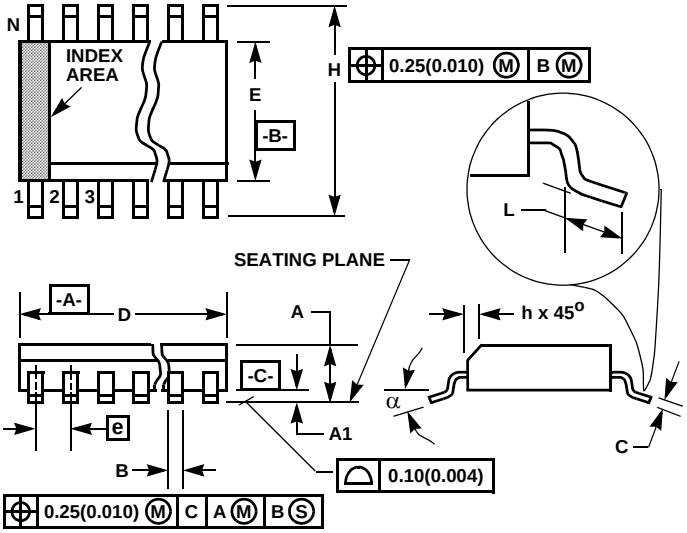
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		12		2
Nd		3		3
Ne		3		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 5/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93