CD4514BMS
CD4515BMS

CMOS 4-Bit Latch/4-to-16 Line Decoders

December 1992

Features

- **High-Voltage Types (20-Volt Rating)**
- **CD4514BMS Output “High” on Select**
- **CD4515BMS Output “Low” on Select**
- **Strobed Input Latch**
- **Inhibit Control**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C**
- **Noise Margin (Full Package-Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **5V, 10V, and 15V Parametric Ratings**
- **Standardized, Symmetrical Output Characteristics**
- **Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of ‘B’ Series CMOS Devices"**

Applications

- **Digital Multiplexing**
- **Address Decoding**
- **Hexadecimal/BCD Decoding**
- **Program-counter Decoding**
- **Control Decoder**

Description

CD4514BMS and CD4515BMS consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514BMS) or 1(CD4515BMS) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

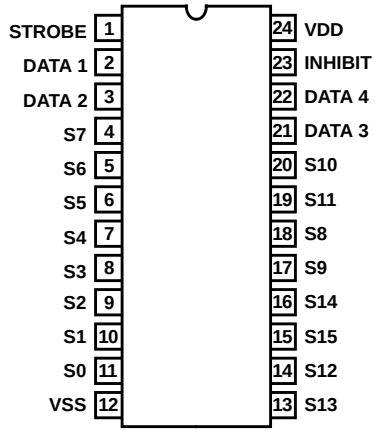
These devices are similar to industry types MC14514 and MC14515.

The CD4514BMS and CD4515BMS are supplied in these 24 lead outline packages:

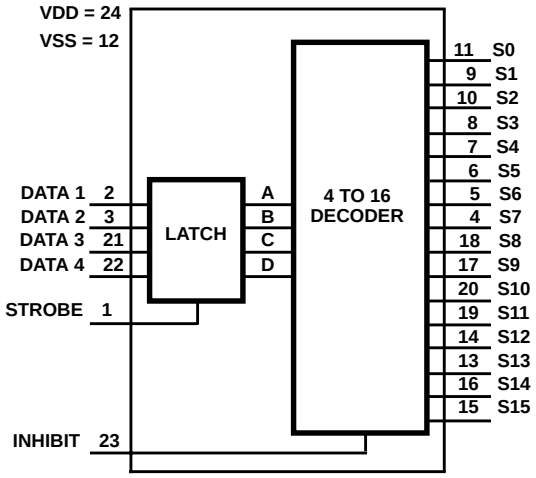
Braze Seal DIP	H4V
Frit Seal DIP	H1Z
Ceramic Flatpack	H4P

Pinout

CD4514BMS, CD4515BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering) . . . . . $+265^oC$
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	$80^oC/W$	$20^oC/W$
Flatpack Package	$70^oC/W$	$20^oC/W$

Maximum Package Power Dissipation (PD) at $+125^oC$
For T_A = -55^oC to $+100^oC$ (Package Type D, F, K) 500mW
For T_A = $+100^oC$ to $+125^oC$ (Package Type D, F, K). . . . . Derate Linearity at 12mW/^oC to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . $+175^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^oC$	-	10	µA
				2	$+125^oC$	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55^oC	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-100	-	nA
				2	$+125^oC$	-1000	-	nA
			VDD = 18V	3	-55^oC	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-	100	nA
				2	$+125^oC$	-	1000	nA
			VDD = 18V	3	-55^oC	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^oC$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^oC$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^oC$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^oC$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^oC$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^oC$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^oC$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	$+25^oC$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	$+25^oC$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^oC$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^oC$			
		VDD = 3V, VIN = VDD or GND		8B	-55^oC			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Strobe or Data	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	970	ns
			10, 11	+125°C, -55°C	-	1310	ns
Propagation Delay Inhibit	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Strobe or Datat	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	370	ns
		VDD = 15V	1, 2, 3	+25°C	-	270	ns
Propagation Delay Inhibit	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Strobe Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	75	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:
1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

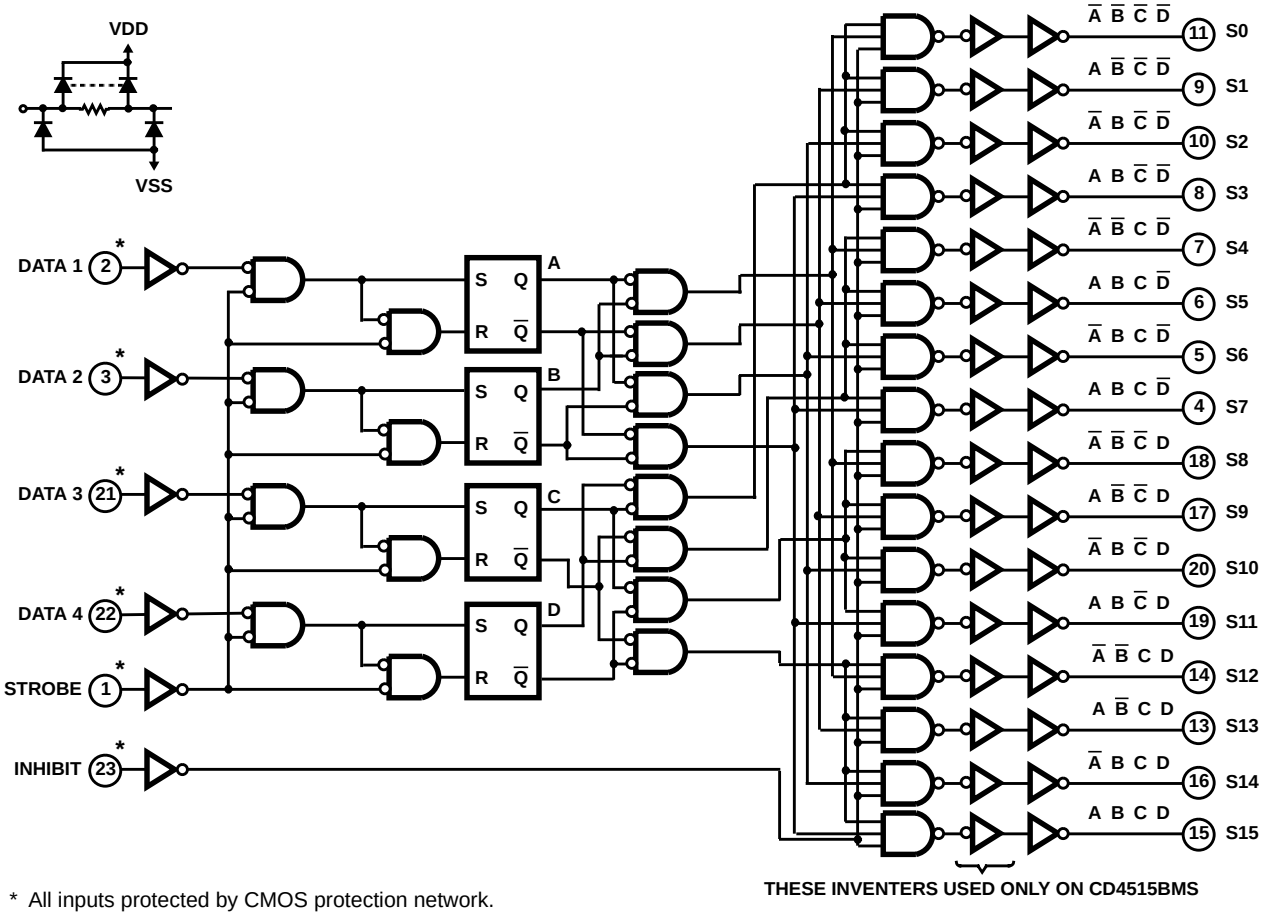
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	4-11, 13-20	1-3, 12, 21-23	24			
Static Burn-In 2 (Note 1)	4-11, 13-20	12	1-3, 21-24			
Dynamic Burn-In (Note 1)	-	2, 3, 12	21, 22, 24	4-11, 13-20	1	23
Irradiation (Note 2)						

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



* All inputs protected by CMOS protection network.

FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

INHIBIT	DECODER INPUTS D	C	B	A	SELECTED OUTPUT CD4514BMS = LOGIC 1 (HIGH) CD4515BMS = LOGIC 0 (LOW)
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514BMS All Outputs = 1, CD4515BMS

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

Typical Performance Characteristics

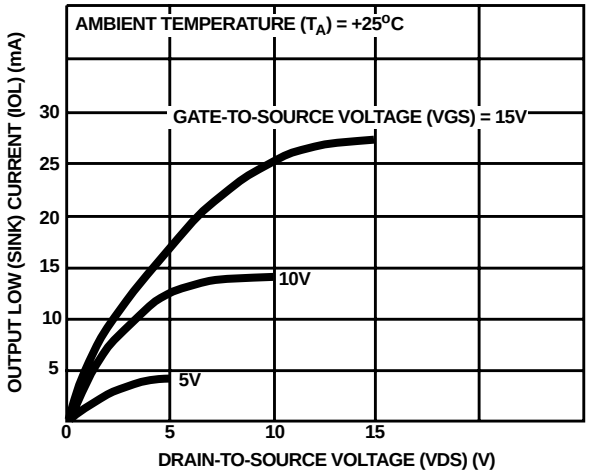


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

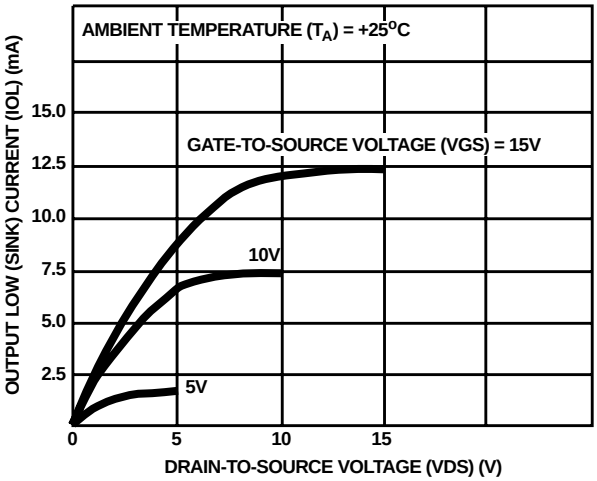


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

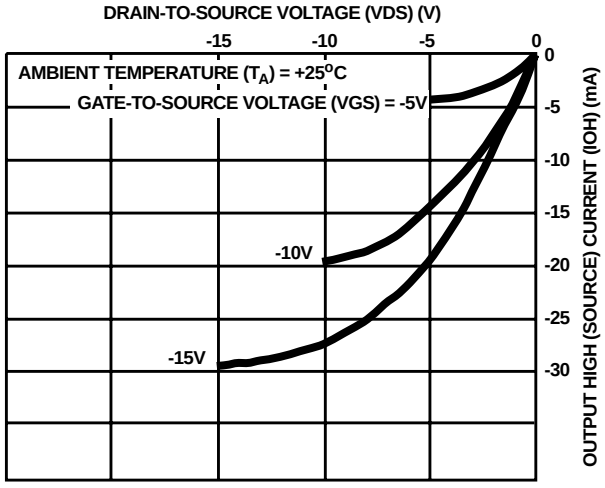


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

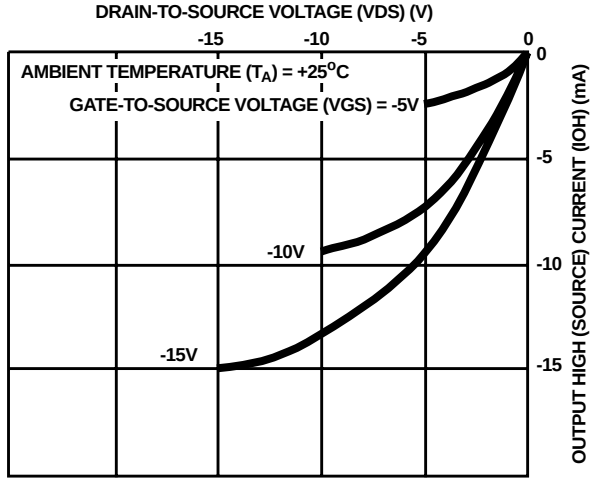


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

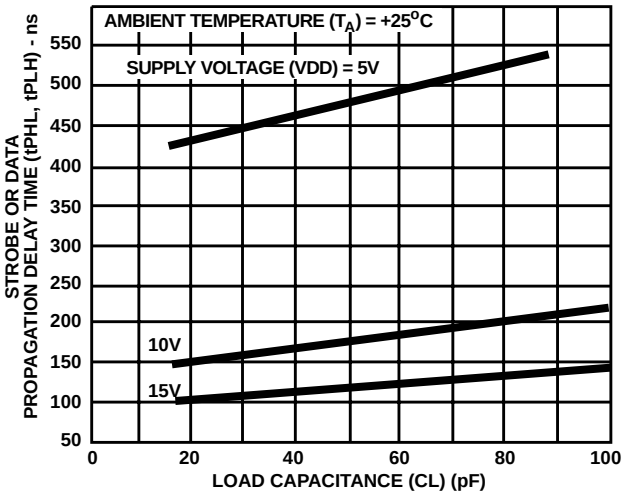


FIGURE 6. TYPICAL STROBE OR DATA PROPAGATION DELAY TIME vs LOAD CAPACITANCE

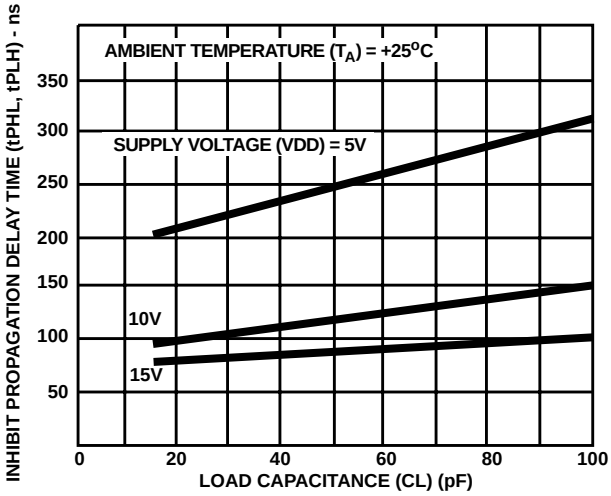


FIGURE 7. TYPICAL INHIBIT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

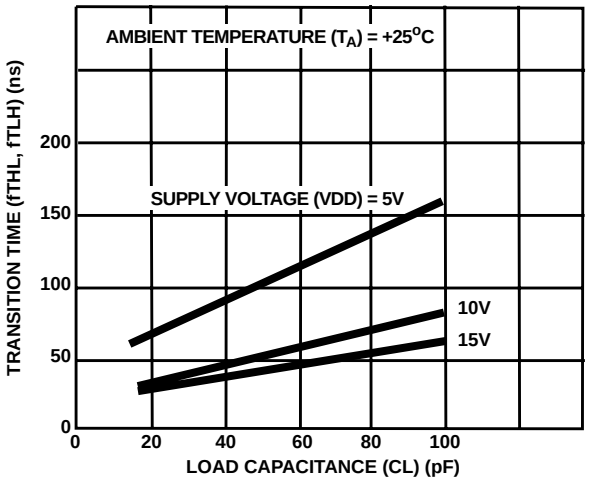


FIGURE 8. TYPICAL LOW-TO-HIGH TRANSITION TIME vs LOAD CAPACITANCE

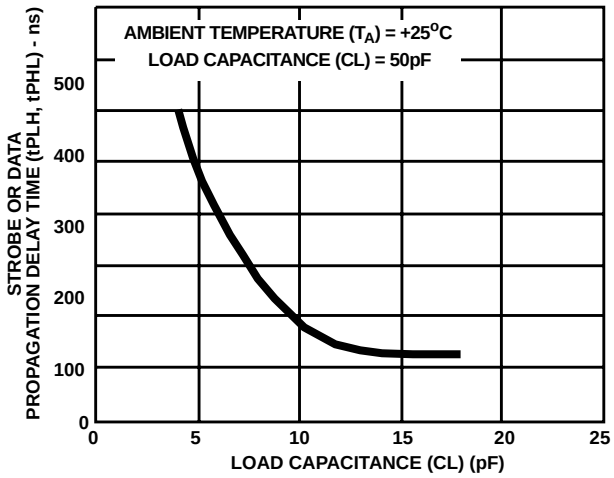
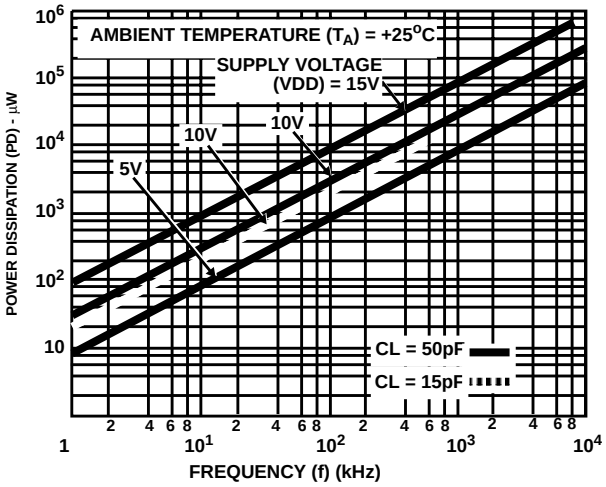


FIGURE 9. TYPICAL STROBE OR DATA PROPAGATION DELAY TIME vs SUPPLY VOLTAGE



10. TYPICAL POWER DISSIPATION vs FREQUENCY

Waveforms

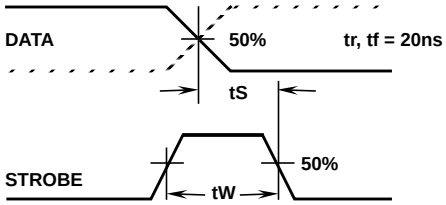
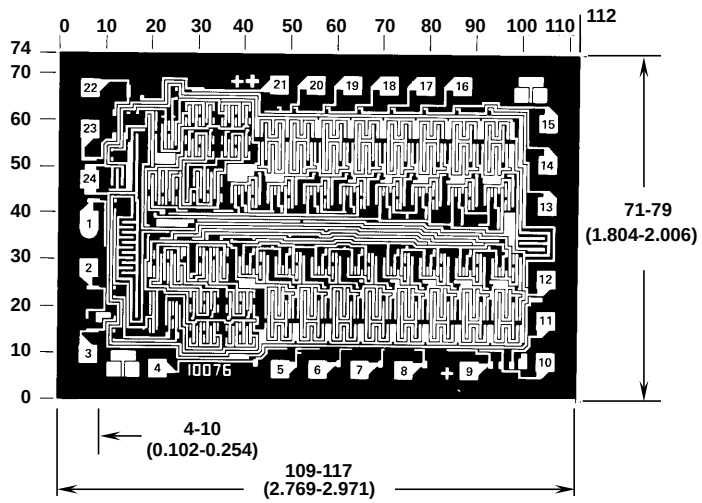


FIGURE 11. WAVEFORMS FOR SETUP TIME AND STROBE PULSE WIDTH

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in milimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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