

**CD54HC4060/3A**  
**CD54HCT4060/3A**

HARRIS SEMICOND SECTOR

T-45-23-17

T-51-11

**Switching Speed** (Limits with black dots (\*) are tested 100%.)  
**SWITCHING CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 6 \text{ ns}$ )

CHARACTERISTIC	SYMBOL	$V_{cc}$ V	25°C				-55°C to +125°C				UNITS	
			HC		HCT		54HC		54HCT			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay $\phi_I$ to $Q_4$	$t_{PLH}$	2	—	300	—	—	—	450	—	—	ns	
		4.5	—	60*	—	66*	—	90*	—	100*		
		6	—	51	—	—	—	78	—	—		
	$t_{PHL}$	2	—	80	—	—	—	120	—	—		
		4.5	—	16*	—	16*	—	24*	—	24*		
		6	—	14	—	—	—	20	—	—		
MR to $Q_n$	$t_{PHL}$	2	—	175	—	—	—	265	—	—		
		4.5	—	35*	—	44*	—	53*	—	66*		
		6	—	30	—	—	—	45	—	—		
Output Transition Time	$t_{TLH}$	2	—	75	—	—	—	110	—	—		
		4.5	—	15	—	15	—	22	—	22		
		6	—	13	—	—	—	19	—	—		
Input Capacitance	$C_I$	—	—	—	—	—	—	—	—	—		

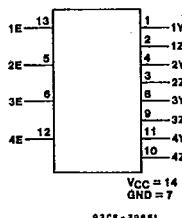
**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	$V_{cc}$ (6V)	OPEN	GROUND	$V_{cc}$ (6V)
CD54HC/HCT4060	1-7,9,10, 13-15	8,11,12	16	1-7,9,10, 13-15	8	11,12,16
Dynamic	OPEN	GROUND	1/2 $V_{cc}$ (3V)	$V_{cc}$ (6V)	OSCILLATOR	
	—	8,12	1-7,9,10,13-15	16	11	25 kHz

NOTE: Each pin except  $V_{cc}$  and Gnd will have a resistor of 2k-47k ohms.
**CD54HC4066/3A**  
**CD54HCT4066/3A**
**Quad Bilateral Switch**

The RCA CD54HC4066 and CD54HCT4066 contain four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear "ON"-resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.


**Package Specifications**  
See Section 11, Fig. 10

**FUNCTIONAL DIAGRAM**

T-SI-11

CD54HC4066/3A  
CD54HCT4066/3A

## Static Electrical Characteristics (Limits with black dots (\*) are tested 100%) — Complete Specification

CHARACTERISTIC	CD54HC4066							CD54HCT4066							UNITS			
	TEST CONDITIONS			LIMITS				TEST CONDITIONS			LIMITS							
	CONTROL $V_I$ V	SWITCH $V_{IS}$ V	$V_{CC}$ V	+25°C		-55/ +125°C		CONTROL $V_I$ V	SWITCH $V_{IS}$ V	$V_{CC}$ V	+25°C		-55/ +125°C					
High-Level Input Voltage	$V_{IH}$	—	—	2	1.5	—	—	1.5	—	—	—	4.5	to 5.5	2*	—	—	2*	—
				4.5	3.15*	—	—	3.15*	—			4.5						
Low-Level Input Voltage	$V_{IL}$	—	—	2	—	—	0.5	—	0.5	—	—	4.5	to 5.5	—	—	0.8*	—	0.8*
				4.5	—	—	1.35*	—	1.35*			4.5						
				9	—	—	2.7	—	2.7			9						
Input Leakage Current (Any Control)	$I_{IL}$	$V_{CC}$ or Gnd	—	10	—	—	$\pm 0.1*$	—	$\pm 1*$	Any Voltage Between $V_{CC}$ & Gnd	—	5.5	—	—	$\pm 0.1*$	—	$\pm 1*$	
Off-Switch Leakage Current	$I_Z$	$V_{IL}$	$V_{CC}$ or Gnd	10	—	—	$\pm 0.1*$	—	$\pm 1*$	$V_{IL}$	$V_{CC}$ or Gnd	5.5	—	—	$\pm 0.1*$	—	$\pm 1*$	
"On" Resistance $I_o = 1 \text{ mA}$	$R_{on}$	$V_{CC}$	$V_{CC}$	4.5	—	25	80	—	128	$V_{CC}$	$V_{CC}$	4.5	—	25	80	—	128	
			Gnd	6	—	20	75	—	113			—	—	—	—	—	—	
		$V_{CC}$	$V_{CC}$ to Gnd	9	—	15	60	—	95		$V_{CC}$	4.5	—	35	95*	—	142*	
	$\Delta R_{on}$	$V_{CC}$	$V_{CC}$	4.5	—	35	95*	—	142*		$V_{CC}$	—	—	—	—	—	—	
			Gnd	6	—	24	84	—	126			—	—	—	—	—	—	
			$V_{CC}$	9	—	16	70*	—	105*			—	—	—	—	—	—	
"On" Resistance Between Any Two Switches	$\Delta R_{on}$	$V_{CC}$	—	4.5	—	1	—	—	—	$V_{CC}$	—	4.5	—	1	—	—	—	
			$V_{CC}$	6	—	0.75	—	—	—			—	—	—	—	—	—	
			Gnd	9	—	0.5	—	—	—			—	—	—	—	—	—	
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or Gnd	—	6	—	—	2*	—	40*	$V_{CC}$ or Gnd	—	5.5	—	—	2*	—	40*	
			$V_{CC}$	10	—	—	16	—	320			5.5	—	—	2*	—	40*	
Additional Quiescent Device Current per Input Pin: 1 Unit Load	$\Delta I_{CC}$ *	—	—	—	—	—	—	—	—	$V_{CC}-2.1$	—	4.5 to 5.5	—	100	360	—	490	

\*For dual-supply systems theoretical worst case ( $V_I = 2.4 \text{ V}$ ,  $V_{CC} = 5.5 \text{ V}$ ) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	1

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 360  $\mu\text{A}$  max. @ 25°C.

**CD54HC4066/3A**  
**CD54HCT4066/3A**

HARRIS SEMICONDUCTOR

T-51-12

**Switching Speed** (Limits with black dots (\*) are tested 100%.)  
**SWITCHING CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 6 \text{ ns}$ )

CHARACTERISTIC	SYMBOL	V <sub>cc</sub> V	25°C				-55°C to +125°C				UNITS	
			HC		HCT		54HC		54HCT			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay Switch In to Out	$t_{PLH}$	2	—	60	—	—	—	90	—	—	ns	
	$t_{PHL}$	4.5	—	12	—	12	—	18	—	18		
		9	—	8	—	—	—	13	—	—		
Switch Turn On Delay	$t_{PZH}$	2	—	100	—	—	—	150	—	—	ns	
	$t_{PZL}$	4.5	—	20*	—	24*	—	30*	—	36*		
		9	—	12	—	—	—	18	—	—		
Switch Turn Off Delay	$t_{PHZ}$	2	—	150	—	—	—	225	—	—	ns	
	$t_{PLZ}$	4.5	—	30*	—	35*	—	45*	—	53*		
		9	—	24	—	—	—	36	—	—		
Input Capacitance	$C_I$	—	—	10	—	10	—	10	—	10	pF	

**Burn-In Test-Circuit Connections** (Use Static II for /3A burn-in and Dynamic for Life Test.)

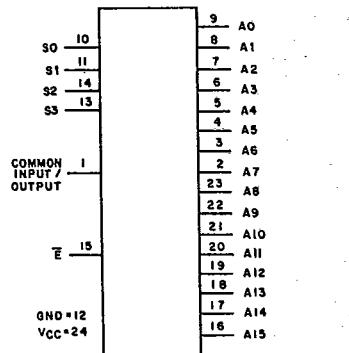
Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V <sub>cc</sub> (6V)	OPEN	GROUND	V <sub>cc</sub> (6V)
CD54HC/HCT4066	1-4,8-11	5-7,12,13	14	1-4,8-11	7	5,6,12-14
Dynamic	OPEN	GROUND	1/2 V <sub>cc</sub> (3V)	V <sub>cc</sub> (6V)	OSCILLATOR	
	—	7	2,3,9,10	14	50 kHz	25 kHz
CD54HC/HCT4066					5,6,12,13	1,4,8,11

NOTE: Each pin except V<sub>cc</sub> and Gnd will have a resistor of 2k-47k ohms.

**CD54HC4067/3A**  
**CD54HCT4067/3A**
**16-Channel Analog Multiplexer/Demultiplexer**

The RCA CD54HC4067 and CD54HCT4067 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage-supply range. They are bidirectional switches thus allowing any analog input to be used as an output and vice versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which when high will disable all switches to their "off" state.


**Package Specifications**  
See Section 11, Fig. 15

**FUNCTIONAL DIAGRAM**