2N4351
N-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch

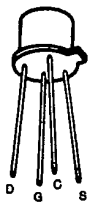
INTERSIL

2N4351

FEATURES
- Low ON Resistance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

PIN CONFIGURATION

TO-72



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ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Source Voltage or Drain-Body Voltage 25V
Peak Gate-Source Voltage (Note 1) ..... ±125V
Drain Current 100mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 375mW
Derate above 25°C ..... 3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-72
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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Substrate connected to source.

Symbol	Parameter	Test Conditions	Min	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10μA, V_{GS}=0	25		V
I_{GSS}	Gate Leakage Current	V_{GS}=±30V, V_{DS}=0		10	pA
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=10V, V_{GS}=0		10	nA
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS}=10V, I_D=10μA	1	5	V
$I_{D(on)}$	'ON' Drain Current	V_{GS}=10V, V_{DS}=10V	3		mA
$V_{DS(on)}$	Drain-Source "ON" Voltage	I_D=2mA, V_{GS}=10V		1	V
$r_{DS(on)}$	Drain-Source Resistance	V_{GS}=10V, I_D=0, f=1kHz		300	ohms
$\|y_{fs}\|$	Forward Transfer Admittance	V_{DS}=10V, I_D=2mA, f=1kHz	1000		μs
C_{rss}	Reverse Transfer Capacitance (Note 2)	V_{DS}=0, V_{GS}=0, f=1MHz		1.3	pF
C_{iss}	Input Capacitance (Note 2)	V_{DS}=10V, V_{GS}=0, f=1MHz		5.0	pF
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 2)	$V_{D(SUB)}$=10V, f=1MHz		5.0	pF
$t_{d(on)}$	Turn-On Delay (Note 2)	Switching Times Test Circuit		45	ns
t_r	Rise Time (Note 2)			65	ns
$t_{d(off)}$	Turn-Off Delay (Note 2)			60	ns
t_f	Fall Time (Note 2)			100	ns

NOTES: 1. Device must not be tested at ±125V more than once or longer than 300ms.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.