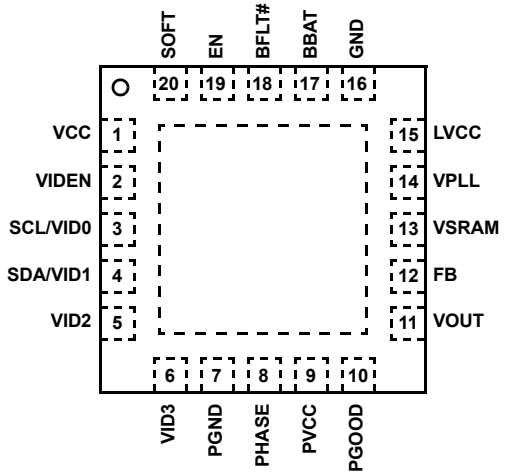
Integrated XScale Regulator

The ISL6271 is a versatile power management IC (PMIC) designed for the Xscale type of processors. The device integrates three regulators, two fault indicators and an I^2C bus for communication with a host microprocessor. Two of the three regulators function as low power, low drop out regulators, designed to power SRAM and phase-lock loop circuitry internal to the Xscale processor. The third regulator uses a proprietary switch-mode topology to power the processor core and facilitate Dynamic Voltage Management (DVM), as defined by Intel.

Since power dissipation inside a microprocessor is proportional to the square of the core voltage, Intel XScale processors implement DVM as a means to more efficiently utilize battery capacity. To support this power saving architecture, the ISL6271 integrates an I^2C bus for communication with the host processor. The processor, acting as the bus master, transmits a “voltage level” and “voltage slew rate” to the ISL6271 appropriate to the processing requirements; higher core voltages support higher operating frequencies and code execution. The bus is fully compliant with the Phillips® I^2C protocol and supports both standard and fast data transmission modes. Alternatively, the output of the core regulator can be programmed in 50mV increments from 0.85V to 1.6V using the input Voltage ID (VID) pins. All three regulators share a common enable pin and are protected against overcurrent, over temperature and undervoltage conditions. When disabled via the enable pin, the ISL6271 enters a low power state that can be used to conserve battery life while maintaining the last programmed VID code and slew rate. An integrated soft-start circuit transitions the ISL6271 output voltages to their default values at a rate determined by an external soft-start capacitor.

Pinout

ISL6721 (4x4 QFN) TOP VIEW



Features

- Three Voltage Regulators (1 Buck, 2 LDOs)
- High-Efficiency, fully-Integrated synchronous buck regulator with DVM
- Proprietary ‘Synthetic Ripple’ Control Topology
- Greater than 1MHz Switching Frequency
- Diode emulation for light load efficiency
- I^2C Interface Module for DVM from 0.85V to 1.6V
- Optional fixed 4-bit VID-control in lieu of DVM
- Small Output Inductor and Capacitor
- Battery Fault signal
- Input Supply Voltage Range: 2.76V–5.5V
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile

Applications

- PDA
- Cell Phone
- Tablet Devices
- Embedded Processors

Related Literature

- Technical Brief TB379 “*Thermal Characterization of Packaged Semiconductor Devices”*
- Technical Brief TB389 “*PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages“*

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6271CR	-25 to 85	20 Ld 4x4 QFN	L20.4x4
ISL6271CR-T	20 Ld 4x4 QFN Tape and Reel		

Regulator Block Diagram

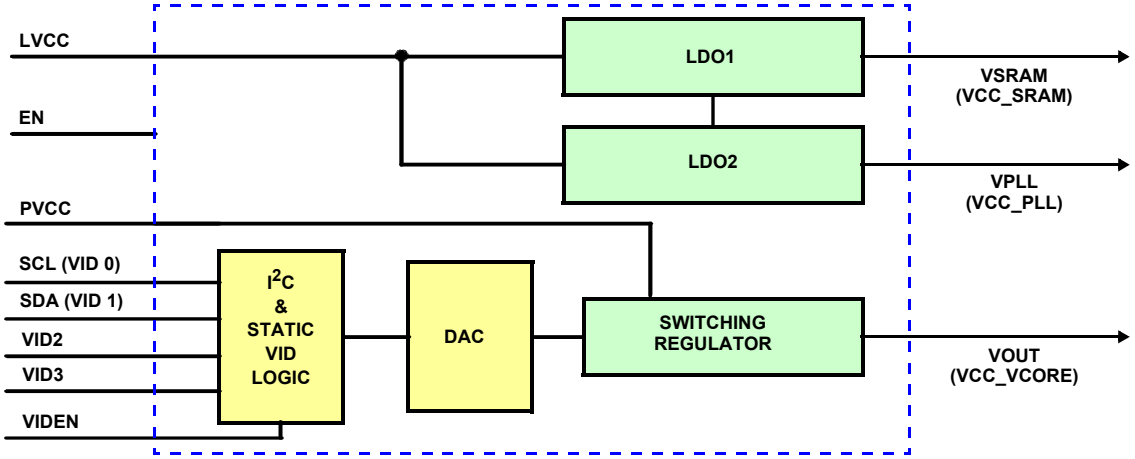


FIGURE 1. BULVERDE POWER CONTROLLER

Functional Block Diagram

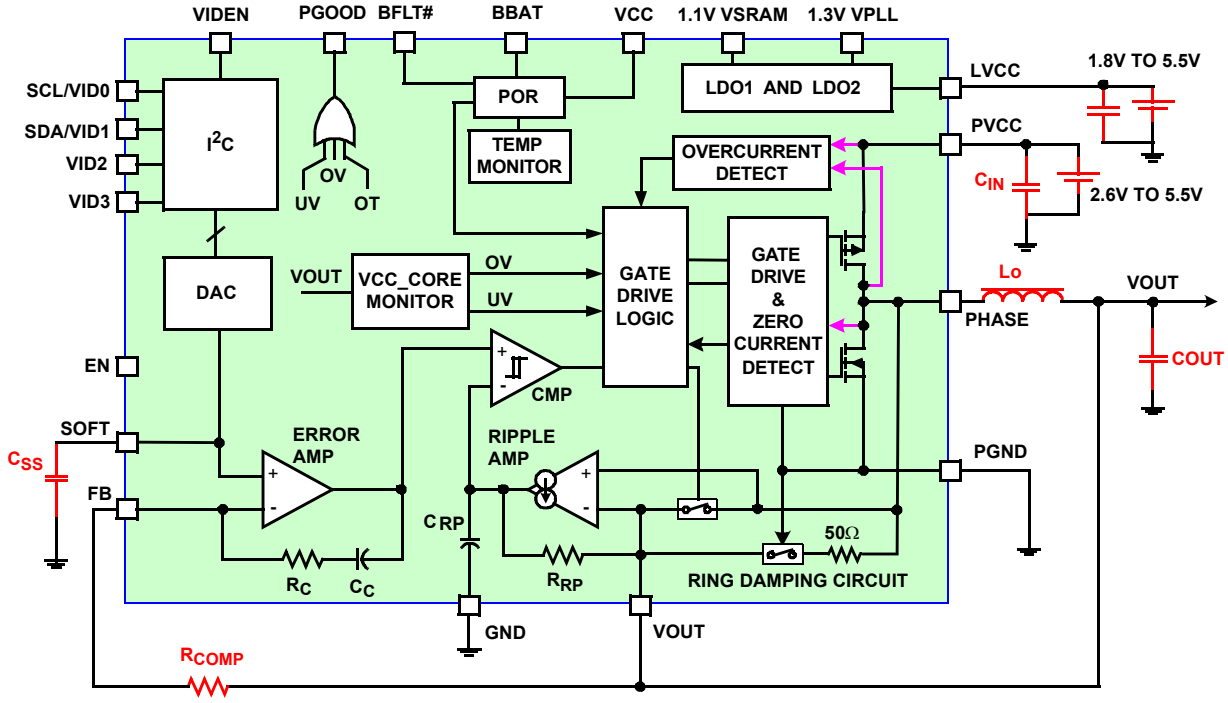


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

Supply Voltage (PVCC, VCC, LVCC). 7V
Signal Input Voltage (EN, VID (Note 1), VIDEN) . . . . GND-0.3 to 7V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model (Per EIAJ ED-4701 Method C-111). 200V

Operating Conditions

Ambient Temperature Range. . . . . .-25°C to 85°C
Supply Voltage (PVCC, VCC) . . . . . 2.76 to 5.5V
Supply Voltage (LVCC) . . . . . 1.7 - 5.5V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package (Notes 2, 3)	45	7.5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Switching frequency is a function of input, output voltage and load.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features (TB379).
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions, Unless Otherwise Noted; T_A = -25°C to 85°C, PVCC, VCC = 3.7V. Component values as shown in Figure 19, Typical Application Circuit: Vout = 1.6V.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CORE BUCK REGULATOR						
Output Voltage Nominal Range	VOUT	Programmable in 50mV increments	0.85		1.60	V
Max. DC Output Current	Icore		600			mA
Current Limit (DC plus Ripple)	Icore_lim	(wafer level test only)	700	800		mA
PMOS on Resistance	$r_{DS(ON)p}$	Iout = 200mA		275		mΩ
NMOS on Resistance	$r_{DS(ON)n}$	Iout = 200mA		140		mΩ
Frequency (Note 4)	f	Vin = 3.7V, Vo = 1.0V		1.2		MHz
Load Regulation		VOUT = 1.6V; Io = 1mA–500mA		0.05	1	%
Line Regulation		Over VCC range		1		%
Pk-Pk Ripple	V_{P-P}	Vout = 1.6V, I = 0.4A, CCM		5		mV
		Discontinous Mode Operation		10		mV
System Accuracy		Over Temperature	-1		2	%
		Room Temperature	-1		1	%
Undervoltage Threshold (Note 5)		Rising, as % of nominal VOUT		94		%
		Falling, as % of nominal VOUT		86		%
Overvoltage threshold		Rising, as % of nominal VOUT		114		%
		Falling, as % of nominal VOUT		106		%
Start-up Time	t_{st}	From Enable Active @ Io = 10mA; Vo = 1.6V		1.3		ms
Ring Damping Switch Resistance	$R_{on(RD)}$			50	75	Ω
LINEAR REGULATORS						
Input Voltage	LVCC	Connected to PVCC	1.70		5.5	V
		Not connected to PVCC	1.70		3.5	V
Output Voltage	VSRAM			1.1		V
	VPLL			1.3		V
Output Tolerance		Iout = 1mA	-2.5		2.5	%

Electrical Specifications Operating Conditions, Unless Otherwise Noted; T_A = -25°C to 85°C, PVCC, VCC = 3.7V. Component values as shown in Figure 19, Typical Application Circuit: Vout = 1.6V. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Average Output Current	I_SRAM		50			mA
	I_PLL		30			mA
Current Limit	I_{ldo_lim}	Each LDO regulator	120	300		% (Note 7)
Line Regulation		LVCC = 1.7–5.5V			0.25	%
Load Regulation		Io = 1 to 25mA			0.5	%
Undervoltage Threshold		Rising - % of VPLL, VSRAM		91		%
		Falling - % of VPLL, VSRAM		86		%
Start-Up Time	tst	Soft-start power up to 1.3V, Csoft = 10nF		1.3		ms
SYSTEM						
Supply Current (VCC)	I_Q	I_{core} = No load		380		µA
	I_Q	EN = 0V		2	5	µA
Supply Current (LVCC)	I_{LVCC}			25		µA
EN Voltage	V_{IH}				2.0	V
	V_{IL}		0.55			V
Soft-Start Source Current (Controlled by I2C control bits D5, D4)	I_{00}		2.75	4.8	7.25	µA
	I_{01}		5.4	9.4	14.5	µA
	I_{10}		13.5	23.4	36	µA
	I_{11}		27	46	72	µA
Temperature Shutdown	T_r	Rising T	130	140	150	°C
	T_f	Falling T	85	95	105	°C
POR/BFLT# Threshold (Note 6)	V_{POR}	Rising VCC	2.60	2.80	3.0	V
	V_{POR}	Falling VCC	2.44	2.60	2.76	V
PGOOD Pull Down Resistance	R_{on}			700	960	Ω
VIDEN, VID2, VID3 Voltage Threshold	$V_{IH(VID)}$				2.4	V
	$V_{IL(VID)}$		1.0			V
I^2C LOGIC						
SCL, SDA Voltage Threshold	$V_{IH(I^2C)}$				2.0	V
	$V_{IL(I^2C)}$		0.55			V
SDA Pull Down Resistance	$R_{on(SDA)}$				132	Ω

NOTES:

4. Switching frequency is a function of input, output voltage and load.
5. As a result of an overcurrent condition exceeding 600mA. Will result in a PGOOD fault.
6. A high rising POR tracks with a high falling POR.
7. Percentage of Maximum Average Output Current (I_SRAM or I_PLL).

Typical Operating Performance

Test results from the Intersil ISL6271 Customer Reference Board (CRB). Output filter on switcher made up of a 3.3µH drumcore with 100mΩ of DCR and an output capacitance of 4.7µF. X5R; Rcomp = 100kΩ, Vin = 3.7V unless otherwise noted.

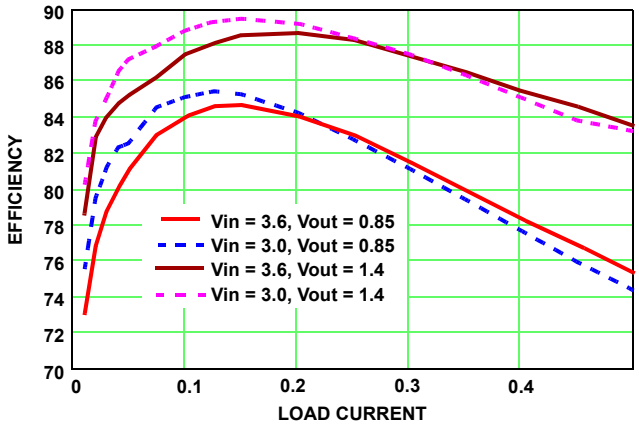


FIGURE 3. SWITCHING FREQUENCY REGULATION

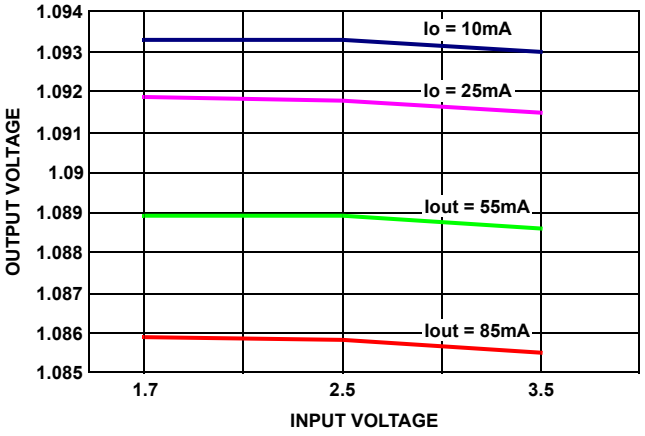


FIGURE 4. VSRAM LINE-LOAD REGULATION

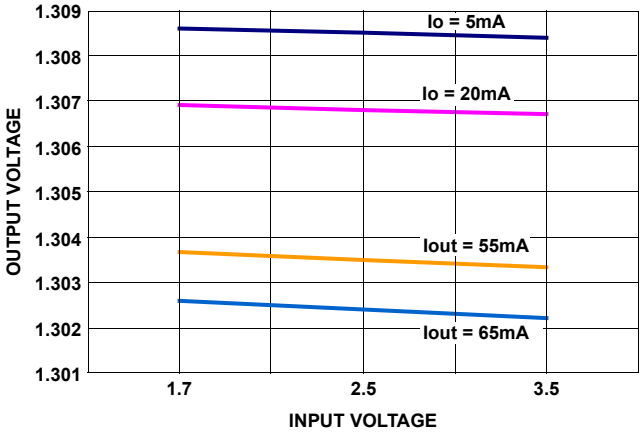
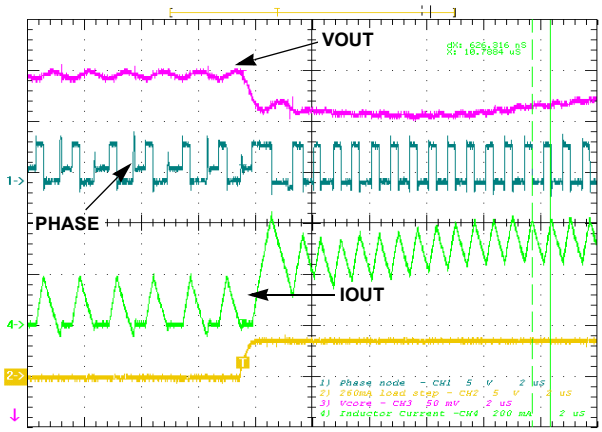
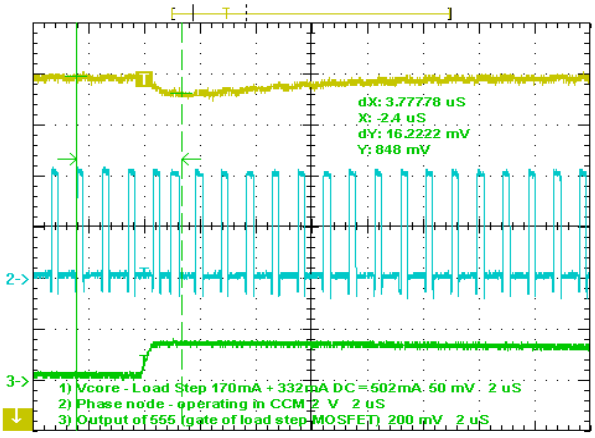


FIGURE 5. SWITCHING REGULATOR EFFICIENCY



50mA to 260mA load step on VOUT.
Top: Output voltage, 50mV/DIV; Phase node, 5V/DIV.;
Inductor current, 200mA/DIV, 2µs/DIV

FIGURE 6. DCM TO CCM

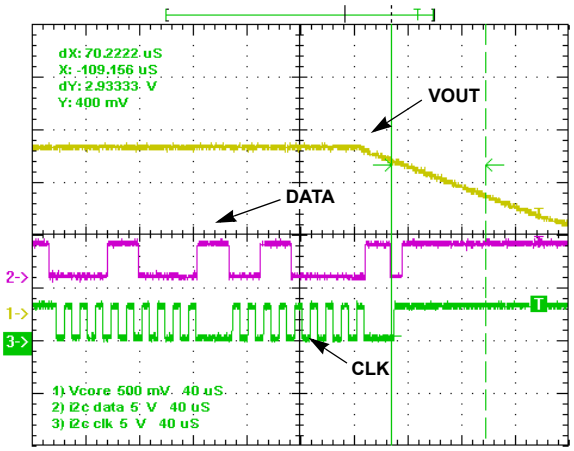


Top: phase node output voltage ripple, 10mV/DIV.
Bottom: Inductor current, 100mA/DIV, 1µs/DIV

FIGURE 7. CCM TO CCM

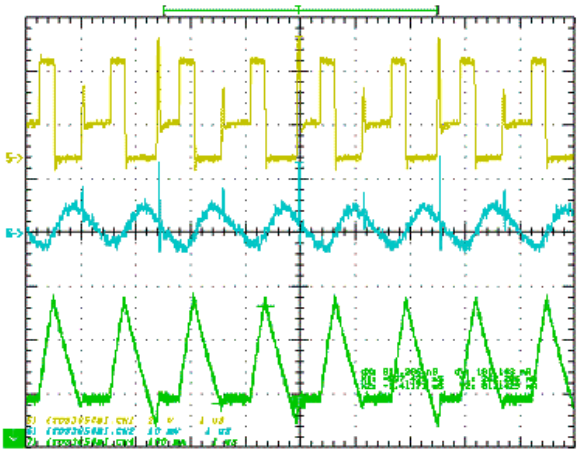
Typical Operating Performance (Continued)

Test results from the Intersil ISL6271 Customer Reference Board (CRB). Output filter on switcher made up of a 3.3µH drumcore with 100mΩ of DCR and an output capacitance of 4.7µF. X5R; Rcomp = 100kΩ, Vin = 3.7V unless otherwise noted.



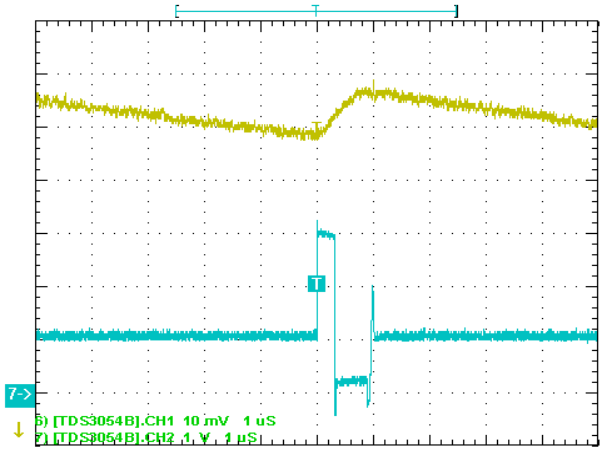
I²C Vout = 0.85 to 1.6V 5mV/µs, 40µs/DIV

FIGURE 8. TYPICAL I²C COMMUNICATION



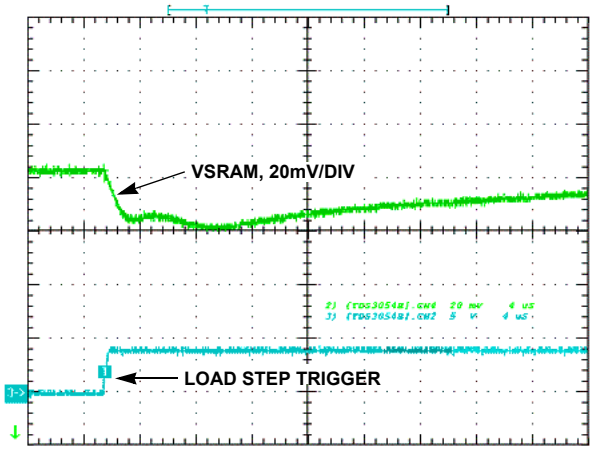
Top: phase node output voltage ripple, 10mV/DIV
Bottom: Inductor current, 100mA/DIV, 1µs/DIV

FIGURE 9. RIPPLE IN DCM



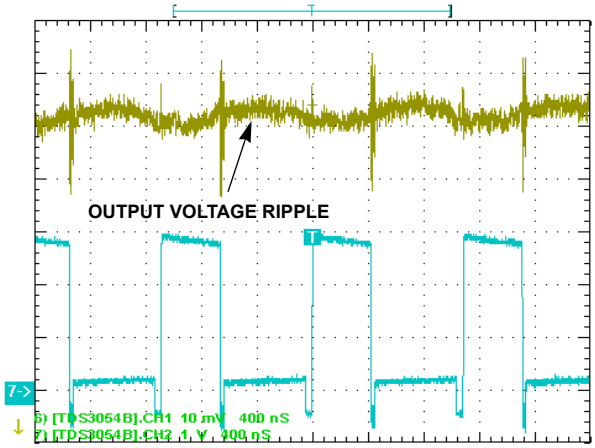
Ripple in DCM: Fripple = 145kHz, Vin = 2.85V, Vout = 0.85V, Iout = 10mA Ripple = 10mV (worst case), 1µs/DIV

FIGURE 10. PHASE NODE TO DCM



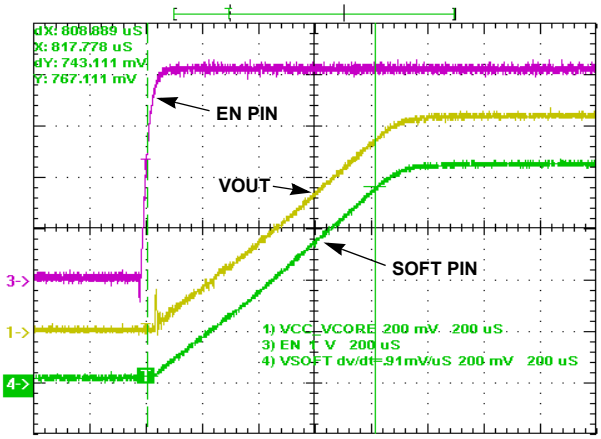
LDO transient response with 3.3µF output capacitance. LVCC = 4.1V. 10mA DC load+ 55mA step load.

FIGURE 11. LDO TRANSIENT RESPONSE



Ripple in CCM Vin = 2.85V, Vo = 0.850V, Fripple = 1MHz, Io = 500mA, Ripple = 4.2mV, 400ns/DIV

FIGURE 12. RIPPLE IN CCM

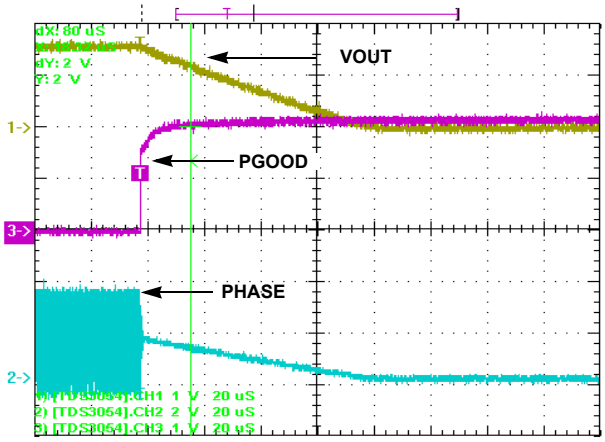


Soft-start into CCM, VIN = 4.2V, CH3 = EN pin. Vout = 0.85 Soft-Start capacitor = 10nF. 200µs/DIV

FIGURE 13. SOFT-START INTO CCM

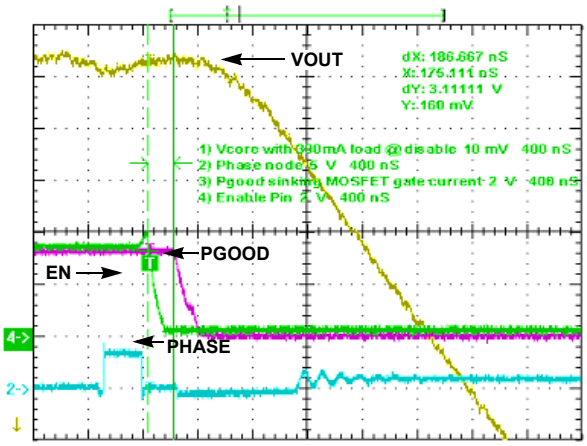
Typical Operating Performance (Continued)

Test results from the Intersil ISL6271 Customer Reference Board (CRB). Output filter on switcher made up of a 3.3µH drumcore with 100mΩ of DCR and an output capacitance of 4.7µF. X5R; Rcomp = 100kΩ, Vin = 3.7V unless otherwise noted.



Forced PGOOD fault. Converter operating in CCM at 420mA prior to applying a 320mA transient step. This pushes the regulator beyond the overcurrent threshold of 700mA. The phase node three-stated and follows Vout to 0V. 20µs/DIV

FIGURE 14. FORCED PGOOD FAULT



PGOOD delay = 186ns from disable.
Vout = 0.85V prior to EN going low, 400ns/DIV

FIGURE 15. PGOOD DELAY

Functional Pin Description

PVCC - Input power to the core switching regulator. This voltage is typically supplied by a the primary, single-cell Li-ion battery or power adapter.

VCC - Voltage source for control circuitry. Must be held within 0.2V of PVCC.

BBAT - Secondary back-up voltage used to provide an indication of the main battery status when the main battery is low or absent. BBAT is typically a coin cell device and must be maintained between 1.5V and 3.75V.

PHASE - The output switching node that connects to the output inductor to generate the processor core voltage.

VOUT - Output voltage of the core regulator. Programmable from 0.85 to 1.6V via the integrated I^2C bus or VID pins.

LVCC - Input voltage to the VSRAM and VPLL LDO pass elements. To minimize power loss across the pass element this should be tied to a pre-regulated system voltage between 1.8V and 2.5V. LVCC can operate from the main battery input when lower voltages are unavailable.

VPLL - 1.3V LDO regulator designed to supply power to the phase-locked loop circuitry internal to the microprocessor.

VSRAM - 1.1V LDO regulator designed to supply power to the microprocessor SRAM circuitry.

FB - Core voltage feedback (to the error amplifier) via an external compensation resistor.

SOFT - An external capacitor connected between this pin and ground controls the regulators output rise time. The start-up ramp begins when VCC reaches its power-on-reset (POR) rising threshold and the EN pin is high.

EN - The ISL6271 outputs are enabled when a voltage greater than 2V is applied to the EN pin. The core regulator output MOSFETs bridge is turned off and the LDOs are disabled when EN is pulled low.

BFLT# - Battery fault indicator. A high level indicates the adequacy of the battery for regulator start-up. Designed to interface with the processor General Purpose IO, this pin is actively pulled low when the main battery is absent.

PGOOD - An open-drain output that indicates the status of the three regulators. It is pulled low when any of the regulators are outside their voltage tolerances.

VIDEN - Pull this pin low to enable I^2C communication. Connecting this pin to VCC disables the I^2C bus and enables the VID inputs. In this mode the slew rate is fixed at a value determined by the soft-start capacitor.

SCL (VID0) - This is a dual function pin. When VIDEN is low it acts as the I^2C clock input (SCL). When VIDEN is high this pin acts as bit 0 to the VID DAC.

SDA (VID1) - This is a dual function pin. When VIDEN is low it acts as the I^2C data/address line (SDA) used to transfer voltage level and slew rate instructions to the ISL6271. When VIDEN is high this pin acts as bit 1 to the VID DAC.

VID2, VID3 - VID inputs to the error amplifier reference DAC. Used to control the core voltage when VIDEN is high.

GND - Device signal ground. Connected to PGND at a single point to avoid ground loops.

PGND - Power ground return connection for the internal synchronous rectifier.

Operational Description

Initialization

Upon application of input power to the ISL6271, the power good signal (PGOOD) will switch from low to high after four conditions are met - (1) VCC exceeds the power on reset “rising threshold”, (2) the EN pin is high and (3) the LDO input voltage (LVCC) is greater than 1.6V, (4) All three outputs are in regulation. Figure 3 illustrates this start-up sequence. The outputs are powered on under a soft-start regime with the core output voltage defaulting to 1.3V (unless under VID control) and the LDOs at their fixed output levels. Once the outputs are in regulation, the ISL6271 will respond to a voltage change command via the I^2C bus.

Core Regulator Output

The ISL6271 core regulator is a synchronous buck regulator that employs an Intersil proprietary switch-mode topology known as Synthetic Ripple Regulation (SRR). The SRR architecture is a derivative of the conventional hysteretic-mode regulator without the inherent noise sensitivities and dependence on output capacitance ESR. The topology achieves excellent transient response and high efficiency over the entire operating load range. Output voltage ripple is typically under 5mV in Continuous Conduction Mode (CCM) and under 10mV in DCM (diode emulation). The output core voltage is derived from the main battery pak (typically a single cell Li-ion battery) and is programmable in 50mV steps between 0.85 and 1.6V. The output regulator set-point is controlled by an on-chip DAC which receives its input either from the I^2C bus or the VID input pins (VID0-VID3). Table 1 identifies the VID code states and corresponding output voltage. To minimize core voltage over-shoot and under-shoot between code states, the ISL6271 implements programmable, voltage slew rate control via the I^2C bus. The slew rate is a function of the data in the slew rate control register and also the soft-start capacitor; the slew rates in Table 2 assume a soft-start capacitor value of 10nF. Once the regulator has initialized, the IC can be placed in a low quiescent state by pulling low the EN pin. The regulator ‘remembers’ the last programmed voltage level and slew rate after each subsequent EN cycle, and return to the previous set-point once EN is brought high.

TABLE 1. VOLTAGE-SET COMMAND BITS

I^2C DATA BYTE OR VID PINS								
MSB				D3	D2	D1	LSB D0	NOMINAL OUTPUT
X	X	X	X	0	0	0	0	**0.850**
X	X	X	X	0	0	0	1	**0.900**
X	X	X	X	0	0	1	0	**0.950**
X	X	X	X	0	0	1	1	**1.000**
X	X	X	X	0	1	0	0	**1.050**
X	X	X	X	0	1	0	1	**1.100**
X	X	X	X	0	1	1	0	**1.150**
X	X	X	X	0	1	1	1	**1.200**
X	X	X	X	1	0	0	0	**1.250**
X	X	X	X	1	0	0	1	**1.300**
X	X	X	X	1	0	1	0	**1.350**
X	X	X	X	1	0	1	1	**1.400**
X	X	X	X	1	1	0	0	**1.450**
X	X	X	X	1	1	0	1	**1.500**
X	X	X	X	1	1	1	0	**1.550**
X	X	X	X	1	1	1	1	**1.600**

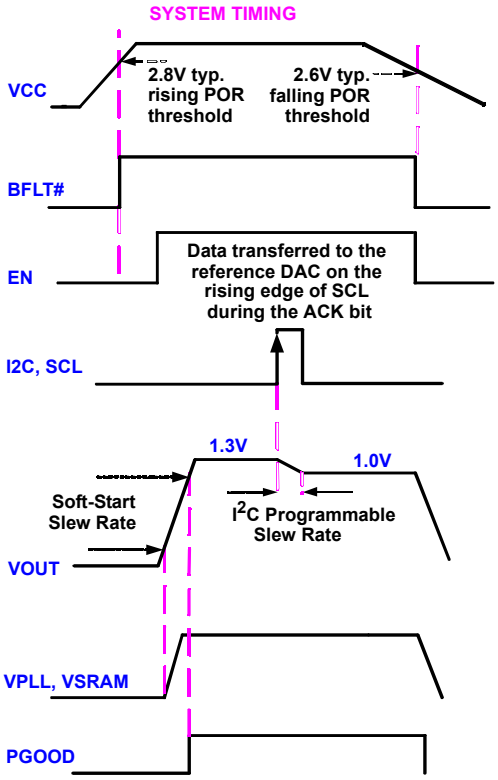


FIGURE 16. SYSTEM TIMIMG DIAGRAM

TABLE 2. SLEW RATE-SET BIT

I²C DATA BYTE								RATE mV/µs
		D5	D4					
X	X	0	0	X	X	X	X	**0.5**
X	X	0	1	X	X	X	X	**1**
X	X	1	0	X	X	X	X	**2.5**
X	X	1	1	X	X	X	X	**5**

Soft-Start and Slew Rate Control

To assure stability and minimize overshoot at start-up and during DVM transitions, the ISL6271 implements a controlled rise time of each regulator output. The Slew Rate control bits in Table 2 are used to route one of 4 current sources to the SOFT pin. These current sources along with the soft-start capacitor will control the rate of rise of voltage during DVM transitions. The recommended 10nF soft-start capacitor will result in a typical slew rate of 1mV/µs at start-up and the programmable DVM slew rates defined in Table 2. Slower or faster start-up and DVM transactions can be accommodated by selecting a smaller or larger soft-start capacitor. By default bits D5 and D4 are set to “01” corresponding to a SS current of 10µA. Writing “00” will result in a 5µA of current whereas “10” corresponds to 25µA and “11” corresponds to a typical source current of 47µA. The expression i = cdv/dt can be used to solve for the appropriate slew rate.

Example: Desired slew rate = 10mV/µs fixed slew rate and the slew rate control bits are set to “11”. Then:

Isource = I_{11}= 47nA (nominal), therefore

$$C = \frac{Isource}{\frac{dv}{dt}} = \frac{47nA}{\frac{10mV}{u}} = 4.7nF \quad \text{(EQ. 1)}$$

NOTE: Intel specifies a maximum slew rate for Vcore transitions. To satisfy this requirement, the SS capacitor and SOFT pin sink/source current tolerances must be considered. Refer to the Electrical Specification table and appropriate Intel documents for details. Note that when D5 and D4 are set to “11” the maximum source current is 69nA. Under this condition, the slew rate would be 17.3mV/µs if a 4.7nF SS capacitor varied by 15% negative. For this reason a 6.8nF capacitor is recommended when D5 and D4 are set to “11”.

Undervoltage and Overvoltage on VOUT

If the output voltage of the switching regulator exceeds 112% of the SOFT pin voltage (programmed DAC voltage) for longer than 1.5µs, an overvoltage fault will be tripped and the phase node will be three-stated. Hysteresis requires the voltage to fall to 106% before the fault is automatically reset.

An undervoltage occurs when the output voltage falls below 88% of SOFT pin voltage. Once this fault is triggered, hysteresis sets the reset point to 90%. An undervoltage condition will occur if the output DC current plus the ripple exceeds the current limit point for a period longer than the output capacitance hold-up time.

Loop Compensation

All three regulators are internally compensated for stability; however, an external resistor connected between the core regulator output and the FB pin can be used to alter the closed loop gain of the switching regulator and optimize transient response for a given output filter selection. The following combinations of component values are recommended:

TABLE 3. RECOMMENDED KEY COMPONENT VALUES FOR CORE REGULATOR

LO	COUT	RCOMP
3.3µH	4.7µF	100kΩ
4.7µH	10µF	50kΩ

Overcurrent Limit

To protect against an overcurrent condition, the core regulator employs a proprietary current sensing circuit that monitors the voltage drop across the internal upper MOSFET. When an overcurrent condition is detected the controller will limit the output current and if the condition persists the output voltage level will drop below the undervoltage level tripping the PGOOD indicator. See “Applications section” for details.

SRAM and PLL LDOs

The two linear regulators on the ISL6271 are designed to satisfy the power requirements of the SRAM and phase-lock loop circuitry internal to XScale processors. These regulators share a common input voltage pin (LVCC) that can be tied to the main battery PVCC or preferably to a lower system voltage to effect a higher conversion efficiency. It is recommended that LVCC be connected to a pre-regulated voltages between 1.8V - 2.5V.

Each LDO is internally compensated and designed to operate with a low-ESR ceramic capacitors (X5R or better) between 2.2µF and 3.3µF. Both LDOs have overcurrent, undervoltage and thermal protection and share a common enable signal (EN) with the core regulator, allowing them to be enabled/disabled together as required by the processor.

BFLT#

The logic state of the BFLT# output indicates whether the main battery input is adequate to power the system in normal operation. A battery low (or absent) condition is indicated by this pin being pulled low. Upon initial application of battery power, it will indicate a battery good condition when the battery voltage is greater than 2.8V (nominal), and it will sustain the battery good indication until the voltage drops below 2.6V (nominal). The output is pulled actively low, with no main battery connected by tapping power from the secondary input, BBAT. It is actively driven to BBAT when the main battery is within the POR thresholds.

BBAT

The BBAT pin is an input voltage to the ISL6271 that supports the BFLT# indicator function as described above. When the main battery is absent, or of inadequate potential, the BBAT input voltage supplies power to support the BFLT# indicator. The input voltage must be between 2.25V and 3.75V for proper operation and is typically supplied from the system back-up battery. The maximum current drain from the BBAT pin is 0.1µA.

PGOOD

PGOOD is an open-drain output that indicates the status of the three regulators (VOUT, VSRAM, VPLL). This output is held low until all outputs are within their specified voltage tolerance. As soon as outputs are in regulation, the output is released and pulled high by an external resistor tied to a compliant system voltage. This output can be AND'd with other system power-good indicators that also have open-drain outputs. Note that this is not a latched output and under a soft short condition on any of the regulators it is possible to see this pin oscillate at a frequency proportional to the fault current level and the fault monitoring hysteresis internal to the ISL6271 regulator.

Phase Node Damping Circuit

To enhance system reliability and minimize radiated emission, the ISL6271 implements an anti-ringing, phase node snubber while operating in diode emulation. The active snubber places a 50Ω (nominal) resistor across the output inductor when the low side synchronous rectifier is turned off to prevent reverse current.

Inter-IC Communications

Communication between the host processor and the ISL6271 takes place over a two-wire I^2C interface. The bus consists of one bidirectional signal line, SDA (data) and a clock pin input, SCL generated by the bus master. Both pins are pulled-high to a system voltage with external pull-up resistors. A typical pull-up resistor value for a single master/slave interface operating in normal mode is 5kΩ.

See the Phillips specification listed in the reference section for specific details on the selection of the pull-up resistor. The bus supports both standard mode and fast mode data rates as defined by the Phillips protocol. A typical I^2C transmission is illustrated in Figure 17. When the bus-resident master (processor) wants to communicate with a bus-resident slave (ISL6271), it will pull the SDA line low while the SCL line is still high. This signals a "start" condition. It will then clock the address of the desired slave device at a rate of one bit per clock cycle. The address is embedded in the first seven bits of the first byte transfer, with the eighth bit giving the directional information (Read/Write) for the next byte of information. When the slave detects an address match, it will hold the SDA line low during the ninth clock pulse to acknowledge a match (ACK). If the direction bit indicates a "write" (send) byte, the slave will receive the byte clocked in by the master and will give an "acknowledge" by again pulling the SDA line low during the ninth clock cycle. The master then can either terminate transmission by issuing a "stop" bit, or continue to transfer successive bytes until complete.

Multiple successive bytes can be transferred with only an acknowledge bit separating them until a "stop" or repeated "start" signal is given by the master. The data embedded in the byte is latched into its appropriate register(s) on the rising edge of the SCL during the acknowledge pulse and is applied to the ISL6271 DAC. The internal DAC on the ISL6271 converts the 4 bit digital input as defined in Table 1 into the reference voltage of the core regulator error amplifier.

If the master issues a 'read' command to the ISL6271, to verify the contents of the internal registers, the device will place the byte on the bus to be clocked in by the master. After the host master receives the byte, the cycle is terminated by a "NOT acknowledge" signal, and a 'stop' bit. A 'stop' is generated by releasing the SDA line to pull high during a high state on the SCL line.

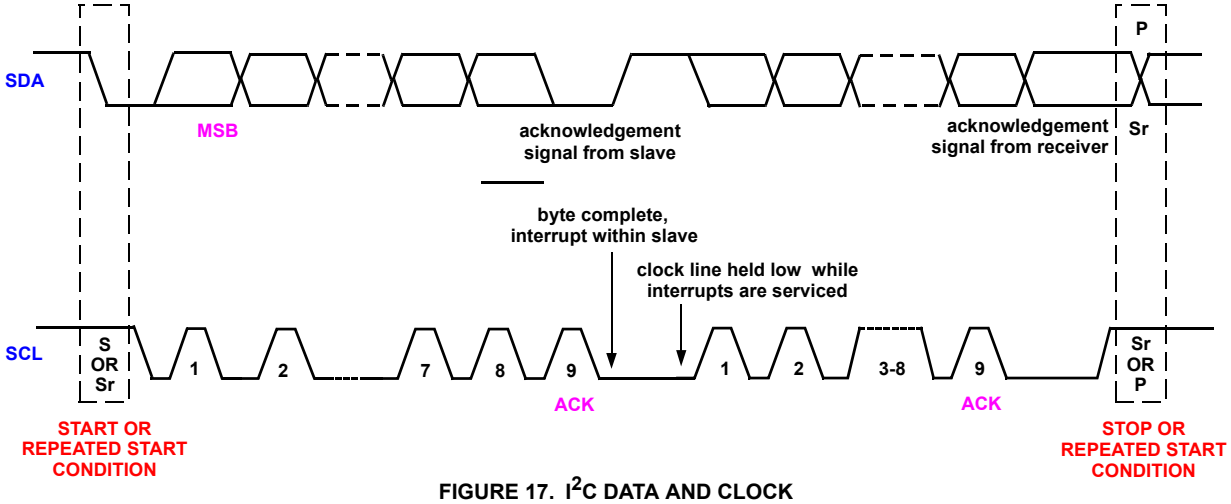


FIGURE 17. I^2C DATA AND CLOCK

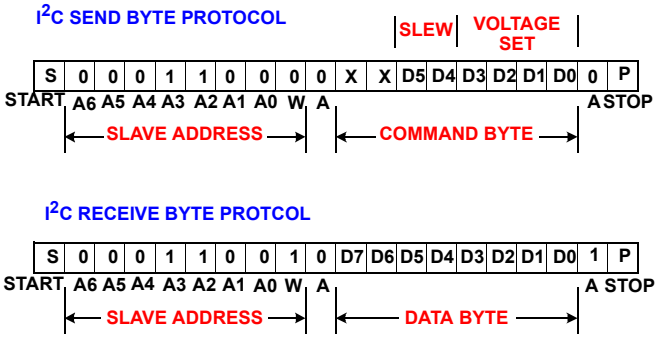


FIGURE 18. INTERFACE BIT DEFINITION AND PROTOCOL

VID and Slew Rate Program Register

In a typical XScale configuration, the processor's "Power Manager" will issue the voltage and slew rate commands to the ISL6271 over it's PWR_ I^2C bus after the ISL6271 acknowledges its address. The data byte is composed of two pieces of 'set' information: The prescribed voltage level embedded in bits D0-D3, and the prescribed transition slew rate (from the previous voltage to the target voltage) embedded in bits D4-D5. Each set of bits is transmitted MSB first. This protocol is depicted in Figure 19.

Application Guidelines

Every effort should be made to place the ISL6271 as close as possible to the processor, with the orientation favoring the shortest voltage routing. The regulator input capacitors should be located close to their respective input pins.

All output capacitors should be kept close to their respective output pins with the ground pins connected immediately to the ground plane. Care should be taken to avoid routing sensitive, high impedance signals near the PHASE pin on the controller, and the attendant PCB traces

To minimize switching noise, it is important to keep the loop area associated with the phase node and output filter as short as possible. It is also important that the input voltage decoupling capacitor C7 be located as close to the PVCC pin as possible and that it has a low impedance return path to the PGND pin. In general a good approach to layout is to consider how switching current flows in a circuit, and to minimize the loop area associated with this current. In the case of the switching regulator, current flows from C7 through the internal upper P-MOSFET, to the load through the output filter and back to the PGND pin. *To maximize the effectiveness of any decoupling capacitor, minimize the parasitic inductance between the capacitor and the circuit it is decoupling.* Notice that Figure 19 illustrates the SIGNAL ground with RED highlighting. All components associated with these terminals should be tied together first. Be sure to make only one connection between this net and the PGND pin to avoid ground loops and noise injection points into sensitive analog circuitry.

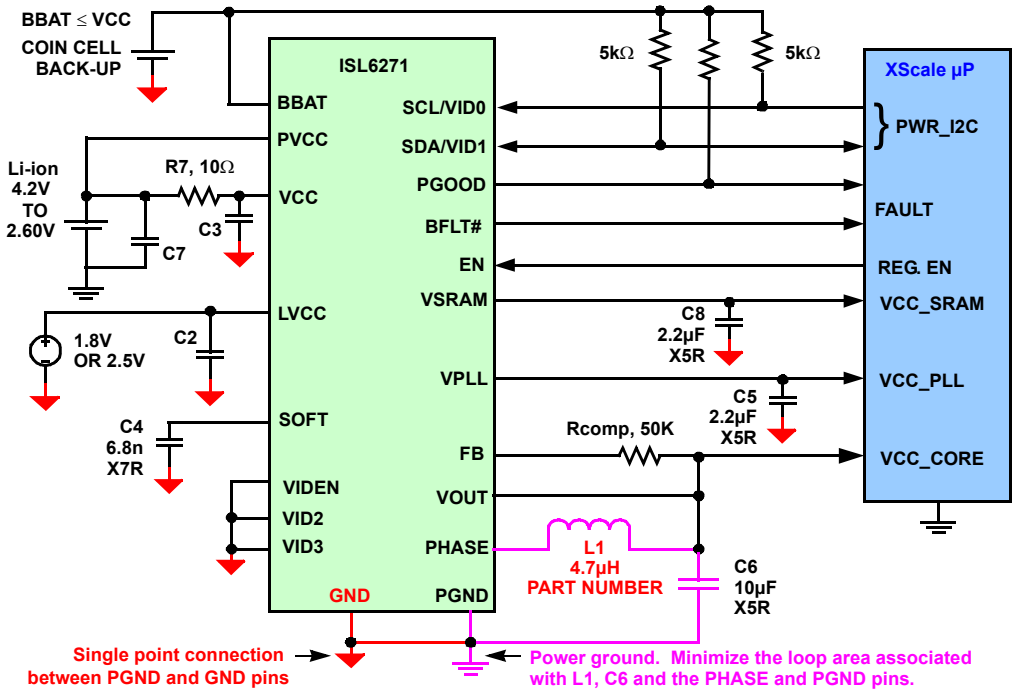


FIGURE 19. TYPICAL APPLICATION CIRCUIT

Loop stability calculations are simplified when using the ISL6271 and are limited to the selection of a single feedback resistor, Rcomp. The Rcomp resistor will affect the closed loop gain of the internal compensation network as in Equation 1. Empirical and theoretical testing suggests that a value of 50K will provide the most ideal transient response to the expected XScale load and voltage transitions when used with the recommended 4.7µH output inductor and 10µF output capacitor. Using the ISL6271 evaluation board, a 50K feedback resistor resulted in a minimum of 60 degrees of phase margin under worst case line and load transitions. When placing the Rcomp feedback resistor be sure to avoid routing it parallel to switching circuits especially the phase node, that could otherwise induce noise into the FB pin.

$$Gcomp = \frac{(Rc \bullet Cc \bullet s + 1)}{Rcomp \bullet Cc \bullet s} \quad \text{(EQ. 2)}$$

Overcurrent Protection and Ripple Current

The OCL trip level inside the ISL6271 is a function of the upper PMOS output transistor's on-resistance and overcurrent comparator threshold voltage. The device was designed to accommodate a maximum RMS current of 470mA, and to accommodate this DC current level plus the associated ripple current, the OC limit of the ISL6271 will not trip below 600mA. Ripple current inside the ISL6271 is defined by the expression,

$$Iripple = \frac{(Vin - Vout)}{L \bullet fs} \bullet \frac{Vout}{Vin} \quad \text{(EQ. 3)}$$

where *"fs"* is the switching frequency of the converter. The architecture of the ISL6271 is such that the switching frequency will increase with higher input voltage. This behavior attempts to keep the ripple current constant for a given output inductor, input voltage and output voltage. To minimize ripple current and preserve transient response, Intersil recommends an output inductor between 3.3µH and 4.7µH. Higher values of inductance will minimize the risk of tripling the overcurrent minimum threshold of 600mA.

SSR Theoretical Operation

The ISL6271 is a PWM controller that uses a novel architecture developed by Intersil called *Synthetic Ripple Regulation*. The architecture operates similar to a hysteretic converter without the deficiencies and noise sensitivities. Reduced to its simplest form, the Synthetic Ripple Regulator inside the ISL6271 is made up of three elements as illustrated in Figure 20: A transconductance amplifier (Rippler Amplifier), a window comparator with hysteresis and an Error Amplifier. While operating in continuous conduction mode, the converter has a natural switching frequency of 1.2MHz delivering an ultra low output voltage ripple and exceptional transient response as illustrated in Figures 23 and 24.

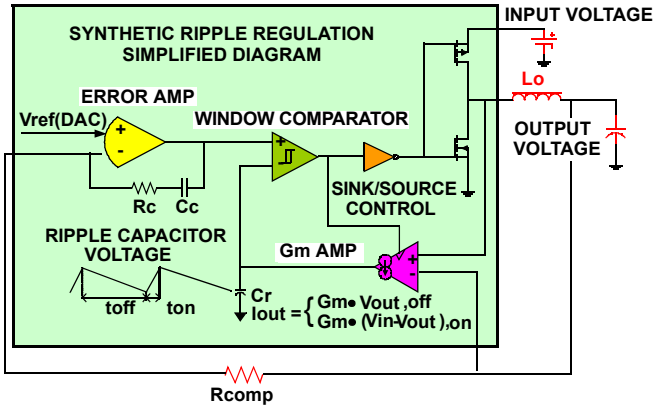


FIGURE 20. SIMPLIFIED SRR DIAGRAM

Figure 20 illustrates the two control loops inherent to the SRR architecture. The inner loop consists of the ripple amplifier, the window comparator, gate drive circuitry and the power stage. The outer loop controls the inner loop and is made up a high bandwidth error amplifier with internal and external compensation.

CCM Operation - Heavy Current

Figure 21 illustrates the SSR in CCM. When the upper P-MOSFET is turned on, the phase voltage equals the input voltage and the ripple transconductance amplifier outputs a current proportional to the difference of the input and output voltage. This current will ramp the voltage on the ripple capacitor Cr in Figure 21. As this voltage reaches the upper threshold of the hysteretic comparator, the comparator output will switch low. After a propagation delay, the upper P-MOSFET is turned off and the lower N-MOSFET is turned on, forcing synchronous rectification. At this point, the ripple amplifier now has inputs of 0V and VOUT and will sink current to discharge the ripple capacitor. When the voltage across the ripple capacitor reaches the lower threshold of the hysteresis window, the window comparator outputs a high signal. After a propagation delay, the upper P-MOSFET turns on, repeating the previous switching cycle.

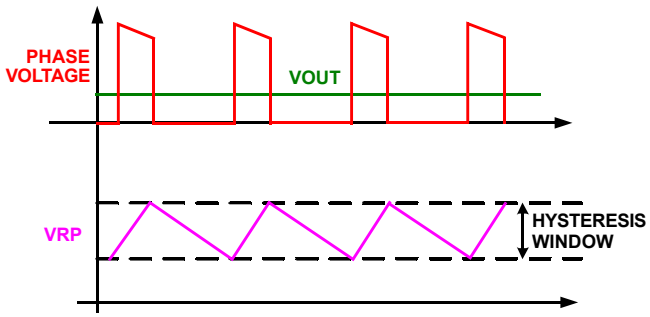


FIGURE 21. SYNTHETIC RIPPLE REGULATION IN CCM

Light Load Operation - DCM

A light load is defined when the output inductor ripple current reaches zero before the next switching cycle. Under this condition, the ISL6271 synchronous rectifier will turn off emulating a diode to prevent negative inductor current. As explained below, the switching frequency and losses associated with turning on the synchronous rectifier will be reduced to enhance the low current efficiency. The top waveform in Figure 22 shows the phase voltage in DCM. The middle waveforms include the error amplifier voltage, ripple capacitor voltage and the boundaries of the hysteresis comparator which track the EA output. The waveform at the bottom is representative of the inductor current. Notice that in a switching cycle the inductor current rises as the upper P-MOSFET turns on, falls when the lower N-MOSFET turns on, and stays at zero after the current reaches zero as a result of diode emulation.

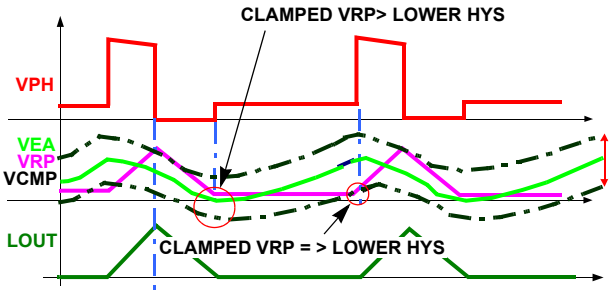


FIGURE 22. SRR IN DCM

To understand the ISL6271 light load operation, look carefully at the waveforms in the middle of Figure 22. Notice that the voltage across the ripple capacitor, VRP, has a minimum clamp voltage (typically 0.4V), and that the Error Amplifier can go below this voltage (typically clamped to 0.2V). In DCM, the voltage across ripple capacitor will be discharged each cycle to the clamp voltage. While the lower hysteresis is below this voltage, the ripple capacitor will remain clamped keeping the upper P-MOSFET off. As the EA voltage increases, so too, will the lower threshold of the hysteresis window until it reaches the ripple capacitor clamp voltage (VCLMP). At this point, the upper FET will be enabled and will turn on. The lighter the load, the lower the error amplifier output is, and the longer the ripple capacitor voltage stays at the VCLMP voltage. This results in a phase node switching frequency that is proportional to load current (that is, lower switching losses and higher efficiency at lighter loads). In DCM the switching frequency will be lower than in a heavy load, CCM.

A load transition from full load to no load will result in a finite period of time during which the error amplifier settles to a new steady state condition. As illustrated in Figure 23, the SSR architecture inherent to the ISL6271 responds within 6µs of the mode change, slewing the error amplifier output below the clamped ripple capacitor voltage and preventing the upper FET from turning on. Prior to reaching the new stability point, the phase node applies four phase pulses before the controller forces the output voltage to the prescribed regulation point. Once the output falls below the reference voltage the controller then pumps up the output voltage and enters its steady state DCM. Mode changes that take the converter from CCM into DCM will have much higher output voltage spike than a load step that remains in CCM. Compared with competitive solutions the ISL6271 responds very well during this severe mode change and it is more than sufficient to meet Vcore tolerance specifications as required by Intel.

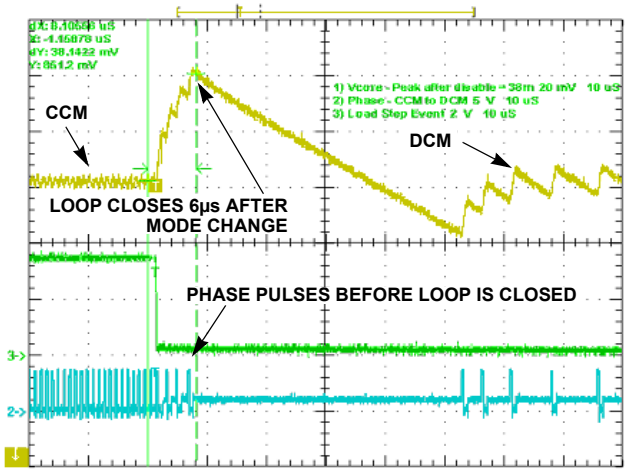


FIGURE 23. CCM TO DCM MODE

NOTE: Note that the peak voltage in Figure 23 is only 38mV, or less than one VID code transition above the reference set-point.

TRANSITION BETWEEN LIGHT LOAD AND HEAVY LOAD

Unlike most control topologies that require two sets of circuits to control the light and heavy load operation, the SRR control naturally switches between heavy and light load with the same control circuit. As the load gets lighter, the feedback forces the error amplifier output to a lower voltage and when the lower threshold of the hysteresis window is lower than VCLMP, light load operation begins. The scope shot in Figure 24 illustrates a mode transition from a DCM (10mA load current) to CCM (170mA) with trace 4 (GRN) being the command pulse that initiates the mode change. Prior to the load step, and while the converter is in DCM, the ripple voltage is approximately 10mV and the ripple frequency is 125kHz. In CCM, the converter operates at a frequency of approximately 10X that of DCM and the ripple is reduced by more than a factor of two.

Measured Core Voltage Conversion Efficiency

The actual efficiency of the ISL6271 switching regulator is illustrated in Figure 3 from 10mA to 500mA, and at two important input voltages. The first, 3.0V, is typical of a Li-ion End Of Charge (EOC) battery voltage. The second, 3.6V, is typical of the “plateau voltage” where most of the battery energy is available. Once a Li-ion battery reaches 3.0V, there is very little energy left in the battery and discharging it significantly below this point can compromise the number of charge cycles the battery will accept. Recall that the 2.76V falling POR threshold on the ISL6271 acts to prevent a deep discharge condition from occurring. The efficiency curves in Figure 3 were taken at room temperature using the ISL6271 evaluation board. The output inductor used is an ultralow profile, drumcore device with a DCR of 100mΩ.

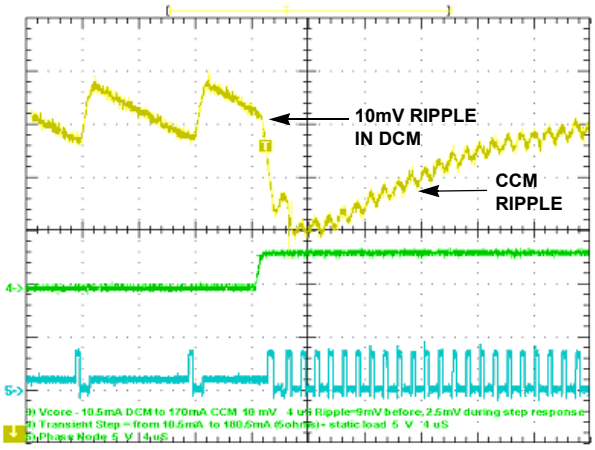


FIGURE 24. DCM TO CCM MODE TRANSITION

Thermal Management

Although the ISL6271 is characteristically a low heat generator, it will generate some heat as a result of the inefficiencies in power conversion. The worst-case internal power dissipation should be less than 170mW translating into a 7°C rise in junction temperature above ambient. If the temperature of the chip does exceed 150° ±10°C as a result of a high ambient temperature, the controller will disable the outputs until the temperature decreases by 45°C.

Powering Intel XScale Processors

Intel identifies ten power domains required for powering XScale processors. Of these ten power domains or voltages, many may be strapped together as in Figure 25 and supplied by a single regulator. These voltages however must be applied systematically to the processor and two pins, SYS_EN and PWR_EN facilitate this power sequence. The PWR_EN pin is dedicated to enabling the CORE, PLL and SRAM power domains and should be connected to the ISL6271 enable pin. The SYS_EN pin is responsible for enabling the system regulator. Figure 27 illustrates one possible configuration using the Intersil EL7536 to power five of the 10 domains.

NOTE: Intel warns that an improper power sequence can damage the processor. Refer to the appropriate Intel applications material to ensure proper voltage sequencing.

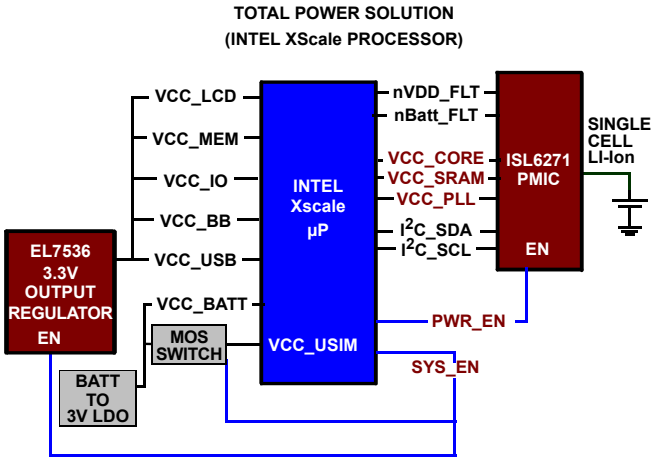


FIGURE 25. XSCALE POWER DOMAINS

Design Notes

Refer to Table 3, "RECOMMENDED KEY COMPONENT VALUES FOR CORE REGULATOR".

1. Do not leave pins VID2(5) or pin VID3(6) floating when using the I^2C bus. Tie these pins to GND (16).
2. Make sure that load current on VOUT returns to the pin (7) (PGND). Pin 16 (GND) functions as a quiet return for the LVCC loads. It is internally tied to the device substrate (pin 21). Tie Pin 16 to Pin 7 at a single point as in Figure 19.
3. Select the output capacitor for VSRAM and VPLL as follows: 2.2µF<C8, C5<4.7µF, X5R.
4. BFLT# is internally pulled up to BBAT. Do not pull-up to any other external voltage.
5. The I^2C pull-up resistors will affect standby leakage power. A typical value to accommodate the I^2C bus slew rate requirements in “Standard Mode” is 5K.
6. Set the soft-start capacitor to 10nF to implement a 1mV/µs slew rate of the output voltage at start-up. For maximum slew rate, use 6.8nF soft-start capacitor.
7. Tie PGOOD to the XScale nVDD_fault pin.
8. Tie the BFLT# pin to the XScale nBatt_fault pin. The BFLT# pin is pulled up internally to BBAT. A valid BFLT# state under all conditions can be achieve by connecting BBAT to the system BACK-UP battery. Otherwise, consider the system start-up/shut-down voltage timing to determine what system voltage that BBAT can be tied to that will ensure the correct BFLT# operation. Current drain on BBAT is much less than 1µA.
9. It is a good design practice to isolate PVCC from VCC with a low pass filter (LPF) made up of a 10Ω resistor and 1µF ceramic capacitor. Ensure that VCC is kept within 0.1V of PVCC to avoid turning on internal protection diodes.

Internal ESD Structures

The ISL6271 input/output pins are protected from overvoltage conditions by clamping the pin to one diode drop above or below the VCC voltage rail. During shutdown it is possible that the SDA and SCL pins have a voltage greater than VCC. Under this condition, the ESD diodes will provide a reverse current path to circuitry on VCC that can act as a load on the back-up battery. To avoid this condition interrupt VCC from external circuitry if a voltage greater than VCC is expected on any of the pins identified below.

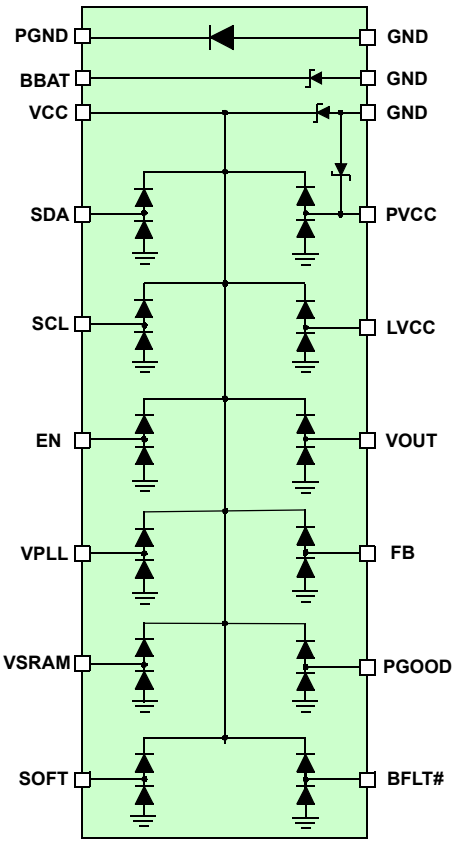


FIGURE 26. INTERNAL ESD STRUCTURES

Layout Recommendation

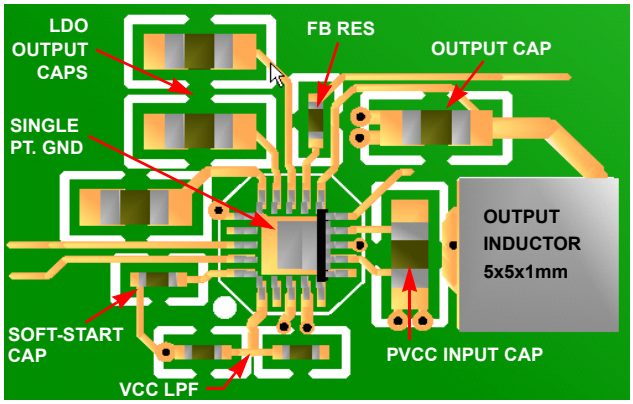


FIGURE 27. COMPONENT PLACEMENT AND TOP COPPER

Since the ISL6271 can operate at a high switching frequency, it is especially important to apply good layout practices. Decoupling of the regulator's input voltage (PVCC) and minimizing the loop area associated with the phase node output filter is essential for reliable operation. Return currents from the load should find a low impedance path to the PGND pin on the IC (Pin 8). Ideally, the core voltage would be distributed to the embedded processor on a low impedance power plane; however, a 30-50mil, short trace should be sufficient. When implementing DVM it is important to minimize inductance between the load and the output filter. The processors can command slew rates of up to 200mA/ns and local decoupling at the processor socket is essential to satisfying this requirement.

References

[1] ISL6292 data sheet - Battery Charger

[2] EL7536 data sheet - System Regulator

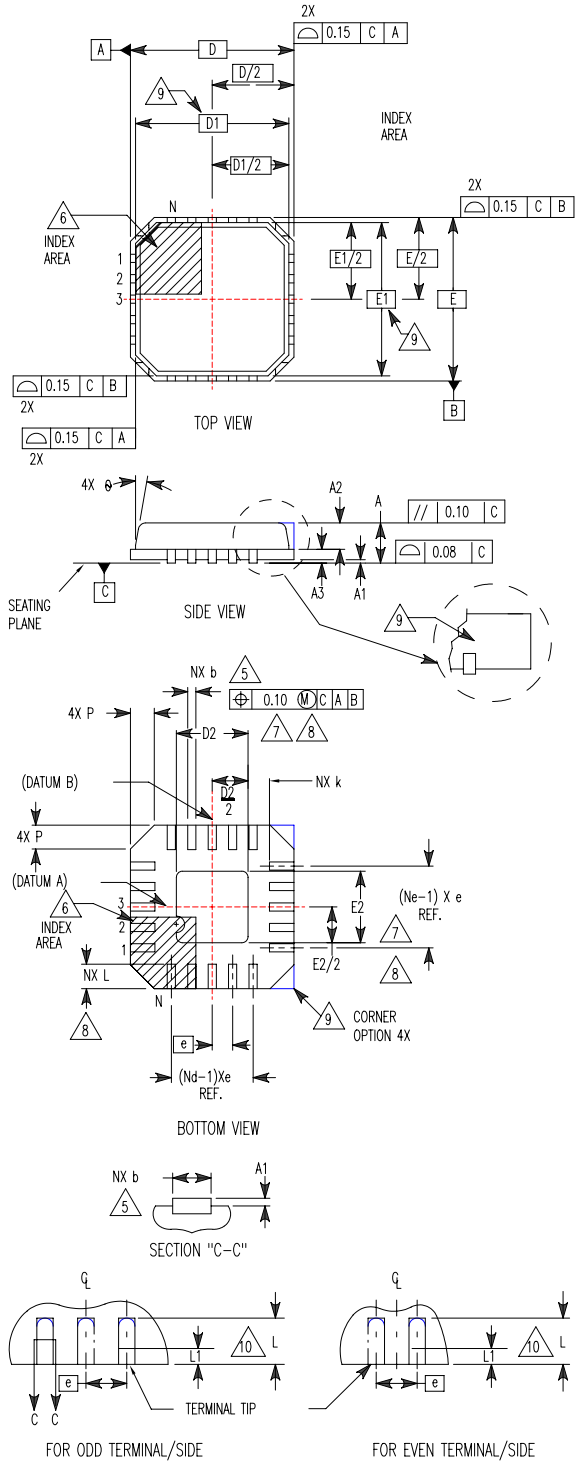
[3] C-Code examples for PWR_I2C bus communication - Intersil support documentation available upon request.

[4] PHILLIPS I^2C BUS Specification

[5] http://www.semiconductors.philips.com/buses/i2c/

[6] Technical Brief TB389 "*PCB Land Pattern Design and Surface Mount Guidelines for MLF Packages*"

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.4x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne	5	5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.