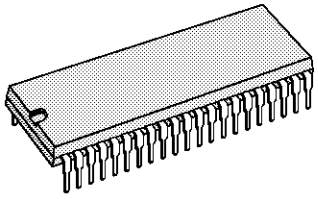
SGS-THOMSON MICROELECTRONICS

TDA8204

NICAM DECODER

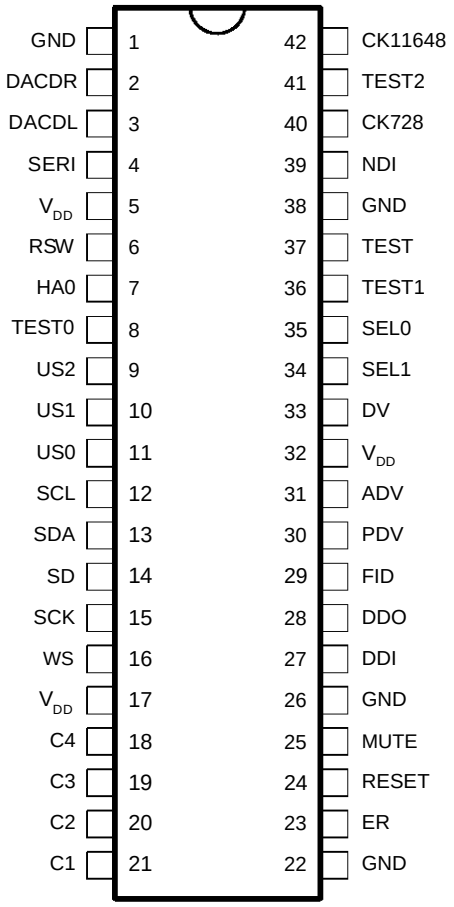
- HIGHLY INTEGRATED TWO-CHIP SOLUTION FOR NICAM DEMODULATION (using TDA8205 QSPK)
- DATA AND SOUND RECOVERY ACCORDING TO EBU SPB 424 SPECIFICATIONS
- I^2S INTERFACE FOR DIGITAL AUDIO PURPOSES (14-bit samples, 32kHz word select clock, 896kHz serial clock)
- 4 TIMES UP SAMPLING DIGITAL FILTER AND NOISE SHAPER
- I^2C INTERFACE FOR MICROCONTROLLER SOFTWARE DRIVE
- PAY TV APPLICATION CAPABILITIES
- AUTOMATIC ERROR MONITORING (programmable error rate limit)



SHRINK 42
(Plastic Package)

ORDER CODE : TDA8204

PIN CONNECTIONS



8204-01.EPS

DESCRIPTION

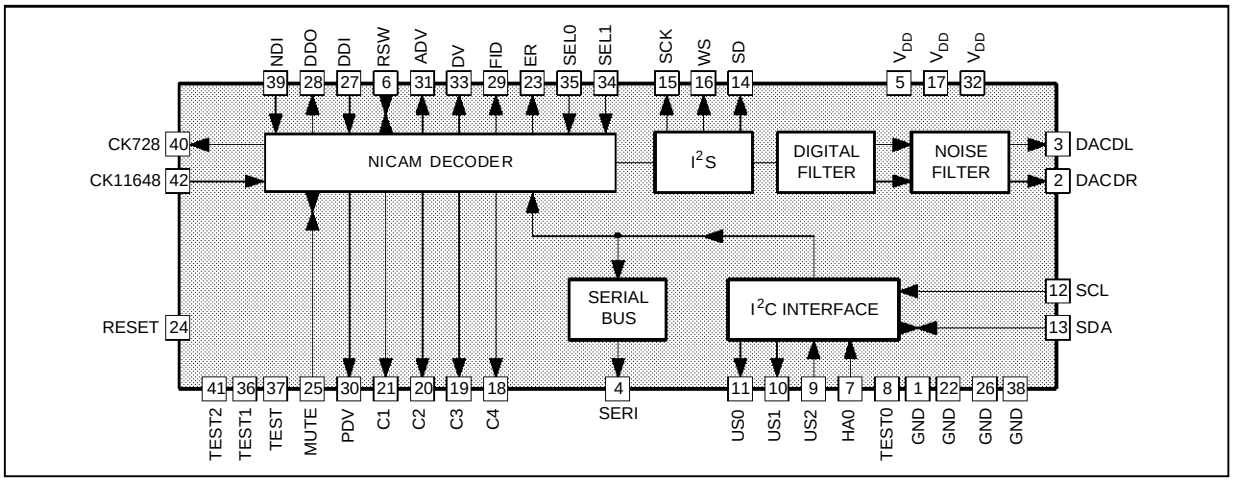
The TDA8204 performs two main functions, first one is NICAM decoding, second one is audio signal recovery (DAC) combined with audio signal switching (Matrix). An I^2S output is provided for digital audio when required and all functions of both the TDA8204 and the TDA8205 are accessed via an on-chip I^2C bus interface. The I^2S interface can be used as an input for converting to analog some I^2S digital sound.

PIN ASSIGMENT

Pin N°	PIn Name	Function	Pin N°	Pin Name	Function
1	GND	Ground	22	GND	Ground
2	DACDR	PWM Data Output Right	23	ER	Error Monitor Flag Output
3	DACDL	PWM Data Output Left	24	RESET	Reset
4	SERI	Inter Chip Serial Bus Output	25	MUTE	NICAM Mute
5	V_{DD}	+5V Supply	26	GND	Ground
6	RSW	Reserve Sound Switch Status/Control	27	DDI	Descrambled Data Input
7	HA0	Hardware Address Selection	28	DDO	Descrambled Data Output
8	TEST0	To be connected to V_{DD} or GND	29	FID	Frame Identification Flag Output
9	US2	User bit 2 (input)	30	PDV	Parity Data Valid Flag Output
10	US1	User bit 1 (output)	31	ADV	Additional Data Valid Flag Output
11	US0	User bit 0 (output)	32	V_{DD}	+5V Supply
12	SCL	I^2C Bus Clock	33	DV	Data Valid Flag Output
13	SDA	I^2C Bus Data	34	SEL1	Language Selection 1 Input
14	SD	I^2S Bus Data	35	SEL0	Language Selection 0 Input
15	SCK	I^2S Bus Clock	36	TEST1	Not to be connected
16	WS	I^2S Bus Word Select	37	TEST	To be connected to GND
17	V_{DD}	+5V Supply	38	GND	Ground
18	C4	Application Control Bit 4 Flag	39	NDI	NICAM Data Input
19	C3	Application Control Bit 3 Flag	40	CK728	728kHz bit Clock Output
20	C2	Application Control Bit 2 Flag	41	TEST2	Not to be connected
21	C1	Application Control Bit 1 Flag	42	CK11648	11.648MHz bit Clock Input

8204-01.TBL

BLOCK DIAGRAM



8204-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	7	V
P_{tot}	Total Power Dissipation	1.2	W
T_{oper}	Operating Temperature Range	0, + 70	°C
T_{stg}	Storage Temperature Range	- 20, + 150	°C

8204-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Juntion-ambient	Max.	67	°C/W

8204-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
V_{DD}	Supply Voltage Range	4.75	5	5.25	V
I_{DD}	Supply Current	30	60	92	mA
OUTPUTS					
DACDR, DACDL, SERI, US1, SCK, WS, C4, ER, DDO, FID, PDV, ADV, DV, CK728					
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 4mA)	0.7 V_{DD}			V
US0 (open drain)					
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
I_{LK}	High Output Current (leakage)			± 2	µA
CONSTANT CURRENT LED DRIVERS C1, C2, C3					
I_{OL}	Low Output Current (V_{OL} = 0.4V)	- 10			mA
INPUTS					
HA0, US2, RESET, DDI, SEL1, SEL0, TEST, NDI, CK11					
V_{IL}	Low Input Voltage			0.8	V
V_{IH}	High Input Voltage	0.6 V_{DD}			V
I_{LK}	Input Leakage Current			± 2	µA
BI-DIRECTIONAL					
	RSW, MUTE				
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High OUtput Voltage (I_{OH} = 100µA)	0.7 V_{DD}			V
V_{IL}	Low Input Voltage			0.8	V
	SD				
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 4mA)	0.7 V_{DD}			V
V_{IL}	Low Input Voltage			0.8	V
V_{IH}	High Input Voltage	0.6 V_{DD}			V
I_{LK}	Input Leakage Current			± 2	µA
I^2C INTERFACE					
	SCL				
V_{IL}	Low Input Voltage	0		1.5	V
V_{IH}	High Input Voltage	3		V_{DD}	V
f_{SCL}	SCL Clock Frequency			100	kHz
t_r, t_f	Input Rise and Fall Times			2	µs
I_{IL}	Input Leakage Current (V_I = 5.5V)			10	µA
C_I	Input Capacitance			7	pF
	SDA				
V_{IL}	Input Low Voltage	0		1.5	V
V_{IH}	Input High Voltage	3		V_{DD}	V
t_r, t_f	Input Rise / Fall Times			2	µs
I_{IL}	Input Leakage Current (V_I = 5.5V with output off)			10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0		0.5	V
t_f	Output Fall Time between 3.0V and 1.0V			200	ns
C_I	Load Capacitance			400	pF

8204-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I^2C BUS TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)				
t_{LOW} t_{HIGH}	Low Period Clock High Period Clock	4 4			µs µs
t_{SU}, d_{AT}	Data Set-up Time	250			ns
t_{HD}, d_{AT}	Data Hold Time	170			ns
t_{SU}, S_{TO}	Stop Set-up Time from Clock High	4			µs
t_{BUF}	Start Set-up Time following a Stop	4			µs
t_{HD}, S_{TA}	Start Hold Time	4			µs
t_{SU}, S_{TA}	Start Set-up Time following Clock Low to High Transition	4			µs

8204-05.TBL

Figure 1 : I^2C Serial Bus Timing

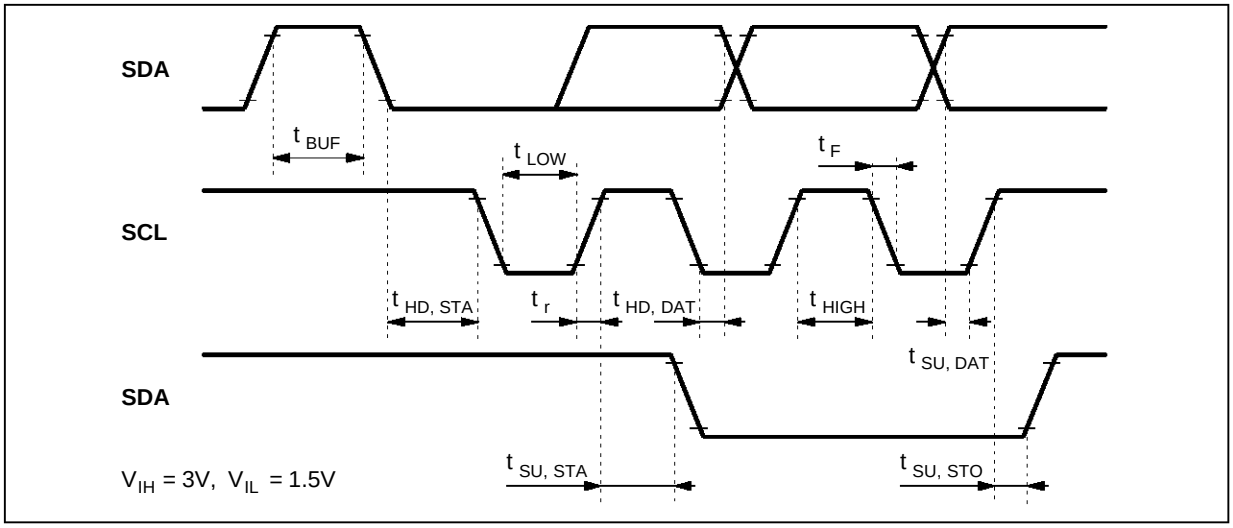


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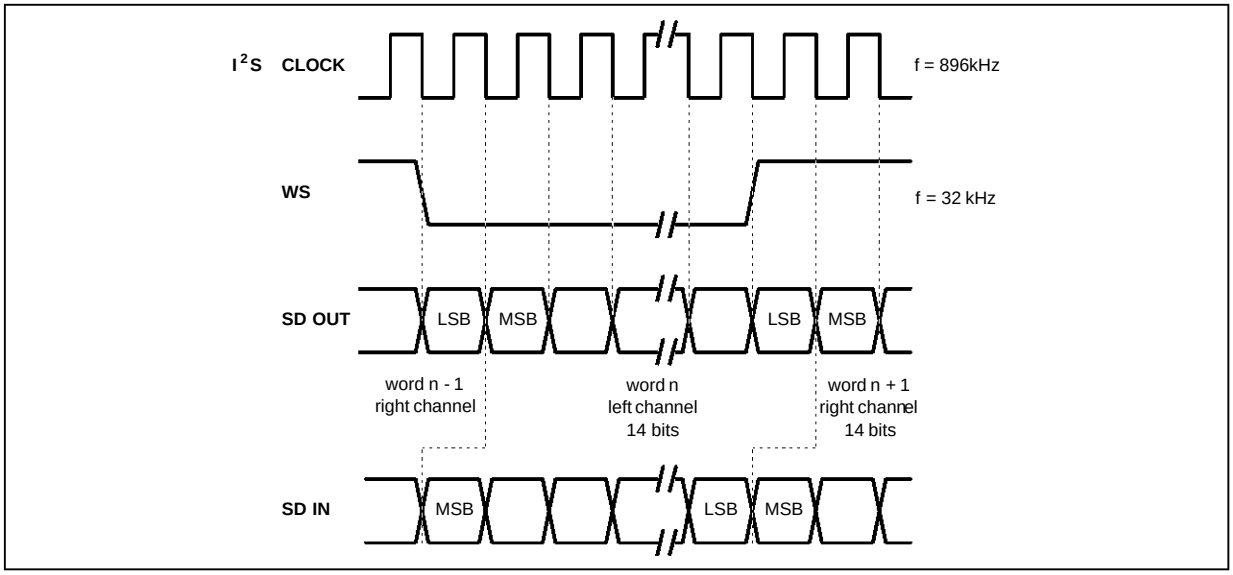
Figure 2 : I^2S Bus Timing Diagram



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FUNCTION DESCRIPTION

The TDA8204 is partitioned into 6 major parts shown in the block diagram.
The NICAM Decoder performs data and sound recovery from the signals specified in EBU SPB 424. The expanded digital audio signals (14-bit) are made available at the digital audio interface (I^2S) in a serial multiplex of left and right channels. They are also processed by a 4 times upsampling digital filter and noise shaper which results in a high speed digital data stream at the output pins DACDL/DACDR. This data stream can be applied to the 1-bit D-A convertors contained in the TDA8205.
The TDA8204 is I^2C bus controlled and provides control over the functions of the TDA8205 by means of a serial inter-chip bus.

1 - NICAM Decoder

1.1 - BLOCK DIAGRAM (see Figure 3)

1.2 - DESCRIPTION

NICAM frame alignment requires searching out a frame alignment word (FAW) and a 16 frame sequence conveyed by C0 bit. Because of noise, interferences, errors in the incoming NICAM Data, aliases of the FAW, a robust scheme is implemented. It ensures the decoder will align, and stay aligned, to signals beyond the limit of maximum useable error rate. Thanks to a 511 bit PRBS synchronized by the recovered clock and a modulo 2 adder, original data are recovered. This data stream can be processed externaly for de-encryption in Pay TV applications using descrambled data Pins DDO, DDI.
To allow simultaneous reading and writing of mono/stereo samples, de-interleaved data frames are stored in a 3 page RAM.

The 10-bit input audio samples are expanded to 14-bit using scale factor bits according to NICAM decoding rules. Samples in error by the parity check are replaced by interpolated one or repeated.

Mute is set according to an error counter when the error rate exceeds error rate limit (ERL) and reset when the error rate is below ERL/4.
Application control information (bit C1, C2, C3, C4) is recovered by majority decision logic over 16 frames. the C1, C2, C3 , C4 bits can be read in SR0 register and are set on the C1, C2, C3, C4 pins according to the state of bit 0 (BEA) of the CR2 register.

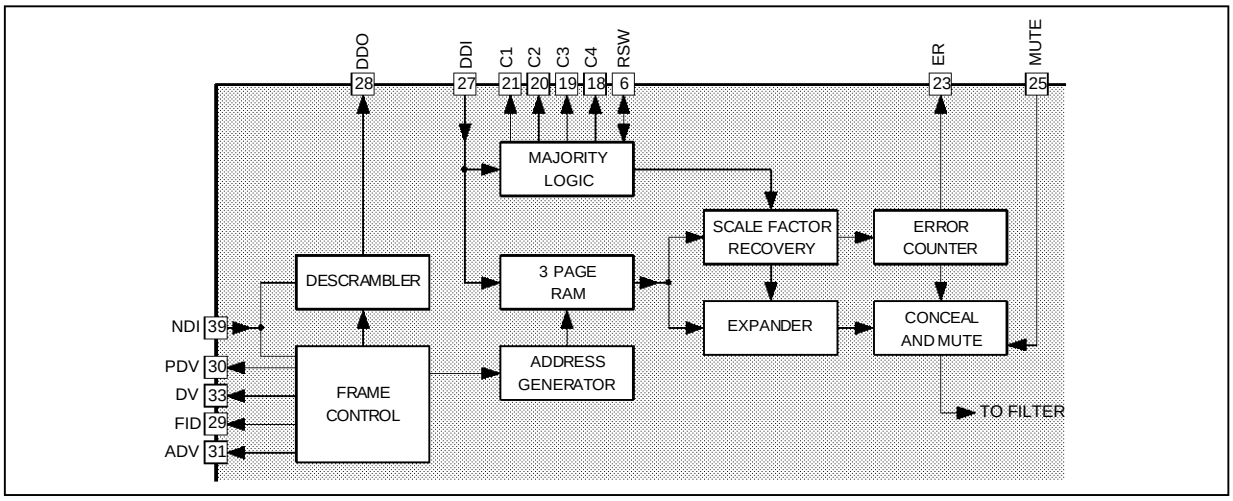
2 - Digital Filter and Noise Shaper

A digital filter performs 4X upsampling in two stages. The main FIR 2x upsampler is followed by a smaller 2x FIR upsampler. Digital upsampling means a much simpler post-DAC reconstruction filter can be used thus saving on external component count and cost.
A noise shaper converts the samples from the digital filter into two high speed serial bitstreams which can be applied to the DACs in the TDA8205.

3 - I^2S Bus

A standard three-wire interface, conforming to the I^2S bus protocol, is provided, allowing connection of an external DAC or DAT interface. Audio samples contain 14-bit, so 16-bit DACs will pad the two LSBs with 0. The word select clock operates at 32kHz and the serial clock at 896kHz.
By setting SDI bit of CR2 to 1, the I^2S interface can receive the digital I^2S sound. This prevents duplicating the dual D/A converter.

Figure 3 : NICAM Decoder Block Diagram



4 - Interchip Bus

A one-line serial bus provides interchip communications allowing control of all functions through the single I^2C bus interface.

5 - I^2C Bus

An I^2C bus interface provides access to control and status registers within the two chips to allow control of their functions and monitoring of status. A digital filter is included to improve noise immunity.

5.1 - DATA FLAGS (see Figure 4)

These indicate the status of the descrambled data on the DDO pin. They are inhibited if the decoder is out of alignement.

- FID : Frame alignment word (scrambled)
- PDV : Parity Data Valid. CIB0 and CIB1 overwrite the first 2 bits of FAW
- ADV : 11 additional data bits
- DV : Data valid (mode dependant)

5.2 - DECRYPTION (see Figure 5)

The PRBS generator (used for descrambling) is normally preset to all ones at the start of each frame. However, it is possible to preset it to any value on each frame by means of a code word clock (CWC) and serial code word data (CWD) interface on pins SEL0 and SEL1.

CWD, which is clocked in on the negative going edges of the CWC clock, can be sent anywhere during the frame except when FID = 1. The CWC is asynchronous with respect to the Nicam clock and the CWD will be used on the following frame. During the time FID = 1, the levels on the SEL0, SEL1 pins are read for language selection. Code words for descrambler presetting may be sent in either an 8-bit or 9-bit formats. There are four possibilities :

- if 7 or less clock cycles are counted on CW-clock during a frame, the PRBS generator is preset to all ones ;
- if 8 clock cycles are counted, 8 bits of CW-data are clocked into the shift register, the first bit of the previous transfer now moving to bit 9 position in the shift register. The resulting value is used to preset the PRBS generator on the next frame.
- if 9 clock cycles are counted, the CW-data (which has been clocked into a 9-bit shift register) is used to preset the PRBS generator on the next frame.
- if 10 or more clock cycles are counted, only the first 9 bits of the CW-data are used and loaded into the PRBS generator on the next frame.

Figure 4 : Data Flags

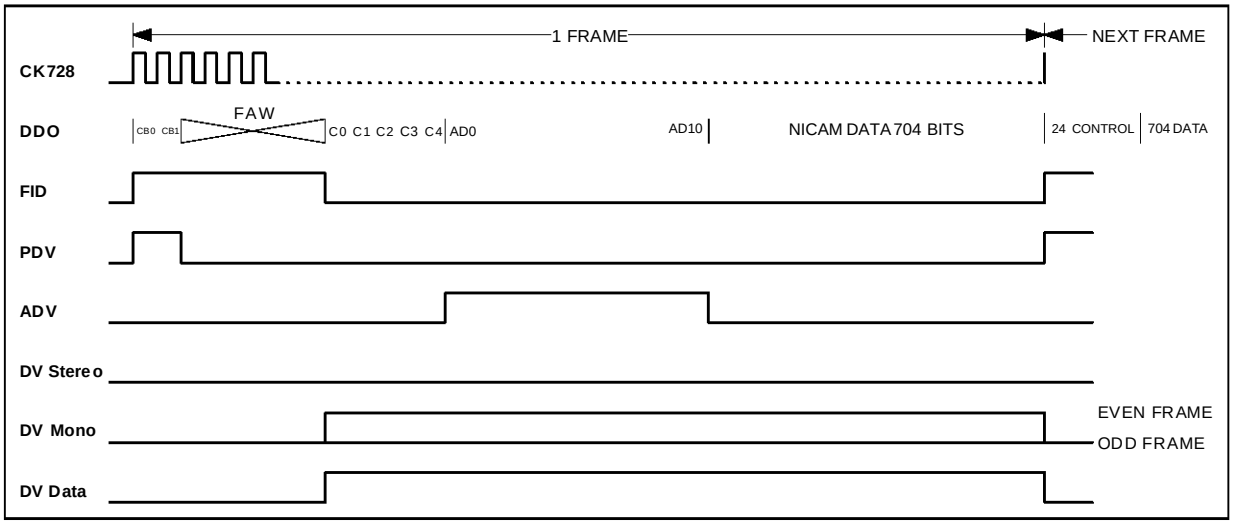
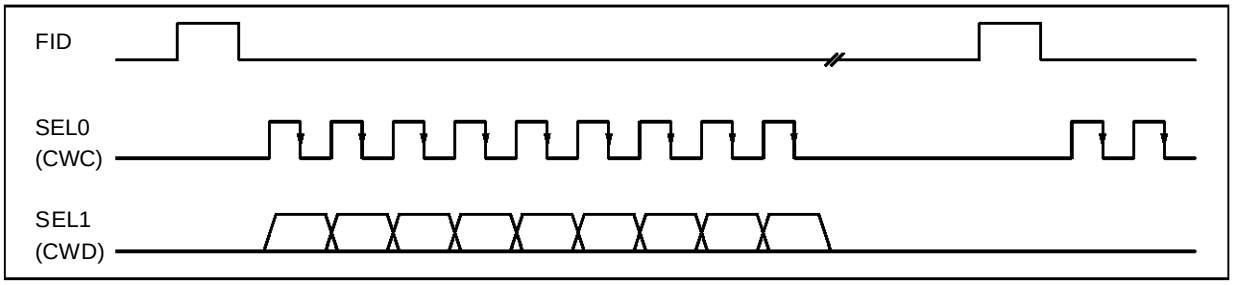


Figure 5 : PRBS Presetter



5.3 - SOFTWARE SPECIFICATION

Software control of IC's is given by programming four registers, one read only status register (SR0) and three read and write control registers (CR1, CR2, CR3).

Transmit format : S = Start, A = Acknowledge
P = stop

S	CHIP ADDRESS	0	A	REG SUB ADDRESS	A	DATA	A	P

Receive format :

S	CHIP ADDRESS	1	A	SR0 DATA	A	CR1 DATA	A	P

Note : All registers are read sequentially; device status and the contents of all registers may be read. The sequence may be terminated by not acknowledging (NOACK) the slave.

Chip address

1	0	1	1	0	1	HAO	R/$\overline{W}$

MSB LSB

HAO : Hardware address selection pin

Register addresses

Reg. Name	Sub Adress								Function
SR0	0	0	0	0	0	0	0	0	NICAM status
CR1	0	0	0	0	0	0	0	1	Matrix and mutes
CR2	0	0	0	0	0	0	1	0	NICAM control
CR3	0	0	0	0	0	0	1	1	Switches

Register contents

SR0 : NICAM status (read only)

US2	C1	C2	C3	C4	MUT	LA2	L/S
US2	0	0	0	1	1	1	1

MSB LSB

L/S :
- If FN1 bit of CR2 is 0, LS bit is loss of frame alignment status
  LS =1, FAW is lost
  LS = 0 FAW is identified
- If FN1 bit of CR2 is 1, LS bit is selected system status
  LS = 1, B/G standard
  LS = 0, I standard

LA2 : Loss of sub-frame alignment (1 = loss of alignment)
MUT : NICAM mute (1 = DAC outputs muted)
C4 : Reserve sound flag (1 = FM backup)
C3 : Application control bit 3
C2 : Application control bit 2
C1 : Application control bit 1
US2 : User bit 2 (input)
US2 bit indicates the state of US2 input Pin

CR1 : Matrix and mutes (read and write register)

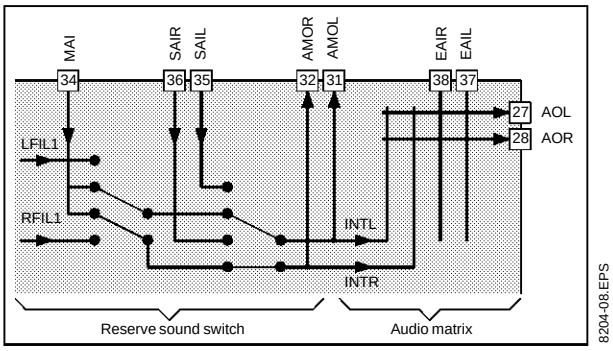
Q1	Q0	I2	I1	I0	G0	AUM	FRE
0	0	0	0	0	0	0	0

MSB LSB

Qn : Output select (see tables)
In : Input select (see tables)
G0 : Auxiliary output gain, 0 = 0dB, 1 = 6dB
AUM : Auxiliary output mute, 0 = no-mute, 1 = muted
FRE : Free run clock VCXO for set up, 0 = normal, 1 = free run
To set crystal series capacitor

Switches and Matrix Description

Figure 6



Output selection

Q1	Q0	Output
0	0	AOL
0	1	AOR

Mute and gain selection

Q0	I2	Mute	Gain
0	0	OFF*	-
0	1	ON*	-
1	0	-	0dB**
1	1	-	+6dB**

* Mute is activated by left channel selection
** Gain is activated by right channel selection

Input selection

I1	I0	Input
0	0	INTL
0	1	INTR
1	0	EAIL
1	1	EAIR

Example of programming

First step : 0 0 1 0 0 X X X
INTL connected to AOL, mute ON on AOL/AOR

Second step : 0 1 0 1 1 X X X
EAIR connected to AOR, gain 0dB on AOL/AOR

Thrird step : 0 0 0 0 0 X X X
INTL connected to AOL, mute OFF on AOL/AOR

The power up default configuration is 0dB and unmute for both channels AOL/R, and INTL connected to AOL, and INTR connected to AOR.

CR2 : NICAM control (read and write register)

SDI	ECT	MAE	FN1	UMT	LA1	LA0	BEA
0	0	0	0	0	0	0	1

MSB LSB

SDI : I^2S direction
0 = Output, 1 = Input
ECT : Bit error rate counting time
0 = 128ms, 1 = 64ms
MAE : Max allowed errors
0 = 511, 1 = 255
FN1 : Set function of bit 0 in SR0, 0 = loss of alignment (status), 1 = system status (I or B/G)
UMT : Un-mute NICAM, 1 = un-mute, 0 = mute
LA1 : Language select 1 (LA1 ⊕ SEL1)
LA0 : Language select 0 (LA0 ⊕ SEL0)
BEA : Set C1-C3 function

ECT	MAE	BER MUTE
0	0	8.9×10^{-3} (1 in 112)
0	1	4.4×10^{-3} (1 in 225)
1	0	1.8×10^{-2} (1 in 56)
1	1	8.9×10^{-3} (1 in 112)

Un-mute at BER/4.

TDA8204 Output (Pin)	BEA	
	0	1
C1 (21)	C1*	Single mono mode
C2 (20)	C2*	Dual mono mode
C3 (19)	C3*	Stereo mode

* Application control bit of NICAM signal

Note : C4 pin remains unchanged. The function of C1-C4 in SR0 remains unchanged.

CR3 : Switches (read and write register)

US1	US0	AUT	IBG	FS1	FS0	X	SYN
0	0	1	0	0	0	0	1

MSB LSB

US1 : User bit 1 (output)
US0 : User bit 0 (output)
AUT : Automatic selection, 1 = enable
IBG : Select system I or B/G, 1 = B/G
FSn : Force switch (see table)
SYN : 1 = synthesiser, 0 = dual VCXO (carrier loop)

FS1	FS0	Selection
0	0	Auto NICAM
0	1	FM-Mono
1	0	FM-Stereo
1	1	NICAM

NICAM STAND-ALONE APPLICATION

The NICAM kit has been designed to be monitored by the I^2C bus; nevertheless stand-alone working capability is offered to the designer for low cost applications.
In order to know the status of the kit in stand-alone mode, consider the contents of the four I^2C registers at power-ON (4 registers : SR0 - CR1 - CR2 - CR3). Hardware configurable pins will be described later.

1 - Power-ON Configuration

SR0 (status)

US2	C1	C2	C3	C4	MUT	LA2	L/S
US2	0	0	0	1	1	1	1

MSB LSB

US2 : Not used in stand-alone
C1 :
C2 : Application control bit status for NICAM signal
C3 :
C4 : Reserve Sound Flag
MUT : DAC outputs muted (demuted as soon as NICAM appears)
LA2 : the subframe alignment is been lost
L/S : FAW status (FN1 of CR2 = 0)

CR1 (R/$\overline{W}$)

Q1	Q0	I2	I1	I0	G0	AUM	FRE
0	0	0	0	0	0	0	0

MSB LSB

Q1 :
Q0 : NICAM sound is sent on all matrix
I2 : outputs and on AMOx pins
I1 :
G0 : Gain = 0dB on AMOx
AUM : AMOx pins un-muted
FRE : VCXO in normal mode

CR2 (R/$\overline{W}$)

SDA	ECT	MAE	FN1	UMT	LA1	LA0	BEA
0	0	0	0	0	0	0	1

MSB LSB

SDA : Normal mode
ECT & MAE : BER = 1/112
FN1 : Bit L/S of SR0 set to alignment loss status
UMT : TDA8204 mute pin 25 to 0
LA1 : Result depending of SEL1
LA0 : Result depending of SEL0
BEA : Beacon decoding mode but all diodes are OFF until a NICAM signal has been found

CR3 (R/$\overline{W}$)

US1	US0	AUT	IBG	FS1	FS0	X	SYN
0	0	1	0	0	0	0	1

MSB LSB

US1 : Not used in stand-by mode
US0 : Not used in stand-by mode
AUT : Automatic standard

IBG : Standard I (don't care)
FSn : Set to Auto NICAM (if NICAM fails, FM mono is selected)
FN2 : Not used
SYN : Synthesizer selected

2 - Hardware Configurable Pins

2.1 - TDA8204 - PIN 6 - (RSW)
- as an output :
  status of the RSW switch
  - 0 = FM mono
  - 1 = NICAM
- as an input :
  - 0 = FM mono (forced)

2.2 - TDA8204 - PINS 34/35 - (SEL0/SEL1) (see Figure 7)
- to select the language in case of bilingual operation
- selected value is related to LA0 and LA1

As the I^2C bus is not used LA0 and LA1 = 0 (power-ON condition) / SEL0 = Q0, SEL1 = Q1

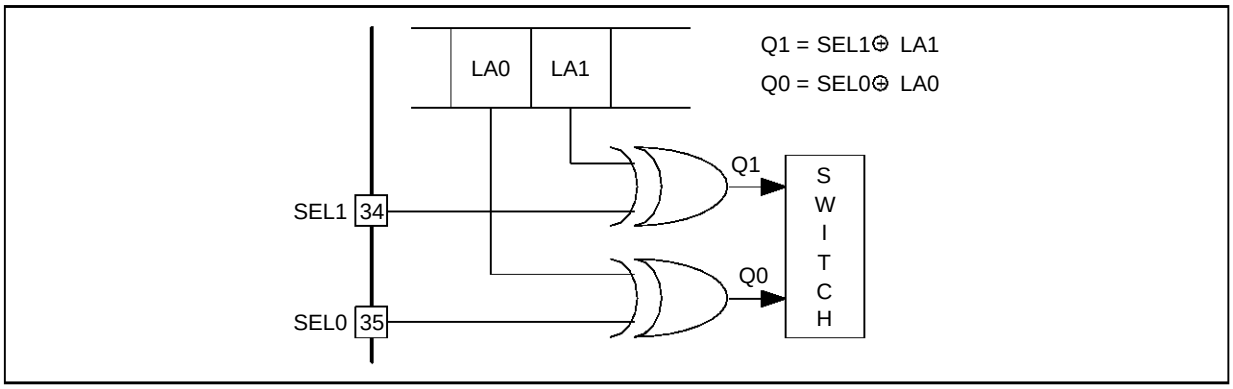
The 4 choices are summarized in the table below.

SEL0	SEL1	DACDL	DACDR
0	0	M1	M2
0	1	M1	M1
1	0	M2	M2
1	1	M2	M1

M1 = Mono 1
M2 = Mono 2

VII - 2.3. TDA8204 - PIN 25 - (MUTE)
- as an output :
  status of the DAC
  - 0 = unmuted
  - 1 = muted
- as an input :
  - 0 = unmute DAC (forced)

Figure 7



APPLICATION DIAGRAMS

Figure 8 : Stand Alone Application (I standard)

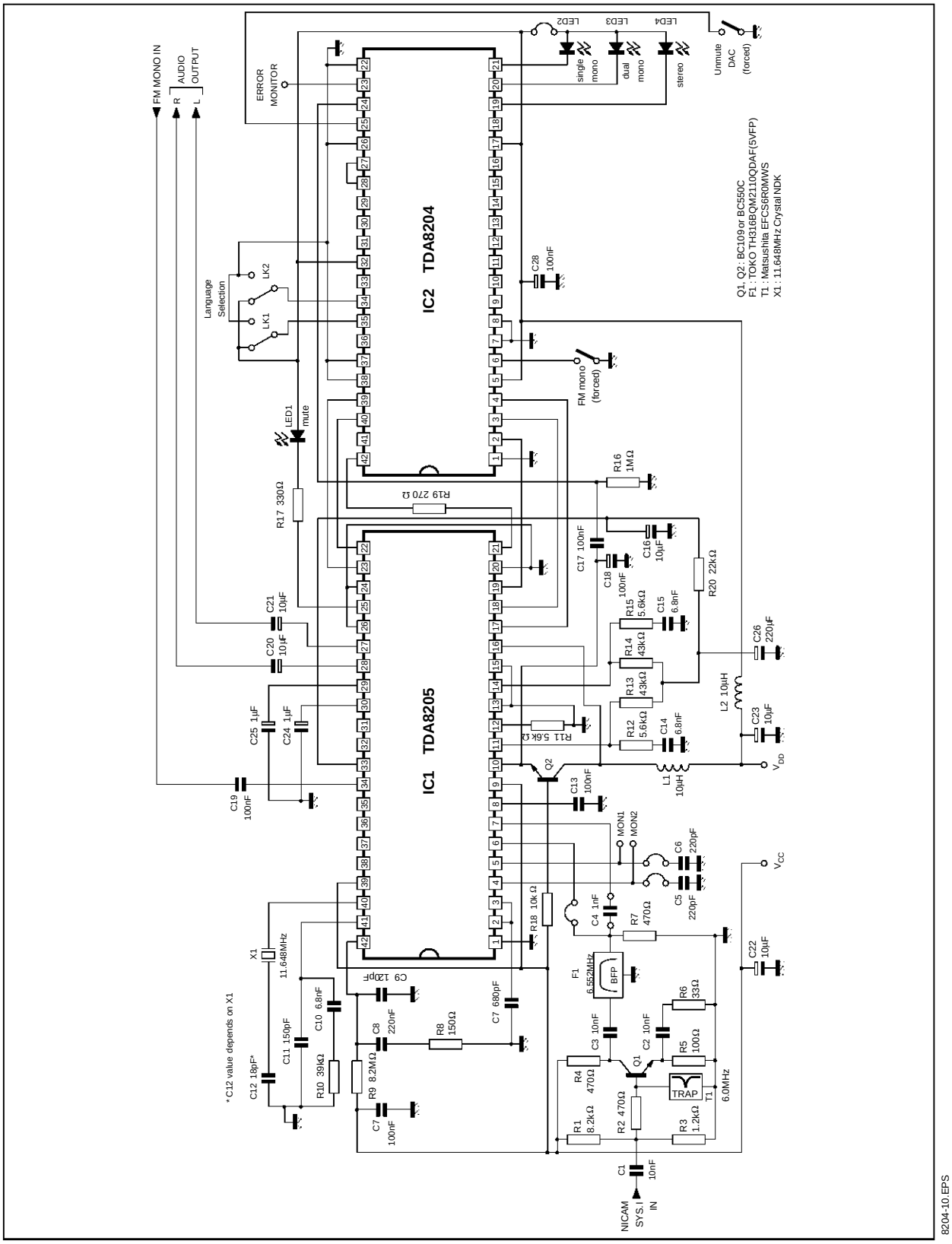
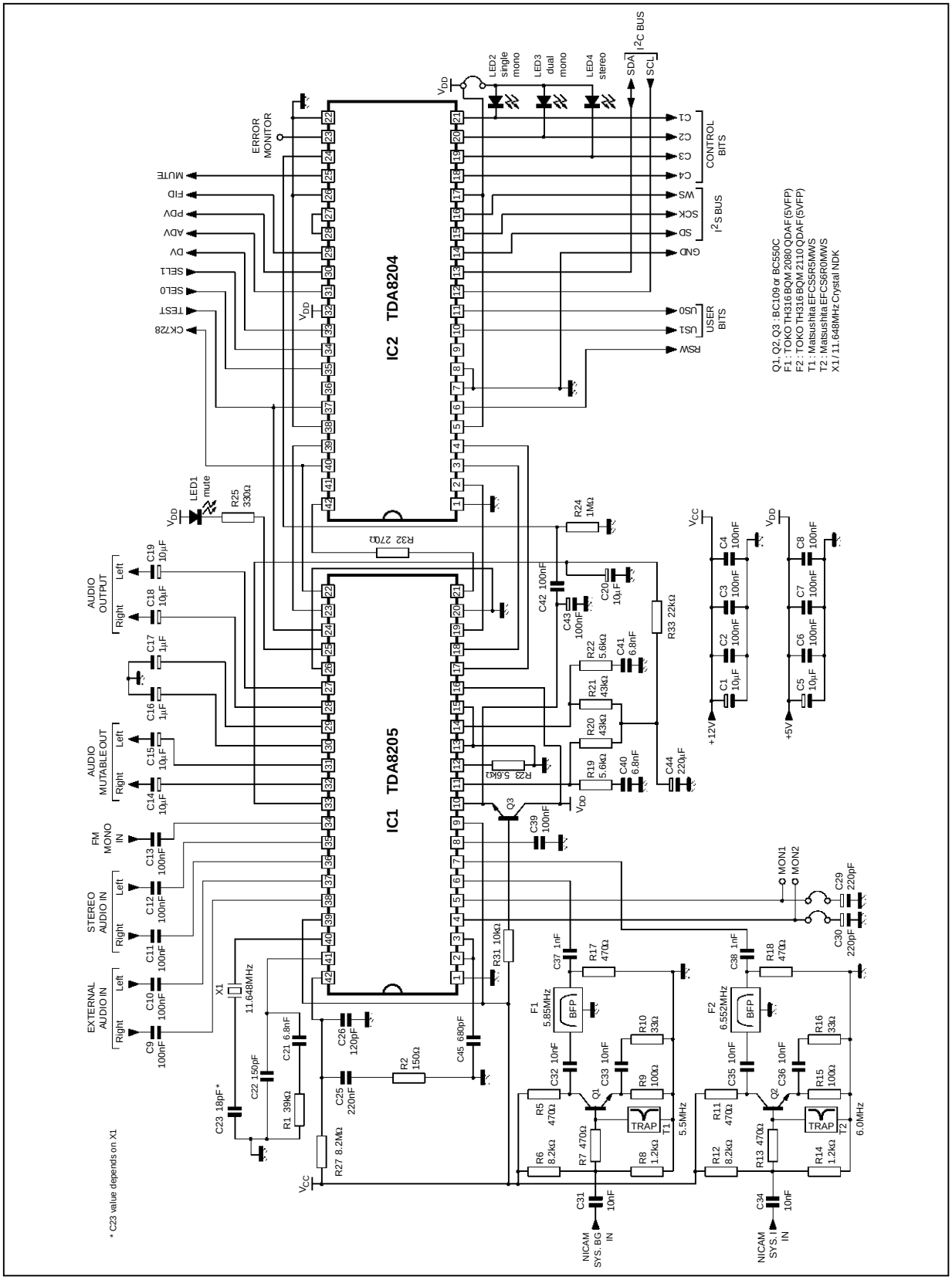
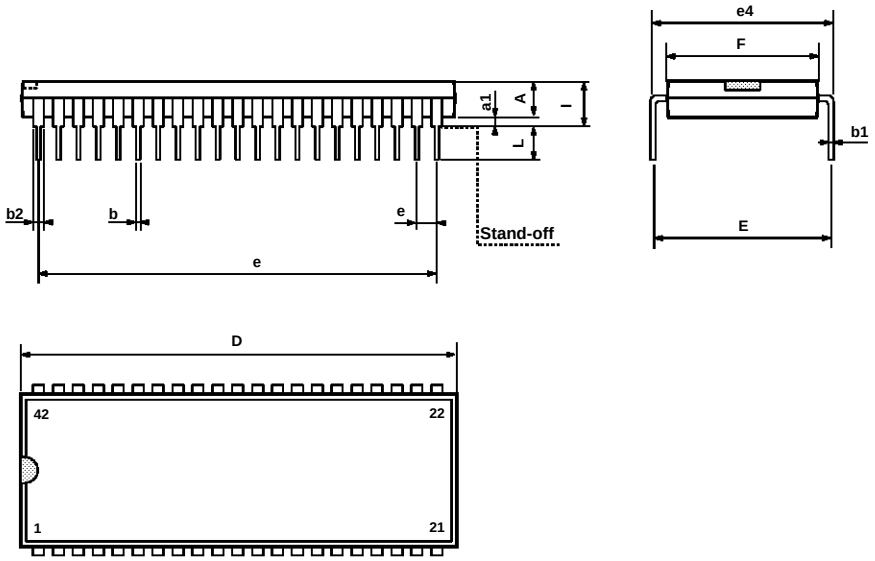


Figure 9 : I²C Bus Controlled Application (I and B/G standard)



PACKAGE MECHANICAL DATA
42 PINS - PLASTIC SHRINK



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.056
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
i			5.08			0.200
L		2.54			0.100	

SDIP42.TBL