RF1K49211

HARRIS SEMICONDUCTOR

June 1997

7A, 12V, 0.020Ω, Logic Level, Single N-Channel Power MOSFET

Features

- **7A, 12V**
- **$r_{DS(ON)}$ = 0.020Ω**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49211	MS-012AA	RF1K49211

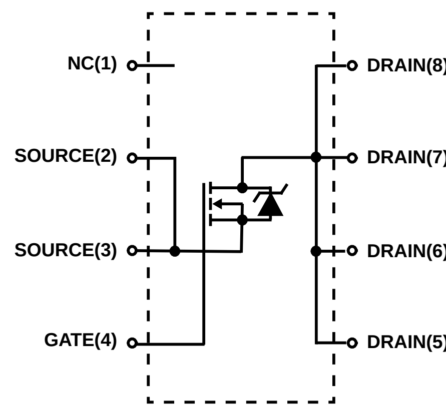
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4921196.

Description

The RF1K49211 Single N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This product achieves full-rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

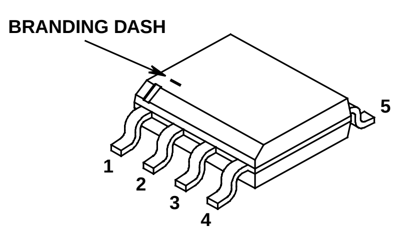
Formerly developmental type TA49211.

Symbol



Packaging

JEDEC MS-012AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Absolute Maximum Ratings $T_A = 25^oC$ Unless Otherwise Specified

		RF1K49211	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	12	V
Drain to Gate Voltage (Rgs = 20KΩ) (Note 1)	V_{DGR}	12	V
Gate to Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous (Pulse Width = 1s)	I_D	7	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	2	W
Derate Above 25^oC		0.016	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		12	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12V$, $V_{GS} = 0V$	$T_A = 25^oC$	-	-	1	µA
			$T_A = 150^oC$	-	-	50	µA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm10V$		-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 7A$, $V_{GS} = 5V$		-	-	0.020	Ω
Turn-On Time	t_{ON}	$V_{DD} = 6V$, $I_D \cong 7A$, $R_L = 0.86\Omega$, $V_{GS} = 5V$, $R_{GS} = 25\Omega$ (Figures 18, 19)		-	-	250	ns
Turn-On Delay Time	$t_{d(ON)}$			-	50	-	ns
Rise Time	t_r			-	150	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	120	-	ns
Fall Time	t_f			-	160	-	ns
Turn-Off Time	t_{OFF}			-	-	350	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 9.6V$, $I_D \cong 7A$, $R_L = 1.37\Omega$ $I_{g(REF)} = 1.0mA$ (Figures 20, 21)	-	60	75	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0V$ to $5V$		-	35	45	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $1V$		-	2	2.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 12V$, $V_{GS} = 0V$, f = 1MHz (Figure 14)		-	1850	-	pF
Output Capacitance	C_{OSS}			-	1600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	600	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse Width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 7A$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 7A$, $dI_{SD}/dt = 100A/\mu s$	-	-	95	ns

Typical Performance Curves

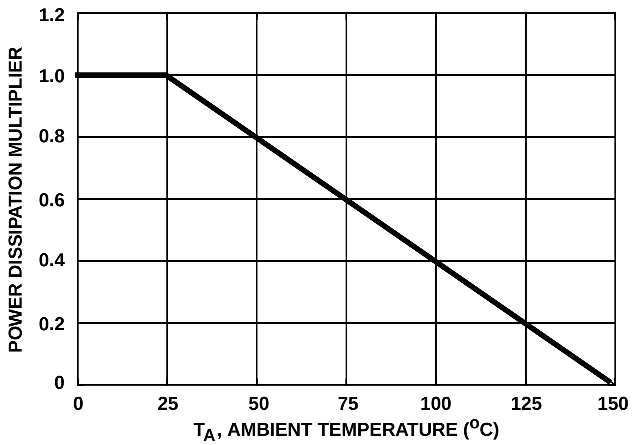


FIGURE 1. NORMALIZED POWER DISSIPATION vs TEMPERATURE

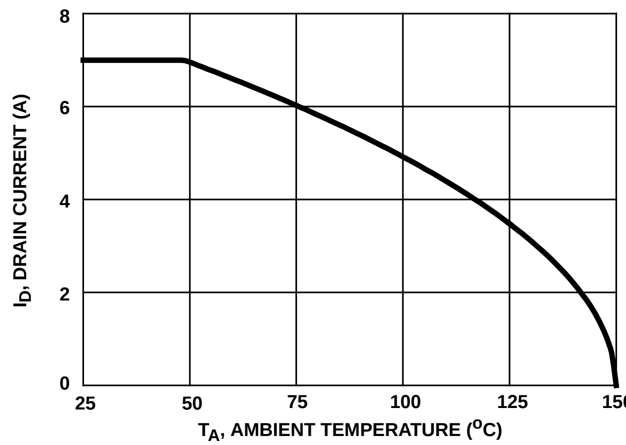


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

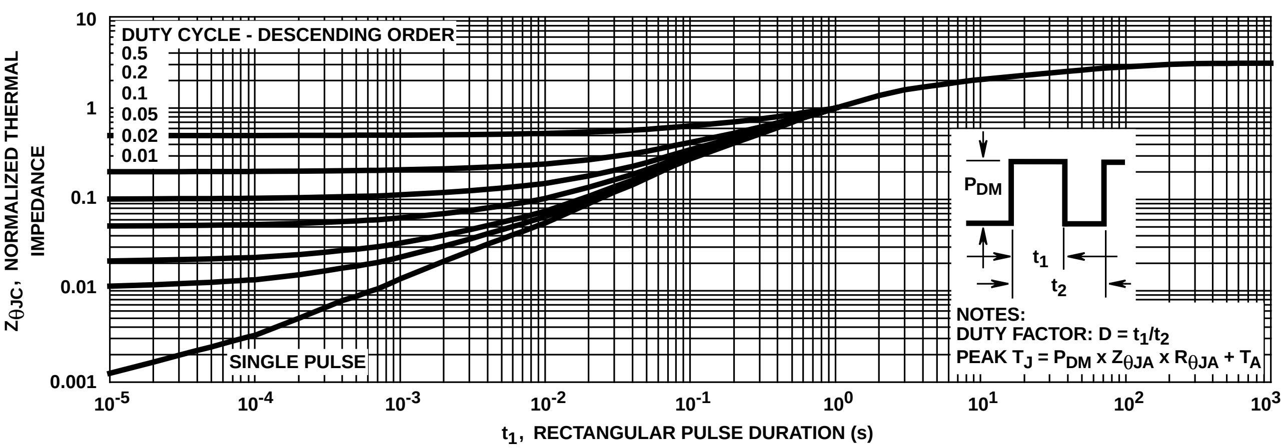


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

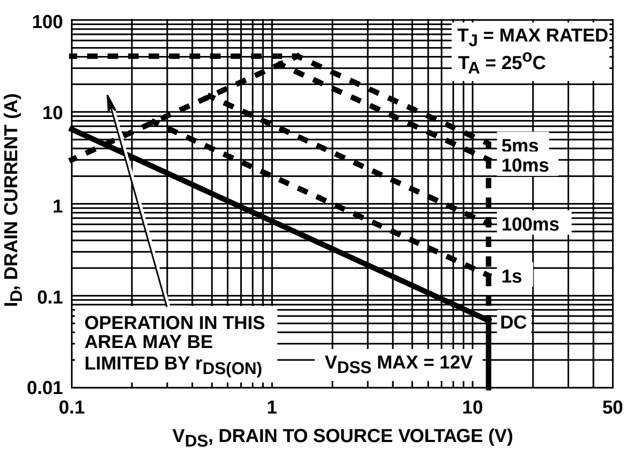


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

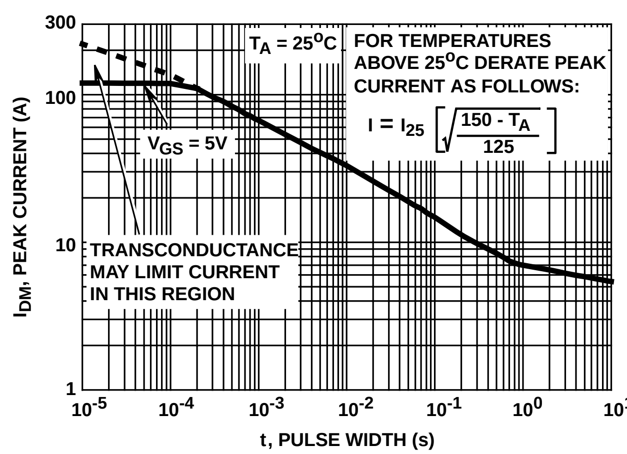
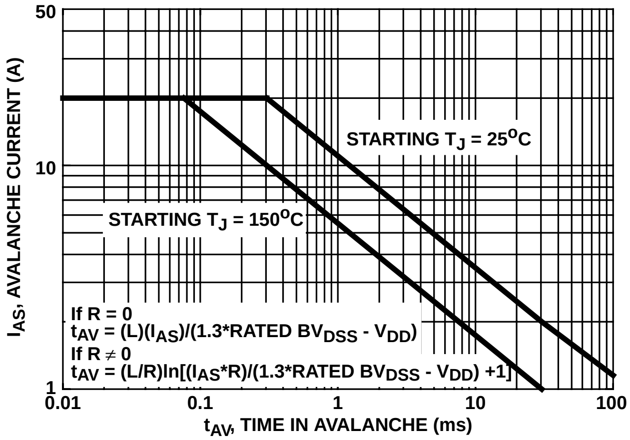


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

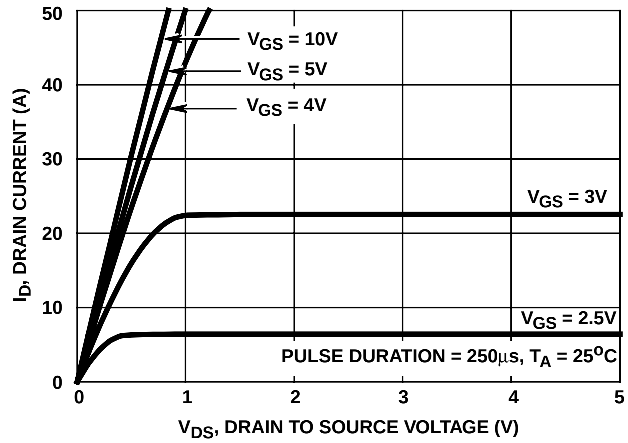


FIGURE 7. SATURATION CHARACTERISTICS

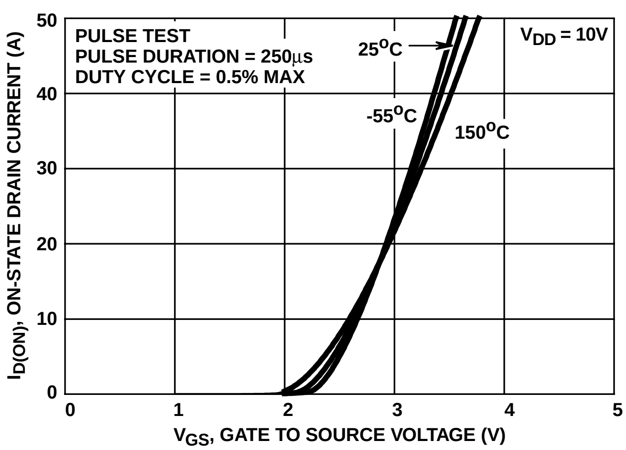


FIGURE 8. TRANSFER CHARACTERISTICS

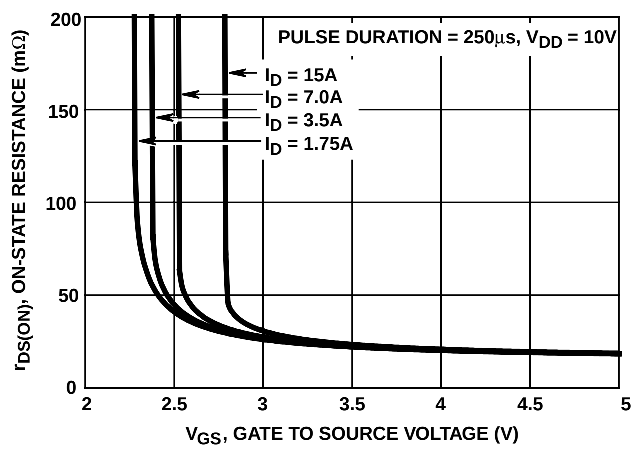


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

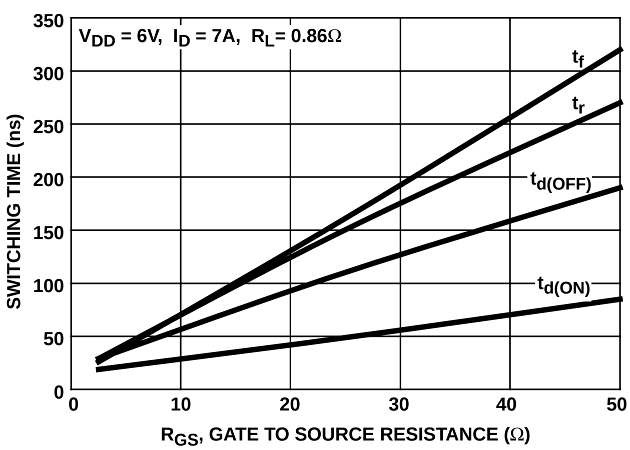


FIGURE 10. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

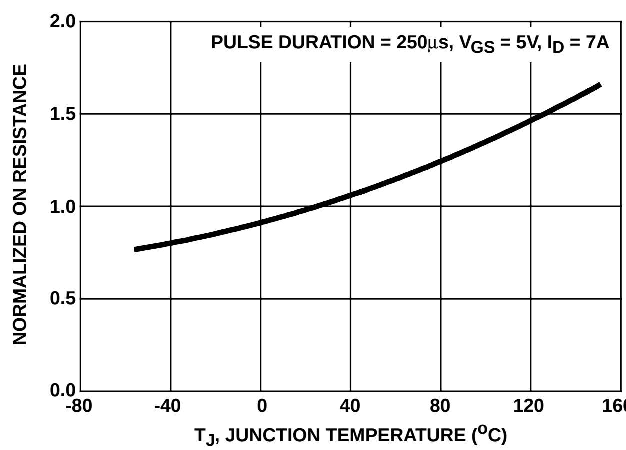


FIGURE 11. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

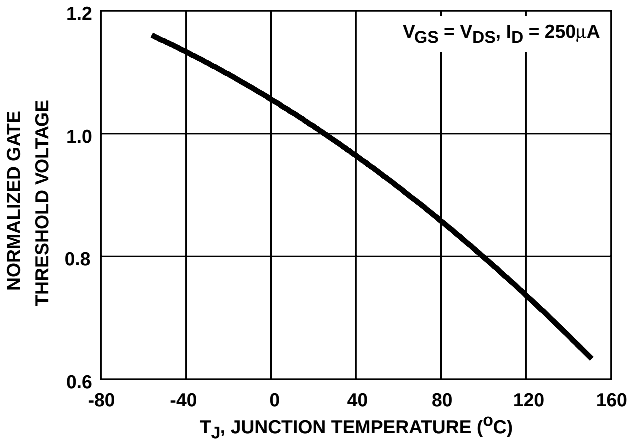


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

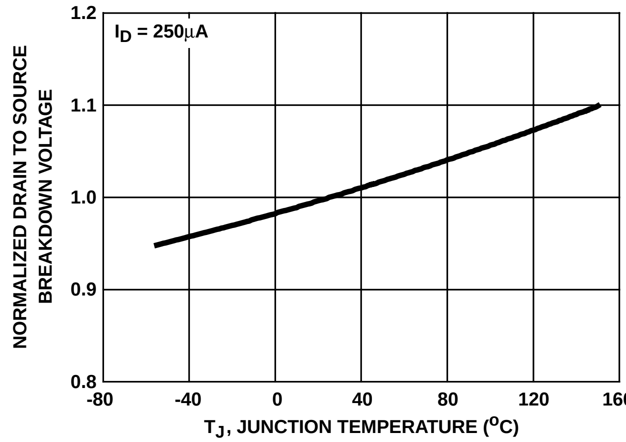


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

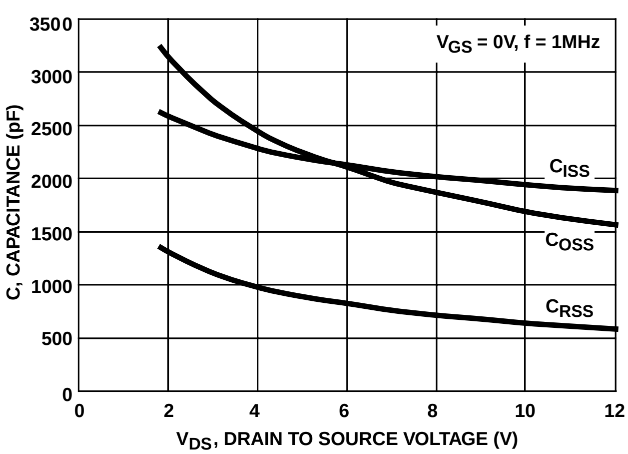
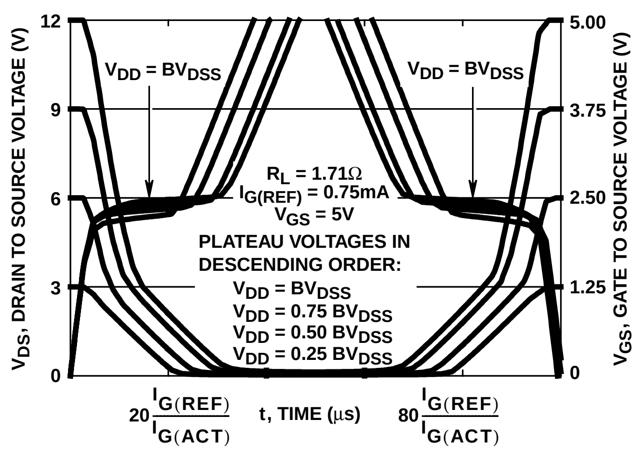


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

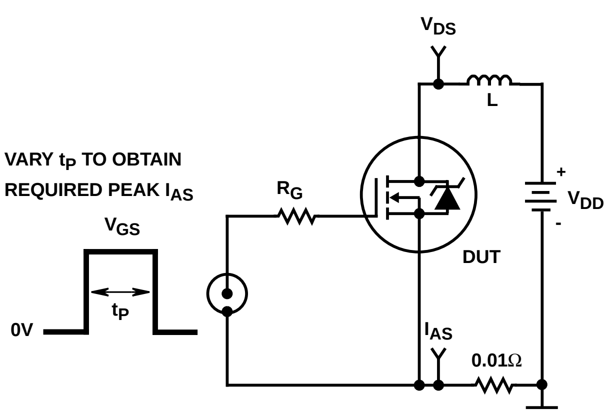


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

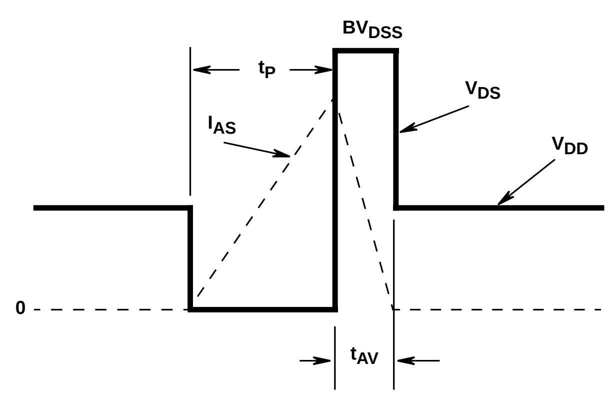


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms

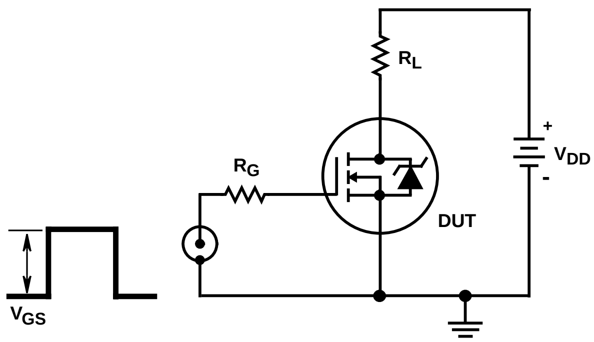


FIGURE 18. SWITCHING TIME TEST CIRCUIT

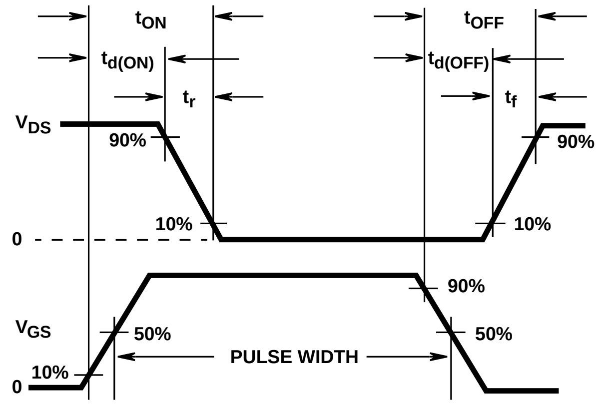


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

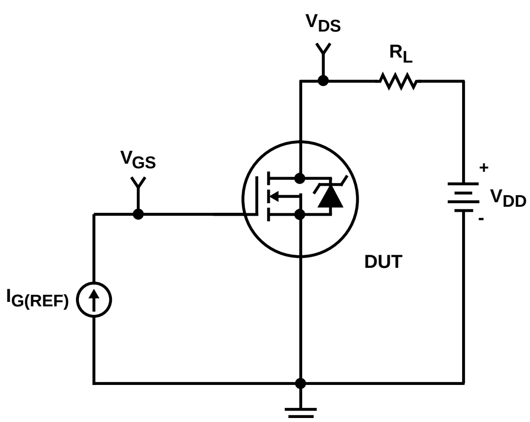


FIGURE 20. GATE CHARGE TEST CIRCUIT

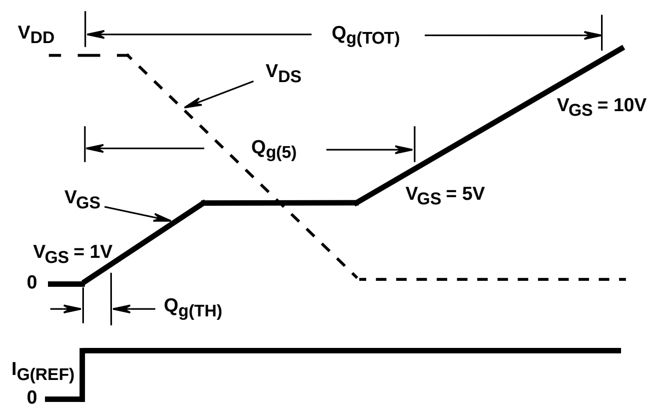


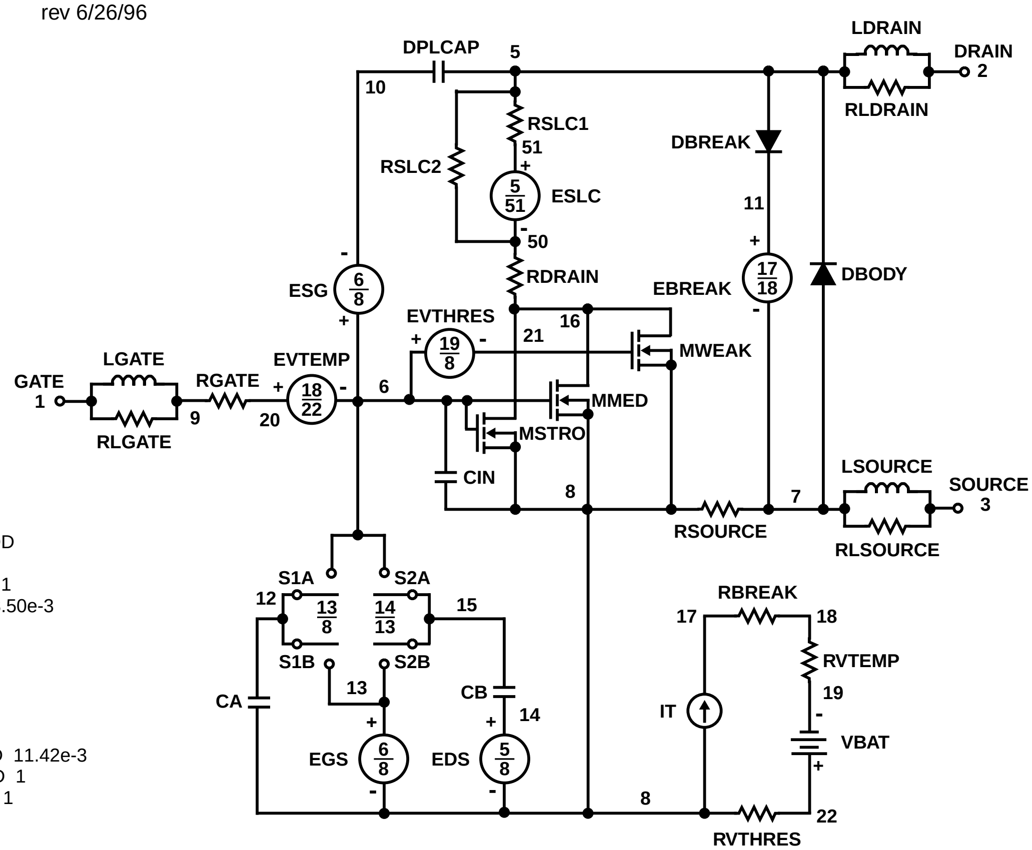
FIGURE 21. GATE CHARGE WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100^{o}C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5^{o}C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30^{o}C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260^{o}C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

Temperature Compensated PSPICE Model for the RF1K49211

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SUBCKT  RF1K49211 2 1 3 ;        rev 6/26/96

CA  12  8  2.11e-9
CB  15  14  2.99e-9
CIN  6  8  1.30e-9

DBODY  7  5  DBODYMOD
DBREAK  5 11  DBREAKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  15.81
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTHRES  6  21 19  8  1
EVTEMP  20  6  18  22  1

IT  8  17  1

LDRAIN  2  5  1e-9
LGATE 1  9  1.04e-9
LSOURCE  3  7  2.37e-10

MMED 16  6  8  8  MMEDMOD
MSTRO 16  6  8  8  MSTROMOD
MWEAK 16  21  8  8  MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN  50  16  RDRAINMOD  3.50e-3
RGATE  9  20  1.57
RLDRAIN  2  5  10
RLGATE  1  9  10.4
RLSOURCE  3  7  2.37
RSLC1  5  51  RSLCMOD  1e-6
RSLC2  5  50  1e3
RSOURCE  8  7  RSOURCEMOD  11.42e-3
RVTHRES  22  8  RVTHRESMOD  1
RVTEMP  18  19  RVTEMPMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  22 19  DC  1

ESLC  51  50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*170),3))}

.MODEL DBODYMOD D (IS = 1.36e-12  RS = 1.65e-2  TRS1 = 3.88e-3  TRS2 = -5.45e-6  CJO = 2.95e-9 TT = 2.70e-8 M = 0.43)
.MODEL DBREAKMOD D (RS = 2.75e-3  TRS1 = -5.01e-4  TRS2 = -1.60e-4)
.MODEL DPLCAPMOD D (CJO = 2.40e-9  IS = 1e-30  N = 10 M = 0.55)
.MODEL MMEDMOD NMOS (VTO = 1.62  KP = 1.5 IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u RG = 1.57)
.MODEL MSTROMOD NMOS (VTO = 2.08  KP = 98.0 IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.402  KP = 0.067  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u RG = 15.7 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 8.51e-4  TC2 = 7.88e-7)
.MODEL RDRAINMOD RES (TC1 = 1.55e-2  TC2 = 5.78e-5)
.MODEL RSLCMOD RES (TC1 =1.02e-4  TC2 = 1.07e-6)
.MODEL RSOURCEMOD RES (TC1 = 0  TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.20e-3  TC2 = -7.29e-6)
.MODEL RVTEMPMOD RES (TC1 = -5.10e-4  TC2 = 8.07e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.1  VOFF = -1.1)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.1  VOFF = -4.1)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.5  VOFF = 2.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.5   VOFF = -0.5)

.ENDS
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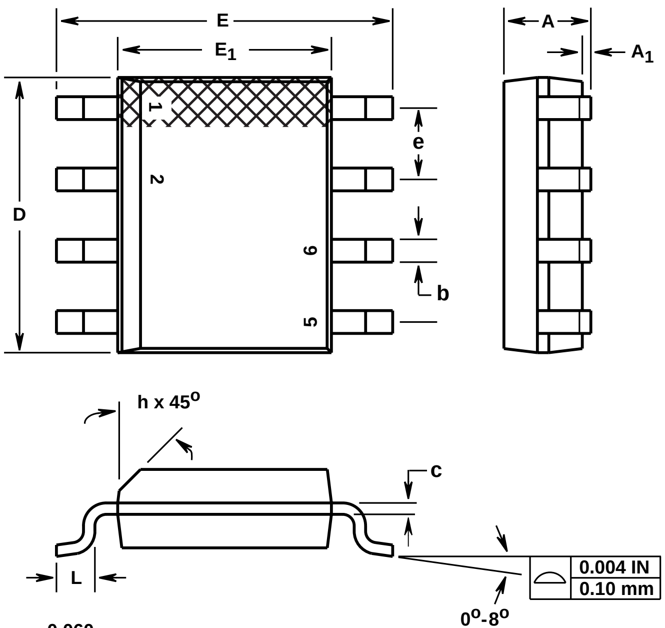
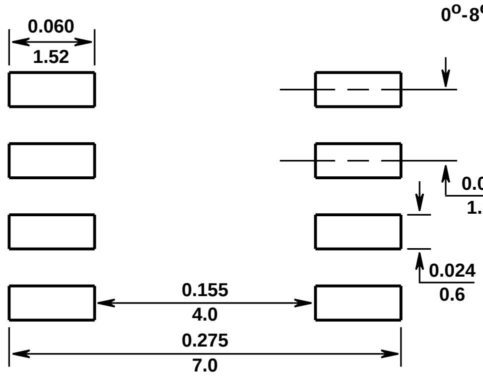
NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

MS-012AA

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE





MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

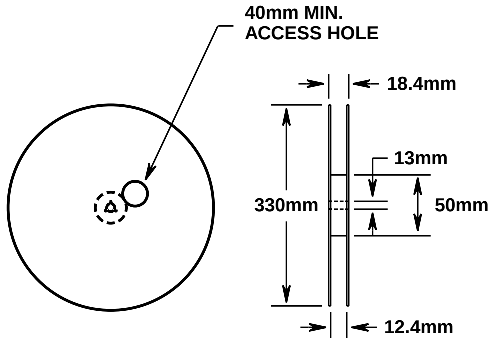
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

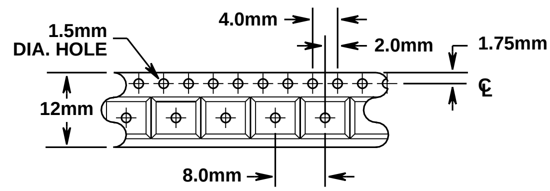
NOTES:

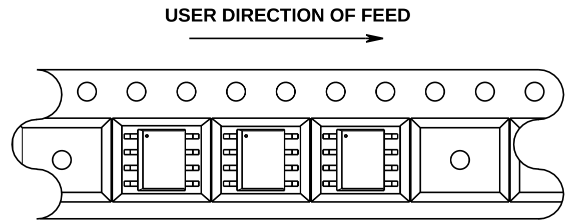
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension “E_1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. “L” is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 5 dated 2-23-96.

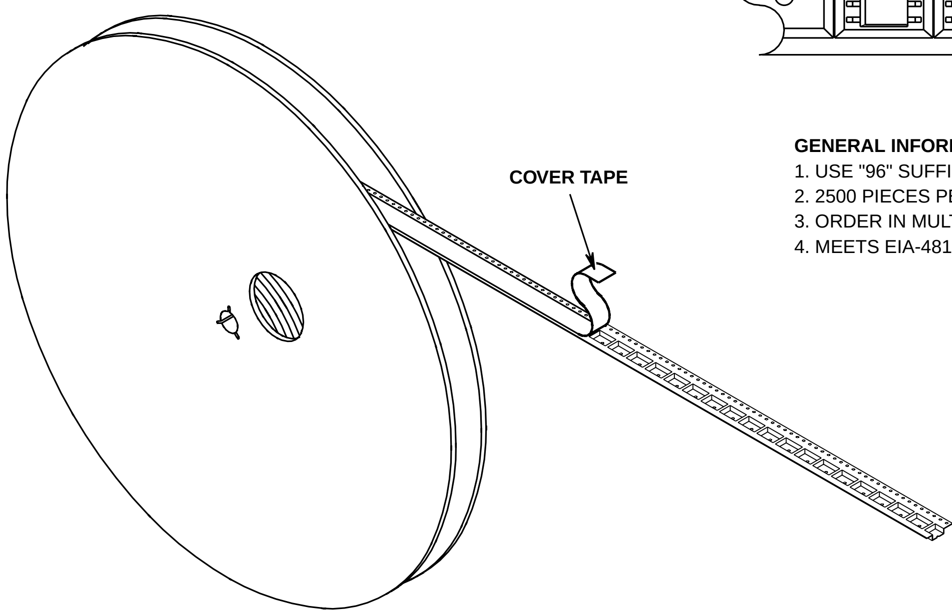
MS-012AA

12mm TAPE AND REEL









GENERAL INFORMATION

1. USE "96" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 5 dated 2-96

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Sales Office Headquarters

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HARRIS
SEMICONDUCTOR