HM514270C Series
HM51S4270C Series

262,144-word × 16-bit Dynamic Random Access Memory

HITACHI

ADE-203-365A (Z)
Rev. 1.0
Jul. 21, 1995

Description

The Hitachi HM51(S)4270C are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM51(S)4270C have realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM51(S)4270C offer fast page mode as a high speed access mode. Multiplexed address input permits the HM51(S)4270C to be packaged in standard 400-mil 40-pin plastic SOJ and standard 400-mil 44-pin plastic TSOPII. Internal refresh timer enables HM51S4270C self refresh operation.

Features

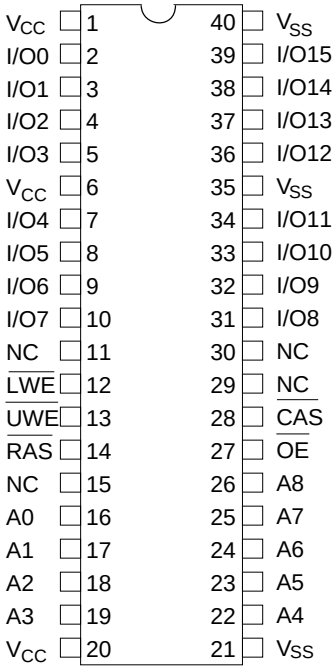
- Single 5 V (±10%)
- High speed
  - — Access time: 70 ns/80 ns (max)
- Low power dissipation
  - — Active mode:
    770 mW/688 mW (max)
  - — Standby mode: 11 mW (max)
    1.1 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycles: 8 ms
  128 ms (L-version)
- 2 $\overline{WE}$-byte control
- 2 variations of refresh
  - — $\overline{RAS}$-only refresh
  - — $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Battery backup operation (L-version)
- Self refresh operation (HM51S4270C)

Ordering Information

Type No.	Access Time	Package
HM514270CJ-7 HM514270CJ-8	70 ns 80 ns	400-mil 40-pin plastic SOJ (CP-40DA)
HM514270CLJ-7 HM514270CLJ-8	70 ns 80 ns	
HM51S4270CJ-7 HM51S4270CJ-8	70 ns 80 ns	
HM51S4270CLJ-7 HM51S4270CLJ-8	70 ns 80 ns	
HM514270CTT-7 HM514270CTT-8	70 ns 80 ns	400 mil 44-pin plastic TSOP II (TTP-44/40DB)
HM514270CLTT-7 HM514270CLTT-8	70 ns 80 ns	
HM51S4270CTT-7 HM51S4270CTT-8	70 ns 80 ns	
HM51S4270CLTT-7 HM51S4270CLTT-8	70 ns 80 ns	

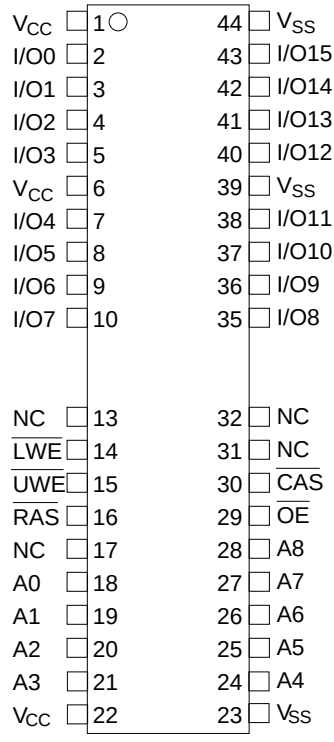
Pin Arrangement

HM514270CJ/CLJ Series
HM51S4270CJ/CLJ Series



(Top view)

HM514270CTT/CLTT Series
HM51S4270CTT/CLTT Series

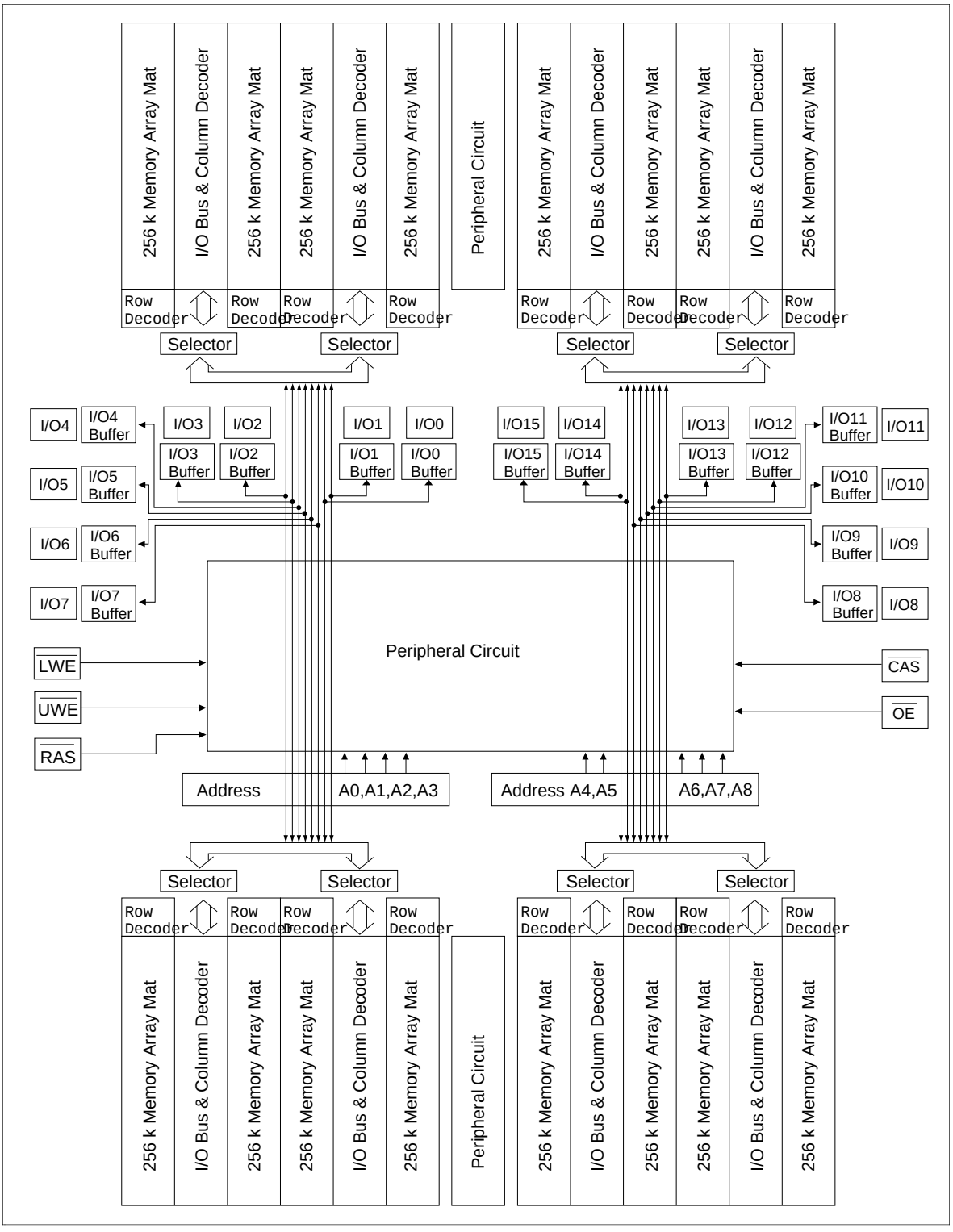


(Top view)

Pin Description

Pin Name	Function
A0 – A8	Address input –Row address A0 - A8 –Column address A0 - A8 –Refresh address A0 - A8
I/O0 – I/O15	Data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{UWE}$ / $\overline{LWE}$	Read/write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Mode

The HM51(S)4270C series has the following 11 operation modes.

1. Read cycle
2. Early write cycle
3. Delayed write cycle
4. Read-modify-write cycle
5. $\overline{\text{RAS}}$-only refresh cycle
6. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle
7. Self refresh cycle (HM51S4270C)
8. Fast page mode read cycle
9. Fast page mode early write cycle
10. Fast page mode delayed write cycle
11. Fast page mode read-modify-write cycle

Inputs					
$\overline{\text{RAS}}$	**$\overline{\text{CAS}}$**	**$\overline{\text{UWE}}$**	**$\overline{\text{LWE}}$**	**Output**	**Operation**
H	H	D	D	Open	Standby
H	L	H	H	Valid	Standby
L	L	H	H	Valid	Read cycle
L	L	L*2	L*2	Open	Early write cycle
L	L	L*2	L*2	Undefined	Delayed write cycle
L	L	H to L	H to L	Valid	Read-modify-write cycle
L	H	D	D	Open	$\overline{\text{RAS}}$-only refresh cycle
H to L	L	D	D	Open	$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle Self refresh cycle (HM51S4270C)
L	H to L	H	H	Valid	Fast page mode read cycle
L	H to L	L*2	L*2	Open	Fast page mode early write cycle
L	H to L	L*2	L*2	Undefined	Fast page mode delayed write cycle
L	H to L	H to L	H to L	Valid	Fast page mode read modify-write cycle

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2. $t_{WCS} \geq 0$ ns Early write cycle
   $t_{WCS} < 0$ ns Delay write cycle
3. Mode is determined by the OR function of the $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$. (Mode is set by the earliest of $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ active edge and reset by the latest of $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{\text{UWE}}$, $\overline{\text{LWE}}$.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)[*2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	2
	V_{CC}	4.5	5.0	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low	V_{IL}	–1.0	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current[*1, *2]	I_{CC1}	—	140	—	125	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	200	—	200	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{UWE}$, $\overline{LWE}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current[*2]	I_{CC3}	—	130	—	110	mA	t_{RC} = min

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Standby current[*1]	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current[*2]	I_{CC6}	—	130	—	110	mA	t_{RC} = min
Fast page mode current[*1, *3]	I_{CC7}	—	130	—	120	mA	t_{PC} = min
Battery backup current[*4] (Standby with CBR refresh) (L-version)	I_{CC10}	—	300	—	300	µA	Standby: CMOS interface Dout = High-Z CBR refresh: t_{RC} = 250 µs t_{RAS} ≤ 1 µs, $\overline{CAS}$ = V_{IL} $\overline{LWE}$, $\overline{UWE}$, $\overline{OE}$ = V_{IH}
Self-refresh mode current (HM51S4270C)	I_{CC11}	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V, Dout = High-Z
Self-refresh mode current (HM51S4270CL)		—	200	—	200	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V, Dout = High-Z
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 6.5 V
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 6.5 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5.0 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $V_{IH} \geq V_{CC} - 0.2$ V, $0 \leq V_{IL} \leq 0.2$ V, Address can be changed once or less while $\overline{RAS}$ = V_{IL}
5. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)[*1, *14, *15, *17, *18]

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Input levels: 0 V, 3 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	ns	22
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	15	—	15	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	ns	3, 5, 13
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	ns	3, 22
Read command setup time	t_{RCS}	0	—	0	—	ns	20
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	16, 19
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	16, 19
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	15	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	15	—	ns	

Write Cycle

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	10, 19
Write command hold time	t_{WCH}	15	—	15	—	ns	20
Write command pulse width	t_{WP}	10	—	10	—	ns	21
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	ns	21
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	ns	21
Data-in setup time	t_{DS}	0	—	0	—	ns	11, 21
Data-in hold time	t_{DH}	15	—	15	—	ns	11, 21
$\overline{CAS}$ to $\overline{OE}$ delay time	t_{COD}	—	0	—	0	ns	22

Read-Modify-Write Cycle

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	180	—	200	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	95	—	105	—	ns	10,19
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	ns	10,19
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	ns	10, 19
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	20	—	20	—	ns	21

Refresh Cycle

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	19
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	19
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

		HM514270C, HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	45	—	50	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	ns	
Fast page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{UWE}$, $\overline{LWE}$ delay time	t_{CPW}	65	—	70	—	ns	21
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	ns	

Self refresh Mode

		HM51S4270C					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	µs	23, 24, 25
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	−50	—	−50	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. After power up pause for 100 µs, then DRAM initialization requires a minimum of eight $\overline{RAS}$-only refresh or eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. If the user will implement $\overline{CAS}$-before-$\overline{RAS}$ timing in their system, then the eight initialization cycles MUST be $\overline{CAS}$-before-$\overline{RAS}$ cycles.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. The supply voltage with all Vcc pins must be on the same level.
    The supply voltage with all Vss pins must be on the same level.
18. A word of data can be written only when $\overline{UWE}$ and $\overline{LWE}$ go low at the same time. This implies that early write cycles cannot be combined with delayed write cycles in the same cycles because all data is latched at the fall of the first $\overline{WE}$. In other words, staggering the $\overline{WE}$ signals in one cycle is not permitted.
19. t_{RCH}, t_{RRH}, t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are determined by the earlier falling edge of $\overline{UWE}$ and $\overline{LWE}$.
20. t_{WCH} and t_{RCS} are determined by the later rising edge of $\overline{UWE}$ or $\overline{LWE}$.
21. t_{WP}, t_{RWL}, t_{CWL}, t_{OEH}, t_{DS}, t_{DH} and t_{CPW} should be satisfied by both $\overline{UWE}$ and $\overline{LWE}$.

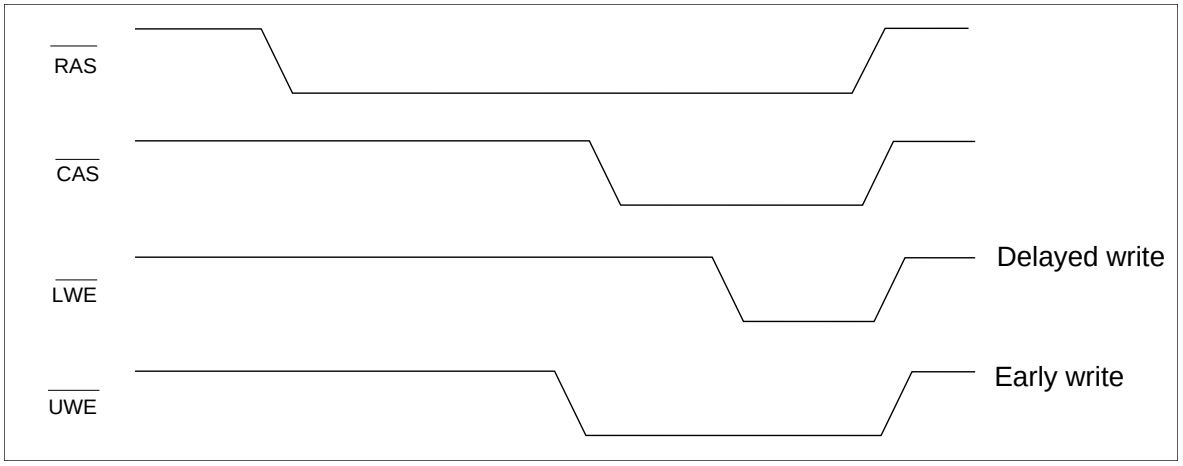
22. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} (min)/V_{IL} (max) level.
23. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBRrefresh should be executed within 15.6 µs immediately after exiting from and before enteringinto self refresh mode.
24. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
25. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
26.  H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max)
 Invalid Dout

Notes concerning 2$\overline{WE}$ control

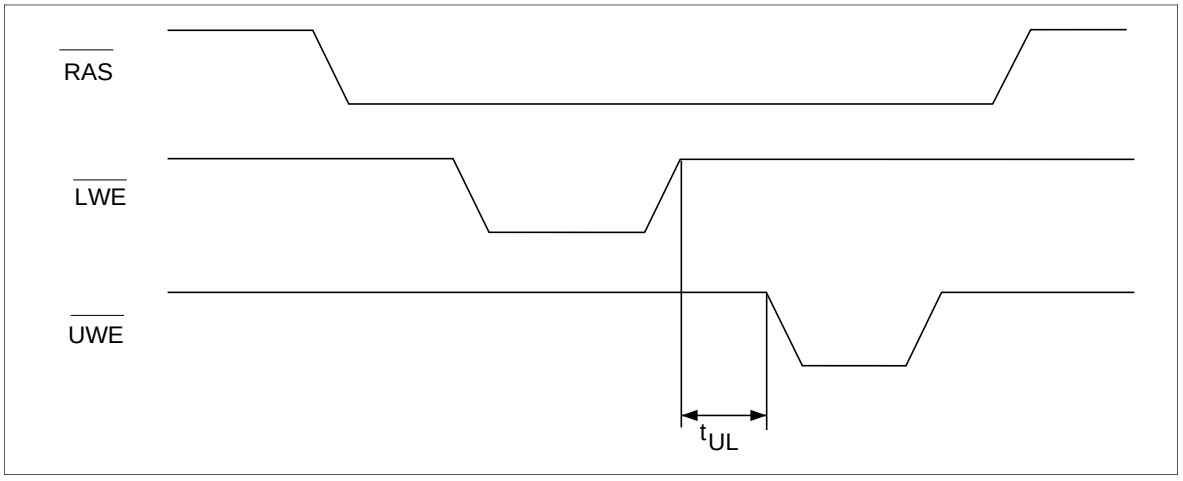
Please do not separate the $\overline{UWE}/\overline{LWE}$ operation timing intentionally. However skew between $\overline{UWE}/\overline{LWE}$ are allowed under the following conditions.

(1) Each of the $\overline{UWE}/\overline{LWE}$ should satisfy the timing specifications individually.

(2) Different operation mode for upper/lower byte is not allowed; such as following.

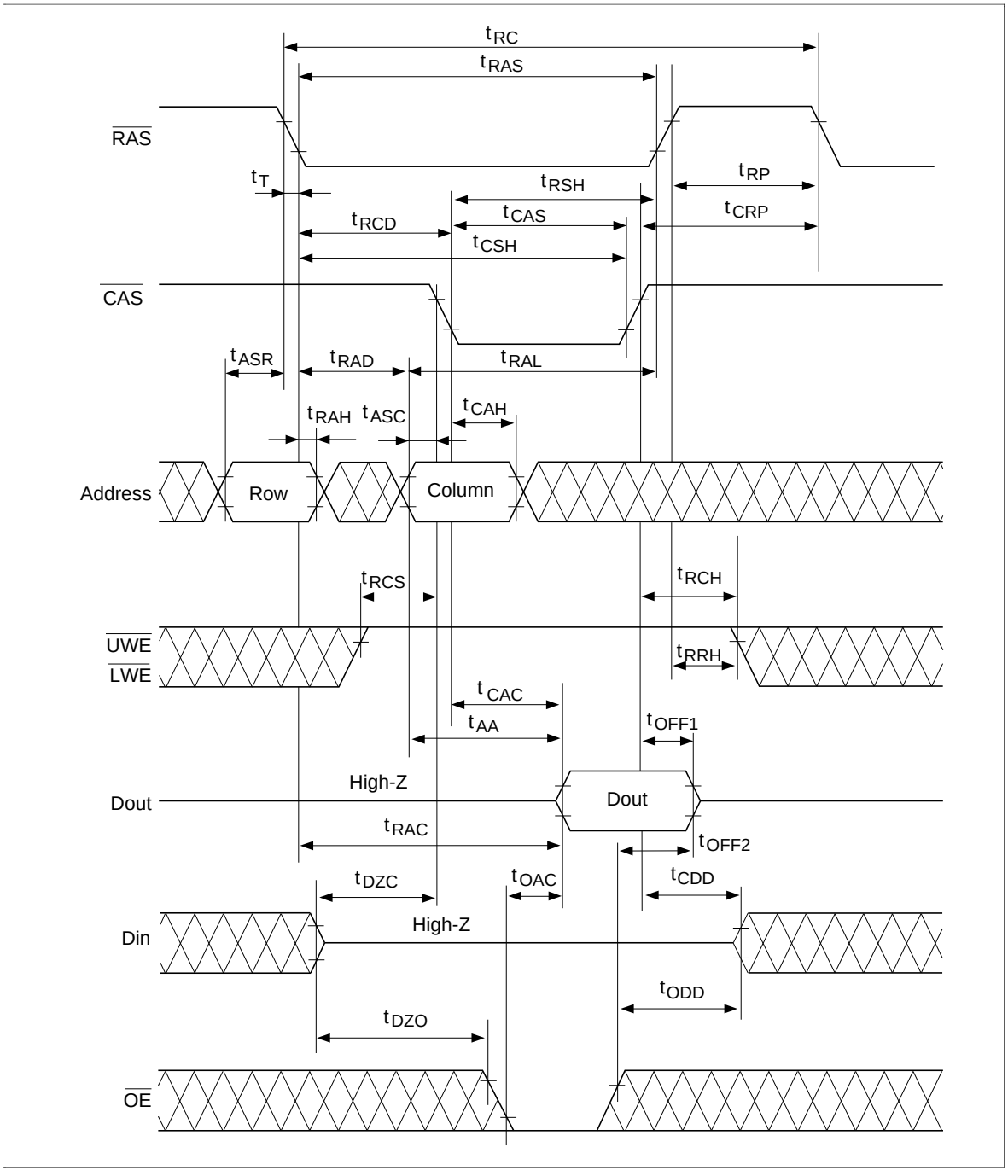


(3) Closely separated upper/lower byte control is not allowed, unless the condition ($t_{CP} \leq t_{UL}$) is satisfied.

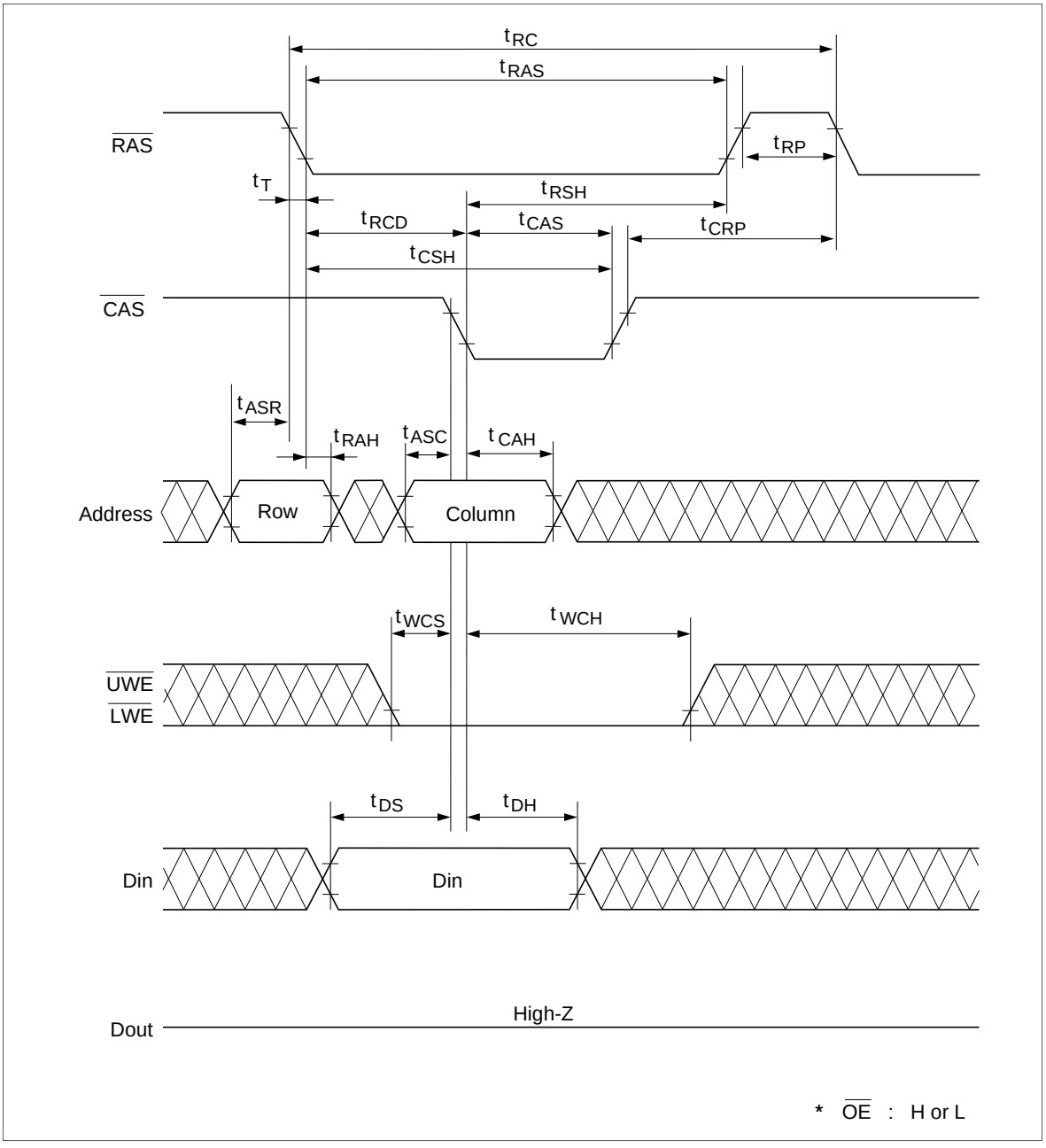


Timing Waveforms [*26]

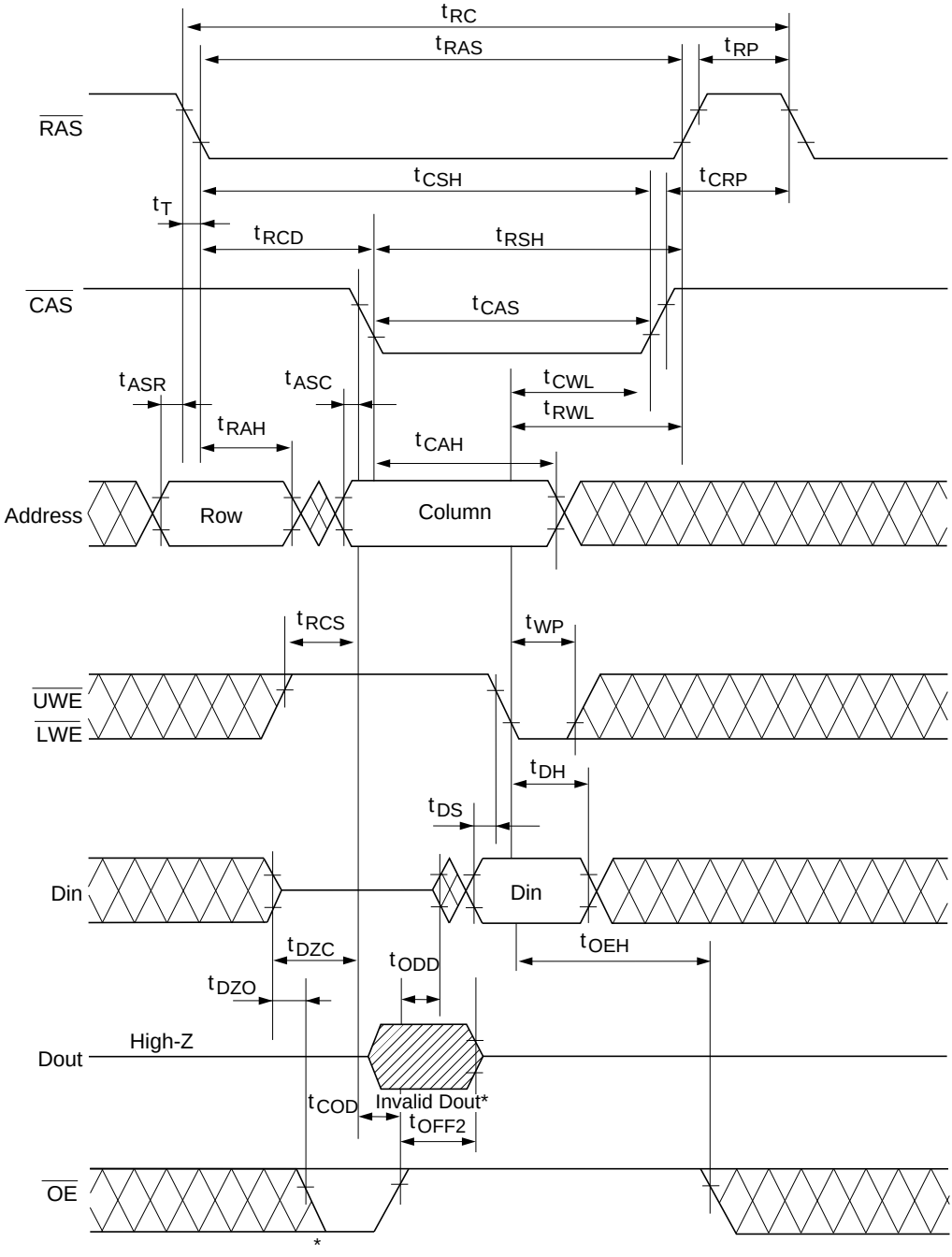
Read Cycle



Early Write Cycle

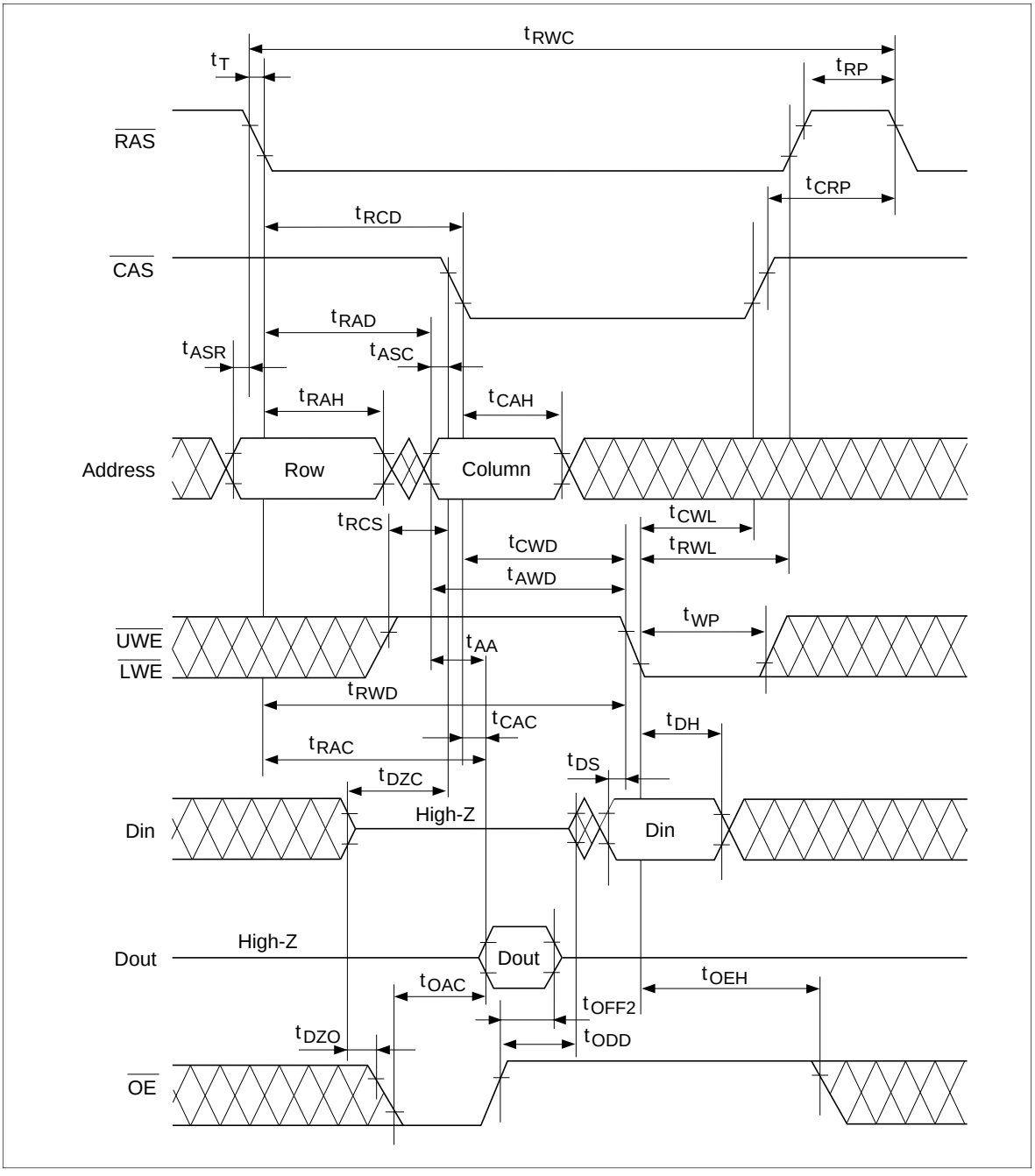


Delayed Write Cycle

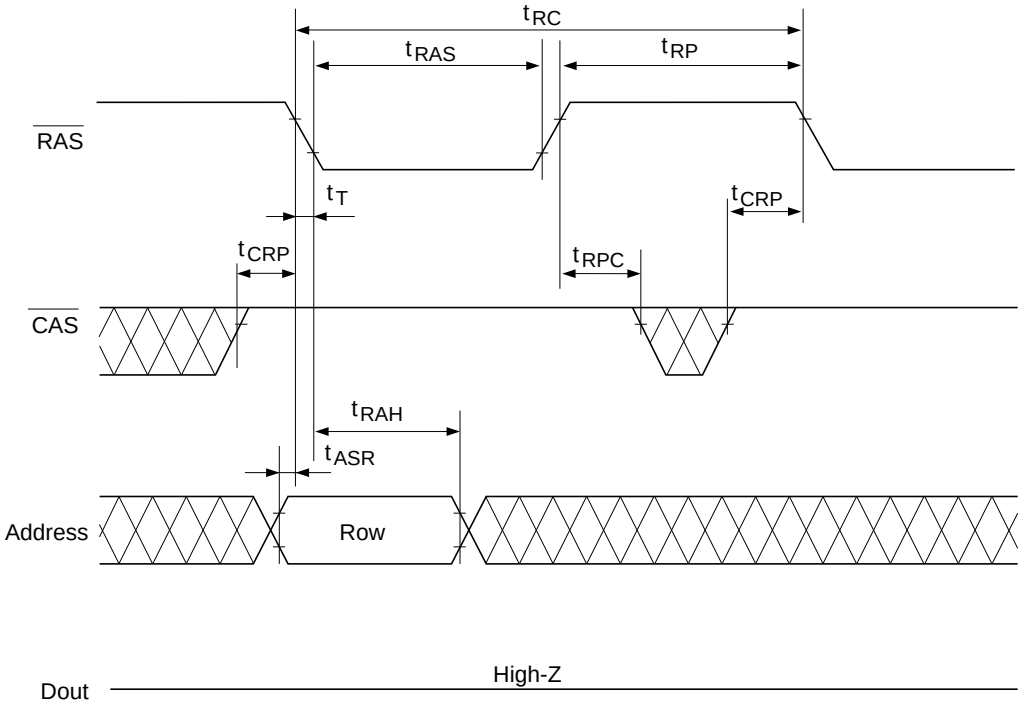


* Do not enable Dout during delayed write cycle.

Read-Modify-Write Cycle


tRWC
tT
tRP
RAS
tCRP
tRCD
CAS
tRAD
tASR
tASC
tRAH
tCAH
Address
Row
Column
tRCS
tCWL
tCWD
tRWL
tAWD
tWP
UWE
LWE
tAA
tRWD
tCAC
tDH
tRAC
tDS
tDZC
Din
High-Z
Din
Dout
High-Z
Dout
tOAC
tOEH
tOFF2
tDZO
tODD
OE

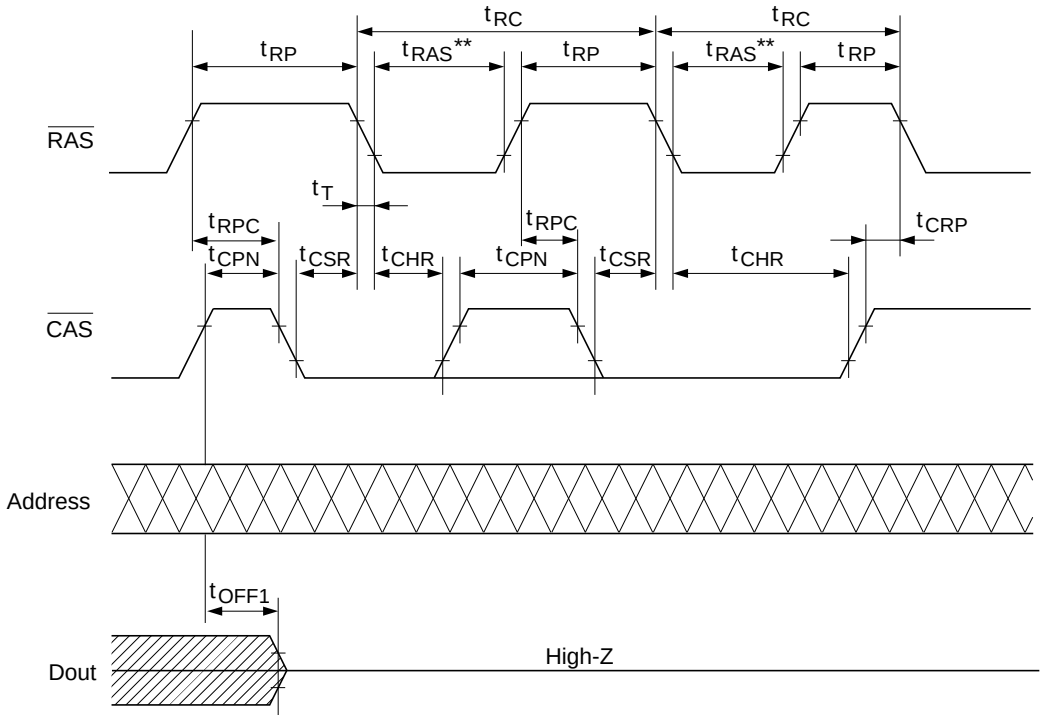
$\overline{\text{RAS}}$-Only Refresh Cycle



* $\overline{\text{UWE}}$, $\overline{\text{LWE}}$ and $\overline{\text{OE}}$: H or L

** Refresh address : A0 – A8 (AX0 – AX8)

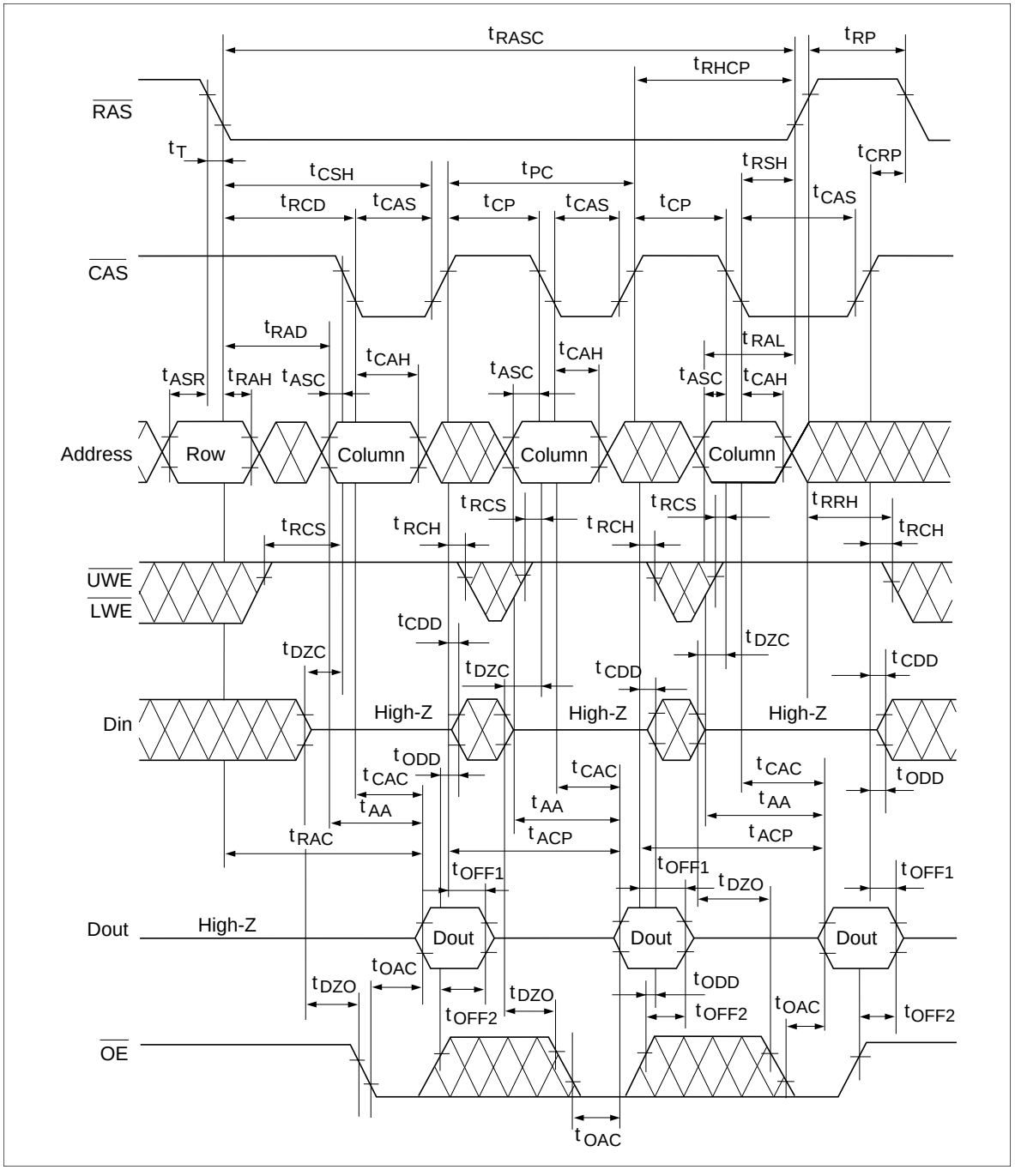
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



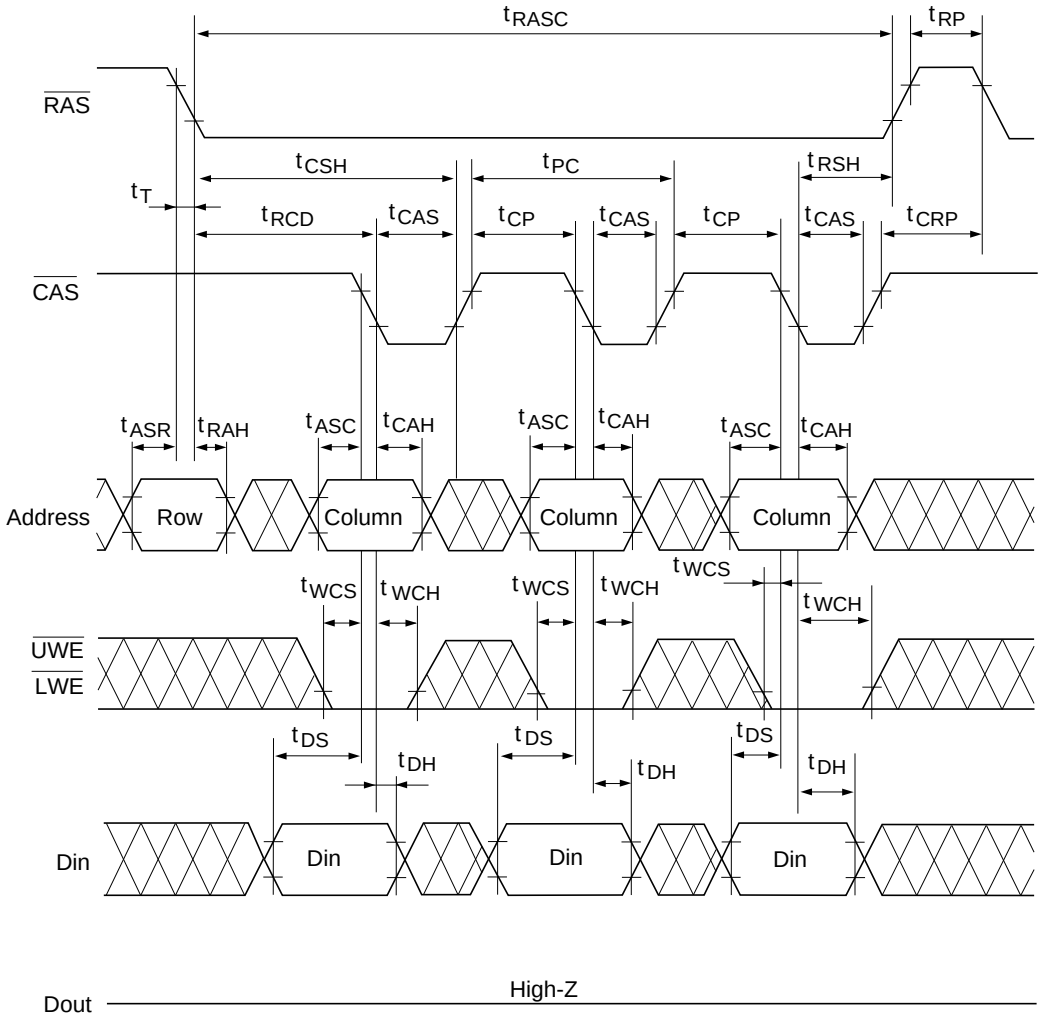
* $\overline{\text{UWE}}$, $\overline{\text{LWE}}$: H or L

** Do not extend $t_{RAS} \geq t_{RAS}$ max.
Untested self refresh mode may be activated and loss of data may be resulted.
(HM514270C)

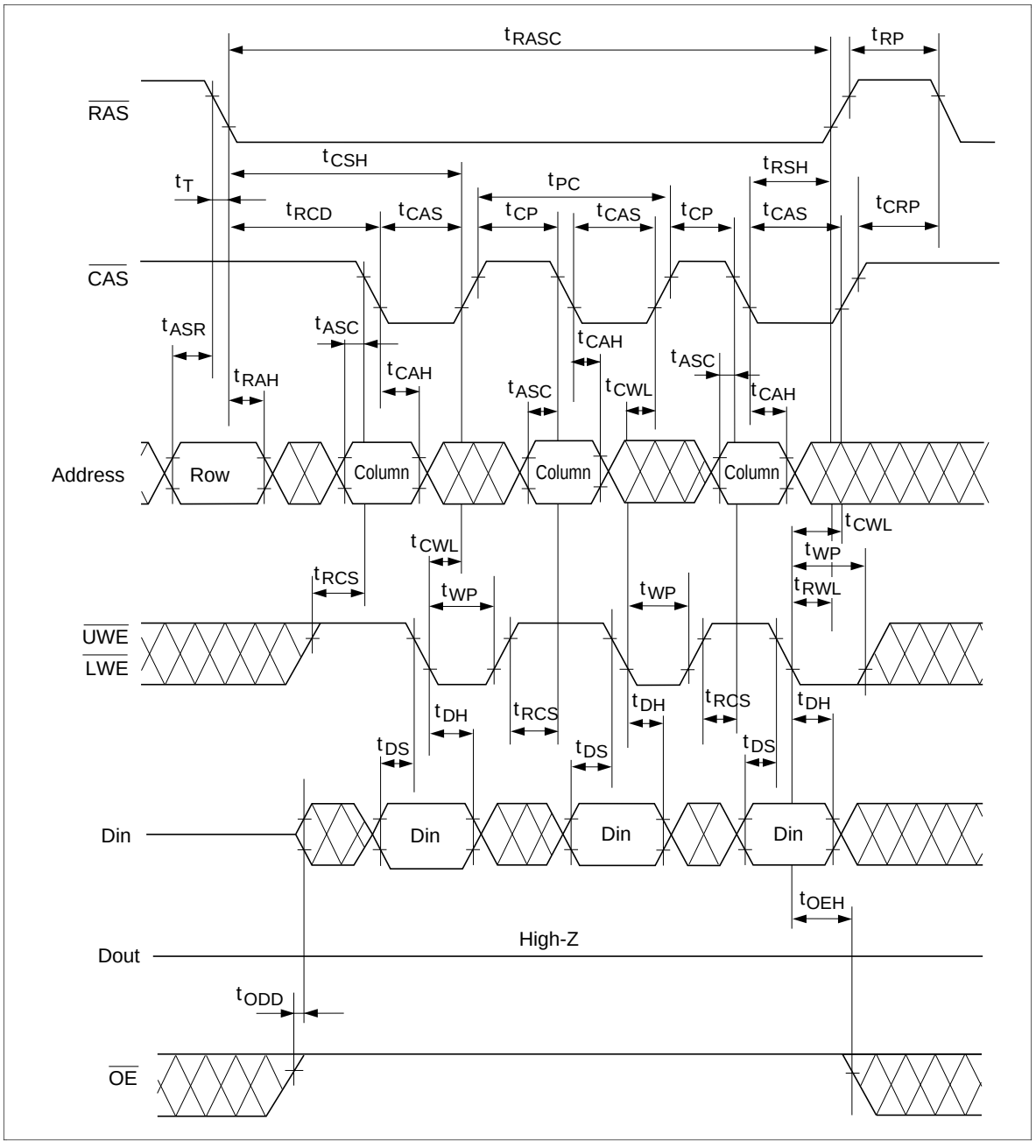
Fast Page Mode Read Cycle



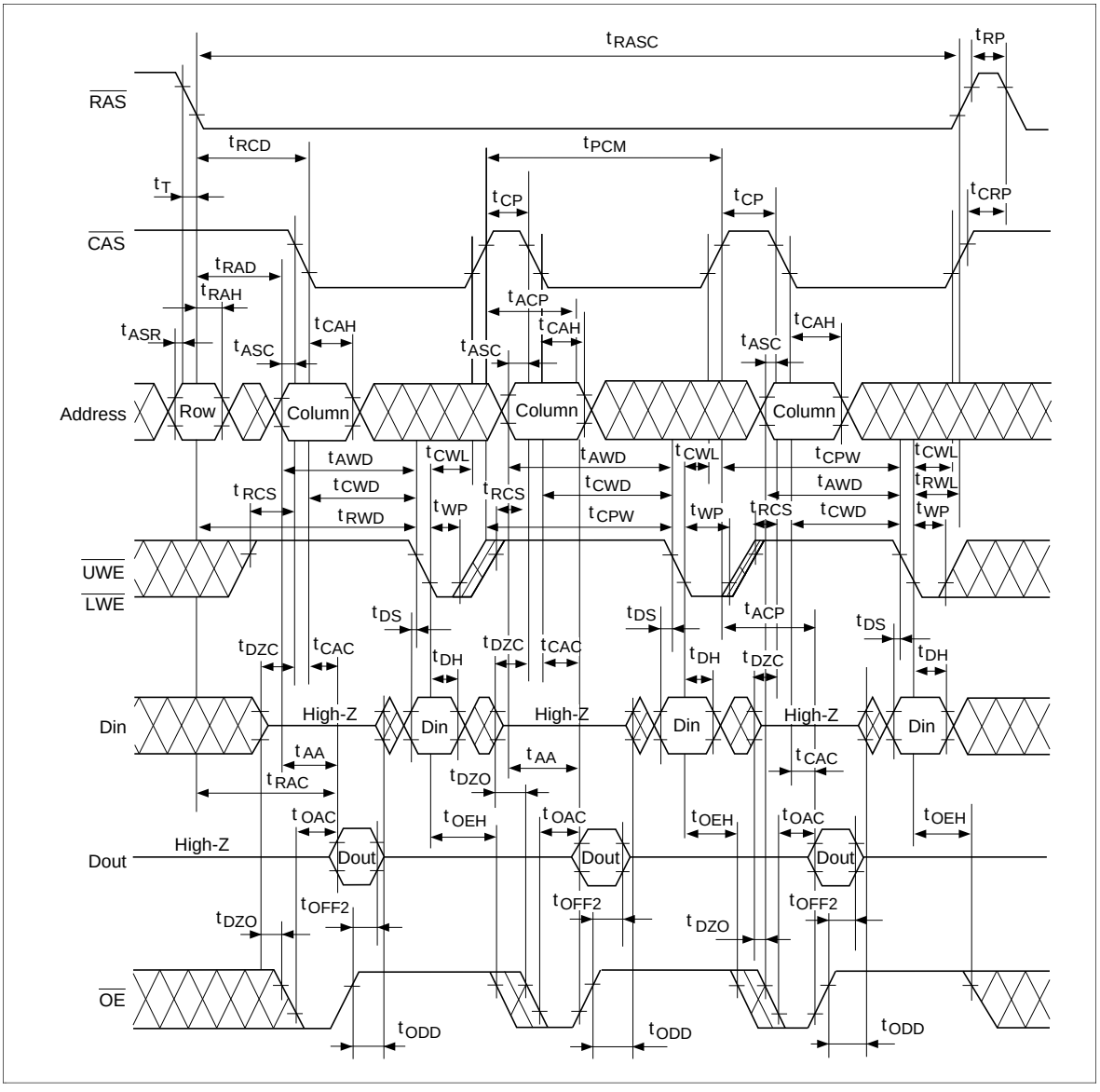
Fast Page Mode Early Write Cycle



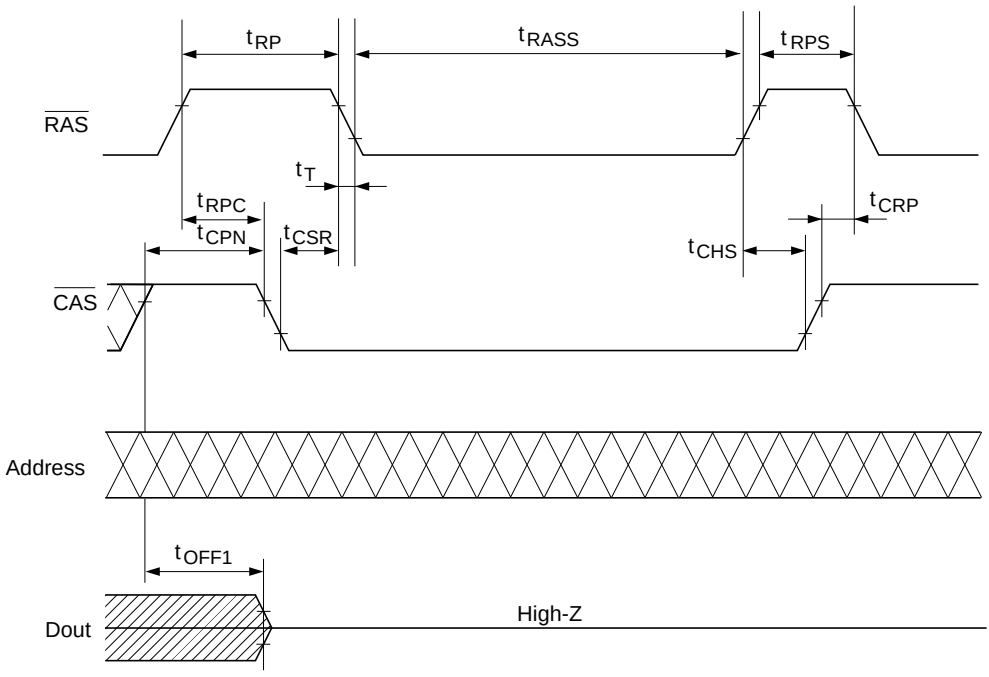
Fast Page Mode Delayed Write Cycle



Fast Page Mode Read-Modify-Write Cycle



Self Refresh Cycle



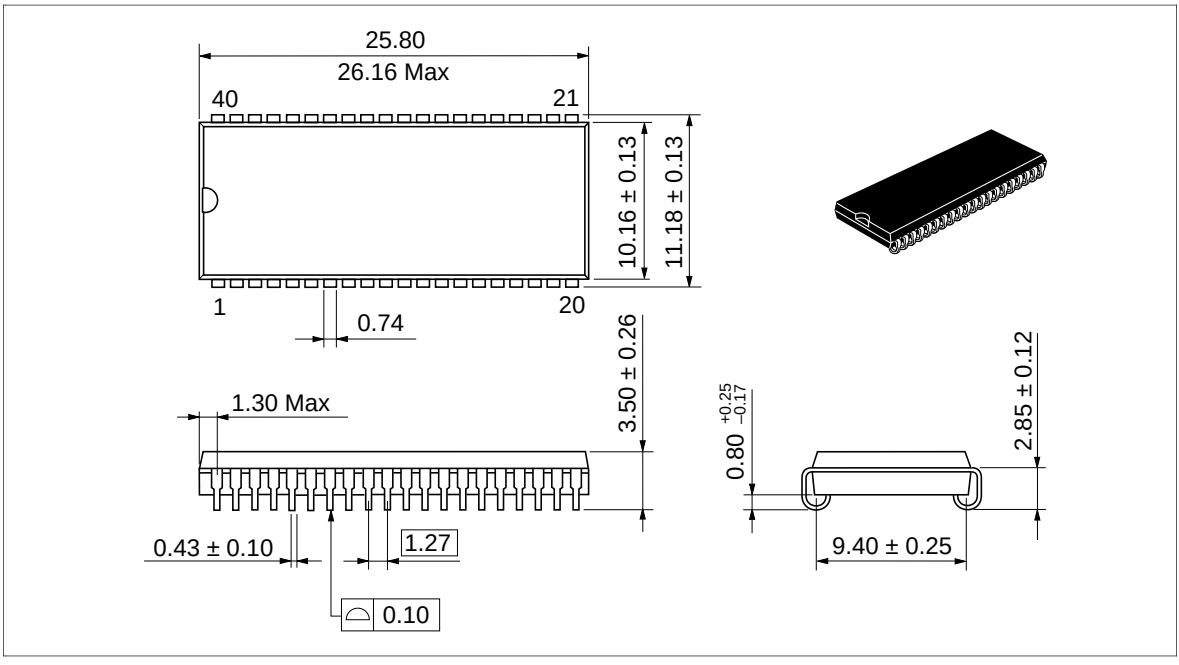
* $\overline{UWE}$, $\overline{LWE}$, and $\overline{OE}$: H or L

The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≥ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

Package Dimensions

HM51(S)4270CJ/CLJ Series (CP-40DA) Unit: mm



HM51(S)4270CTT/CLTT Series (TTP-44/40DB) Unit: mm