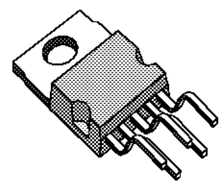
L387A

VERY LOW DROP 5V REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5 V ± 4 %)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR



Pentawatt®

ORDERING NUMBER : L387A

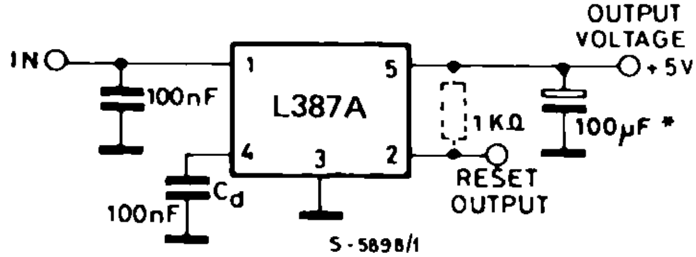
DESCRIPTION

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387A particularly suitable for microprocessor systems. This output provides a reset signal when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.

ABSOLUTE MAXIMUM RATINGS

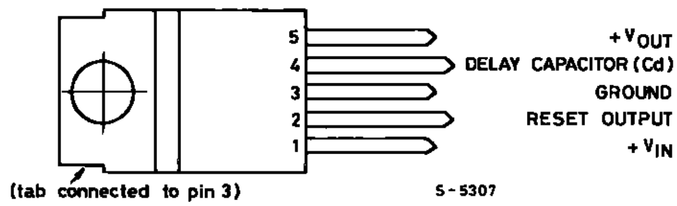
Symbol	Parameter	Value	Unit
V_i	D.C. Input Voltage	35	V
T_j, T_{stg}	Junction and Storage Temperature Range	–55 to 150	°C

APPLICATION CIRCUIT

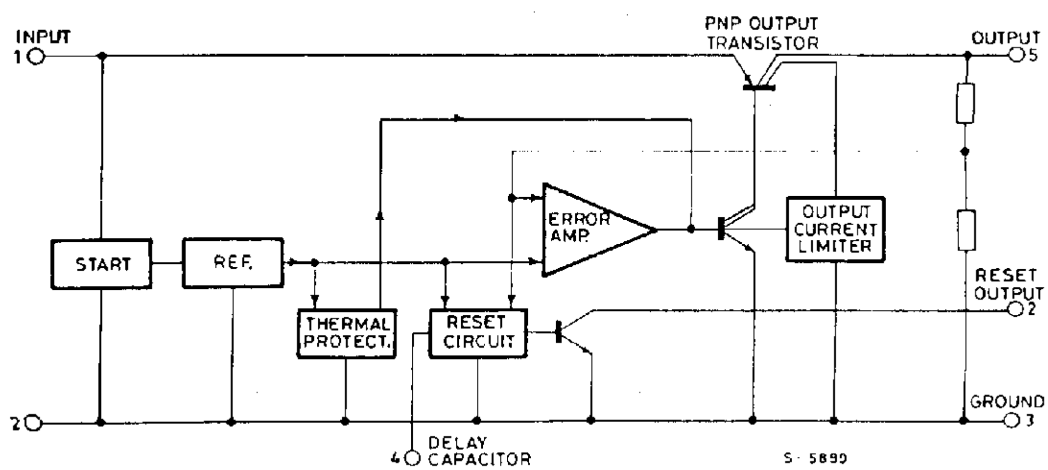


* Min 33 μF and max. ESR ≤ 3 Ω over temperature range.

PIN CONNECTION (Top views)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14.4 V, T_j = 25 °C, C_o = 100 μF; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5 mA to 500 mA T_j = 25 °C – 40 ≤ T_j ≤ 125 °C	4.80 4.75	5.00 5.00	5.20 5.25	V V
V_I	Operating Input Voltage	(*), Over Full T Range (– 40 to 125 °C) (see note **)			26	V
ΔV_o	Line Regulation	V_i = 6 V to 26 V I_o = 5 mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5 mA to 500 mA		15	60	mV
$V_I - V_o$	Dropout Voltage	$V_O = V_{O\ NOM}$ – 100 mV I_o = 350 mA I_o = 500 mA		 0.40 0.60	 0.65 0.8	 V V
I_q	Quiescent Current	I_o = 0 mA I_o = 150 mA I_o = 350 mA I_o = 500 mA		5 20 60 100	15 35 100 160	mA mA mA mA
		V_i = 6.2 V I_o = 500 mA		160	180	mA
$\frac{\Delta V_o}{\Delta T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Voltage Rejection	I_o = 350 mA f = 120 Hz C_o = 100 μF V_i = 12 V ± 5 V_{pp}			60	
I_{SC}	Output Short Circuit Current			1.2	1.6	A
V_R	Reset Output Voltage	I_R = 3 mA 1 < V_o < 4.70 V I_R = 16 mA 1.5 < V_o < 4.75 V Over Full T (– 40 °C ≤ T_j ≤ 125 °C)			0.5 0.8	V V
I_R	Reset Output Leakage Current	V_o in Regulation V_R = 5V Over Full T Range			50	μA
t_d	Delay Time for Reset Output	Cd = 100 nF Over Full T Range		25		ms
$V_{RT\ (off)}$		V_o @ Reset out H to L Transition, Over Full T Range	4.75	V_o – 0.15		V
I_{C4}	Charging Current (current generator)	V_4 = 3 V	10	20	30	μA
$V_{RT\ (on)}$	Power on V_oThreshold	V_o @ Reset out L to H Transition , Over Full T Range		$V_{RT\ (off)}$ + 0.05 V	V_o – 0.04 V	V
V_4	Comparator Threshold (pin 4)	V_4 @ Reset out H to L Transition	3.2		3.9	V
		V_4 @ Reset out L to H Transition	3.7		4.3	V
V_H	Hysteresis Voltage	Over Full T Range		450		mV

(*) For a DC voltage 26 < Vi < 37 V the device is not operating.
(**) Design limits are guaranteed (but not 100 % production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : Dropout Voltage vs. Output Current.

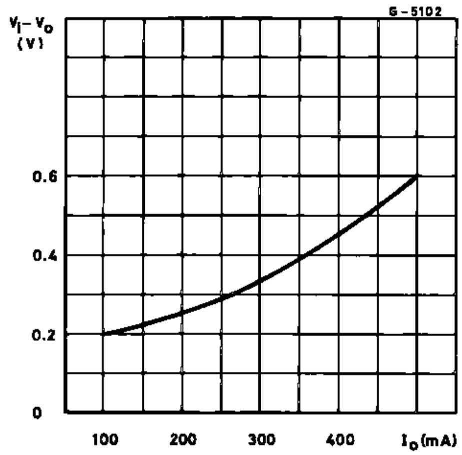


Figure 2 : Quiescent Current vs. Output Current.

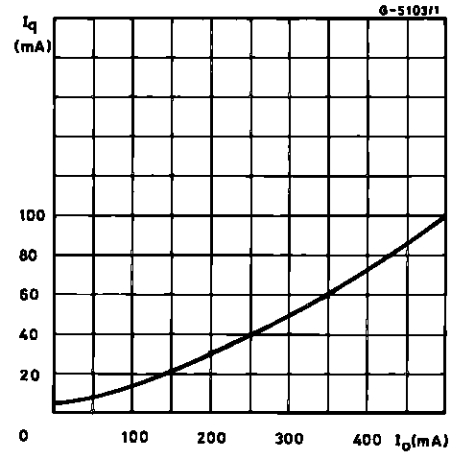
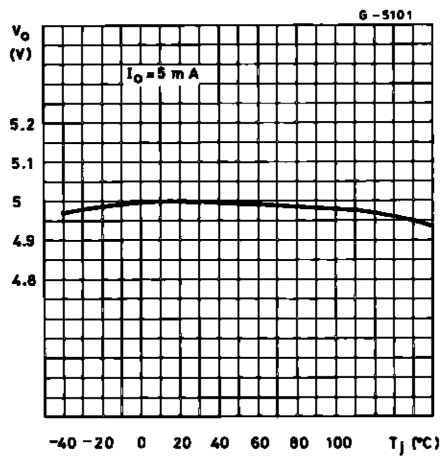
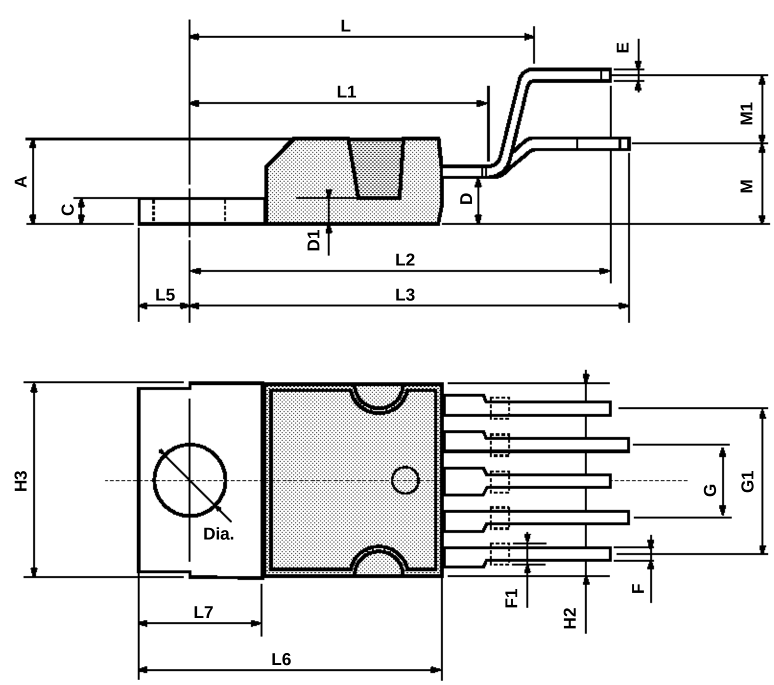


Figure 3 : Output Voltage vs. Temperature.



PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

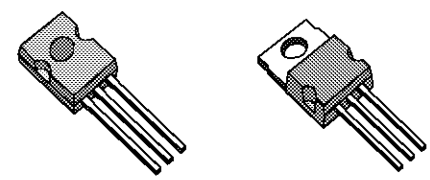


SGS-THOMSON MICROELECTRONICS

L4805-L4885-L4892 L4808-L4810-L4812

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.4V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION (± 60V)
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN



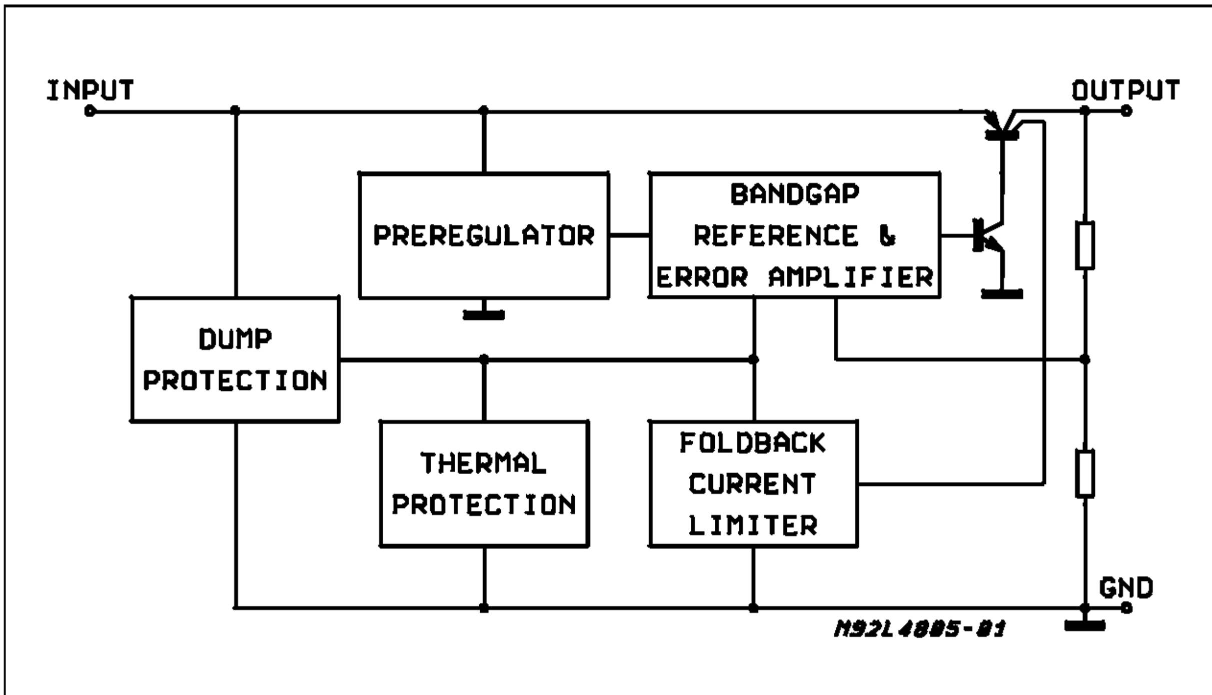
SOT-82 TO-220

DESCRIPTION

L4800 series devices are voltage regulators with a very low voltage drop (typically 0.4V at full rated current), output current up to 400mA, low quiescent current and comprehensive on-chip protection. These devices are protected against load dump and field decay transients of ± 60V, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V, 9.2V, 10V and 12V versions (all ± 4%, $T_l = 25°C$) these regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In automotive applications the L4805 is ideal for 5V logic supplies because it can operate even when the battery voltage falls below 6V. In battery backup and standby applications the low consumption of these devices extends battery life.

BLOCK DIAGRAM



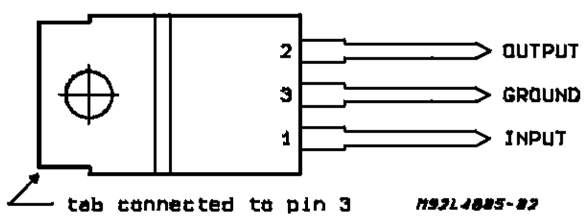
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	+ 35	V
	DC Input Reverse Voltage	- 18	V
	Transient Input Overvoltages : Load Dump : 5ms $\leq T_{rise} \leq$ 10ms, τ_f Fall Time Constant = 100ms, $R_{source} \leq 0.5\Omega$	60	V
	Field Decay : 5ms $\leq t_{fall} \leq$ 10ms, $R_{source} \leq 10\Omega$ τ_r Rise Time Constant = 33ms	- 60	V
T_j, T_{stg}	Junction and Storage Temperature Range	- 55 to + 150	°C

THERMAL DATA

Symbol	Parameter		SOT82	TO220	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	8	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	75	°C/W

PIN CONNECTION (top view)



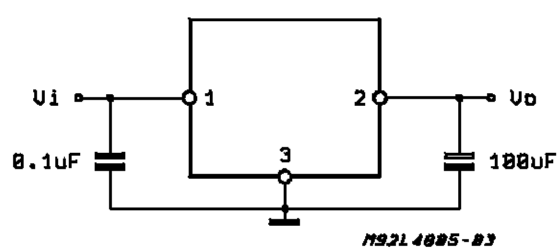
Order Codes		Output Voltage
TO-220	SOT-82	
L4805CV	L4805CX	5V
L4808CV	L4808CX	8V
L4885CV	L4885CX	8.5 V
L4892CV	L4892CX	9.2 V
L4810CV	L4810CX	10 V
L4812CV	L4812CX	12 V

TEST AND APPLICATION CIRCUIT

The output capacitor is required for stability. Though the 100 µF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristics of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than – 30 °C, reducing their effective capacitance to zero. To maintain regulator stability down to – 40 °C, capacitors rated at that temperature (such as tantalums) must be used.



ELECTRICAL CHARACTERISTICS (V_I = 14.4V; C_O = 100µF; T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	I_O = 5mA to 400mA (L4805)	4.80	5.00	5.20	V
		I_O = 5mA to 400mA (L4808)	7.68	8.00	8.32	V
		I_O = 5mA to 400mA (L4810)	8.16	8.50	8.84	V
		I_O = 5mA to 400mA (L4812)	8.83	9.20	9.57	V
		I_O = 5mA to 400mA (L4885)	9.60	10.00	10.40	V
		I_O = 300mA (L4892)	11.50	12.00	12.50	V
V_I	Operating Input Voltage				26	V
$\Delta V_O/V_O$	Line Regulation	VI = 13 to 26V; I_O = 5mA		1	10	mV/V
$\Delta V_O/V_O$	Load Regulation	IO = 5 to 400mA*		3	15	mV/V
V_I - V_O	Dropout Voltage	I_O = 400mA*		0.4	0.7	V
		I_O = 150mA		0.2	0.4	V
I_q	Quiescent Current	I_O = 0mA		0.8	2	mA
		I_O = 150mA		25	45	mA
		I_O = 400mA*		65	90	mA
$\frac{\Delta V_O}{\Delta T \bullet V_O}$	Temperature Output Voltage Drift			0.1		$\frac{mV}{°C \bullet V}$
SVR	Supply Voltage Rejection	I_O = 350mA; f = 320Hz; C_O = 100µF; V_I = V_O +3V+2V_{pp}		60		dB
I_O	Max Output Current			800		mA
I_{SC}	Output Short Circuit Current (fold back condition)			350	500	mA

* only for L4892 the current test conditions is I_O = 300mA

ELECTRICAL CHARACTERISTICS (V_I = 14.4V; C_O = 100µF; T_j = -40 to 125°C (note 1) unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	I_O = 5mA to 400mA (L4805)	4.70	5.00	5.30	V
		I_O = 5mA to 400mA (L4808)	7.50	8.00	8.50	V
		I_O = 5mA to 400mA (L4810)	8.00	8.50	9.00	V
		I_O = 5mA to 400mA (L4812)	8.65	9.20	9.75	V
		I_O = 5mA to 400mA (L4885)	9.40	10.00	10.60	V
		I_O = 300mA (L4892)	11.30	12.00	12.70	V
V_I	Operating Input Voltage	see note 2			26	V
$\Delta V_O/V_O$	Line Regulation	VI = 14 to 26V; I_O = 5mA		2	15	mV/V
$\Delta V_O/V_O$	Load Regulation	IO = 5 to 400mA*		5	25	mV/V
V_I - V_O	Dropout Voltage	I_O = 400mA*		0.5	0.9	V
		I_O = 150mA		0.25	0.5	V
I_q	Quiescent Current	I_O = 0mA		1.2	3	mA
		I_O = 150mA		40	70	mA
		I_O = 400mA*		80	140	mA
I_O	Max Output Current			870		mA
I_{SC}	Output Short Circuit Current (fold back condition)			230		mA

Notes : 1. This limits are guaranteed by design, correlation and statistical control on production samples over the indicated temperature and supply voltage ranges..
2. For a DC voltage 26V < Vi < 35V the device is not operating.

Figure 1: Dropout Voltage vs. Output Current

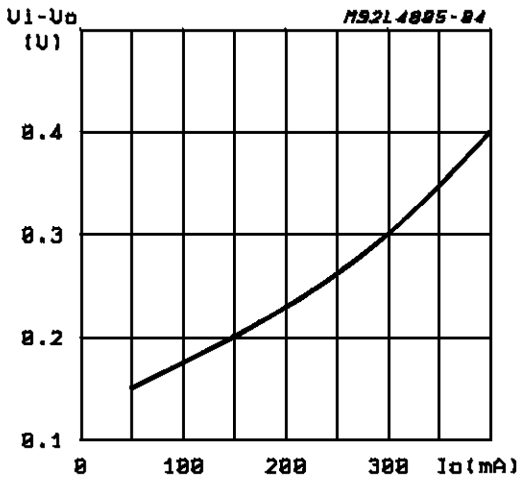


Figure 2: Quiescent Current vs. Output Current

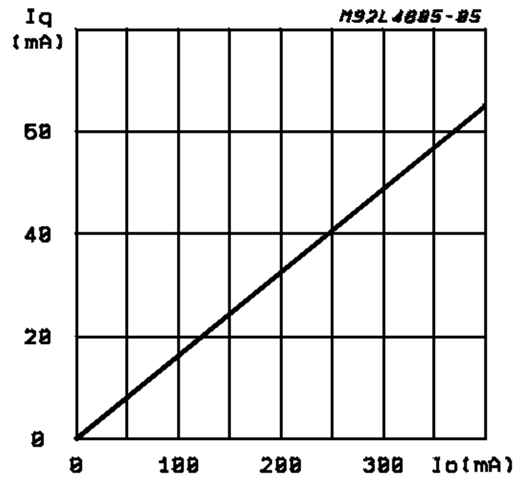


Figure 3: Output Voltage vs. Temperature

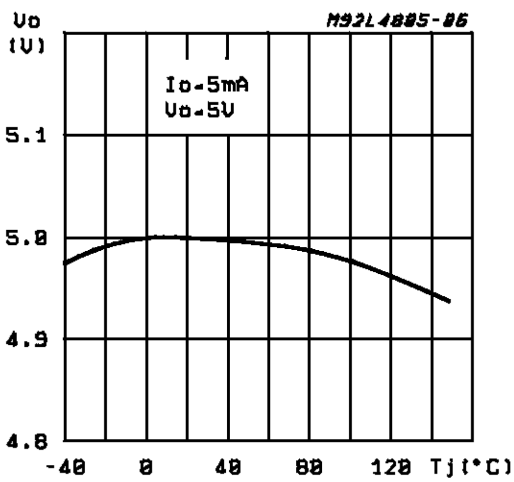


Figure 4: Foldback Current Limiting(L4805)

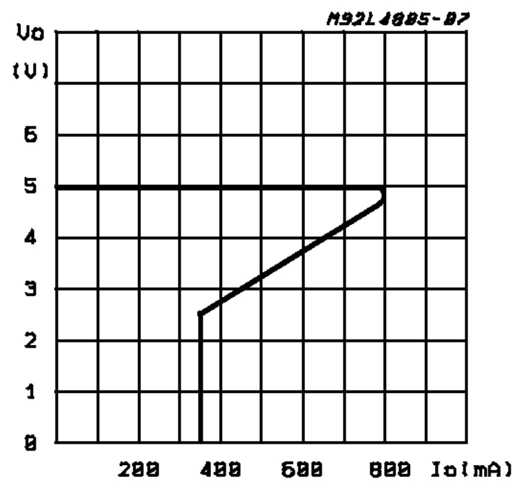
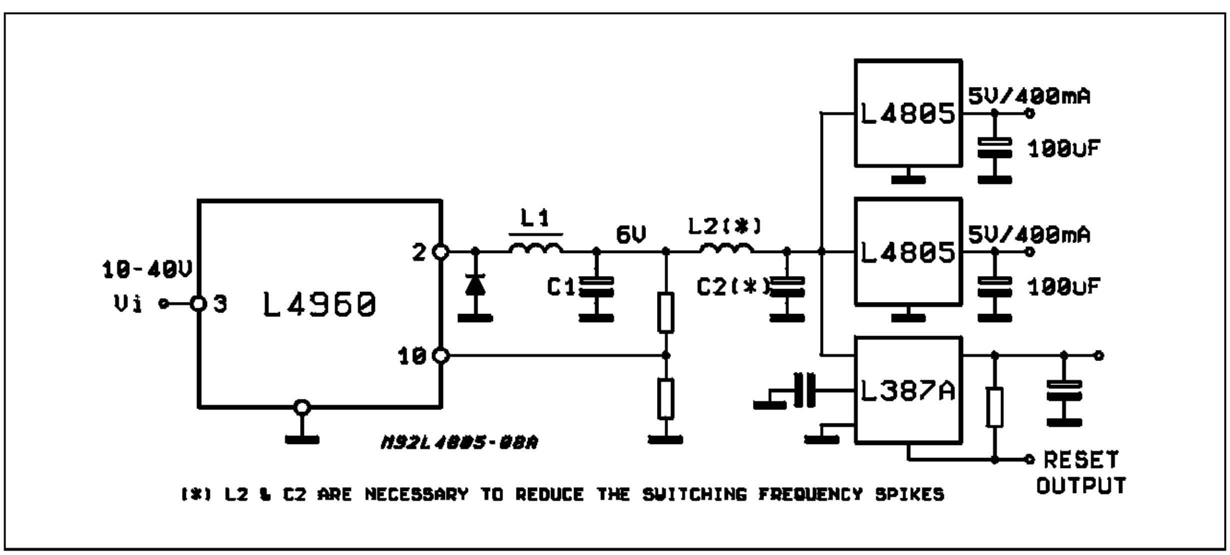
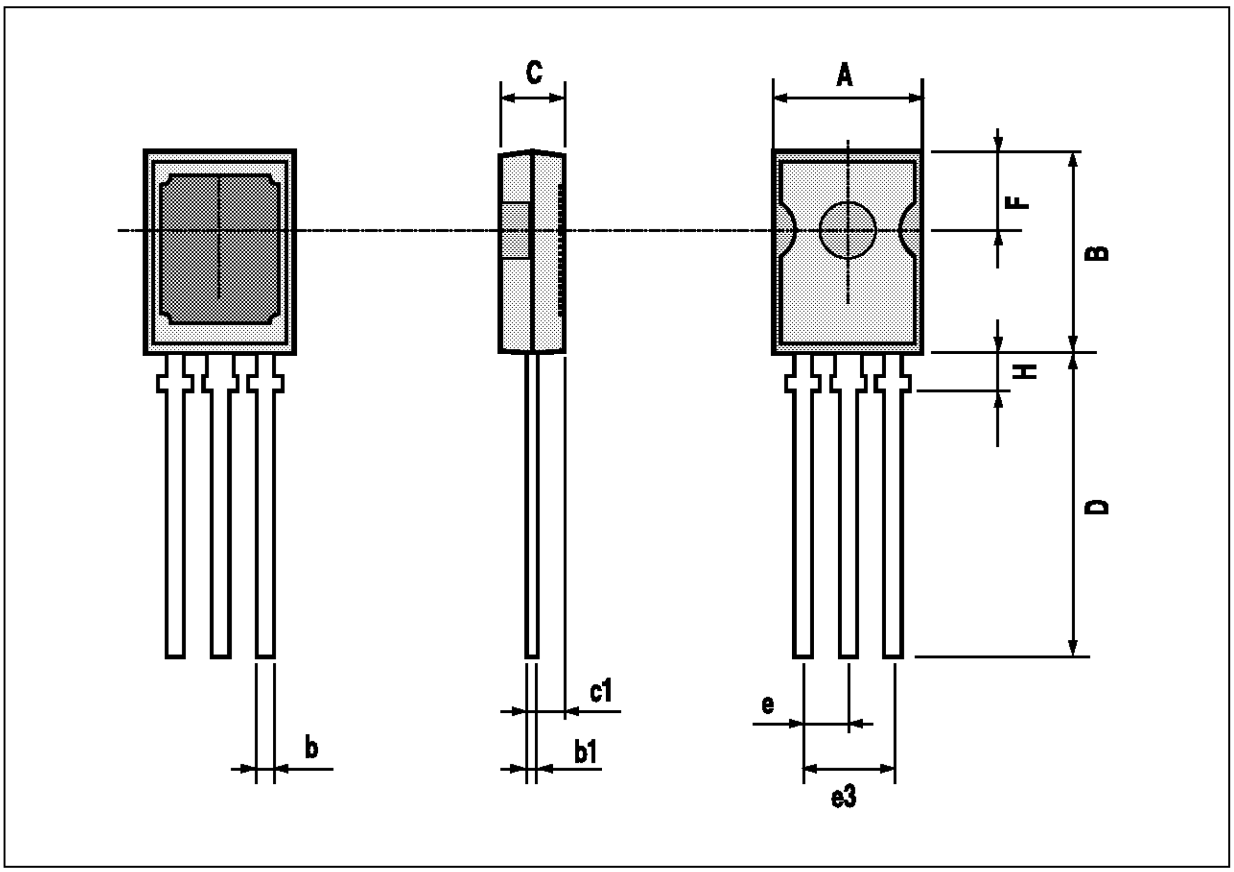


Figure 5: Preregulator for Distributed Supplies



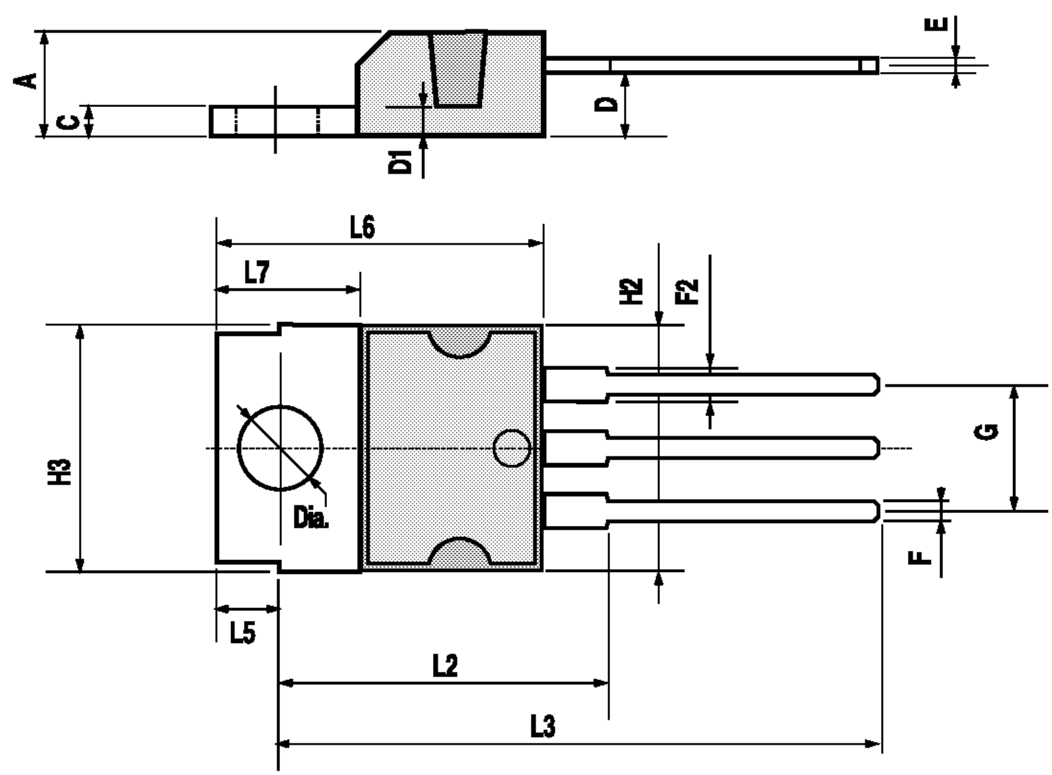
SOT82 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.425
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
D		15.7			0.618	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54			0.100



TO220 PACKAGE MECHANICAL DATA

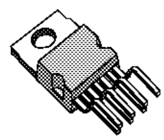
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152



DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS : I_{01} = 400mA
  $I_{0\,2}$ = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1µA AT OUTPUT 1
- LOW QUIESCENT CURRENT (Input 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SO A PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION



HEPTAWATT (Vertical)
(Plastic Package)

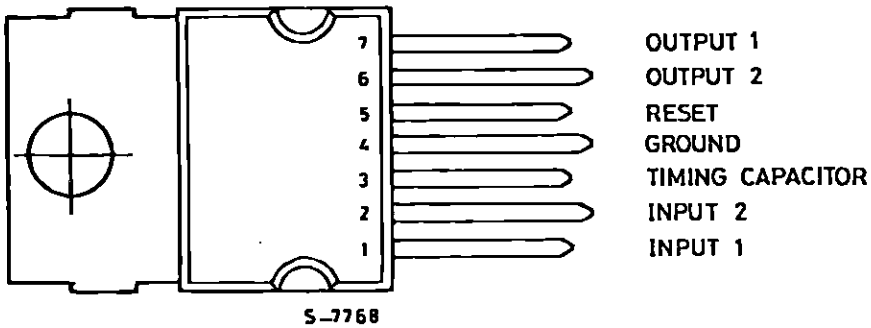
ORDERING NUMBER : L4901A

DESCRIPTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

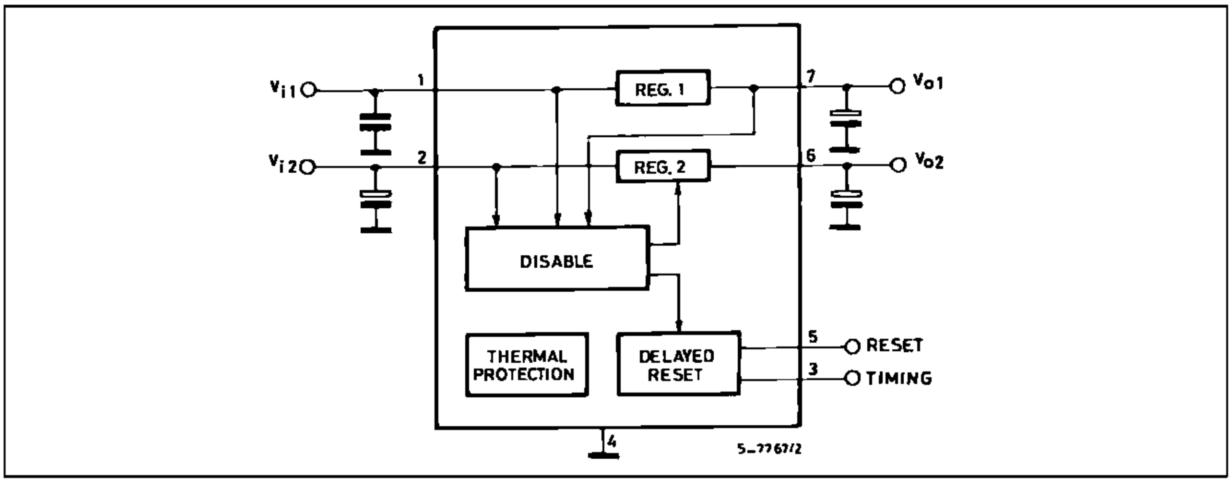
PIN CONNECTION



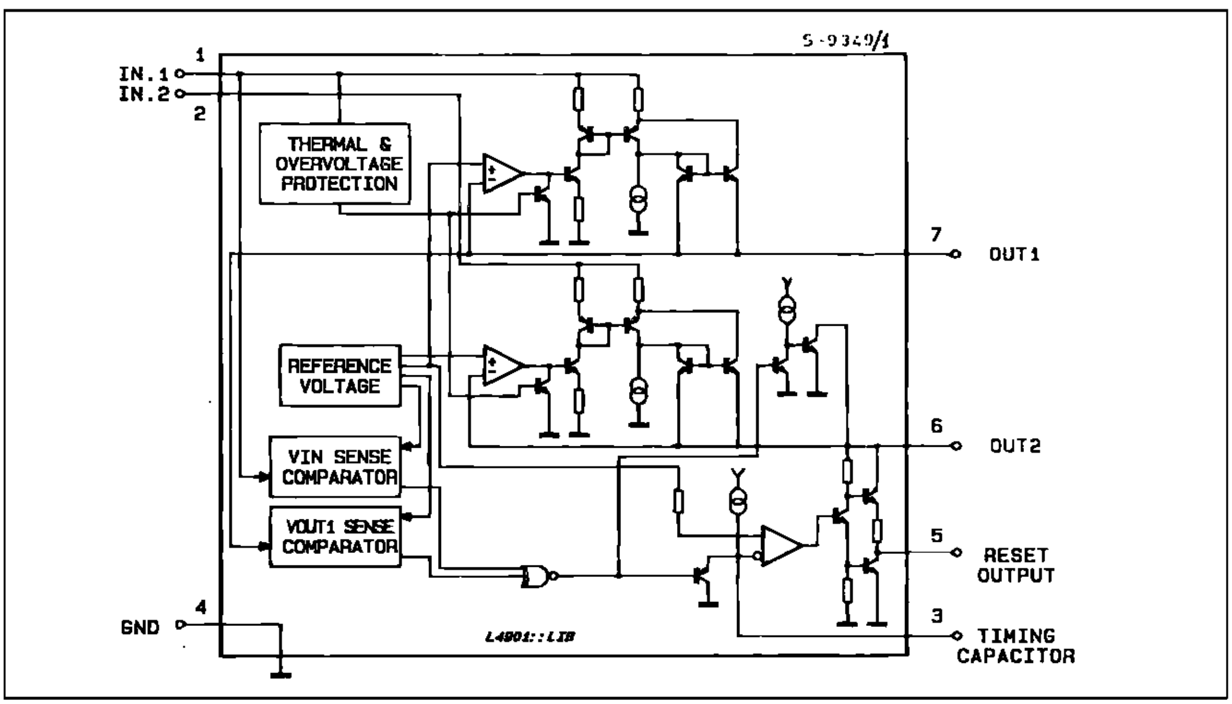
PIN DESCRIPTION

N°	Name	Function
1	Input 1	Low Quiescent Current 400mA Regulator Input.
2	Input 2	400mA regulator input.
3	Timing Capacitor	If Reg. 2 is switched-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is decharged.
4	GND	Common Ground.
5	Reset Output	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF)
6	Output 2	5V – 400mA Regulator Output. Enabled if $V_o 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	Output 1	5V – 400mA regulator output with Low leakage (in switch-OFF condition).

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Transient Input Overvoltage (t = 40ms)	24 60	V V
I_o	Output Current	Internally Limited	
T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

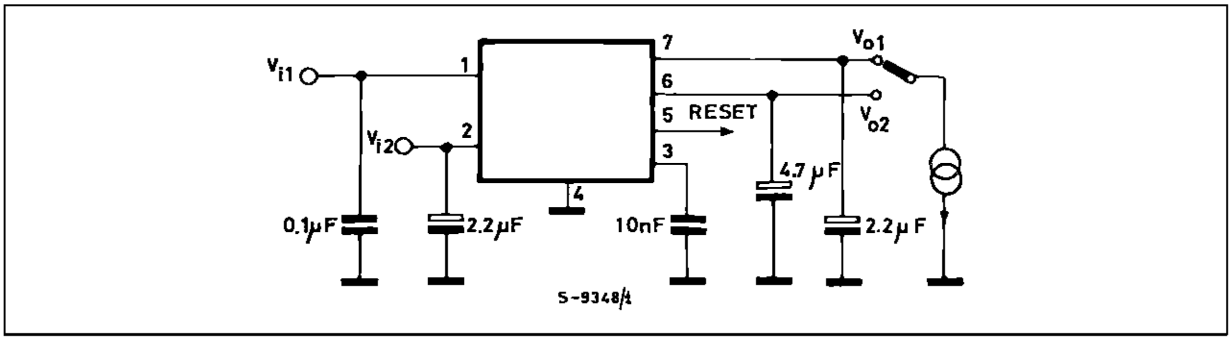
Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}c)}$	Thermal Resistance Junction-case	Max.	4	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 14, 4V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC Operating Input Voltage				20	V
V_{01}	Output Voltage 1	R Load 1kΩ	4.95	5.05	5.15	V
$V_{02\ H}$	Output Voltage 2 HIGH	R Load 1kΩ	V_{01} –0.1	5	V_{01}	V
$V_{02\ L}$	Output Voltage 2 LOW	I_{02} = – 5mA		0.1		V
I_{01}	Output Current 1	ΔV_{01} = – 100mV	400			mA
I_{L01}	Leakage Output 1 Current	V_{IN} = 0, $V_{01} \leq$ 3V			1	µA
I_{02}	Output Current 2	ΔV_{02} = – 100mV	400			mA
V_{I01}	Output 1 Dropout Voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input Threshold Voltage		V_{01} + 1.2	6.4	V_{01} + 1.7	V
V_{ITH}	Input Threshold Voltage Hyst.			250		mV
ΔV_{01}	Line Regulation 1	7V < V_{IN} < 18V, I_{01} = 5mA		5	50	mV
ΔV_{02}	Line Regulation 2	7V < V_{IN} < 18V, I_{02} = 5mA		5	50	mV
ΔV_{01}	Load Regulation 1	5mA < I_{01} < 400mA		50	100	mV
ΔV_{02}	Load Regulation 2	5mA < I_{01} < 400mA		50	100	mV
I_Q	Quiescent Current	I_{02} = $I_{01} \leq$ 5mA 0 < V_{IN} < 13V 7V < V_{IN} < 13V		 4.5 1.6	 6.5 3.5	mA
I_{Q1}	Quiescent Current 1	$I_{01} \leq$ 5mA, I_{02} = 0, V_{IN2} = 0 6.3V < V_{IN} < 13V		0.6	0.9	mA
V_{RT}	Reset Threshold Voltage		V_{02} – 0.15	4.9	V_{02} –0.05	V
V_{RTH}	Reset Threshold Hysteresis		30	50	80	mV
V_{RH}	Reset Output Voltage HIGH	I_R = 500µA	V_{02} – 1	4.12	V_{02}	V
V_{RL}	Reset Output Voltage LOW	I_R = –<0>5mA		0.25	0.4	V
t_{RD}	Reset Pulse Delay	C_t = 10nF	3	5	11	ms
t_d	Timing Capacitor Discharge Time	C_t = 10nF			20	µs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
SVR1	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V Io = 100mA	50	84		dB
SVR2	Supply Voltage Rejection		50	80		dB
T_{JSD}	Thermal Shut Down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25 mV under constant output current condition.

TEST CIRCUIT



APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments ; it provides two voltage regulators (both 5 V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Figure 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs :

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$) ;
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$) ;

and they start again as before when the condition is removed.

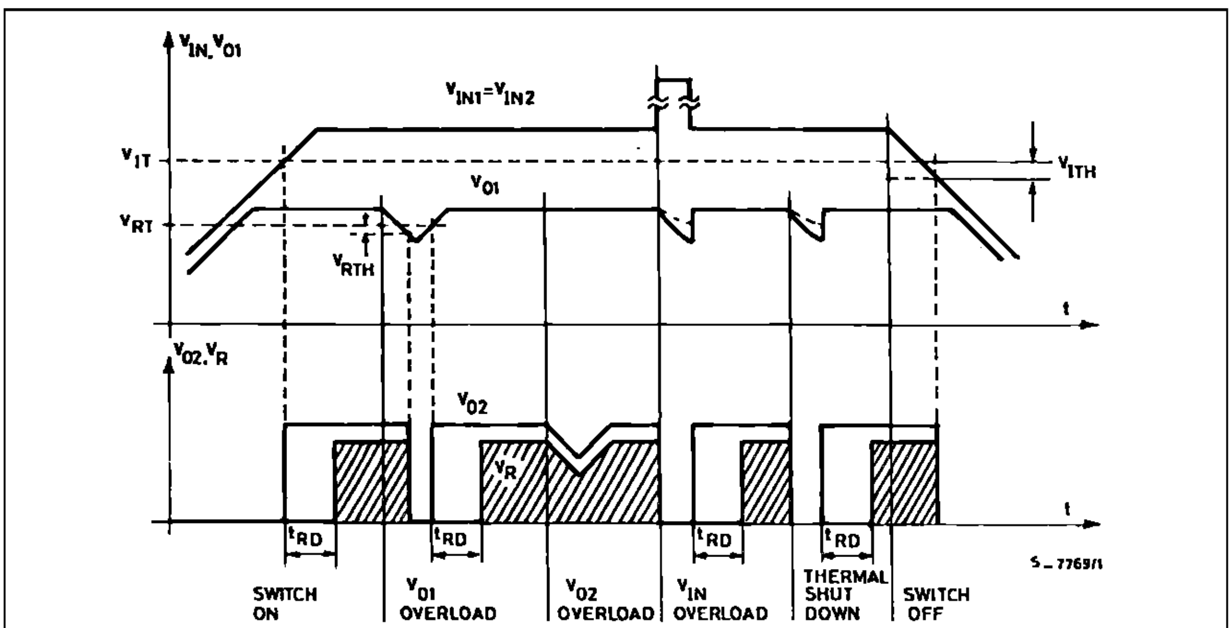
An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features :

- 5 V internal reference without voltage divider between the output and the error comparator ;
- very low drop series regulator element utilizing current mirrors ;

permit high output impedance and then very low leakage current error even in power down condition.

Figure 1



This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6 mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5 V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

APPLICATIONS SUGGESTIONS

Figure 2 shows an application circuit for a µP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Figure 2

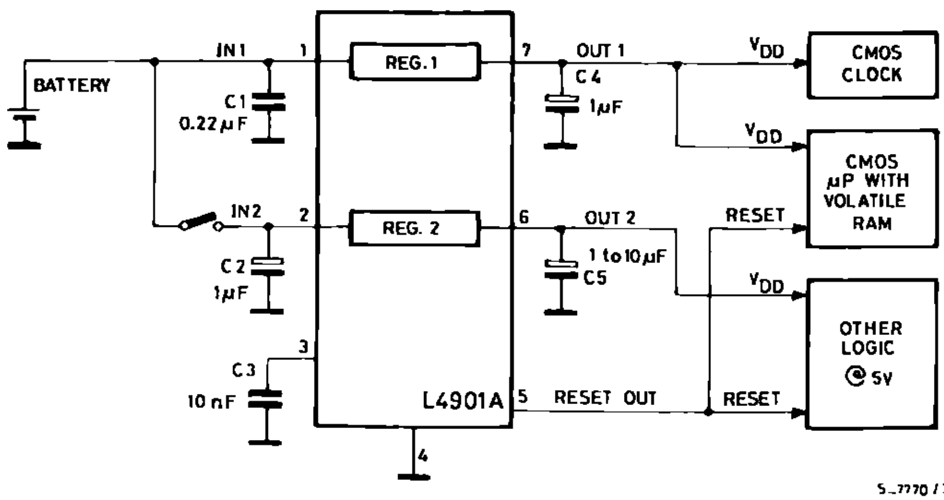


Figure 3 : P.C. Board Component Layout of Figure 2.

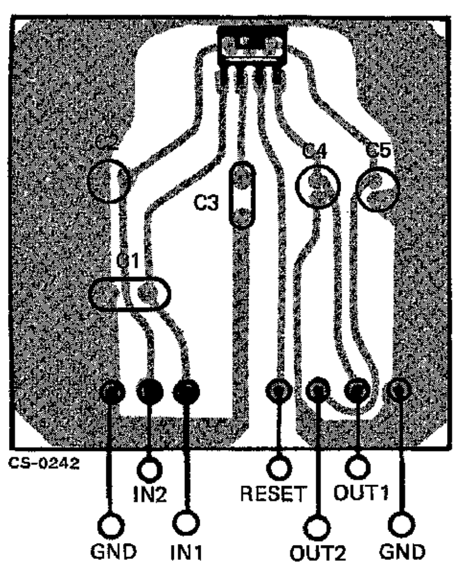


Figure 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS µP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in Figure 5 the reset output is used both to disable the µP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Figure 4

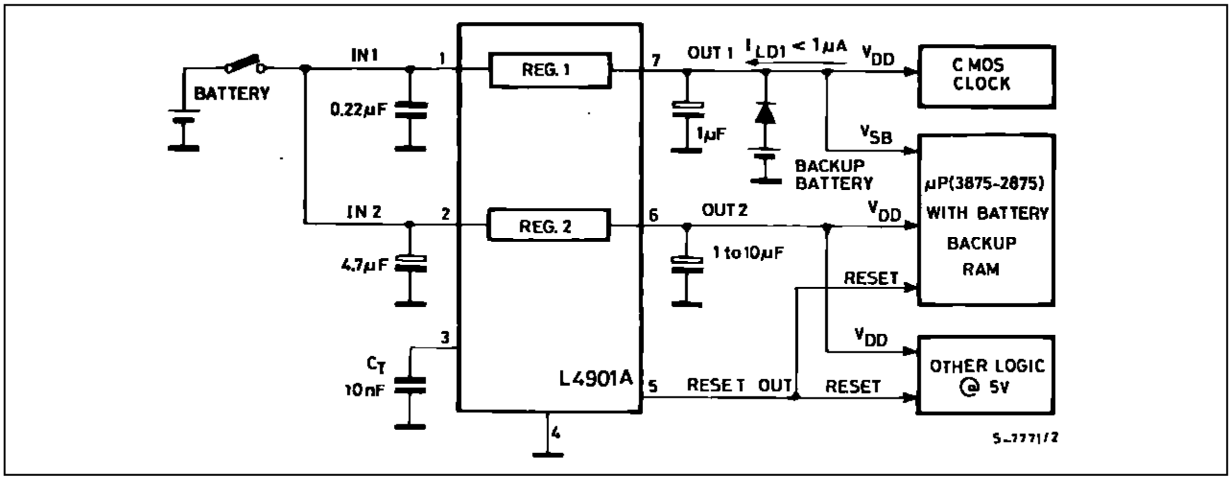
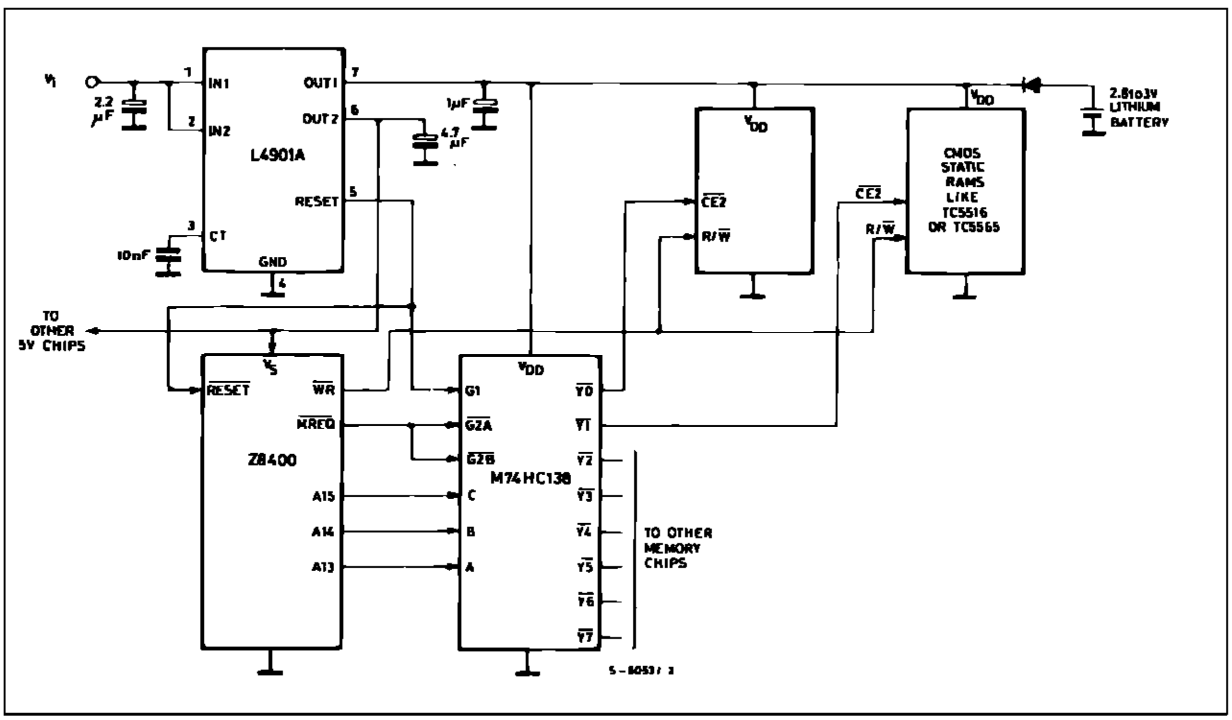


Figure 5



Another interesting application of the L4901A is in µP system with shadow memories (see Figure 6). When the input voltage goes below V_{IT}, the reset ouput enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680 µF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_1 occurs.

Figure 6

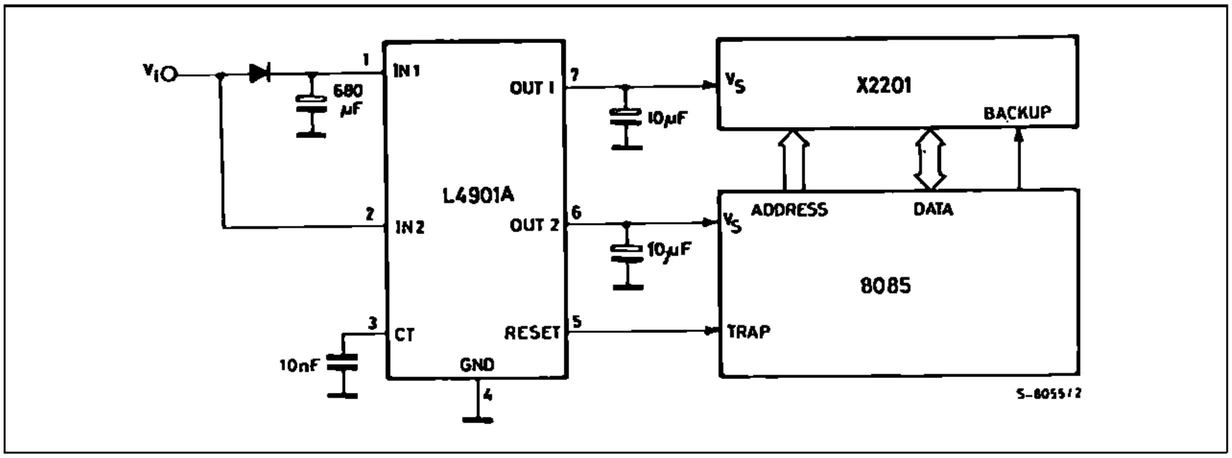


Figure 7 : Quiescent Current (reg.1) versus Output Current

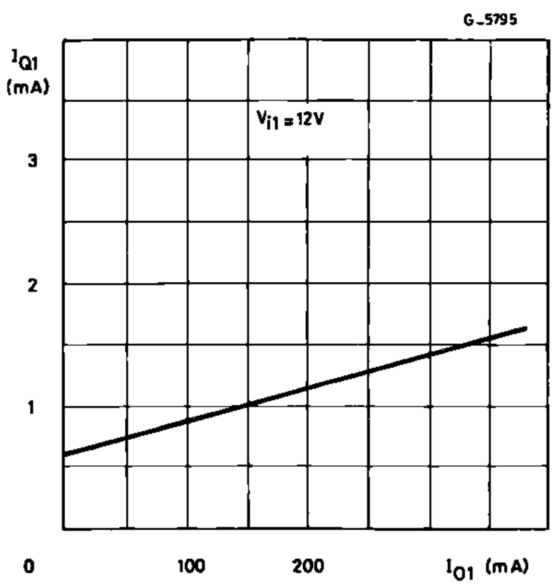


Figure 8 : Quiescent Current (reg.1) versus Input Voltage

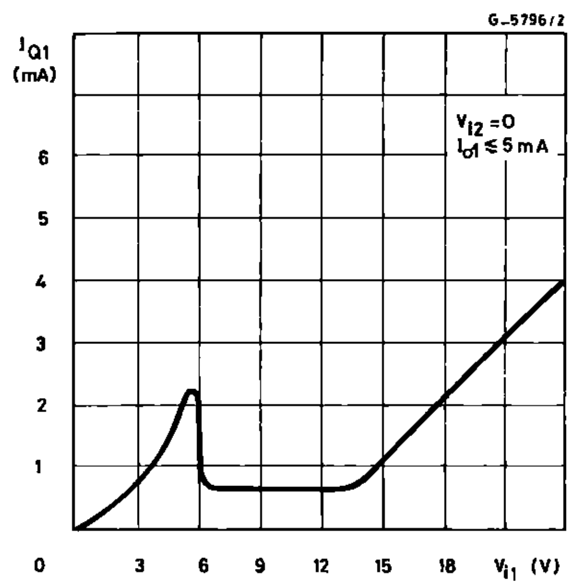


Figure 9 : Total Quiescent Current versus Input Voltage

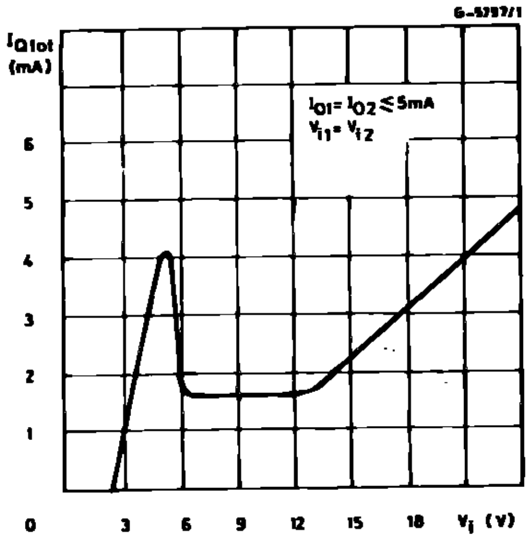


Figure 10 : Regulator 1 Output Current and Short Circuit Current versus Input Voltage

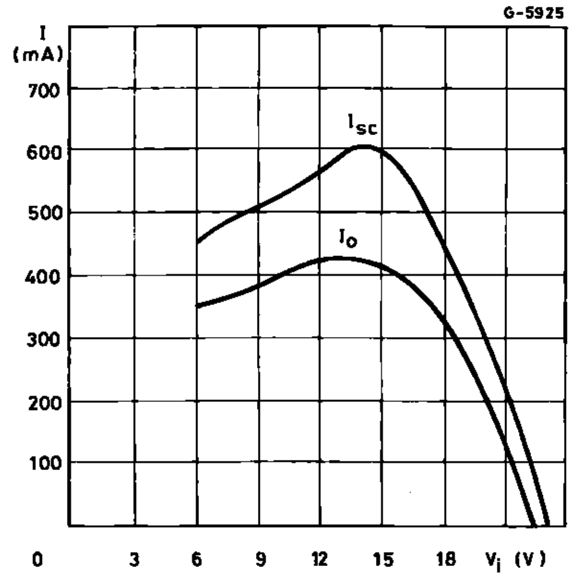


Figure 11 : Regulator 1 Output Current and Short Circuit Current versus Input Voltage

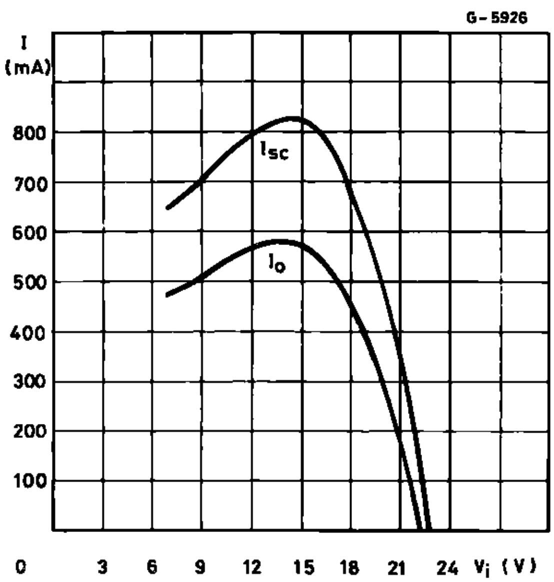
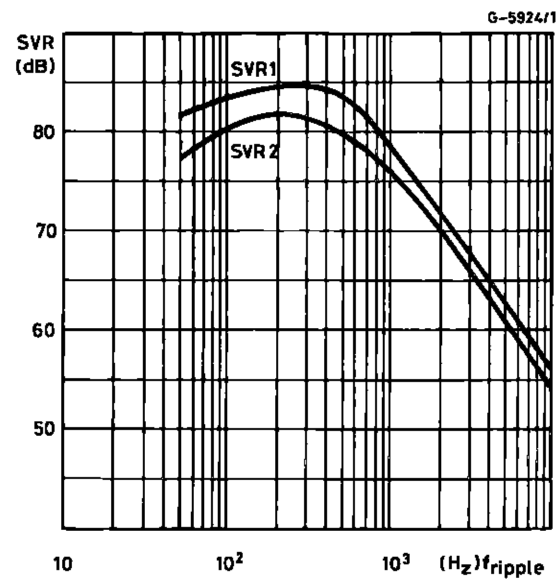
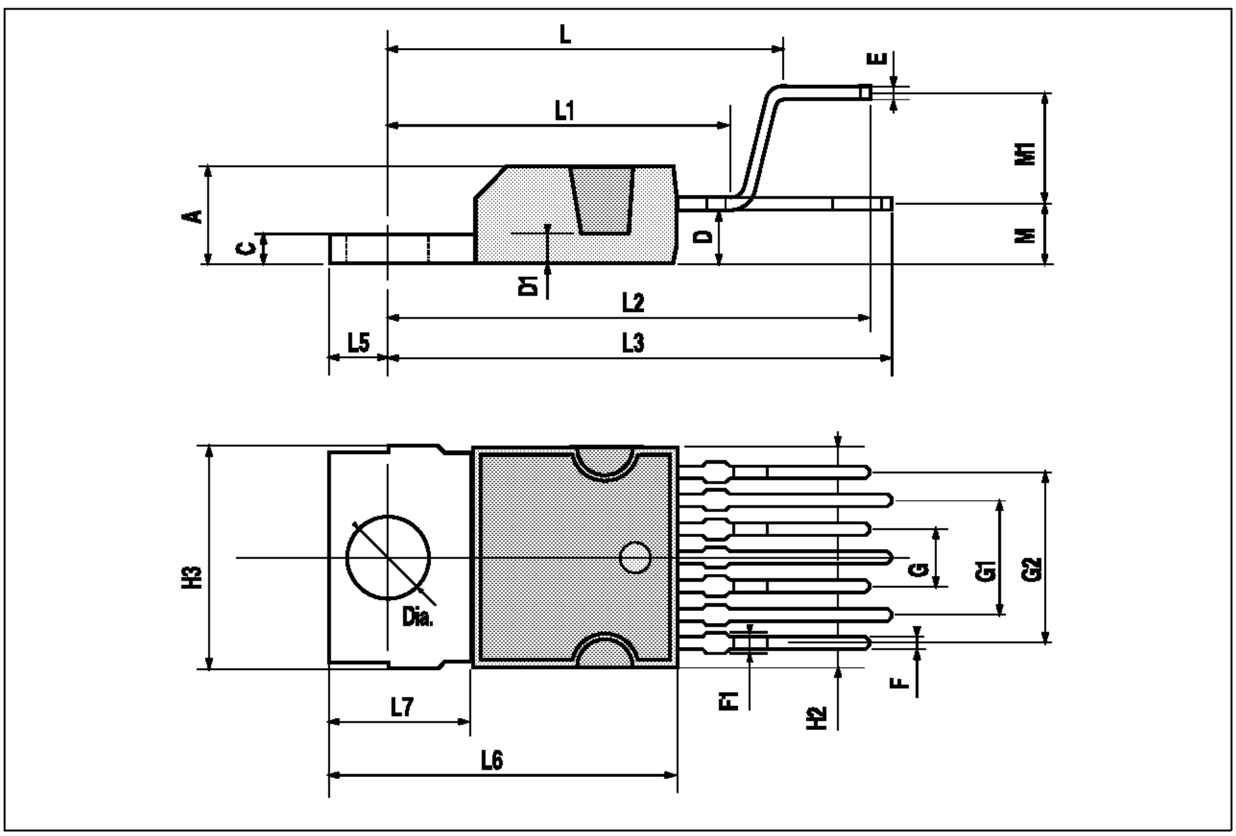


Figure 12 : Supply Voltage Rejection Regulators 1 and 2 versus Input Ripple Frequence



HEPTAVATT PACKAGE MECHANICAL DATA

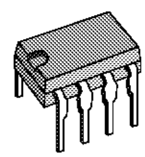
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152



DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS : I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2 %
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1µA AT OUTPUT 1
- LOW QUIESCENT CURRENT (Input 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION



Minidip

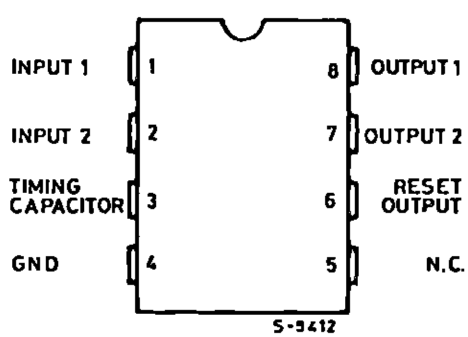
ORDERING NUMBER : L4904A

DESCRIPTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

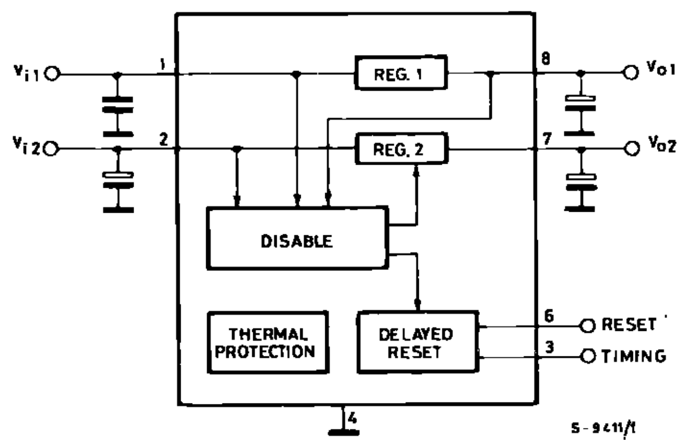
PIN CONNECTION



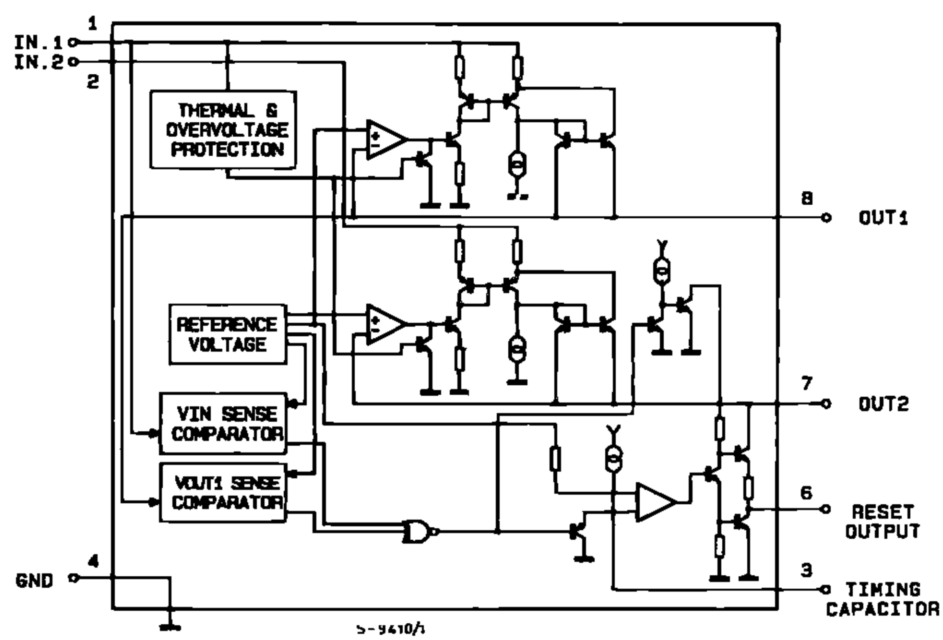
PIN FUNCTIONS

N°	Name	Function
1	Input 1	Low Quiescent Current 50mA Regulator Input.
2	Input 2	100mA Regulator Input.
3	Timing Capacitor	If Reg. 2 is switching-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common Ground.
5	N.C.	Not connected.
6	Reset Output	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	Output 2	5V – 100mA Regulator Output. Enabled if $V_{o\,1} > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{o2} capacitor is discharged.
8	Output 1	5V – 50mA regulator output with low leakage in switch-OFF condition.

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Transient Input Overvoltage (t = 40ms)	24 60	V V
I_o	Output Current	Internally Limited	
P_{tot}	Power Dissipation at T_{amb} = 50°C	1	W
T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC Operating Input Voltage				20	V
V_{01}	Output Voltage 1	R Load 1kΩ	4.95	5.05	5.15	V
$V_{02\ H}$	Output Voltage 2 HIGH	R Load 1kΩ	V_{01} –0.1	5	V_{01}	V
$V_{02\ L}$	Output Voltage 2 LOW	I_{02} = – 5mA		0.1		V
I_{01}	Output Current 1	ΔV_{01} = – 100mV	50			mA
I_{L01}	Leakage Output 1 Current	V_{IN} = 0, $V_{01} \leq$ 3V			1	µA
I_{02}	Output Current 2	ΔV_{02} = – 100mV	100			mA
V_{I01}	Output 1 Dropout Voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input Threshold Voltage		V_{01} + 1.2	6.4	V_{01} + 1.7	V
V_{ITH}	Input Threshold Voltage Hyst.			250		mV
ΔV_{01}	Line Regulation	7V < V_{IN} < 18V, I_{01} = 5mA		5	50	mV
ΔV_{02}	Line Regulation 2	7V < V_{IN} < 18V, I_{02} = 5mA		5	50	mV
ΔV_{01}	Load Regulation 1	V_{IN} = 8V, 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load Regulation 2	V_{IN} = 8V, 5mA < I_{02} < 100mA		10	50	mV
IQ	Quiescent Current	$I_{02} = I_{01} \leq$ 5mA 0 < V_{IN} < 13V 7V < V_{IN} < 13V		 4.5 1.6	 6.5 3.5	mA
I_{Q1}	Quiescent Current 1	6.3V < V_{IN1} < 13V, V_{IN2} = 0 $I_{01} \leq$ 5mA, I_{02} = 0		0.6	0.9	mA
V_{RT}	Reset Threshold Voltage		V_{02} –0.15	4.9	V_{02} – 0.05	V
V_{RTH}	Reset Threshold Hysteresis		30	50	80	mV
V_{RH}	Reset Output Voltage HIGH	I_R = 500µA	V_{02} – 1	4.12	V_{02}	V
V_{RL}	Reset Output Voltage LOW	I_R = – 5mA		0.25	0.4	V
t_{RD}	Reset Pulse Delay	C_t = 10nF	3		11	ms
t_d	Timing Capacitor Discharge Time	C_t = 10nF			20	µs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal Drift	– 20°C ≤<0>T_{amb} ≤ 125°C		0.3 –0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal Drift	– 20°C ≤<0>T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
S_{VR1}	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V, I_o = 50mA	50	84		dB
S_{VR2}	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal Shut Down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25 mV under constant output current condition.

TEST CIRCUIT

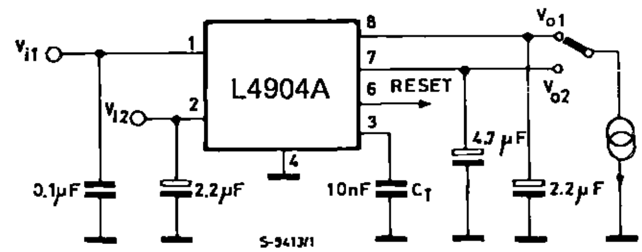
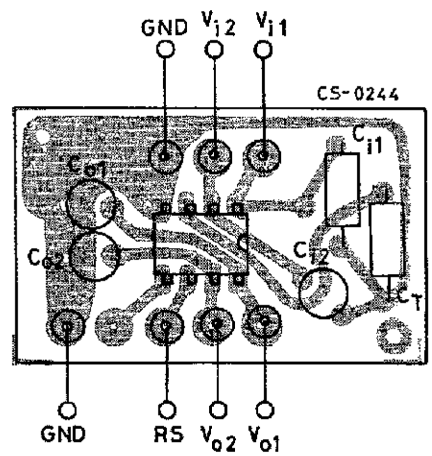


Figure 1 : P.C. Board and Components Layout of the Test Circuit (1:1 scale)



APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments ; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Figure 2)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs :
- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$) ;
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$) ;

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features :
- 5 V internal reference without voltage divider between the output and the error comparator ;
- very low drop series regulator element utilizing mirrors ;

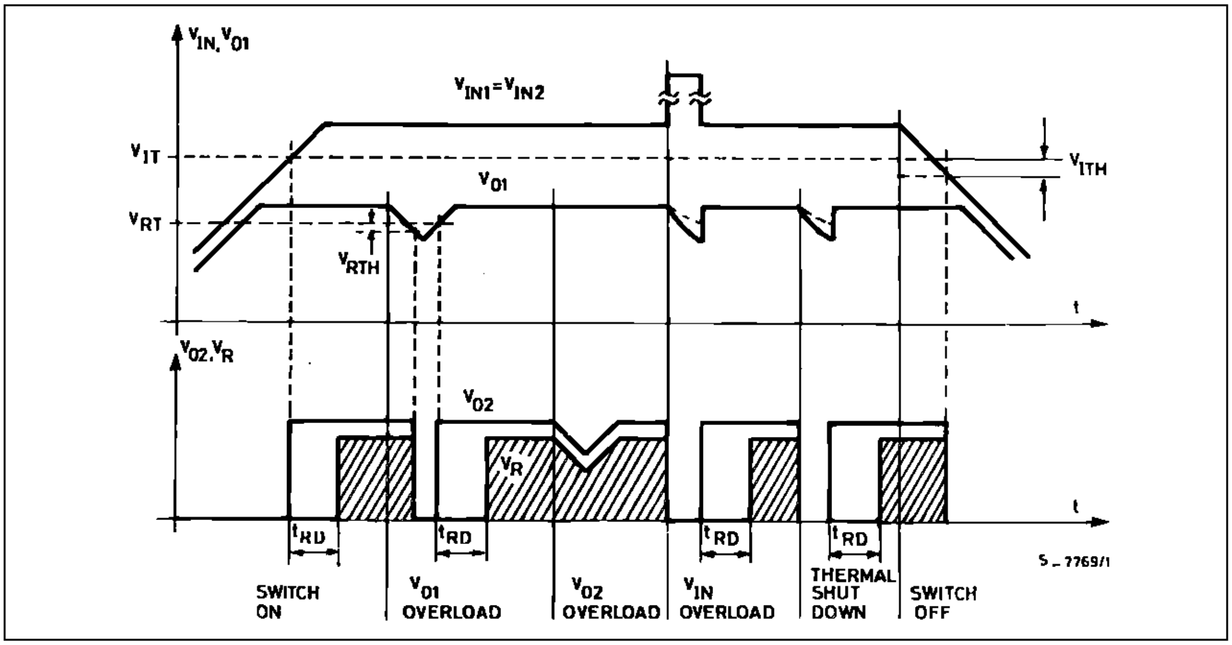
permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6 mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5 V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Figure 2



APPLICATION SUGGESTIONS

Figure 3 shows an application circuit for a µP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Figure 4 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS µP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

Application Circuits of a Microprocessor system (Figure 3) or with data save battery (Figure 4). The reset output provide delayed rising front at the turn-off of the regulator 2.

Figure 3

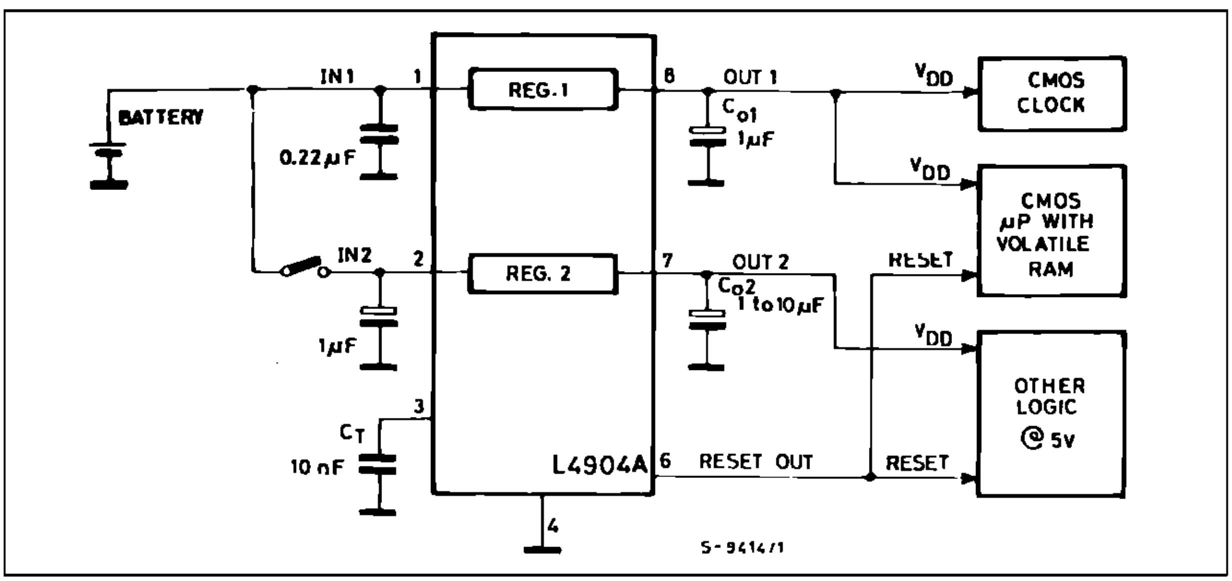


Figure 4

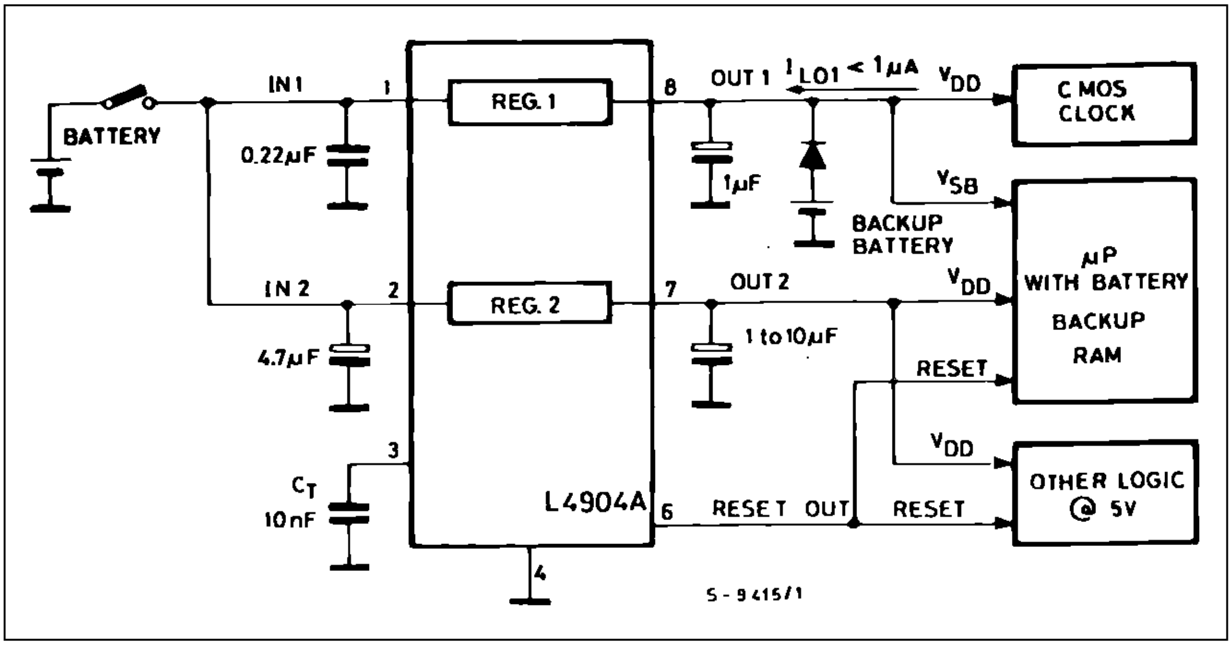

BATTERY
IN1
0.22µF
1
REG. 1
8
OUT 1
I LO1 < 1µA
VDD
C MOS
CLOCK
1µF
VSB
BACKUP
BATTERY
IN 2
2
REG. 2
7
OUT 2
VDD
µP
WITH BATTERY
BACKUP
RAM
4.7µF
1 to 10µF
RESET
VDD
3
CT
10nF
L4904A
6
RESET OUT
RESET
OTHER LOGIC
@ 5V
4
S - 9415/1

Figure 5 : Quiescent Current (reg. 1) versus Output Current

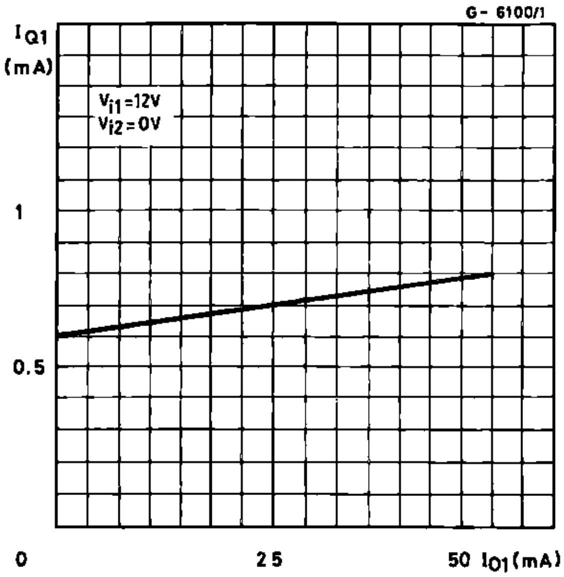


Figure 6 : Quiescent Current (reg. 1 versus Input Voltage

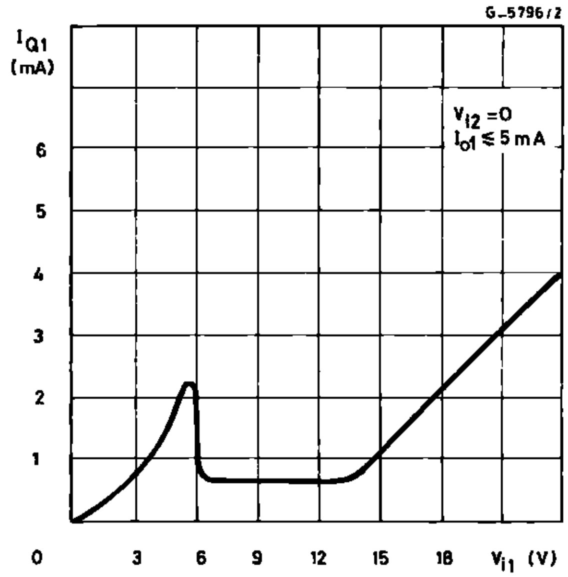


Figure 7 : Total Quiescent Current versus Input Voltage

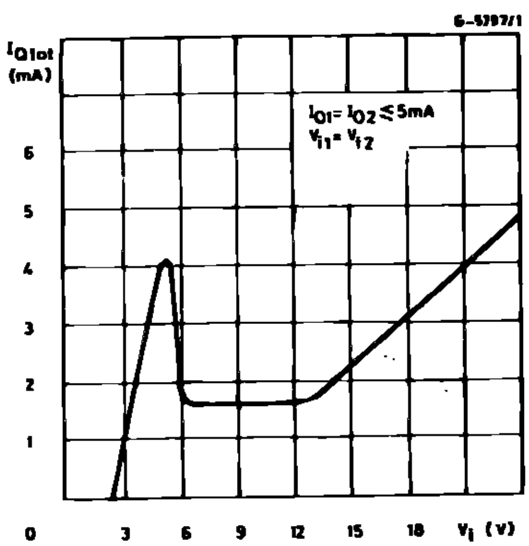
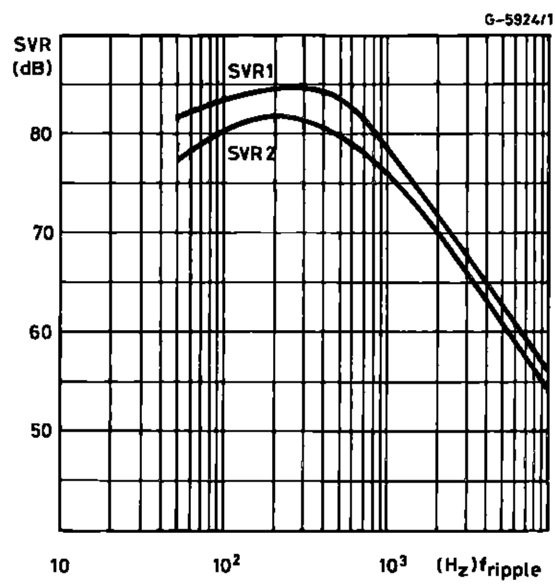
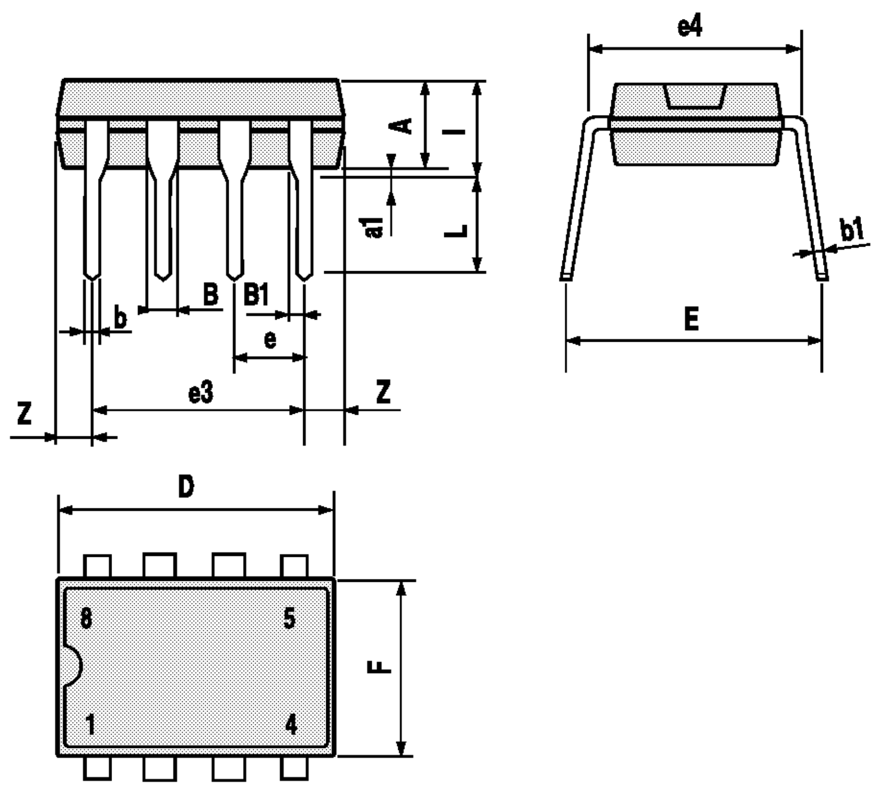


Figure 8 : Supply Voltage Rejection Regulators 1 and 2 versus Input Ripple Frequence



MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

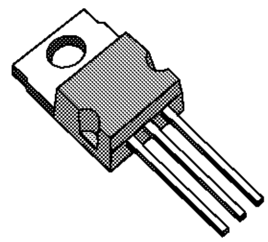


SGS-THOMSON MICROELECTRONICS

L4940 SERIES

VERY LOW DROP 1.5 A REGULATORS

- PRECISE 5 V, 8.5 V, 10 V, 12 V OUTPUTS
- LOW DROPOUT VOLTAGE (500 mV typ at 1.5A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHOUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION

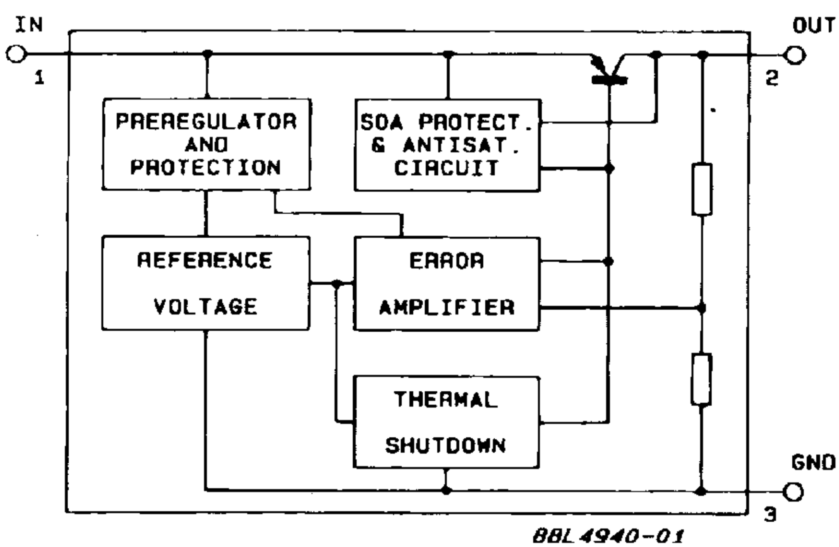


TO-220

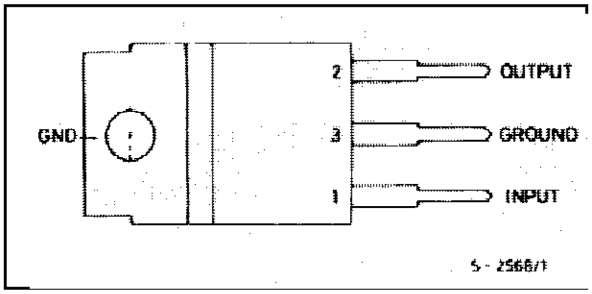
DESCRIPTION

The L4940 series of three terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of industrial and consumer applications. Thanks to its very low input/output voltage drop, these devices are particularly suitable for battery powered equipments, reducing consumption and prolonging battery life. Each type employs internal current limiting, antisaturation circuit, thermal shutdown and safe area protection.

APPLICATION CIRCUIT



PIN CONNECTION AND ORDER CODES



ORDERING NUMBERS	OUTPUT VOLTAGE
L4940V5	5V
L4940V85	8.5V
L4940V10	10V
L4940V12	12V

ABSOLUTE MAXIMUM RATING

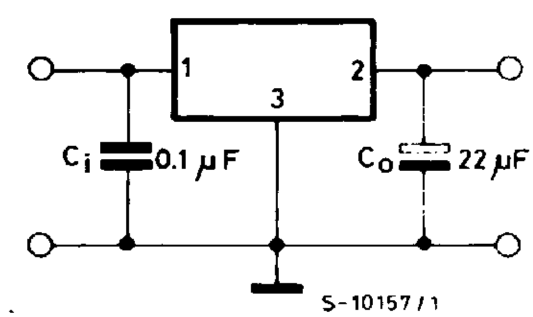
Symbol	Description			Values	Unit
V_I	Forward Input Voltage			30	V
V_{IR}	Reverse Input Voltage	V_O = 5 V	R_O = 100 Ω	-15	V
		V_O = 8.5 V	R_O = 180 Ω		
		V_O = 10 V	R_O = 200 Ω		
		V_O = 12 V	R_O = 240 Ω		
I_O	Output Current			Internally Limited	
P_{tot}	Power Dissipation			Internally Limited	
T_j, T_{stg}	Junction and Storage Temperature			-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\text{-}j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\text{-}j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	°C/W

TEST CIRCUITS

Figure 1. - DC Parameters.



TEST CIRCUITS: (continued)

Figure 2. - Load Regulation

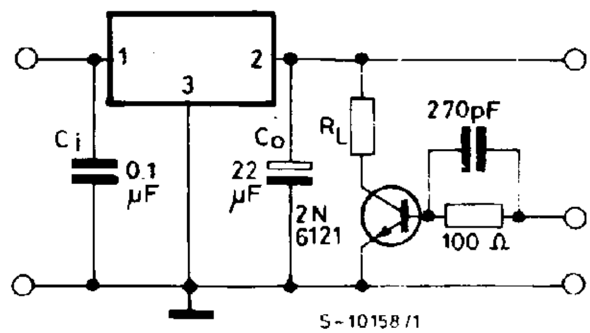
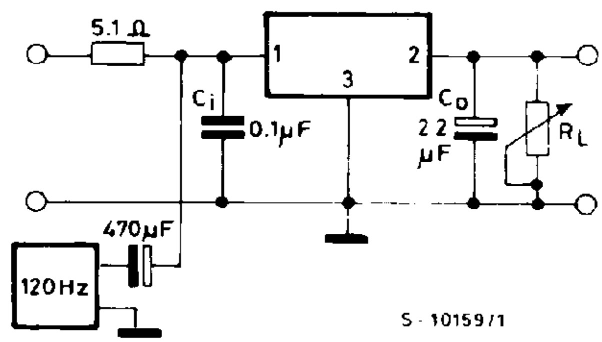


Figure 3. - Ripple Rejection



ELECTRICAL CHARACTERISTICS FOR L4940V5 (refer to the test circuits, T_j = 25 °C, V_i = 7V, C_i = 0.1 µF, C_o = 22 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mA	4.9	5	5.1	V
V_o	Output Voltage	I_o = 5 mA to 1500 mA V_i = 6.5 to 16 V	4.8	5	5.2	V
V_i	Operating Input Voltage	I_o = 5 mA			17	V
ΔV_o	Line Regulation	I_o = 5 mA V_i = 6 to 17 V		4	10	mV
ΔV_o	Load Regulation	I_o = 5 to 1500 mA I_o = 500 to 1000 mA		8 5	25 15	mV
I_Q	Quiscent Current	I_o = 5 mA I_o = 1.5 A V_i = 6.5 V		5 30	8 50	mA
ΔI_Q	Quiscent Current Change	I_o = 5 mA I_o = 1.5 A V_i = 6.5 to 16 V			3 15	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			0.5		mV/°C
SVR	Supply Voltage Rejection	I_o = 1 A f = 120 Hz	58	68		dB
V_d	Dropout Voltage	I_o = 0.5 A I_o = 1.5 A		200 500	400 900	mV
I_{sc}	Short Circuit Current	V_i = 14 V V_i = 6.5 V		2 2.2	2.7 2.9	A
Z_o	Output Impedance	f = 1 KHz I_o = 0.5A		30		mΩ
e_N	Output Noise Voltage	B = 100 Hz to 100 KHz		30		µV/V_o

ELECTRICAL CHARACTERISTICS FOR L4940V85 (refer to the test circuits, T_j = 25 °C, V_i = 10.5V, C_i = 0.1 µF, C_o = 22 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mA	8.3	8.5	8.7	V
V_o	Output Voltage	I_o = 5 mA to 1500 mA V_i = 10.2 to 16 V	8.15	8.5	8.85	V
V_i	Operating Input Voltage	I_o = 5 mA			17	V
ΔV_o	Line Regulation	I_o = 5 mA V_i = 9.5 to 17 V		4	9	mV
ΔV_o	Load Regulation	I_o = 5 to 1500 mA I_o = 500 to 1000 mA		12 8	30 16	mV
I_Q	Quiscent Current	I_o = 5 mA I_o = 1.5 A V_i = 10.2 V		4 30	8 50	mA
ΔI_Q	Quiscent Current Change	I_o = 5 mA I_o = 1.5 A V_i = 10.2 to 16 V			2.5 15	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			0.8		mV/°C
SVR	Supply Voltage Rejection	I_o = 1 A f = 120 Hz	58	66		dB
V_d	Dropout Voltage	I_o = 0.5 A I_o = 1.5 A		200 500	400 900	mV
I_{sc}	Short Circuit Current	V_i = 14 V V_i = 10.2 V		2 2.2	2.7 2.9	A
Z_o	Output Impedance	f = 1 KHz I_o = 0.5A		32		mΩ
e_N	Output Noise Voltage	B = 100 Hz to 100 KHz		30		µV/V_o

ELECTRICAL CHARACTERISTICS FOR L4940V10 (refer to the test circuits, T_j = 25 °C, V_i = 12V, C_i = 0.1 µF, C_o = 22 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mV	9.8	10	10.2	V
V_o	Output Voltage	I_o = 5 mA to 1500 mA V_i = 11.7 to 16 V	9.6	10	10.4	V
V_i	Operating Input Voltage	I_o = 5 mA			17	V
ΔV_o	Line Regulation	I_o = 5 mA V_i = 11 to 17 V		3	8	mV
ΔV_o	Load Regulation	I_o = 5 to 1500 mA I_o = 500 to 1000 mA		15 10	35 20	mV
I_Q	Quiscent Current	I_o = 5 mA I_o = 1.5 A V_i = 11.7 V		4 30	8 50	mA
ΔI_Q	Quiscent Current Change	I_o = 5 mA I_o = 1.5 A V_i = 11.7 to 16 V			2 13	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			1		mV/°C
SVR	Supply Voltage Rejection	I_o = 1 A f = 120 Hz	56	62		dB
V_d	Dropout Voltage	I_o = 0.5 A I_o = 1.5 A		200 500	400 900	mV
I_{sc}	Short Circuit Current	V_i = 14 V V_i = 11.7 V		2 2.2	2.7 2.9	A A
Z_o	Output Impedance	f = 1 KHz I_o = 0.5A		36		mΩ
e_N	Output Noise Voltage	B = 100 Hz to 100 KHz		30		µV/V_o

ELECTRICAL CHARACTERISTICS FOR L4940V12 (refer to the test circuits, T_j = 25 °C, V_i = 14V, C_i = 0.1 µF, C_o = 22 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 500 mV	11.75	12	12.25	V
V_o	Output Voltage	I_o = 5 mA to 1500 mA V_i = 13.8 to 17 V	11.5	12	12.5	V
V_i	Operating Input Voltage	I_o = 5 mA			17	V
ΔV_o	Line Regulation	I_o = 5 mA V_i = 13 to 17 V		3	7	mV
ΔV_o	Load Regulation	I_o = 5 to 1500 mA I_o = 500 to 1000 mA		15 10	35 25	mV
I_Q	Quiscent Current	I_o = 5 mA I_o = 1.5 A V_i = 13.8 V		4 30	8 50	mA
ΔI_Q	Quiscent Current Change	I_o = 5 mA I_o = 1.5 A V_i = 13.8 to 16 V			1.5 10	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			1.2		mV/°C
SVR	Supply Voltage Rejection	I_o = 1 A f = 120 Hz	55	61		dB
V_d	Dropout Voltage	I_o = 0.5 A I_o = 1.5 A		200 500	400 900	mV
I_{sc}	Short Circuit Current	V_i = 14 V		2	2.7	A
Z_o	Output Impedance	f = 1 KHz I_o = 0.5A		40		mΩ
e_N	Output Noise Voltage	B = 100 Hz to 100 KHz		30		µV/V_o

Figure 4. Dropout voltage vs. Output Current

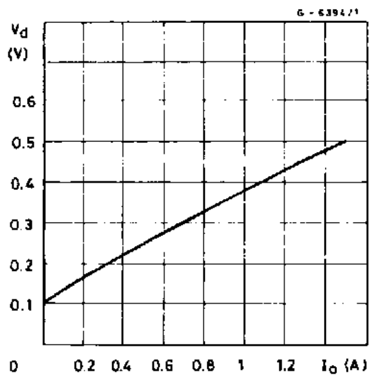


Figure 5. Dropout Voltage vs. Temperature

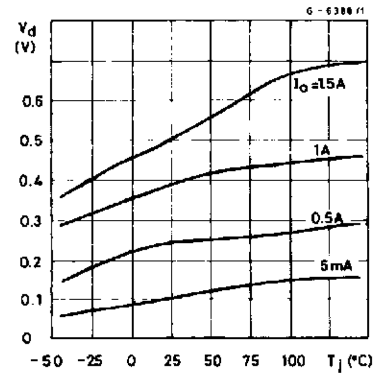


Figure 6. Output voltage vs. Temperature (L4940V5).

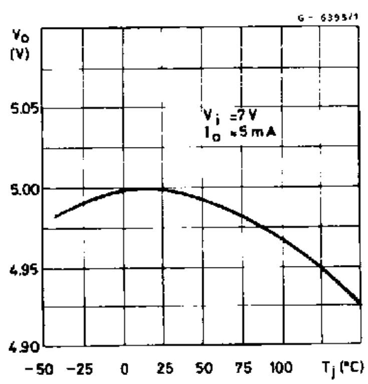


Figure 7. Output Voltage vs. Temperature (L4940V85).

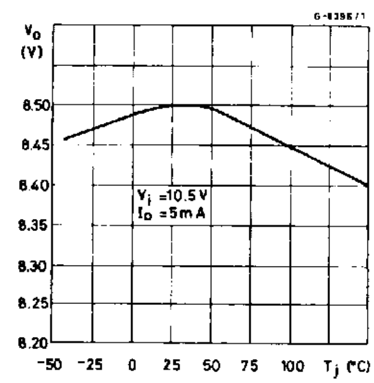


Figure 8. Output voltage vs. Temperature (L4040V10).

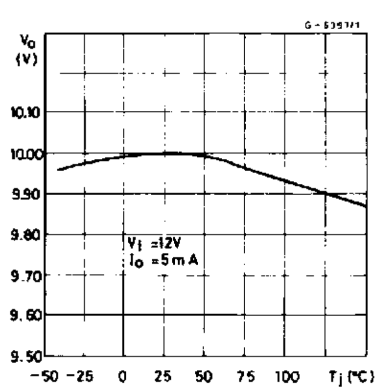


Figure 9. Output Voltage vs. Temperature (L4940V12).

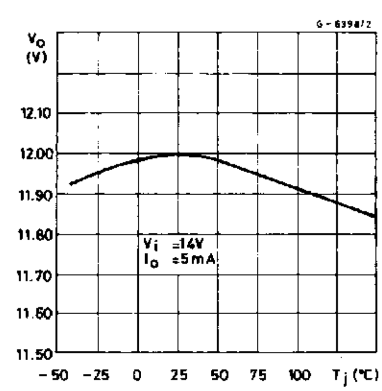


Figure 10. Quiescent Current vs. Temperature (L4940V5).

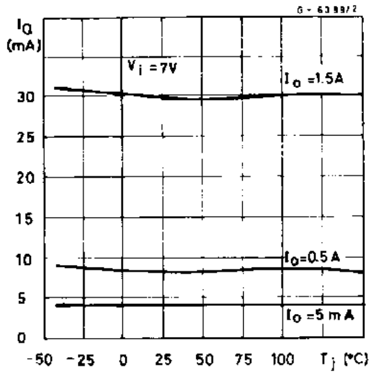


Figure 11. Quiescent Current vs. Input Voltage (L4940V5).

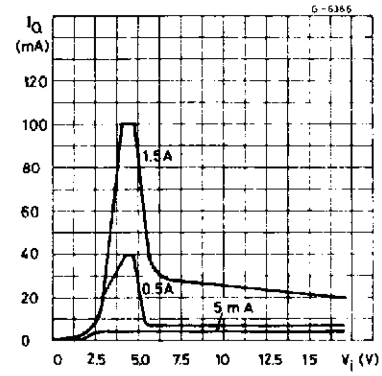


Figure 12. Quiescent Current vs. Output Current (L4940V5).

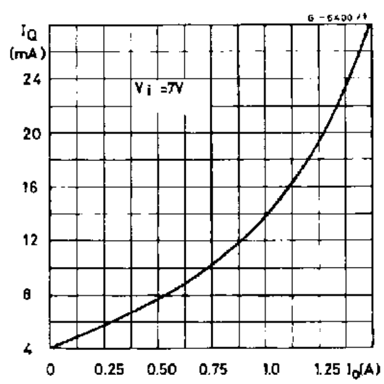


Figure 13. Short-circuit Current vs. Temperature (L4940V5).

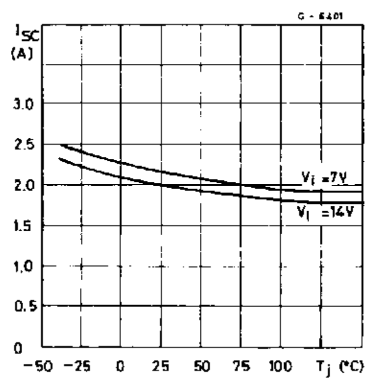


Figure 14. Peak Output Current vs. Input/Output Differential Voltage (L4940V5).

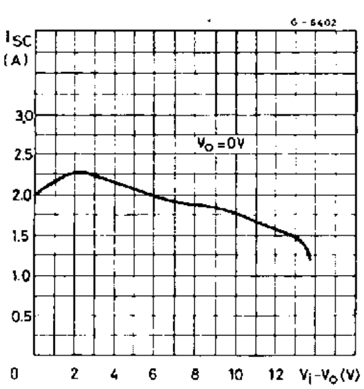


Figure 15. Low Voltage Behavior (L4940V5).

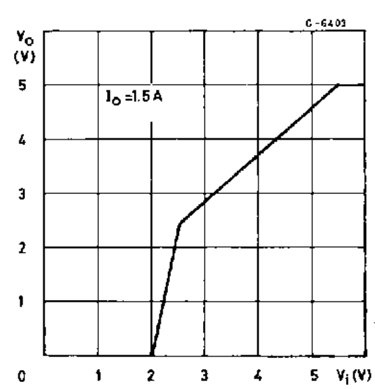


Figure 16. Low Voltage Behavior (L4940V85).

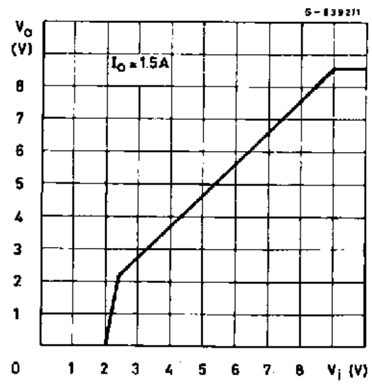


Figure 17. Low Voltage Behavior (L4940V10).

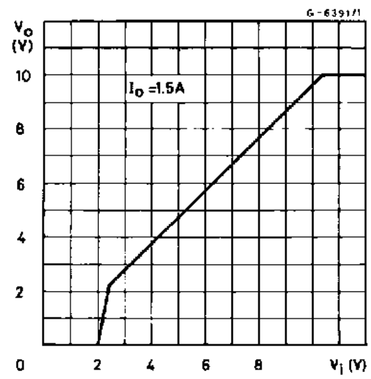


Figure 18. Low Voltage Behavior (L4940V12).

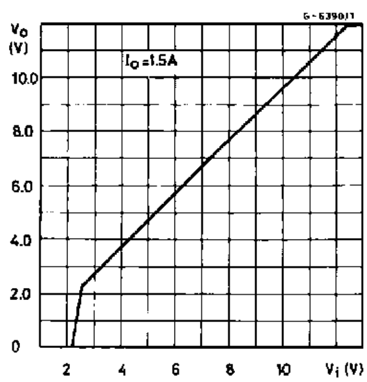


Figure 19. Supply Voltage Rejection vs. Frequency (L4940V5).

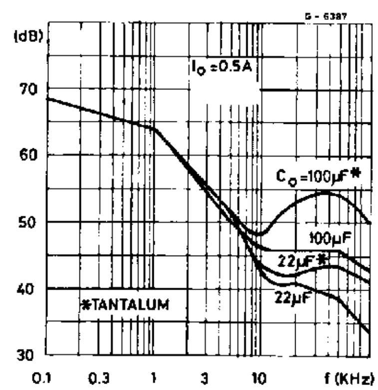


Figure 20. Supply Voltage Rejection vs. Output Current.

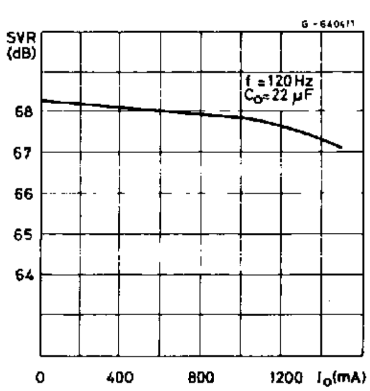
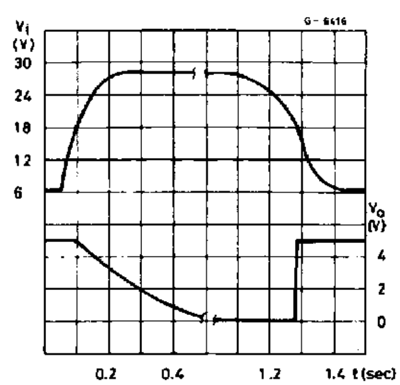


Figure 21. Load Dump Characteristics (L4940V5).



SGS-THOMSON MICROELECTRONICS

Figure 22. Line Transient Response (L4940V5).

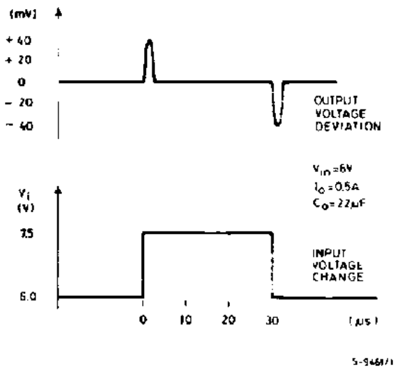


Figure 23. Load Transient Response.

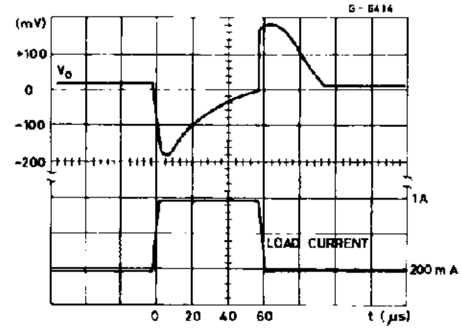


Figure 24. Total Power Dissipation.

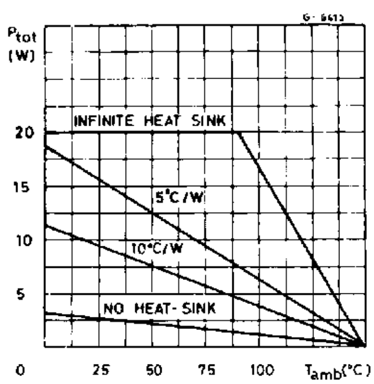


Figure 25. Distributed Supply with On-card L4940 and L4941 Low-drop Regulators.

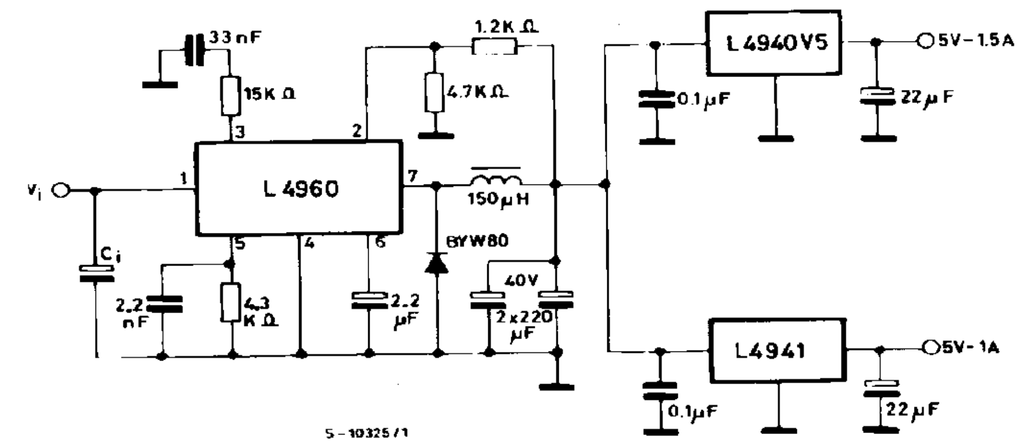
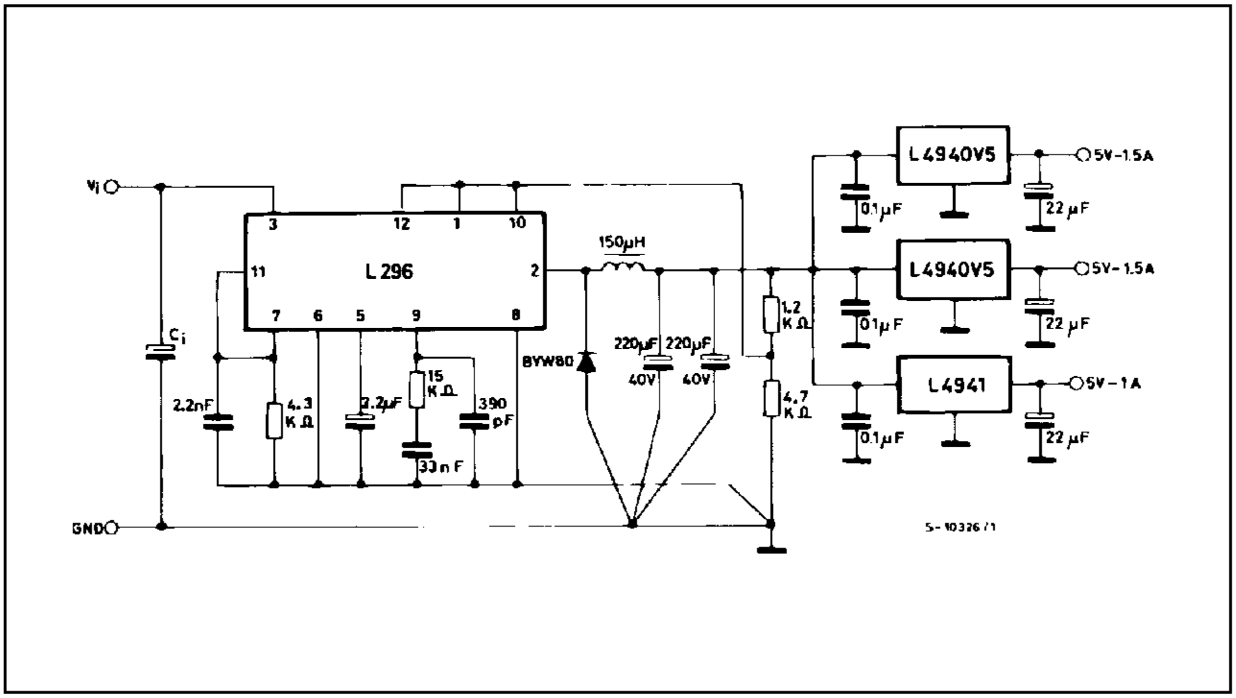


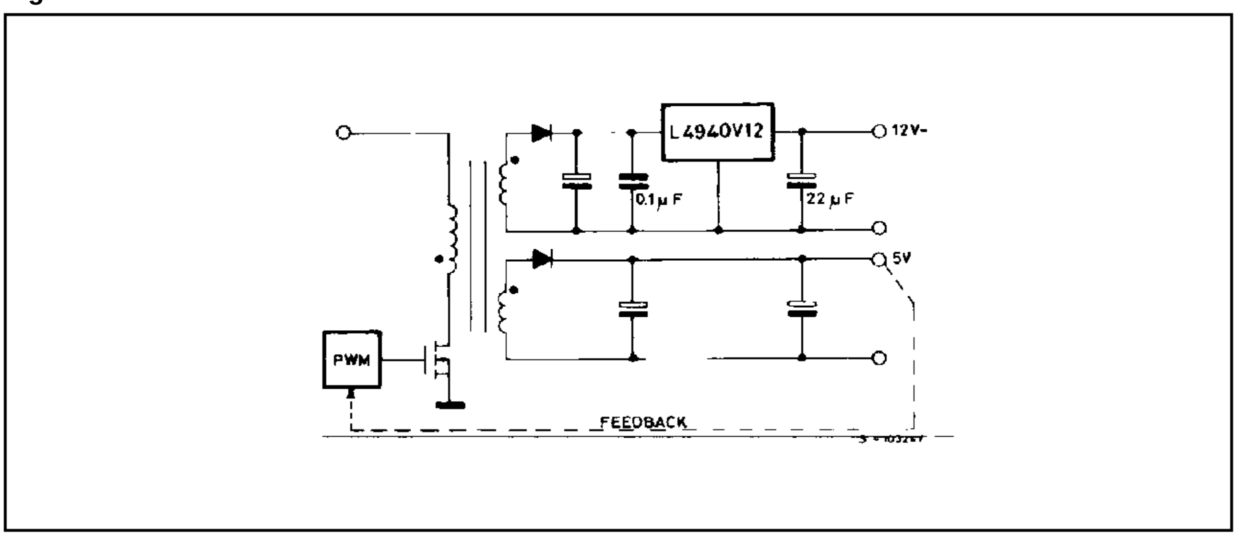
Figure 26. Distributed Supply with On-card L4940 and L4941 Low-drop Regulators.



ADVANTAGES OF THESE APPLICATIONS ARE :

- On card regulation with short-circuit and thermal protection on each output.
- Very high total system efficiency due to the switching preregulation and very low-drop postregulations.

Figure 27.

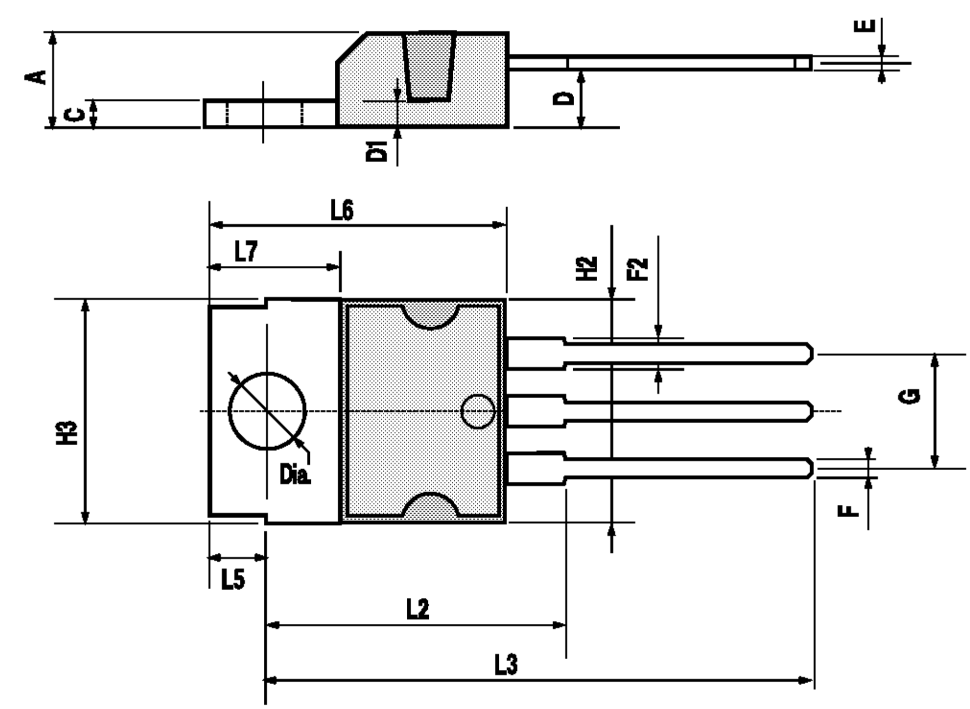


ADVANTAGES OF THIS CONFIGURATION ARE :

- Very high regulation (line and load) on both the output voltages.
- 12 V output short-circuit and thermally protected.
- Very high efficiency on the 12 V output due to the very low drop regulator.

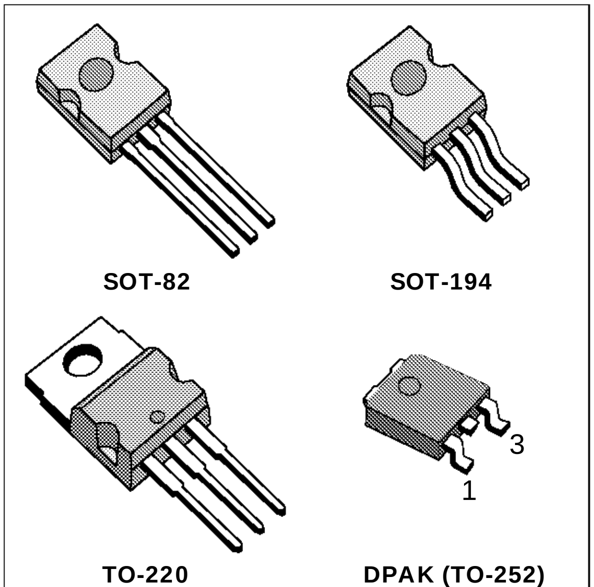
TO220 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152



VERY LOW DROP 1A REGULATOR

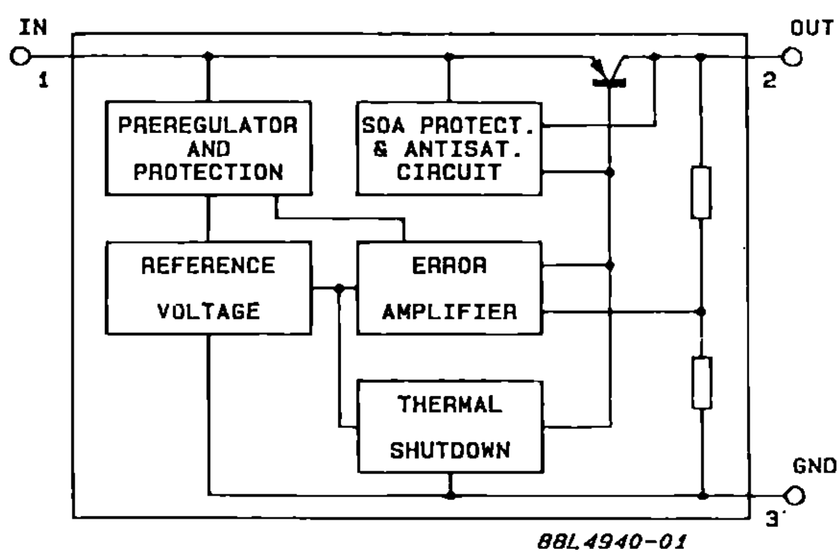
- LOW DROPOUT VOLTAGE (450 mV typ at 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION



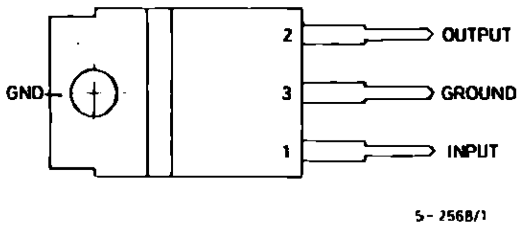
DESCRIPTION

The L4941 is a three terminal 5 V positive regulator available in TO-220, SOT-82, SOT-194 and DPAK packages, making it useful in a wide range of the industrial and consumer applications. Thanks to its very low input/output voltage drop, this device is particularly suitable for battery powered equipment, reducing consumption and prolonging battery life. It employs internal current limiting, antisaturation circuit, thermal shut-down and safe area protection.

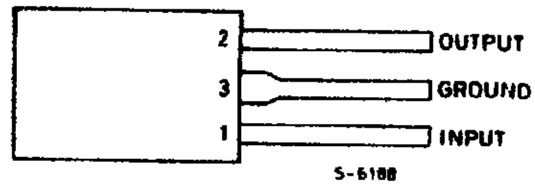
BLOCK DIAGRAM



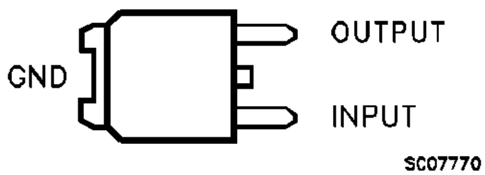
PIN CONNECTIONS AND ORDERING NUMBER (top view)



TO-220



SOT-82/SOT-194



DPAK

ORDERING NUMBERS	OUTPUT VOLTAGE	PACKAGE
L4941BV	5V	TO-220
L4941BX	5V	SOT-82
L4941BS	5V	SOT-194
L4941BDT	5V	DPAK

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Forward Input Voltage	30	V
V_{iR}	Reverse Input Voltage (R_O = 100 Ω)	– 15	V
I_O	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

THERMAL DATA

			SOT-82 SOT-194 DPAK	TO-220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	8	3	°C/W
$R_{thj\text{-}amb}$	Termal resistance Junction-ambient	Max	100	50	°C/W

TEST CIRCUITS

Figure 1 : DC Parameters.

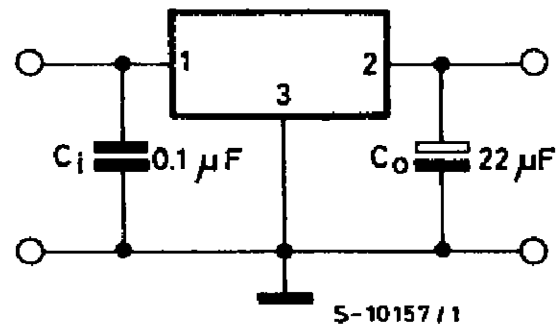


Figure 2 : Load Regulation.

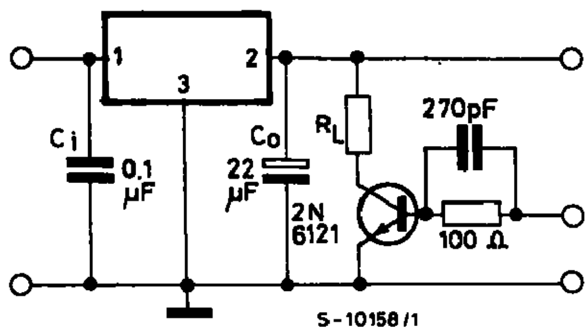
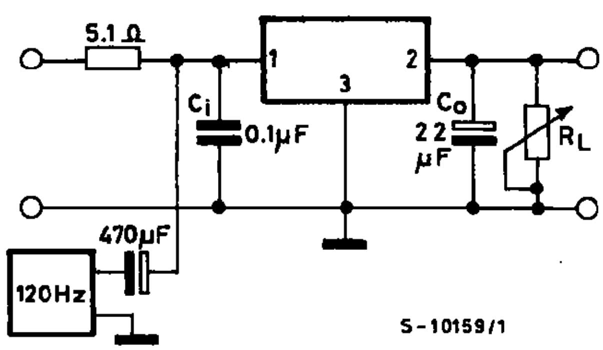


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, C_i = 0.1 µF, C_o = 22 µF, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Output Voltage				5			
Input Voltage (unless otherwise specified)				7			
V_o	Output Voltage	I_o = 5 mA to 1 A V_i = 6 V to 14 V		4.8	5	5.2	V
V_i	Operating Input Voltage	I_o = 5 mA				16	V
ΔV_o	Line Regulation	V_i = 6 V to 16 V I_o = 5 mA			5	20	mV
ΔV_o	Load Regulation	I_o = 5 mA to 1 A I_o = 0.5 A to 1 A			8 5	20 15	mV
I_Q	Quiescent Current	V_i = 6 V	I_o = 5 mA		4	8	mA
			I_o = 1 A		20	40	
ΔI_Q	Quiescent Current Change	V_i = 6 V to 14 V	I_o = 5 mA			3	mA
			I_o = 1 A			– 10	
V_d	Dropout Voltage	I_o = 0.5 A			250	450	mV
		I_o = 1 A			450	700	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift				0.6		mV/°C
SVR	Supply Voltage Rejection	f = 120 Hz I_o = 0.5 A		58	68		dB
I_{sc}	Short Circuit Current Limit	V_i = 14 V			1.6	2.0	A
		V_i = 6 V			1.8	2.2	
Z_o	Output Impedance	f = 1 kHz I_o = 0.5 A			30		mΩ
e_N	Output Noise Voltage	B = 100 Hz to 100 kHz			30		µV/V_o

Figure 4 : Dropout voltage vs. Output Current.

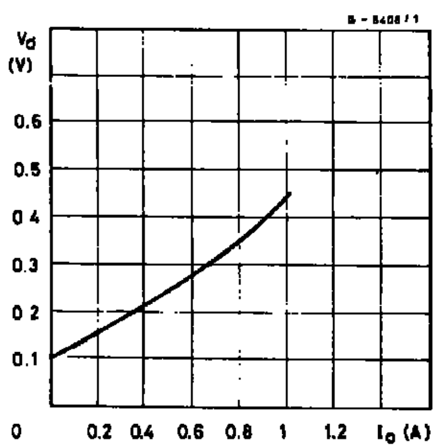


Figure 5 : Dropout Voltage vs. Temperature.

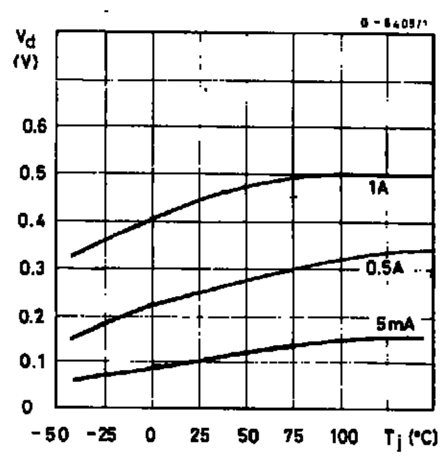


Figure 6 : Output voltage vs. Temperature.

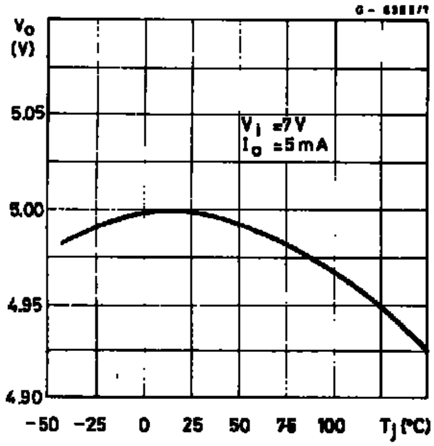


Figure 7 : Quiescent Current vs. Temperature

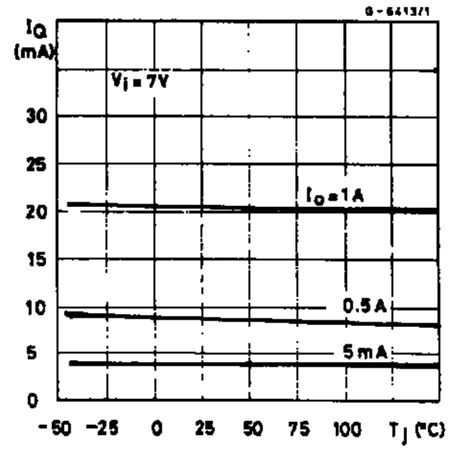


Figure 8 : Quiescent Current vs.Input Voltage.

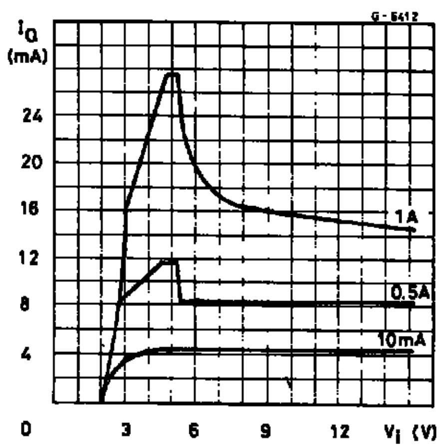


Figure 9 : Quiescent Current vs.Output Current.

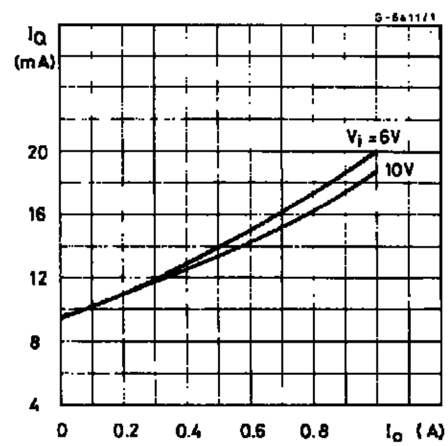


Figure 10 : Short-circuit Current vs. Temperature.

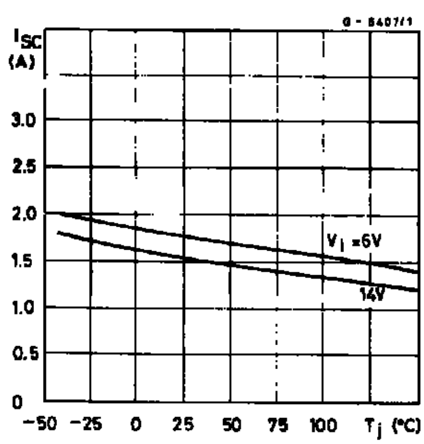


Figure 11 : Peak Output Current vs. Input/Output Differential Voltage.

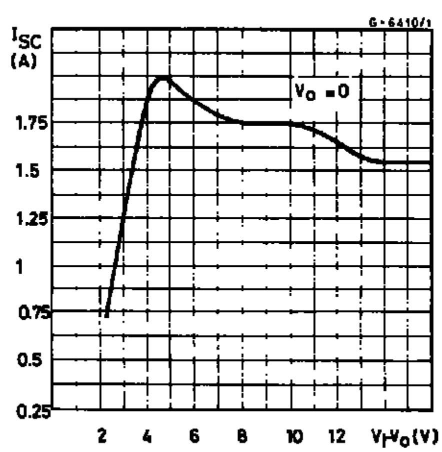


Figure 12 : Low Voltage Behavior.

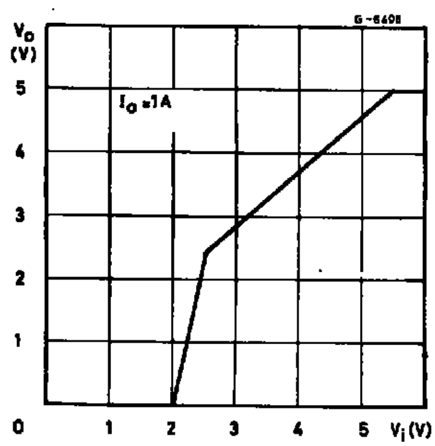


Figure 13 : Supply Voltage Rejection vs. Frequency

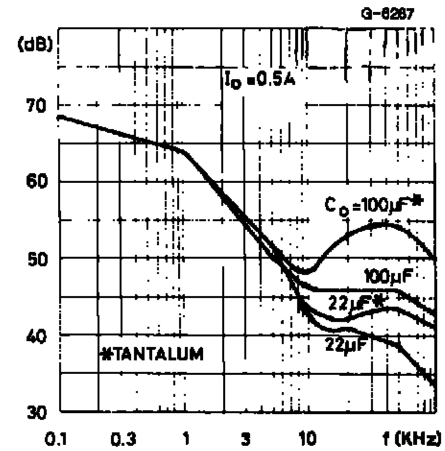


Figure 14 : Supply Voltage Rejection vs. Output Current.

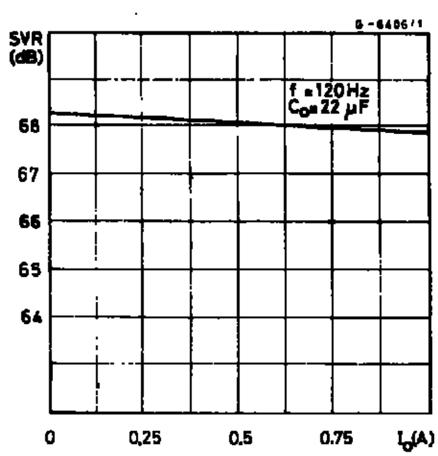


Figure 15 : Load Dump Characteristics.

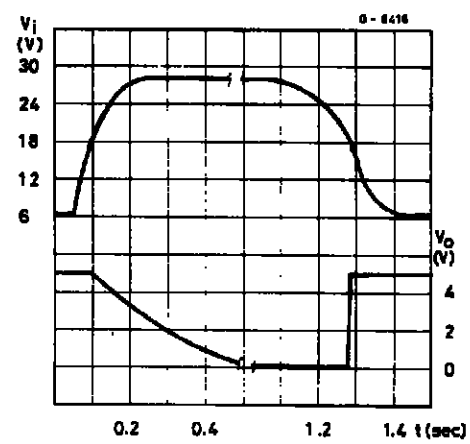


Figure 16 : Line Transient Response.

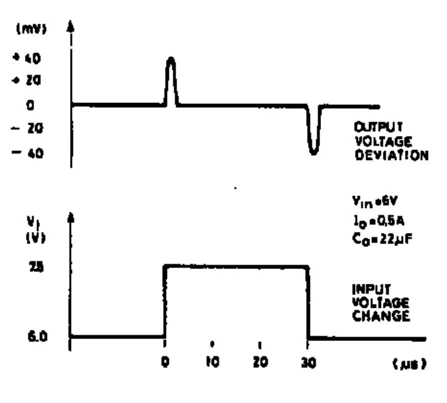


Figure 17 : Load Transunt Response.

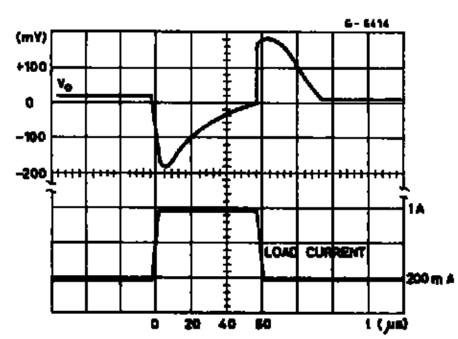


Figure 18 : Total Power Dissipation (TO-220).

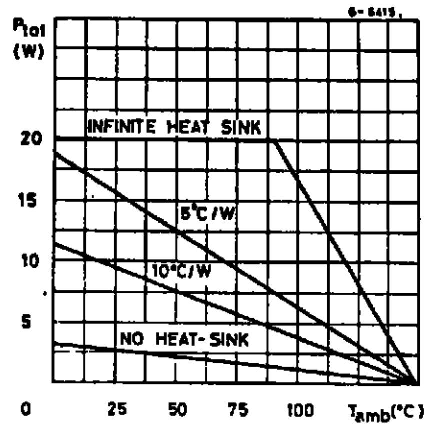
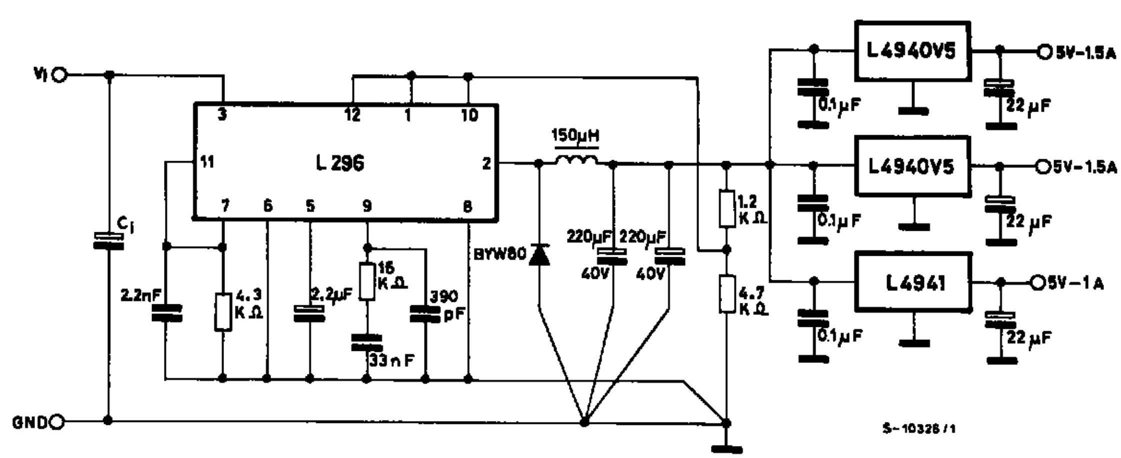


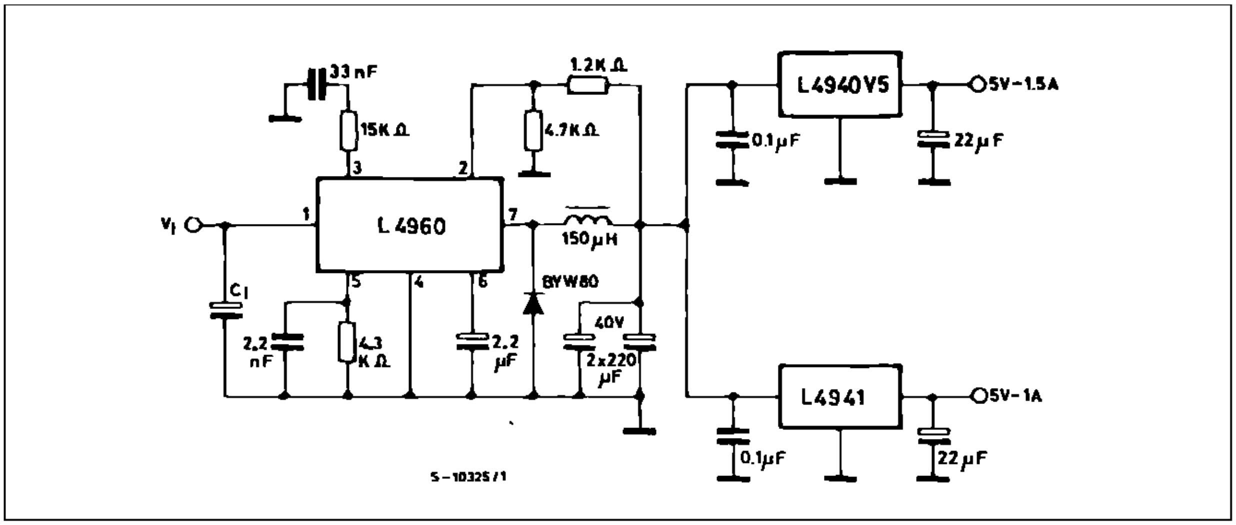
Figure 19 : Distribued Supply with On-card L4940 and L4941 Low-drop Regulators.



ADVANTAGES OF THESE APPLICATIONS ARE :

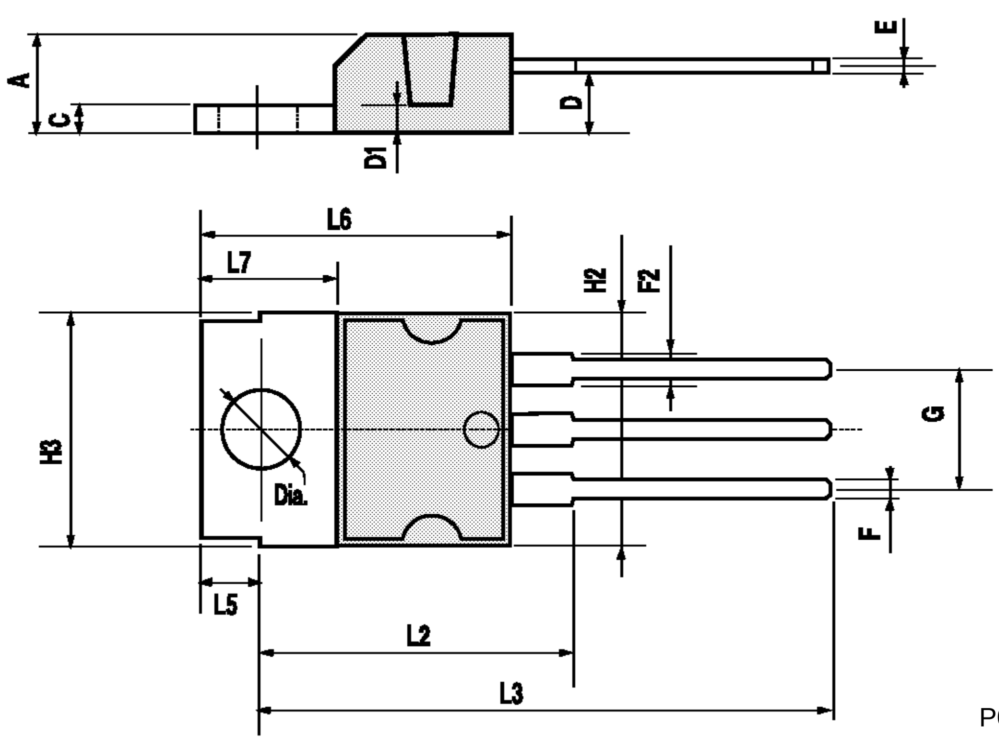
- On card regulation with short-circuit and thermal protection on each output.
- Very high total system efficiency due to the switching preregulation and very low-drop postregulations.

Figure 20 : Distribued Supply with On-card L4940 and L4941 Low-drop Regulators.



TO-220 MECHANICAL DATA

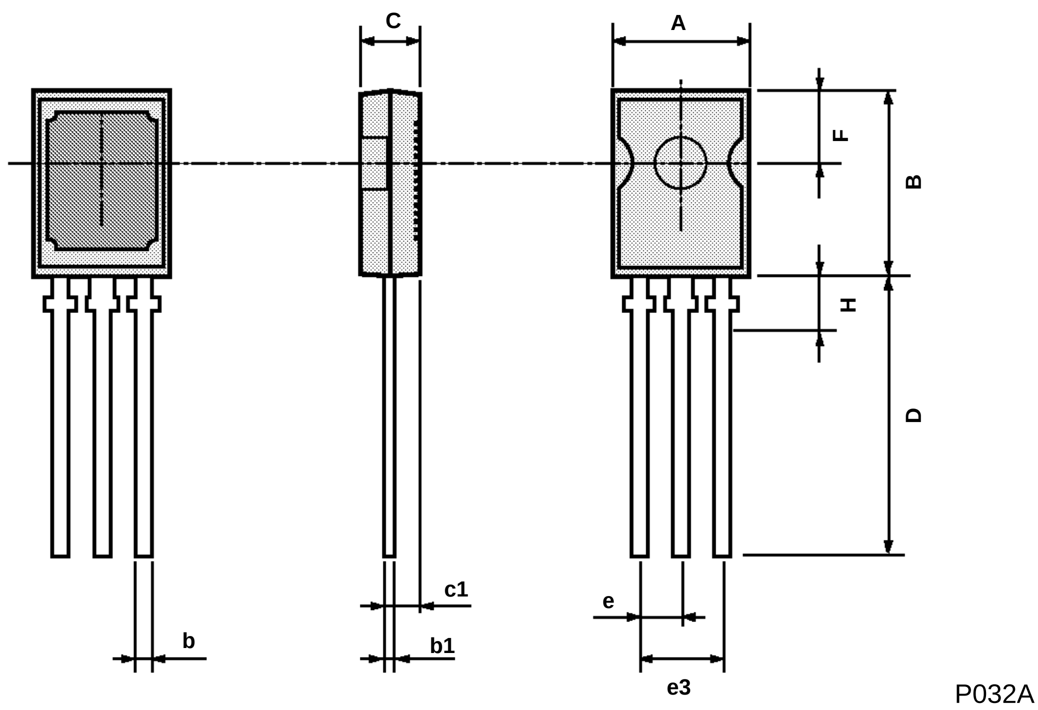
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia.	3.65		3.85	0.144		0.152



P011D

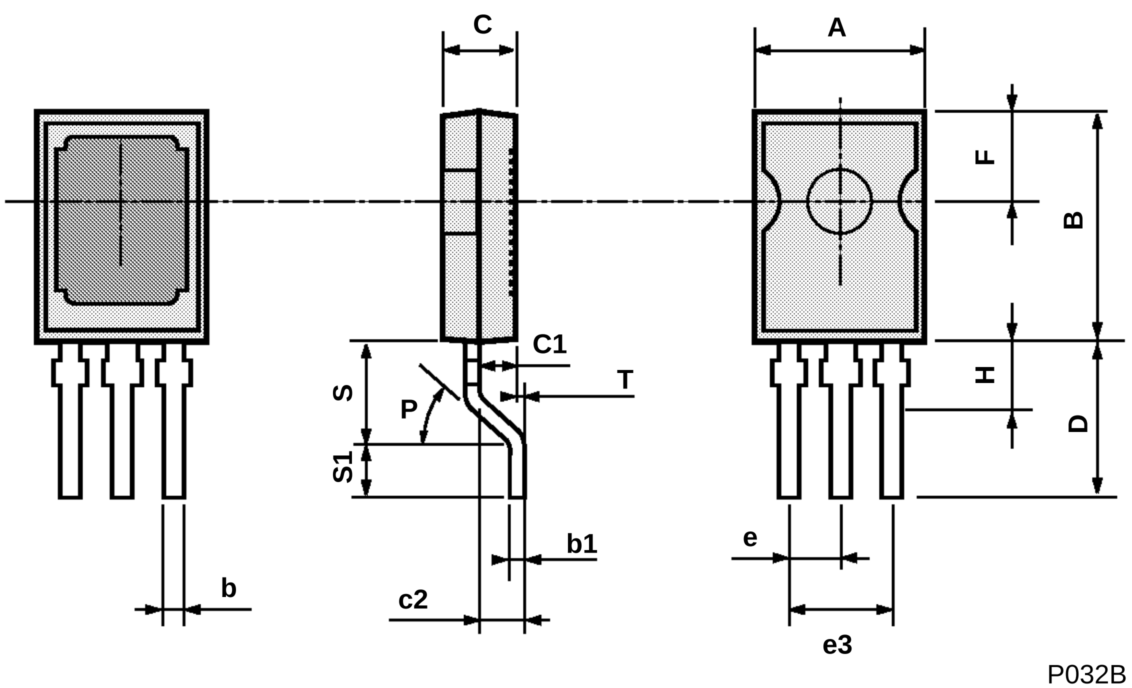
SOT-82 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		11.3	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.04		0.106
c1		1.2			0.047	
D		15.7			0.618	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54		0.100	



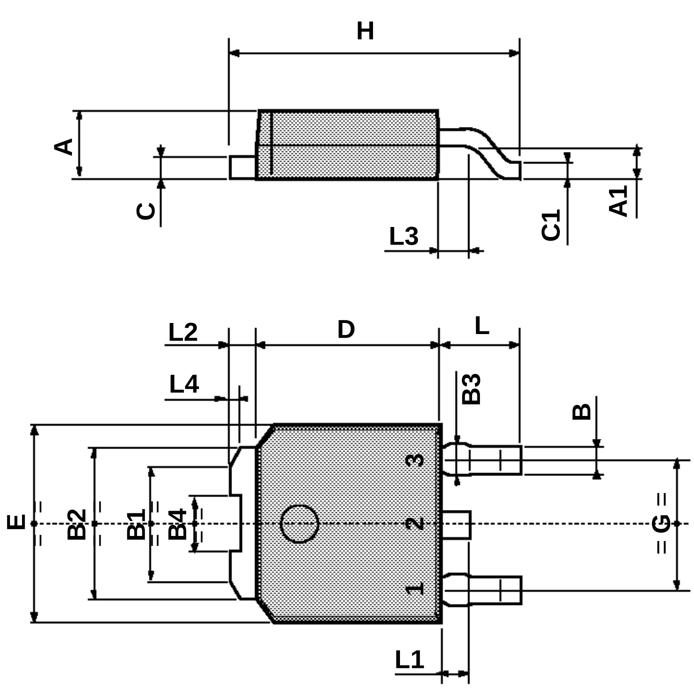
SOT-194 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		11.3	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
c2		1.3			0.051	
D		6			0.236	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54			0.100
P	45° (typ.)					
S		4			0.157	
S1		2			0.079	
T		0.1			0.004	



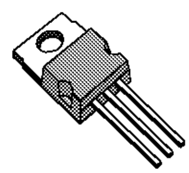
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
B	0.64		0.8	0.025		0.031
B1	3.4		3.6	0.133		0.141
B2	5.2		5.4	0.204		0.212
B3			0.9			0.035
B4	1.9		2.1	0.074		0.082
C	0.48		0.6	0.018		0.023
C1	0.45		0.6	0.017		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	2.55		3.05	0.100		0.120
L1	0.6		1	0.023		0.039
L2		0.8			0.031	
L3	0.8		1.2	0.031		0.047
L4	0.3		0.45	0.012		0.017



5V/8.5V/10V VERY LOW DROP VOLTAGE REGULATORS

- PRECISE OUTPUT VOLTAGE:
  5V ± 4% (L4945)
  8.5V ± 4% (L4950)
  10V ± 4% (L4951)
  OVER FULL TEMPERATURE RANGE
  (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL TEMPERATURE RANGE
- OUTPUT CURRENT UP TO 500mA
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTIONS
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



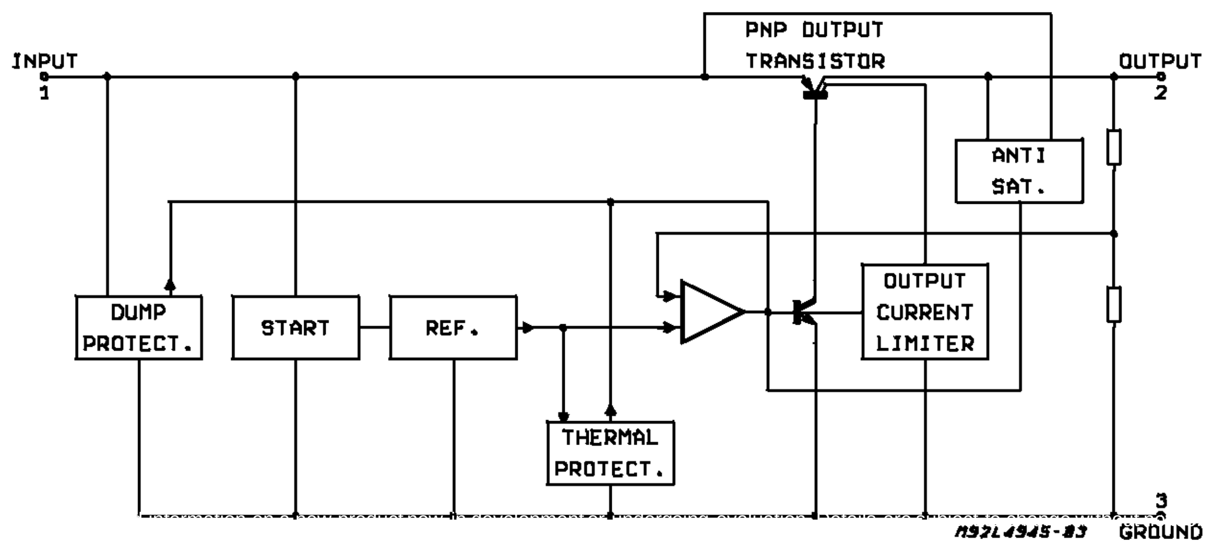
TO220

ORDERING NUMBER: L4945
L4950
L4951

DESCRIPTION

The devices are a monolithic integrated circuit in Versawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to their very low voltage drop, in automotive applications the devices can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, they incorporate a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car.

BLOCK DIAGRAM

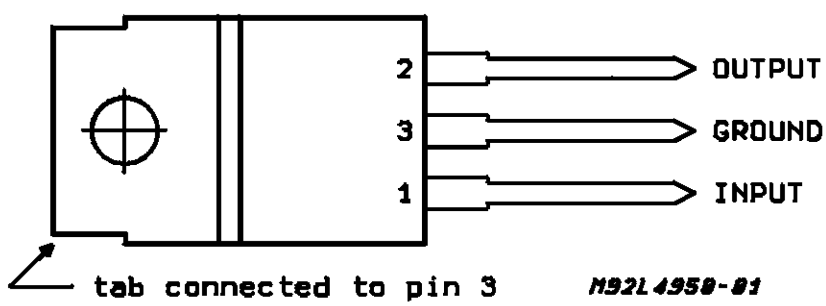


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage DC Reverse Input Voltage Transient Input Overvoltages : Load Dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant = 100ms R_{SOURCE} ≥ 0.5Ω Field Decay : 5ms ≤ t_{fall} ≤ 10ms, R_{SOURCE} ≥ 10Ω τ_r Rise Time Constant = 33ms Low Energy Spike : t_{rise} = 1µs, t_{fall} = 500µs, R_{SOURCE} ≥ 10Ω f_r Repetition Frequency = 5Hz	35 – 18 80 – 80 ± 100	V V V V V
T_J	Junction Temperature Range	– 40 to 150	°C
T_{OP}	Operating Temperature Range	– 40 to 125	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

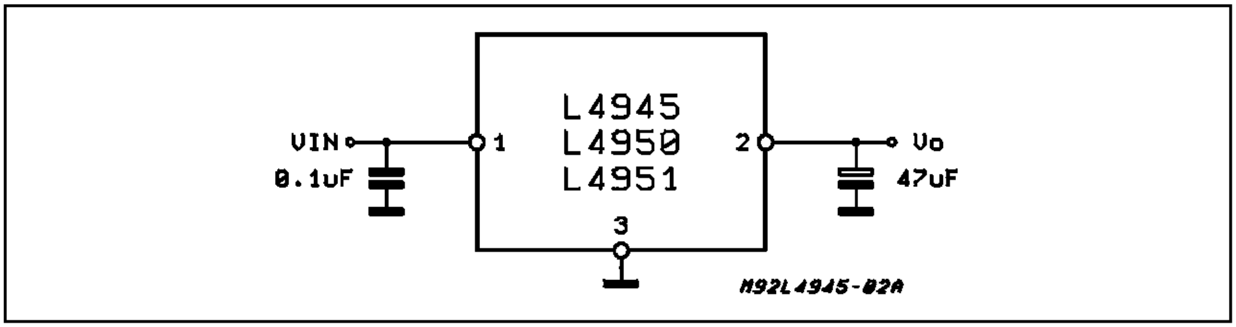
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case Max	3	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14. 4V, C_o = 47µF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, –40°C ≤ T_J ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 0mA to 500mA Over Full T Range for L4945 for L4950 for L4951	 4.80 8.16 9.60	 5.00 8.50 10	 5.20 8.84 10.4	 V V V
		T_j = 25°C for L4945 for L4950 for L4951	4.90 8.33 9.80	5.00 8.50 10	5.10 8.67 10.2	V V V
V_i	Operating Input Voltage	I_o = 0mA to (*) 500mA	6		26	V
ΔV_o	Line Regulation	V_i = 6V to 26V ; I_o = 5mA		2	10	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_i - V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C Over Full T Range		0.40	0.55 0.75	V V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C I_o = 0mA Over Full T I_o = 500mA Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_i = 12V ± 5V_{pp}	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A

(*) For a DC voltage 26 < V_i < 37V the device is not operating

FUNCTIONAL DESCRIPTION

The block diagram shows the basic structure of the devices : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

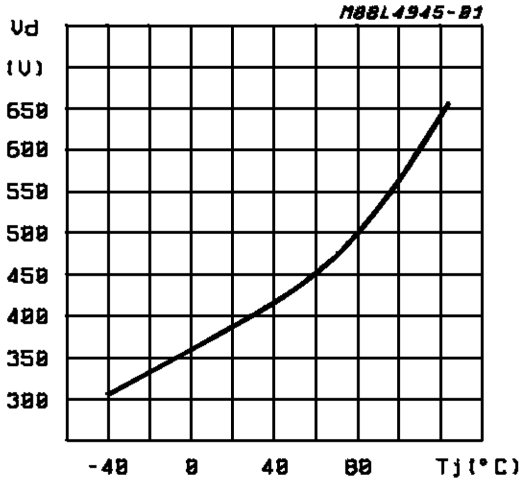
The current consumption of the devices (quiescent current) are maximum 10mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V, t = 300ms), reverse voltage (– 18V) and short circuit protection, thermal shutdown are the main features that make the devices specially suitable for applications in the automotive enviroment.

Figure 1: Typical Dropout Voltage vs. T_j (I_o = 500mA).



EXTERNAL COMPENSATION

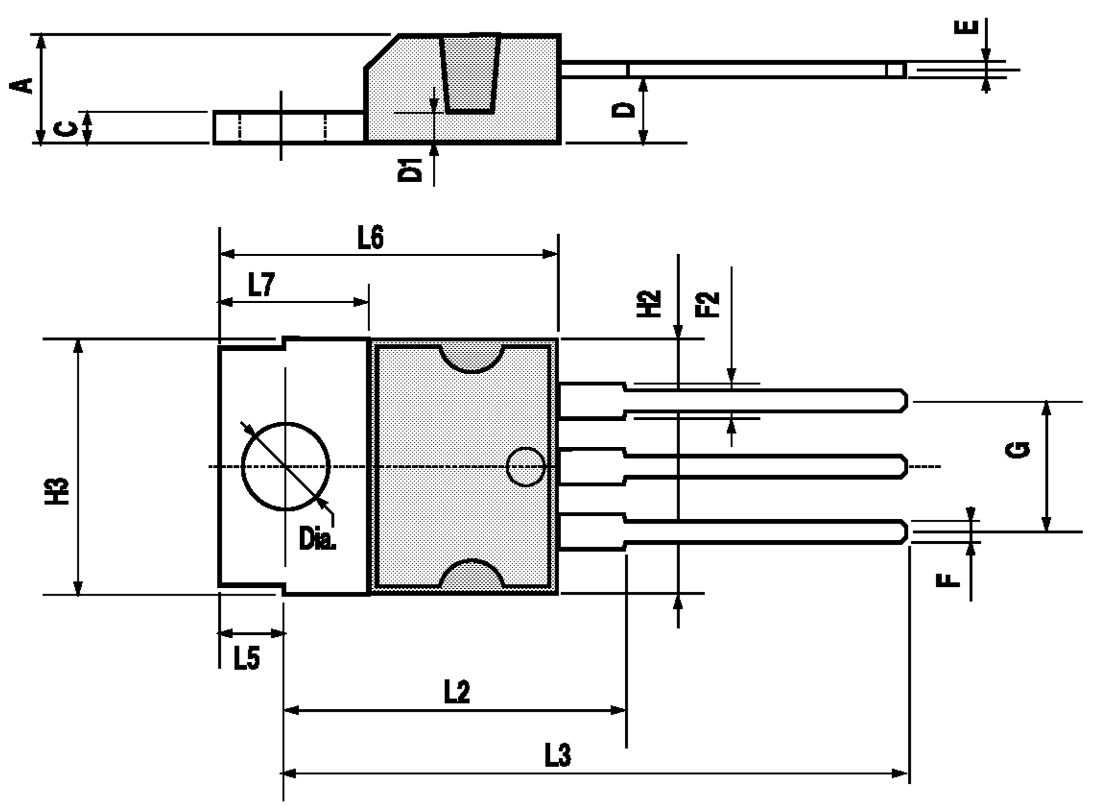
Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulators must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these others poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor esed to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequencybtoo low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The paeassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

TO220 (VERSAWATT) PACKAGE MECHANICAL DATA

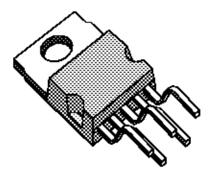
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152



L4947
L4947R

5V-0.5A VERY LOW DROP REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL TEMPERATURE RANGE (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL T RANGE
- OUTPUT CURRENT UP TO 500mA
- RESET FUNCTION
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- + 80V LOAD DUMP PROTECTION
- – 80V LOAD DUMP PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



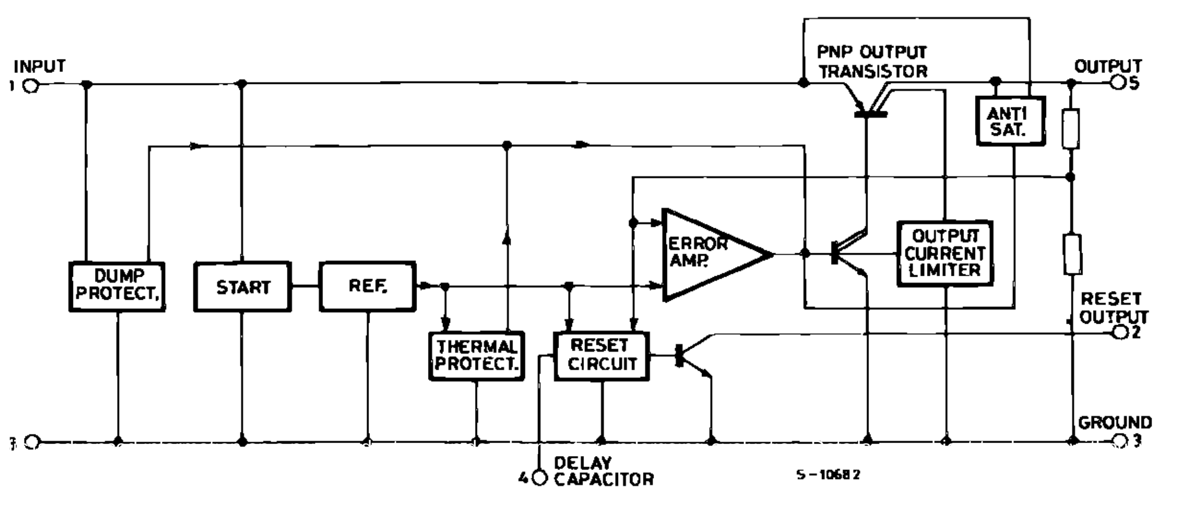
Pentawatt

ORDERING NUMBER: L4947
L4947R

DESCRIPTION

The L4947/L4947R is a monolithic integrated circuit in Pentawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L4947/L4947R can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems : a signal is available (after an externally programmable delay) to reset the microprocessor at power-on phase ; at power-off, this signal becomes low inhibiting the microprocessor.

BLOCK DIAGRAM

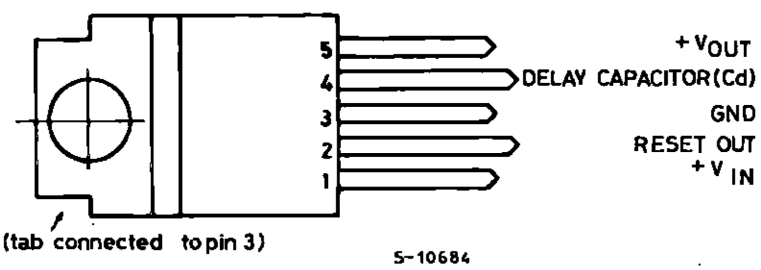


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage DC Reverse Input Voltage Transient Input Overvoltages : Load Dump : $5ms \le t_{rise} \le 10ms$ τ_f Fall Time Constant = 100ms $R_{SOURCE} \ge 0.5\Omega$ Field Decay : $5ms \le t_{fall} \le 10ms$, $R_{SOURCE} \ge 10\Omega$ τ_r Rise Time Constant = 33ms Low Energy Spike : $t_{rise} = 1\mu s$, $t_{fall} = 500\mu s$, $R_{SOURCE} \ge 10\Omega$ f_r Repetition Frequency = 5Hz	35 – 18 80 – 80 ± 100	V V V V V
V_R	Reset Output Voltage	35	V
T_J, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

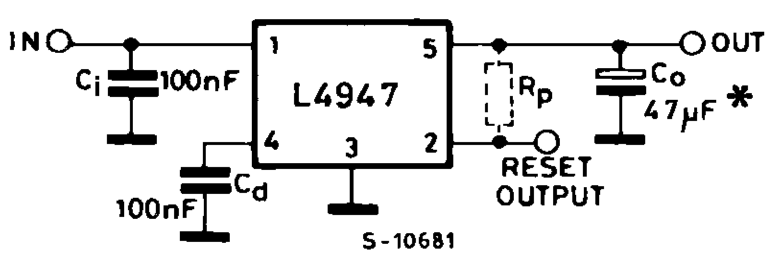
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W

TEST CIRCUIT



(*) Min. 20µF, ESR < 10Ω over full temperature range R_P (pull up resistor) and R_L (load) are both equal to 1KΩ.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14. 4V, C_o = 47µF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, –40°C ≤ T_J ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 0mA to 500mA Over Full T Range T_J = 25°C	4.80 4.90	5.00 5.00	5.20 5.10	V V
V_i	Operating Input Voltage	I_o = 0mA to (*) 500mA	6		26	V
ΔV_o	Line Regulation	V_i = 6V to 26V ; I_o = 5mA		2	10	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_i - V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C Over Full T Range		0.40	0.55 0.75	V V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C I_o = 0mA Over Full T I_o = 500mA Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100µF ; V_i = 12V ± $5V_{pp}$	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A
V_R	Reset Output Saturation Voltage	1.5V < V_o < $V_{RT (off)}$, I_R = 1.6mA 3.0V < V_o < $V_{RT (off)}$, I_R = 8mA			0.40 0.40	V V
I_R	Reset Output Leakage Current	V_O in Regulation, V_R = 5V			50	µA
$V_{RT peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_o, T_J = 25°C		0.50	0.80	V
$V_{RT (off)}$	Power OFF V_o Threshold	T_J = 25°C **L4947:** V_o @ Reset Out H to L Transition	4.70 4.75	Vo–0.15		V V
		L4947R: V_o @ Reset Out H to L Transition	4.55	Vo–0.30		V
$V_{RT (on)}$	Power ON V_o Threshold	V_o @ Reset Out L to H Transition		$V_{RT (off)}$ + 0.05	V_o – 0.04	V
V_{Hyst}	Power ON-Off Hysteresis	$V_{RT (on)} - V_{RT (off)}$		0.05		V
V_d	Delay Comparator Threshold	V_d @ Reset Out L to H Transition	3.65	4.00	4.35	V
		V_d @ Reset Out H to L Transition	3.20	3.55	3.90	V
V_{dH}	Delay Comparator Hysteresis			0.45		V
I_d	Delay Capacitor Charging Current	V_d = 3V, T_J = 25°C		20		/µA
V_{disch}	Delay Capacitor Discharge Voltage	V_o < $V_{RT (off)}$		0.55	1.20	V
T_d	Power on Reset Delay Time	C_d = 100nF, T_J = 25°C	10	20	30	ms

(*) For a DC voltage 26 < V_i < 37V the device is not operating

FUNCTIONAL DESCRIPTION

The L4947/L4947R is a very low drop 5V/0.5A voltage regulator provided with a reset function and therefore particularly suited to meet the requirements of supplying the microprocessor systems used in automotive and industrial applications.

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

The current consumption of the device (quiescent current) is maximum 13mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The reset function supervises the regulator output voltage inhibiting the microprocessor when the device is out of regulation and resetting it at the power-on after a settable delay. The reset is LOW when the output voltage value is lower than the reset threshold voltage. At the power-on phase the output voltage increases (see Fig. 2) and - when it reaches the power-on V_O threshold V_{RT} (On) - the reset output becomes HIGH after a delay time set by the external capacitor C_d. At the power-off the output voltage decreases : at the $V_{RT(Off)}$ threshold value (V_O-0.15V typ. for L4947 and V_O-0.3V typ. for L4947R value) the reset output instantaneously goes down (LOW status) inhibiting the microprocessor. The typical power on-off hysteresis is 50mV.

Figure 1: Typical Dropout Voltage vs. T_j (I_o = 500mA).

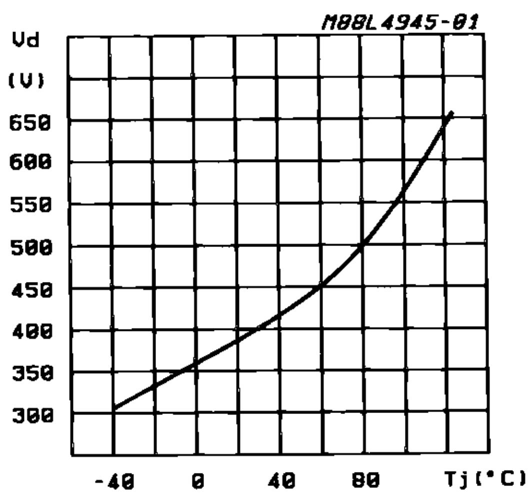
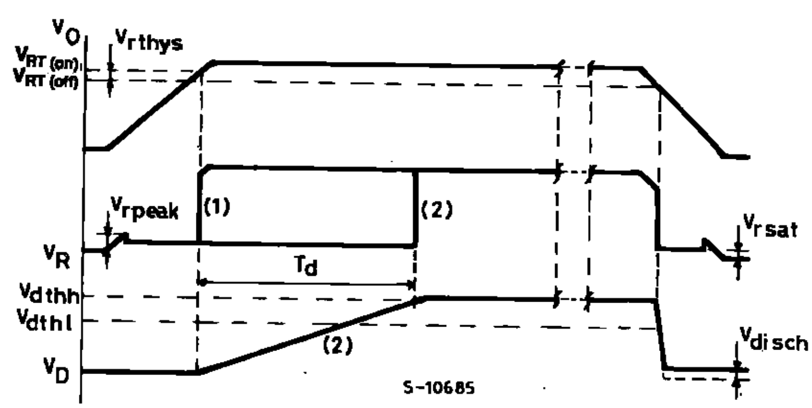


Figure 2: Reset Waveforms:
(1) Without External Capacitor C_d.
(2) With External Capacitor C_d.



The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V), reverse voltage (– 18V) and short circuit protection, thermal shutdown are the main features that make the L4947/L4947R specially suitable for applications in the automotive enviroment.

EXTERNAL COMPENSATION

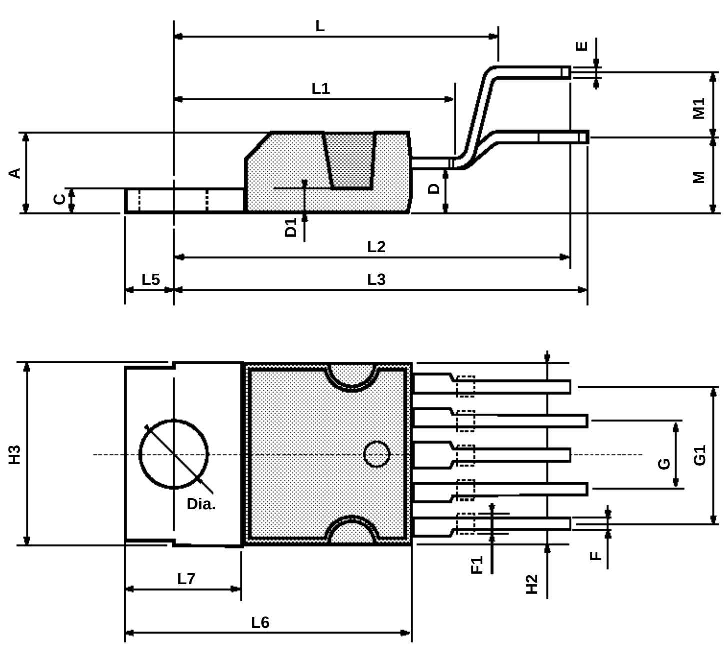
Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these others poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor esed to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequencybtoo low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The paeassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

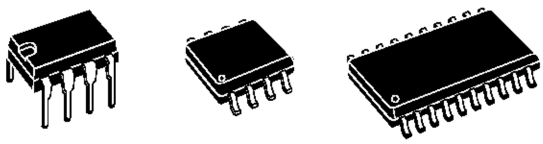


L4949E

MULTIFUNCTION VERY LOW DROP VOLTAGE REGULATOR

PRODUCT PREVIEW

- OPERATING DC SUPPLY VOLTAGE RANGE 5V - 28V
- TRANSIENT SUPPLY VOLTAGE UP TO 40V
- EXTREMELY LOW QUIESCENT CURRENT IN STANDBY MODE
- HIGH PRECISION STANDBY OUTPUT VOLTAGE 5V±1%
- OUTPUT CURRENT CAPABILITY UP TO 100mA
- VERY LOW DROPOUT VOLTAGE LESS THAN 0.5V
- RESET CIRCUIT SENSING THE OUTPUT VOLTAGE
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- VOLTAGE SENSE COMPARATOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



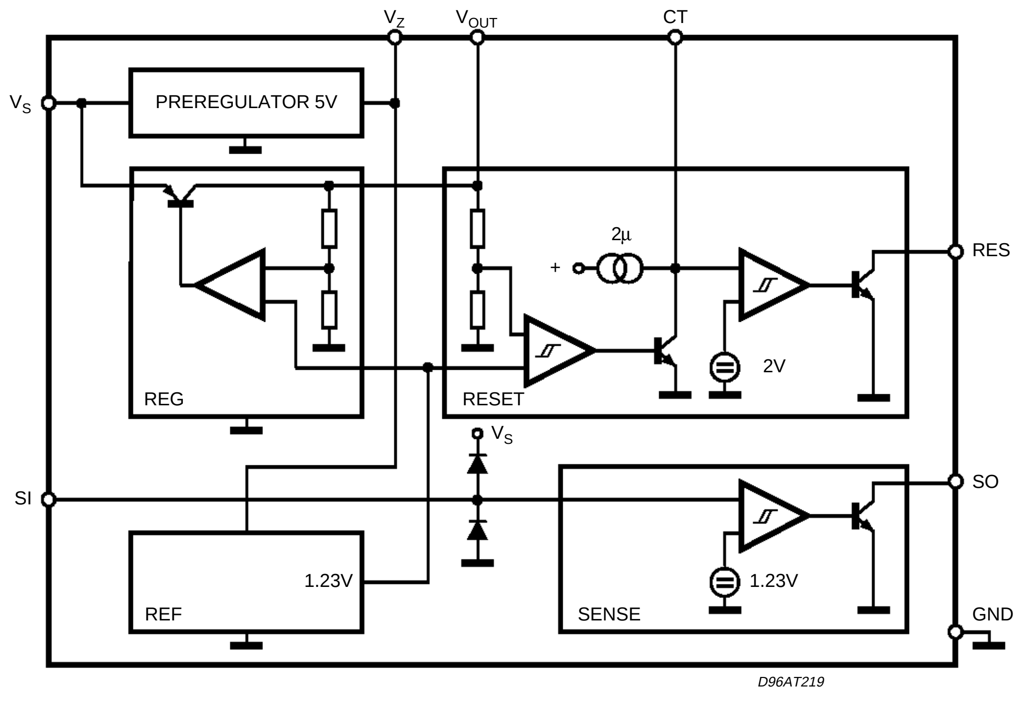
Minidip **SO8** **SO20L (12+4+4)**

ORDERING NUMBERS: L4949E (minidip)
L4949ED (SO8)
L4949EP (SO20L)

DESCRIPTION

The L4949E is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense. It is designed for supplying the microcomputer controlled systems especially in automotive applications.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

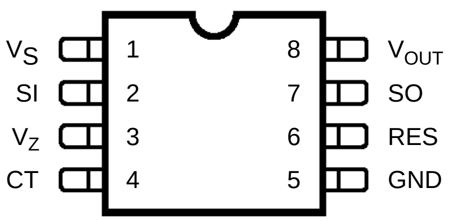
Symbol	Parameter	Value	Unit
V_{SDC}	DC Operating Supply Voltage	28	V
V_{STR}	Transient Supply Voltage (T < 1s)	40	V
I_O	Output Current	Internally Limited	
V_O	Output Voltage	20	V
I_{SI}	Sense Input Current	±1	mA
I_{EN}	Enable Input Current	-1	mA
V_{EN}	Enable Input Voltage	V_S	
V_{RES}, V_{SO}	Output Voltages	20	V
I_{RES}, I_{SO}	Output Currents	5	mA
V_Z	Preregulator Output Voltage	7	V
I_Z	Preregulator Output Current	5	mA
T_J	Junction Temperature	-40 to +150	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

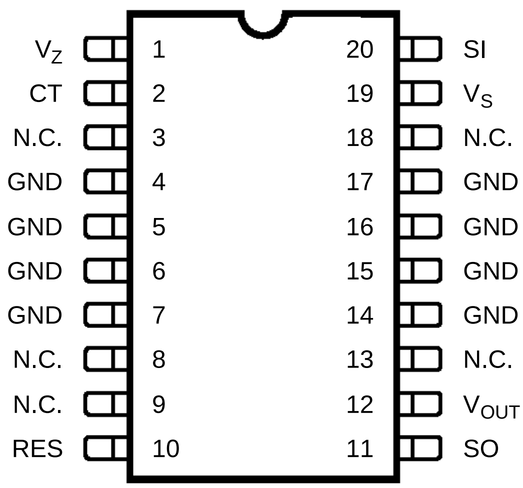
THERMAL DATA

Symbol	Description		Minidip	SO-8	SO20L	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	200	50	°C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-ambient	Max			15	°C/W
TJSD	Thermal Shutdown Junction temperature		165			°C

PIN CONNECTIONS



D95AT217



D95AT218

ELECTRICAL CHARACTERISTICS (V_S = 14V; -40°C < T_j < 125°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = 25°C; I_O = 1mA	4.95	5	5.05	V
V_O	Output Voltage	6V < V_{IN} < 28V, 1mA < I_O < 50mA	4.90	5	5.10	V
V_O	Output Voltage	V_{IN} = 40V; T < 1s 1mA < I_O < 50mA	4.85		5.20	V
V_{DP}	Dropout Voltage	I_O = 10mA I_O = 50mA I_O = 100mA		0.1 0.2 0.3	0.25 0.4 0.5	V V V
V_{IO}	Input to Output Voltage Difference in Undervoltage Condition	V_{IN} = 4V, I_O = 35mA			0.4	V
I_{outh} **	Max Output Leakage	V_{IN} = 25V, V_O = 5.5V	20	50	80	µA
V_{OL}	Line Regulation	6V < V_{IN} < 28V; I_O = 1mA			20	mV
V_{OLO}	Load Regulation	1mA < I_O < 100mA			30	mV
I_{LIM}	Current Limit	V_O = 4.5V V_O = 0V (note 1)	105	200 100	400	mA mA
I_{QSE}	Quiescent Current	I_O = 0.3mA; T_J < 100°C		200	300	µA
I_Q	Quiescent Current	I_O = 100mA			5	mA

** With this test we guarantee that with no output current the output voltage will not exceed 5.5V

RESET

V_{RT}	Reset Thereshold Voltage			V_O -0.5V		V
V_{RTH}	Reset Thereshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF; T_R ≥100µs	55	100	180	ms
t_{RR}	Reset Reaction Time	C_T = 100nF		5	30	µs
V_{RL}	Reset Output Low Voltage	R_{RES} = 10KΩ to V_O V_S ≥ 1.5V			0.4	V
I_{RH}	Reset Output High Leakage Current	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Thereshold			2		V
$V_{CTth, hy}$	Delay Comparator Thereshold Hysteresis			100		mV

SENSE

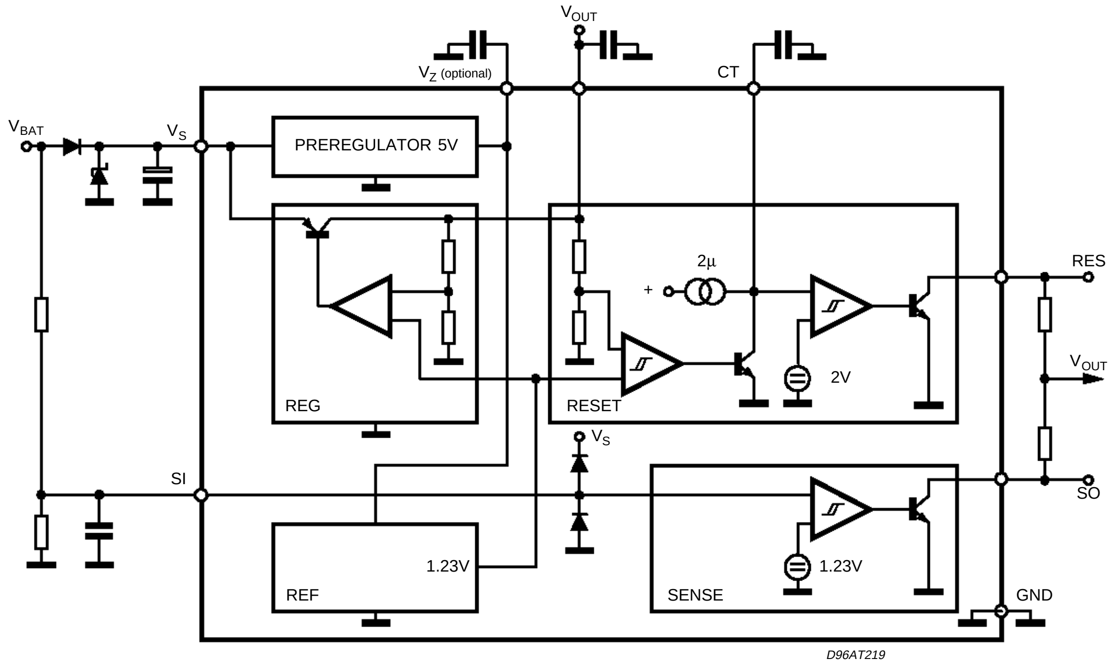
V_{st}	Sense Low Thereshold		1.16	1.23	1.35	V
V_{sth}	Sense Thereshold Hysteresis		20	100	200	mV
V_{SL}	Sense Output Low Voltage	V_{SI} ≤ 1.16V; V_S ≥ 3V R_{SO} = 10KΩ to V_O			0.4	V
I_{SH}	Sense Output Leakage	V_{SO} = 5V; V_{SI} ≥ 1.5V			1	µA
I_{SI}	Sense Input Current	V_{SI} = 0	-20	-8	-3	µA

PREREGULATOR

V_Z	Preregulator Output Voltage	I_Z = 10µA	4.5	5	6	V
I_Z	Preregulator Output Current				10	µA

Note 1: Foldback characteristic

APPLICATION CIRCUIT



For stability: $C_S \geq 1\mu F$, $C_O \geq 4.7\mu F$, ESR < 10Ω at 10KHz
Recommended for application: $C_S = C_O = 10\mu F$ to $100\mu F$

APPLICATION INFORMATION

Supply Voltage Transient

High supply voltage transients can cause a reset output signal disturbation.

For supply voltages greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than 100V/µs.
For supply voltages less than 8V supply transients of more than 0.4V/µs can cause a reset signal disturbation.

To improve the transient behaviour for supply voltages less than 8V a capacitor at pin 3 can be used.

A capacitor at pin 3 ($C3 \leq 1\mu F$) reduces also the output noise.

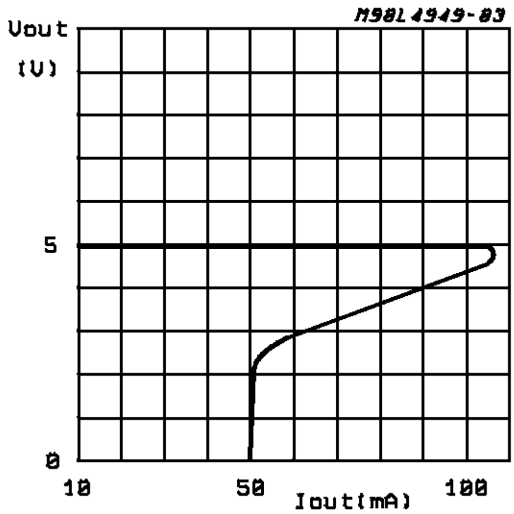
FUNCTIONAL DESCRIPTION

The L4949E is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approch. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

Voltage Regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element.

Figure 1: Foldback Characteristic of V_O



With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. With this feature no functional interruption due to overvoltage pulses is generated. The typical curve showing the standby output voltage as a function of the input supply voltage is shown in Fig. 2. The current consumption of the device (quiescent current) is less than 300µA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in Fig. 3.

Figure 2: Output Voltage vs. Input Voltage

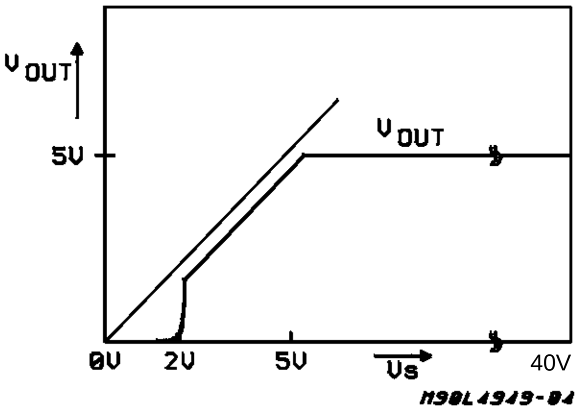
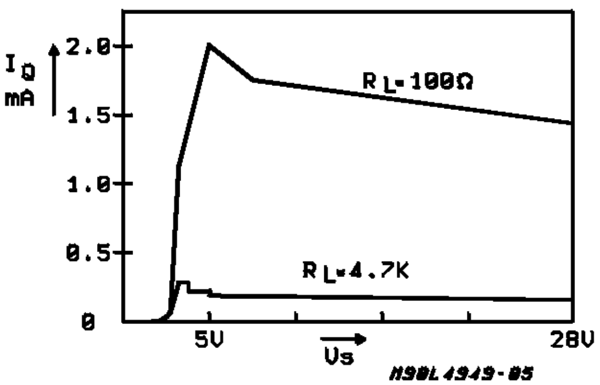


Figure 3: Quiescent Current vs. Supply Voltage



Preregulator

To improve the transient immunity a preregulator stabilized the internal supply voltage to 5V. This internal voltage is present at Pin 3 (V_Z). This voltage should not be used as an output because the output capability is very small (≤10µA).

This output may be used as an option when a better transient behaviour for supply voltages less than 8V is required (see also application note).

In this case a capacitor (100nF - 1µF) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.

Reset Circuit

The block circuit diagram of the reset circuit is shown in Fig. 4. The reset circuit supervises the output voltage.

The reset thereshold of 4.5V is defined with the internal reference voltage and standby output drivider.

The reset pulse delay time t_{RD}, is defined with the charge time of an external capacitor C_T:

$$t_{RD} = \frac{C_T \bullet 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50µs.

The typical reset output waveforms are shown in Fig. 5.

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after the protection diode and to give additional informations to the microprocessor like low voltage warnings.

Figure 4

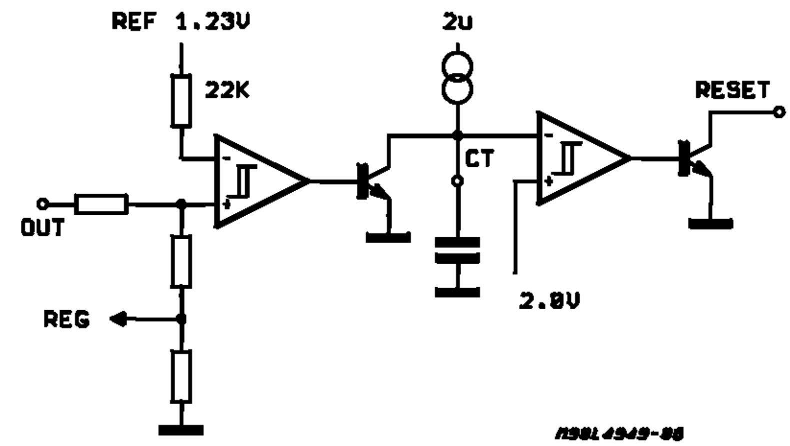
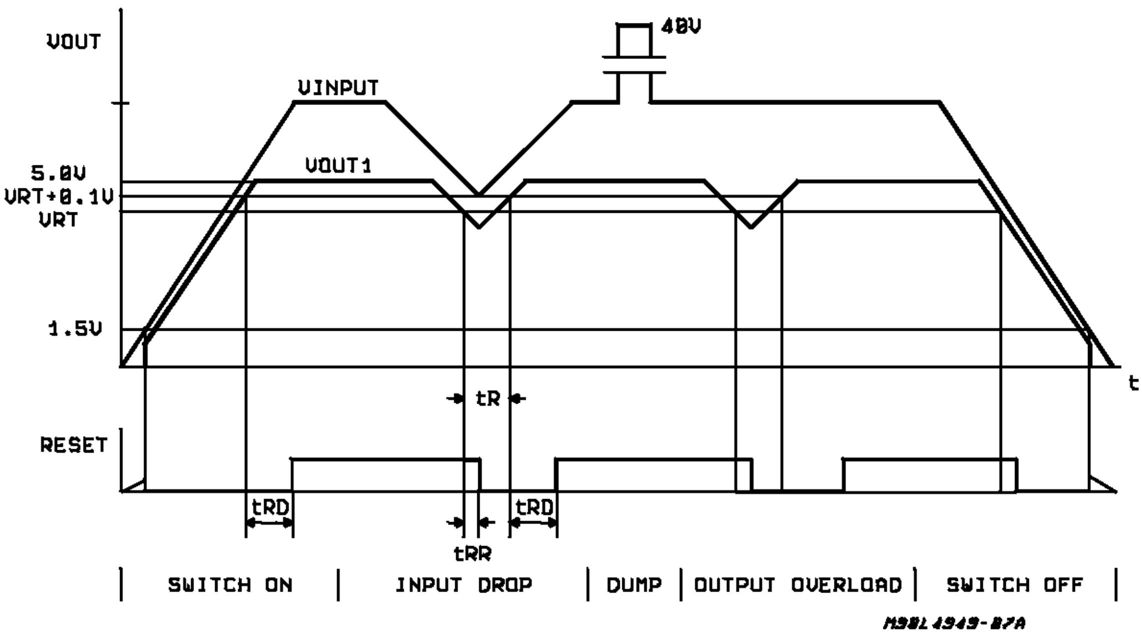
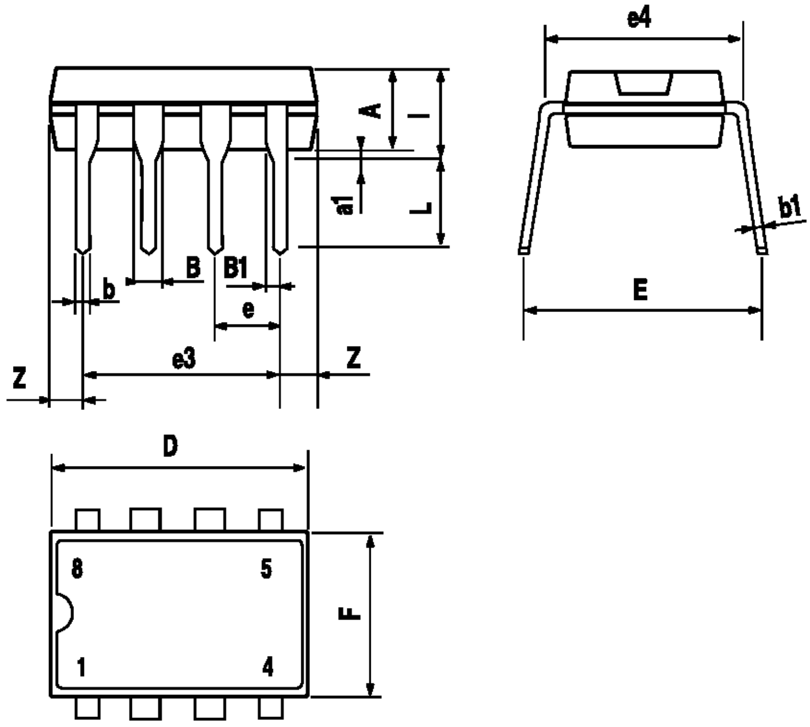


Figure 5



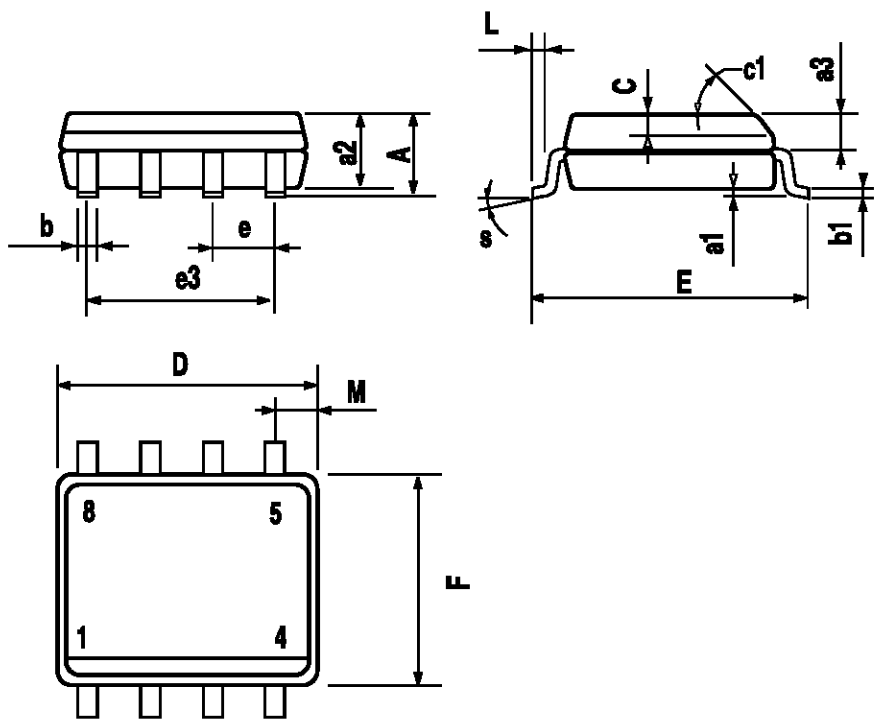
MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



SO8 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1		45			1.772	
D		1	4.8		0.039	0.189
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F		1	3.8		0.039	0.150
G						
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S			8			0.315



SO20L PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1		45			1.772	
D		1	12.6		0.039	0.496
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F		1	7.4		0.039	0.291
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S			8			0.315