Fast ±150mA Power Buffer

FEATURES

- 20MHz Bandwidth
- 75V/μs Slew Rate
- Drives ±10V into 75Ω
- 5mA Quiescent Current
- Drives Capacitive Loads >1μF
- Current and Thermal Limit
- Operates from Single Supply ≥4.5V
- Very Low Distortion Operation

APPLICATIONS

- Boost Op Amp Output
- Isolate Capacitive Loads
- Drive Long Cables
- Audio Amplifiers
- Video Amplifiers
- Power Small Motors
- Operational Power Supply
- FET Driver

DESCRIPTION

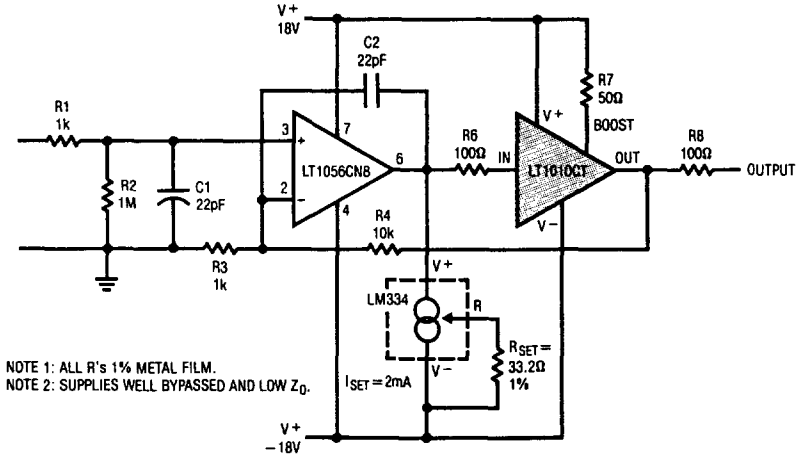
The LT1010 is a fast, unity-gain buffer that can increase the output capability of existing IC op amps by more than an order of magnitude. This easy-to-use part makes fast amplifiers less sensitive to capacitive loading, reduces thermal feedback in precision dc amplifiers and is recommended for a wide range of fast and slow applications.

Designed to be incorporated within the feedback loop, the buffer can isolate almost any reactive load. Internal operating currents are essentially unaffected by supply or output voltage, accounting for the 4.5V to 40V supply voltage range with unchanged specifications. Single-supply operation is also practical.

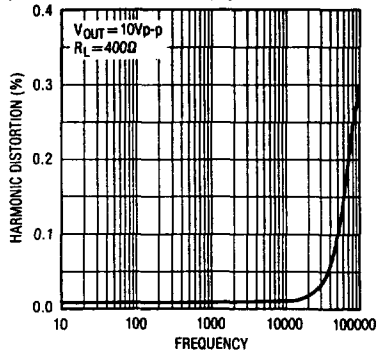
This monolithic IC is supplied in an 8-pin miniDIP and three standard power packages: the solid kovar base TO-5 (TO-39), the steel TO-3 and the plastic TO-220. The low thermal resistance power packages are an aid in reducing operating junction temperatures. With the TO-3, TO-220, and miniDIP packages, an option is available to raise quiescent current and improve speed. The miniDIP version is supplied for those applications not requiring high power dissipation or where board space is a premium.

In the TO-39 package, the LT1010 can sometimes replace the hybrid LH0002. With the exception of speed it exceeds key specifications and fault protection is vastly superior. Further, the lower thermal resistance package and higher maximum operating temperature of the new monolithic circuit allow more usable output.

Very Low Distortion Buffered Pre-Amplifier



NOTE 1: ALL R's 1% METAL FILM.
NOTE 2: SUPPLIES WELL BYPASSED AND LOW Z_O.



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ..... ±22V
Continuous Output Current ..... ±150mA
Continuous Power Dissipation (Note 1)
- LT1010MK 5.0W
- LT1010CK 4.0W
- LT1010CT 4.0W
- LT1010MH 3.1W
- LT1010CH 2.5W
- LT1010CN8 ..... 0.75W

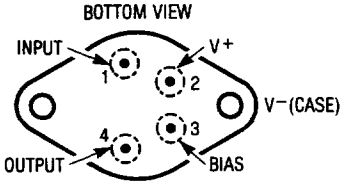
Input Current (Note 2) ..... ±40mA
Operating Junction Temperature
- LT1010M ..... –55°C to 150°C
- LT1010C ..... 0°C to 125°C

Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

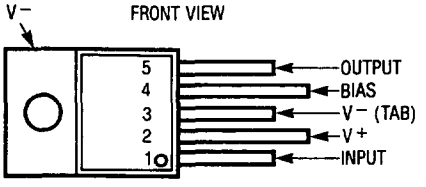
PRECONDITIONING

100% Thermal Limit Burn in

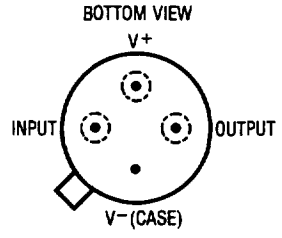
PACKAGE/ORDER INFORMATION

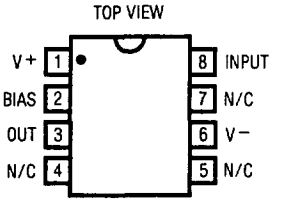
<table>
<tr>
<td> 

K PACKAGE
4-LEAD TO-3 METAL CAN
(STEEL)</td>
<td>ORDER PART NUMBER

LT1010MK
LT1010CK</td>
<td> 

T PACKAGE
5-LEAD TO-220 PLASTIC</td>
<td>ORDER PART NUMBER

LT1010CT</td>
</tr>
<tr>
<td> 

H PACKAGE
4-LEAD TO-39 METAL CAN
(KOVAR BASE)</td>
<td>LT1010MH
LT1010CH</td>
<td> 

N PACKAGE
8-LEAD PLASTIC DIP</td>
<td>LT1010CN8</td>
</tr>
</table>

ELECTRICAL CHARACTERISTICS (See Note 3. Typical values in curves)

SYMBOL	PARAMETER	CONDITIONS (NOTE 3)		LT1010M MIN	LT1010M MAX	LT1010C MIN	LT1010C MAX	UNITS
V_{OS}	Output Offset Voltage	Note 3		20	110	0	150	mV
			●	−10	220	−20	220	mV
		$V_S = \pm 15V$, $V_{IN} = 0$		40	90	20	100	mV
I_B	Input Bias Current	$I_{OUT} = 0$		0	150	0	250	µA
		$I_{OUT} \leq 150mA$		0	250	0	500	µA
			●	0	300	0	800	µA
A_V	Large Signal Voltage Gain		●	0.995	1.00	0.995	1.00	V/V
R_{OUT}	Output Resistance	$I_{OUT} = \pm 1mA$		6	9	5	10	Ω
		$I_{OUT} = \pm 150mA$		6	9	5	10	Ω
			●		12		12	Ω
	Slew Rate	$V_S = \pm 15V$, $V_{IN} = \pm 10V$						
		$V_{OUT} = \pm 8V$, $R_L = 100\Omega$		75		75		V/µs
V_{SOS}^+	Positive Saturation Offset	Note 4, $I_{OUT} = 0$			1.0		1.0	V
			●		1.1		1.1	V
V_{SOS}^-	Negative Saturation Offset	Note 4, $I_{OUT} = 0$			0.2		0.2	V
			●		0.3		0.3	V
R_{SAT}	Saturation Resistance	Note 4, $I_{OUT} = \pm 150mA$			18		22	Ω
			●		24		28	Ω
V_{BIAS}	Bias Terminal Voltage	Note 5, $R_{BIAS} = 20\Omega$		750	810	700	840	mV
			●	560	925	560	880	mV
I_S	Supply Current	$I_{OUT} = 0$, $I_{BIAS} = 0$			8		9	mA
			●		9		10	mA

Note 1: For case temperatures above 25°C, dissipation must be derated based on a thermal resistance of 25°C/W with the K and T packages, 40°C/W with the H package, and 130°C/W for N8 package for *ambient* temperatures above 25°C. See applications information.

Note 2: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V^+ or 0.5V below V^-.

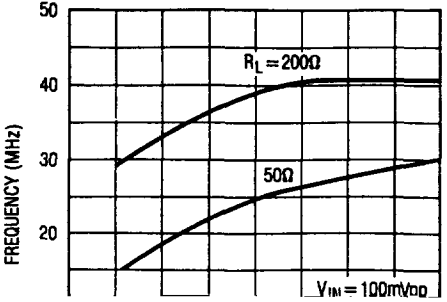
Note 3: Specifications apply for $4.5V \leq V_S \leq 40V$, $V^- + 0.5V \leq V_{IN} \leq V^+ - 1.5V$ and $I_{OUT} = 0$, unless otherwise stated. Temperature range is $-55°C \leq T_j \leq 150°C$, $T_C \leq 125°C$, for the LT1010M and $0°C \leq T_j \leq 125°C$, $T_C \leq 100°C$, for the LT1010C. The ● denotes the specifications that apply over the full temperature range.

Note 4: The output saturation characteristics are measured with 100mV output clipping. See applications information for determining available output swing and input drive requirements for a given load.

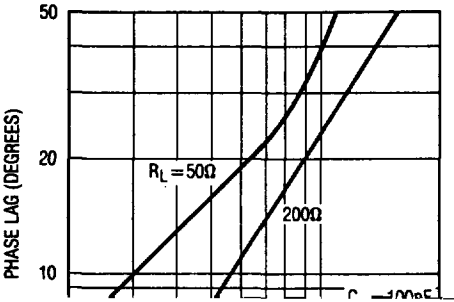
Note 5: With the TO-3 and TO-220 packages, output stage quiescent current can be increased by connecting a resistor between the bias pin and V^+. The increase is equal to the bias terminal voltage divided by this resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

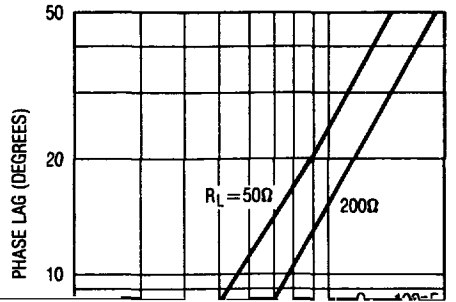
Bandwidth



Phase Lag

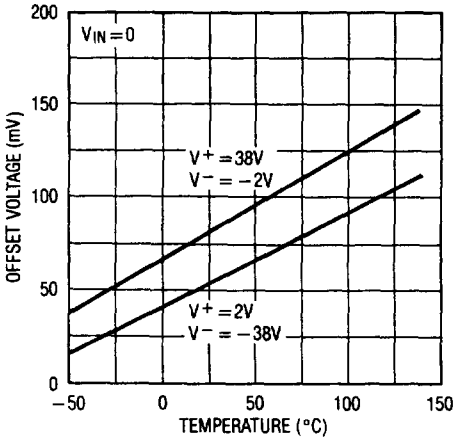


Phase Lag

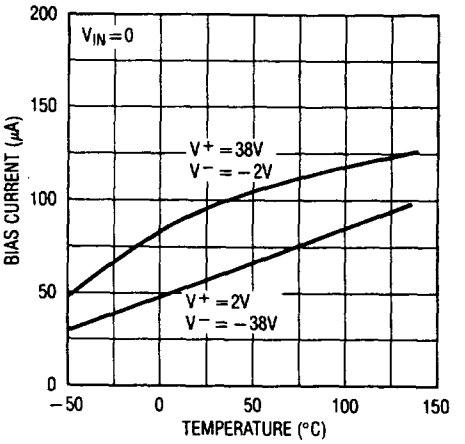


TYPICAL PERFORMANCE CHARACTERISTICS

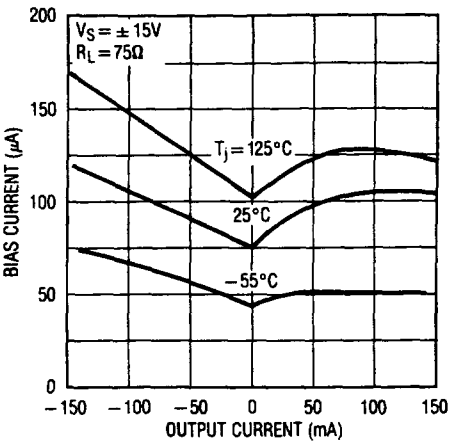
Output Offset Voltage



Input Bias Current

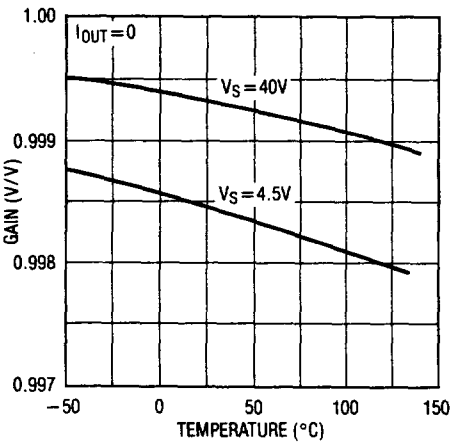


Input Bias Current

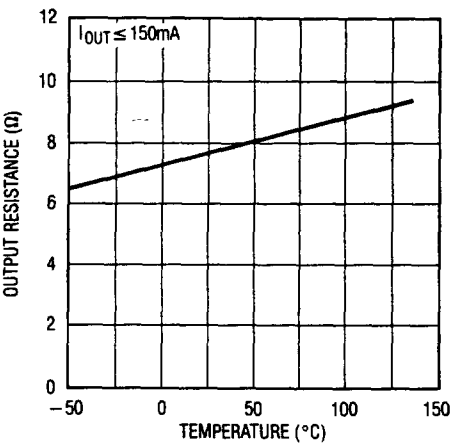


2

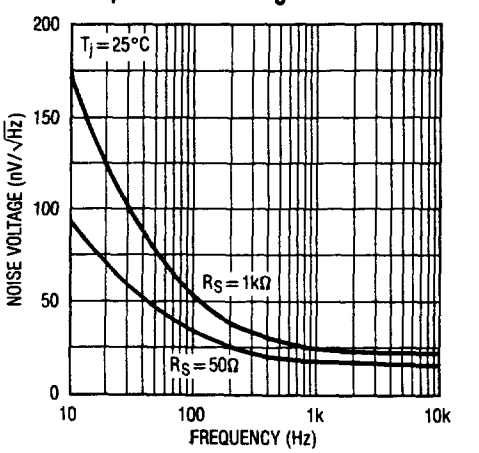
Voltage Gain



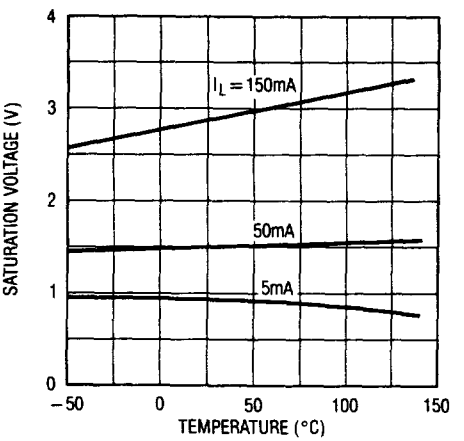
Output Resistance



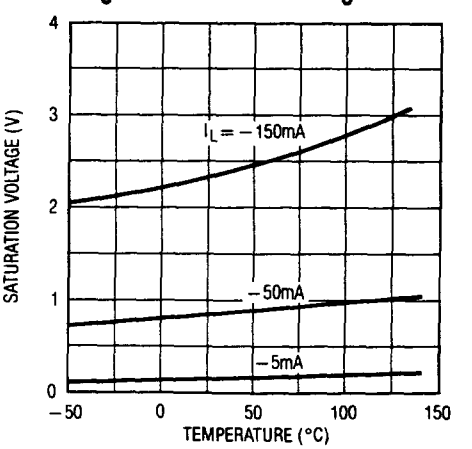
Output Noise Voltage



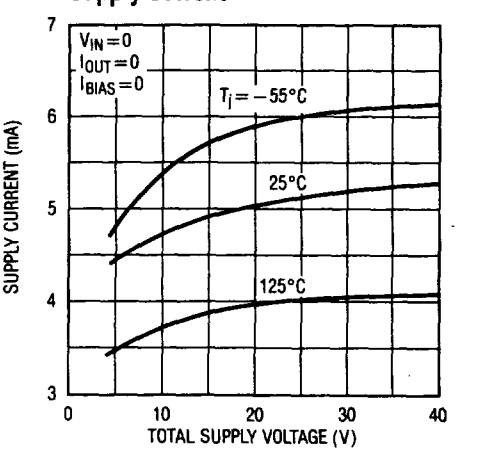
Positive Saturation Voltage



Negative Saturation Voltage

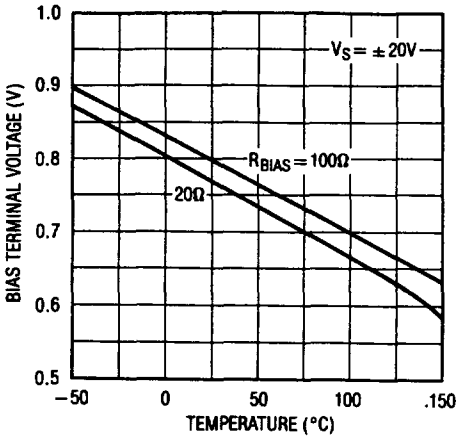


Supply Current

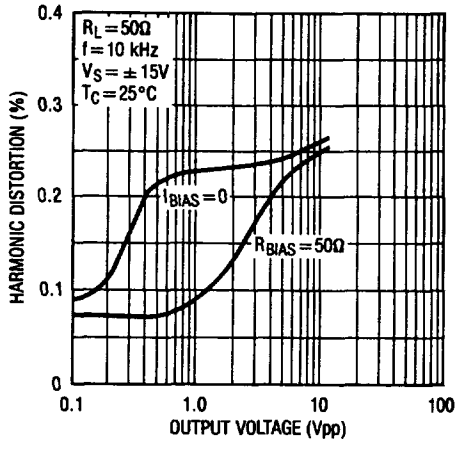


TYPICAL PERFORMANCE CHARACTERISTICS

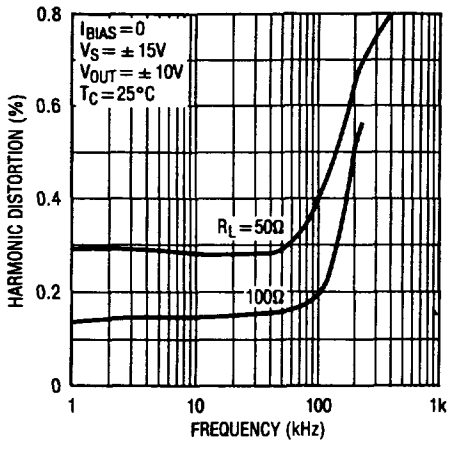
Bias Terminal Voltage



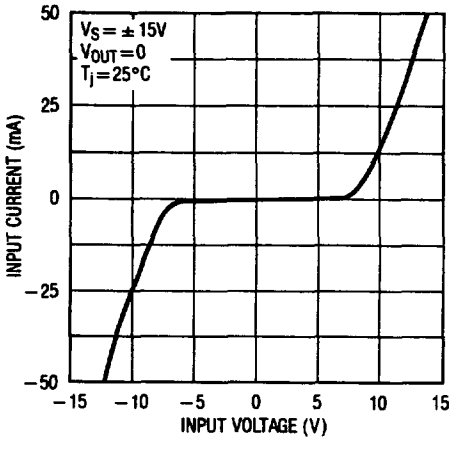
Total Harmonic Distortion



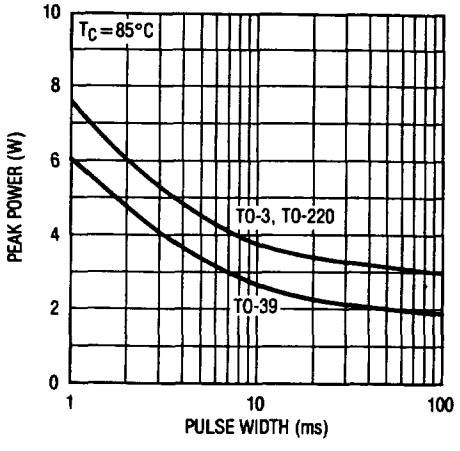
Total Harmonic Distortion



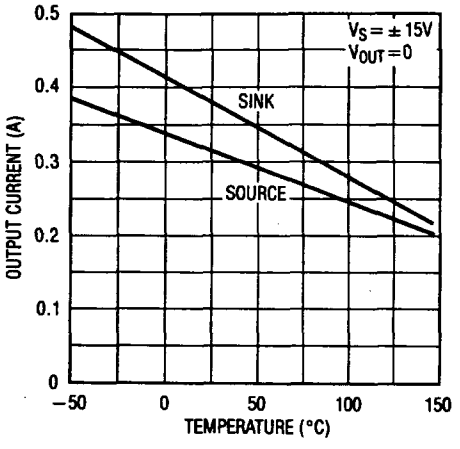
Shorted Input Characteristics



Peak Power Capability



Peak Output Current



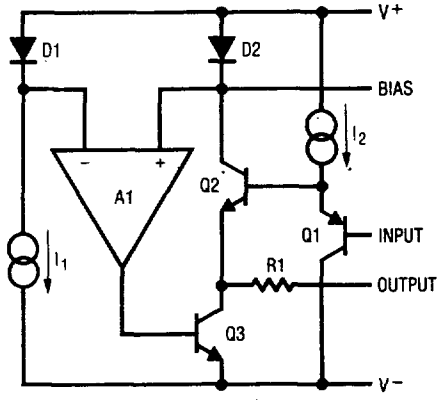
APPLICATIONS INFORMATION

General

These notes briefly describe the LT1010 and how it is used; a detailed explanation is given elsewhere*. Emphasis here will be on practical suggestions that have resulted from working extensively with the part over a wide range of conditions. A number of applications are also outlined that demonstrate the usefulness of the buffer beyond that of driving a heavy load.

Design Concept

The schematic below describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower, Q2, never drops below the quiescent value (determined by I_1 and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.

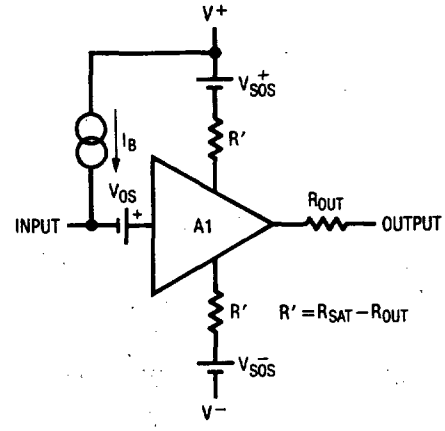


The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V^+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single-supply operation.

*R. J. Widlar, "Unique IC Buffer Enhances Op Amp Designs; Tames Fast Amplifiers," *Linear Technology Corp. TP-1*, April, 1984.

Equivalent Circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown here for both small and large signal operation. The internal element, A1, is an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. Its output also saturates to the internal supply terminals†.



Loaded voltage gain can be determined from the unloaded gain, A_V, the output resistance, R_{OUT}, and the load resistance, R_L, using:

$$A_{VL} = \frac{A_V R_L}{R_{OUT} + R_L}$$

Maximum positive output swing is given by:

$$V_{OUT}^+ = \frac{(V^+ - V_{SOS}^+) R_L}{R_{SAT} + R_L}$$

The input swing required for this output is:

$$V_{IN}^+ = V_{OUT}^+ \left(1 + \frac{R_{OUT}}{R_L}\right) - V_{OS} + \Delta V_{OS},$$

where ΔV_{OS} is the 100mV clipping specified for the saturation measurements. Negative output swing and input drive requirements are similarly determined.

† See electrical characteristics section for guaranteed limits.

APPLICATIONS INFORMATION

Supply Bypass

The buffer is no more sensitive to supply bypassing than slower op amps, as far as stability is concerned. The 0.1μF disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/μs, using 10μF solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time. Adequate bypassing can usually be provided by 10μF solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air is 150°C/W for the TO-39 package, 100°C/W for the TO-220 package, 60°C/W for the TO-3 package, and 130°C/W for the miniDIP package. Circulating air, a heat sink, or mounting the package to a printed circuit board will reduce thermal resistance.

In dc circuits, buffer dissipation is easily computed. In ac circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With ac loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case, to 30°C/W for the TO-39 package and 15°C/W for the TO-3 and TO-220 packages, as long as the peak rating of neither output transistor is exceeded. The typical curves indicate the peak dissipation capabilities of one output transistor.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to insure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

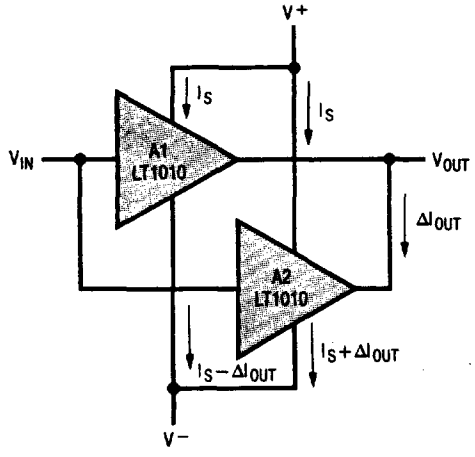
Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this cannot be done with the TO-39 package.

APPLICATIONS INFORMATION

Parallel Operation



Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT}, flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}},$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst case $(V_{IN} - V^+)$ increase in standby dissipation can be assumed to be $\Delta I_{OUT}\, V_T$, where V_T is the total supply voltage.

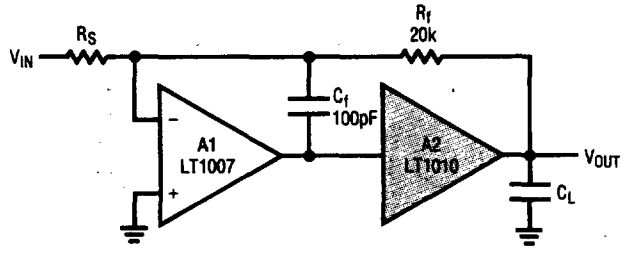
Offset voltage is specified worst case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25°C$ will suffice for a worst case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage, the 25°C limits should be used for worst case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at 25°C.

Isolating Capacitive Loads



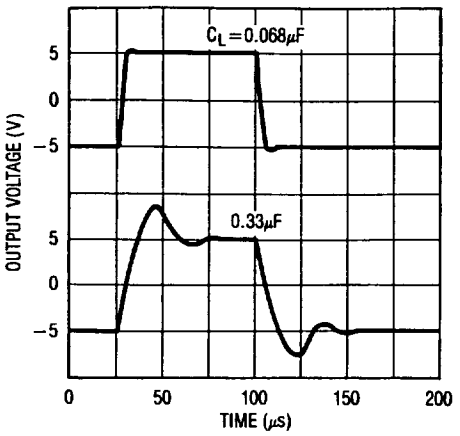
The inverting amplifier above shows the recommended method of isolating capacitve loads. Non-inverting amplifiers are handled similarly.

At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f, so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

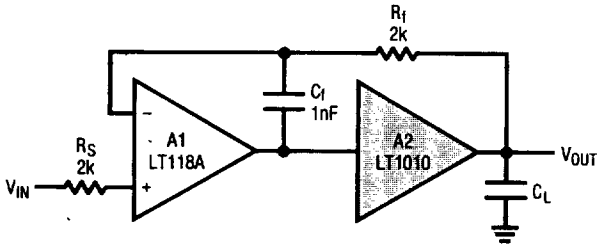
Stability depends upon the R_fC_f time constant, or the closed loop bandwidth. With an 80kHz bandwidth, ringing is negligible for $C_L = 0.068\mu F$ and damps rapidly for $C_L = 0.33\mu F$. The pulse response is shown in the graph.

APPLICATIONS INFORMATION

Pulse Response



Small signal bandwidth is reduced by C_f, but considerable isolation can be obtained without reducing it below the power bandwidth. Often, a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

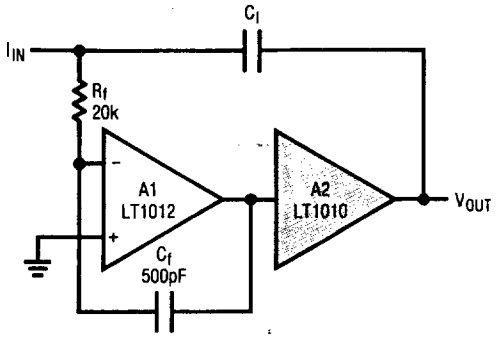


The follower configuration is unique in that capacitive load isolation is obtained without a reduction in small signal bandwidth, although the output impedance of the buffer comes into play at high frequencies. The precision unity-gain buffer above has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3μF, again determined by R_fC_f.

This is a good example of how fast op amps can be made quite easy to use by employing an output buffer.

Integrator

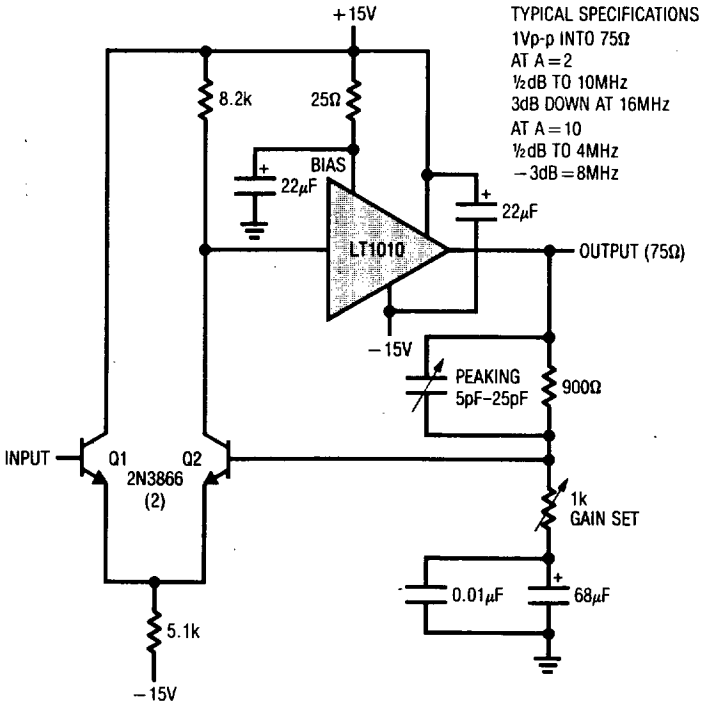
A low pass amplifier can be formed just by using large C_f in the inverter described earlier, as long as the increasing closed loop output impedance above the cutoff frequency is not a problem and the op amp is capable of supplying the required current at the summing junction.



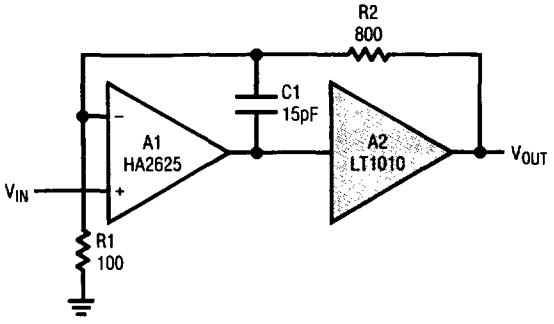
If the integrating capacitor must be driven from the buffer output, the circuit above can be used to provide capacitive load isolation. As before, the stability with large capacitive loads is determined by R_fC_f.

Wideband Amplifiers

This simple circuit provides an adjustable gain video amplifier which will drive 1Vp-p into 75Ω. The differential pair provides gain, with the LT1010 serving as an output stage. Feedback is arranged in the conventional manner, although the 68μF – 0.01 combination limits dc gain to unity for all gain settings. For applications sensitive to NTSC requirements, dropping the 25Ω output stage bias value will aid performance.



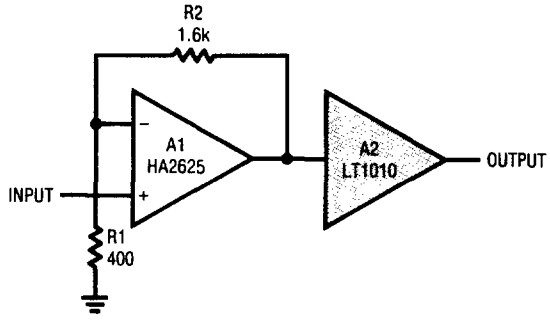
APPLICATIONS INFORMATION



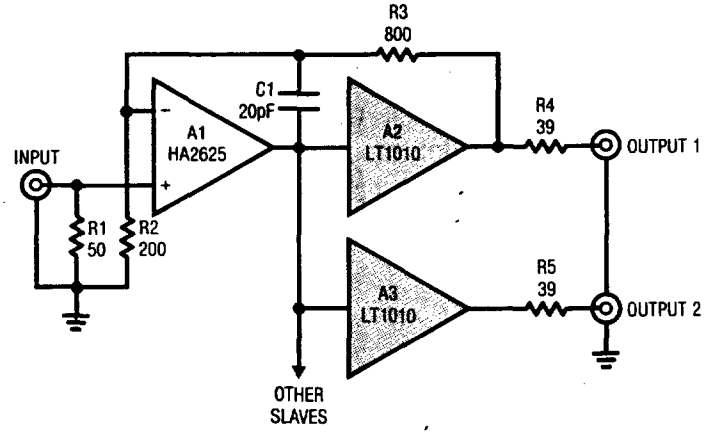
This shows the buffer being used with a wideband amplifier that is not unity-gain stable. In this case, C1 cannot be used to isolate large capacitive loads. Instead, it has an optimum value for a limited range of load capacitances.

The buffer can cause stability problems in circuits like this. With the TO-3 and TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V^+. Alternately, devices in the TO-39 package or miniDIP can be operated in parallel.

It is possible to improve capacitive load stability by operating the buffer class-A at high frequencies. This is done by using quiescent current boost and bypassing the bias terminal to V^- with more than 0.02μF.



Putting the buffer outside the feedback loop as shown here will give capacitive load isolation, with large output capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.



The 50Ω video line splitter here puts feedback on one buffer, with the others slaved. Offset and gain accuracy of slaves depend on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers,special attention should *always* be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

APPLICATIONS INFORMATION

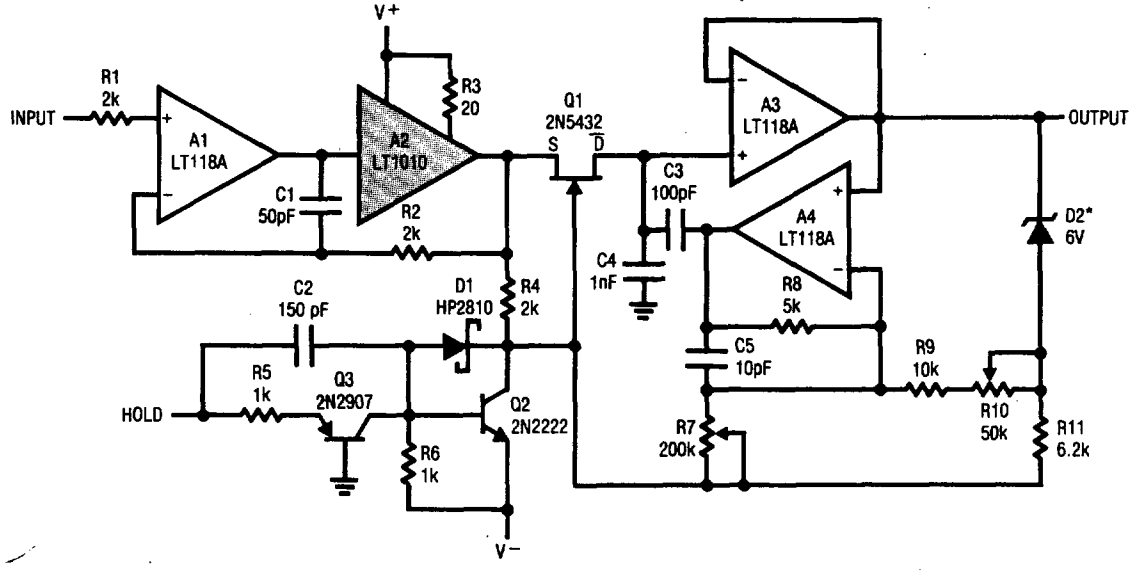
Track and Hold

The 5MHz track and hold shown here has a 400kHz power bandwidth driving ±10V. A buffered input follower drives the hold capacitor, C4, through Q1, a low resistance FET switch. The positive hold command is supplied by TTL logic, with Q3 level shifting to the switch driver, Q2. The output is buffered by A3.

When the gate is driven to V⁻ for HOLD, it pulls charge out of the hold capacitor. A compensating charge is put into the hold capacitor through C3. The step into hold is made independent of the input level with R7 and adjusted to zero with R10.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended. Raising buffer quiescent current to 40mA with R3 improves frequency response.

This circuit is equally useful as a fast acquisition sample and hold. An LF156 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.

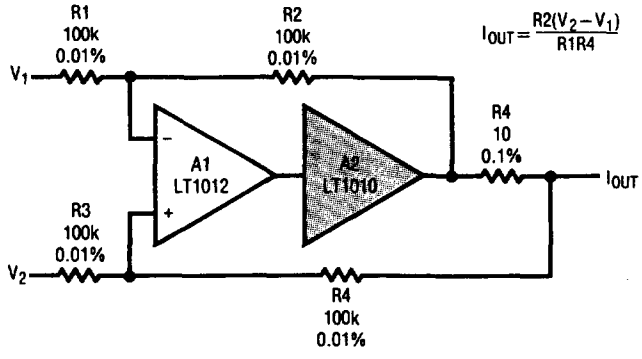


*2N2369 EMITTER BASE JUNCTION

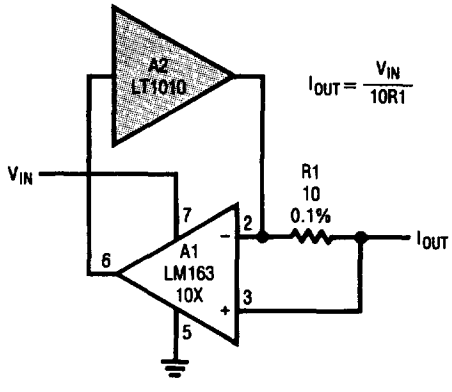
APPLICATIONS INFORMATION

Current Sources

A standard op amp voltage to current converter with a buffer to increase output current is shown here. As usual, excellent matching of the feedback resistors is required to get high output resistance. Output is bi-directional.



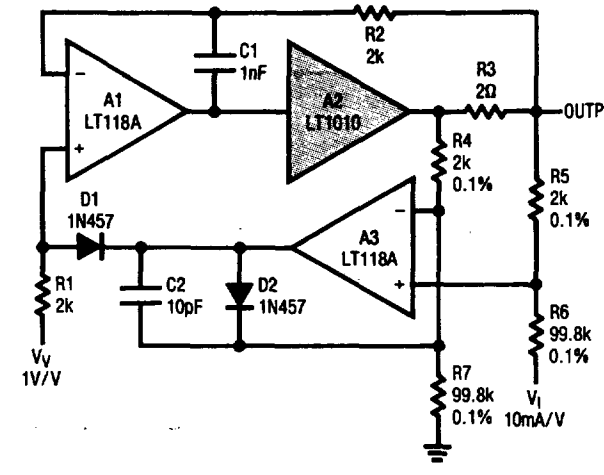
This circuit uses an instrumentation amplifier to eliminate the matched resistors. The input is not high impedance and must be driven from a low impedance source like an op amp. Reversal of output sense can be obtained by grounding pin 7 of the LM163 and driving pin 5.



Output resistances of several megohms can be obtained with both circuits. This is impressive considering the ±150mA output capability. High frequency output characteristics will depend on the bandwidth and slew rate of the amplifiers. Both these circuits have an equivalent output capacitance of about 30nF.

Voltage/Current Regulator

This circuit regulates the output voltage at V_V until the load current reaches a value programmed by V_I. For heavier loads, it is a precision current regulator.



With output currents below the current limit, the current regulator is disconnected from the loop by D1, with D2 keeping its output out of saturation. This output clamp enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

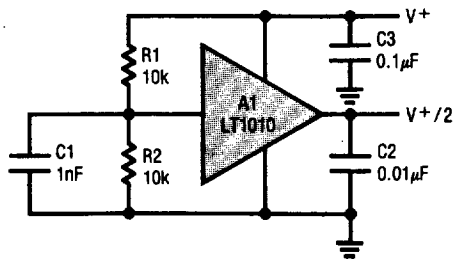
In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery as well as capacitive load stability are determined by C1. Recovery from short circuit is clean.

Bi-directional current limit can be obtained by adding another op amp connected as a complement to A3.

APPLICATIONS INFORMATION

Supply Splitter

Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown here can source or sink 150mA.

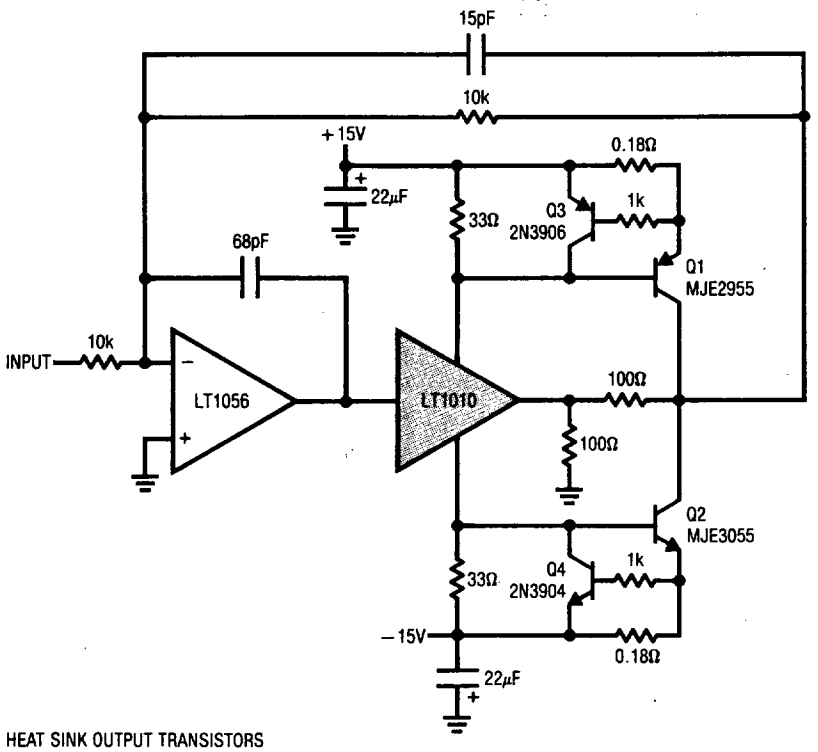


The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

High Current Booster

The circuit below uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads, such as linear actuator coils in disk drives.

The 33Ω resistors sense the LT1010's supply current, with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.



HEAT SINK OUTPUT TRANSISTORS

Wideband FET Input Stabilized Buffer

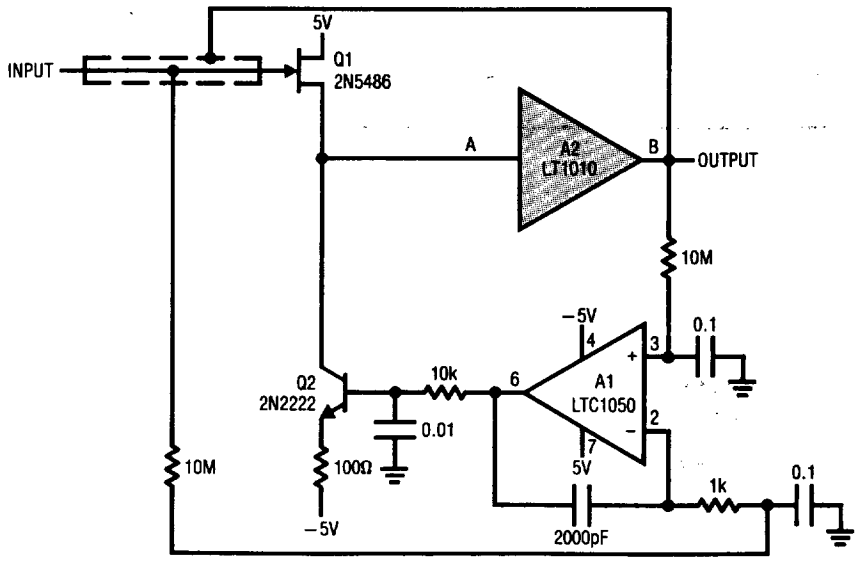
The figure below shows a highly stable unity gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open loop configuration would be quite drifty because there is no dc feedback. The LTC1050 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

Gain Trimmable Wideband FET Amplifier

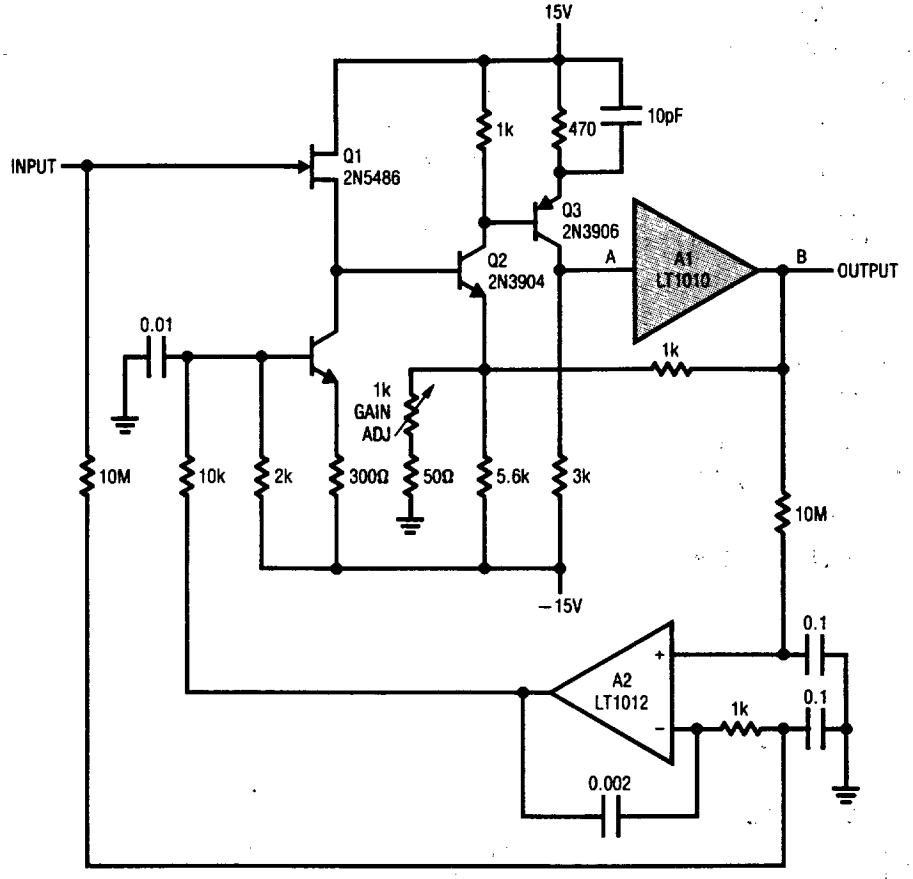
A potential difficulty with the previous circuit is that the gain is not quite unity. The figure labelled (A) on the next page maintains high speed and low bias while achieving a true unity gain transfer function.

This circuit is somewhat similar, except that the Q2-Q3 stage takes gain. A2 dc stabilizes the input-output path, and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010 output stage slew and full power bandwidth (1Vp-p) are 100V/μs and 10MHz, respectively. –3dB bandwidth exceeds 35MHz. At A = 10 (e.g., 1k adjustment set at 50Ω) full power bandwidth stays at 10MHz while the –3dB point falls to 22MHz.

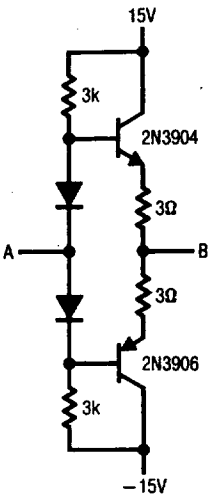
With the optional discrete stage, slew exceeds 1000V/μs and full power bandwidth (1Vp-p) is 18MHz. –3dB bandwidth is 58MHz. At A = 10, full power is available to 10MHz, with the –3dB point at 36MHz.



Figures A and B show response with both output stages. The LT1010 is used in Figure A (Trace A = input, Trace B = output). Figure B uses the discrete stage and is slightly faster. Either stage provides more than adequate performance for driving video cable or data converters, and the LT1012 maintains dc stability under all conditions.



(A)



(B)

Gain Trimmable Wideband FET Amplifier

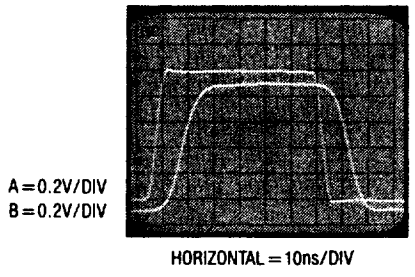


Figure A. Waveforms Using LT1010

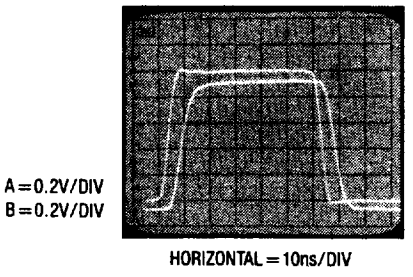


Figure B. Waveforms Using Discrete Stage

DEFINITION OF TERMS

Output Offset Voltage: The output voltage measured with reference to the input.

Input Bias Current: The current out of the input terminal.

Large Signal Voltage Gain: The ratio of the output voltage change to the input voltage change over the specified input voltage range.

Output Resistance: The ratio of the change in output voltage to the change in load current producing it.*

Output Saturation Voltage: The voltage between the output and the supply rail at the limit of the output swing toward that rail.

Saturation Offset Voltage: The output saturation voltage with no load.

Saturation Resistance: The ratio of the change in output saturation voltage to the change in current producing it, going from no load to full load.*

Slew Rate: The average time rate of change of output voltage over the specified output range with an input step between the specified limits.

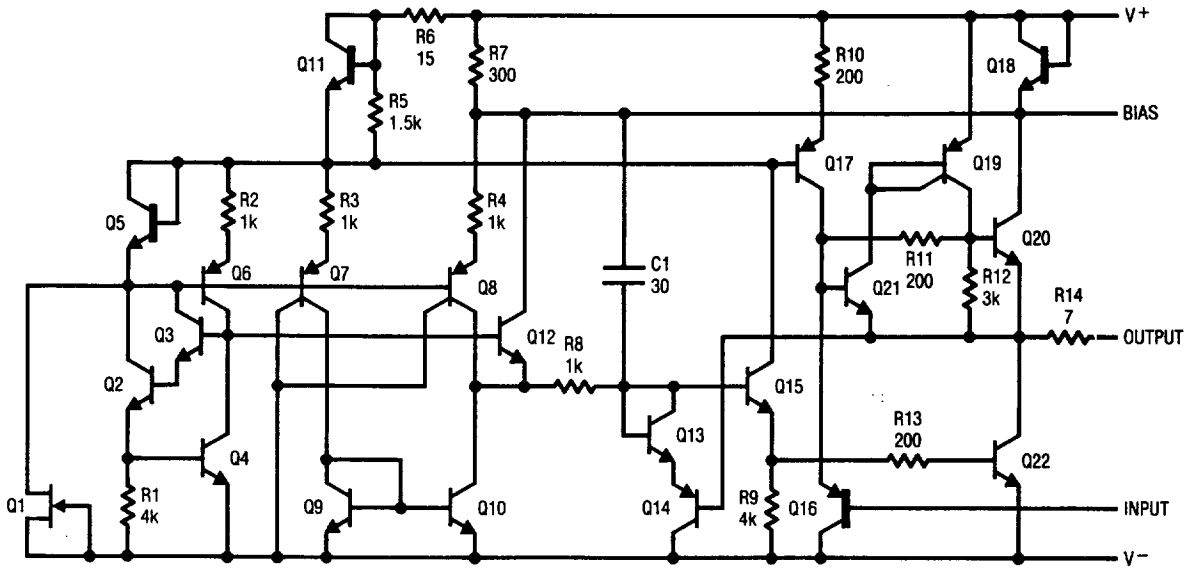
Bias Terminal Voltage: The voltage between the bias terminal and V^+.

Supply Current: The current at either supply terminal with no output loading.

*Pulse measurements (~1ms) as required to minimize thermal effects.

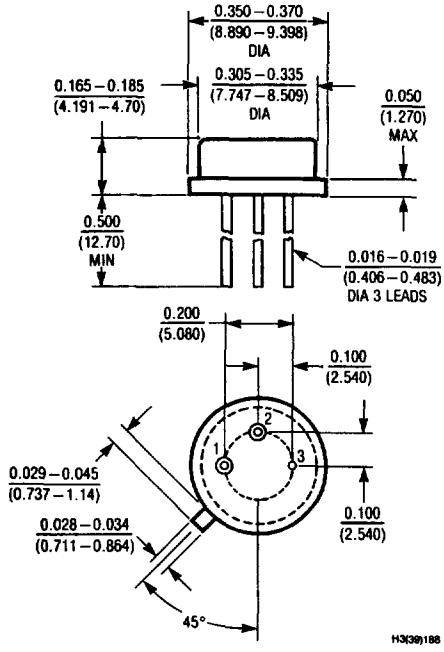
2

SCHEMATIC DIAGRAM (excluding protection circuits)



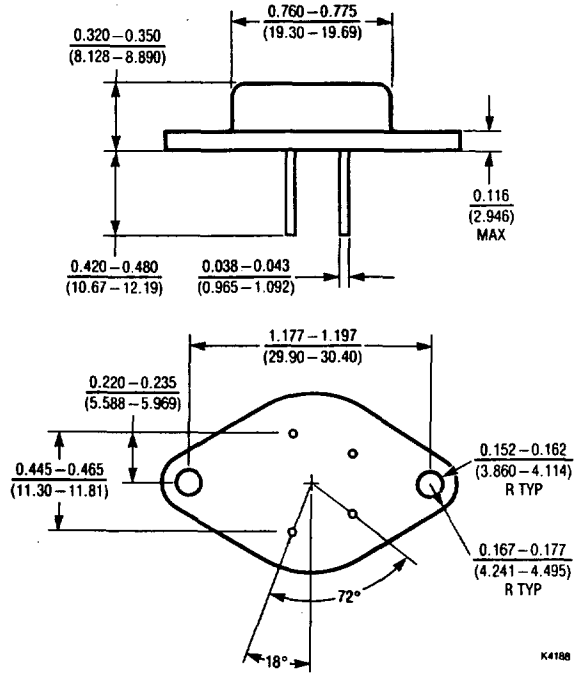
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
4-Lead TO-39 Metal Can
(Kovar Base)



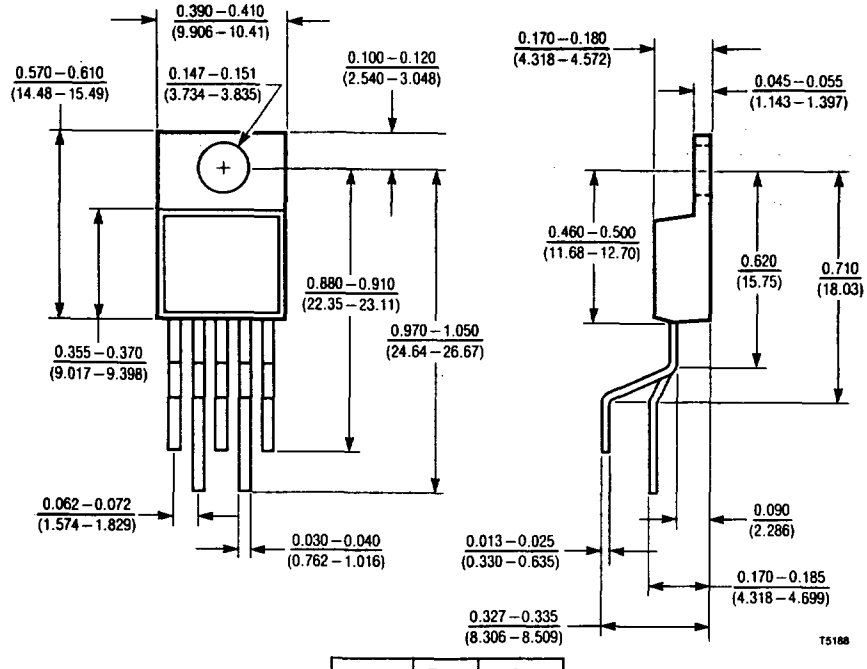
	T_{jmax}	θ_{jc}
LT1010M	150°C	40°C/W
LT1010C	125°C	40°C/W

K Package
4-Lead TO-3 Metal Can
(Steel)



	T_{jmax}	θ_{jc}
LT1010M	150°C	25°C/W
LT1010C	125°C	25°C/W

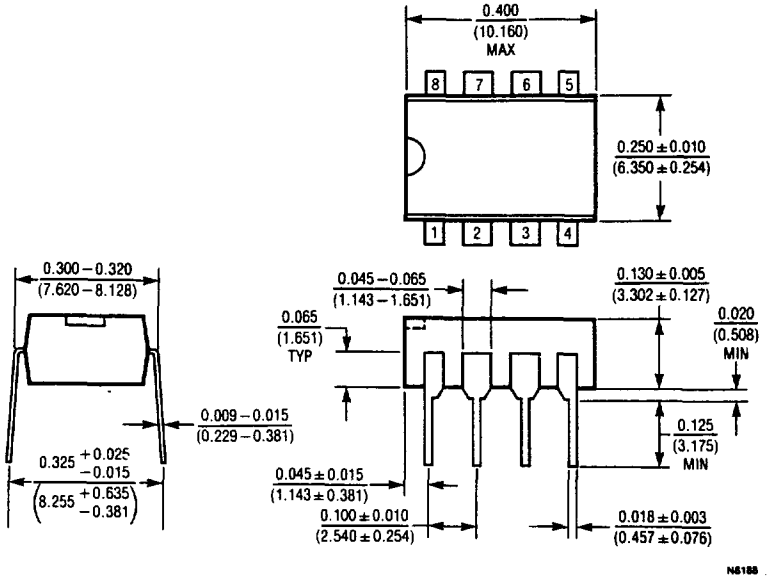
T Package
5-Lead TO-220 Plastic



	T_{jmax}	θ_{jc}
LT1010C	125°C	25°C/W

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N Package
8-Lead Plastic DIP



T_{jmax}	θ_{jc}
150°C	130°C/W

Quad Precision Op Amp (LT1014)
Dual Precision Op Amp (LT1013)

FEATURES

- Single Supply Operation
  - Input Voltage Range Extends to Ground
  - Output Swings to Ground while Sinking Current
- Pin Compatible to 1458 and 324 with Precision Specs
- *Guaranteed* Offset Voltage 150μV Max.
- *Guaranteed* Low Drift 2μV/°C Max.
- *Guaranteed* Offset Current 0.8nA Max.
- *Guaranteed* High Gain
  - 5mA Load Current 1.5 Million Min.
  - 17mA Load Current 0.8 Million Min.
- *Guaranteed* Low Supply Current 500μA Max.
- Low Voltage Noise, 0.1Hz to 10Hz 0.55μVp-p
- Low Current Noise—Better than OP-07, 0.07 pA/√Hz

APPLICATIONS

- Battery-Powered Precision Instrumentation
  - Strain Gauge Signal Conditioners
  - Thermocouple Amplifiers
  - Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detection
- Active Filters
- Multiple Gain Blocks

DESCRIPTION

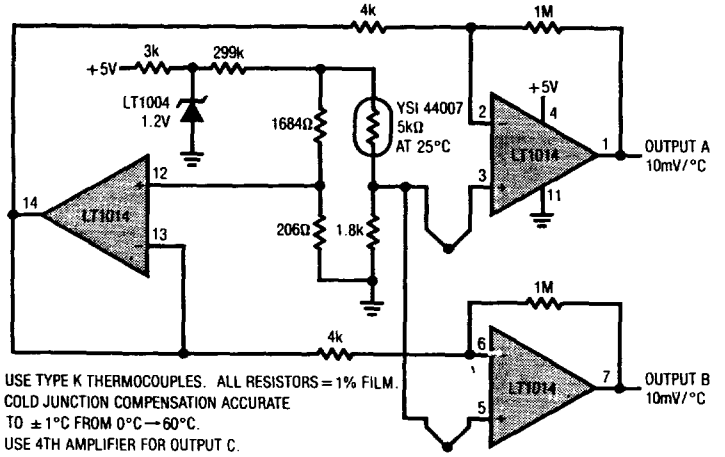
The LT1014 is the first precision quad operational amplifier which directly upgrades designs in the industry standard 14-pin DIP LM324/LM348/OP-11/4156 pin configuration. It is no longer necessary to compromise specifications, while saving board space and cost, as compared to single operational amplifiers.

The LT1014's low offset voltage of 50μV, drift of 0.3μV/°C, offset current of 0.15nA, gain of 8 million, common-mode rejection of 117dB, and power supply rejection of 120dB qualify it as four truly precision operational amplifiers. Particularly important is the low offset voltage, since no offset null terminals are provided in the quad configuration. Although supply current is only 350μA per amplifier, a new output stage design sources and sinks in excess of 20mA of load current, while retaining high voltage gain.

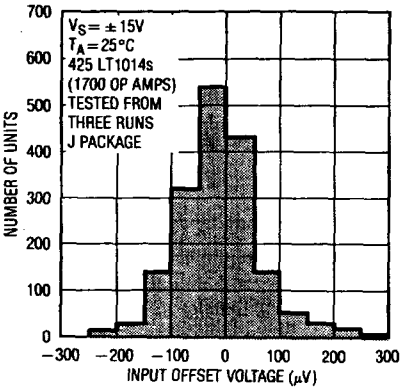
Similarly, the LT1013 is the first precision dual op amp in the 8-pin industry standard configuration, upgrading the performance of such popular devices as the MC1458/1558, LM158 and OP-221. The LT1013's specifications are similar to (even somewhat better than) the LT1014's.

Both the LT1013 and LT1014 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with ±15V and single 5V supplies.

3 Channel Thermocouple Thermometer



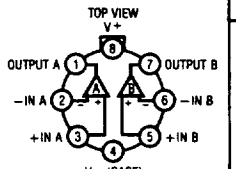
LT1014 Distribution of Offset Voltage



ABSOLUTE MAXIMUM RATINGS

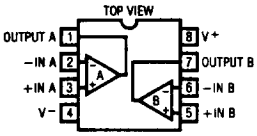
Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range
All Grades ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Operating Temperature Range
LT1013AM/LT1013M/
LT1014AM/LT1014M ..... –55°C to 125°C
LT1013AC/LT1013C/LT1013D
LT1014AC/LT1014C/LT1014D ..... 0°C to 70°C
LT1013I/LT1014I ..... –40°C to 85°C

PACKAGE/ORDER INFORMATION



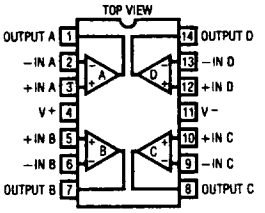
H PACKAGE
8-LEAD TO-5 METAL CAN

ORDER PART NUMBER
LT1013AMH
LT1013MH
LT1013ACH
LT1013CH



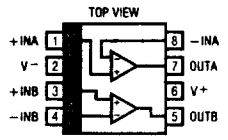
J PACKAGE
8-LEAD CERAMIC DIP
N PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER
LT1013AMJ8
LT1013MJ8
LT1013ACJ8
LT1013CJ8
LT1013CN8
LT1013DN8
LT1013IN8



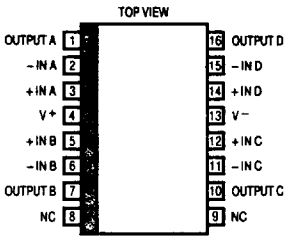
J PACKAGE
14-LEAD CERAMIC DIP
N PACKAGE
14-LEAD PLASTIC DIP

ORDER PART NUMBER
LT1014AMJ
LT1014MJ
LT1014ACJ
LT1014CJ
LT1014CN
LT1014DN
LT1014IN



SO PACKAGE
8-LEAD PLASTIC SOIC
NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE STANDARD 8-PIN DUAL-IN-LINE CONFIGURATION

ORDER PART NUMBER
LT1013DS8
LT1013IS8
PART MARKING
1013
1013I



S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER
LT1014DS
LT1014IS
PART MARKING
LT1014DS
LT1014IS

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/AC LT1014AM/AC			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013	—	40	150	—	60	300	μV
		LT1014	—	50	180	—	60	300	μV
		LT1013D/I, LT1014D/I	—	—	—	—	200	800	μV
	Long Term Input Offset Voltage Stability		—	0.4	—	—	0.5	—	μV/Mo.
I_{OS}	Input Offset Current		—	0.15	0.8	—	0.2	1.5	nA
I_B	Input Bias Current		—	12	20	—	15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	—	0.55	—	—	0.55	—	μVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$	—	24	—	—	24	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$	—	22	—	—	22	—	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_O = 10Hz$	—	0.07	—	—	0.07	—	$pA/\sqrt{Hz}$
	Input Resistance—Differential	(Note 1)	100	400	—	70	300	—	MΩ
	Common-Mode		—	5	—	—	4	—	GΩ

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/AC LT1014AM/AC			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$ $V_O = \pm 10V$, $R_L = 600\Omega$	1.5 0.8	8.0 2.5	— —	1.2 0.5	7.0 2.0	— —	V/μV V/μV
	Input Voltage Range		+13.5 −15.0	+13.8 −15.3	— —	+13.5 −15.0	+13.8 −15.3	— —	V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V, -15.0V$	100	117	—	97	114	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	103	120	—	100	117	—	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$	123	140	—	120	137	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±13	±14	—	±12.5	±14	—	V
	Slew Rate		0.2	0.4	—	0.2	0.4	—	V/μs
I_S	Supply Current	Per Amplifier	—	0.35	0.50	—	0.35	0.55	mA

Note 1: This parameter is guaranteed by design and is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1014s (or 100 LT1013s) typically 240 op amps (or 120) will be better than the indicated specification.

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{OUT} = 1.4V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/AC LT1014AM/AC			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013 LT1014 LT1013D/I, LT1014D/I	— — —	60 70 —	250 280 —	— — —	90 90 250	450 450 950	μV μV μV
I_{OS}	Input Offset Current		—	0.2	1.3	—	0.3	2.0	nA
I_B	Input Bias Current		—	15	35	—	18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	—	1.0	—	—	1.0	—	V/μV
	Input Voltage Range		+3.5 0	+3.8 −0.3	— —	+3.5 0	+3.8 −0.3	— —	V V
V_{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 600Ω to Ground Output Low, $I_{SINK} = 1mA$ Output High, No Load Output High, 600Ω to Ground	— — — 4.0 3.4	15 5 220 4.4 4.0	25 10 350 — —	— — — 4.0 3.4	15 5 220 4.4 4.0	25 10 350 — —	mV mV mV V V
I_S	Supply Current	Per Amplifier	—	0.31	0.45	—	0.32	0.50	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1013AM MIN	LT1013AM TYP	LT1013AM MAX	LT1014AM MIN	LT1014AM TYP	LT1014AM MAX	LT1013M/LT1014M MIN	LT1013M/LT1014M TYP	LT1013M/LT1014M MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	80	300	—	90	350	—	110	550	μV
		$V_S = +5V, 0V$; $V_O = +1.4V$											
		$-55°C \le T_A \le 100°C$	●	—	80	450	—	90	480	—	100	750	μV
		$V_{CM} = 0.1V$, $T_A = 125°C$		—	120	450	—	150	480	—	200	750	μV
		$V_{CM} = 0V$, $T_A = 125°C$		—	250	900	—	300	960	—	400	1500	μV
	Input Offset Voltage Drift	(Note 2)	●	—	0.4	2.0	—	0.4	2.0	—	0.5	2.5	μV/°C
I_{OS}	Input Offset Current		●	—	0.3	2.5	—	0.3	2.8	—	0.4	5.0	nA
		$V_S = +5V, 0V$; $V_O = +1.4V$	●	—	0.6	6.0	—	0.7	7.0	—	0.9	10.0	nA
I_B	Input Bias Current		●	—	15	30	—	15	30	—	18	45	nA
		$V_S = +5V, 0V$; $V_O = +1.4V$	●	—	20	80	—	25	90	—	28	120	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	0.5	2.0	—	0.4	2.0	—	0.25	2.0	—	V/μV
CMRR	Common-Mode Rejection	$V_{CM} = +13.0V, -14.9V$	●	97	114	—	96	114	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	100	117	—	100	117	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.8	—	±12	±13.8	—	±11.5	±13.8	—	V
		$V_S = +5V, 0V$;											
		$R_L = 600\Omega$ to Ground											
		Output Low	●	—	6	15	—	6	15	—	6	18	mV
		Output High	●	3.2	3.8	—	3.2	3.8	—	3.1	3.8	—	V
I_S	Supply Current Per Amplifier		●	—	0.38	0.60	—	0.38	0.60	—	0.38	0.7	mA
		$V_S = +5V, 0V$; $V_O = +1.4V$	●	—	0.34	0.55	—	0.34	0.55	—	0.34	0.65	mA

ELECTRICAL CHARACTERISTICS

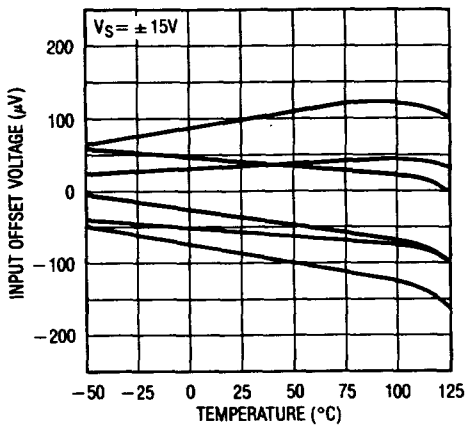
$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$ for LT1013I, LT1014I, $0°C \le T_A \le 70°C$ for LT1013C, LT1013D, LT1014C, LT1014D unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1013AC MIN	LT1013AC TYP	LT1013AC MAX	LT1014AC MIN	LT1014AC TYP	LT1014AC MAX	LT1013C/D/I LT1014C/D/I MIN	LT1013C/D/I LT1014C/D/I TYP	LT1013C/D/I LT1014C/D/I MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	55	240	—	65	270	—	80	400	μV
		LT1013D/I, LT1014D/I	●	—	—	—	—	—	—	—	230	1000	μV
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	75	350	—	85	380	—	110	570	μV
		LT1013D/I, LT1014D/I											
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	—	—	—	—	—	—	280	1200	μV
	Average Input Offset Voltage Drift	(Note 2)	●	—	0.3	2.0	—	0.3	2.0	—	0.4	2.5	μV/°C
		LT1013D/I, LT1014D/I	●	—	—	—	—	—	—	—	0.7	5.0	μV/°C
I_{OS}	Input Offset Current		●	—	0.2	1.5	—	0.2	1.7	—	0.3	2.8	nA
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	0.4	3.5	—	0.4	4.0	—	0.5	6.0	nA
I_B	Input Bias Current		●	—	13	25	—	13	25	—	16	38	nA
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	18	55	—	20	60	—	24	90	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	1.0	5.0	—	1.0	5.0	—	0.7	4.0	—	V/μV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.0V, -15.0V$	●	98	116	—	98	116	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	101	119	—	101	119	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12.5	±13.9	—	±12.5	±13.9	—	±12.0	±13.9	—	V
		$V_S = +5V, 0V$; $R_L = 600\Omega$											
		Output Low	●	—	6	13	—	6	13	—	6	13	mV
		Output High	●	3.3	3.9	—	3.3	3.9	—	3.2	3.9	—	V
I_S	Supply Current per Amplifier		●	—	0.36	0.55	—	0.36	0.55	—	0.37	0.60	mA
		$V_S = +5V, 0V$; $V_O = 1.4V$	●	—	0.32	0.50	—	0.32	0.50	—	0.34	0.55	mA

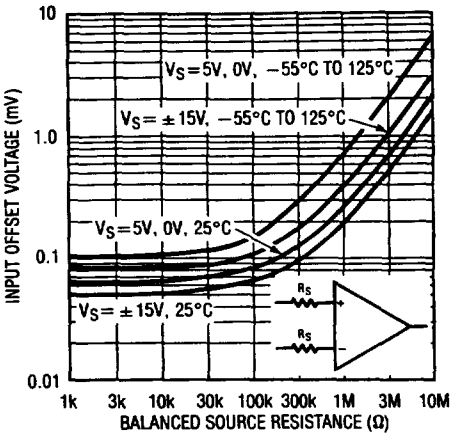
Note 2: This parameter is not 100% tested. The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

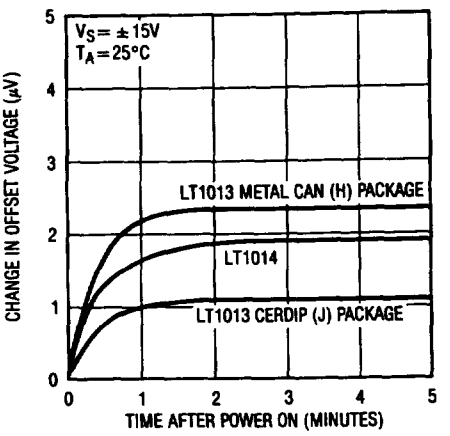
Offset Voltage Drift with Temperature of Representative Units



Offset Voltage vs Balanced Source Resistance

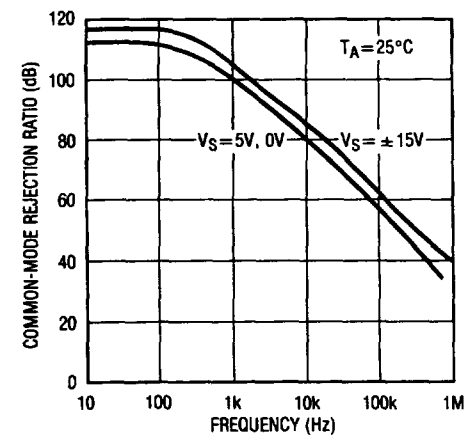


Warm-Up Drift

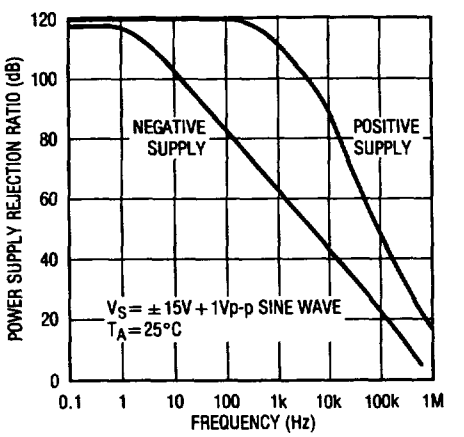


2

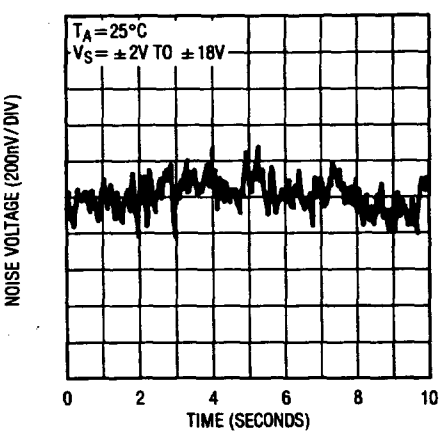
Common-Mode Rejection Ratio vs Frequency



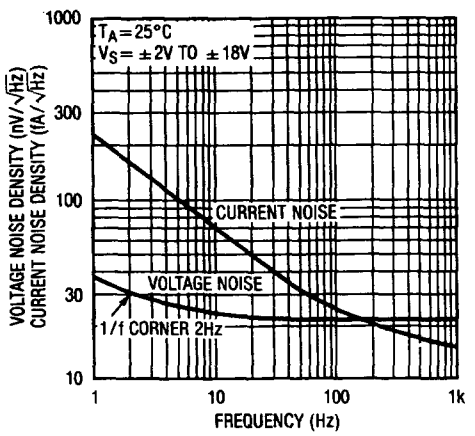
Power Supply Rejection Ratio vs Frequency



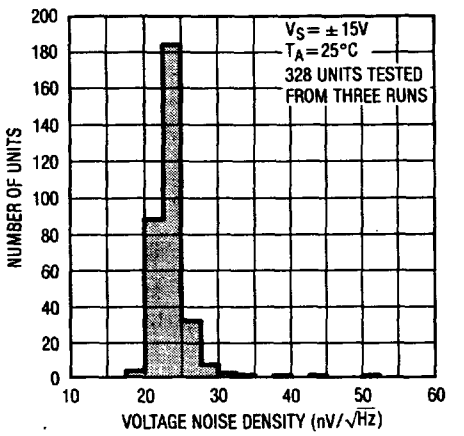
0.1Hz to 10Hz Noise



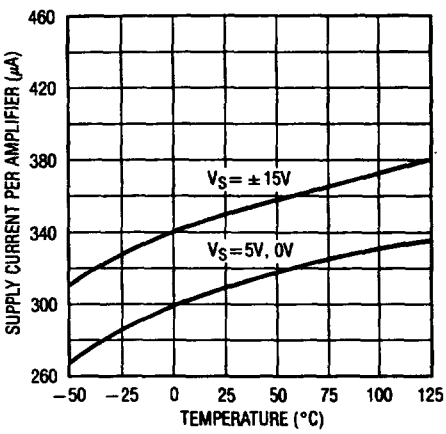
Noise Spectrum



10Hz Voltage Noise Distribution

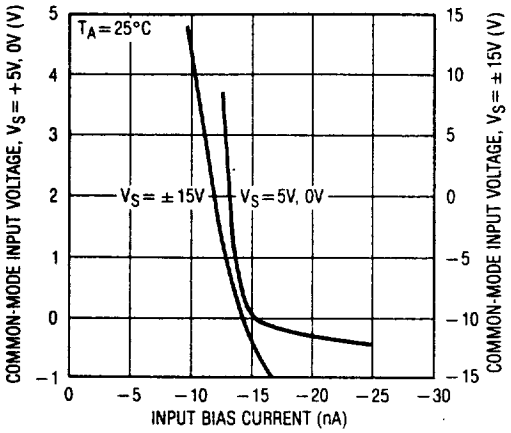


Supply Current vs Temperature

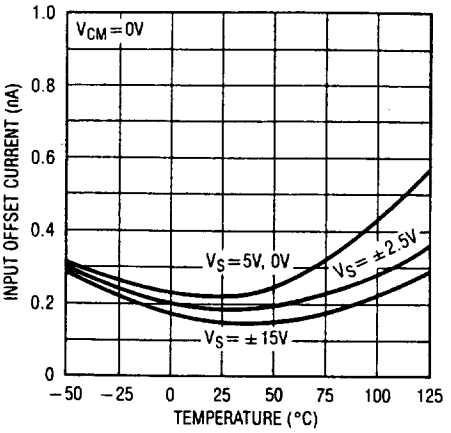


TYPICAL PERFORMANCE CHARACTERISTICS

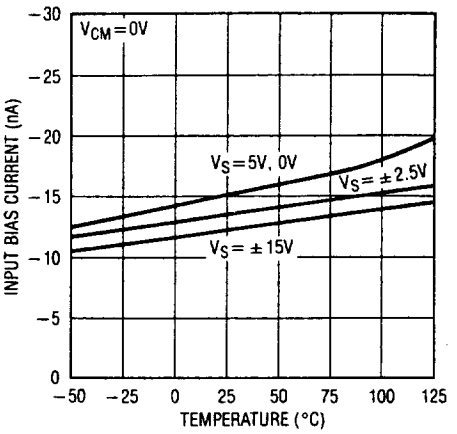
Input Bias Current vs Common-Mode Voltage



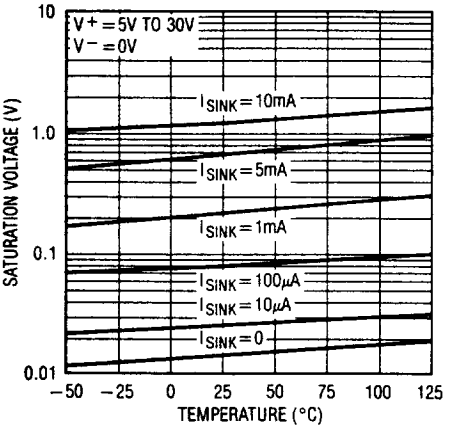
Input Offset Current vs Temperature



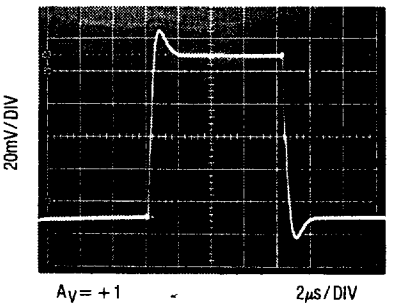
Input Bias Current vs Temperature



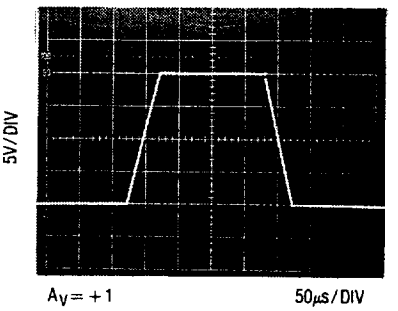
Output Saturation vs Sink Current vs Temperature



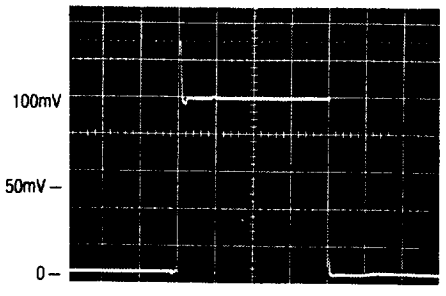
Small Signal Transient Response, $V_S = \pm 15V$



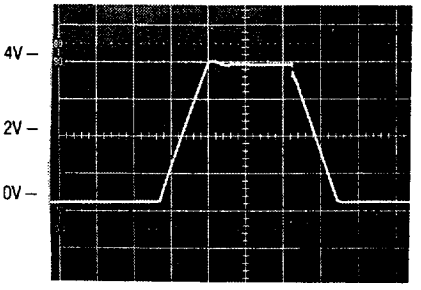
Large Signal Transient Response, $V_S = \pm 15V$



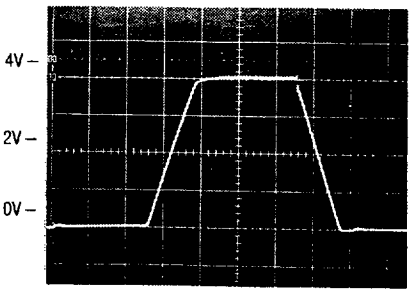
Small Signal Transient Response, $V_S = 5V, 0V$



Large Signal Transient Response, $V_S = 5V, 0V$

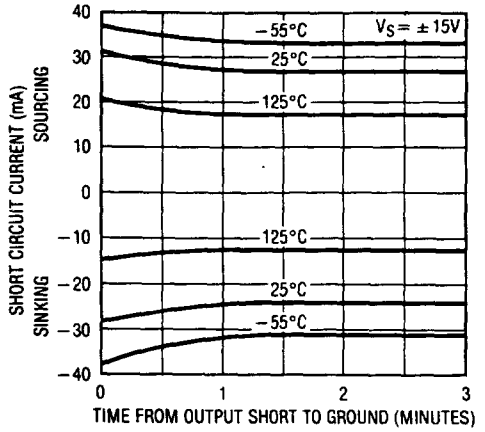


Large Signal Transient Response, $V_S = 5V, 0V$

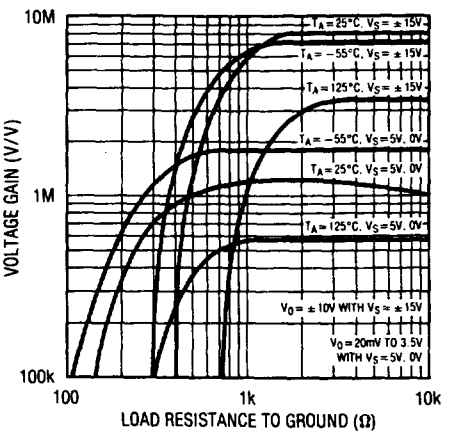


TYPICAL PERFORMANCE CHARACTERISTICS

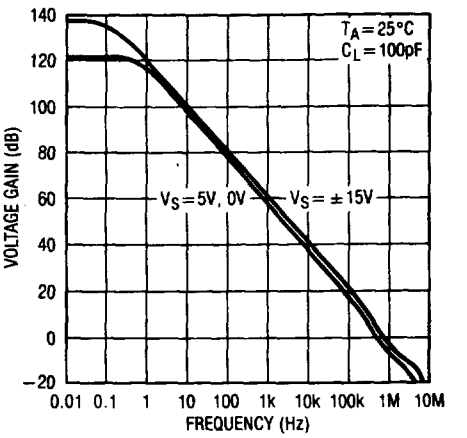
Output Short Circuit Current vs Time



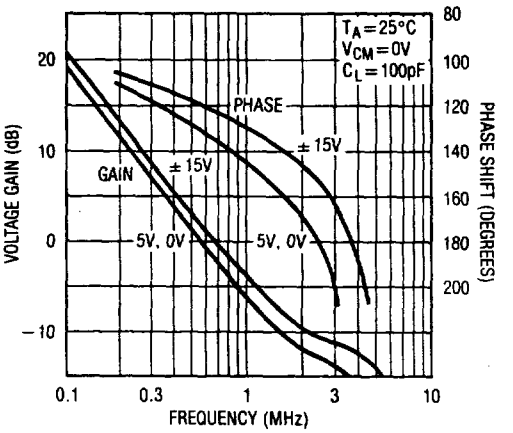
Voltage Gain vs Load Resistance



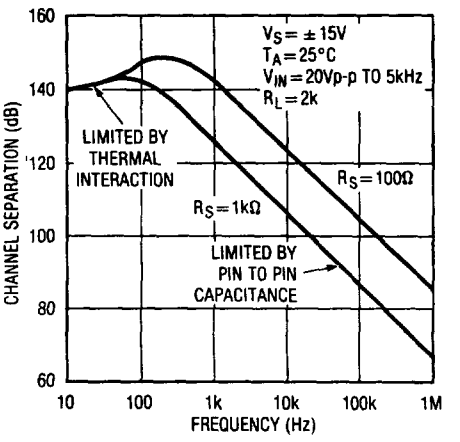
Voltage Gain vs Frequency



Gain, Phase vs Frequency



Channel Separation vs Frequency



APPLICATIONS INFORMATION

Single Supply Operation

The LT1013/1014 are fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1013/LT1014 have specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1013/1014, the 400Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.

APPLICATIONS INFORMATION

(b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1013/1014's outputs do not reverse, as illustrated below, even when the inputs are at −1.5V.

There is one circumstance, however, under which the phase reversal protection circuitry does not function: when the other op amp on the LT1013, or one specific amplifier of the other three on the LT1014, is driven hard into negative saturation at the output.

Phase reversal protection does not work on amplifier:
A when D's output is in negative saturation. B's and C's outputs have no effect.
B when C's output is in negative saturation. A's and D's outputs have no effect.
C when B's output is in negative saturation. A's and D's outputs have no effect.
D when A's output is in negative saturation. B's and C's outputs have no effect.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1013/1014's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

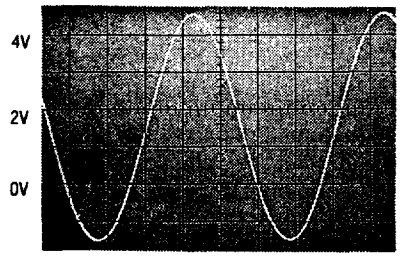
In dual supply operations, the output stage is crossover distortion-free.

Comparator Applications

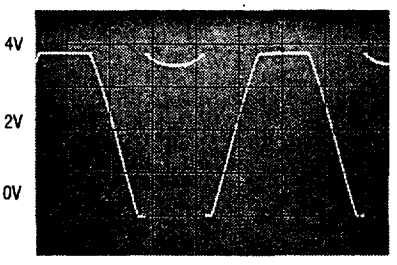
The single supply operation of the LT1013/1014 lends itself to its use as a precision comparator with TTL compatible output:

In systems using both op amps and comparators, the LT1013/1014 can perform multiple duties; for example, on the LT1014, two of devices can be used as op amps and the other two as comparators.

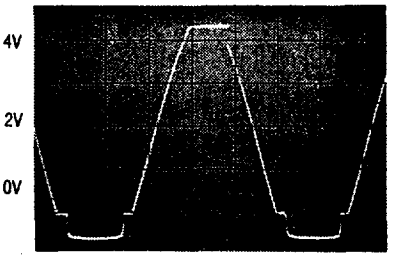
Voltage Follower with Input Exceeding the Negative Common-Mode Range



6Vp-p INPUT, −1.5V TO 4.5V

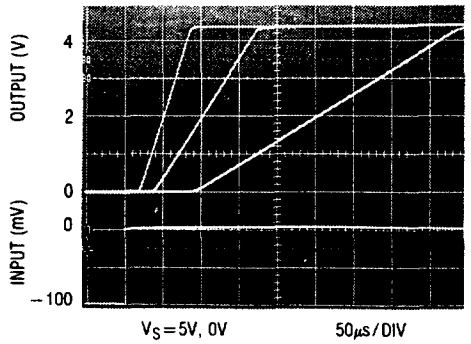


LM324, LM358, OP-20 EXHIBIT OUTPUT PHASE REVERSAL



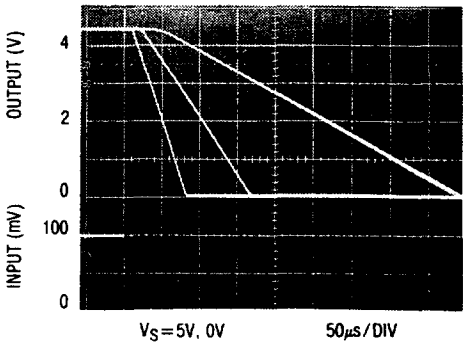
LT1013/LT1014 NO PHASE REVERSAL

Comparator Rise Response Time 10mV, 5mV, 2mV Overdrives



V_S=5V, 0V 50µs/DIV

Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



V_S=5V, 0V 50µs/DIV

APPLICATIONS INFORMATION

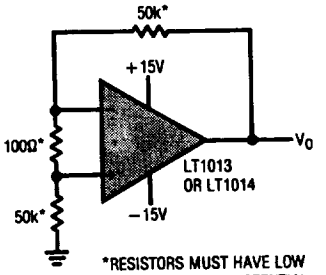
Low Supply Operation

The minimum supply voltage for proper operation of the LT1013/1014 is 3.4V (three Ni-Cad batteries). Typical supply current at this voltage is 290μA, therefore power dissipation is only one milliwatt per amplifier.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1008 data sheet.

Test Circuit for Offset Voltage and Offset Drift with Temperature

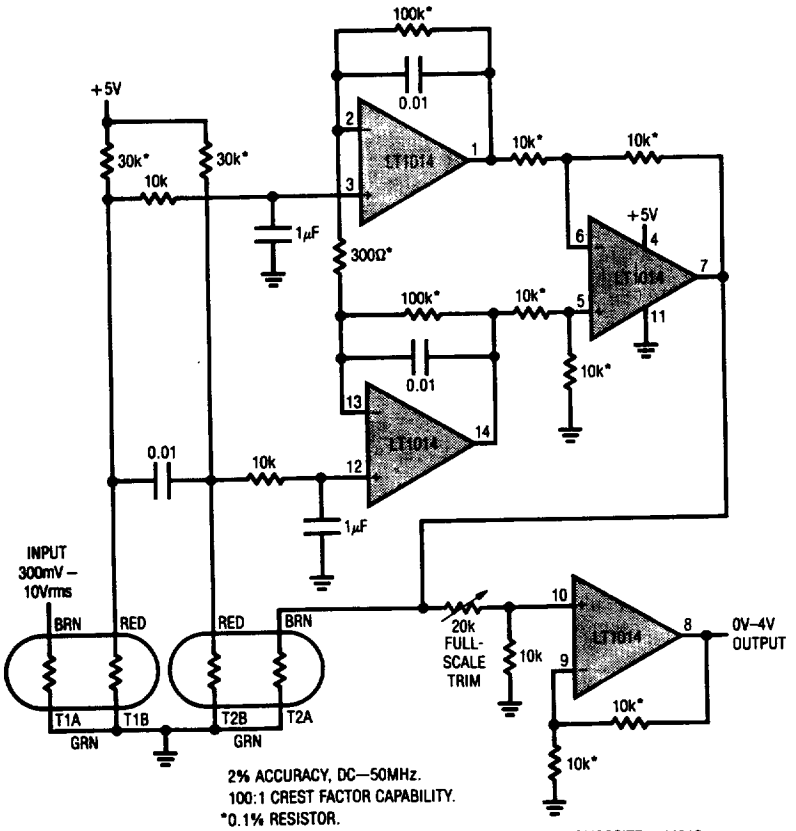


*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO ±20V.
$V_O = 1000V_{OS}$

2

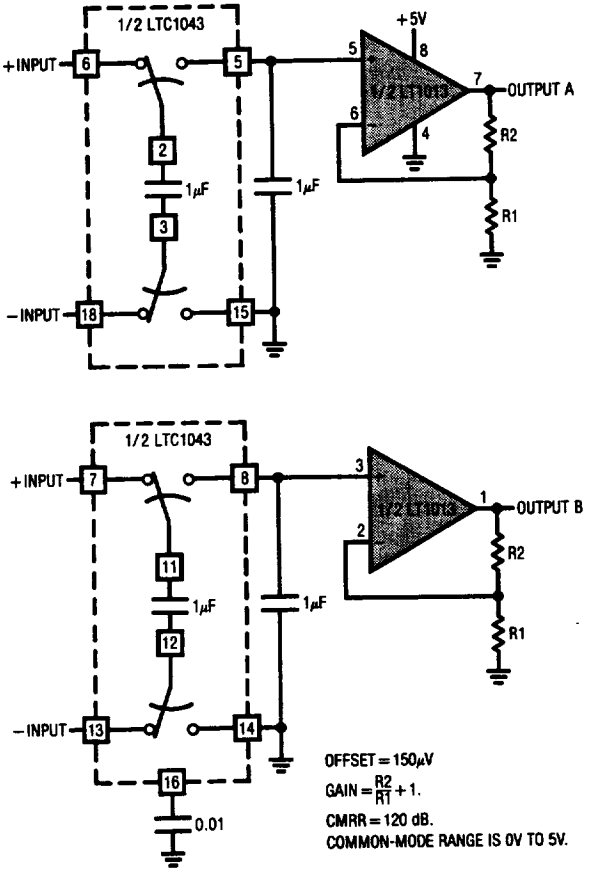
TYPICAL APPLICATIONS

50MHz Thermal rms to DC Converter



2% ACCURACY, DC—50MHz.
100:1 CREST FACTOR CAPABILITY.
*0.1% RESISTOR.
T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE #44018.
ENCLOSE T1 AND T2 IN STYROFOAM.
7.5mW DISSIPATION.

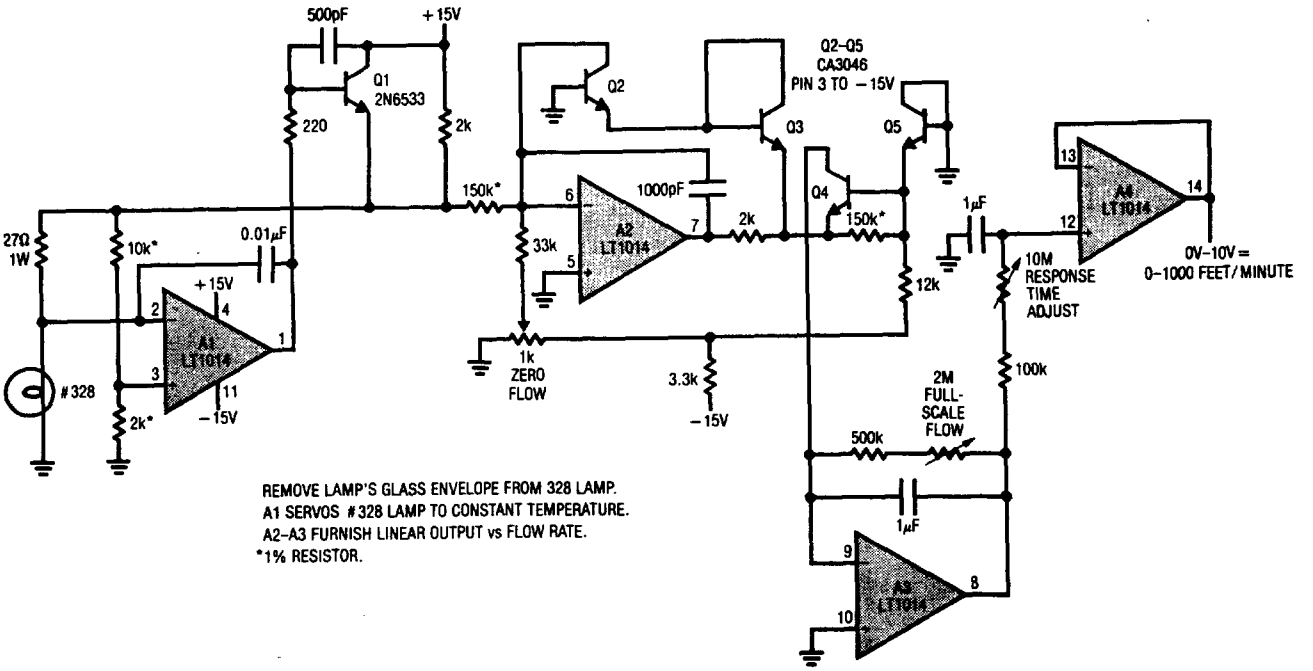
5V Single Supply Dual Instrumentation Amplifier



OFFSET = 150μV
GAIN = $\frac{R2}{R1}$ + 1.
CMRR = 120 dB.
COMMON-MODE RANGE IS 0V TO 5V.

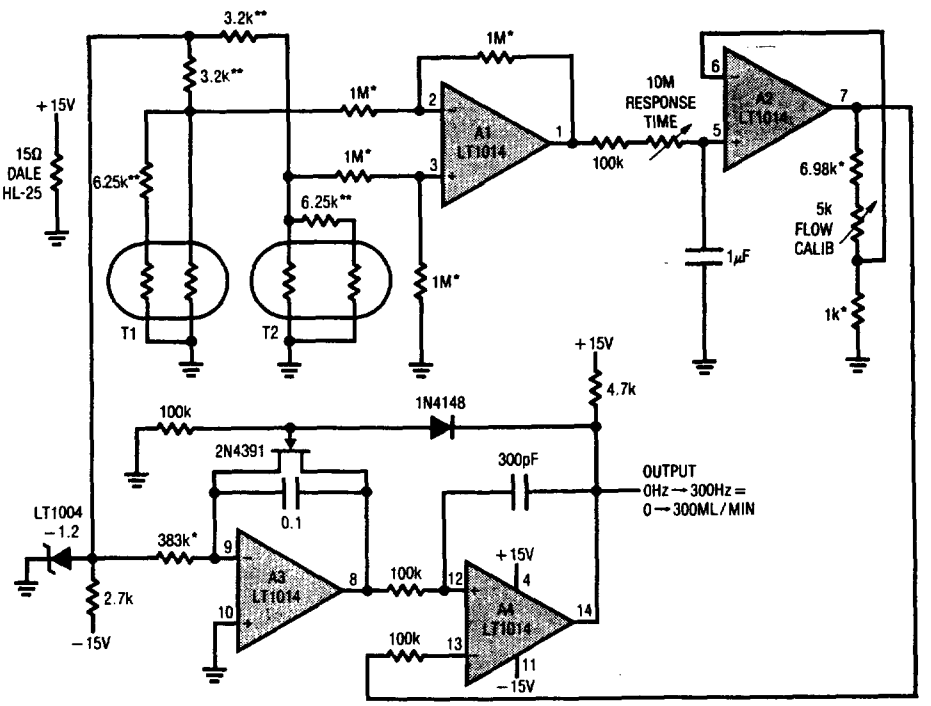
TYPICAL APPLICATIONS

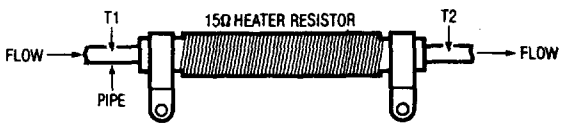
Hot Wire Anemometer



REMOVE LAMP'S GLASS ENVELOPE FROM 328 LAMP.
A1 SERVOS #328 LAMP TO CONSTANT TEMPERATURE.
A2–A3 FURNISH LINEAR OUTPUT vs FLOW RATE.
*1% RESISTOR.

Liquid Flowmeter

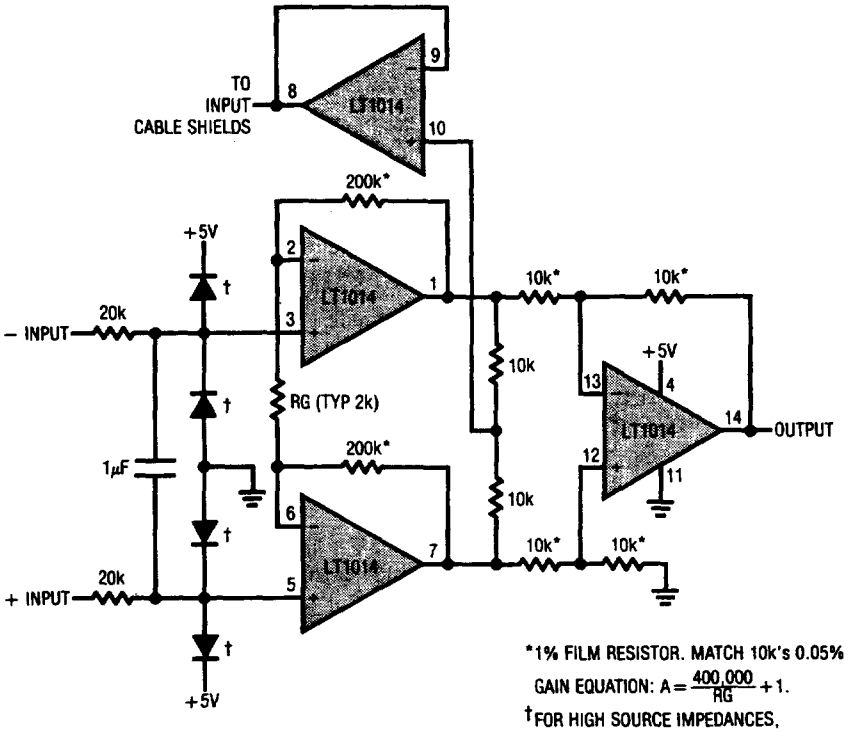




*1% FILM RESISTOR.
**SUPPLIED WITH YSI THERMISTOR NETWORK.
T1, T2 YSI THERMISTOR NETWORK = #44201.
FLOW IN PIPE IS INVERSELY PROPORTIONAL TO RESISTANCE OF T1–T2 TEMPERATURE DIFFERENCE.
A1–A2 PROVIDE GAIN. A3–A4 PROVIDE LINEARIZED FREQUENCY OUTPUT.

TYPICAL APPLICATIONS

5V Powered Precision Instrumentation Amplifier

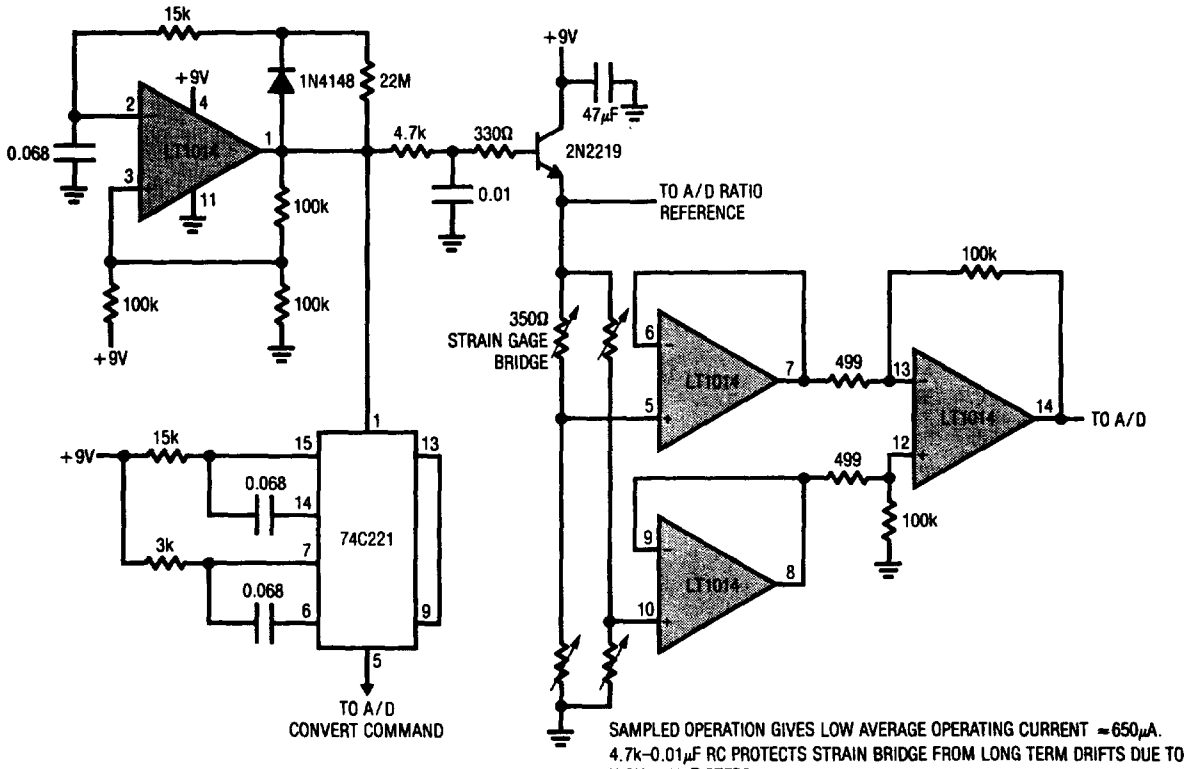


*1% FILM RESISTOR. MATCH 10k's 0.05%

GAIN EQUATION: $A = \frac{400,000}{RG} + 1$.

†FOR HIGH SOURCE IMPEDANCES, USE 2N2222 AS DIODES.

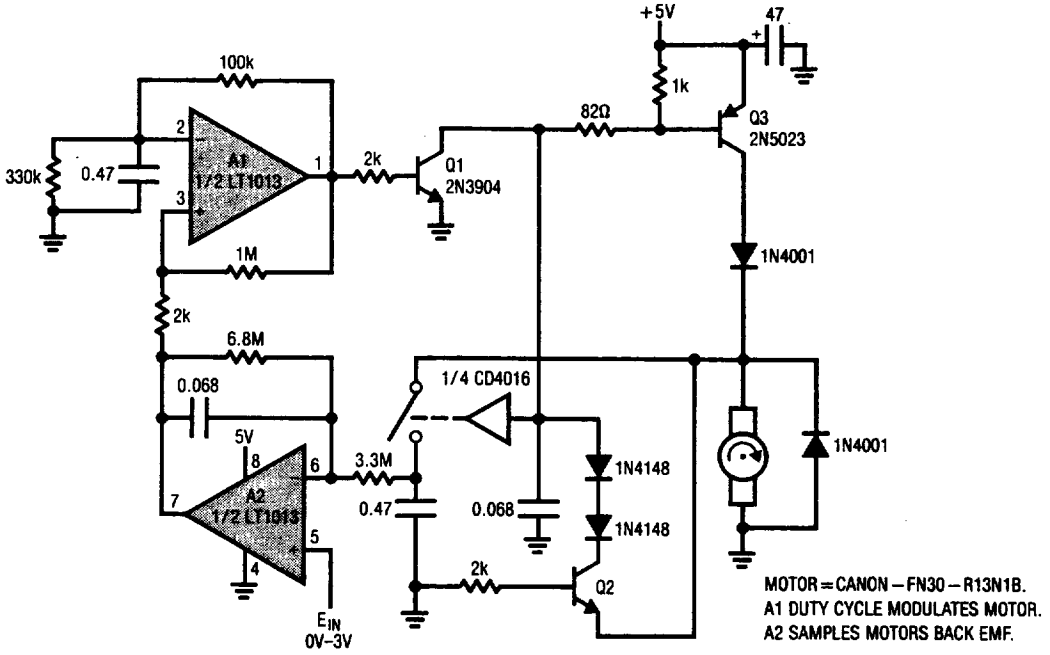
9V Battery Powered Strain Gage Signal Conditioner



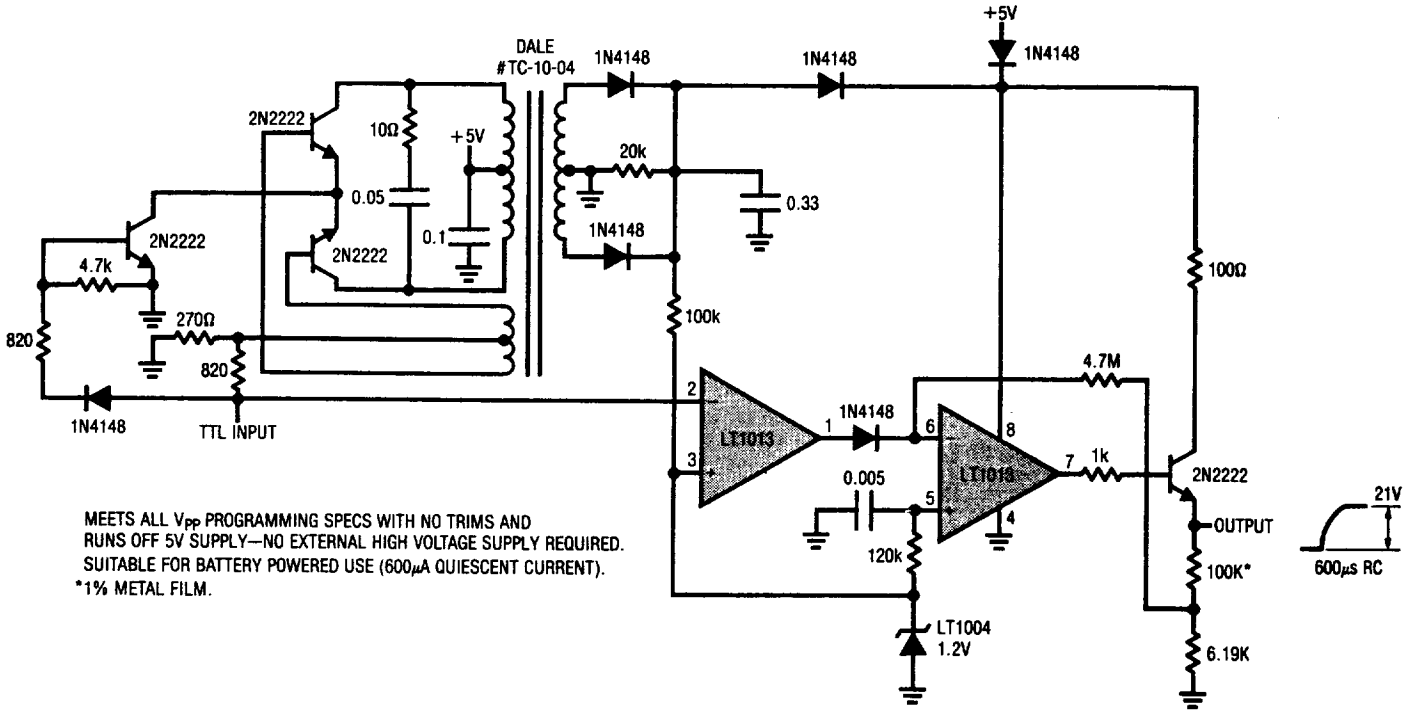
SAMPLED OPERATION GIVES LOW AVERAGE OPERATING CURRENT ≈650μA. 4.7k–0.01μF RC PROTECTS STRAIN BRIDGE FROM LONG TERM DRIFTS DUE TO HIGH ΔV/ΔT STEPS.

TYPICAL APPLICATIONS

5V Powered Motor Speed Controller
No Tachometer Required

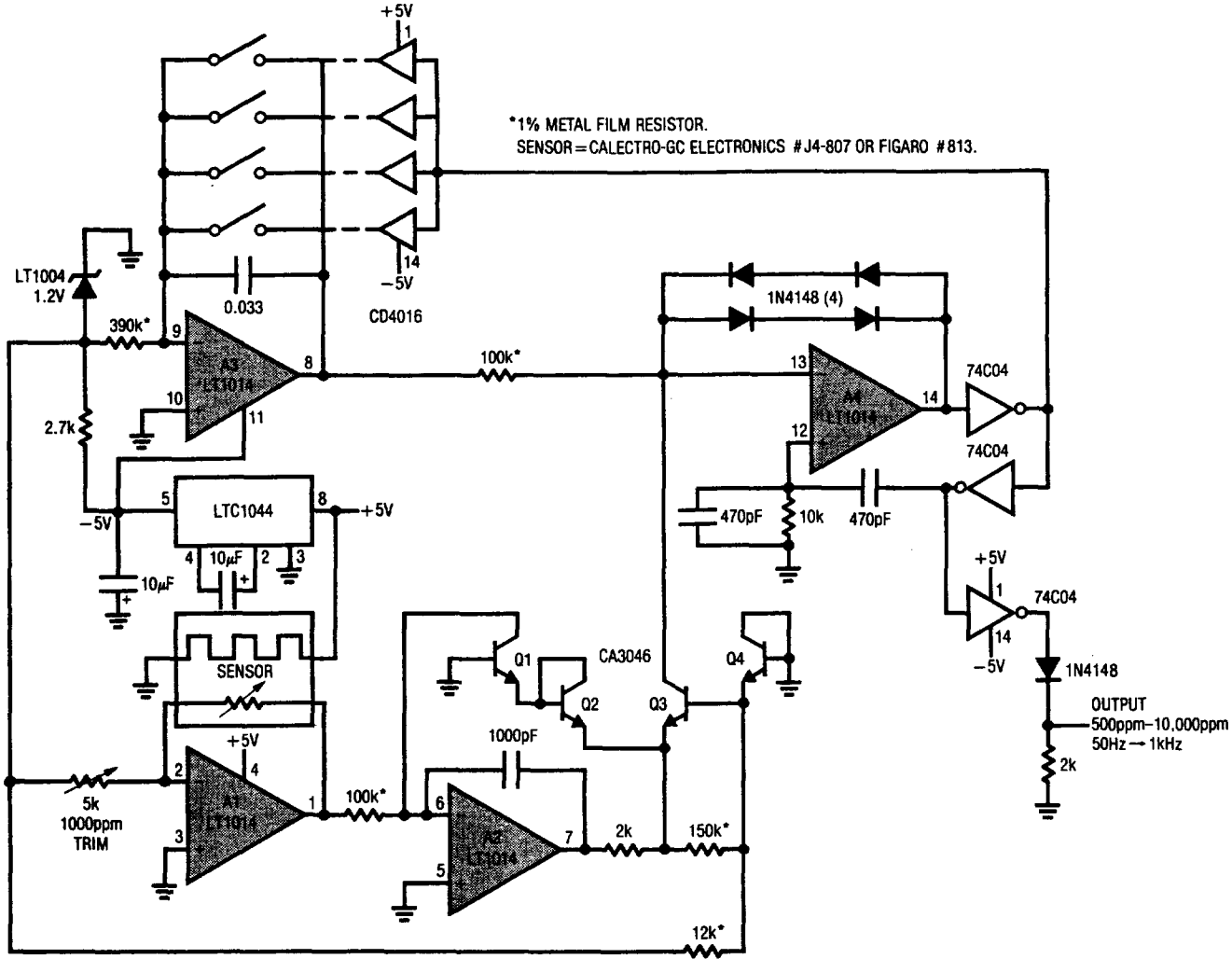


5V Powered EEPROM Pulse Generator

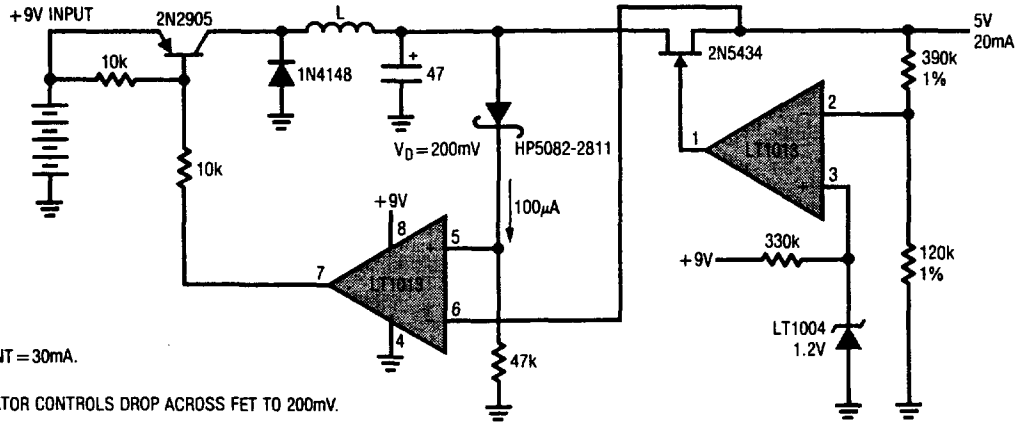


TYPICAL APPLICATIONS

Methane Concentration Detector with Linearized Output



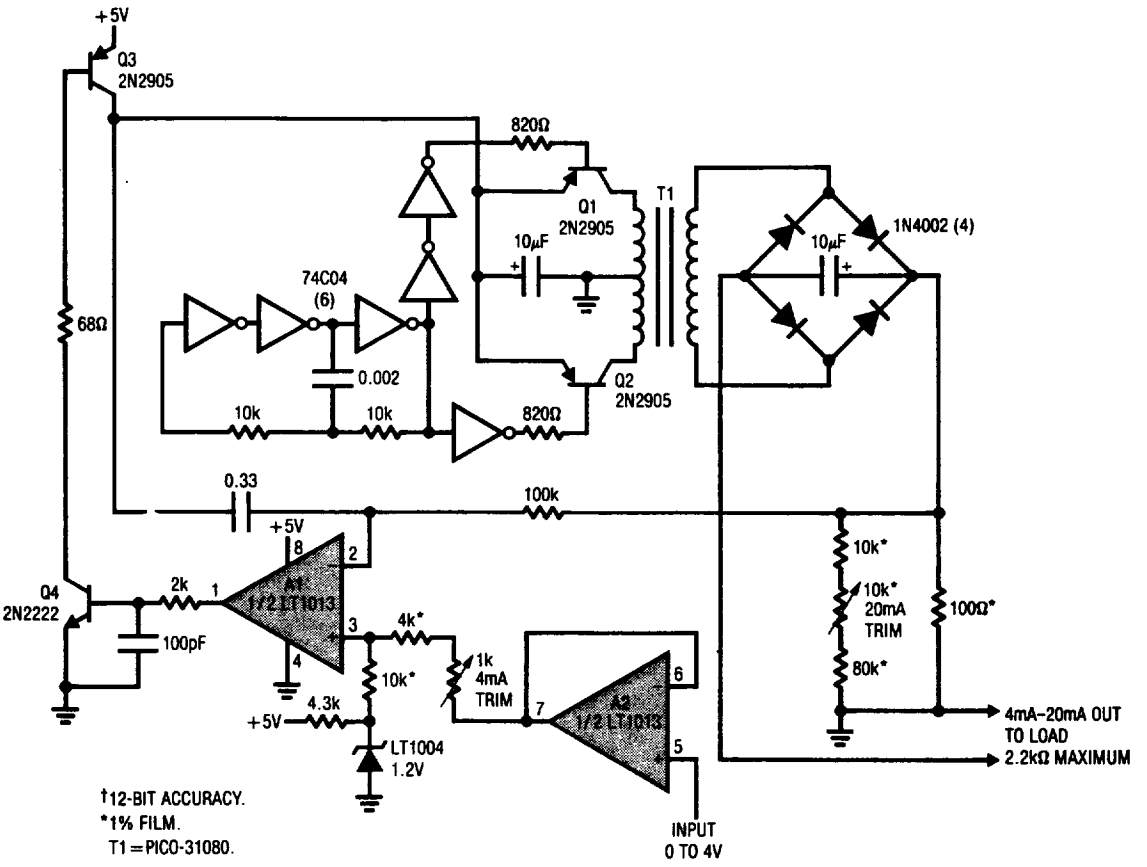
Low Power 9V to 5V Converter



L = DALE TE-3/Q3/TA.
SHORT CIRCUIT CURRENT = 30mA.
≈ 75% EFFICIENCY.
SWITCHING PREREGULATOR CONTROLS DROP ACROSS FET TO 200mV.

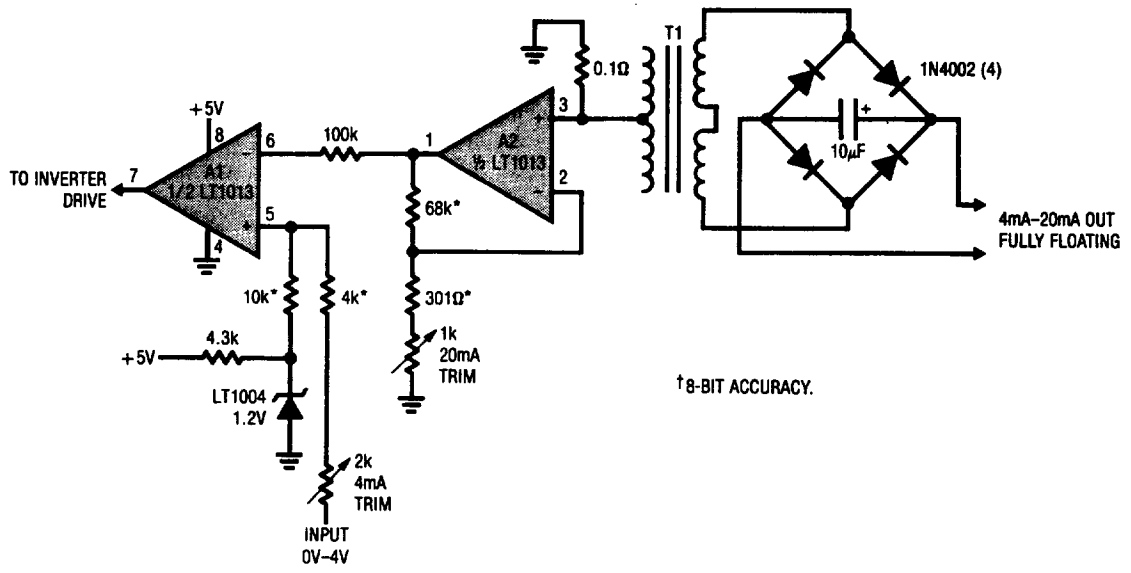
TYPICAL APPLICATIONS

5V Powered 4mA–20mA Current Loop Transmitter †



†12-BIT ACCURACY.
*1% FILM.
T1 = PICO-31080.

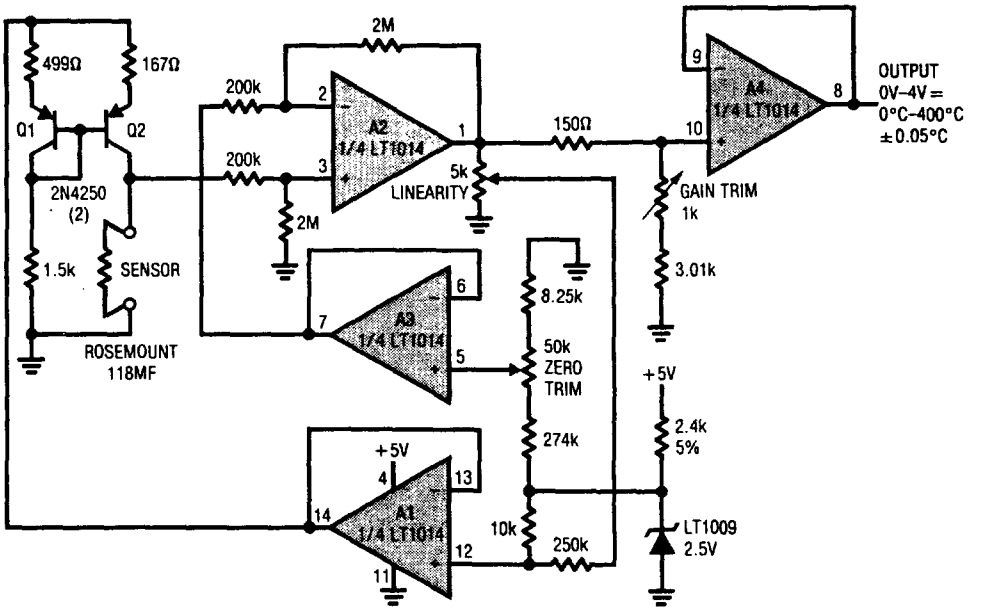
Fully Floating Modification to 4mA–20mA Current Loop †



†8-BIT ACCURACY.

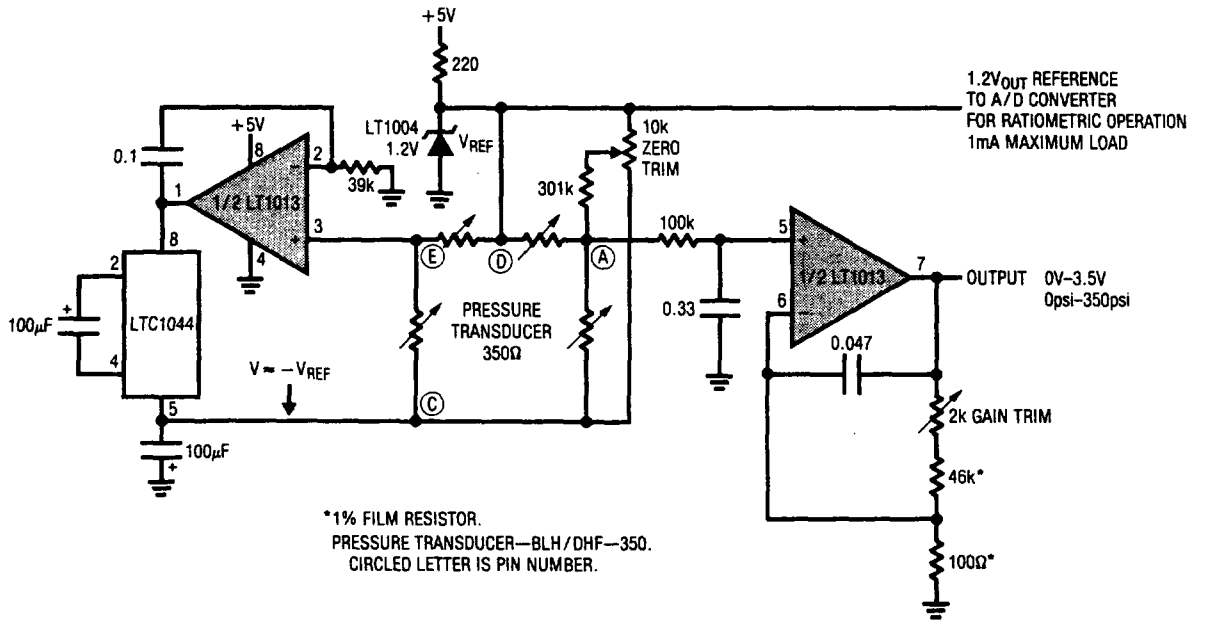
TYPICAL APPLICATIONS

5V Powered, Linearized Platinum RTD Signal Conditioner



ALL RESISTORS ARE TRW-MAR-6 METAL FILM.
RATIO MATCH 2M–200K ±0.01%.
TRIM SEQUENCE:
SET SENSOR TO 0° VALUE.
ADJUST ZERO FOR 0V OUT.
SET SENSOR TO 100°C VALUE.
ADJUST GAIN FOR 1.000V OUT.
SET SENSOR TO 400°C.
ADJUST LINEARITY FOR 4.000V OUT, REPEAT AS REQUIRED.

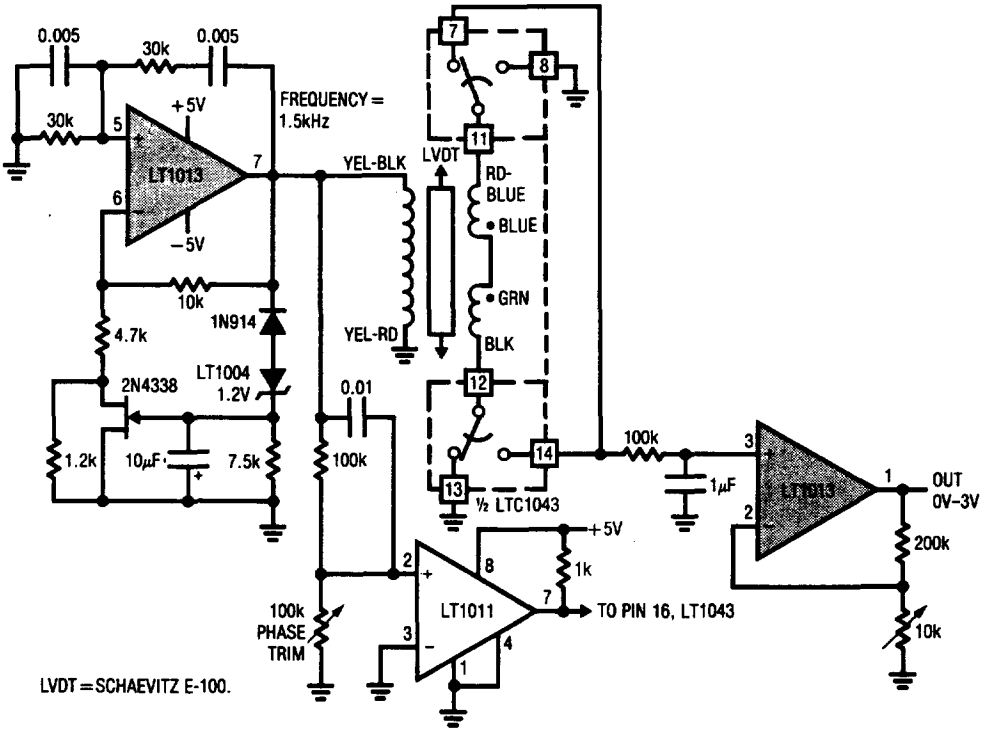
Strain Gage Bridge Signal Conditioner



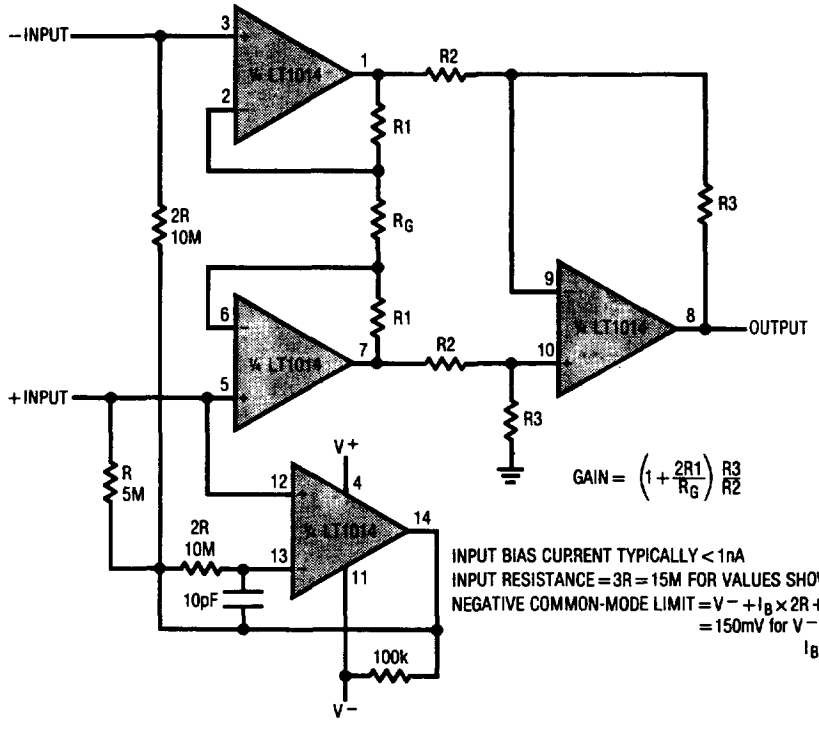
*1% FILM RESISTOR.
PRESSURE TRANSDUCER—BLH/DHF–350.
CIRCLED LETTER IS PIN NUMBER.

TYPICAL APPLICATIONS

LVDT Signal Conditioner

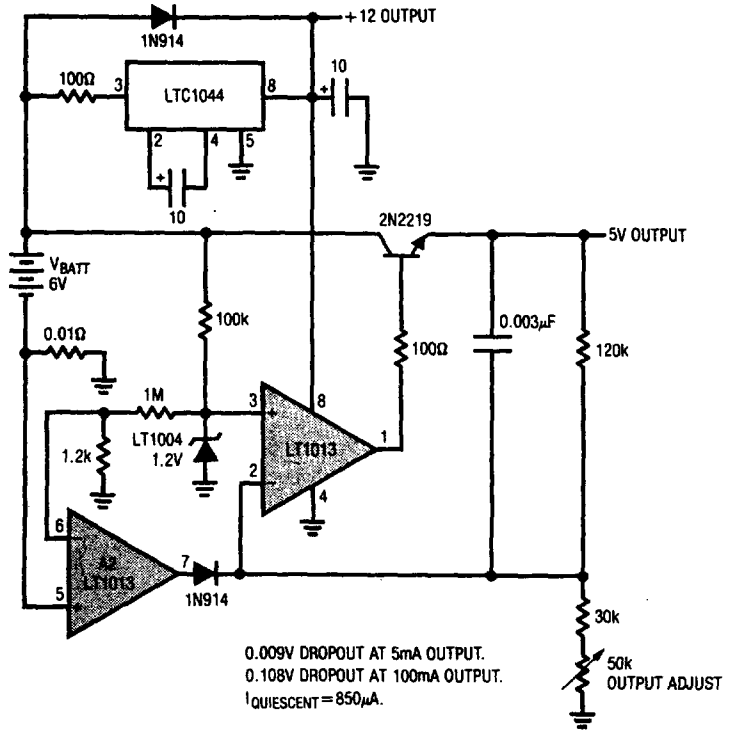


Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation



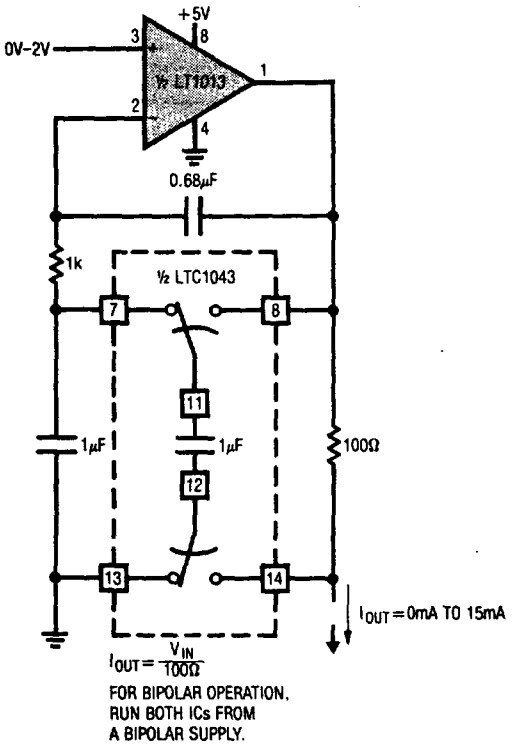
TYPICAL APPLICATIONS

Low Dropout Regulator for 6V Battery



0.009V DROPOUT AT 5mA OUTPUT.
0.108V DROPOUT AT 100mA OUTPUT.
$I_{QUIESCENT} = 850\mu A$.

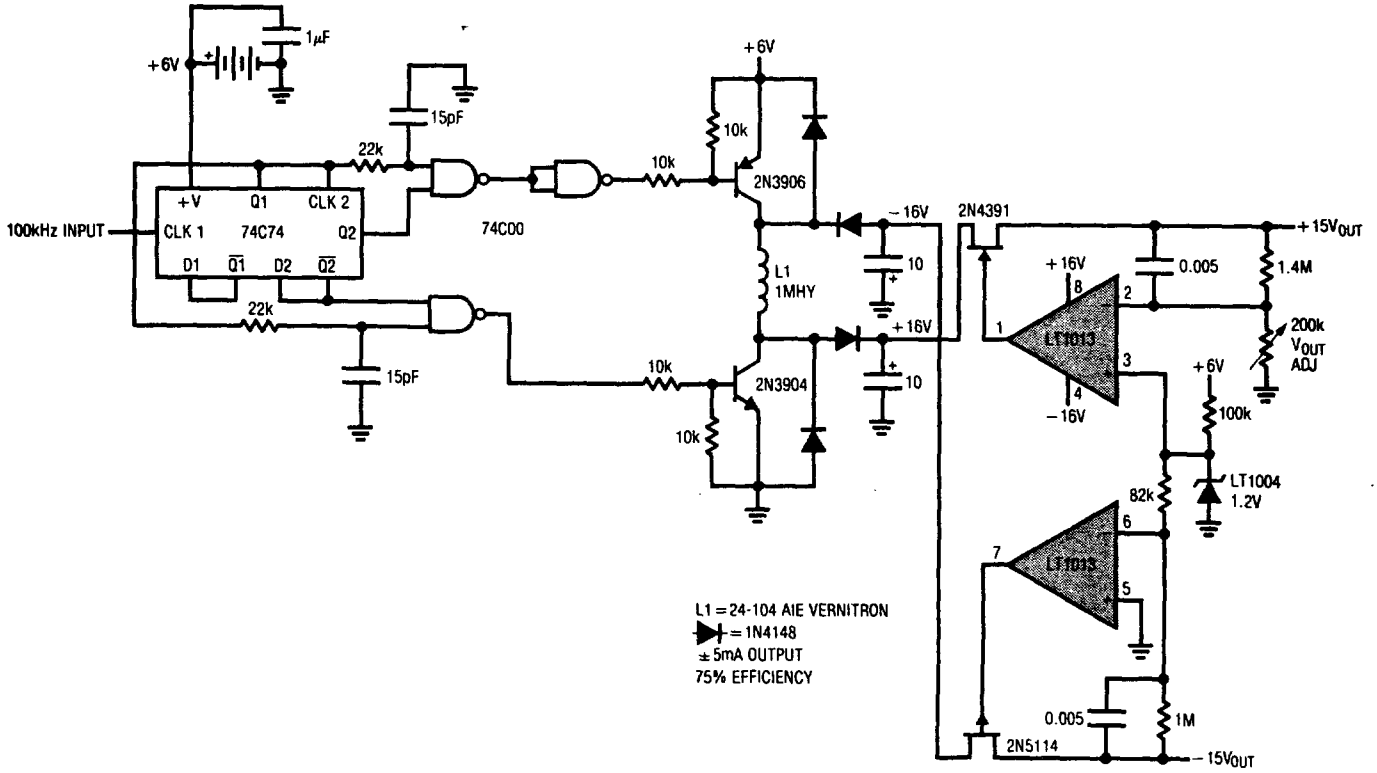
Voltage Controlled Current Source with Ground Referred Input and Output



$I_{OUT} = \frac{V_{IN}}{100\Omega}$

FOR BIPOLAR OPERATION, RUN BOTH ICs FROM A BIPOLAR SUPPLY.

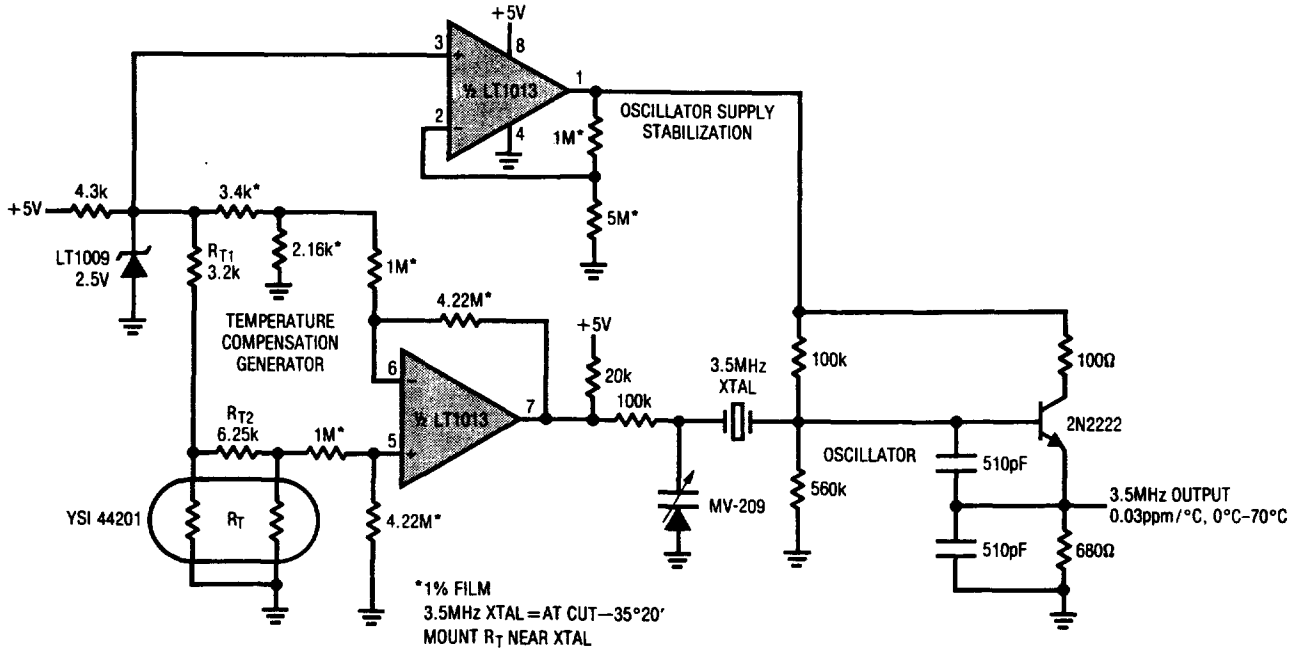
6V to ±15V Regulating Converter



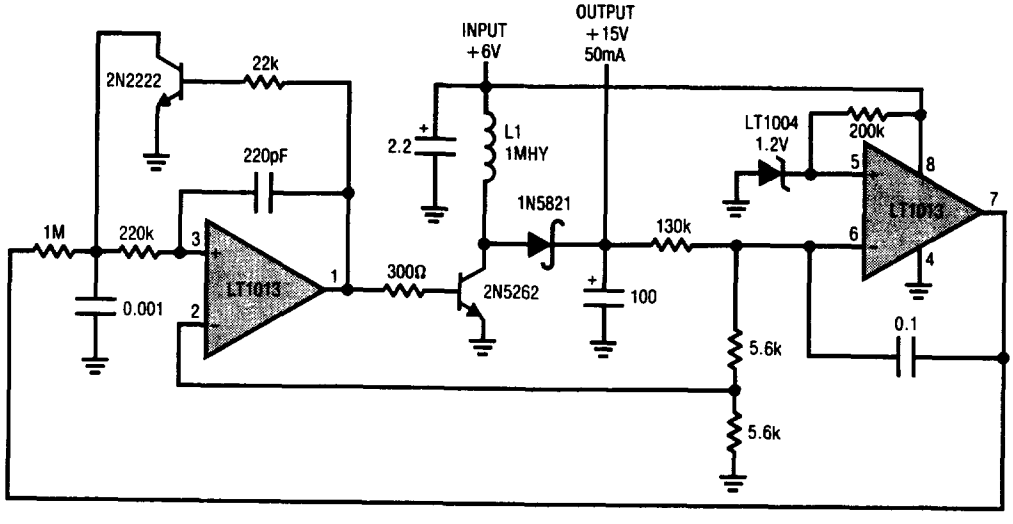
L1 = 24-104 AIE VERNITRON
▶|— = 1N4148
±5mA OUTPUT
75% EFFICIENCY

TYPICAL APPLICATIONS

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator (TXCO)†



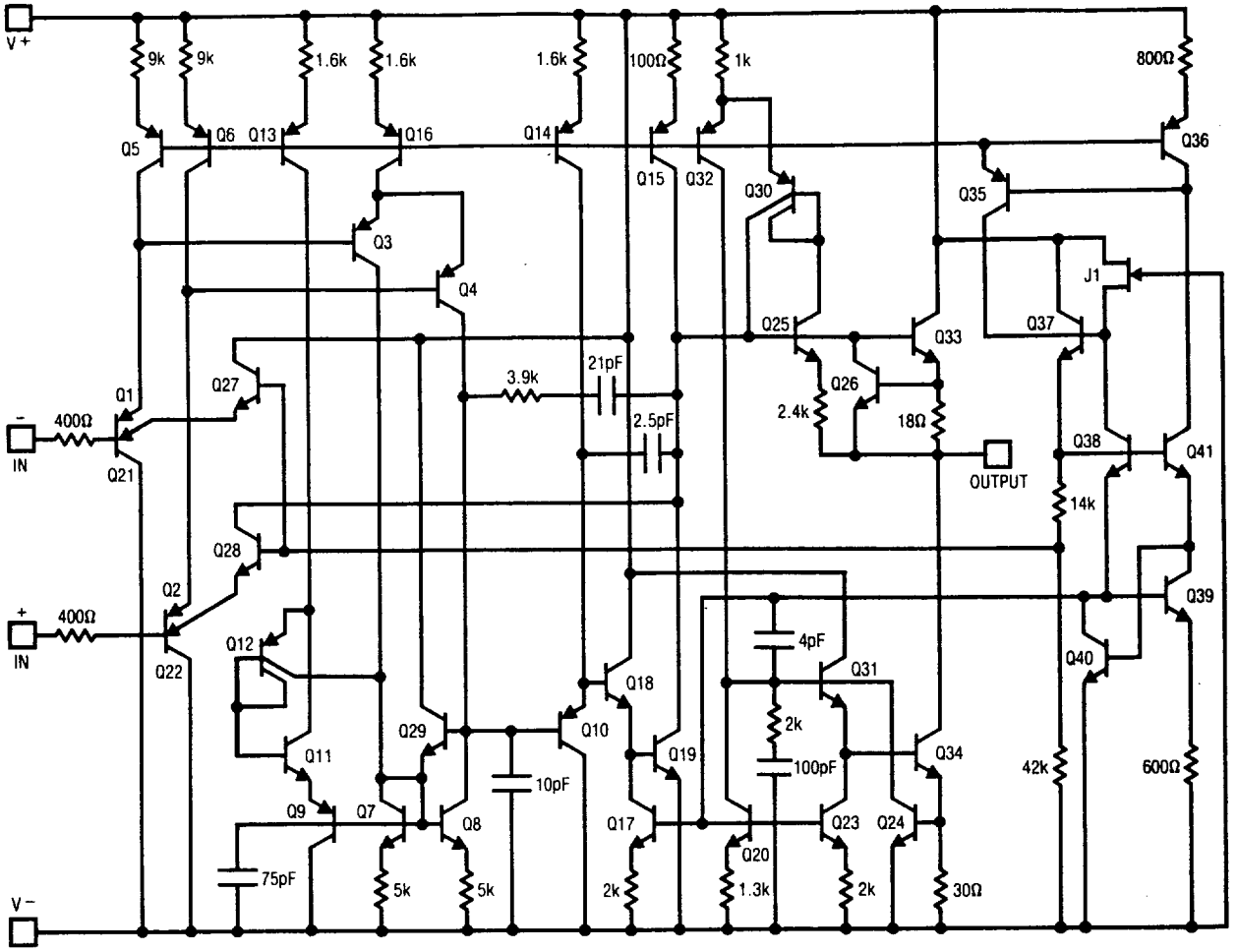
Step-Up Switching Regulator for 6V Battery



L1 = AIE—VERNITRON 24-104
78% EFFICIENCY

SCHEMATIC DIAGRAM

½ LT1013, ¼ LT1014



Precision, High Speed, JFET Input Operational Amplifiers

FEATURES

- *Guaranteed* Offset Voltage 150µV Max
  –55°C to 125°C 500µV Max
- *Guaranteed* Drift 4µV/°C Max
- *Guaranteed* Bias Current
  70°C 150pA Max
  125°C 2.5nA Max
- *Guaranteed* Slew Rate 12V/µs Min

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters
- Fast, Precision Sample-and-Hold

DESCRIPTION

The LT1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/µs slew rate and 6.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 50µV, 1.2µV/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

The 150µV maximum offset voltage specification is the best available on any JFET input operational amplifier.

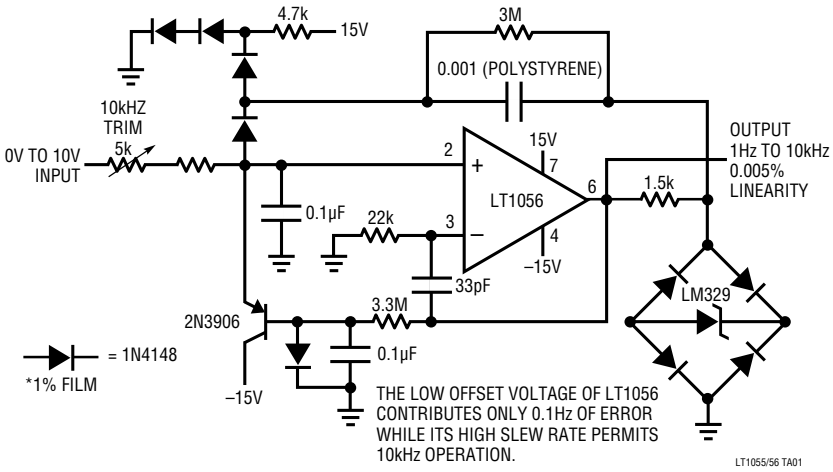
The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

The voltage-to-frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

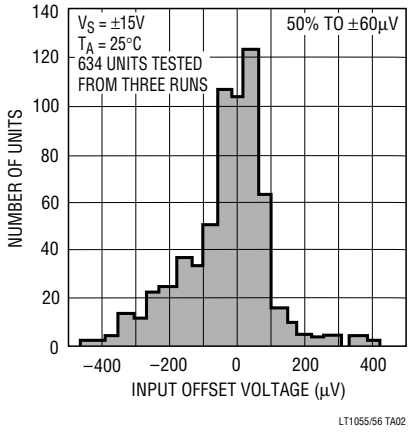
For a JFET input op amp with 23V/µs guaranteed slew rate, refer to the LT1022 data sheet.

TYPICAL APPLICATION

0kHz to 10kHz Voltage-to-Frequency Converter



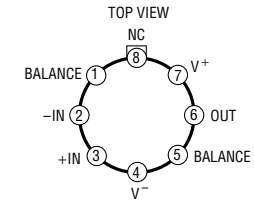
Distribution of Input Offset Voltage (H Package)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LT1055AM/LT1055M/LT1056AM/
LT1056M ..... –55°C to 125°C
LT1055AC/LT1055C/LT1056AC/
LT1056C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

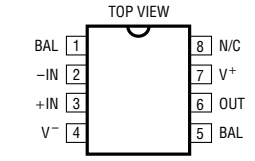
PACKAGE/ORDER INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN
T_{JMAX} = 150°C, θ_{JA} = 150°C/W, θ_{JC} = 45°C/W

ORDER PART NUMBER

LT1055ACH LT1056ACH
LT1055CH LT1056CH
LT1055AMH LT1056AMH
LT1055MH LT1056MH



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 100°C, θ_{JA} = 130°C/W

LT1055CN8
LT1056CN8

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/LT1056AM LT1055AC/LT1056AC MIN	TYP	MAX	LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note1)	LT1055 H Package	—	50	150	—	70	400	µV
		LT1056 H Package	—	50	180	—	70	450	µV
		LT1055 N8 Package	—	—	—	—	120	700	µV
		LT1056 N8 Package	—	—	—	—	140	800	µV
I_{OS}	Input Offset Current	Fully Warmed Up	—	2	10	—	2	20	pA
I_B	Input Bias Current	Fully Warmed Up	—	±10	±50	—	±10	±50	pA
		V_{CM} = 10V	—	30	130	—	30	150	pA
	Input Resistance: Differential		—	10^{12}	—	—	10^{12}	—	Ω
	Common Mode	V_{CM} = –11V to 8V	—	10^{12}	—	—	10^{12}	—	Ω
		V_{CM} = 8V to 11V	—	10^{11}	—	—	10^{11}	—	Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055	—	1.8	—	—	2.0	—	μV_{P-P}
		LT1056	—	2.5	—	—	2.8	—	μV_{P-P}
	Input Noise Voltage Density	f_0 = 10Hz (Note 2)	—	28	50	—	30	60	$nV/\sqrt{Hz}$
		f_0 = 1kHz (Note 3)	—	14	20	—	15	22	$nV/\sqrt{Hz}$
I_n	Input Noise Current Density	f_0 = 10Hz, 1kHz (Note 4)	—	1.8	4	—	1.8	4	$fA/\sqrt{Hz}$
A_{VOL}	Large-Signal Voltage Gain	V_0 = ±10V R_L = 2k	150	400	—	120	400	—	V/mV
		R_L = 1k	130	300	—	100	300	—	V/mV
	Input Voltage Range		±11	±12	—	±11	±12	—	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±11V	86	100	—	83	98	—	dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V	90	106	—	88	104	—	dB
V_{OUT}	Output Voltage Swing	R_L = 2k	±12	±13.2	—	±12	±13.2	—	V
SR	Slew Rate	LT1055	10	13	—	7.5	12	—	V/µs
		LT1056	12	16	—	9.0	14	—	V/µs
GBW	Gain-Bandwidth Product	f = 1MHz LT1055	—	5.0	—	—	4.5	—	MHz
		LT1056	—	6.5	—	—	5.5	—	MHz
I_S	Supply Current	LT1055	—	2.8	4.0	—	2.8	4.0	mA
		LT1056	—	5.0	6.5	—	5.0	7.0	mA
	Offset Voltage Adjustment Range	R_{POT} = 100k	—	±5	—	—	±5	—	mV

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AC LT1056AC MIN	LT1055AC LT1056AC TYP	LT1055AC LT1056AC MAX	LT1055CH/LT1056CH LT1055CN8/LT1056CN8 MIN	LT1055CH/LT1056CH LT1055CN8/LT1056CN8 TYP	LT1055CH/LT1056CH LT1055CN8/LT1056CN8 MAX	UNITS
V_{OS}	Input Offset Voltage (Note1)	LT1055 H Package	●	—	100	330	—	140	750	µV
		LT1056 H Package	●	—	100	360	—	140	800	µV
		LT1055 N8 Package	●	—	—	—	—	250	1250	µV
		LT1056 N8 Package	●	—	—	—	—	280	1350	µV
	Average Temperature Coefficient of Input Offset Voltage	H Package (Note 5)	●	—	1.2	4.0	—	1.6	8.0	µV/°C
		N8 Package (Note 5)	●	—	—	—	—	3.0	12.0	µV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	10	50	—	16	80	pA
		$T_A = 70°C$ LT1056	●	—	14	70	—	18	100	pA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±30	±150	—	±40	±200	pA
		$T_A = 70°C$ LT1056	●	—	±40	±80	—	±50	±240	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	80	250	—	60	250	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{Cm} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	89	105	—	87	103	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.1	—	±12	±13.1	—	V

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AM LT1056AM MIN	LT1055AM LT1056AM TYP	LT1055AM LT1056AM MAX	LT1055M LT1056M MIN	LT1055M LT1056M TYP	LT1055M LT1056M MAX	UNITS
V_{OS}	Input Offset Voltage (Note1)	LT1055	●	—	180	500	—	250	1200	µV
		LT1056	●	—	180	550	—	250	1250	µV
	Average Temperature Coefficient of Input Offset Voltage	(Note 5)	●	—	1.3	4.0	—	1.8	8.0	µV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	0.20	1.2	—	0.25	1.8	nA
		$T_A = 125°C$ LT1056	●	—	0.25	1.5	—	0.30	2.4	nA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±0.4	±2.5	—	±0.5	±4.0	nA
		$T_A = 125°C$ LT1056	●	—	±0.5	±3.0	—	±0.6	±5.0	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120	—	35	120	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.9	—	±12	±12.9	—	V

The ● denotes specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25°C$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

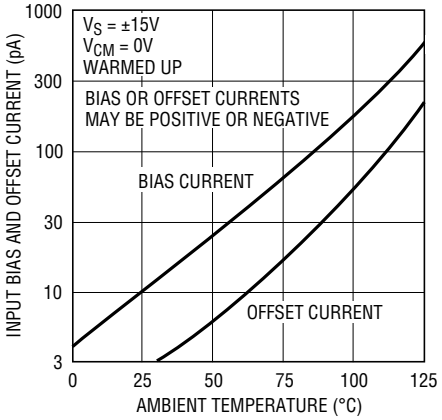
Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

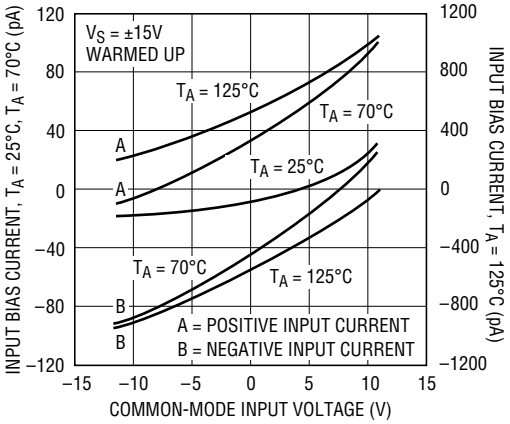
Note 5: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+. Devices tested to tighter drift specifications are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

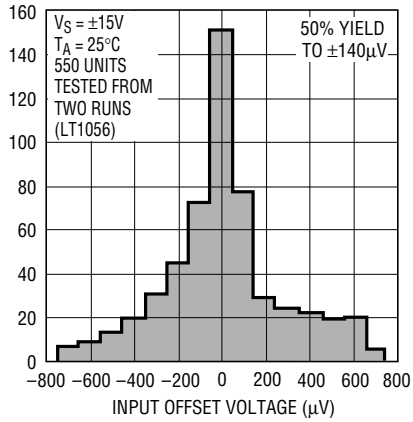
Input Bias and Offset Currents vs Temperature



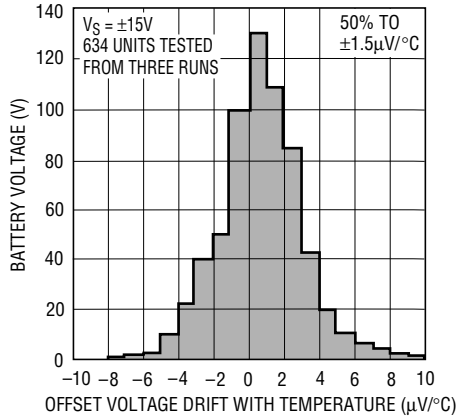
Input Bias Current Over the Common-Mode Range



Distribution of Input Offset Voltage (N8 Package)

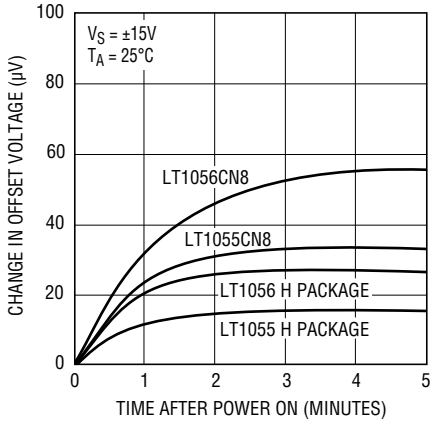


Distribution of Offset Voltage Drift with Temperature (H Package)*

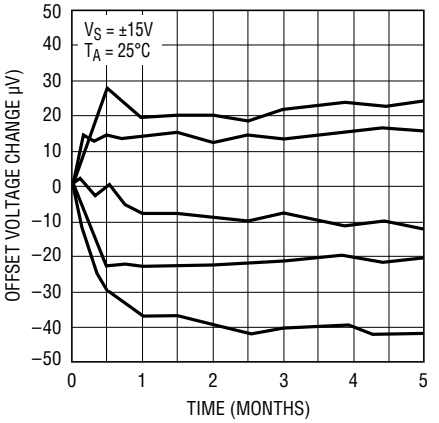


*DISTRIBUTION IN THE PLASTIC (N8) PACKAGE IS SIGNIFICANTLY WIDER.

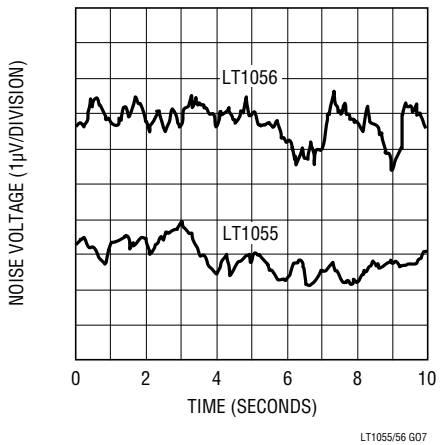
Warm-Up Drift



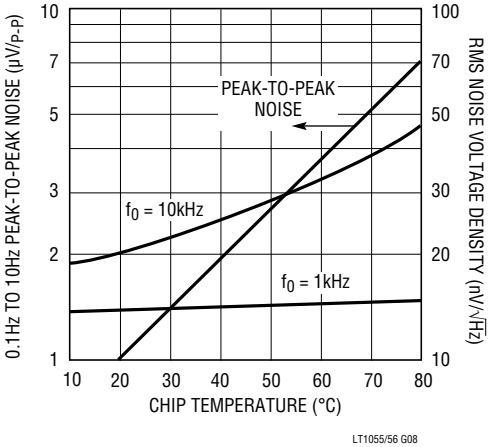
Long Term Drift of Representative Units



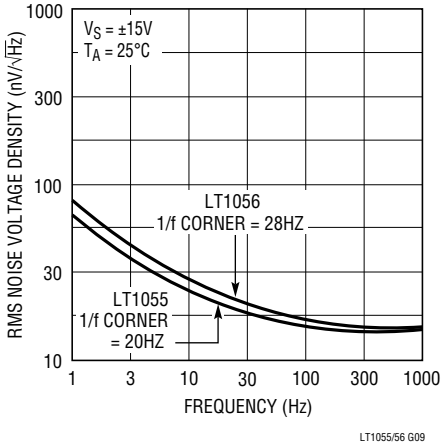
0.1Hz to 10Hz Noise



Noise vs Chip Temperature

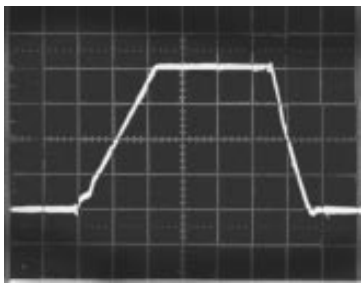


Voltage Noise vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

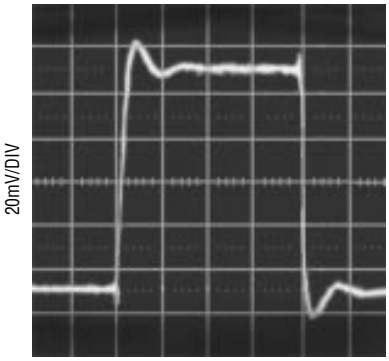
LT1056 Large-Signal Response



A_V = 1, C_L = 100pF, 0.5µs/DIV

LT1055/56 G10

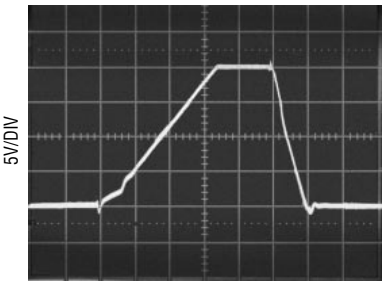
Small-Signal Response



A_V = 1, C_L = 100pF, 0.2µs/DIV

LT1055/56 G11

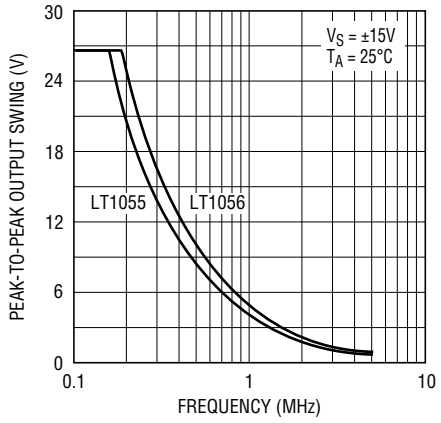
LT1055 Large-Signal Response



A_V = 1, C_L = 100pF, 0.5µs/DIV

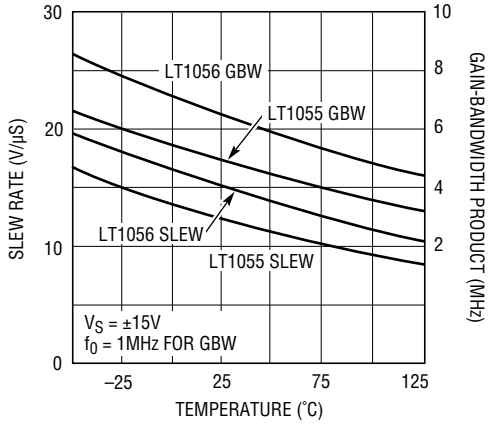
LT1055/56 G12

Undistorted Output Swing vs Frequency



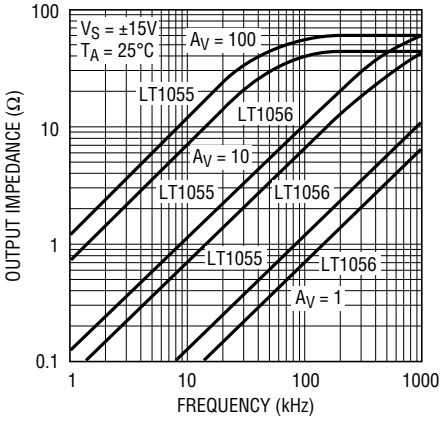
LT1055/56 G13

Slew Rate, Gain-Bandwidth vs Temperature



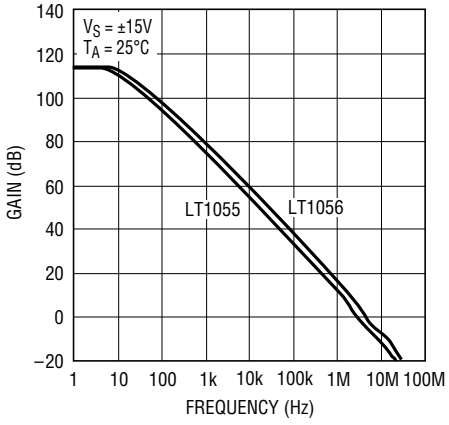
LT1055/56 G14

Output Impedence vs Frequency



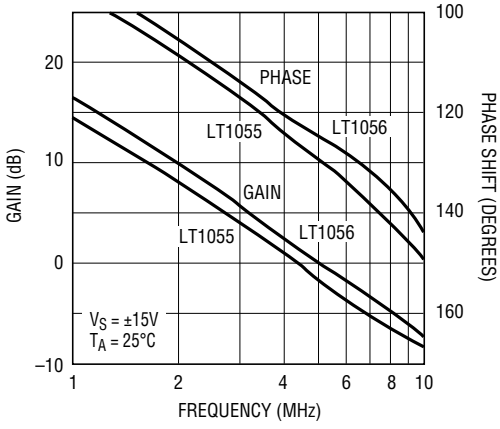
LT1055/56 G15

Gain vs Frequency



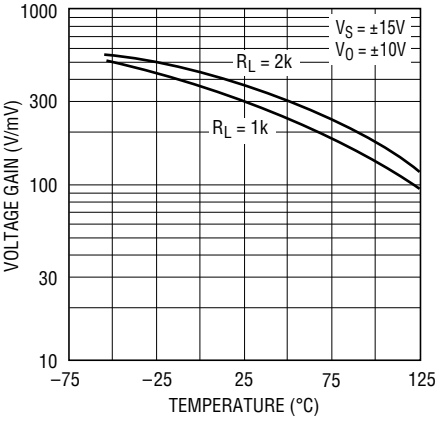
LT1055/56 G16

Gain, Phase Shift vs Frequency



LT1055/56 G17

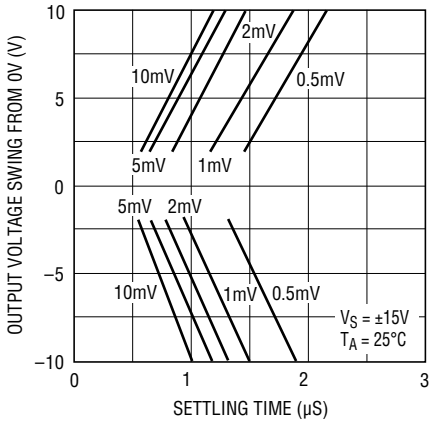
Voltage Gain vs Temperature



LT1055/56 G18

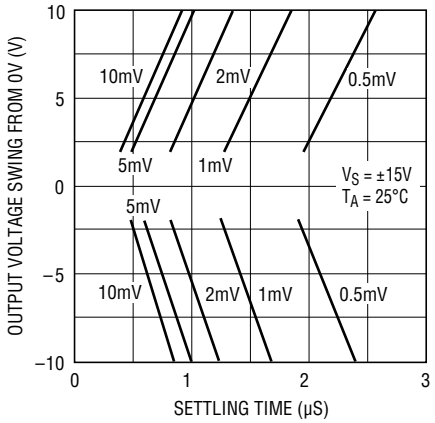
TYPICAL PERFORMANCE CHARACTERISTICS

LT1055 Settling Time



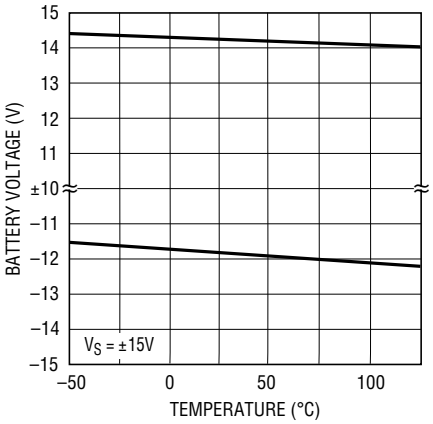
LT1055/56 G19

LT1056 Settling Time



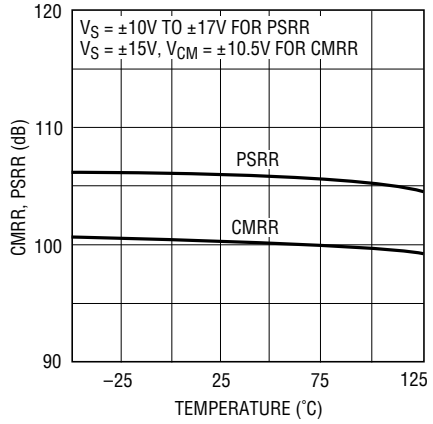
LT1055/56 G20

Common-Mode Range vs Temperature



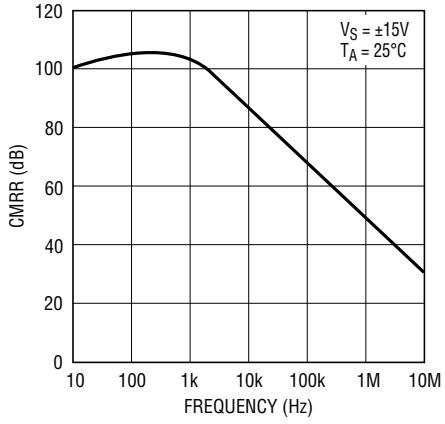
LT1055/56 G21

Common-Mode and Power Supply Rejections vs Temperature



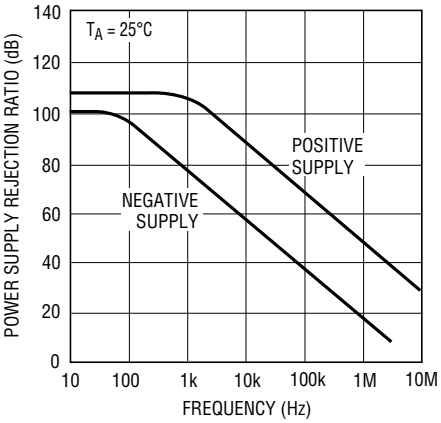
LT1055/56 G22

Common-Mode Rejection Ratio vs Frequency



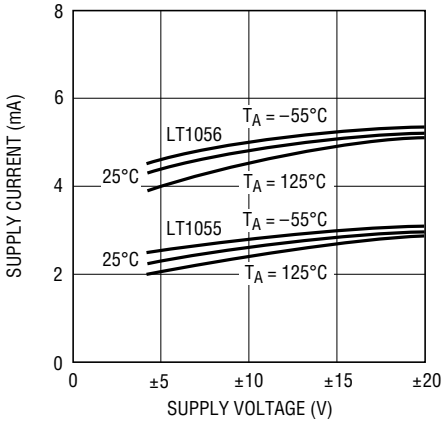
LT1055/56 G23

Power Supply Rejection Ratio vs Frequency



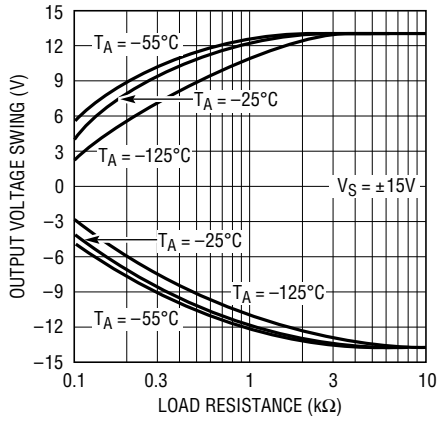
LT1055/56 G24

Supply Current vs Supply Voltage



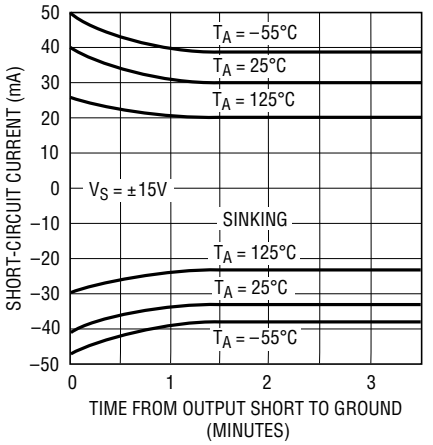
LT1055/56 G25

Output Swing vs Load Resistance



LT1055/56 G26

Short-Circuit Current vs Time

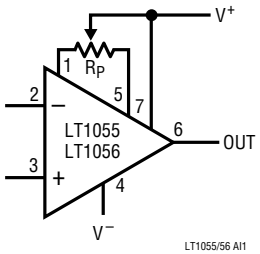


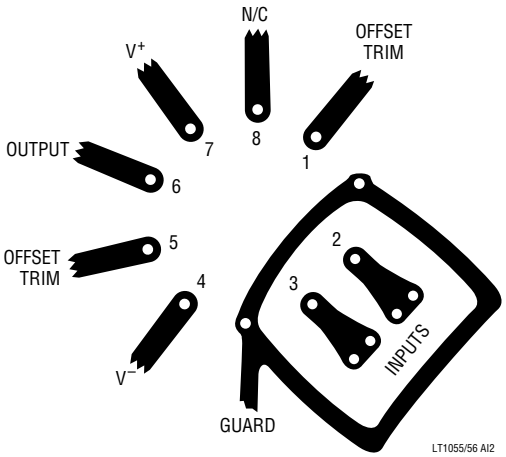
LT1055/56 G27

APPLICATIONS INFORMATION

The LT1055/LT1056 may be inserted directly into LF155A/LT355A, LF156A/LT356A, OP-15 and OP-16 sockets. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.

Offset Nulling





No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_P, ranging from 10k to 200k.

The LT1055/LT1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling cicuitry is removed. Because of the LT1055/LT1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/LT1056 proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in noninverting connnections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Teflon is a trademark of Dupont.

The LT1055/LT1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 20μV hysteresis (30μV on the M grades) when cycled over the –55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 10μV) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/LT1056 is practically immeasurable at $1.8fA/\sqrt{Hz}$. At 25°C it is negligible up to 1G of source resistance, R_S (compound to the noise of R_S). Even at 125°C it is negligible to 100M of R_S.

APPLICATIONS INFORMATION

The voltage noise spectrum is characterized by a low 1/f corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that with any JFET IC amplifier, the frequency location of the 1/f corner is proportional to the square root of the internal gate leakage currents and, therefore, noise doubles every 20°C. Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise (f_0 = 1kHz) is practically unaffected by temperature.

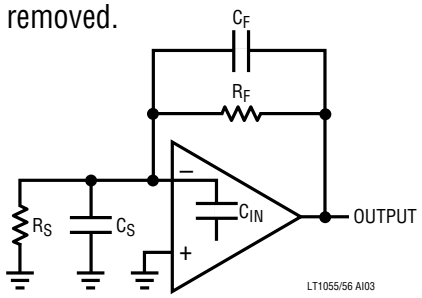
Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operating an LT1056 at ±5V supplies or with a 20°C/W case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically 2.5μV_{P-P} (±15V, free-air) to 1.5μV_{P-P}. Similiarly, the noise of an LT1055 will be 1.8μV_{P-P} typically because of its lower power dissipation and chip temperature.

High Speed Operation

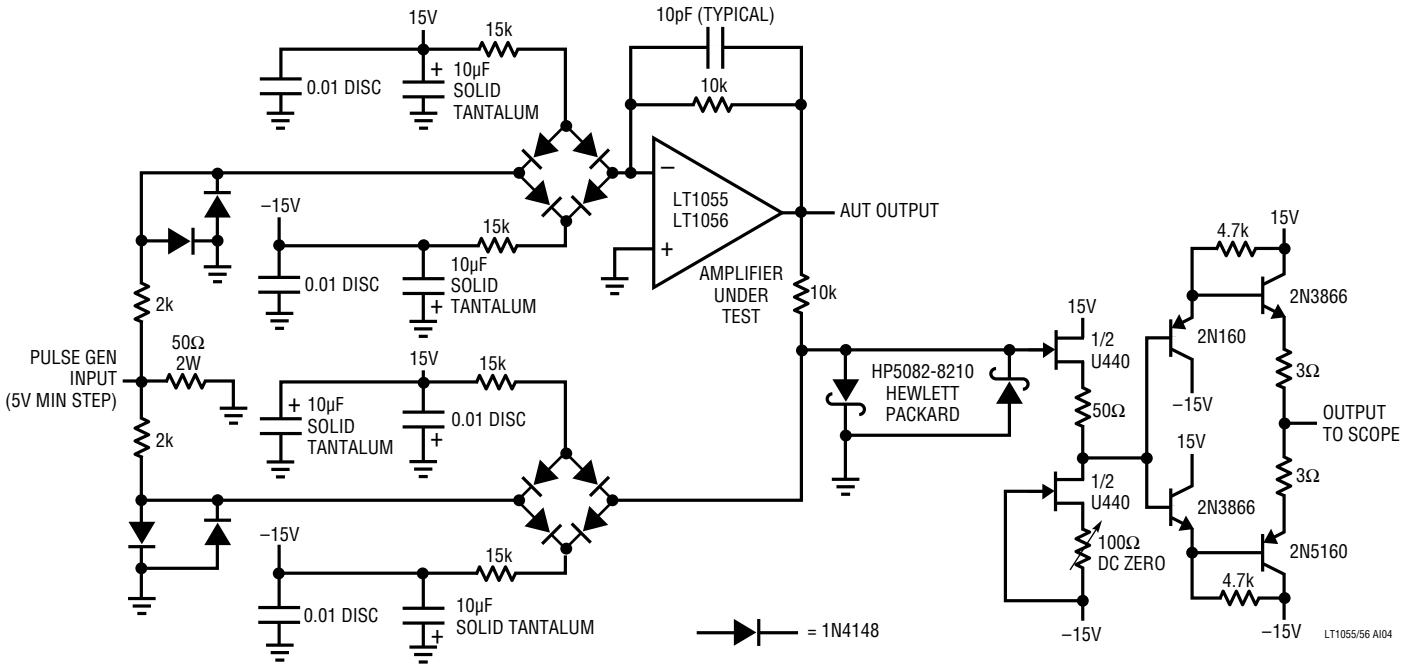
Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurments: (1) probe capacitance is isolated from the "false summing" node, and (2) it does not require a "flat top" input pulse since the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx$ 4pF). In low closed-loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With R_S (C_S + C_{IN}) = R_FC_F, the effect of the feedback pole is completely removed.



Settling Time Test Circuit

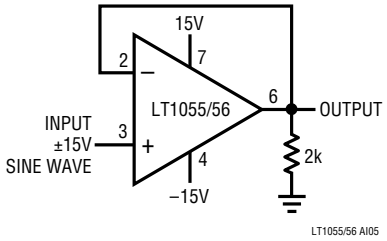


APPLICATIONS INFORMATION

Phase Reversal Protection

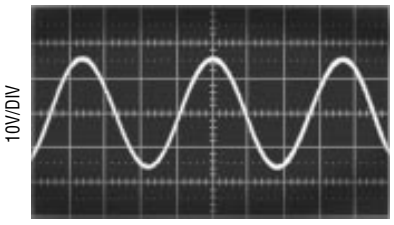
Most industry standard JFET input op amps (e.g., LF155/LF156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negitive common-mode limit at the input is exceeded (i.e., from –12V to –15V with ±15V supplies). This can cause lock-up in servo systems. As shown below, the LT1055/LT1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).

Voltage Follower with Input Exceeding the Negative Common-Mode Range



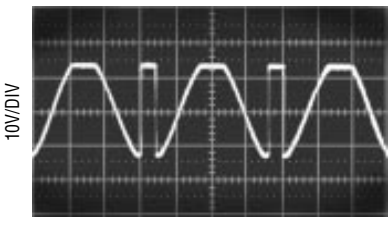
LT1055/56 AI05

Input



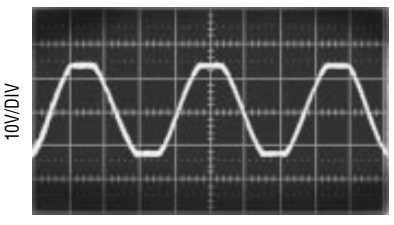
LT1055/56 AI06

Output (LF155/LF56, LF441, OP-15/OP-16)



LT1055/56 AI07

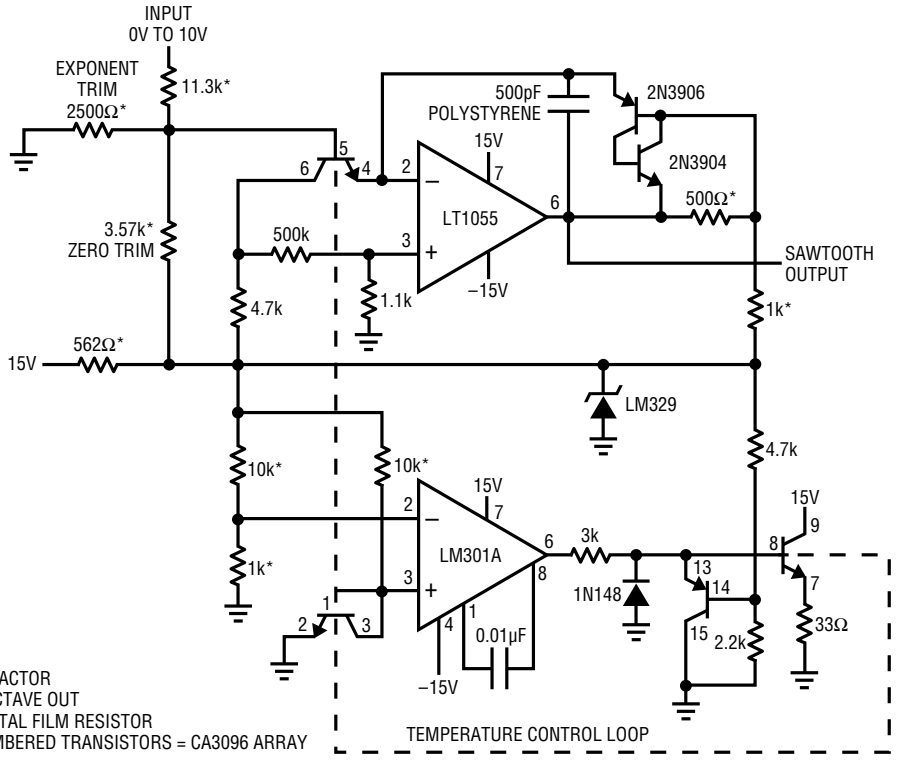
Output LT1055/LT1056



LT1055/56 AI08

TYPICAL APPLICATIONS †

Exponential Voltage-to-Frequency Converter for Music Synthesizers

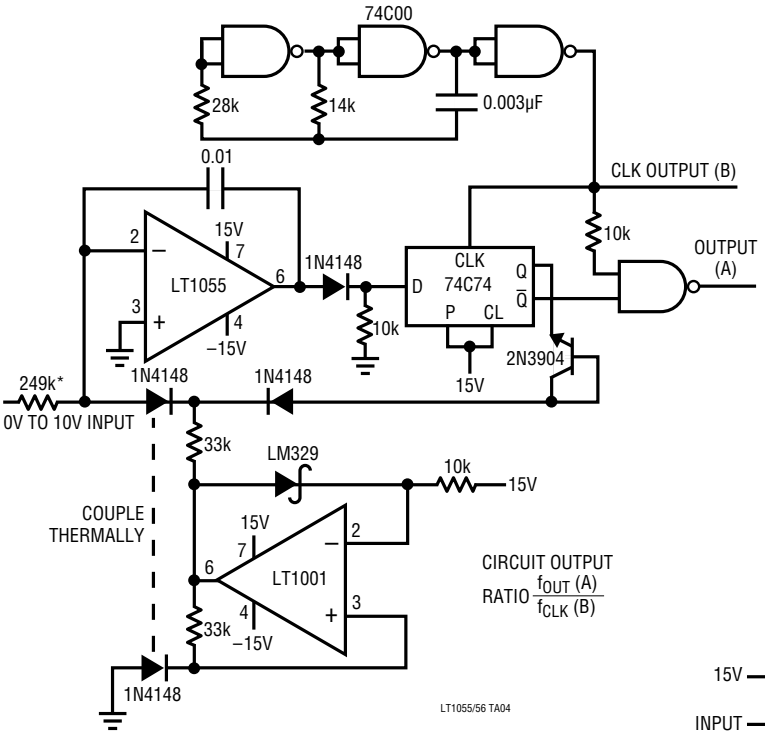


LT1055/56 TA03

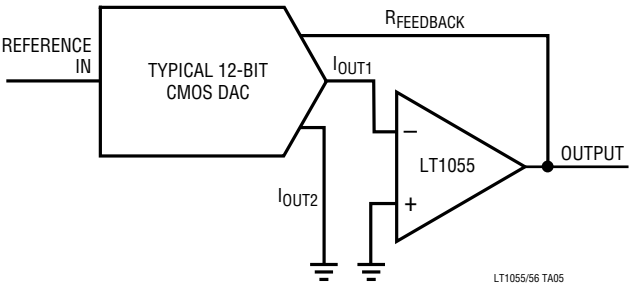
†For ten additional applications utilizing the LT1055 and LT1056, please see the LTC1043 data sheet and Application Note 3.

TYPICAL APPLICATIONS

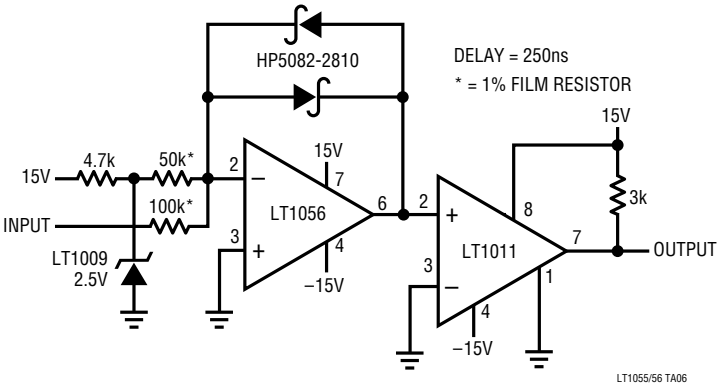
12-Bit Charge Balance A/D Converter



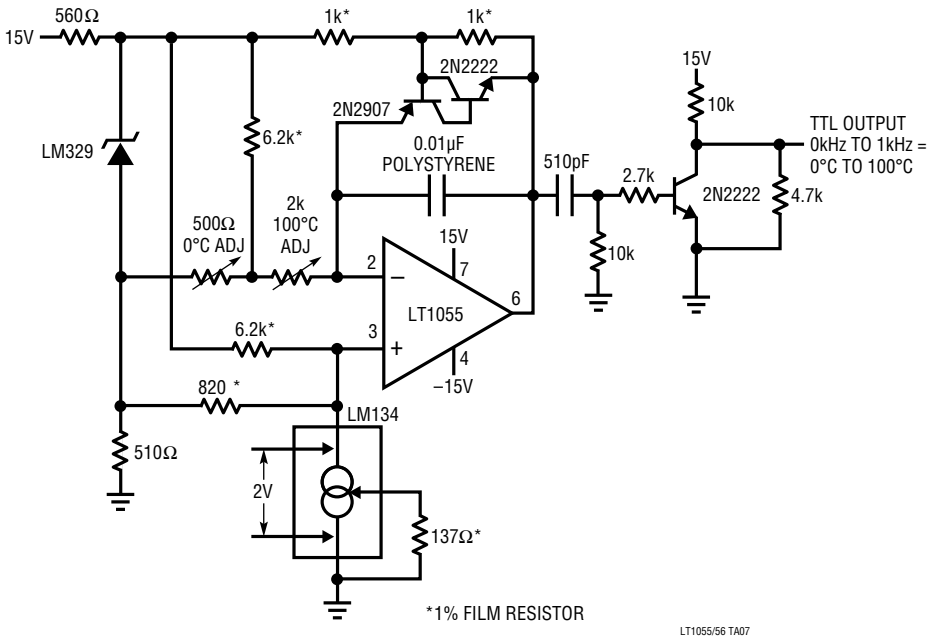
Fast "No Trims" 12-Bit Multiplying CMOS DAC Amplifier



Fast, 16-Bit Current Comparator

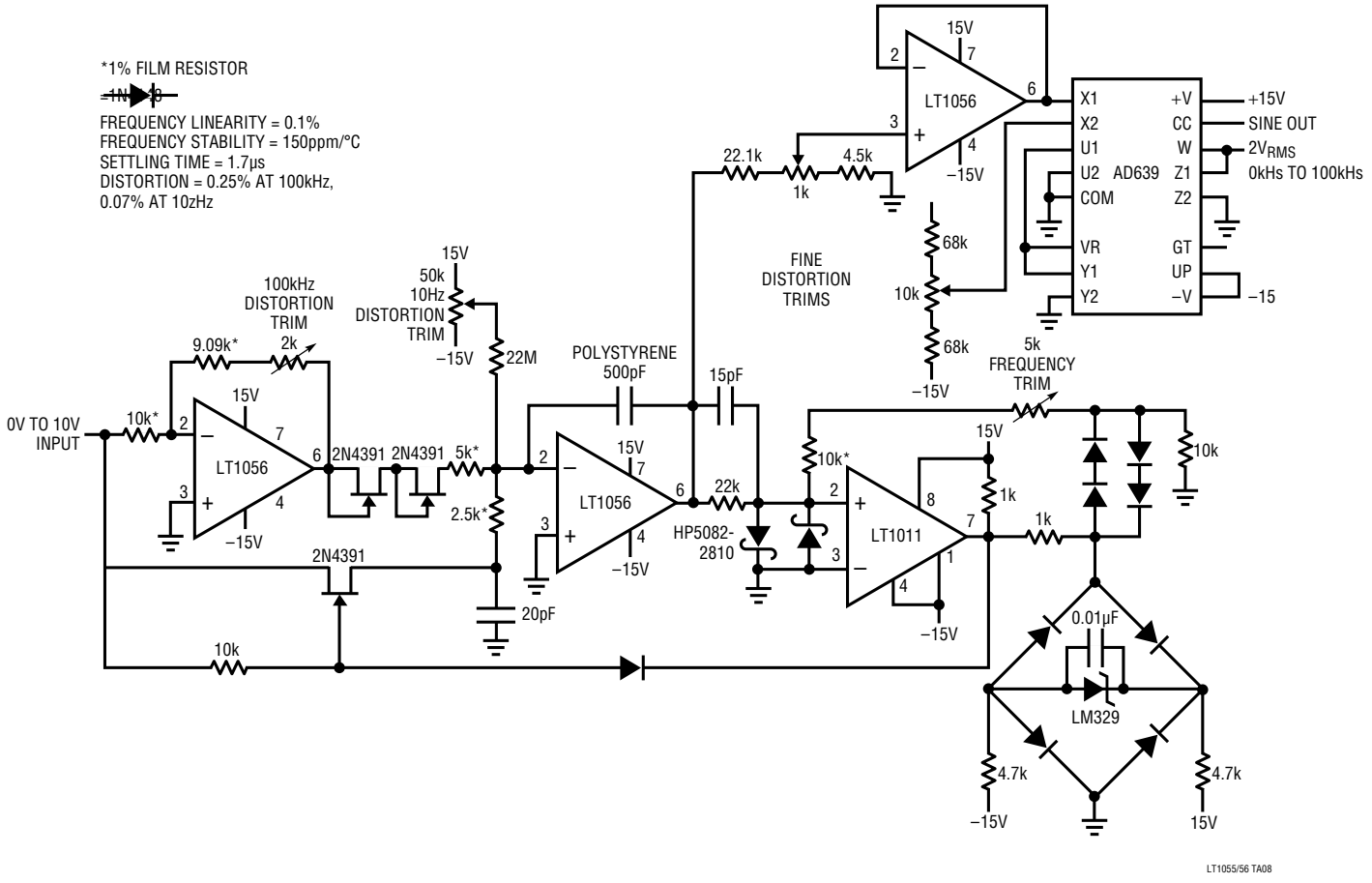


Temperature-to-Frequency Converter



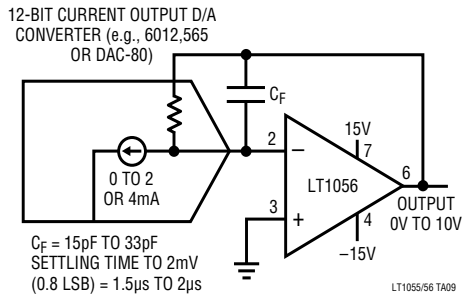
TYPICAL APPLICATIONS

100kHz Voltage Controlled Oscillator



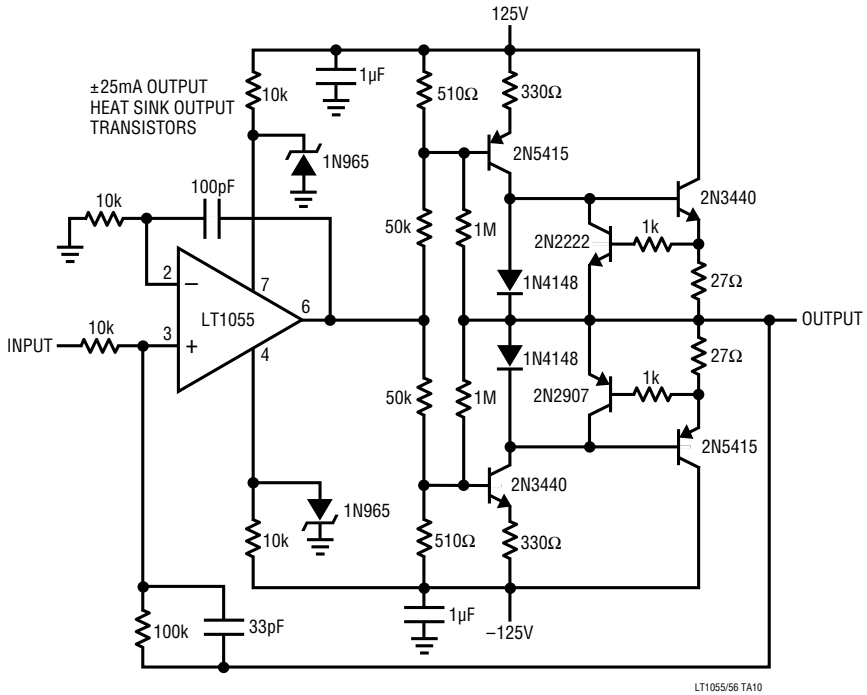
LT1055/56 TA08

12-Bit Voltage Output D/A Converter



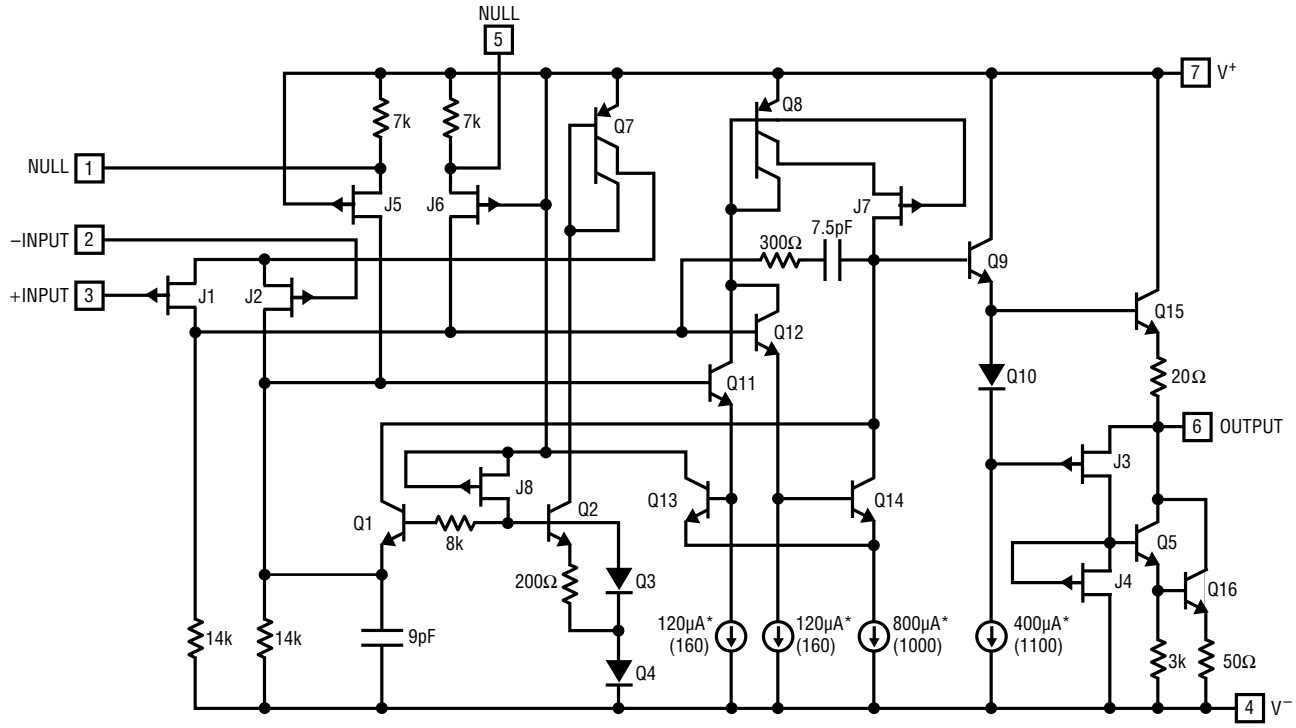
LT1055/56 TA09

±120V Output Precision Op Amp



LT1055/56 TA10

SIMPLIFIED SCHEMATIC



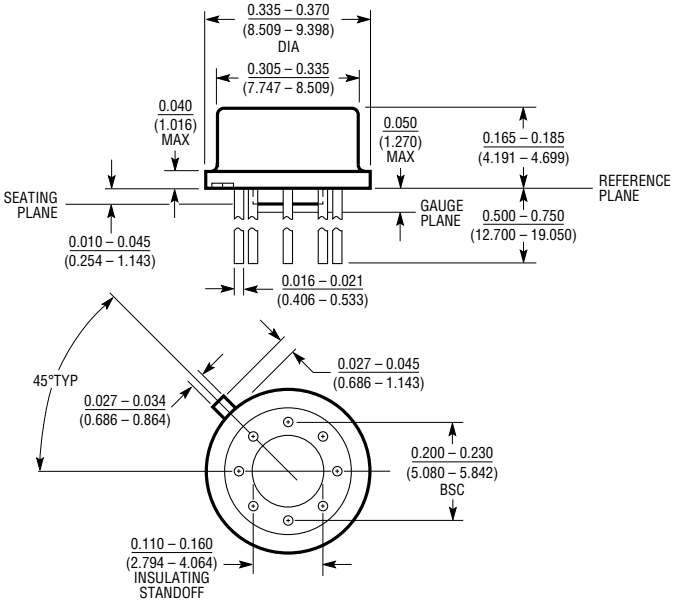
*CURRENTS AS SHOWN FOR LT1055. (X) = CURRENTS FOR LT1056.

LT1055/56 SCHM

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

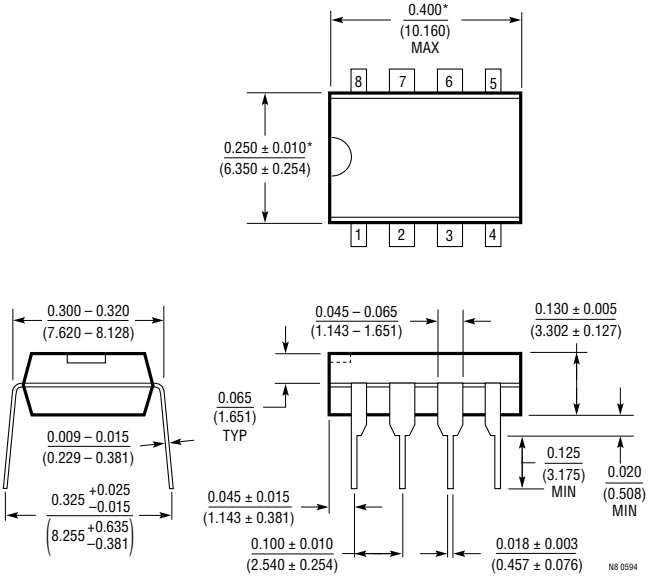
H Package Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

H8(5) 0592

N8 Package
8-Lead Plastic



N8 0594

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 0894 2K REV A • PRINTED IN USA

140MHz Video Current Feedback Amplifier

FEATURES

- **140MHz Bandwidth: A_V = 2, R_L = 150Ω**
- **1100V/μs Slew Rate**
- Low Cost
- 30mA Output Drive Current
- 0.01% Differential Gain
- 0.01° Differential Phase
- High Input Impedance: 14MΩ, 3pF
- Wide Supply Range: ±2V to ±15V
- Shutdown Mode: I_S < 250μA
- Low Supply Current: I_S = 10mA
- Inputs Common Mode to Within 1.5V of Supplies
- Outputs Swing Within 0.8V of Supplies

APPLICATIONS

- Video Amplifiers
- Cable Drivers
- RGB Amplifiers
- Test Equipment Amplifiers
- 50Ω Buffers for Driving Mixers

DESCRIPTION

The LT1227 is a current feedback amplifier with wide bandwidth and excellent video characteristics. The low differential gain and phase, wide bandwidth, and 30mA output drive current make the LT1227 well suited to drive cables in video systems.

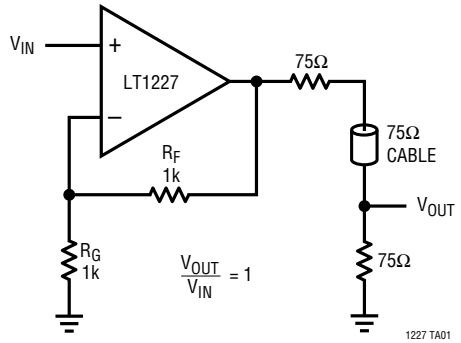
A shutdown feature switches the device into a high impedance, low current mode, allowing multiple devices to be connected in parallel and selected. Input to output isolation in shutdown is 70dB at 10MHz for input amplitudes up to $10V_{P-P}$. The shutdown pin interfaces to open collector or open drain logic and takes only 4μs to enable or disable.

The LT1227 comes in the industry standard pinout and can upgrade the performance of many older products. For a dual or quad version, see the LT1229/1230 data sheet.

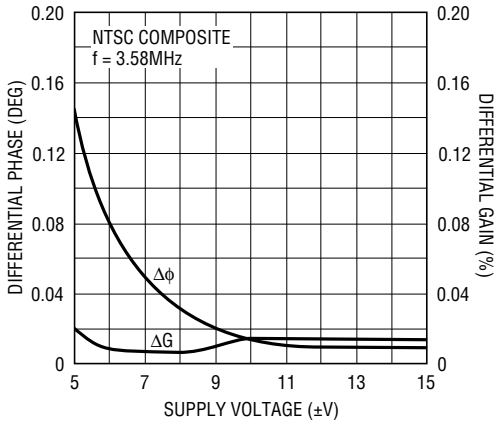
The LT1227 is manufactured on Linear Technology's proprietary complementary bipolar process.

TYPICAL APPLICATION

Video Cable Driver



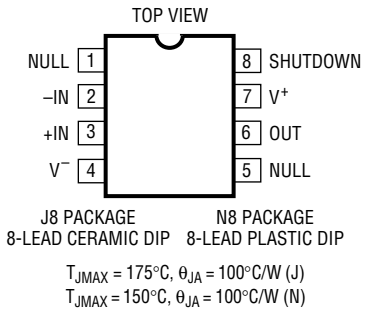
Differential Gain and Phase vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Input Current ..... ±15mA
Output Short Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1227C ..... 0°C to 70°C
LT1227M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature
Plastic Package ..... 150°C
Ceramic Package ..... 175°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



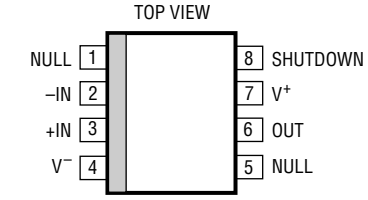
J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)

ORDER PART NUMBER

LT1227MJ8
LT1227CN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

LT1227CS8

S8 PART MARKING

1227

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			±3	±10	mV
			●			±15	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{IN+}	Noninverting Input Current	T_A = 25°C			±0.3	±3	µA
			●			±10	µA
$I_{IN–}$	Inverting Input Current	T_A = 25°C			±10	±60	µA
			●			±100	µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1k, R_G = 10Ω, R_S = 0Ω			3.2		nV/√Hz
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.7		pA/√Hz
$–i_n$	Inverting Input Noise Current Density	f = 1kHz			32		pA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±13V, V_S = ±15V	●	1.5	14		MΩ
		V_{IN} = ±3V, V_S = ±5V	●	1.5	11		MΩ
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range	V_S = ±15V, T_A = 25°C		±13	±13.5		V
			●	±12			V
		V_S = ±5V, T_A = 25°C		±3	±3.5		V
			●	±2			V
CMRR	Common-Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C		55	62		dB
		V_S = ±15V, V_{CM} = ±12V	●	55			dB
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C		55	61		dB
		V_S = ±5V, V_{CM} = ±2V	●	55			dB
	Inverting Input Current Common-Mode Rejection	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C			3.5	10	µA/V
		V_S = ±15V, V_{CM} = ±12V	●			10	µA/V
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C			4.5	10	µA/V
		V_S = ±5V, V_{CM} = ±2V	●			10	µA/V

ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V, T_A = 25°C		60	80		dB
		V_S = ±3V to ±15V	●	60			dB
	Noninverting Input Current Power Supply Rejection	V_S = ±2V to ±15V, T_A = 25°C			2	50	nA/V
		V_S = ±3V to ±15V	●			50	nA/V
	Inverting Input Current Power Supply Rejection	V_S = ±2V to ±15V, T_A = 25°C			0.25	5	µA/V
		V_S = ±3V to ±15V	●			5	µA/V
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1k	●	55	72		dB
		V_S = ±5V, V_{OUT} = ±2V, R_L = 150Ω	●	55	72		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN^-}$	V_S = ±15V, V_{OUT} = ±10V, R_L = 1k	●	100	270		kΩ
		V_S = ±5V, V_{OUT} = ±2V, R_L = 150Ω	●	100	240		kΩ
V_{OUT}	Maximum Output Voltage Swing	V_S = ±15V, R_L = 400Ω, T_A = 25°C		±12	±13.5		V
			●	±10			V
		V_S = ±5V, R_L = 150Ω, T_A = 25°C		±3	±3.7		V
			●	±2.5			V
I_{OUT}	Maximum Output Current	R_L = 0Ω, T_A = 25°C		30	60		mA
I_S	Supply Current (Note 2)	V_S = ±15V, V_{OUT} = 0V, T_A = 25°C			10	15.0	mA
			●			17.5	mA
	Positive Supply Current, Shutdown	V_S = ±15V, Pin 8 Voltage = 0V, T_A = 25°C			120	300	µA
			●			500	µA
I_8	Shutdown Pin Current (Note 3)	V_S = ±15V	●			300	µA
	Output Leakage Current, Shutdown	V_S = ±15V, Pin 8 Voltage = 0V, T_A = 25°C				10	µA
SR	Slew Rate (Notes 4 and 5)	T_A = 25°C		500	1100		V/µs
t_r, t_f	Rise and Fall Time, V_{OUT} = $1V_{P-P}$	V_S = ±5V, R_F = 1k, R_G = 1k, R_L = 150Ω			8.7		ns
BW	Small-Signal Bandwidth	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 150Ω			140		MHz
t_r, t_f	Small-Signal Rise and Fall Time	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 100Ω			3.3		ns
	Propagation Delay	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 100Ω			3.4		ns
	Small-Signal Overshoot	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 100Ω			5		%
t_S	Settling Time	0.1%, V_{OUT} = 10V, R_F = 1k, R_G = 1k, R_L = 1k			50		ns
	Differential Gain (Note 6)	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 150Ω			0.014		%
		V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 1k			0.010		%
	Differential Phase (Note 6)	V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 150Ω			0.010		DEG
		V_S = ±15V, R_F = 1k, R_G = 1k, R_L = 1k			0.013		DEG

The ● denotes specifications which apply over the operating temperature range.

Note 1: A heat sink may be required depending on the power supply voltage.

Note 2: The supply current of the LT1227 has a negative temperature coefficient. For more information, see Typical Performance Characteristics curves.

Note 3: Ramp pin 8 voltage down from 15V while measuring I_S. When I_S drops to less than 0.5mA, measure pin 8 current.

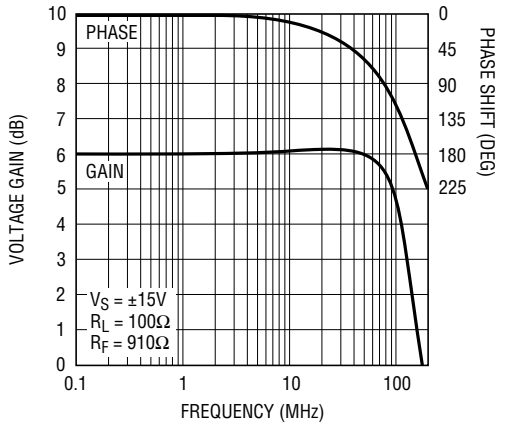
Note 4: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with R_F = 2k, R_G = 220Ω and R_L = 400Ω.

Note 5: AC parameters are 100% tested on the ceramic and plastic DIP package parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

Note 6: NTSC composite video with an output level of 2V.

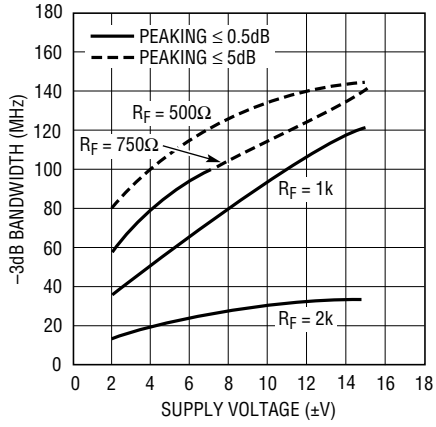
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain and Phase vs Frequency, Gain = 6dB



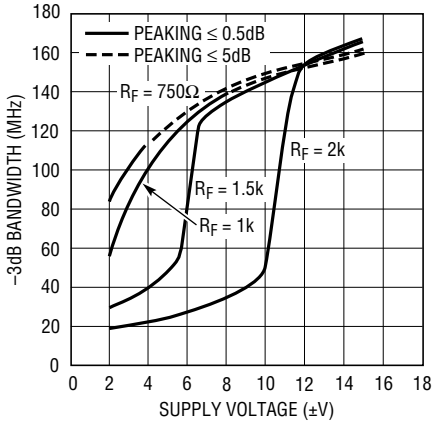
LT1227 • TPC01

–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 100Ω



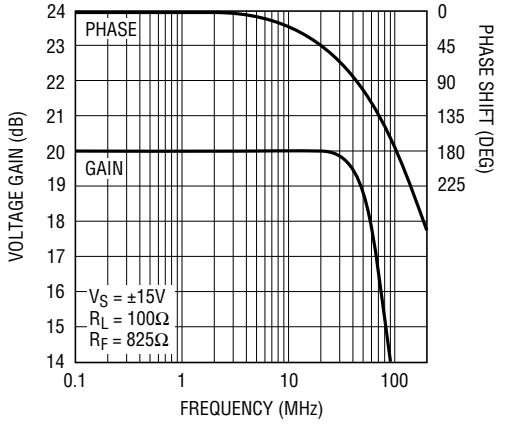
LT1227 • TPC02

–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 1k



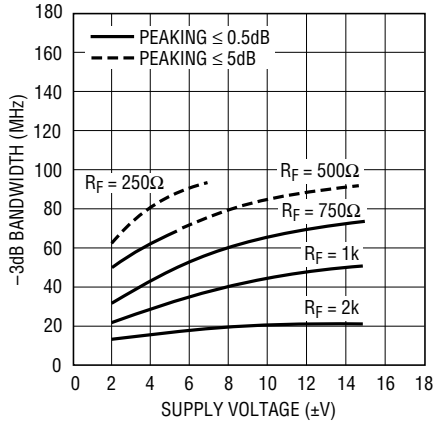
LT1227 • TPC03

Voltage Gain and Phase vs Frequency, Gain = 20dB



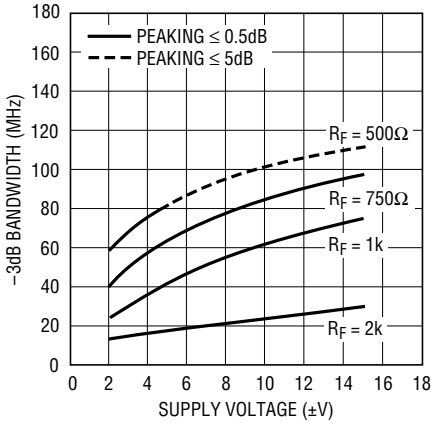
LT1227 • TPC04

–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 100Ω



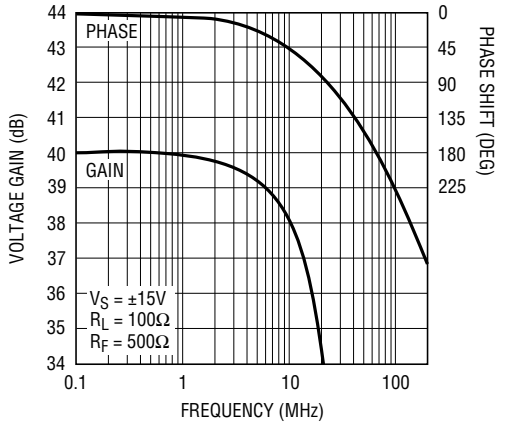
LT1227 • TPC05

–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 1k



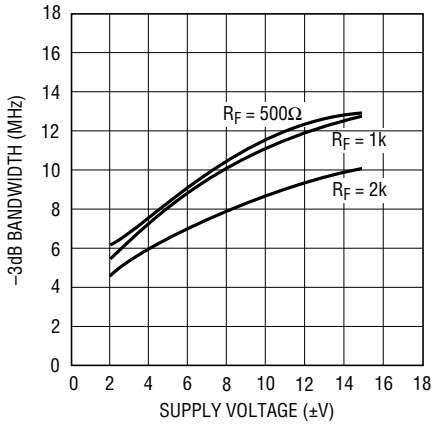
LT1227 • TPC06

Voltage Gain and Phase vs Frequency, Gain = 40dB



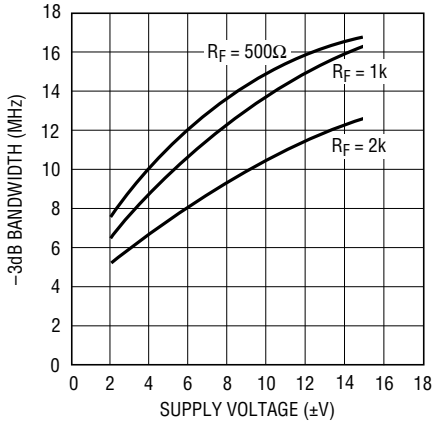
LT1227 • TPC07

–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 100Ω



LT1227 • TPC08

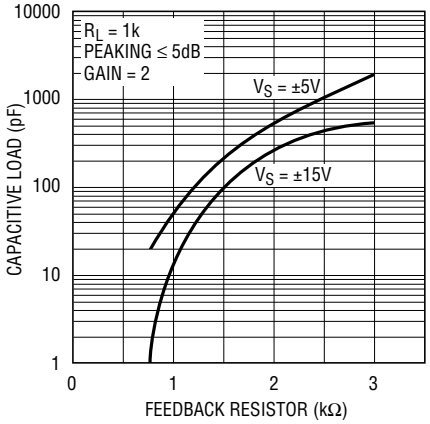
–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 1k



LT1227 • TPC09

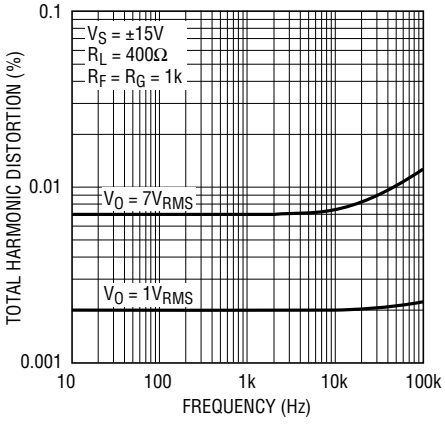
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Capacitive Load vs Feedback Resistor



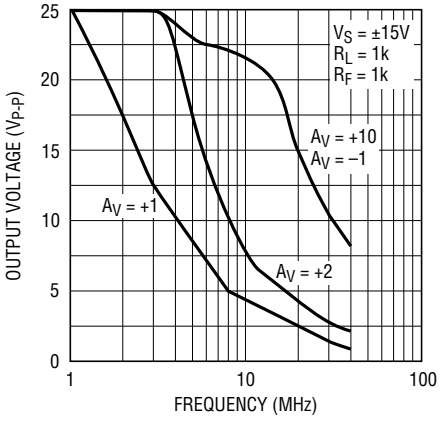
LT1227 • TPC10

Total Harmonic Distortion vs Frequency



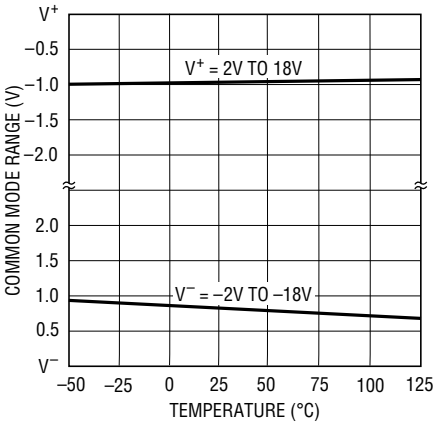
LT1227 • TPC11

Maximum Undistorted Output vs Frequency



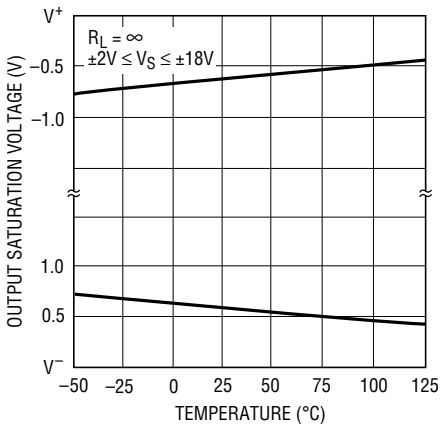
LT1127 • TPC12

Input Common Mode Limit vs Temperature



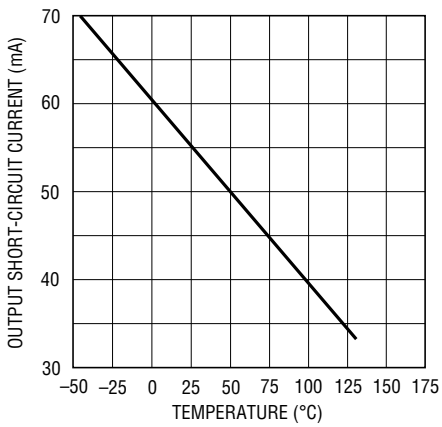
LT1227 • TPC13

Output Saturation Voltage vs Temperature



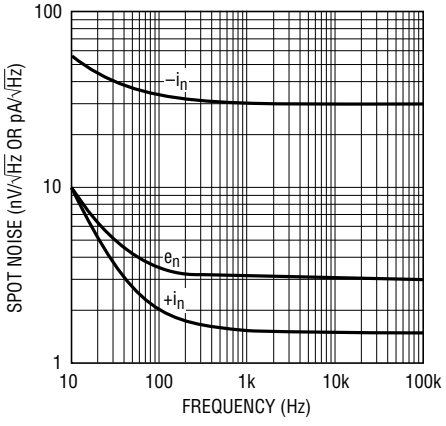
LT1227 • TPC14

Output Short-Circuit Current vs Junction Temperature



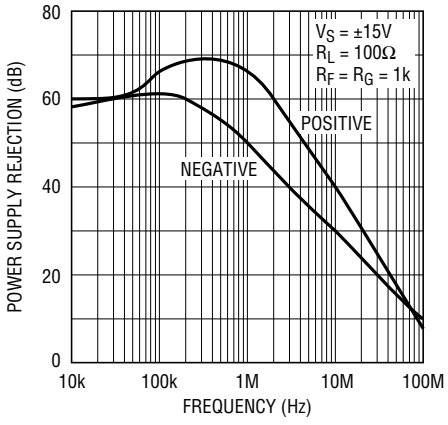
LT1227 • TPC15

Spot Noise Voltage and Current vs Frequency



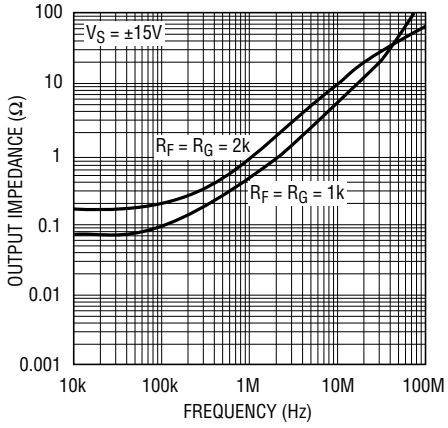
LT1227 • TPC16

Power Supply Rejection vs Frequency



LT1227 • TPC17

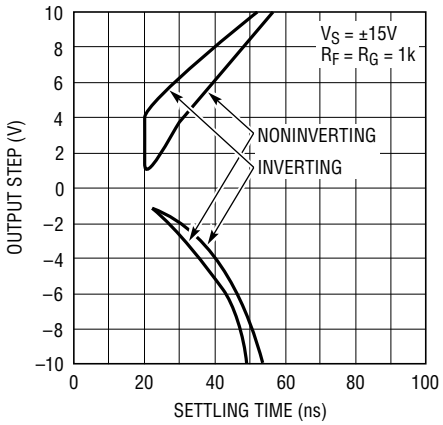
Output Impedance vs Frequency



LT1227 • TPC18

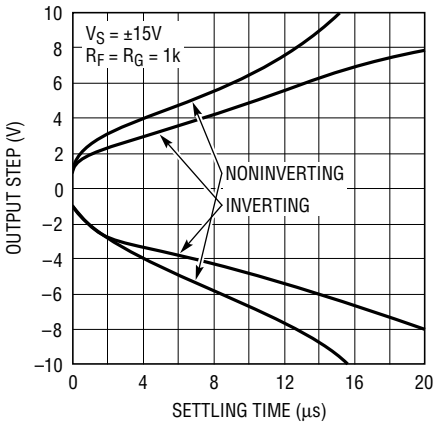
TYPICAL PERFORMANCE CHARACTERISTICS

Settling Time to 10mV vs Output Step



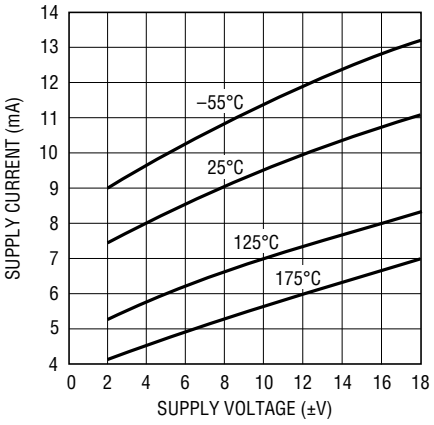
LT1227 • TPC19

Settling Time to 1mV vs Output Step



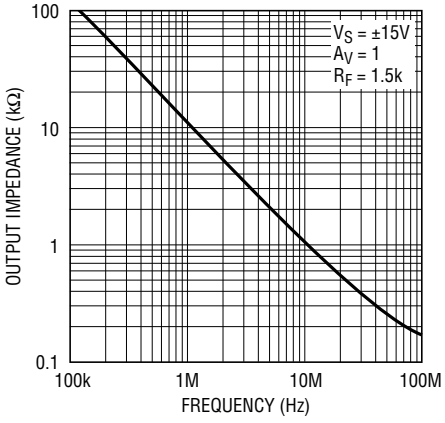
LT1227 • TPC20

Supply Current vs Supply Voltage



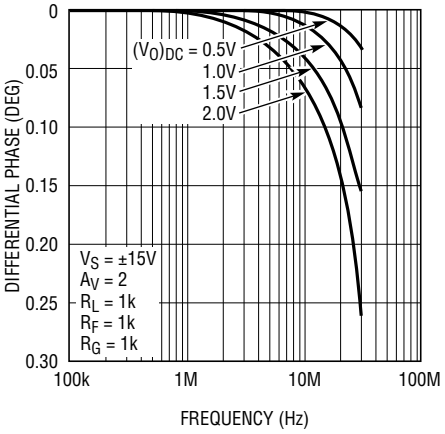
LT1227 • TPC21

Output Impedance in Shutdown vs Frequency



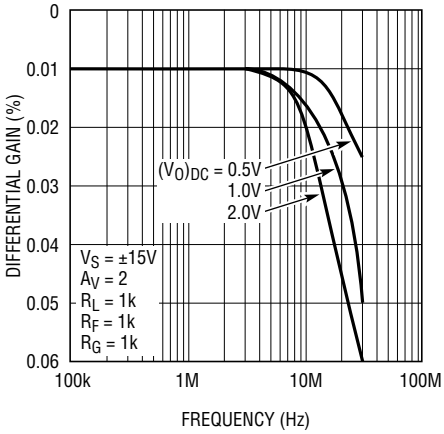
LT1227 • TPC22

Differential Phase vs Frequency



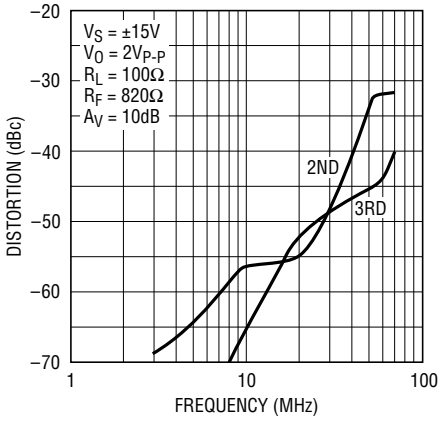
LT1227 • TPC23

Differential Gain vs Frequency



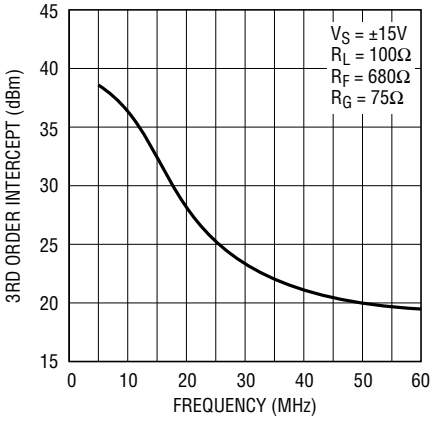
LT1227 • TPC24

2nd and 3rd Harmonic Distortion vs Frequency



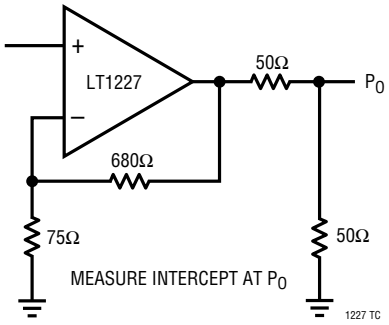
LT1227 • TPC25

3rd Order Intercept vs Frequency

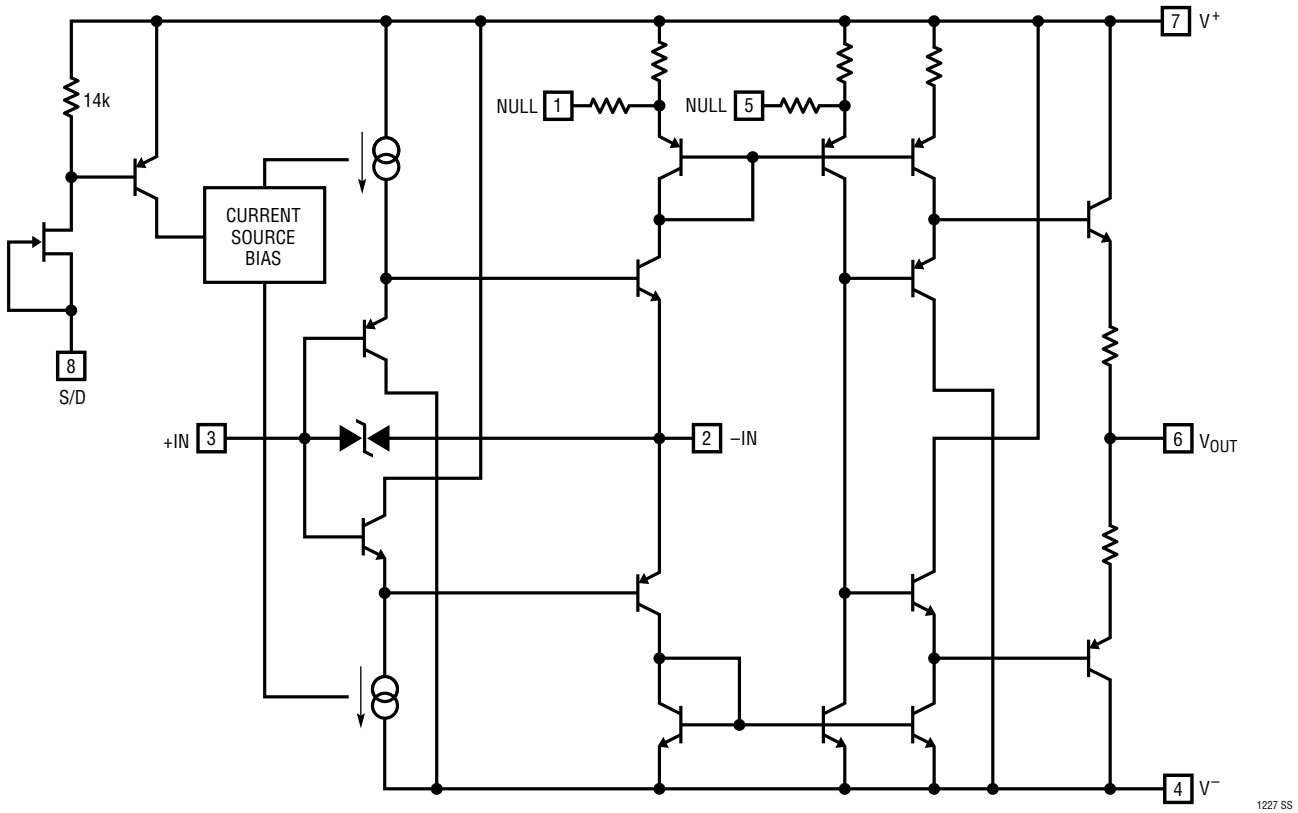


LT1227 • TPC26

Test Circuit for 3rd Order Intercept



SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

The LT1227 is a very fast current feedback amplifier. Because it is a current feedback amplifier, the bandwidth is maintained over a wide range of voltage gains. The amplifier is designed to drive low impedance loads such as cables with excellent linearity at high frequencies.

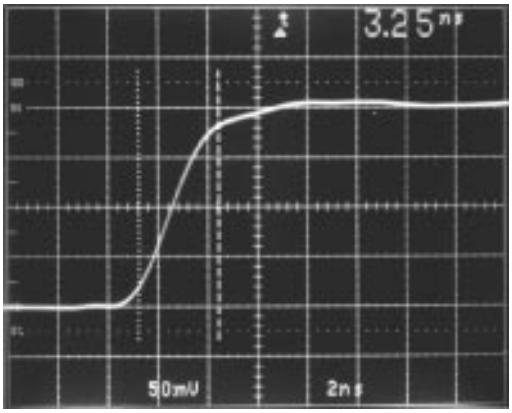
Feedback Resistor Selection

The small-signal bandwidth of the LT1227 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed-loop gain and load resistor. The characteristic curves of Bandwidth vs Supply Voltage show the effect of a heavy load (100Ω) and a light load (1k). These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

At a gain of two, on ±15V supplies with a 1k feedback resistor, the bandwidth into a light load is over 140MHz, but into a heavy load the bandwidth reduces to 120MHz. The loading has this effect because there is a mild resonance in the output stage that enhances the bandwidth at light loads but has its Q reduced by the heavy load. This enhancement is only useful at low gain settlings; at a gain of ten it does not boost the bandwidth. At unity gain, the enhancement is so effective the value of the feedback resistor has very little effect. At very high closed-loop gains, the bandwidth is limited by the gain bandwidth product of about 1GHz. The curves show that the bandwidth at a closed-loop gain of 100 is 12MHz, only one tenth what it is at a gain of two.

APPLICATIONS INFORMATION

Small-Signal Rise Time, A_V = +2



R_F = 1k, R_G= 1k, R_L = 100Ω AI01

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier.

Capacitive Loads

The LT1227 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1k load at a gain of 2. This is a worst case condition, the amplifier is more stable at higher gains and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present and the disadvantage that the gain is a function of the load resistance.

Power Supplies

The LT1227 will operate from single or split supplies from ±2V (4V total) to ±15V (30V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about 500μV per volt of supply mismatch. The inverting bias current can change as much as 5.0μA per volt of supply mismatch, though typically the change is less than 0.5μA per volt.

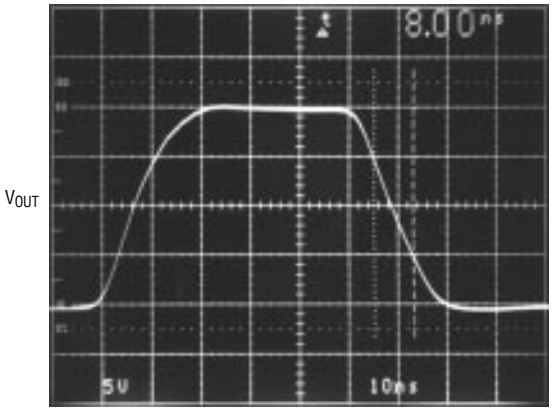
Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way slew rate is in a traditional op amp. This is because both the input stage and the output stage have slew rate limitations. In the inverting mode, and for higher gains in the noninverting mode, the signal amplitude between the input pins is small and the overall slew rate is that of the output stage. For gains less than ten in the noninverting mode, the overall slew rate is limited by the input stage.

The input stage slew rate of the LT1227 is approximately 125V/μs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistors and the internal capacitances. At a gain of ten with a 1k feedback resistor and ±15V supplies, the output slew rate is typically 1100V/μs. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

The graph of Maximum Undistorted Output vs Frequency relates the slew rate limitations to sinusoidal inputs for various gain configurations.

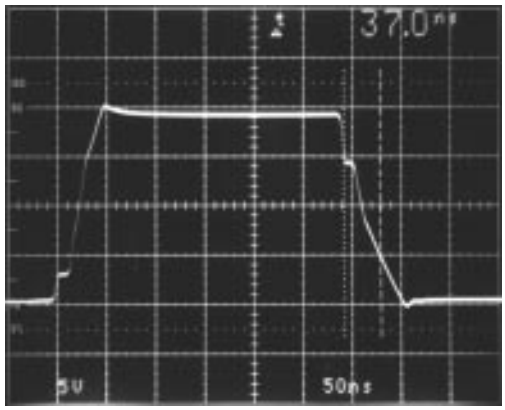
Large-Signal Transient Response, A_V = +10



R_F = 910Ω, R_G= 100Ω, R_L = 400Ω AI02

APPLICATIONS INFORMATION

Large-Signal Transient Response, A_V = +2

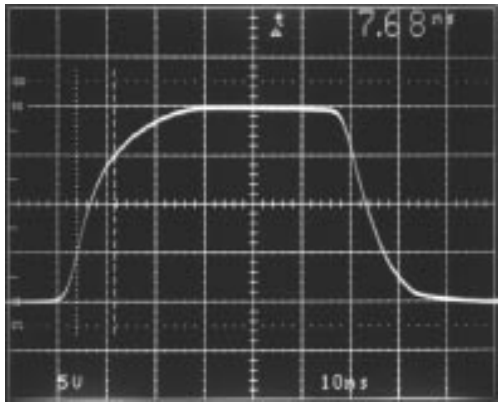


V_{OUT}

R_F = 1k, R_G= 1k, R_L = 400Ω

AI03

Large-Signal Transient Response, A_V = –2



V_{OUT}

R_F = 1k, R_G= 510Ω, R_L = 400Ω

AI04

Settling Time

The characteristic curves show that the LT1227 amplifier settles to within 10mV of final value in 40ns to 55ns for any output step up to 10V. The curve of settling to 1mV of final value shows that there is a slower thermal contribution up to 20μs. The thermal settling component comes from the output and the input stage. The output contributes just under 1mV per volt of output change and the input contributes 300μV per volt of input change. Fortunately the input thermal tends to cancel the output thermal. For this reason the noninverting gain of two configuration settles faster than the inverting gain of one.

Shutdown

The LT1227 has a high impedance, low supply current mode which is controlled by pin 8. In the shutdown mode, the output looks like a 12pF capacitor and the supply current drops to approximately the pin 8 current. The shutdown pin is referenced to the positive supply through an internal pullup circuit (see the simplified schematic). Pulling a current of greater than 50μA from pin 8 will put the device into the shutdown mode. An easy way to force shutdown is to ground pin 8, using open drain (collector) logic. Because the pin is referenced to the positive supply, the logic used should have a breakdown voltage of greater than the positive supply voltage. No other circuitry is necessary as an internal JFET limits the pin 8 current to about 100μA. When pin 8 is open, the LT1227 operates normally.

Differential Input Signal Swing

The differential input swing is limited to about ±6V by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small, so this clamp has no effect; however, in the shutdown mode, the differential swing can be the same as the input swing. The clamp voltage will then set the maximum allowable input voltage. To allow for some margin, it is recommended that the input signal be less than ±5V when the device is shutdown.

Offset Adjust

Pins 1 and 5 are provided for offset nulling. A small current to V^+ or ground will compensate for DC offsets in the device. The pins are referenced to the positive supply (see the simplified schematic) and should be left open if unused. The offset adjust pins act primarily on the inverting input bias current. A 10k pot connected to pins 1 and 5 with the wiper connected to V^+ will null out the bias current, but will not affect the offset voltage much. Since the output offset is

$$V_O \cong A_V \bullet V_{OS} + (I_{IN}-) \bullet R_F$$

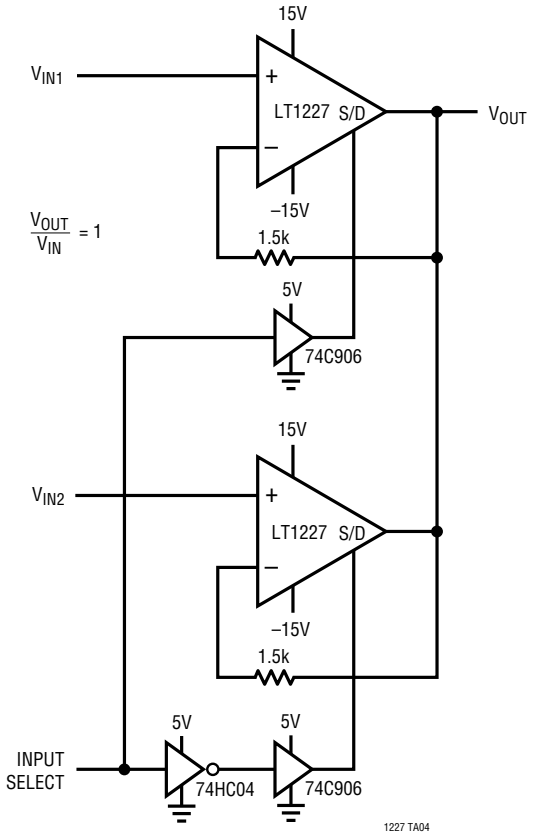
at higher gains ($A_V > 5$), the V_{OS} term will dominate. To null out the V_{OS} term, use a 10k pot between pins 1 and 5 with a 150k resistor from the wiper to ground for 15V split supplies, 47k for 5V split supplies.

TYPICAL APPLICATIONS

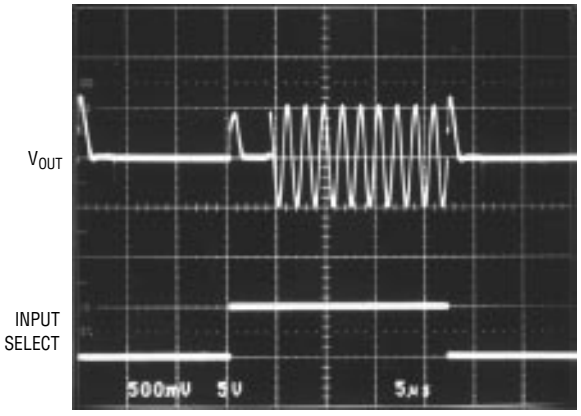
MUX Amplifier

The shutdown function can be effectively used to construct a MUX amplifier. A two-channel version is shown, but more inputs could be added with suitable logic. By configuring each amplifier as a unity-gain follower, there is no loading by the feedback network when the amplifier is off. The open drains of the 74C906 buffers are used to interface the 5V logic to the shutdown pin. Feedthrough from the unselected input to the output is –70dB at 10MHz. The differential voltage between MUX inputs V_{IN1} and V_{IN2} appears across the inputs of the shutdown device, this voltage should be less than ±5V to avoid turning on the clamp diodes discussed previously. If the inputs are sinusoidal having a zero DC level, this implies that the amplitude of each input should be less than $5V_{P-P}$. The output impedance of the off amplifier remains high until the output level exceeds approximately $6V_{P-P}$ at 10MHz, this sets the maximum usable output level. Switching time between inputs is about 4µs without an external pullup. Adding a 10k pullup resistor from each shutdown pin to V^+ will reduce the switching time to 2µs but will increase the positive supply current in shutdown by 1.5mA.

MUX Amplifier

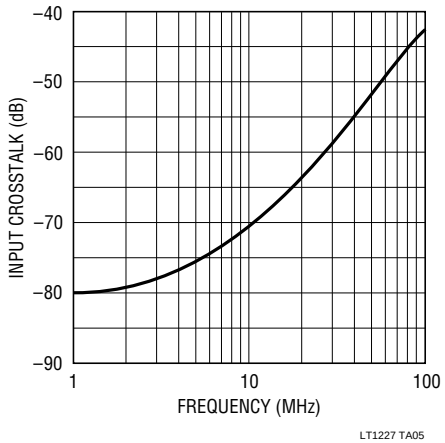


MUX Output



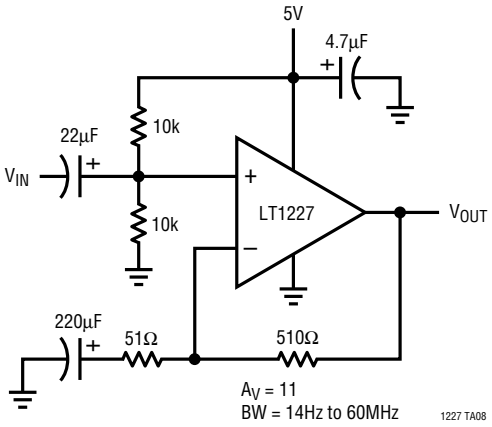
$V_{IN1} = 1V_{P-P}$, $V_{IN2} = 0V$

MUX Input Crosstalk vs Frequency

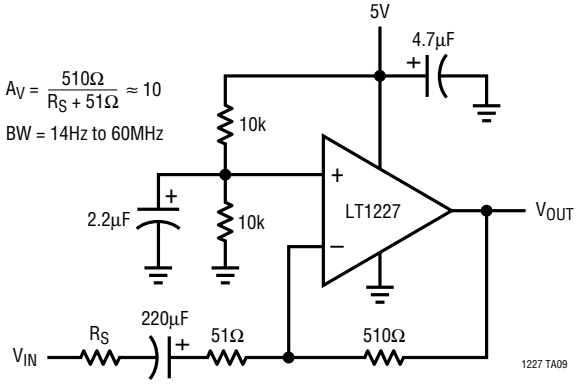


TYPICAL APPLICATIONS

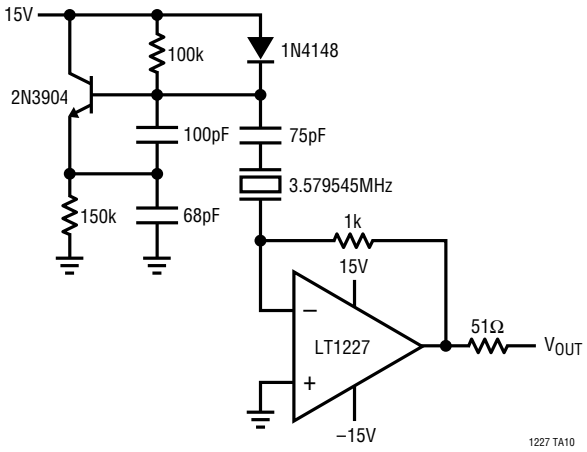
Single Supply AC-Coupled Amplifier Noninverting



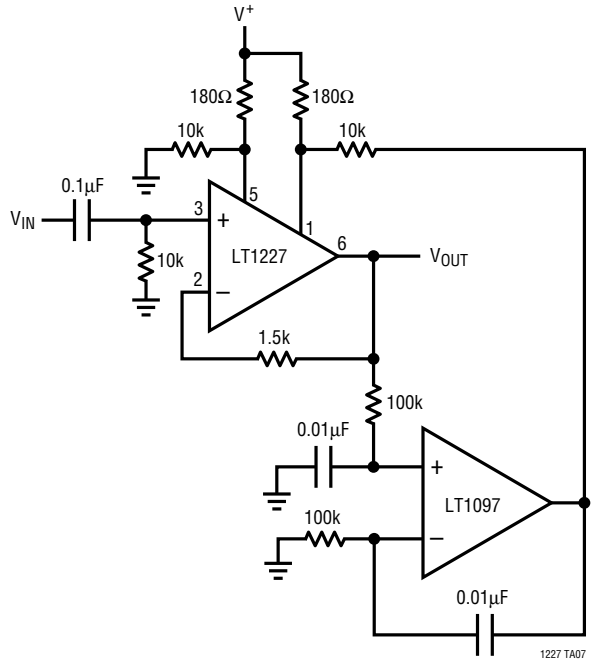
Single Supply AC-Coupled Amplifier Inverting



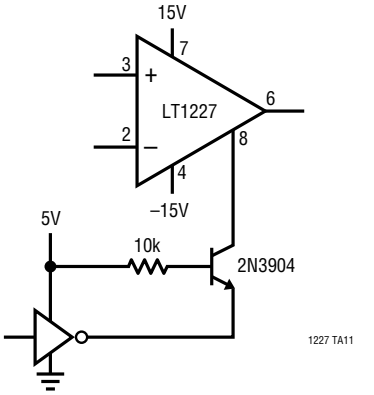
3.58MHz Oscillator



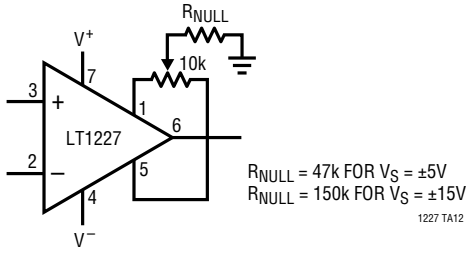
Buffer with DC Nulling Loop



CMOS Logic to Shutdown Interface

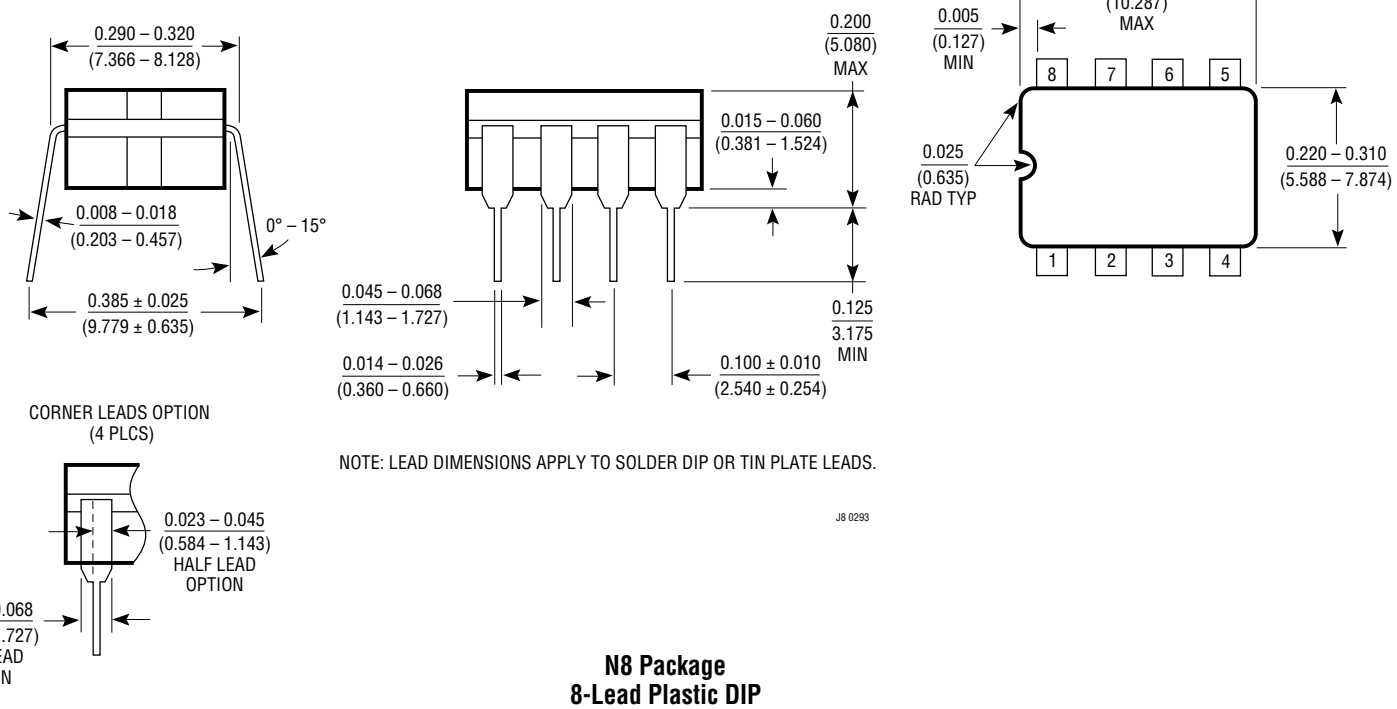


Optional Offset Nulling circuit



PACKAGE DESCRIPTION

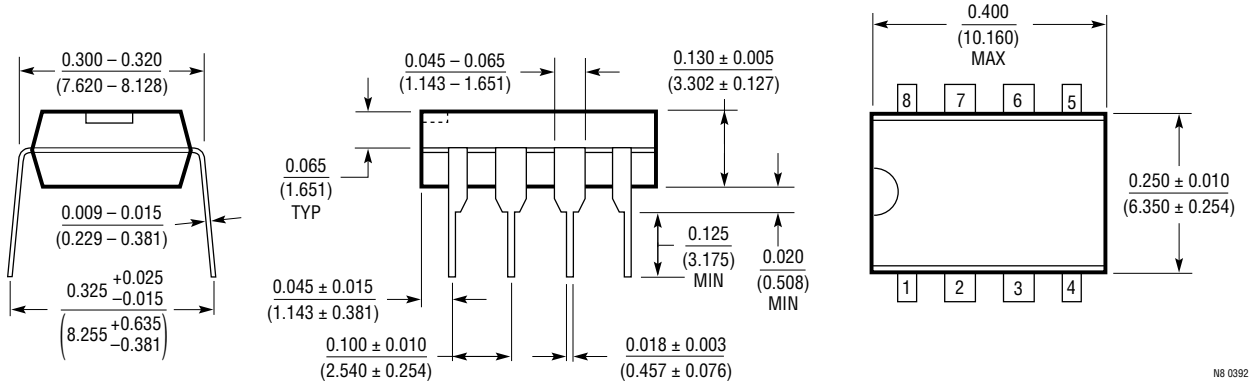
J8 Package
8-Lead Ceramic DIP



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

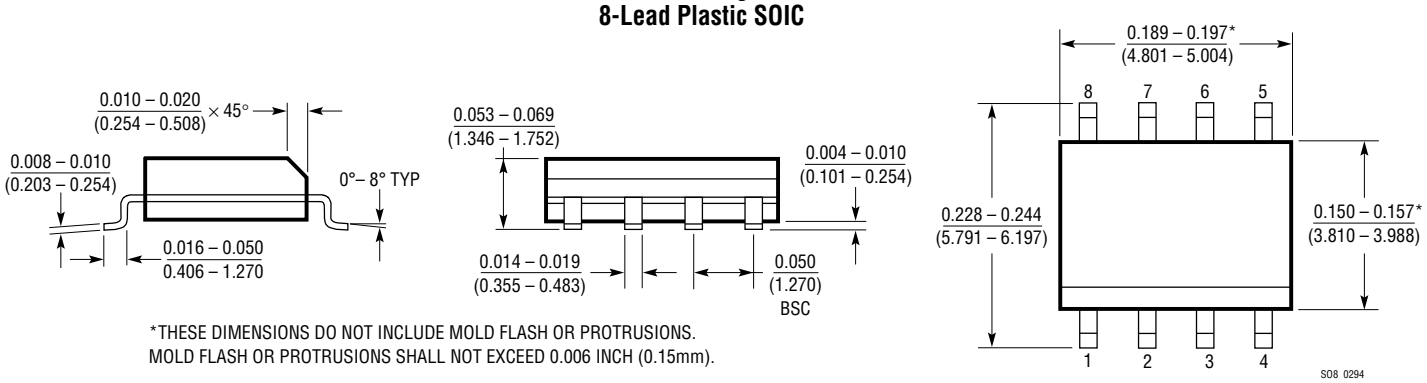
J8 0293

N8 Package
8-Lead Plastic DIP



N8 0392

S8 Package
8-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

SO8 0294

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 0394 5K REV A

Dual/Quad Precision Chopper Stabilized Operational Amplifiers With Internal Capacitors

FEATURES

- Dual/Quad Low Cost Precision Op Amp
- No External Components Required
- Maximum Offset Voltage 5μV
- Maximum Offset Voltage Drift 0.05μV/°C
- Low Noise 1.5μV_{p-p} (0.1Hz to 10Hz)
- Minimum Voltage Gain, 120dB
- Minimum PSRR, 120dB
- Minimum CMRR, 114dB
- Low Supply Current 1mA/Op Amp
- Single Supply Operation 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time 3ms
- Pin Compatible with Industry Standard Dual and Quad Op Amps

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition
- DC Accurate R, C Active Filters

DESCRIPTION

The LTC1051/LTC1053 is a high performance, low cost dual/quad chopper stabilized operational amplifier. The unique achievement of the LTC1051/LTC1053 is that it integrates on chip the sample-and-hold capacitors usually required externally by other chopper amplifiers. Further, the LTC1051/LTC1053 offers better combined overall DC and AC performance than is available from other chopper stabilized amplifiers with or without internal sample/hold capacitors

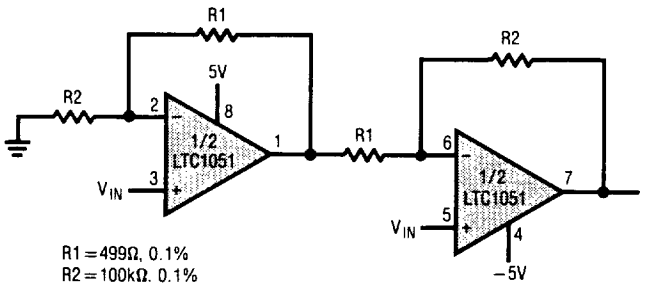
The LTC1051/LTC1053 has an offset voltage of 0.5μV, drift of 0.01μV/°C, DC to 10Hz, input noise voltage typically 1.5μV_{p-p} and typical voltage gain of 140dB. The slew rate of 4V/μs and gain bandwidth product of 2.5MHz are achieved with only 1mA of supply current per op amp.

Overload recovery times from positive and negative saturation conditions are 1.5ms and 3ms respectively, about a 100 or more times improvement over chopper amplifiers using external capacitors.

The LTC1051 is available in standard plastic and ceramic dual in line packages as well as a 16-pin SOL package. The LTC1053 is available in a standard 14-pin plastic package and an 18-pin SOIC. The LTC1051/LTC1053 is a plug in replacement for most standard dual/quad op amps with improved performance.

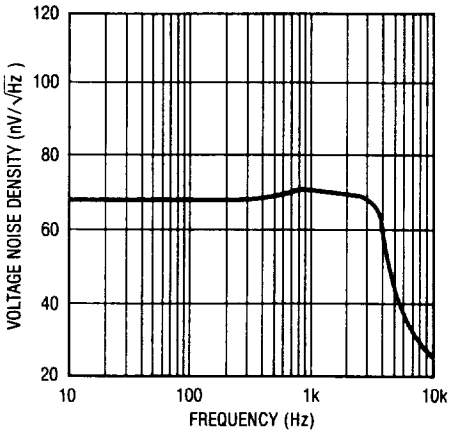
TYPICAL APPLICATION

High Performance Low Cost Instrumentation Amplifier



R1 = 499Ω, 0.1%
R2 = 100kΩ. 0.1%
GAIN = 201
MEASURED CMRR – 120dB AT DC
MEASURED INPUT V_{OS} 3μV
MEASURED INPUT NOISE 2μVp-p (DC – 10Hz)

LTC1051 Noise Spectrum



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V–) 16.5V
Input Voltage ..... (V+ + 0.3V) to (V– – 0.3V)
Output Short Circuit Duration ..... Indefinite

Operating Temperature Range
LTC1051M, LTC1051AM ..... –55°C to 125°C
LTC1051C/LTC1053C, LTC1051AC ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
TOP VIEW OUT A 1, –IN A 2, +IN A 3, V– 4, 8 V+, 7 OUT B, 6 –IN B, 5 +IN B J PACKAGE 8-LEAD CERAMIC DIP N PACKAGE 8-LEAD PLASTIC DIP	LTC1051MJ8 LTC1051CJ8 LTC1051CN8 LTC1051AMJ8 LTC1051ACJ8 LTC1051ACN8	TOP VIEW OUT A 1, –IN A 2, +IN A 3, V+ 4, +IN B 5, –IN B 6, OUT B 7, 14 OUT D, 13 –IN D, 12 +IN D, 11 V–, 10 +IN C, 9 –IN C, 8 OUT C N PACKAGE 14-LEAD PLASTIC DIP	LTC1053CN
TOP VIEW NC 1, NC 2, OUT A 3, –IN A 4, +IN A 5, V– 6, NC 7, NC 8, 16 NC, 15 NC, 14 V+, 13 OUT B, 12 –IN B, 11 +IN B, 10 NC, 9 NC S PACKAGE 16-LEAD PLASTIC SOL	LTC1051CS LTC1051ACS	TOP VIEW NC 1, OUT A 2, –IN A 3, +IN A 4, V+ 5, +IN B 6, –IN B 7, OUT B 8, NC 9, 18 NC, 17 OUT D, 16 –IN D, 15 +IN D, 14 V–, 13 +IN C, 12 –IN C, 11 OUT C, 10 NC S PACKAGE 18-LEAD PLASTIC SOL	LTC1053CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, T_A = operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS		LTC1051/LTC1053 MIN	TYP	MAX	LTC1051A MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$			±0.5	±5		±0.5	±5	μV
Average Input Offset Drift		●		±0.0	±0.05		±0.0	±0.05	μV/°C
Long Term Offset Drift				50			50		nV/√Mo
Input Bias Current	$T_A = 25°C$			±15	±65		±15	±50	pA
LTC1051C/LTC1053C		●			±135			±100	pA
LTC1051M		●			±450			±300	pA
Input Offset Current (All Grades)	$T_A = 25°C$			±30	±125		±30	±100	pA
		●			±175			±150	pA
Input Noise Voltage (Note 1)	$R_S = 100\Omega$, DC to 10Hz			1.5			1.5	2	μV_{p-p}
	$R_S = 100\Omega$, DC to 1Hz			0.4			0.4		μV_{p-p}
Input Noise Current	f = 10Hz			2.2			2.2		fA/√Hz
Common Mode Rejection Ratio, CMRR	$V_{CM} = V-$ to +2.7V, $T_A = 25°C$		106	130		114	130		dB
		●	100			110			dB
Differential CMRR LTC1051, LTC1053 (Note 2)	$V_{CM} = V^-$ to +2.7V, $T_A = 25°C$		112			112			dB
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to ±8V	●	116	140		120	140		dB
Large Signal Voltage Gain	$R_L = 10k\Omega$, $V_{OUT} = \pm 4V$	●	116	160		120	160		dB
Maximum Output Voltage Swing	$R_L = 10k\Omega$	●	±4.5	±4.85		±4.7	±4.85		V
	$R_L = 100k\Omega$		±4.5	±4.95			±4.95		V
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$			4			4		V/μs

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, T_A = operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS		LTC1051A/LTC1051/LTC1053 MIN	TYP	MAX	UNITS
Gain Bandwidth Product				2.5		MHz
Supply Current/Op Amp	No Load, $T_A = 25°C$			1	2	mA
		●			2.5	mA
Internal Sampling Frequency				3		kHz

$V_S = 5V$, GND, T_A = operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS		LTC1051A/LTC1051/LTC1053 MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$			±0.5	±5	μV
Input Offset Drift				±0.01	±0.05	μV/°C
Input Bias Current	$T_A = 25°C$			±10	±50	pA
Input Offset Current	$T_A = 25°C$			±20	±80	pA
Input Noise Voltage	DC to 10Hz			1.8		μV_{P-P}
Supply Current/Op Amp	No Load, $T_A = 25°C$	●			1.5	mA

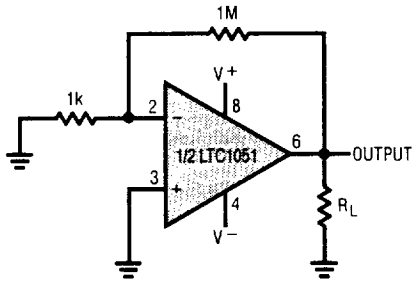
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For guaranteed noise specification contact LTC marketing.

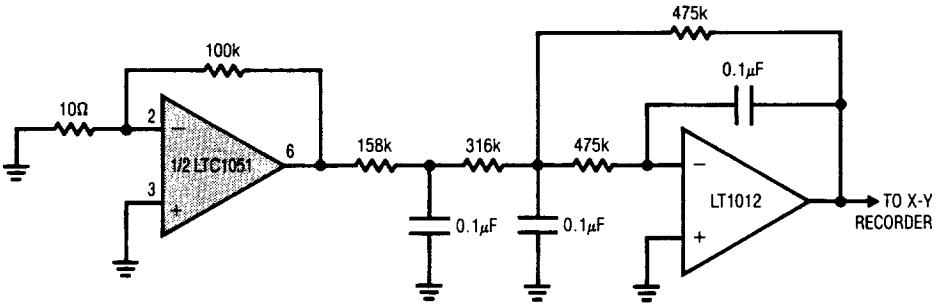
Note 2: Differential CMRR for the LTC1053 is measured between amplifiers A and D, and amplifiers B and C.

TEST CIRCUITS

Electrical Characteristics Test Circuit



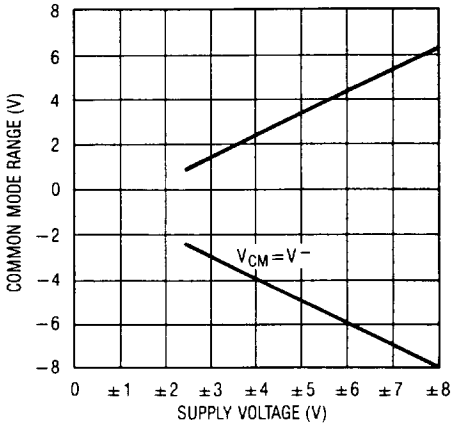
DC-10Hz Noise Test Circuit



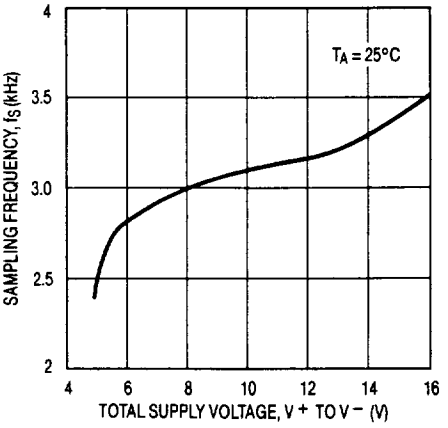
FOR 1Hz NOISE BW INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

TYPICAL PERFORMANCE CHARACTERISTICS

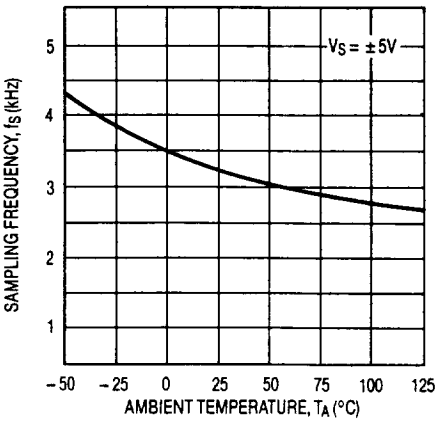
Common Mode Input Range vs Supply Voltage



Sampling Frequency vs Supply Voltage

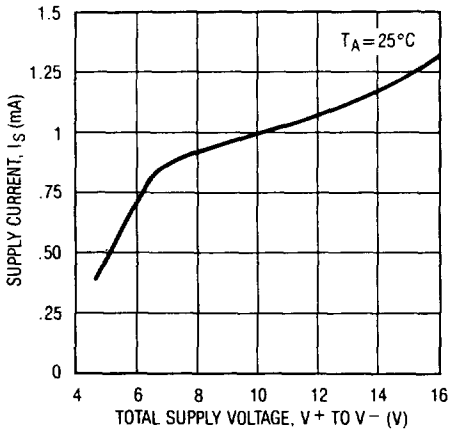


Sampling Frequency vs Temperature

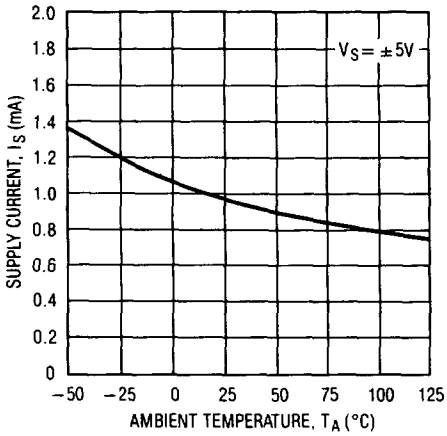


TYPICAL PERFORMANCE CHARACTERISTICS

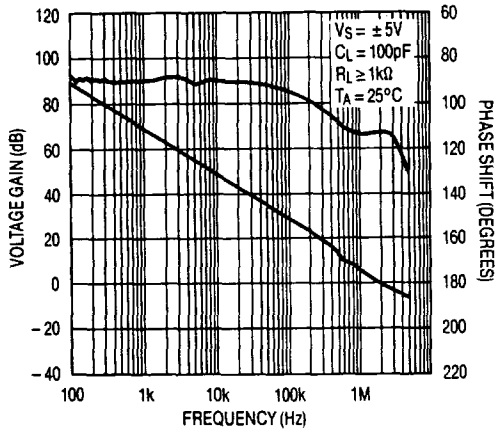
Supply Current vs Supply Voltage Per Op Amp



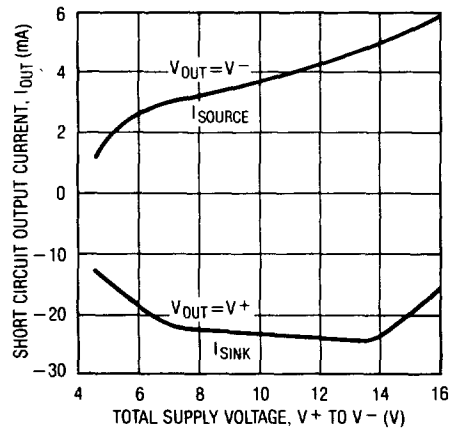
Supply Current vs Temperature Per Op Amp



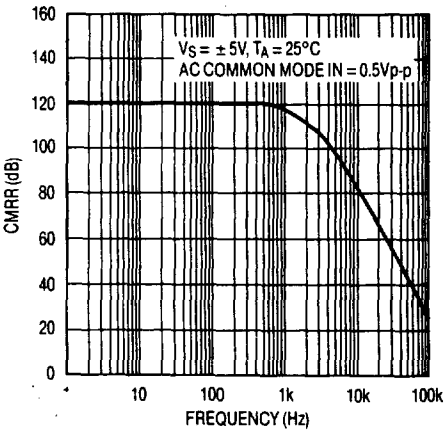
Gain/Phase vs Frequency



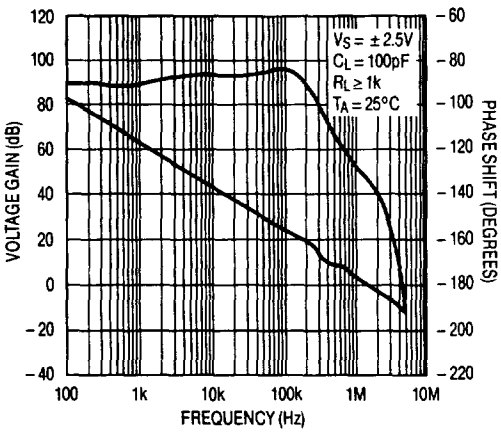
Output Short Circuit Current vs Supply Voltage



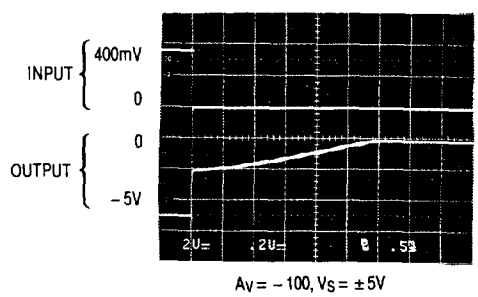
CMRR vs Frequency



Gain/Phase vs Frequency

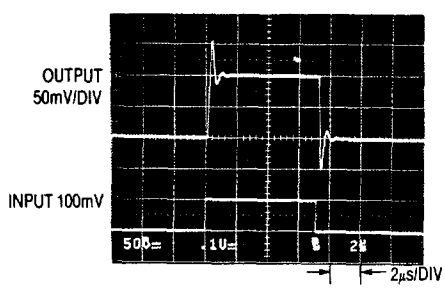


Overload Recovery



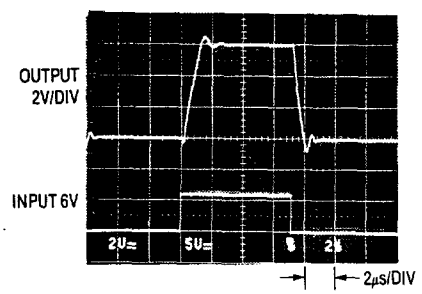
$A_V = -100, V_S = \pm 5V$

Small Signal Transient Response



$A_V = +1, R_L = 10k, C_L = 100pF$
$V_S = \pm 5V, T_A = 25°C$

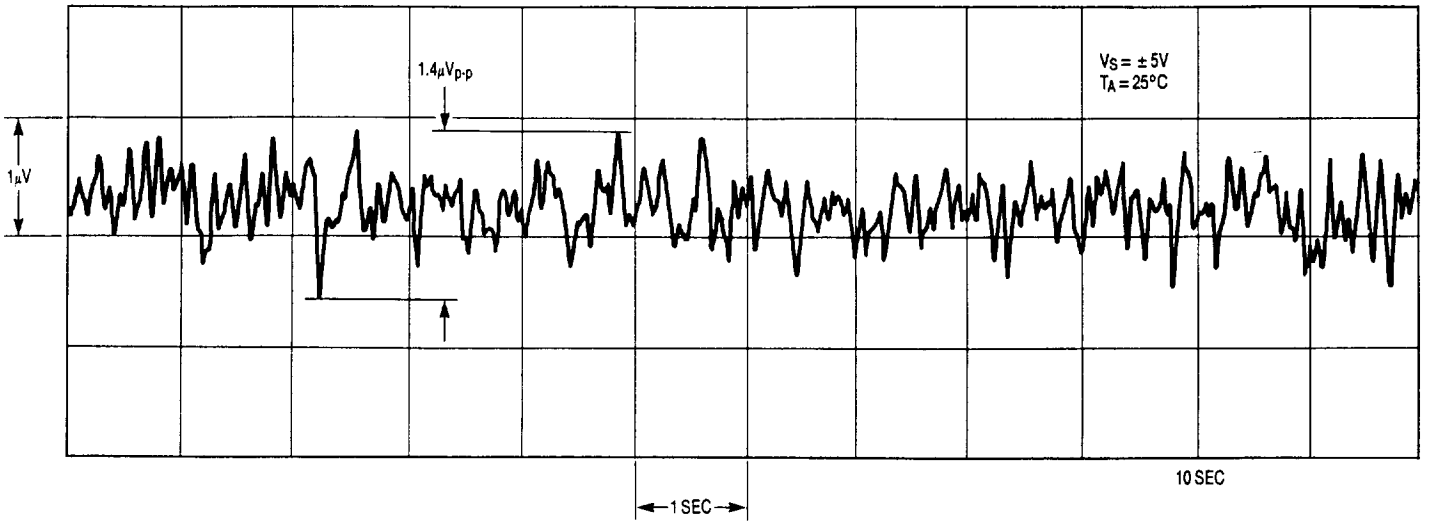
Large Signal Transient Response



$A_V = +1, R_L = 10k, C_L = 100pF$
$V_S = \pm 5V, T_A = 25°C$

TYPICAL PERFORMANCE CHARACTERISTICS

LTC1051/LTC1053 DC to 10Hz Noise



APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1051/LTC1053, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary — particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1051/LTC1053's ultra low drift op amps are to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C — 4 times the maximum drift specification of the LTC1051/LTC1053. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C — 700 times the maximum drift specification of the LTC1051/LTC1053.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of juctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt

APPLICATIONS INFORMATION

to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The termal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

Resistor Type	Thermal EMF/°C Gradient
Tin Oxide	~mV/°C
Carbon Composition	~450μV/°C
Metal Film	~20μV/°C
Wire Wound Evenohm Manganin	 ~2μV/°C ~2μV/°C

INPUT BIAS CURRENT, CLOCK FEEDTHROUGH

At ambient temperatures below 60°C, the input bias current of the LTC1051/LTC1053 op amps is dominated by the small amount of charge injection occurring during the sampling and holding of the op amps input offset voltage. The average value of the resulting current pulses is 10pA to 15pA with sign convention shown in Figure 1.

As the ambient temperature rises, the leakage current of the input protection devices increases, while the charge injection component of the bias current, for all practical purposes, stays constant. At elevated temperatures (above 85°C) the leakage current dominates and the bias current of both inputs assumes the same sign.

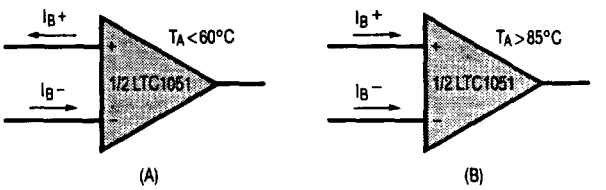


Figure 1. LTC1051 Bias Current

The charge injection at the op amp input pins will cause small output spikes. This phenomenon is often referred to as "clock feedthrough" and it can be easily observed when the closed loop gain exceeds 10V/V, Figure 2. The magnitude of the clock feedthrough is temperature independent but it increases when the closed loop gain goes up, when the source resistance increases, and when the gain setting resistors increase, Figure 2A, 2B. It is important to note that the output small spikes are centered at 0V level and they do not add to the output offset error budget. For instance, with $R_S = 1M\Omega$, the typical output offset voltage of Figure 2C is $V_{OS(OUT)} \approx 10^8 \times I_{B^+} + 101V_{OS(in)}$. A 10pA bias current will yield an output of 1mV ± 100μV. The output clock feedthrough can be attenuated by lowering the value of the gain setting resistors, i.e. R2 = 10k, R1 = 100Ω, instead of (100k, 1k; Figure 2).

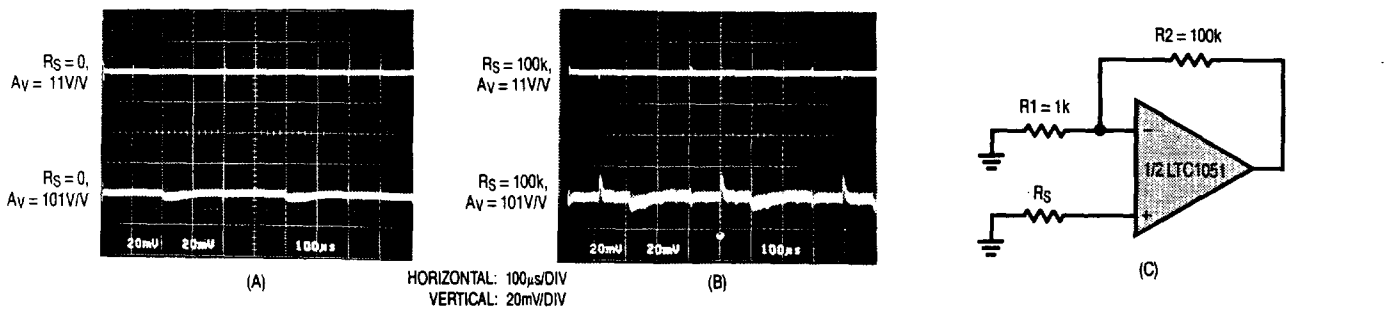


Figure 2. Clock Feedthrough

APPLICATIONS INFORMATION

Clock feedthrough can also be attenuated by adding a capacitor across the feedback resistor to limit the circuit bandwidth below the internal sampling frequency, Figure 3.

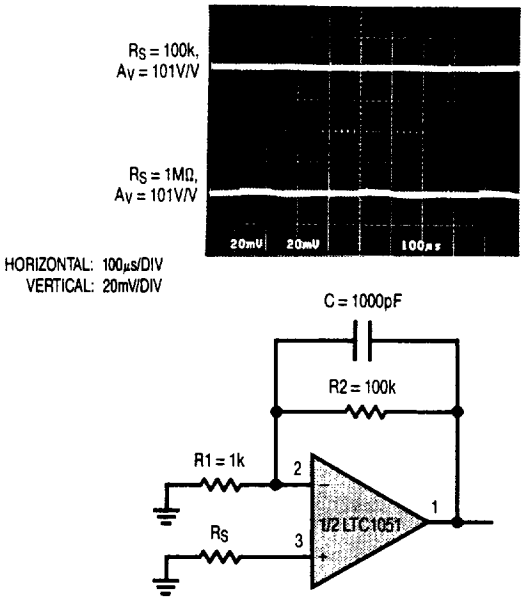


Figure 3. Adding a Feedback Capacitor to Eliminate Clock Feedthrough

INPUT CAPACITANCE

The input capacitance of the LTC1051/LTC1053 op amps is approximately 12pF. When the LTC1051/LTC1053 op amps are used with feedback factors approaching unity, the feedback resistor value should not exceed 7kΩ for industrial temperature range and 5kΩ for military temperature range. If a higher feedback resistor value is required, a feedback capacitor of 20pF should be placed across the feedback resistor. Note that the most common circuits with feedback factors approaching unity are unity gain followers and instrumentation amplifier front ends, Figure 4.

LTC1051/LTC1053 AS AC AMPLIFIERS

Although initially chopper stabilized op amps were designed to minimize DC offsets and offset drifts, the LTC1051/LTC1053 family, on top of its outstanding DC characteristics, presents efficient AC performance. For instance, at single +5V supply, each op amp typically consumes 0.5mA and still provides 1.8MHz gain bandwidth product and 3V/μs slew rate. This, combined with almost distortionless swing to the supply rails, Figure 8, makes the LTC1051/LTC1053 op amps nearly general purpose. To further expand this idea, the "aliasing" phenomenon, which could occur under AC conditions, should be described and properly evaluated.

ALIASING

The LTC1051/LTC1053 are equipped with internal circuitry to minimize aliasing. Aliasing, no matter how small, occurs when the input signal approaches and exceeds the internal clock frequency. Aliasing is caused by the sampled data nature of the chopper op amps. A generalized study of this phenomenon is beyond the scope of a datasheet, however, a set of rules of thumb can answer many questions.

1. Alias signals can be generally defined as output AC signals at a frequency of $nf_{CLK} \pm mf_{IN}$. The nf_{CLK} term is the internal sampling frequency of the chopper stabilized op amps, and its harmonics, mf_{IN} is the frequency of the input signal and its harmonics, if any.

2. If we arbitrarily accept that "aliasing" occurs when output alias signals reach an amplitude of 0.01% or more of the output signal, then: The approximate minimum frequency of an AC input signal which will cause aliasing is equal to the internal clock frequency multiplied by the square root of the op amp feedback factor. For instance, with closed loop gain of −10, the feedback factor is 1/11, and if f_{CLK} = 2.6kHz, alias signals can be detected when the frequency of the input signal exceeds 750Hz to 800Hz, Figure 5A.

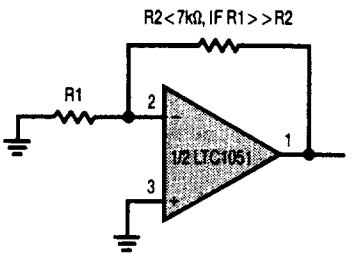


Figure 4. Operating the LTC1051 with Feedback Factors Approaching Unity

APPLICATIONS INFORMATION

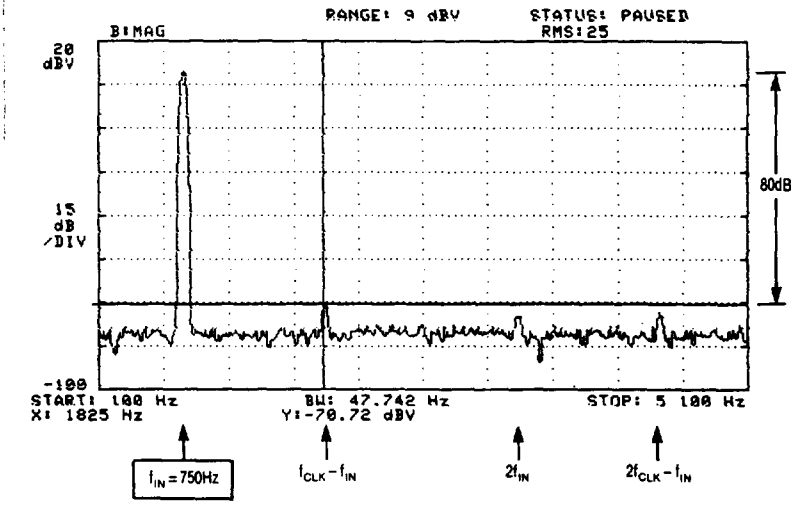
3. The number of alias signals increases when the input signal frequency increases, Figure 5B.

4. When the frequency, f_{IN}, of the input signal is less than f_{CLOCK}, the alias signal(s) amplitude(s) directly scale with the amplitude of the incoming signal. The output "signal to alias ratio" cannot be increased by just boosting the input signal amplitude. However, when the input AC signal frequency well exceeds the clock frequency, the amplitude of the alias signals does not directly scale with the input amplitude. The "signal to alias ratio" increases when the output swings closely to the rails, Figures 5B, 7. It is important to note that the LTC1051/LTC1053 op amps under light loads ($R_L \geq 10k\Omega$) swing closely to the supply rails without generating harmonic distortion, Figure 8.

5. For unity gain inverting configuration, all the alias frequencies are 80dB to 84dB down from the output signal, Figures 6A, 6B. Combined with excellent THD under wide swing, the LTC1051/LTC1053 op amps make efficient unity gain inverters.

   For gain higher than −1, the "signal to alias" ratio decreases at an approximate rate of −6dB per decade of closed loop gain Figure 8.

2



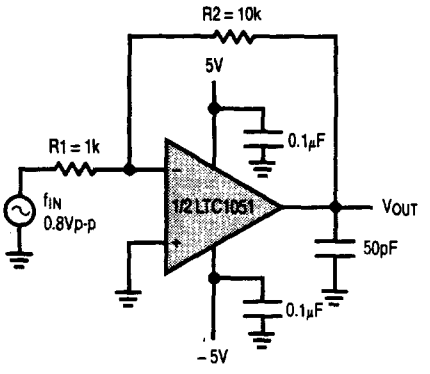


Figure 5A. Output Voltage Spectrum of 1/2 LTC1051 Operating as an Inverting Amplifier with Gain of 10, and Amplifying a 750Hz, 800mV Input AC Signal.

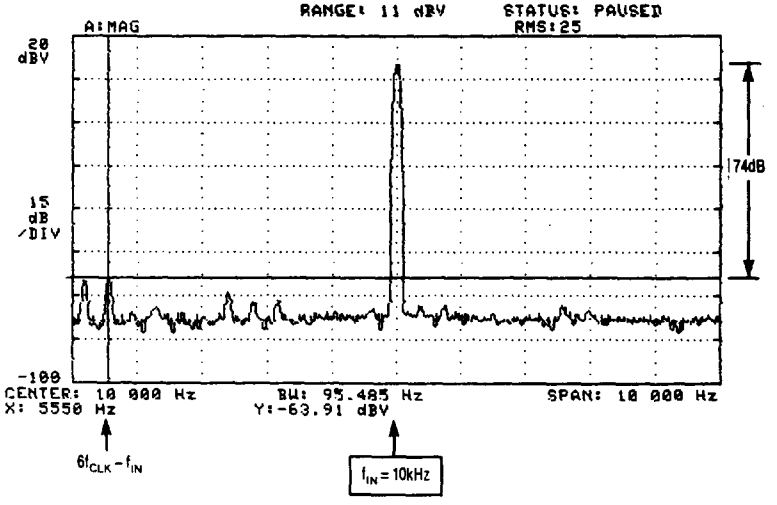


Figure 5B. Same as Figure 5A, but the AC Input Signal is 900mV, 10kHz

APPLICATIONS INFORMATION

6. For closed loop gains of −10 or higher, the "signal to alias" ratio degrades when the value of the feedback gain setting resistor increases beyond 50kΩ. For instance, the 68dB value of Figure 7, decreases to 56dB if a (1kΩ, 100kΩ) resistor set will be used to set the gain of −100.

7. When the LTC1051/LTC1053 are used as non-inverting amplifiers all the previous approximate rules of thumb apply with the following exceptions: When the closed loop gain is +10(V/V) and below, the "signal to alias" ratio is 1dB to 3dB less than the inverting case. When the closed loop gain is 100(V/V) the degradation can be up to 9dB, especially when the input signal is much higher than the clock frequency (i.e. f_{IN} = 10kHz).

8. The signal/alias ratio performance improves when the op amp has bandlimited loop gain.

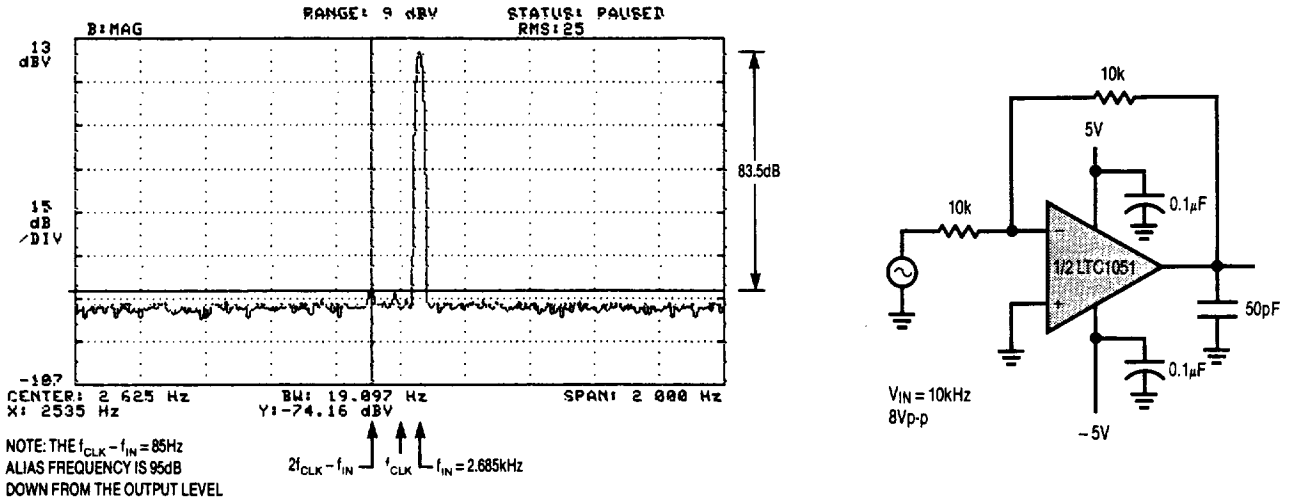


Figure 6A. Output Voltage Spectrum of 1/2 LTC1051 Operating as a Unity Gain Inverting Amplifier. V_S = ±5V, R_L = 10k, C_L = 50pF, V_{IN} = 8Vp-p, 2.685kHz.

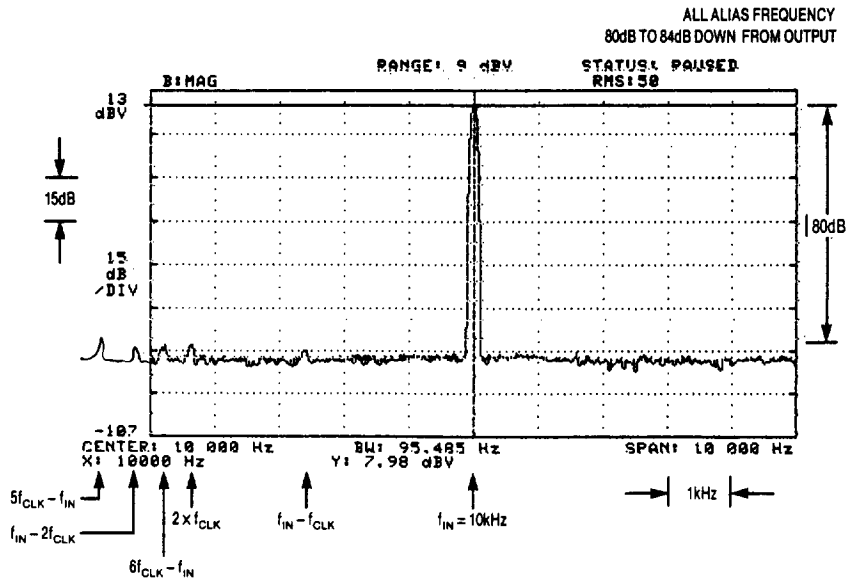
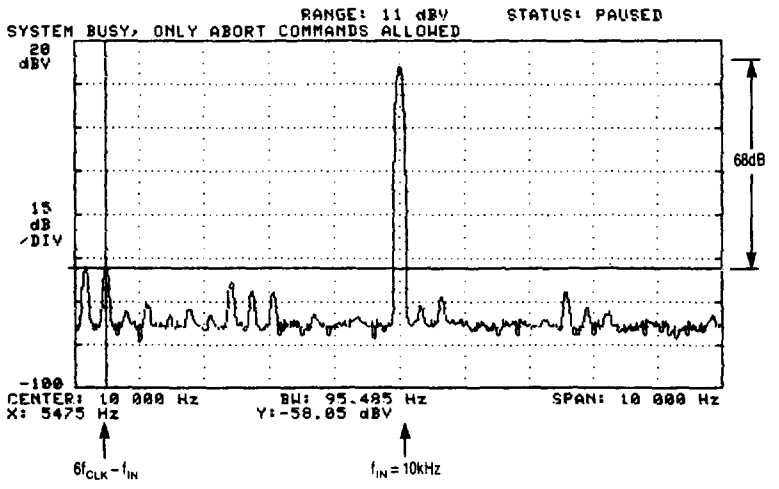


Figure 6B. Output Voltage Spectrum of 1/2 LTC1051, Operating as a Unity Gain Inverting Amplifier. V_S = ±5V, R_L = 10k, C_L = 50pF, V_{IN} = 8Vp-p, 10kHz.

APPLICATIONS INFORMATION



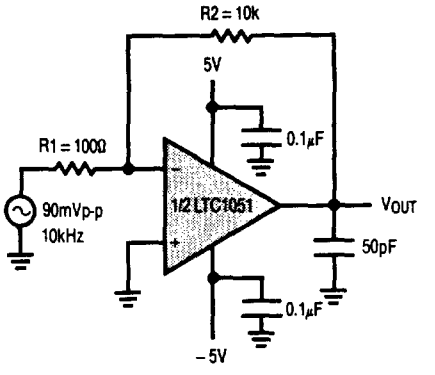


Figure 7. Output Voltage Spectrum of 1/2 LTC1051 Operating as an Inverting Amplifier with a Gain of −100 and Amplifying a 90mVp-p, 10kHz Input Signal. With a 9Vp-p Output Swing the Measured 2nd Harmonic (20kHz) was 75 Down from the 10kHz Input Signal.

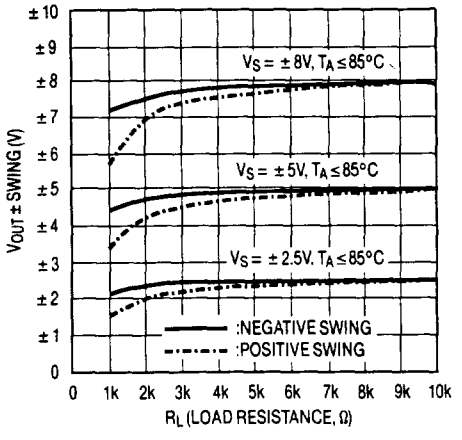


Figure 8. Output Voltage Swing vs Load

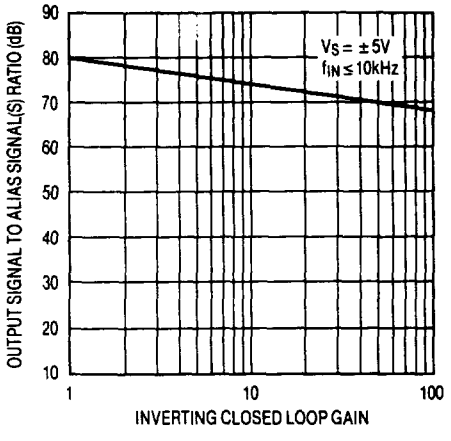
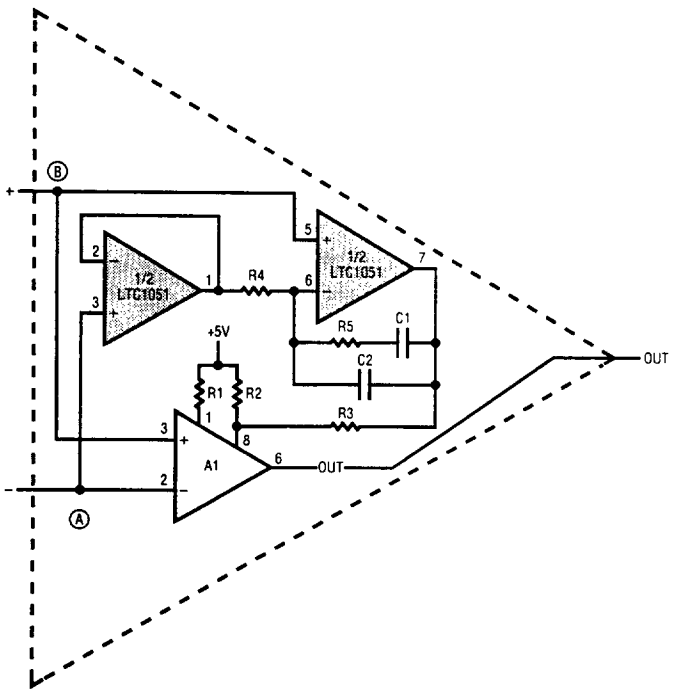


Figure 9. Signal to Alias Ratio vs Closed Loop Gain

APPLICATION CIRCUITS

Obtaining Ultra-Low V_{OS} Drift and Low Noise



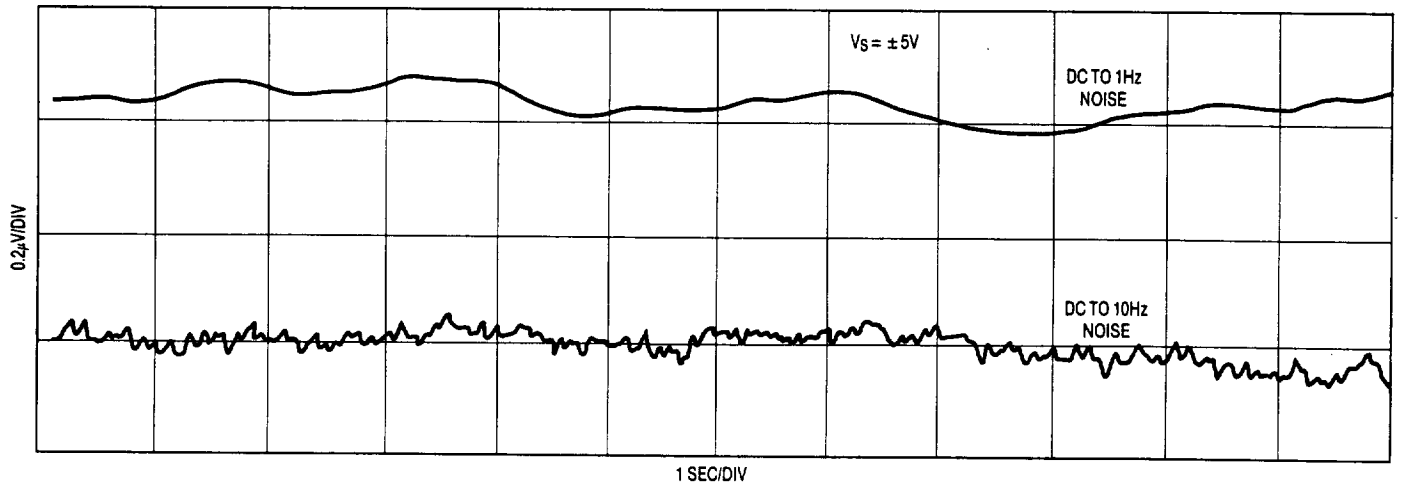
The dual chopper op amp buffers the inputs of A, and corrects its offset voltage and offset voltage drift. With the shown R,C values, the power up warm up time is typically 20s. The step response of the composite amplifier does not present settling tails. The LT1007 should be used when extremely low noise, V_{OS} and V_{OS} drift are sought when the input source resistance is low. (For instance a 350Ω strain gauge bridge.) The LT1012 or equivalent should be used when low bias current (100pA) is also required in conjunction with DC to 10Hz low noise, and low V_{OS} and V_{OS} drift. The measured typical input offset voltages were less than 2μV.

A1	R1	R2	R3	R4	R5	C1	C2	$\bar{e}_{OUT}$ (DC – 1Hz)**	$\bar{e}_{OUT}$ (DC – 10Hz)**
LT1007	3k	2k	340k	10k	100k	0.01μF	0.001μF	0.1μVp-p	0.15μVp-p
LT1012*	750Ω	57Ω	250k	10k	100k	0.01μF	0.001μF	0.3μVp-p	0.4μVp-p

*Interchange connections (A) and (B).

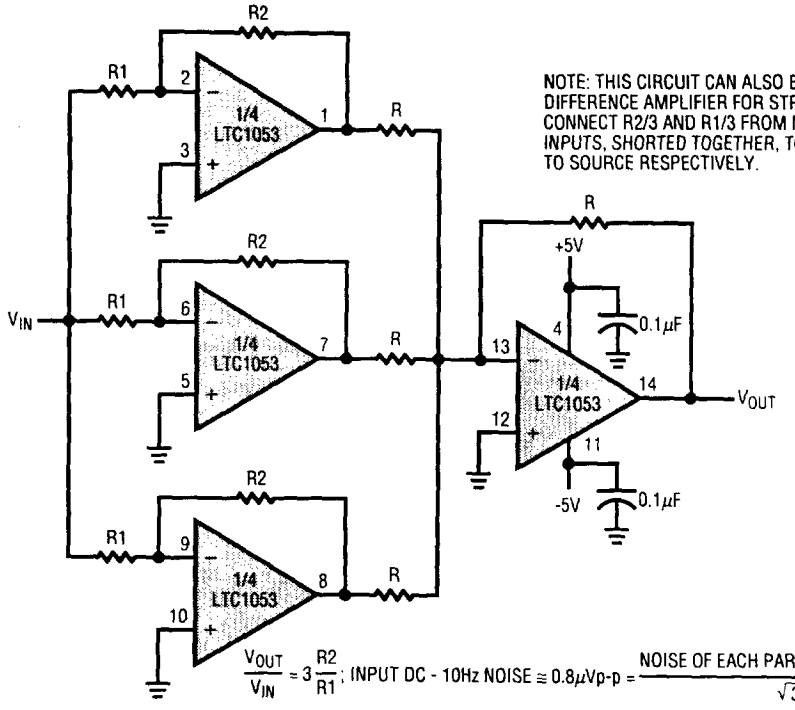
**Noise measured in a 10 sec. window. Peak-to-peak noise was also measured for 10 continuous minutes: With the LT1007 op amp the recorded noise was 0.2μVp-p for both DC-1Hz and DC-10Hz.

LTC1051/LT1007 Peak-to-Peak Noise

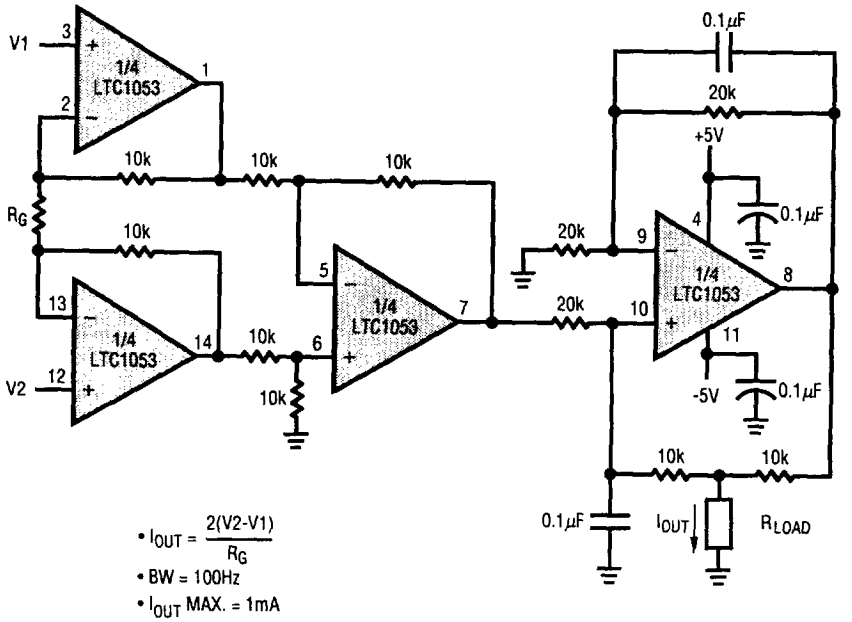


APPLICATION CIRCUITS

Paralleling Choppers to Improve Noise

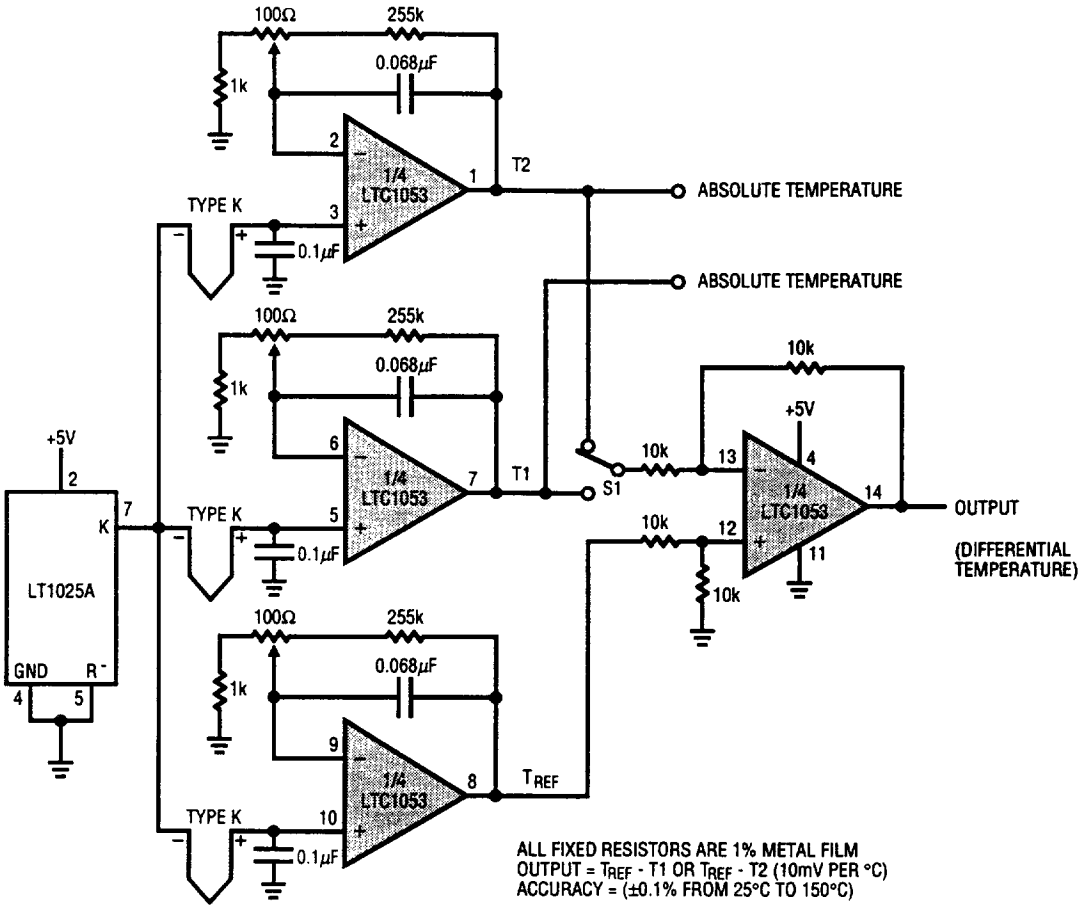


Differential Voltage to Current Converter



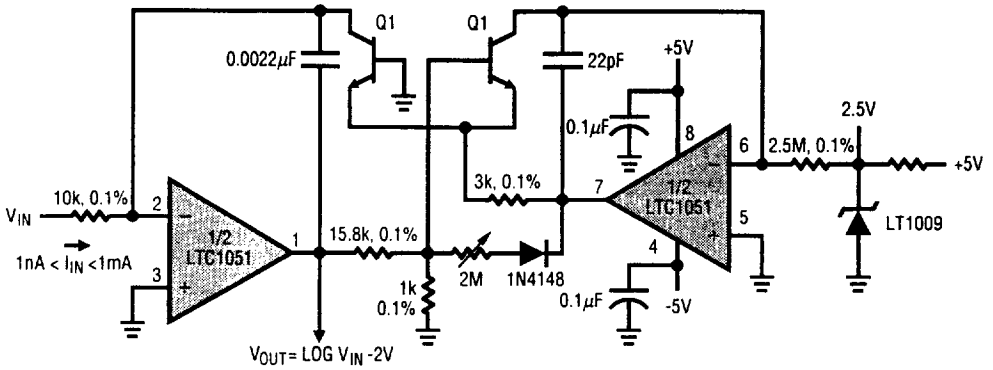
APPLICATION CIRCUITS

Multiplexed Differential Thermometer



ALL FIXED RESISTORS ARE 1% METAL FILM
OUTPUT = T_{REF} - T1 OR T_{REF} - T2 (10mV PER °C)
ACCURACY = (±0.1% FROM 25°C TO 150°C)

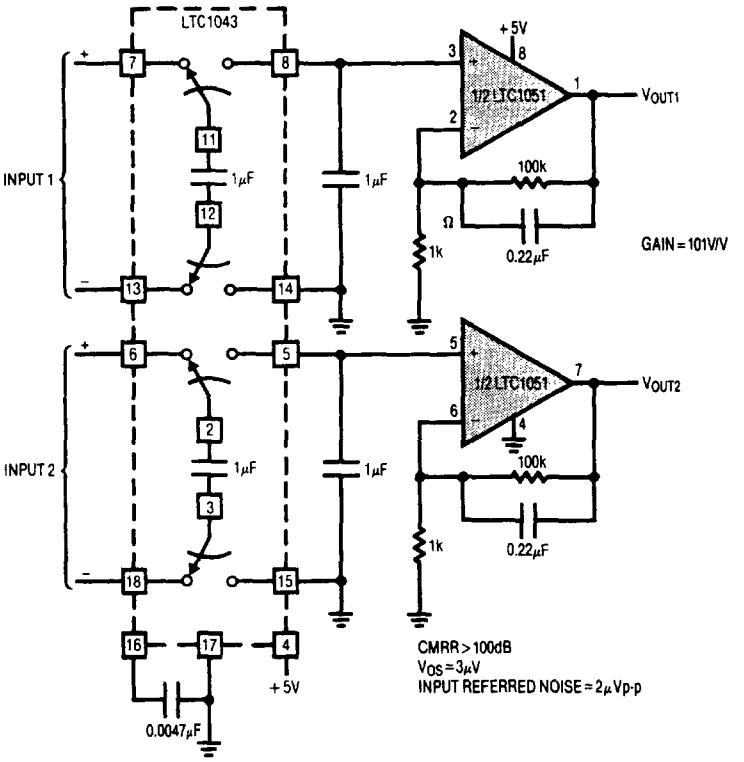
Six Decade Log Amplifier



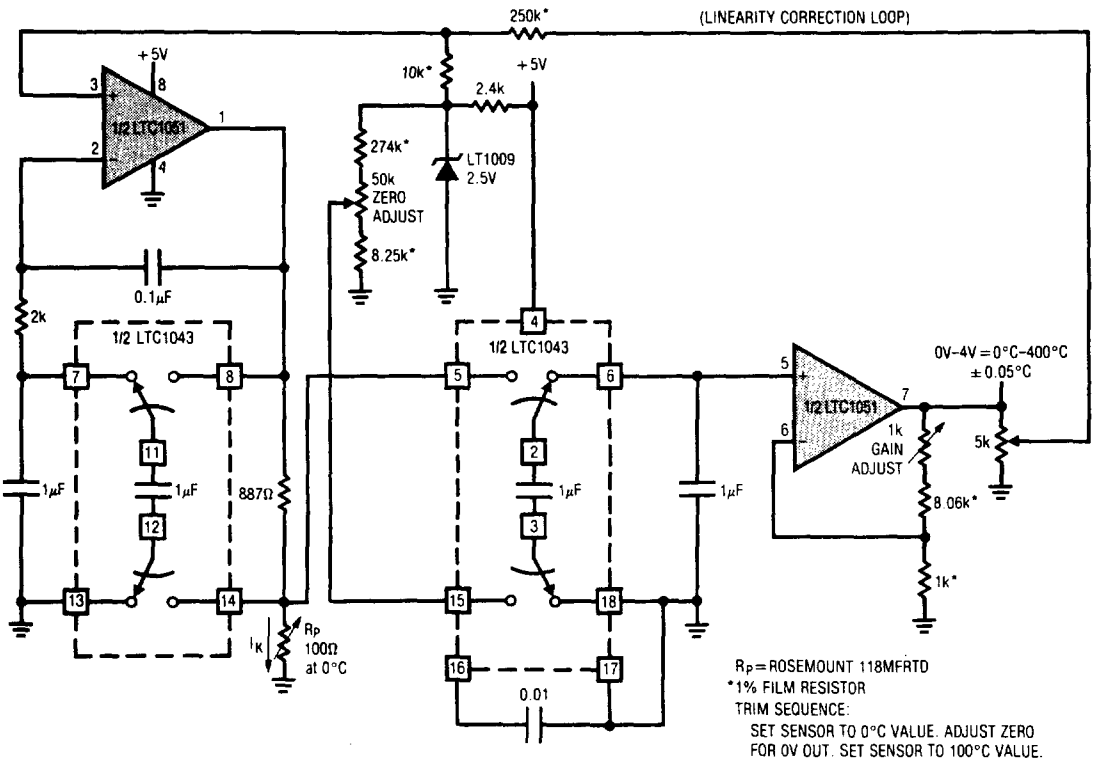
Q1: TEL LAB TYPE Q81
ADJUST 2M POR. FOR NON-LINEARITIES

APPLICATION CIRCUITS

Dual Instrumentation Amplifier

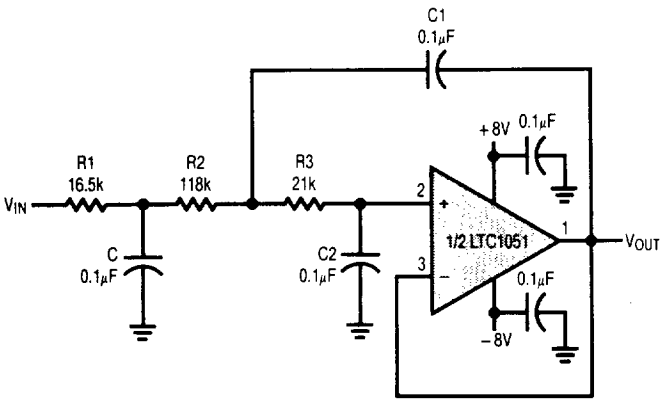


Linearized Platinum Signal Conditioner



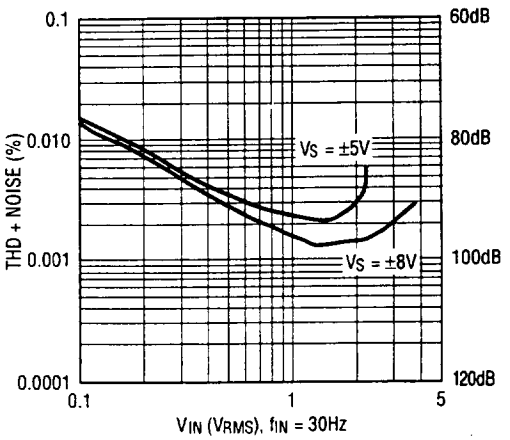
APPLICATION CIRCUITS

DC Accurate, 3rd Order, 100Hz, Butterworth Antialiasing Filter

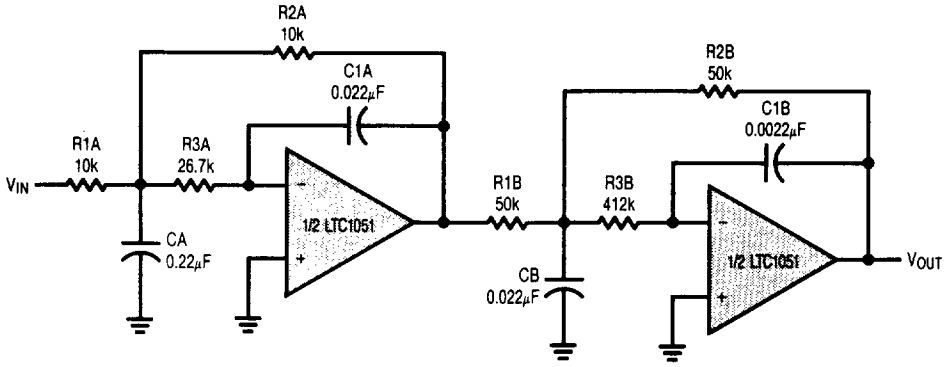


WIDEBAND NOISE 9μV_{RMS}
THD + NOISE = 0.0012%, $1V_{RMS} < V_{IN} < 2V_{RMS}$, $V_S = \pm 8V$
V_{OS} (OUT) < 5μV

Dynamic Range



DC Accurate, 18-Bit 4th Order Antialiasing Bessel (Linear Phase), 100Hz, Lowpass Filter



WIDEBAND RMS NOISE 4.5μV_{RMS}
THD + NOISE = 0.0005% (= 106dB DYN. RANGE), $2V_{RMS} \leq V_{IN} \leq 3V_{RMS}$
V_{OS} OUT < 10μV

Dynamic Range