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- Power MOS FET Array

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Section 1 Lineup by Application

1.1 Power Supply Use

1. Recommended products in each power range

Type	Input Voltage	Recommended Products in Each Power Range: Up to 10 W	10 W to 30 W	30 W to 50 W	50 W to 100 W	100 W to 200 W	200 W
Switching power supply	100 V to 132 V AC	□ 2SK1151 (3.5)	▲ 2SK1153 (2.0)	▲ 2SK1155 (1.0)	▲ 2SK1159 (0.55)	● 2SK1163 (0.55)	● 2SK1169 (0.2)
		□ 2SK1152 (4.0)	▲ 2SK1154 (2.2)	▲ 2SK1156 (1.2)	▲ 2SK1160 (0.6)	● 2SK1164 (0.6)	● 2SK1170 (0.22)
			▼ 2SK1862 (2.0)	▲ 2SK1157 (0.6)	● 2SK1161 (0.6)	● 2SK1165 (0.4)	◇ 2SK1971 (0.19)
			▼ 2SK1863 (2.2)	▲ 2SK1158 (0.7)	● 2SK1162 (0.7)	● 2SK1166 (0.45)	◇ 2SK1526 (0.11)
				■ 2SK1313 (1.0)	● 2SK1163 (0.55)	● 2SK1167 (0.25)	◇ 2SK1527 (0.12)
				■ 2SK1314 (1.2)	■ 2SK1315 (0.55)	● 2SK1168 (0.3)	◇ 2SK1629 (0.22)
				■ 2SK1540 (0.6)	■ 2SK1316 (0.60)	2SK1403A (1.0)	◇ 2SK1836 (0.08)
				■ 2SK1541 (0.7)	▼ 2SK1567 (0.6)		◇ 2SK1837 (0.085)
				▼ 2SK1626 (1.0)	■ 2SK1869 (0.6)		◆ 2SK2174 (0.22)
				▼ 2SK1627 (1.2)	▽ 2SK2117 (0.6)		
				▼ 2SK1567 (0.7)			
				▽ 2SK2114 (1.0)			
				▽ 2SK2115 (1.2)			
				▽ 2SK2117 (0.6)			
	200 V to 264 V AC	□ 2SK1880 (6.5)	▲ 2SK1338 (5)	● 2SK1339 (5)	● 2SK1340 (3)	● 2SK1342 (1.2)	● 2SK1342 (1.2)
			□ 2SK2059 (3.8)	▲ 2SK1402A (2.0)	● 2SK1341 (2)	● 2SK1968 (0.68)	● 2SK1573 (0.35)
			▼ 2SK1572 (3.8)	■ 2SK1624 (1.8)	■ 2SK1528 (3)	● 2SK1573 (0.35)	◎ 2SK1770 (0.5)
			■ 2SK1618 (3.8)	▼ 2SK1637 (1.8)	■ 2SK1625 (0.9)		● 2SK1773 (1.5)
			▽ 2SK2144 (3.8)	▼ 2SK1404 (1.0)	▲ 2SK1809 (1.1)		● 2SK1933 (0.9)
				▽ 2SK2097 (1.8)			● 2SK1934 (1.2)
				▽ 2SK2118 (1.0)			

Notes:
1. ═══ : DIII Series
   - - - - : DIV Series
2. Package: □: DPAK ▲: TO-220AB ▼: TO-220FM ●: TO-3P +: TO-92M ▽: TO-220CFM
   △: UPAK ◎: TO-3PFM ■: LDPAK ◇: TO-3PL ◆: HDPAK
3. Values in ( ) show typical “on” resistance $R_{DS(ON)}$ (Ω) typ.
4. Withstand voltages

Input Voltage		Withstand Voltages
AC	100 V to 132 V	300 V, 350 V, 450 V, 500 V
	200 V to 264 V	600 V, 800 V, 900 V, 1000 V

Input Voltage		Withstand Voltages
DC	5 V to 12 V	30 V, 60 V
	24 V, 48 V	100 V, 120 V, 150 V, 200 V, 250 V

5. The chart above does not show L and S indicating long and short leads on DPAK, LDPAK and HDPAK packages.

Type	Input Voltage	Recommended Products in Each Power Range: Up to 10 W	10 W to 30 W	30 W to 50 W	50 W to 100 W	100 W to 200 W	200 W
DC-DC converter	5 V to 12 V DC	△ 2SJ278 (0.6)	□ 2SJ333 (0.1)	■ 2SJ220 (0.065)	■ 2SJ280 (0.03)	▲ 2SK1296 (0.024)	● 2SK2586 (0.007)
		* HAT1002F (0.06)	□ 2SK1949 (0.12)	■ 2SJ297 (0.055)	■ 2SK1919 (0.018)	▲ 2SK1911 (0.018)	● 2SK2554 (0.005)
		* HAT1005F (0.13)	■ 2SJ214 (0.13)	■ 2SK1918 (0.03)	▼ 2SK1952 (0.018)	● 2SK2096 (0.018)	
		* HAT2002F (0.03)	■ 2SJ296 (0.075)	▼ 2SK1951 (0.03)	◎ 2SJ218 (0.033)	■ 2SK2553 (0.007)	
		* HAT2007F (0.05)	■ 2SK1648 (0.055)	▽ 2SK2119 (0.03)	▽ 2SK2120 (0.018)		
	24 V DC	△ 2SJ278 (0.6)	□ 2SJ279 (0.17)	■ 2SJ296 (0.075)	■ 2SJ280 (0.03)	● 2SK1303 (0.05)	● 2SK1304 (0.025)
		□ 2SJ245 (0.2)	□ 2SJ389 (0.1)	■ 2SJ297 (0.055)	■ 2SK1623 (0.065)		
		* HAT1006F (0.1)	□ 2SK1299 (0.25)	▼ 2SK1305 (0.2)	◎ 2SJ218 (0.033)		
		* HAT2006F(0.045)	□ 2SK1254 (0.3)	▼ 2SK1306 (0.1)			
		■ 2SJ279 (0.17)	■ 2SJ214 (0.13)	▼ 2SJ294 (0.055)			
	48 V DC	△ 2SJ186 (8.0)	▼ 2SJ248 (0.25)	▼ 2SJ222 (0.12)	■ 2SK1636 (0.22)	● 2SK1671 (0.075)	◇ 2SK1948 (0.047)
		△ 2SK1334 (2.5)	▼ 2SK1668 (0.4)	▼ 2SK1762 (0.23)	◎ 2SK1670 (0.075)	◎ 2SK1670 (0.075)	
		□ 2SK1838 (5.5)	□ 2SK1335 (0.5)	▼ 2SK1957 (0.33)	● 2SK2075 (0.1)		
		□ 2SJ319 (1.7)	■ 2SK1621 (0.4)	■ 2SK1636 (0.22)			
				▼ 2SK2212 (0.3)			

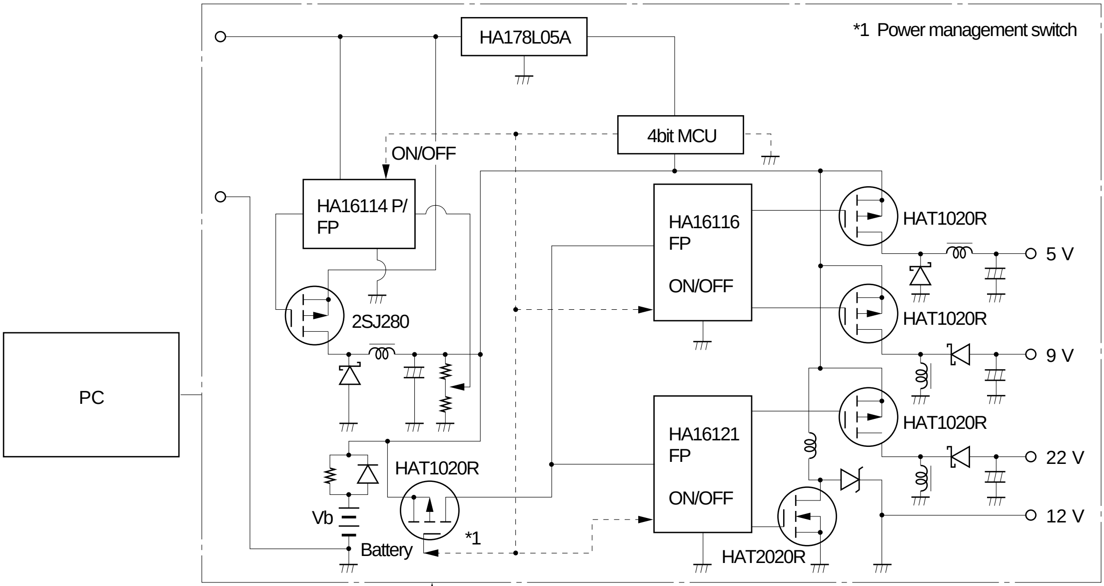
Notes:
1. ——— : DII Series
   ═══ : DIII Series
   - - - - : DIV Series
   — — — : DV Series
2. Package: □: DPAK ▲: TO-220AB ▼: TO-220FM ●: TO-3P +: TO-92M ▽: TO-220CFM
   △: UPAK ◎: TO-3PFM ■: LDPAK ◇: TO-3PL ◆: HDPAK *: SOP-8
3. Values in ( ) show typical “on” resistance $R_{DS(ON)}$ (Ω) typ.
4. Withstand voltages

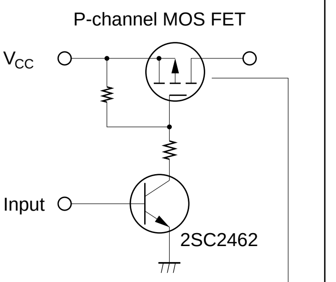
Input Voltage		Withstand Voltages
AC	100 V to 132 V	300 V, 350 V, 450 V, 500 V
	200 V to 264 V	600 V, 800 V, 900 V, 1000 V

Input Voltage		Withstand Voltages
DC	5 V to 12 V	30 V, 60 V
	24 V, 48 V	100 V, 120 V, 150 V, 200 V, 250 V

5. The chart above does not show L and S indicating long and short leads on DPAK, LDPAK and HDPAK packages.

2. Products for notebook personal computer or wordprocessor use





V_{CC} (V)	V_{DSS} (V)	Part Number
5 V to 9 V	12 V to 20 V	2SJ317
		HAT1025R HAT1023R
12 V to 24 V	30 V	HAT1020R
24 V to 40 V	60 V	2SJ389 2SJ280

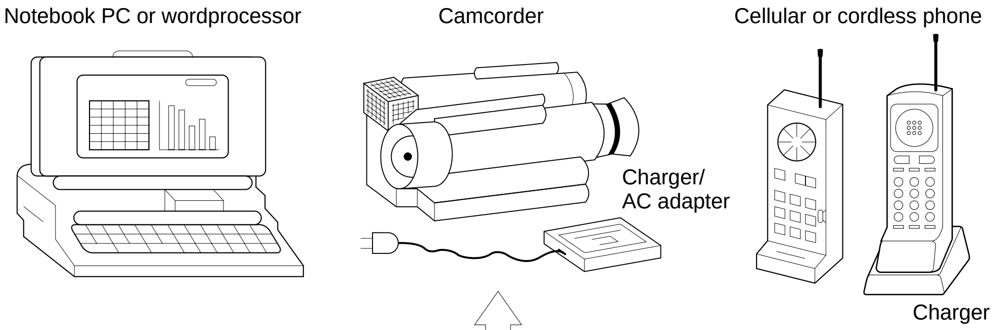
Note: * Power management switch circuit

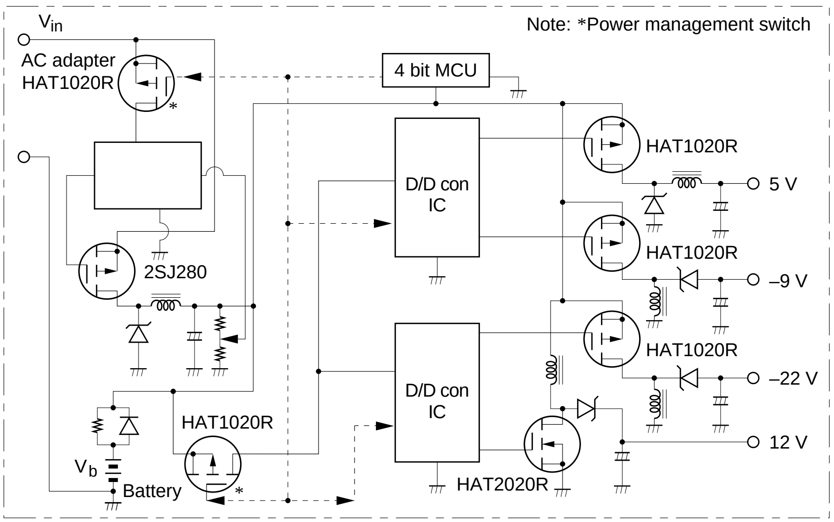
- Lineup

Polarity	Package	Part Number[*1]	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} (W)	4 V $R_{DS(on)}$ (Ω) Typ	4 V $R_{DS(on)}$ (Ω) Max	10 V $R_{DS(on)}$ (Ω) Typ	10 V $R_{DS(on)}$ (Ω) Max	Ciss (pF)	Drive Loss P_d (mW)[*3]
			Maximum Ratings				Electrical Characteristics (typ)					
Pch	UPAK	2SJ317	–12	±7	–2	1[*2]	0.28	0.35	—	—	60	1.2
		2SJ278	–60	±20	–1	1[*2]	0.8	1.2	0.7	0.83	180	1.8
		2SJ450			–1	1[*2]	0.85	1.2	—	—	150	1.8
	DPAK	2SJ234	–30	±20	–2.5	10	0.5	0.7	0.3	0.4	245	1.8
		2SJ246			–7	20	0.18	0.25	0.12	0.17	660	5.4
		2SJ333			–7	20	0.16	0.2	0.12	0.15	750	6.0
		2SJ245	–60		–5	20	0.27	0.38	0.2	0.25	610	5.0
		2SJ279			–5	20	0.23	0.27	0.17	0.2	690	7.0
		2SJ389			–10	30	0.14	0.2	0.1	0.135	910	9.0
	SOP-8 (EIAJ)	HAT1007F	–20	±20	–3.5	1	0.1	0.15	0.06	0.08	730	6.0
		HAT1002F	–30		–3.5	1	0.1	0.13	0.06	0.07	960	7.0
		HAT1005F			–3.5	1	0.095	0.13	0.07	0.09	840	7.0
		HAT1006F	–60		–2.5	1	0.14	0.2	0.1	0.14	910	9.0
	LDPAK	2SJ296	–60	±20	–15	50	0.09	0.12	0.075	0.095	1450	15
		2SJ297			–20	60	0.072	0.095	0.055	0.065	2200	21
		2SJ220			–20	75	0.09	0.13	0.065	0.085	1850	13
		2SJ280			–30	75	0.045	0.06	0.033	0.043	3300	35
	TO-220FM	2SJ293	–60	±20	–15	30	0.09	0.12	0.075	0.095	1450	15
		2SJ294			–20	35	0.075	0.095	0.055	0.065	2200	21
		2SJ295			–30	35	0.045	0.06	0.033	0.043	3300	35
	TO-220CFM	2SJ321	–60	±20	–15	30	0.09	0.12	0.075	0.095	1450	15
		2SJ322			–20	35	0.075	0.095	0.055	0.065	2200	21
		2SJ323			–30	35	0.045	0.06	0.033	0.043	3300	35
Nch	UPAK	2SK1772	30	±20	1	1[*2]	0.6	0.85	0.4	0.6	85	1.3
		2SK2247			2	1[*2]	0.3	0.45	0.22	0.35	177	1.5
		2SK1764	60		2	1[*2]	0.4	0.55	0.3	0.4	140	1.1
		2SK2315			2	1[*2]	0.3	0.45	—	—	175	1.5
	DPAK	2SK1949	60	±20	5	20	0.15	0.2	0.12	0.15	390	3.0
		2SK2334			20	30	0.055	0.07	0.04	0.055	980	9.0
	SOP-8 (EIAJ)	HAT2002F	30	±20	5	1	0.05	0.06	0.03	0.04	860	7.0
		HAT2007F			4	1	0.065	0.11	0.04	0.07	680	5.0
		HAT2006F	60		4	1	0.065	0.075	0.045	0.06	860	9.0
	LDPAK	2SK1918	60	±20	25	50	0.043	0.06	0.03	0.04	1450	15
		2SK1919			40	75	0.023	0.028	0.018	0.022	3530	25
		2SK2553			50	75	0.01	0.016	0.007	0.01	3550	35
	TO-220FM	2SK1094	60	±20	15	25	0.075	0.095	0.055	0.065	860	6.0
		2SK1951			25	30	0.043	0.06	0.03	0.04	1450	15
		2SK1952			40	35	0.023	0.028	0.018	0.022	3530	25
	TO-220CFM	2SK2346	60	±20	20	25	0.05	0.07	0.036	0.045	1130	10
		2SK2119			25	30	0.043	0.06	0.03	0.04	1450	15
		2SK2120			40	35	0.023	0.028	0.018	0.022	3530	25
		2SK2529			50	35	0.01	0.016	0.007	0.01	3550	35

Notes:
1. ( ) indicates a product under development, and subject to specification changes without notice.
2. Allowable value when alumina-ceramic substrate (12.5 × 20 × 0.7 mm) is used.
3. Drive loss when f = 100 kHz and V_{GS} = 5 V. (E.g., if f = 200 kHz, the value is doubled.)

3. Products for power management switch use



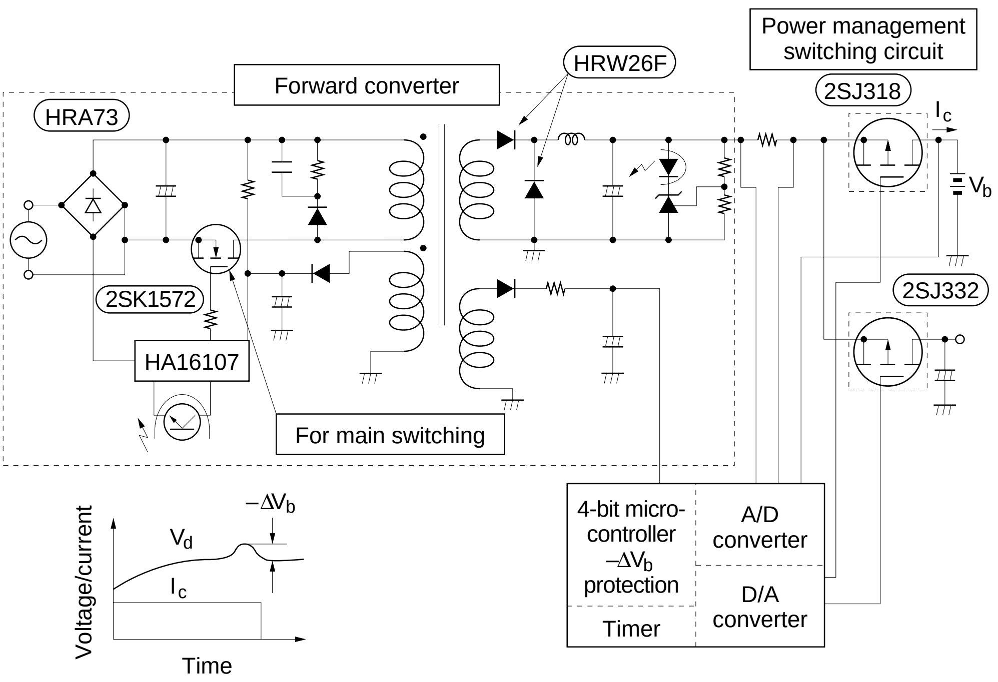


Typical circuit showing application to DC/DC converter power supply of notebook PC

- Lineup

Application	Package	Part Number	Main Characteristics V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) Typ	Max
Notebook PC, wordprocessor, etc.	LDPAK	2SJ280	–60	–30	0.033	0.043
	SOP-8	HAT1002F	–30	–3.5	0.06	0.07
	DPAK	2SJ318	–20	–5	0.09	0.13
		2SJ333	–30	–7	0.1	0.14
	UPAK	2SJ361	–20	–2	0.28	0.4
Camcorder	SOP-8	HAT1001F	–20	–3.5	0.05	0.07
	DPAK	2SJ318		–5	0.09	0.13
		2SJ332		–10	0.05	0.08
Cellular or cordless phone	MPAK	2SJ451	–20	–0.2	2.3	3.5
	UPAK	2SJ317	–12	–2	0.28	0.35
		2SJ361	–20	–2	0.28	0.4
	SOP-8	HAT1001F	–20	–3.5	0.05	0.07
	(EIAJ)	HAT1004F	–20	–2.5	0.1	0.12
	DPAK	2SJ318	–20	–5	0.09	0.13
		2SJ332	–20	–10	0.05	0.08

4. Products for use in AC adapter (camcorder charger, etc.)



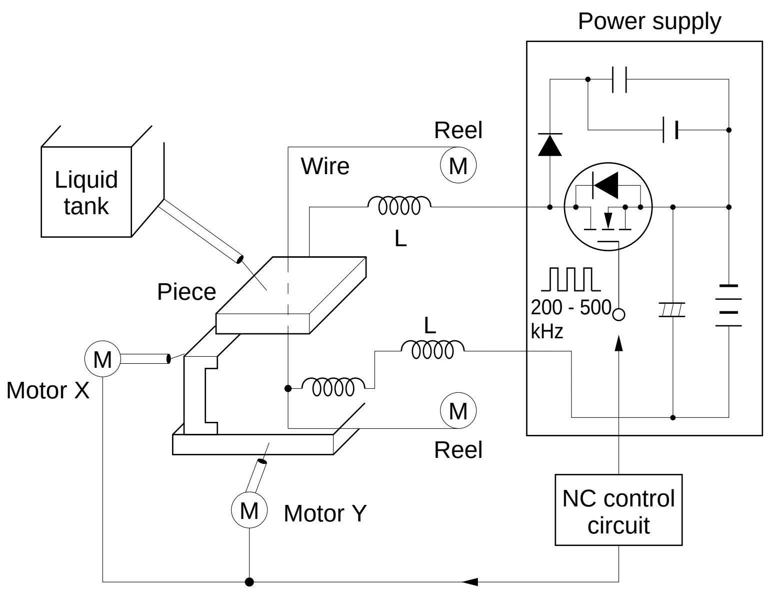
- Lineup

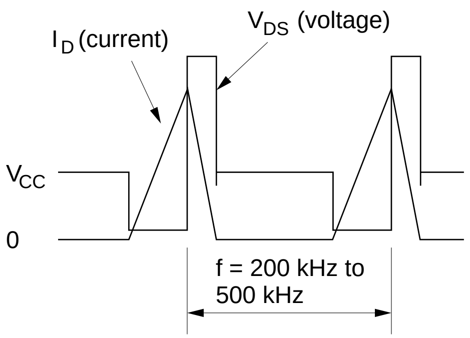
Package	Part Number	Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) Typ	Max	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Drive Loss*1 Pd (mW)
TO-220CFM	2SK2431	450	±30	3	25	2.0	2.8	27	50	330	45
	2SK2423			7	35	0.55	0.7	72	145	1150	150
	2SK2424			8		0.4	0.55	75	180	1450	175
	2SK2114	450	±30	5	35	1.0	1.4	35	80	640	80
	2SK2115	500				1.2	1.5				
	2SK2116	450	±30	7	35	0.6	0.8	70	135	1050	125
	2SK2117	500				0.7	0.9				
	2SK2144	600	±30	3	25	3.8	5.0	33	95	295	40
	2SK2097			4	35	1.8	2.4	38	95	600	80
	2SK2118			5	35	1.1	1.5	57	160	1000	130
TO-220AB	2SK2328	650	±30	7	75	1.0	1.4	65	150	1180	150
	2SK1338	900	±30	2	50	5.0	7.0	45	110	425	85
	2SK1807	900		4	75	3.0	4.0	85	180	740	150
TO-220FM	2SK1862	450	±30	3	25	2.0	2.8	27	50	330	45
	2SK1863	500				2.2	3.0				
	2SK1626	450	±30	5	35	1.0	1.4	35	80	640	80
	2SK1627	500				1.2	1.5				
	2SK1566	450	±30	7	35	0.6	0.8	70	135	1050	125
	2SK1567	500				0.7	0.9				
	2SK1572	600	±30	3	25	3.8	5.0	33	95	295	40
	2SK1637	600		4	35	1.8	2.4	38	95	600	80
	2SK1404	600		5	35	1.1	1.5	57	160	1000	130
	2SK2422	650	±30	4	35	2.0	2.6	38	95	600	80
	2SK1808	900	±30	4	35	3.0	4.0	85	180	740	150
LDPAK	2SK1313	450	±30	5	50	1.0	1.4	35	80	640	80
	2SK1314	500				1.2	1.5				
	2SK1540	450	±30	7	60	0.6	0.8	70	135	1050	125
	2SK1541	500				0.7	0.9				
	2SK1618	600	±30	3	30	3.8	5.0	33	95	295	40
	2SK1624	600		4	50	1.8	2.4	38	95	600	80
	2SK1647	900		2	50	5.0	7.0	45	110	425	85
DPAK	2SK1880	600	±30	1.5	20	6.5	8.0	35	65	250	32
	2SK2059	600		3	20	3.8	5.0	33	95	295	40

Note: 1. Drive loss when f = 500 kHz and V_{GS} = 10 V.

5. Products for machine tool use (electric discharge machine, etc.)

- For electric discharge machine





Power MOS FET operation waveform

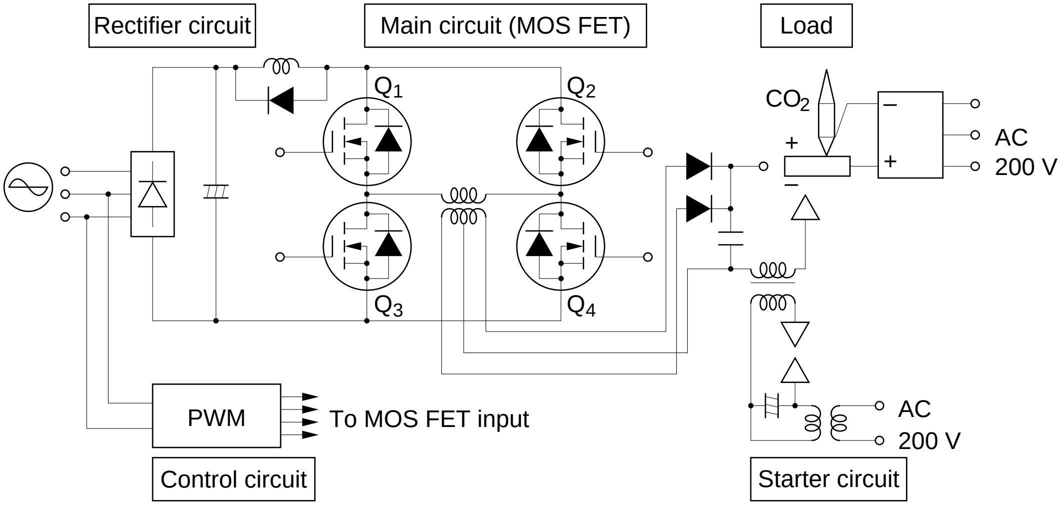
- Lineup

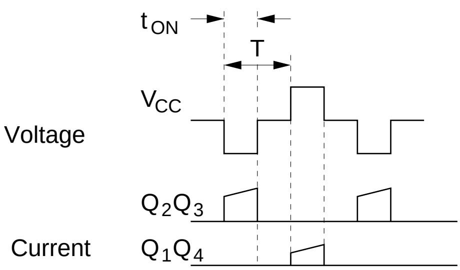
Package	Part Number	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) (V_{GS} = 10 V)	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Remarks
TO-3P	2SK1164	500	±30	11	100	0.55	10	90	180	1450	
	2SK1166	500	±30	12	100	0.45	10	90	180	1450	
	2SK1168	500	±30	15	100	0.3	13	140	220	2050	
	2SK1170	500	±30	20	120	0.22	16	147	290	2800	
	2SK1573	600	±30	15	125	0.35	14	140	340	3150	
TO-3PL	2SK1526	450	±30	40	250	0.11	30	235	580	5800	
	2SK1527	500	±30	40	250	0.12	30	235	580	5800	
	2SK1629	500	±30	30	200	0.22	20	172	300	2800	
	2SK1971	500	±30	35	250	0.19	24	220	450	4320	
Module J/N type	PM5050J	500	±30	50	250	0.14	30	315	390	5800	Contains 2 elements
	PM4575J	450	±30	75	300	0.1	45	410	685	8700	Contains 2 elements
	PM5075J	500	±30	75	300	0.1	45	410	685	8700	Contains 2 elements

Notes: * Allowable value at T_C = 25°C

[ ] : indicates type with built-in high-speed diode. (t_{rr} = 100 ns to 150 ns typ)

- For welding equipment





Power MOS FET operation waveform

• Lineup

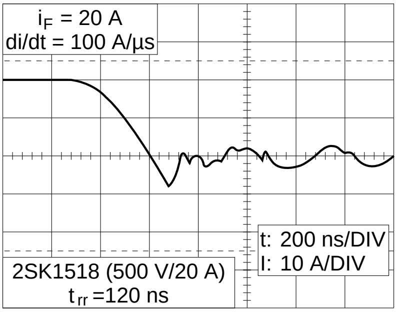
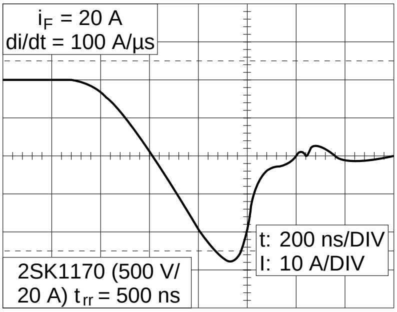
Package	Part Number	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) (V_{GS} = 10 V)	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Remarks
TO-3P	$\boxed{\text{2SK1517}}$	450	±30	20	120	0.20	16	165	345	3050	
	$\boxed{\text{2SK1518}}$	500	±30	20	120	0.22	16	165	345	3050	
TO-3PL	$\boxed{\text{2SK1519}}$	450	±30	30	200	0.11	25	235	615	5800	
	$\boxed{\text{2SK1520}}$	500	±30	30	200	0.12	25	235	615	5800	
	$\boxed{\text{2SK1521}}$	450	±30	50	250	0.08	35	335	850	8700	
	$\boxed{\text{2SK1522}}$	500	±30	50	250	0.085	35	335	850	8700	
	2SK1526	450	±30	40	250	0.11	30	235	580	5800	
	2SK1527	500	±30	40	250	0.12	30	235	580	5800	
	2SK1628	450	±30	30	200	0.20	20	172	300	2800	
	2SK1629	500	±30	30	200	0.22	20	172	300	2800	
	2SK1971	500	±30	35	250	0.19	24	220	450	4320	
Module J/N type	$\boxed{\text{PM4550J}}$	450	±30	50	250	0.14	30	315	390	5800	Contains 2 elements
	$\boxed{\text{PM4575J}}$	450	±30	75	300	0.1	45	410	685	8700	Contains 2 elements

Notes: * Allowable value at T_C = 25°C

$\boxed{}$: indicates type with built-in high-speed diode. (t_{rr} = 100 ns to 150 ns typ)

6. Products for use in uninterruptive power supply (UPS)

- Speed enhancement of built-in diode

Item			DIII-HF (2SK1518)	DIII-H (2SK1170)
Waveform photo showing reverse recovery time (t_{rr}) of built-in diode			 t_{rr} = 120 ns	 t_{rr} = 500 ns
Main characteristics	V_{DSS} (V)		500	500
	I_D (A)		20	20
	$R_{DS(on)}$ (Ω)	Typ	0.22	0.22
		Max	0.27	0.27

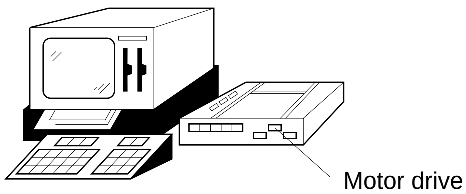
- Lineup

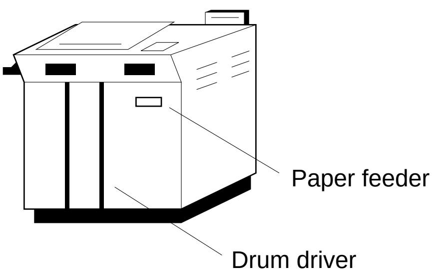
Package	Part Number	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	Electrical Characteristics (typ) 10 V $R_{DS(on)}$ (Ω) Typ	Max	$V_{GSS(OFF)}$ (V)	t_{rr} (ns)
TO-3P	2SK2007	250	±30	20	100	0.12	0.15	2 to 3	120
	2SK1669	250	±30	30	125	0.075	0.095	2 to 3	90
	2SK1515	450	±30	10	100	0.6	0.8	2 to 3	120
	2SK1516	500				0.7	0.9		
	2SK2568	500	±30	12	100	0.45	0.60	2 to 3	120
	2SK1517	450	±30	20	120	0.2	0.25	2 to 3	120
	2SK1518	500				0.22	0.27		
TO-3PL	2SK1947	250	±30	50	200	0.047	0.06	2 to 3	140
	2SK1519	450	±30	30	200	0.11	0.15	2 to 3	120
	2SK1520	500				0.12	0.16		
	2SK1521	450	±30	50	250	0.08	0.10	2 to 3	120
	2SK1522	500				0.085	0.11		
TO-3P · FM	2SK2008	250	±30	20	60	0.12	0.15	2 to 3	120
	2SK1670	250	±30	30	60	0.075	0.095	2 to 3	90
	2SK1405	600	±30	15	60	0.35	0.50	2 to 3	140

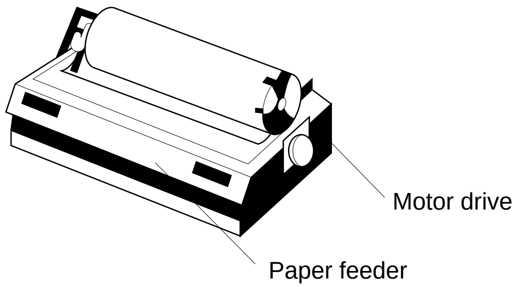
Note: * Allowable value at T_C = 25°C

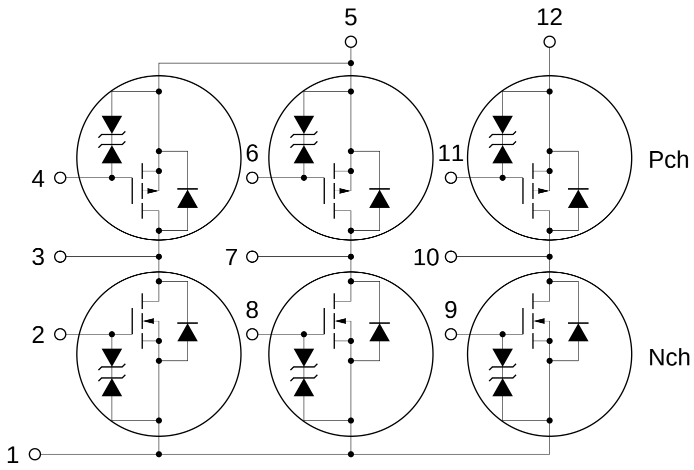
1.2 Motor Drive Use

1. Products for use in office equipment andother small motor driving applications









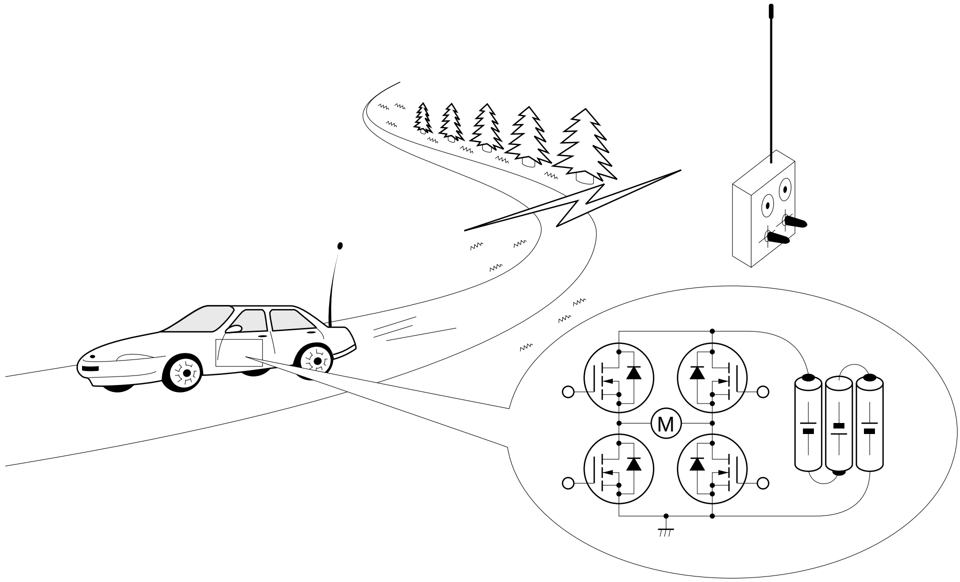
6AM12, 6AM13, 6AM14
Typical equivalent circuit

- Lineup

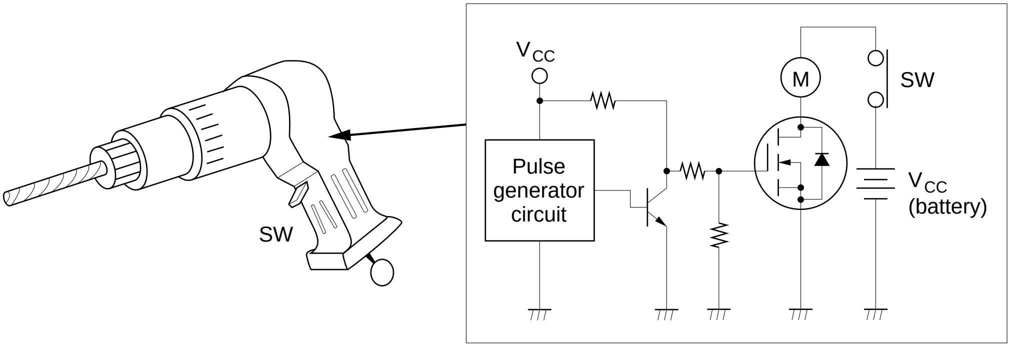
Package	Part Number	Main Characteristics V_{DSS} (V)	I_D (A)	P_{ch} (W)	$R_{DS(on)}$ (10 V) Typ	Max	Built-in Chip (single) N channel	P channel
SP-10	4AM11	60 –60	5 –5	28	0.13 0.15	0.17 0.2	2SK970 × 2	2SJ172 × 2
	4AM12	60 –60	8 –8	28	0.06 0.09	0.075 0.12	2SK971 × 2	2SJ173 × 2
	4AM13	60 –60	3 –3	28	0.25 0.28	0.35 0.4	2SK973 × 2	2SJ182 × 2
SP-12	4AM16	60 –60	8 –8	36	0.13 0.15	0.17 0.2	2SK970 × 2	2SJ172 × 2
	6AM11	60 –60	5 –5	36	0.13 0.15	0.17 0.2	2SK970 × 3	2SJ172 × 3
	4AJ11	–60	–8	28	0.09	0.13	—	2SJ173
	4AK26	60	10	28	0.045	0.065	2SK972 × 4	
SP-12TA	6AM12	60 –60	7 –7	42	0.13 0.15	0.17 0.2	2SK970 × 3	2SJ172 × 3
	6AM13	60 –60	10 –10	42	0.06 0.09	0.075 0.12	2SK971 × 3	2SJ173 × 3
	6AM14	60 –60	7 –7	42	0.11 0.095	0.14 0.13	(no single chip)	(no single chip)
	4AM14	60 –60	8 –8	32	0.13 0.15	0.17 0.2	2SK970 × 2	2SJ172 × 2
	4AM15	200 –200	4 –4	32	0.33 0.7	0.5 0.9	2SK1957 × 2	2SJ410
	4AK23	100	5	32	0.2	0.3	2SK1300 × 4	—

2. Products for use in power tools and radio-controlled models

Radio-controlled model



Power tool

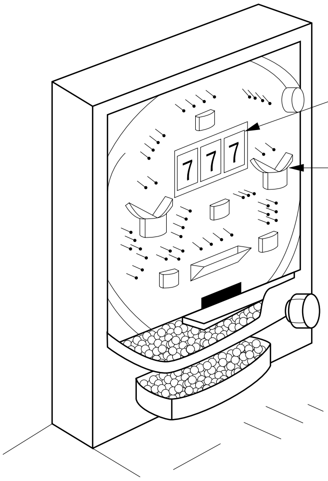


• Lineup

Package	Part Number	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) (V_{GS} = 10 V)	$\lvert y_{fs}\rvert$ (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Remarks
TO-220AB	2SK2205	30	±20	45	75	0.011	38	260	360	3600	DIV
	2SK1911	60	±20	40	75	0.018	35	180	850	3530	DIV
TO-220 CFM	2SK2206	30	±20	45	35	0.011	38	260	360	3600	DIV
	2SK2120	60	±20	40	35	0.018	35	180	850	3530	DIV
	2SK2529	60	±20	50	35	0.007	55	265	830	3550	DV
LDPAK	2SK1919	60	±20	40	75	0.018	35	180	850	3530	DIV
	2SK2204	30	±20	45	75	0.011	38	260	360	3600	DIV
	2SK2553	60	±20	50	75	0.007	55	265	830	3550	DV
TO-3P	2SK2096	60	±20	45	100	0.018	35	180	850	3530	DIV
	2SK2586	60	±20	60	125	0.007	60	295	850	3550	DV
	2SK2554	60	±20	75	150	0.0045	80	480	2100	7700	DV
TO-3PFM	2SK2203	60	±20	50	60	0.007	65	365	560	8330	DIV

Note: * Allowable value at T_C = 25°C

3. Products for game use

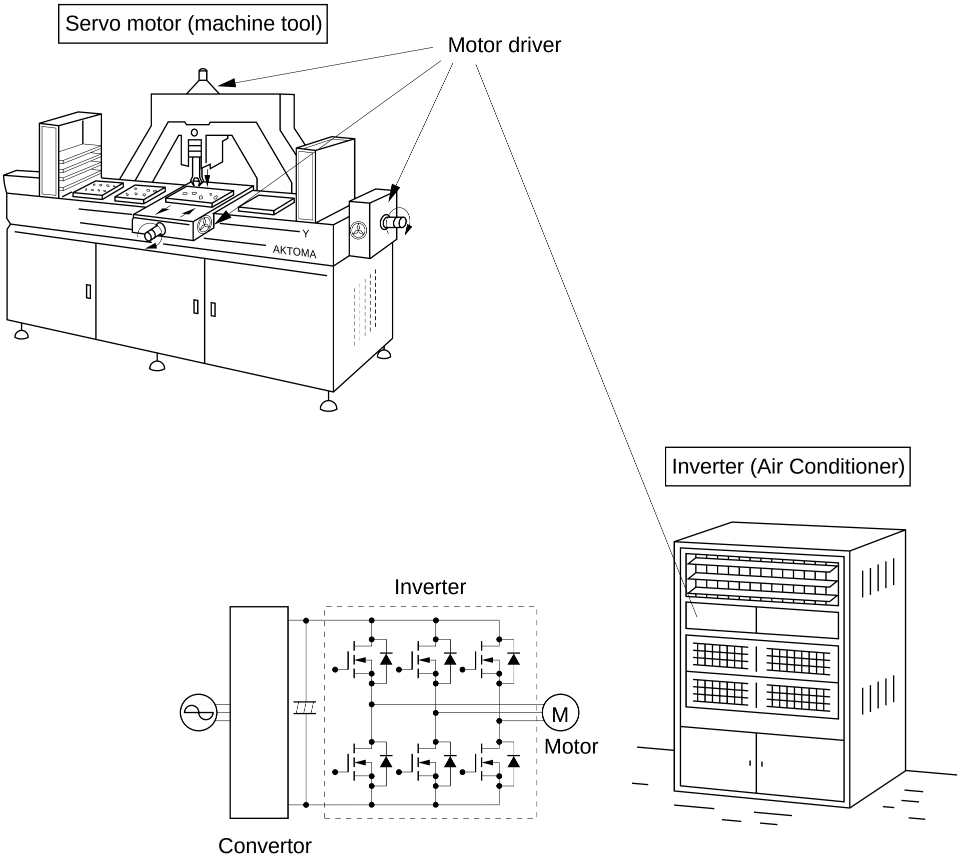


• Lineup

Package	Part Number	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) (V_{GS} = 10 V)	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Remarks
TO-92	2SK1336	60	±20	0.3	0.4	1.3	0.35	6	34	33	4 V drive
TO-92M	2SK975	60	±20	1.5	0.9	0.3	1.5	15	80	140	4 V drive
TO-126	2SK1270	60	±20	2	10	0.3	1.5	15	80	140	4 V drive
DPAK	2SJ182	–60	±20	–3	20	0.28	2.7	35	245	425	4 V drive
	2SK973	60	±20	2	10	0.25	2.0	19	120	240	4 V drive
	2SK974	60	±20	3	20	0.15	4.0	30	255	400	4 V drive
	2SK1299	100	±20	3	20	0.25	4.0	40	220	400	4 V drive
TO-220AB	2SK970	60	±20	10	30	0.12	6.0	60	230	400	4 V drive
	2SK1300	100	±20	10	40	0.2	7.0	65	240	525	4 V drive
TO-220FM	2SK1093	60	±20	10	20	0.12	6.0	60	230	400	4 V drive
	2SK1305	100	±20	10	25	0.2	7.0	65	240	525	4 V drive
SP-10 (array)	4AK18	60	±20	2.5	28	0.25	2.0	19	120	240	4-element array
	4AK22	120	±20	3	28	0.3	4.0	25	195	400	4-element array

Note: * Allowable value at T_C = 25°C

1.3 Servo Motor/Inverter Application

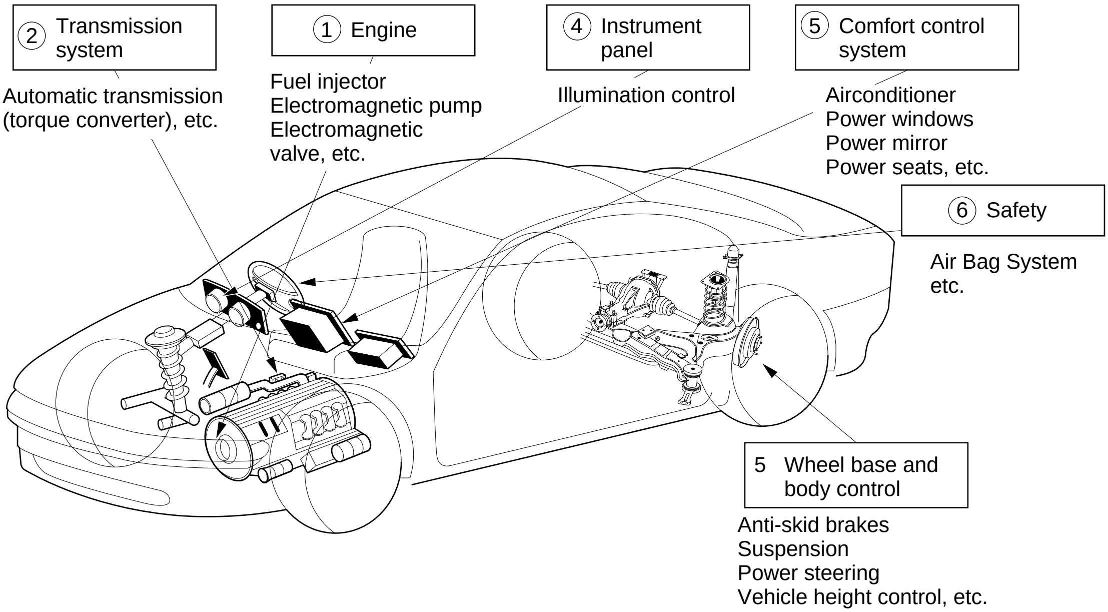


- Lineup

Device		Package	Part No.	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} (W)	Electrical Characteristics 10 V $R_{DS(on)}$ (Ω) Typ	Max	t_{rr}, t_f (ns)
Power MOS FET	High speed built-in diode series	TO-220AB	2SK2408	500	±30	7	60	0.7	0.9	120
		TO-3P	2SK2007	250	±30	20	100	0.12	0.15	120
			2SK1669	250		30	125	0.075	0.095	90
			2SK1515	450		10	100	0.6	0.8	120
			2SK1516	500				0.7	0.9	
			2SK2568	500		12	100	0.45	0.6	120
			2SK1517	450		20	120	0.2	0.25	120
			2SK1518	500				0.22	0.27	
		TO-3PL	2SK1947	250	±30	50	200	0.047	0.06	140
			2SK1519	450		30	200	0.11	0.15	120
			2SK1520	500				0.12	0.16	
			2SK1521	450		50	250	0.08	0.1	120
			2SK1522	500				0.085	0.11	
		TO-3P•FM	2SK2008	250	±30	20	60	0.12	0.15	120
			2SK1670	250		30	60	0.075	0.095	90
			2SK1405	600		15	60	0.35	0.5	140
	Standard series	TO-3P	2SK1671	250	±30	30	125	0.075	0.095	400
		TO-3PL	2SK1948			50	200	0.047	0.06	450
		TO-3P	2SK1170	500	±30	20	120	0.22	0.27	500
		TO-3PL	2SK1629			30	200	0.22	0.27	600
			2SK1671			35	200	0.19	0.23	530
			2SK1527			45	250	0.12	0.16	600
			2SK1837			50	250	0.085	0.11	620

1.4 Automotive Use

Car electrical systems



Advantages of power MOS FET use

($V_{DSS} \leq 150$ V class)

Saturation voltages can be made lower than with bipolar transistors.

(Ex.):

	Bipolar		MOS FET
$V_{CE\,(sat)}$	1.8 V (at 25 A)	$\rightarrow$	0.85 V
	0.85 V (at 5 A)	$\rightarrow$	0.16 V

This means heat sinks can be made smaller or eliminated altogether.

+

Equipment can be driven directly by a 5-V power supply. Lower driving power means simpler circuits.

⇩

Peripheral parts can be made more compact, and fewer parts are needed.

⇩

Smaller, less expensive, and more reliable equipment can be achieved.

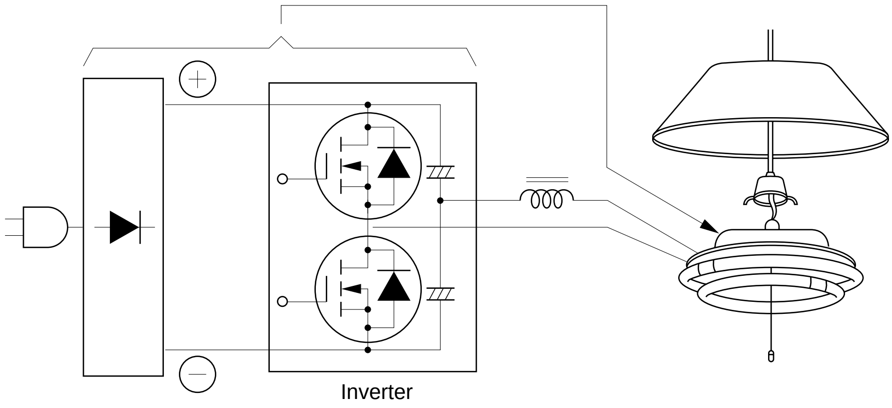
- Lineup

Application Field	Part Number	Package	P_{ch}	V_{DSS}/I_D	R_{on} (typ)
Engine	2SK1318	TO-220FM	35 W	120 V/20 A	0.095 Ω
Fuel injector	2SK1094	TO-220FM	25 W	60 V/15 A	0.055 Ω
Electromagnetic pump	2SK1951	TO-220FM	30 W	60 V/25 A	0.03 Ω
Electromagnetic valve, etc.	2SK1918	LDPAK	50 W	60 V/25 A	0.03 Ω
	2SJ293	TO-220FM	30 W	–60 V/–15 A	0.075 Ω
	2SJ245Ⓛ	DPAK	20 W	–60 V/–5 A	0.2 Ω
	2SJ296	LDPAK	50 W	–60 V/–15 A	0.075 Ω
Transmission system	2SK1951	TO-220FM	30 W	60 V/25 A	0.03 Ω
Automatic transmission (torque converter), etc.	2SJ294	TO-220FM	35 W	–60 V/–20 A	0.055 Ω
	2SJ291	TO-220	75 W	–60 V/–20 A	0.055 Ω
	2SJ279Ⓛ	DPAK	20 W	–60 V/–5 A	0.17 Ω
	2SK1648	LDPAK	50 W	60 V/15 A	0.055 Ω
Wheel base and body control	2SK1307	TO-220FM	35 W	100 V/20 A	0.065 Ω
	2SK1318	TO-220FM	35 W	120 V/20 A	0.095 Ω
Anti-skid brakes	2SK1951	TO-220FM	30 W	60 V/25 A	0.03 Ω
Suspension	2SK974Ⓛ	DPAK	20W	60 V/3 A	0.15 Ω
Power steering	2SK1299Ⓛ	DPAK	20 W	100 V/3 A	0.25 Ω
Vehicle height control, etc.	2SK2096	TO-3P	100 W	60 V/45 A	0.018 Ω
	2SJ217	TO-3P	100 W	–60 V/–45 A	0.033 Ω
	2SJ294	TO-220FM	35 W	–60 V/–20 A	0.055 Ω
	4AK16	SP-10	28 W	60 V/5 A	0.12 Ω
	4AK18	SP-10	28 W	60 V/2.5 A	0.25 Ω
Instrument panel	2SK1910	TO-220	50 W	60 V/25 A	0.03 Ω
Illumination control	2SK971	TO-220	40 W	60 V/15 A	0.055 Ω
	2SK1094	TO-220FM	25 W	60 V/15 A	0.055 Ω
	2SK1951	TO-220FM	30 W	60 V/25 A	0.03 Ω
Comfort control system	2SK1304	TO-3P	100 W	100 V/40 A	0.025 Ω
Airconditioner	2SK2096	TO-3P	100 W	60 V/45 A	0.018 Ω
Power windows	2SK1093	TO-220FM	20 W	60 V/10 A	0.12 Ω
Power mirror	2SK974Ⓛ	DPAK	20 W	60 V/3 A	0.15 Ω
Power seats, etc.	2SK1949Ⓛ	DPAK	20 W	60 V/5 A	0.12 Ω
	2SJ293	TO-220FM	30 W	–60 V/–15 A	0.075 Ω
	2SJ280	LDPAK	75 W	–60 V/–30 A	0.033 Ω
	2SJ217	TO-3P	100 W	–60 V/–45 A	0.033 Ω
	4AK18	SP-10	28 W	60 V/2.5 A	0.25 Ω
	4AK22	SP-10	28 W	120 V/3 A	0.3 Ω

- Lineup (cont)

Application Field	**Part Number**	**Package**	**P_{ch}**	**V_{DSS}/I_D**	**R_{on} (typ)**
Safety	2SK1579	UPAK	1 W	12 V/2 A	0.36 Ω
Air Bag System	2SK975	TO-92Mod	0.9 W	60 V/1.5 A	0.3 Ω
Passive belt etc.	2SK974Ⓛ	DPAK	20 W	60 V/3 A	0.15 Ω
	2SK2334Ⓛ	DPAK	30 W	60 V/20 A	0.04 Ω
	2SJ182Ⓛ	DPAK	20 W	–60 V/–3 A	0.28 Ω
	2SJ389Ⓛ	DPAK	30 W	–60 V/–10 A	0.1 Ω
	2SK1095	TO-220FM	30 W	60 V/25 A	0.033 Ω
	2SK1910	TO-220AB	50 W	60 V/25 A	0.03 Ω
	2SJ220	LDPAK	75 W	–60 V/–20 A	0.065 Ω
	4AM16	SP-10	36 W	60 V/–60 A 8 A/–8 A	0.13/0.15 Ω

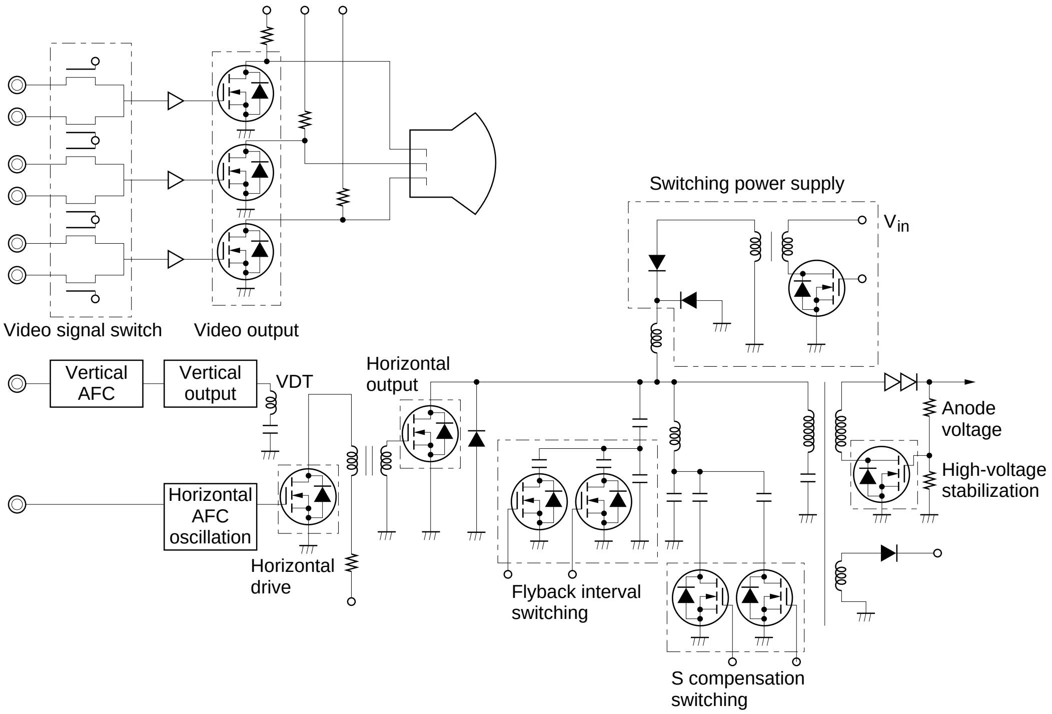
1.5 Lamp Inverter Application



- Lineup

Package	Part Number	Absolute Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} (W)	Electrical Characteristics 10 V $R_{DS(on)}$ (Ω) Typ	Max	V_{GS} (off) (V)
TO-220CFM	2SK2114	450	±30	5	35	1.0	1.4	2 to 3
	2SK2115	500	±30	5	35	1.2	1.5	2 to 3
	2SK2116	450	±30	7	35	0.6	0.8	2 to 3
	2SK2117	500	±30	7	35	0.7	0.9	2 to 3
	2SK2118	600	±30	5	35	1.1	1.5	2 to 3
TO-220FM	2SK1668	250	±30	7	30	0.4	0.55	2 to 3
	2SK1762	250	±30	12	35	0.23	0.35	2 to 3
	2SK1626/27	450/500	±30	5	35	1.0/1.2	1.4/1.5	2 to 3
	2SK1566/67	450/500	±30	7	35	0.6/0.7	0.8/0.9	2 to 3
	2SK1404	600	±30	5	60	1.1	1.5	2 to 3
LDPAK	2SK1313/14	450/500	±30	5	50	1.0/1.2	1.4/1.5	2 to 3
	2SK1540/41	450/500	±30	7	60	0.6/0.7	0.8/0.9	2 to 3
	2SK1315/16	450/500	±30	8	60	0.55/0.6	0.7/0.8	2 to 3
TO-3P	2SK2075	250	±30	20	100	0.105	0.13	2 to 3
	2SK1671	250	±30	30	125	0.075	0.095	2 to 3
	2SK1161/62	450/500	±30	10	100	0.6/0.7	0.8/0.9	2 to 3
	2SK1163/64	450/500	±30	11	100	0.55/0.6	0.7/0.8	2 to 3
	2SK1165/66	450/500	±30	12	100	0.4/0.45	0.55/0.6	2 to 3
TO-3PFM	2SK1831/32	450/500	±30	10	50	0.6/0.7	0.8/0.9	2 to 3
	2SK1328/29	450/500	±30	12	60	0.4/0.5	0.55/0.6	2 to 3
	2SK1405	600	±30	15	60	0.35	0.5	2 to 3

1.6 CRT Display Use



- Lineup

Main Use		Part Number	Package	Maximum Ratings V_{DSS} (V)	I_C (mA)	P_{ch}* (W)	$R_{DS(on)}$ (Ω) Typ	Max
S compensation switching		2SK2212	TO-220FM	200	10	30	0.24	0.30
		2SK2590	TO-220AB	200	10	50	0.33	0.45
Flyback interval switching		2SK1155	TO-220AB	450	5	50	1.0	1.4
		2SK1314	LDPAK	500	5	50	1.2	1.5
		2SK1338	TO-220AB	900	3	50	5.0	7.0
Switching power supply	For 100 V AC	2SK1567	TO-220FM	500	7	60	0.7	0.9
		2SK1831	TO-3PFM	450	10	50	0.6	0.8
		2SK1328		450	12	60	0.4	0.55
		2SK1329		500	12	60	0.4	0.6
	For both 100 V and 200 V AC	2SK1404	TO-220FM	600	5	35	1.1	1.5
		2SK2328	TO-220AB	650	7	75	1.0	1.4
		2SK1341	TO-3P	900	6	100	2.0	3.0
		2SK1342		900	8	100	1.2	1.6
		2SK1775	TO-3PFM	900	8	60	1.2	1.6
Horizontal deflection power supply		2SJ410	TO-220FM	–200	–6	30	0.7	0.85
Horizontal deflection output	High voltage	2SK1773	TO-3P	1000	5	100	1.5	2.0
	Very high voltage	2SK1317	TO-3P	1500	2.5	100	9.0	12
		2SK2225	TO-3PFM	1500	2.0	50	9.0	12
		2SK1835	TO-3P	1500	4	125	4.6	7.0
		2SK2393	TO-3PL	1500	8	200	1.9	2.8
Horizontal deflection drive		2SK1862	TO-220FM	450	3	20	2.0	2.8
		2SK1910	TO-220AB	60	25	50	0.03	0.04
Video output		2SK619	TO-126MOD	70	0.3	10	—	50
		2SK1197	TO-126MOD	100	0.5	20	—	25

* Tc = 25°C

Section 2 Series Lineup

2.1 D Series Lineup (vertical structure)

	I_D (A)										
V_{DS} (V)	0.3 [0.5]	1 [1.5]	2	3 [4]	5	6	7	8	10 [11]	12	13
20			★ 2SJ361 (0.4) ▽ HAT1004F (0.1)	▽ HAT1001F(0.05) ▽ HAT1007F(0.05) ▽ HAT2005(0.05)	■ 2SJ318 (0.085)		□ 2SK2084 (0.04)		□ 2SJ332 (0.05) □ 2SJ387 (0.05)		
30			★ 2SK2247(0.25) ▽ HAT1008F(0.085) ▽ HAT2003F(0.13) □ 2SJ234 (0.3)	▽ HAT1002F (0.06) ▽ HAT1005F (0.07)	▽ HAT2001F (0.035) ▽ HAT2002F (0.03)		□ 2SJ246 (0.13) □ 2SJ333 (0.1) □ 2SK2418 (0.04) □ 2SJ388 (0.06)		□ 2SK2329 (0.03)		
60	× 2SK1336 (1.3) ★ 2SK1697 (1.3)	+ (2SK975) (0.3) ★ 2SJ278 (0.7) ★ 2SJ450 (0.85)	□ 2SK973 (0.25) ◇ 4AK18 (0.25) ★ 2SK1764 (0.3) ▽ HAT1006F (0.11) ★ 2SK2315 (0.4)	□ 2SK974 (0.15) □ 2SJ182 (0.25) □ 2SK1950 (0.2) □ 2SJ235 (0.28)	◇ 4AK16 (0.12) ◇ 4AM11 □ 2SJ245 (0.2) □ 2SJ279 (0.17) □ 2SK1949 (0.12)			◇ 4AK15 (0.055) ◇ 4AM12	▲ 2SK970 (0.12) ◆ 2SJ214 (0.15) ▼ 2SK1093 (0.12) ▽ 2SK2390 (0.07) ▲ 2SJ172 (0.15) ▼ 2SJ175 (0.15) □ 2SJ389 (0.1) ▼ 2SJ390 (0.09)		
100	× 2SK1337 (3.5) ★ 2SK1698 (3.5)	+ 2SK2085 (0.6)		□ 2SK1299 (0.25)				▲ 2SJ247 (0.3)* ▼ 2SJ248 (0.3)*	▲ 2SK1300 (0.2) ▼ 2SK1778 (0.2) ▼ 2SK1305 (0.2)		
120				□ 2SK1254 (0.3)		▼ 2SJ350 (0.5)	▼ 2SK2202 (0.3)				
150									▲ 2SK740 (0.12) ◆ 2SK1620 (0.12)		
200	★ [2SJ186] (8.0)	★ 2SK1334 (2.5)		□ 2SK1335 (0.5)			▼ 2SK1957 (0.33)		▼ 2SK2212 (0.24) ▲ 2SK2590 (0.33)		
250		□ 2SK1838 (5.5)*					▲ 2SK741 (0.4) ◆ 2SK1621 (0.4) ▲ 2SK1667 (0.4) ▼ 2SK1668 (0.4) ▽ 2SK2425 (0.4)		○ 2SK401 (0.3)	▲ 2SK1761 (0.23) ▼ 2SK1762 (0.23) ▽ 2SK2426 (0.23)	
300		□ 2SJ130 (6.0)				▼ 2SK2345 (0.6)	▲ 2SK1400 (0.5)				
350							▲ 2SK1400A (0.6)				
400			▲ 2SJ117 (5.0)								
450		□ [2SK1151] (3.5)		▲ 2SK1153 (2.0) ▼ 2SK1862 (2.0) ▽ 2SK2431 (2.0)	▲ 2SK1155 (1.0) ◆ 2SK1313 (1.0) ▼ 2SK1626 (1.0) ▽ 2SK2114 (1.0)		▲ 2SK1157 (0.6) ◆ 2SK1540 (0.6) ▼ 2SK1566 (0.6) ▽ 2SK2116 (0.7) ▽ 2SK2423 (0.55)	▲ 2SK1159 (0.55) ◆ 2SK1315 (0.55) ▽ 2SK2424 (0.4)	● 2SK1161 (0.6) ● [2SK1163] (0.55) ● 2SK1515 (0.6)	● 2SK1165 (0.40) ◎ 2SK1328 (0.4)	
500		□ [2SK1152] (4.0)		▲ 2SK1154 (2.2) ▼ 2SK1863 (2.2)	▲ 2SK1156 (1.2) ◆ 2SK1314 (1.2) ▼ 2SK1627 (1.2) ▽ 2SK2115 (1.2)		▲ 2SK1158 (0.7) ◆ 2SK1541 (0.7) ▼ 2SK1567 (0.7) ▽ 2SK2117 (0.7) ▲ 2SK2408 (0.7)	▲ 2SK1160 (0.6) ◆ 2SK1316 (0.6) ▽ 2SK2591 (0.45)	● 2SK1162 (0.7) ● [2SK1164] (0.6) ● 2SK1516 (0.6)	● 2SK1166 (0.45) ◎ 2SK1329 (0.45) ● 2SK2568 (0.45)	
600	□ 2SJ181 (15)	□ [2SK1880] (6.5)		▲ [2SK1402] (1.8) ▼ 2SK1572 (3.8) ▼ [2SK1637] (1.8) ◆ 2SK1618 (3.8) ◆ [2SK1624] (1.8) □ 2SK2059 (3.8) ▽ 2SK2144 (3.8) ▽ [2SK2097] (1.8)	▼ 2SK1404 (1.1) ▲ 2SK1809 (1.1) ▽ 2SK2118 (1.1)		◆ 2SK1625 (0.9)	● 2SK1403 (0.9)		● 2SK1968 (0.68)	
650				▲ 2SK1402A (2.0) ▼ 2SK2422 (2.0)			▲ 2SK2328 (1.0)	● 2SK1403A (1.0)			
900			▲ [2SK1338] (5.0) ◆ [2SK1647] (5.0)	● 2SK1339 (5.0) ▲ [2SK1807] (3.0) ▼ [2SK1808] (3.0)	● 2SK1340 (3.0)	● 2SK1341 (2.0) ◎ 2SK1859 (2.0)		● 2SK1342 (1.2) ◎ 2SK1775 (1.2)	● 2SK1933 (0.9)		
1000					● 2SK1773 (1.5)			● 2SK1934 (1.0)			
1500			● 2SK1317 (9)	● [2SK1835] (4.6)							

Notes: 1. ( ) : $R_{DS\,(on)}$ typ (Ω) ▭ : Type with built-in high-speed diode — - — : New device
——— : DII Series - - - - - - : DIII Series : DIV Series
2. □ : DPAK ▼ : TO-220FM ● : TO-3P + : TO-92M ◇ : Module × : TO-92 ◆ : LDPAK
▽ : SOP-8 ◆ : HDPAK ■ : TO-126 ☆ : TO-3PL ▲ : TO-220AB ◎ : TO-3P·FM ★ : UPAK
▽ : TO-220CFM

2.1 D Series Lineup (vertical structure) (cont)

	I_D (A)				
V_{DS} (V)	15 [20]	25	30 [35]	40 [45]	50 [upper 60A]
20					
30				▲ 2SK2205 (0.011) ⊠ 2SK2204 (0.011) ▽ 2SK2206 (0.011)	
60	▲ 2SK971 (0.055) ▼ 2SK1094 (0.055) ▲ 2SJ173 (0.09) ▼ 2SJ176 (0.09) ▲ [2SJ174] (0.065) ▼ [2SJ177] (0.065) ◆ 2SJ219 (0.09) ◆ [2SJ220] (0.065) ◆ 2SK1648 (0.055) ▲ 2SJ290 (0.075) ▲ 2SJ293 (0.075) ◆ 2SJ296 (0.075) ▲ [2SJ291] (0.055) ▼ [2SJ294] (0.055) ◆ [2SJ297] (0.055) ▲ 2SK2175 (0.1) □ 2SK2334 (0.04) ▽ 2SJ321 (0.075) ▽ [2SJ322] (0.05) ▽ [2S2346] (0.036)	▲ 2SK972 (0.03) ▼ 2SK1095 (0.03) ◆ 2SK1622 (0.03) ▲ 2SK1910 (0.03) ▼ 2SK1951 (0.03) ◆ 2SK1918 (0.03) ▽ 2SK2119 (0.03)	▲ 2SK1296 (0.024) ● [2SJ215] (0.045) ◎ [2SJ216] (0.045) ▲ 2SJ292 (0.033) ▼ 2SJ295 (0.033) ◆ 2SJ280 (0.033) ▽ 2SJ323 (0.033)	● 2SK1297 (0.015) ◎ 2SK1298 (0.015) ● [2SJ217] (0.033) ◎ [2SJ218] (0.033) ▲ 2SK1911 (0.018) ▼ 2SK1952 (0.018) ◆ 2SK1919 (0.018) ● 2SK2096 (0.018) ▽ 2SK2120 (0.018)	● 2SK2121 (0.007) ◎ 2SK2203 (0.007) ● 2SJ408 (0.015) ● [2SK2586] (0.007) ● [2SK2554] (0.0045)
100	▲ 2SK1301 (0.1) ▼ 2SK1306 (0.1) ▲ [2SK1302] (0.065) ▼ [2SK1307] (0.065) ■ [2SK1623] (0.065) ▲ [2SJ221] ▼ 2SJ222 (0.12) ■ 2SJ409 (0.12)		● 2SK1303 (0.05)	● 2SK1304 (0.025)	
120					
150					
200					
250	◆ 2SK1636 (0.22) ● 2SK2007 (0.12) ◎ 2SK2008 (0.12)		● 2SK2007 (0.12) ◎ 2SK2008 (0.12) ● 2SK1671 (0.07)		☆ 2SK1947 (0.047) ☆ 2SK1948 (0.047)
300	● 2SK1401 (0.25)				
350	● 2SK1401A (0.3)				
400					
450	● 2SK1167 (0.25) ● [2SK1169] (0.20) ● 2SK1517 (0.20)		◆ PM45302F (0.13) ☆ 2SK1519 (0.11) ☆ 2SK1628 (0.2) ☆ 2SK1526 (0.11)		◇ PM45502C (0.08) ☆ 2SK1521 (0.08) ◆ PM4550J (0.15) ☆ 2SK1836 (0.08)
500	◆ [2SK2174] (0.22) ◆ 2SK2330 (0.3) ● 2SK1168 (0.30) ● [2SK1170] (0.22) ● 2SK1518 (0.22)		◇ PM50302F (0.15) ☆ 2SK1629 (0.22) ☆ 2SK1520 (0.12) ☆ 2SK1527 (0.12) ☆ [2SK1971] (0.19)		◆ PM50502C (0.09) ☆ 2SK1520 (0.085) ◆ PM5050J (0.15) ☆ 2SK1837 (0.09)
600	● 2SK1405 (0.35) ● 2SK1573 (0.35)				
650					
900					
1000					
1500					

Notes: 1. ( ) : $R_{DS\,(on)}$ typ (Ω) ▭ : Type with built-in high-speed diode
——— : DII Series - - - - - - : DIII Series — · — : DIV Series — - - - : DV Series

2. □ : DPAK ▼ : TO-220FM ● : TO-3P + : TO-92M ◇ : Module × : TO-92 ◆ : LDPAK
▽ : SOP-8 ◆ : HDPAK ■ : TO-126 ☆ : TO-3PL ▲ : TO-220AB ◎ : TO-3P·FM ★ : UPAK
▽ : TO-220CFM

2.2 S Series Lineup (lateral structure)

V_{DS} (V)	0.3	0.5	2	4	5	7	8	12	16
120						● 2SK1056 (1.0) ● 2SJ160 (1.0)			
140		▲ 2SK213 (8) ▲ 2SJ76 (10)				● 2SK1057 (1.0) ● 2SJ161 (1.0)			
160		▲ 2SK214 (8) ▲ 2SJ77 (10)				○ 2SK135 (1.0) ○ 2SJ150 (1.0) ● 2SK1058 (1.0) ● 2SJ162 (1.0)			
180		▲ 2SK215 (8) ▲ 2SJ78 (10)	▲ 2SK408 (7) ▲ 2SJ409 (7)	▽ 2SK318 (1.9)			● 2SJ351 (1.0) ● 2SK2220 (1.0)		
200		▲ 2SK216 (8) ▲ 2SJ79 (10)					● 2SJ352 (1.0) ● 2SK2221 (1.0)		

Notes: 1. ( ) : $R_{DS\ (on)}$ typ (Ω)
2. Package: ▲ : TO-220AB ■ : TO-126 ● : TO-3P

Table 2-1 Typical D Series Characteristics

Package	Part Number N-ch	Part Number P-ch	Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) Typ	$R_{DS(on)}$ (Ω) Max	$\|y_{fs}\|$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
TO-3P	2SK1317	—	1500	±20	2.5	100	9.0	12.0	0.75	87	170	990
	2SK1835	—			4	125	4.6	7.0	1.4	105	310	1700
TO-3PFM	2SK2225	—	1500		2	50	9.0	12.0	0.75	67	200	990
HDPAK	2SK2278	—	1500		25	100	9.0	12.0	0.75	87	170	990
TO-3PL	2SK2393	—	1500		8	200	1.9	2.8	3.0	255	385	4370

Notes: 1. Allowable value at $T_C = 25°C$
2. Test conditions: $V_{DS} \geq I_D \times R_{DS(on)}$, $I_D \approx 1/2\ I_D$ max (DC)

Table 2-2 Typical S Series Characteristics

Package	Part Number N-ch	Part Number P-ch	Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*2 (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) Typ	$R_{DS(on)}$ (Ω) Max	$\|y_{fs}\|$*3 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	f_C (MHz)
TO-220AB	2SK213	2SJ76	140*1	±15	0.5	30	8/10	—	0.15/0.1	20	30	90/120	40/30
	2SK214	2SJ77	160*1										
	2SK215	2SJ78	180*1										
	2SK216	2SJ79	200*1	±15	0.5	30	8/10	—	0.15/0.1	20	30	90/120	40/30
TO-3P	2SK1056	2SJ160	120*1	±15	7	100	1.0	1.7	1.0	180/230	60/110	600/900	3/2
	2SK1057	2SJ161	140*1										
	2SK1058	2SJ162	160*1										
	2SK2220	2SJ351	180	±20	8	100	1.0	1.7	1.0	250/320	90/120	800/1200	2/1
	2SK2221	2SJ352	200										

Notes: 1. V_{DSX}
2. Allowable value at $T_C = 25°C$
3. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$, $I_D \approx I_D$ max (DC)

2.3 Power MOS FET DII Series

Table 2-3 Typical DII Series Characteristics

	Part Number		Maximum Ratings				Electrical Characteristics (typ)					
			V_{DSS}	V_{GSS}	I_D	P_{ch}*1	$R_{DS(on)}$ (Ω)		$\|y_{fs}\|$*2	t_{on}	t_{off}	Ciss
Package	N-ch	P-ch	(V)	(V)	(A)	(W)	Typ	Max	(S)	(ns)	(ns)	(pF)
UPAK	2SK1334	2SJ186	200	±20	1/0.5	1	2.5/8.0	3.8/12.0	0.6/0.3	13/12	17/32	80/75
DPAK	—	2SJ130	300	±20	–1	20	6.0	8.5	0.4	35	60	235
	2SK1335	2SJ319	200	±20	3	20	0.5/1.7	0.8/2.3	2.3/1	37/40	50/70	380/330
	—	2SJ181	–600	±15	–0.5	20	15	25	0.45	27	70	220
LDPAK	2SK1620	—	150	±20	10	50	0.12	0.15	7.0	70	110	1200
	2SK1621	—	250		7		0.4	0.55	4.5	50	120	820
TO-220AB	2SK740	—	150	±20	10	50	0.12	0.15	7.0	70	110	1200
	2SK2590	—	200		10	50	0.33	0.45	4.5	65	85	700
	2SK741	—	250		7		0.4	0.55	4.5	50	120	820
TO-220FM	2SJ410	—	–200	±20	–6	30	0.7	0.85	3.5	57	130	920
	2SK1957	—	200		7	30	0.33	0.45	4.5	65	85	700
	2SK2212	—	200		10	30	0.24	0.3	6	98	145	1000

Notes: 1. Allowable value at $T_C = 25°C$
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$, $I_D \approx 1/2\ I_D$ max (DC)

2.4 Power MOS FET DIII Series

1. DIII-L Series

Table 2-5 Typical DIII-L Series Characteristics

Package	Part Number	Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Electrical Characteristics (typ) 4 V $R_{DS(on)}$*2 (Ω) Typ	4 V $R_{DS(on)}$*2 (Ω) Max	10 V $R_{DS(on)}$*2 (Ω) Typ	10 V $R_{DS(on)}$*2 (Ω) Max	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
UPAK	2SJ244	–12	±7	–2	1	0.5	0.7	—	—	1.8	365	1450	130
	2SK1579	12		2	1	0.25	0.35	—	—	2.5	500	1500	110
	2SK1772	30	±20	1	1	0.6	0.85	0.4	0.6	1.0	25	70	85
	2SK1697	60		0.5	1	1.8	2.5	1.3	1.7	0.38	12	32	30
	2SK1698	100		0.3	1	4.5	6.5	3.5	4.5	0.35	6	32	35
	2SK1764	60		2	1	0.4	0.6	0.3	0.45	1.7	18	80	140
TO-92	2SK1336	60	±20	0.3	0.4	1.8	2.5	1.3	1.7	0.35	6	34	33
	2SK1337	100		0.3	0.4	4.0	6.5	3.5	4.5	0.35	6	32	35
TO-92M	2SK975	60	±20	1.5	0.9	0.4	0.55	0.3	0.4	1.5	15	80	140
DPAK	2SJ234	–30	±20	–2.5	10	0.5	0.7	0.3	0.4	1.8	32	157	245
	2SJ246	–30		–7	20	0.21	0.31	0.12	0.17	5.0	65	270	660
	2SJ182	–60		–3	20	0.35	0.50	0.28	0.4	2.7	35	245	425
	2SJ245	–60		–5	20	0.28	0.38	0.2	0.25	3.7	57	260	610
	2SK973	60		2	10	0.4	0.5	0.25	0.35	2.0	19	120	240
	2SK974	60		3	20	0.2	0.25	0.15	0.18	4.0	30	255	400
	2SK1299	100		3	20	0.3	0.45	0.25	0.35	4.0	40	220	400
	2SK1254	120		3	20	0.35	0.55	0.30	0.40	4.0	25	195	420
LDPAK	2SJ214	–60	±20	–10	40	0.18	0.25	0.13	0.18	6.5	73	275	900
	2SJ219			–15	50	0.13	0.17	0.09	0.11	9.5	135	380	1400
	2SJ220			–20	75	0.09	0.13	0.065	0.085	13.0	140	580	1850
	2SJ409	–100		–20	75	0.16	0.22	0.12	0.16	12.0	130	490	1860
	2SK1648	60		15	40	0.075	0.095	0.055	0.065	12.0	80	300	860
	2SK1622			25	50	0.05	0.06	0.033	0.04	20.0	145	450	1400
	2SK1623	100		20	50	0.085	0.12	0.065	0.085	16.0	112	450	1300

Notes: 1. Allowable value at $T_C = 25°C$
2. Test conditions: $R_{DS(on)}$: $V_{GS} = 4$ V, 10 V, $I_D \approx 1/2\ I_D$ max
$|y_{fs}|$: $V_{DS} = 10$ V, $I_D \approx 1/2\ I_D$ max

Table 2-5 Typical DIII-L Series Characteristics (cont)

		Maximum Ratings				Electrical Characteristics (typ)							
						4 V $R_{DS(on)}$*2 (Ω)		10 V $R_{DS(on)}$*2 (Ω)					
Package	Part Number	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Typ	Max	Typ	Max	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
TO-220AB	2SJ172	–60	±20	–10	40	0.18	0.25	0.13	0.18	6.5	73	275	900
	2SJ173			–15	50	0.13	0.17	0.09	0.11	9.5	135	380	1400
	2SJ174			–20	75	0.09	0.13	0.065	0.085	13.0	140	580	1850
	2SK970	60		10	30	0.17	0.22	0.12	0.15	6.0	60	230	400
	2SK971			15	40	0.075	0.095	0.055	0.065	12.0	80	300	860
	2SK972			25	50	0.05	0.06	0.033	0.04	20.0	145	450	1400
	2SK1296			30	75	0.03	0.04	0.024	0.028	27.0	145	615	2250
	2SK1300	100		10	40	0.25	0.35	0.2	0.25	7.0	65	240	525
	2SK1301			15	50	0.13	0.18	0.10	0.13	11.0	80	280	860
	2SK1302			20	50	0.085	0.12	0.065	0.085	16.0	112	450	1300
	2SJ247	–100		–8	40	0.3	0.45	0.25	0.3	5.5	59	225	880
	2SJ221			–20	75	0.16	0.22	0.12	0.16	12.0	130	490	1800
TO-220FM	2SJ175	–60	±20	–10	25	0.18	0.25	0.13	0.18	6.5	73	275	900
	2SJ176			–15	30	0.13	0.17	0.09	0.11	9.5	135	380	1400
	2SJ177			–20	35	0.09	0.13	0.065	0.085	13.0	140	580	1850
	2SK1093	60		10	20	0.17	0.22	0.12	0.15	6.0	60	230	400
	2SK1094			15	25	0.075	0.095	0.055	0.065	12.0	80	300	860
	2SK1095			25	30	0.05	0.06	0.033	0.04	20.0	145	450	1400
	2SK1305	100		10	25	0.25	0.35	0.2	0.25	7.0	65	240	525
	2SK1306			15	30	0.13	0.18	0.10	0.13	11.0	80	280	860
	2SK1307			20	35	0.085	0.12	0.065	0.085	16.0	112	450	1300
	2SK2202	120		7	20	0.35	0.55	0.3	0.4	5.0	59	205	420
	2SJ248	–100		–8	25	0.3	0.45	0.25	0.3	5.5	59	225	880
	2SJ222			–20	35	0.16	0.22	0.12	0.16	12.0	130	490	1800
	2SJ350	–120		–6	20	0.7	0.9	0.5	0.7	5.0	56	250	900
TO-220CFM	2SJ443	–60	±20	–20	75	0.16	0.22	0.12	0.16	12.0	130	490	1800
TO-3P	2SK1297	60	±20	40	100	0.02	0.025	0.015	0.018	35.0	200	1050	3600
	2SJ215	–60		–35	125	0.07	0.09	0.045	0.06	18.0	195	780	2400
	2SJ217			–45	150	0.045	0.06	0.033	0.042	25.0	265	1120	3800
	2SK1303	100		30	100	0.06	0.09	0.05	0.06	22.0	135	585	1750
	2SK1304			40	100	0.03	0.04	0.025	0.03	35.0	195	1030	3500
TO-3PFM	2SK1298	60	±20	40	50	0.02	0.025	0.015	0.018	35.0	200	1050	3600
	2SJ216	–60		–35	50	0.07	0.09	0.045	0.06	18.0	195	780	2400
	2SJ218			–45	60	0.045	0.06	0.033	0.042	25.0	265	1120	3800

Notes: 1. Allowable value at $T_C = 25°C$
2. Test conditions: $R_{DS(on)}$: V_{GS} = 4 V, 10 V, $I_D \approx 1/2\ I_D$ max
$|y_{fs}|$: V_{DS} = 10 V, $I_D \approx 1/2\ I_D$ max

2. DIII-H Series features

Table 2-6 Typical DIII-H Series Characteristics

		Maximum Ratings				Electrical Characteristics (typ)					
						$R_{DS(on)}$ (Ω)					
Package	Part Number	V_{DDS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} *1 (W)	Typ	Max	$\lvert y_{fs}\rvert$ *2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
DPAK	2SK1838	250	±30	1	10	5.5	8.0	0.5	11	15	60
	2SK1151	450		1.5	20	3.5	5.5	1.0	20	30	160
	2SK1152	500				4.0	6.0				
	2SK1880	600				6.5	8.0	1.4	35	65	250
	2SK2059	600		3	20	3.8	5.0	1.2	33	95	295
LDPAK	2SK1636	250	±30	15	75	0.22	0.27	10	109	170	1250
	2SK1869	350		7	50	0.6	0.8	5.0	60	100	635
	2SK1313	450		5	50	1.0	1.4	4.0	35	80	640
	2SK1314	500				1.2	1.5				
	2SK1540	450		7	60	0.6	0.8	6.5	70	135	1050
	2SK1541	500				0.7	0.9				
	2SK1315	450		8	60	0.55	0.7	7.5	72	145	1150
	2SK1316	500				0.6	0.8				
	2SK1618	600		3	30	3.8	5.0	2.0	33	95	295
	2SK1624			4	50	1.8	2.4	3.5	38	95	600
	2SK1625			7	75	0.9	1.3	6.5	65	150	1180
	2SK1647	900		2	50	5.0	7.0	1.5	45	110	425
	2SK1528			4	60	3.0	4.0	2.7	75	180	740
TO-220AB	2SK1667	250	±30	7	50	0.4	0.55	5.0	68	102	690
	2SK1761			12	75	0.23	0.35	8.0	85	144	1100
	2SK1400	300		7	50	0.5	0.7	5.0	60	100	635
	2SK1400A	350				0.6	0.8	5.0			
	2SK1153	450		3	30	2.0	2.8	2.5	27	50	330
	2SK1154	500				2.2	3.0				
	2SK1155	450		5	50	1.0	1.4	4.0	35	80	640
	2SK1156	500				1.2	1.5				

Notes: 1. Allowable value at T_C = 25°C

2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$ max, I_D = 1/2 I_D max

$\boxed{}$: Type with built-in high-speed diode (t_{rr} = 100 ns to 150 ns)

Table 2-6 Typical DIII-H Series Characteristics (cont)

Package	Part Number	Maximum Ratings V_{DDS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) Typ	$R_{DS(on)}$ (Ω) Max	$\|y_{fs}\|$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
TO-220AB	2SK1157	450	±30	7	60	0.6	0.8	6.5	70	135	1050
	2SK1158	500				0.7	0.9				
	$\boxed{\text{2SK2408}}$	500				0.7	0.9	6.0	70	148	1100
	2SK1159	450		8		0.55	0.7	7.5	72	145	1150
	2SK1160	500				0.6	0.8				
	2SK1402	600		4	50	1.8	2.4	3.5	38	95	600
	2SK1402A	650				2.0	2.6				
	2SK2328	650		7	75	1.0	1.4	6.5	65	150	1180
	2SK1809	600		5	60	1.1	1.5	5.0	57	160	1000
	2SK1338	900		2	50	5.0	7.0	1.5	45	110	425
	2SK1807			4	60	3.0	4.0	2.7	75	180	740
TO-220FM	2SK1668	250	±30	7	30	0.4	0.55	5.0	68	102	690
	2SK1762			12	35	0.23	0.35	8.0	85	144	1100
	2SK2345	350		6	35	0.6	0.8	4.5	50	95	635
	2SK1862	450		3	20	2.0	2.8	2.5	27	50	330
	2SK1863	500				2.2	3.0				
	2SK1626	450		5	35	1.0	1.4	4.0	35	80	640
	2SK1627	500				1.2	1.5				
	2SK1566	450		7		0.6	0.8	6.5	70	135	1050
	2SK1567	500				0.7	0.9				
	2SK1572	600		3	25	3.8	5.0	2.0	33	95	295
	2SK1637			4	35	1.8	2.4	3.5	38	95	600
	2SK2422	650				2.0	2.6				
	2SK1404	600		5		1.1	1.5	5.0	57	160	1000
	2SK1808	900		4		3.0	4.0	2.7	75	180	740
TO-220 CFM	2SK2425	250	±30	7	30	0.4	0.55	5.0	68	102	690
	2SK2426	250		12	35	0.23	0.35	8.0	85	144	1100
	2SK2431	450		3	25	2.0	2.8	2.5	27	50	330
	2SK2114	450		5	35	1.0	1.4	4.0	35	80	640
	2SK2115	500				1.2	1.5				
	2SK2116	450		7		0.6	0.8	6.5	70	135	1050
	2SK2117	500				0.7	0.9				

Notes: 1. Allowable value at $T_C = 25°C$

2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$ max, $I_D = 1/2\ I_D$ max

$\boxed{}$: Type with built-in high-speed diode (t_{rr} = 100 ns to 150 ns)

Table 2-6 Typical DIII-H Series Characteristics (cont)

		Maximum Ratings				Electrical Characteristics (typ)					
						$R_{DS(on)}$ (Ω)					
Package	Part Number	V_{DDS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} *1 (W)	Typ	Max	$\lvert y_{fs}\rvert$ *2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
TO-220	2SK2423	450	±30	7	35	0.55	0.7	7.5	72	145	1150
CFM	2SK2424	450		8	35	0.4	0.55	9.0	75	180	1450
	2SK2591	500		8	35	0.45	0.60	9.0	75	180	1450
	2SK2144	600		3	25	3.8	5.0	2.0	33	95	295
	2SK2097			4	35	1.8	2.4	3.5	38	95	600
	2SK2118			5	35	1.1	1.5	5.0	57	160	1000
TO-3P	$\boxed{\text{2SK2007}}$	250	±30	20	100	0.12	0.15	14	155	290	2340
	$\boxed{\text{2SK1669}}$			30	125	0.075	0.095	20	215	420	3100
	2SK1671					0.075	0.095	20	215	380	3000
	2SK2075			20	100	0.105	0.13	14	155	290	2340
	2SK1401	300		8	100	0.25	0.35	9.5	95	155	1250
	2SK1401A	350				0.30	0.40				
	2SK1161	450		10		0.6	0.8	7.0	75	135	1050
	2SK1162	500				0.7	0.9				
	2SK1163	450		11		0.55	0.7	8.0	77	145	1150
	2SK1164	500				0.6	0.8				
	2SK1165	450		12		0.4	0.55	10	90	180	1450
	2SK1166	500				0.45	0.6				
	2SK1167	450		15		0.25	0.36	13	140	220	2050
	2SK1168	500				0.3	0.4				
	2SK1169	450		20	120	0.2	0.25	16	147	290	2800
	2SK1170	500				0.22	0.27				
	$\boxed{\text{2SK1515}}$	450		10	100	0.6	0.8	7.0	80	150	1100
	$\boxed{\text{2SK1516}}$	500				0.7	0.9				
	$\boxed{\text{2SK2568}}$	500		12	100	0.45	0.60	(10)	(100)	(215)	(1550)
	$\boxed{\text{2SK1517}}$	450		20	120	0.20	0.25	16	165	345	3050
	$\boxed{\text{2SK1518}}$	500				0.22	0.27				
	2SK1403	600		8	100	0.9	1.3	6.5	65	150	1180
	2SK1403A	650				1.0	1.4				
	2SK1968	600		12		0.68	0.88	10	95	210	1800
	2SK1573			15	120	0.35	0.5	14	140	340	3150

Notes: 1. Allowable value at $T_C = 25°C$
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$ max, $I_D = 1/2\ I_D$ max
$\boxed{}$: Type with built-in high-speed diode (t_{rr} = 100 ns to 150 ns)

Table 2-6 Typical DIII-H Series Characteristics (cont)

		Maximum Ratings				Electrical Characteristics (typ)					
						$R_{DS(on)}$ (Ω)					
Package	Part Number	V_{DDS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Typ	Max	$\|y_{fs}\|$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)
TO-3P	2SK1339	900	±30	3	80	5.0	7.0	1.9	50	105	425
	2SK1340			5	100	3.0	4.0	3.2	85	180	740
	2SK1341			6		2.0	3.0	3.7	100	225	980
	2SK1342			8		1.2	1.6	5.5	160	315	1730
	2SK1933			10	150	0.9	1.2	7	170	455	2620
	2SK1773	1000		5	100	1.5	2.0	5.0	135	345	1700
	2SK1934			8	150	1.2	1.6	6	170	505	2690
TO-3PFM	$\boxed{\text{2SK2008}}$	250	±30	20	60	0.12	0.15	14	155	290	2340
	$\boxed{\text{2SK1670}}$			30		0.075	0.095	20	215	420	3100
	2SK1831	450		10	50	0.6	0.8	7.0	75	135	1050
	2SK1832	500				0.7	0.9				
	2SK1328	450		12	60	0.40	0.55	10	90	180	1450
	2SK1329	500				0.45	0.60				
	$\boxed{\text{2SK1405}}$	600		15		0.35	0.50	14	155	340	3150
	2SK1859	900		6		2.0	3.0	3.7	100	225	980
	2SK1775			8		1.2	1.6	5.5	160	315	1730
HDPAK	2SK2330	500	±30	15	100	0.3	0.4	13	140	220	2050
	2SK2174	500		20	120	0.22	0.27	16	147	290	2800
TO-3PL	$\boxed{\text{2SK1947}}$	250	±30	50	200	0.047	0.06	30	345	620	5810
	2SK1948								330		5830
	$\boxed{\text{2SK1519}}$	450		30		0.11	0.15	25	235	615	5800
	$\boxed{\text{2SK1520}}$	500				0.12	0.16				
	$\boxed{\text{2SK1521}}$	450		50	250	0.08	0.10	35	335	850	8700
	$\boxed{\text{2SK1522}}$	500				0.085	0.11				
	2SK1628	450		30	200	0.2	0.25	20	172	300	2800
	2SK1629	500				0.22	0.27				
	2SK1971	500		35		0.19	0.23	24	220	450	4320
	2SK1526	450		40	250	0.11	0.15	30	235	580	5800
	2SK1527	500				0.12	0.16				
	2SK1836	450		50		0.08	0.1	35	330	770	8150
	2SK1837	500				0.085	0.11				

Notes: 1. Allowable value at T_C = 25°C
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$ max, I_D = 1/2 I_D max
$\boxed{}$: Type with built-in high-speed diode (t_{rr} = 100 ns to 150 ns)

2.5 Power MOS FET DIV Series

Features	Main Applications
• Low “on” resistance (30% less than DIII Series for same die area), P ch/N ch complementary	• DC/DC converter Notebook PCs, wordprocessors, games, etc.
• Low driving voltage 4 V: for direct driving of microcomputers and TTL 2.5 V: for battery-driven (3 V) systems	• Compact motor drive Copiers, printers, FAX, etc.
• Strongly resistant to load surges (avalanche)	• Automotive Relays, solenoid drives, power steering, power mirror, ABS inverter, etc.
• Built-in diode highly resistant to diode breakdown	• Other uses Power tools, radio-controlled model motors, diode substitute, etc.

Table 2-7 Typical DIV-L Series Characteristics

		Maximum Ratings				Electrical Characteristics (typ)								
						4 V $R_{DS(on)}$*2 (Ω)		10 V $R_{DS(on)}$*2 (Ω)						
Package	Part Number	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Typ	Max	Typ	Max	$\lvert y_{fs}\rvert$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Note
MPAK	2SJ399	–30	±20	–0.2	0.15	2.7	5.0	2.0	3.0	—	2700	16330	1.1	
	2SJ451*3	–20		–0.2	0.15	2.3	3.5	—	—	0.23	850	5800	2.4	
	2SJ452*3	–50		–0.2	0.15	5.0	7.0	—	—	0.19	1750	14000	1.1	
	2SK2373	30		0.2	0.15	1.4	2.5	1.0	1.4	—	175	1060	17.8	
	2SK2569*3	50		0.2	0.15	1.9	2.6	—	—	( )	130	1500	( )	
	(2SK2570)*3	20	±10	0.2	0.15	1.0	1.3	—	—	( )	( )	( )	( )	
UPAK	2SJ317	–12	±7	–2	1	0.28	0.35	—	—	2	590	2350	60	
	2SJ361*3	–20	±20	–2	1	0.85	1.5	0.28	0.4	0.3	2000	14330	3.2	
	2SJ363	–30		–2	1	0.6	0.75	0.35	0.45	2.0	9650	40800	2.1	
	2SJ278	–60		–1	1	0.8	1.2	0.7	0.83	1.0	15	60	180	
	2SJ450*3	–60		–1	1	0.85	1.2	—	—	1.0	15	85	150	
	2SK2247	30		2	1	0.30	0.45	0.22	0.35	1.9	22	70	177	
	2SK2315*3	60		2	1	0.35	0.45	—	—	1.8	21	85	173	
TO-92M	2SJ386	–30	±20	–3	0.9	0.55	0.8	0.3	0.4	1.7	36	105	177	
DPAK	2SJ318	–20	±20	–5	20	0.14	0.19	0.09	0.13	5.5	70	150	580	
	2SJ332			–10	20	0.09	0.14	0.05	0.08	9	83	190	730	
	2SJ333	–30		–7	20	0.16	0.2	0.12	0.15	6	60	220	750	
	2SJ387*3	–20	±10	–10	20	0.05	0.07	—	—	12	345	775	1170	
	2SJ388*3	–30	±20	–10	20	0.12	0.2	0.06	0.08	8	75	490	970	
	2SK2084	20		7	20	0.058	0.075	0.04	0.053	9	75	180	800	
	2SJ279	–60		–5	20	0.20	0.27	0.17	0.2	5.0	50	200	690	
	2SJ389	–60		–10	30	0.14	0.2	0.1	0.135	8	100	365	910	

Notes: ( ) indicates a product under development, and subject to specification changes without notice.
1. Allowable value at $T_C = 25°C$
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$, $I_D = 1/2\ I_D$ max
3. 2.5-V driving

Table 2-7 Typical DIV-L Series Characteristics (cont)

		Maximum Ratings				Electrical Characteristics (typ)								
						4 V $R_{DS(on)}$*2 (Ω)		10 V $R_{DS(on)}$*2 (Ω)						
Package	Part Number	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Typ	Max	Typ	Max	$\|y_{fs}\|$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Note
DPAK	2SK1949	60	±20	5	20	0.15	0.2	0.12	0.15	5	70	110	390	
	2SK1950*3			3	10	0.3	0.45	0.2	0.25	10	60	160	350	
	2SK2329*3	30	±10	10	20	0.03	0.04	—	—	18	165	350	1250	
	2SK2334	60	±20	20	30	0.055	0.07	0.04	0.055	15	104	305	980	
	2SK2418*3	20	±10	7	20	0.04	0.05	—	—	12	105	270	810	
FP-8D	HAT1001F*3	–20	±10	–3.5	1	0.05	0.07	—	—	8.0	265	790	1170	
(EIAJ	HAT1002F	–30	±20	–3.5	1	0.1	0.13	0.06	0.07	6.0	335	140	960	
SOP-8)	HAT1004F*3	–20	±10	–2.5	1.5	0.1	0.12	—	—	5.5	153	270	750	Pch×2
	HAT1005F*3	–30	±20	–3.5	1	0.095	0.13	0.07	0.09	6.0	135	220	840	
	HAT1006F	–60		–2.5	1	0.14	0.2	0.1	0.14	5.5	225	190	910	
	HAT1007F	–20		–3.5	1	0.1	0.15	0.06	0.08	5.0	193	140	730	
	HAT1008F	–30		–2.5	1	0.12	0.2	0.075	0.12	4.5	179	110	670	
	HAT1009F	–30	±10	–2.5	1.5	0.12	0.16	—	—	5.0	116	220	720	Pch×2
	HAT2001F*3	30		5	1	0.035	0.045	—	—	12.0	120	340	1250	
	HAT2002F	30	±20	5	1	0.05	0.06	0.03	0.04	8.0	220	165	860	
	HAT2003F*3	30	±10	2.5	1.5	0.1	0.15	—	—	5.0	95	140	380	Nch×2
	HAT2004F*3	15		3.5	1.5	0.055	0.07	—	—	7.5	112	225	620	Nch×2
	HAT2005F*3	20		4	1	0.05	0.065	—	—	10.0	115	270	810	
	HAT2006F	60	±20	4	1	0.065	0.075	0.045	0.06	6.5	185	160	860	
	HAT2007F	30		4	1	0.065	0.11	0.04	0.07	5.0	125	100	680	
	HAT2008F*3	20	±10	3.5	1.5	0.055	0.075	—	—	7.5	103	210	620	Nch×2
	HAT2009F*3	30		3.5	1.5	0.065	0.08	—	—	7.0	97	200	610	Nch×2
	HAT2010F	30	±20	3.5	1.5	0.09	0.13	0.06	0.075	4.5	110	85	470	Nch×2
	HAT3001F*3	30 –30	±10	2.5 –2.5	1.5	0.1 0.12	0.15 0.16	— —	— —	4.0 5.0	95 116	140 220	380 720	Nch/ Pch in
TO-220AB	2SK2205	–30	±20	45	75	0.016	0.022	0.011	0.015	38	260	795	3600	
	2SK2175	60		15	30	0.13	0.18	0.1	0.13	8	75	180	390	
	2SJ290	–60		–15	50	0.09	0.12	0.075	0.095	12	105	390	1450	
	2SJ291			–20	60	0.072	0.095	0.055	0.065	17	155	500	2200	
	2SJ292			–30	75	0.045	0.06	0.033	0.043	25	200	740	3300	
	2SK1910	60		25	50	0.043	0.06	0.03	0.04	21	130	370	1450	
	2SK1911			40	75	0.023	0.028	0.018	0.022	35	180	850	3530	

Notes: ( ) indicates a product under development, and subject to specification changes without notice.

1. Allowable value at T_C = 25°C
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$, I_D = 1/2 I_D max
3. 2.5-V driving

Table 2-7 Typical DIV-L Series Characteristics (cont)

		Maximum Ratings				Electrical Characteristics (typ)								
						4 V $R_{DS(on)}$*2 (Ω)		10 V $R_{DS(on)}$*2 (Ω)						
Package	Part Number	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Typ	Max	Typ	Max	$\|y_{fs}\|$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Note
TO-220FM	2SJ390	–60	±20	–10	25	0.13	0.19	0.09	0.12	9	78	285	1060	
	2SJ293			–15	30	0.09	0.15	0.075	0.095	12	105	390	1450	
	2SJ294			–20	35	0.075	0.095	0.055	0.065	17	155	500	2200	
	2SJ295			–30	35	0.045	0.06	0.033	0.043	25	200	740	3300	
	2SK1951	60		25	35	0.043	0.06	0.03	0.04	21	130	370	1450	
	2SK1952			40	35	0.023	0.028	0.018	0.022	35	180	850	3530	
TO-220 CFM	2SJ321	–60	±20	–15	30	0.09	0.15	0.075	0.095	12	105	390	1450	
	2SJ322			–20	35	0.075	0.095	0.055	0.065	17	150	500	2200	
	2SJ323			–30	35	0.045	0.06	0.03	0.04	25	130	370	3300	
	2SK2206	30		45	35	0.016	0.022	0.011	0.015	38	260	795	3600	
	2SK2390	60		12	20	0.11	0.15	0.075	0.09	8	65	170	450	
	2SK2346			20	25	0.05	0.07	0.036	0.05	17	105	310	1130	
	2SK2119			25	30	0.043	0.06	0.03	0.04	21	130	370	1450	
	2SK2120			40	35	0.023	0.028	0.018	0.022	35	183	670	3530	
LDPAK	2SK2204	30	±20	45	75	0.016	0.022	0.011	0.015	38	260	795	3600	
	2SJ296	–60		–15	50	0.09	0.15	0.075	0.095	12	105	390	1470	
	2SJ384*3			–15	50	0.12	0.19	0.07	0.1	14	91	540	2170	
	2SJ297			–20	60	0.075	0.095	0.055	0.065	17	155	500	2200	
	2SJ280			–30	75	0.045	0.06	0.033	0.043	25	200	740	3300	
	2SK2322*3	60		15	50	0.08	0.15	0.04	0.05	14	220	250	1600	
	2SK1918			25	50	0.043	0.06	0.03	0.04	21	130	370	1450	
	2SK1919			40	75	0.023	0.028	0.018	0.022	35	180	850	3530	
TO-3P	2SK2096	60	±20	45	100	0.023	0.028	0.018	0.022	35	183	670	3530	
	2SK2121			50	100	0.009	0.013	0.007	0.01	65	360	1955	8330	
HDPAK	2SJ408	–60	±20	–50	100	0.02	0.028	0.015	0.02	50	395	1770	8200	
TO-3PFM	2SK2203	60	±20	50	60	0.009	0.013	0.007	0.01	65	360	1955	8330	

Notes: ( ) indicates a product under development, and subject to specification changes without notice.
1. Allowable value at T_C = 25°C
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$, I_D = 1/2 I_D max
3. 2.5-V driving

2.6 Power MOS FET DV Series

Features

- Super Low "on" resistance; 50% Less $R_{DS(on)}$ than DIV Series for same die area.
- Low driving Gate voltage
  4 V and 2.5 V Gate Drive capability for direct driving of microcomputers and TTL, and 3 V Battery source.
- Low Gate charge capability: 50% Less Qg than DIV Series for same $R_{DS(on)}$ characteristics.
- Pch/Nch complementary
- High avalanche destruction capability

Table 2-8 Typical DV-L Series Characteristics

		Maximum Ratings				Electrical Characteristics (typ)								
						4 V $R_{DS(on)}$ (Ω)*2		10 V $R_{DS(on)}$*2						
Package	Part Number	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}*1 (W)	Typ	Max	Typ	Max	$\|y_{fs}\|$*2 (S)	t_{on} (ns)	t_{off} (ns)	Ciss (pF)	Note
FP-8DA	(HAT1020R)	–30	±20	–4.5	2	0.09	0.13	0.05	0.07	(8.0)	(235)	(95)	(670)	
(JEDEC	(HAT1023R)*3	–20	±10	–6.5	2	0.023	0.04	—	—	(10.0)	(320)	(750)	(1200)	
SOP-8)	(HAT1024R)	–30	±20	–2.5	2	0.25	0.4	0.18	0.25	(4.0)	(80)	(35)	(250)	Pch×2
	(HAT1025R)*3	–20	±10	–4	2	0.09	0.11	—	—	(6.0)	(110)	(210)	(530)	Pch×2
	(HAT2016R)	30	±20	5	2	0.055	0.08	0.04	0.05	(6.5)	(115)	(75)	(350)	Nch×2
	(HAT2020R)	30	±20	7	2	0.04	0.05	0.026	0.03	(10.0)	(180)	(125)	(570)	
	(HAT2022R)	30	±20	10	2	0.016	0.02	0.011	0.0135	(18.0)	(255)	(260)	(1250)	
	(HAT3004R)	30 –30	±20	3.5 –2.5	2	0.11 0.2	0.15 0.4	0.08 0.13	0.1 0.25	(3.0) (3.0)	(70) (70)	(45) (45)	(180) (250)	Nch/ Pch in
TO-220CFM	2SK2529	60	±20	50	35	10 m	16 m	7 m	10 m	55	265	830	3550	
LDPAK	2SK2553	60	±20	50	75	10 m	16 m	7 m	10 m	55	265	830	3550	
TO-3P	2SK2586	60	±20	60	125	10 m	16 m	7 m	10 m	60	295	850	3550	
	2SK2554	60	±20	75	150	5.8 m	10 m	4.5 m	6 m	80	480	2100	7700	

Notes: ( ) indicates a product under development, and subject to specification changes without notice.
1. Allowable value at T_C = 25°C
2. Test conditions: $V_{DS} > I_D \times R_{DS(on)}$, I_D = 1/2 I_D max
3. 2.5-V driving

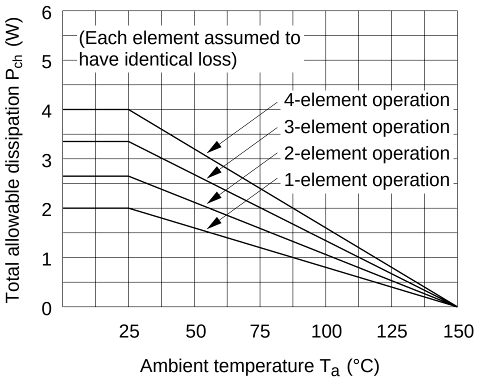
2.7 Power MOS FET Array Series

Table 2-9 Typical Characteristics of Power MOS FET Array Series

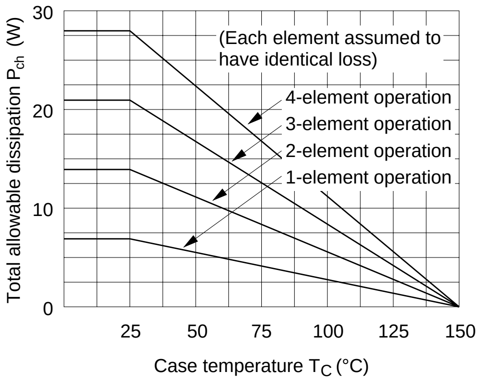
Package		Part Number	Maximum Ratings V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}* (W)	Electrical Characteristics (typ) 4 V $R_{DS(on)}$ (Ω) Typ	4 V $R_{DS(on)}$ (Ω) Max	10 V $R_{DS(on)}$ (Ω) Typ	10 V $R_{DS(on)}$ (Ω) Max	$\|y_{fs}\|$ (S)	t_{on} (ns)	t_{off} (ns)	Equivalent Single Device
SP-10	(A)	4AK17	60	±20	10	28	0.04	0.065	0.033	0.045	17	110	470	2SK972
		4AK15			8		0.075	0.095	0.055	0.07	12	80	300	2SK971
		4AK16			5		0.17	0.25	0.12	0.18	6	60	230	2SK970
		4AK18			2.5		0.4	0.53	0.25	0.38	2	19	120	2SK973
	(B)	4AM13	60	±20	3	28	0.35	0.5	0.25	0.35	2.5	24	120	2SK973
			–60		–3		0.4	0.55	0.28	0.40	2.5	30	260	2SJ182
		4AM11	60	±20	5	28	0.18	0.24	0.13	0.17	4.5	35	245	2SK970
			–60		–5		0.20	0.27	0.15	0.2	5.0	43	265	2SJ172
		4AM12	60	±20	8	28	0.08	0.11	0.06	0.075	9.0	55	300	2SK971
			–60		–8		0.135	0.18	0.09	0.12	7.5	100	400	2SJ173
	(A)	4AK20	100	±20	5	28	0.25	0.35	0.2	0.25	5.0	40	250	2SK1300
		4AK21	100	±20	8	28	0.09	0.125	0.07	0.09	10	72	440	2SK1302
		4AK22	120	±20	3	28	0.35	0.55	0.3	0.4	3.5	25	200	2SK1254
SP-12TA	(E)	4AM14	60	±20	8	32	0.18	0.24	0.13	0.17	4.5	35	245	2SK970
			–60		–8		0.20	0.27	0.15	0.20	5.0	43	265	2SJ172
	(D)	6AM12	60	±20	7	42	0.19	0.24	0.13	0.17	5.5	50	230	2SK970
			–60		–7		0.20	0.27	0.15	0.20	6.0	58	265	2SJ172
		6AM13	60	±20	10	42	0.08	0.11	0.06	0.075	9.5	60	290	2SK971
			–60		–10		0.12	0.18	0.09	0.12	8.0	115	410	2SJ173
		6AM14	60	±20	7	42	0.14	0.2	0.11	0.14	6.5	100	360	—
			–60		–7		0.12	0.16	0.095	0.13	8.0	85	420	—
SP-12	(G)	4AJ11	–60	±20	–8	28	0.12	0.17	0.09	0.13	7.7	135	380	2SJ173
	(F)	4AK26	60		10		0.056	0.075	0.045	0.06	12	110	470	2SK972
	(E)	4AM16	60		8	36	0.18	0.24	0.13	0.17	4.5	35	245	2SK970
			–60		–8		0.2	0.27	0.15	0.2	5.0	43	265	2SJ172
	(D)	6AM11	60	±20	5	36	0.18	0.24	0.13	0.17	4.5	35	245	2SK970
			–60		–5		0.20	0.27	0.15	0.20	5.0	43	265	2SJ172
SP-10	(A)	4AK25	60	±20	1.5	24	0.47	0.60	0.35	0.45	1.5	15	80	2SK975
SP-12TA	(F)	4AK23	100	±20	5	32	0.25	0.40	0.20	0.30	5.5	37	245	2SK1300
	(E)	4AM15	200		4	32	—	—	0.33	0.50	2.5	50	105	2SK1957
			–200		–4		—	—	0.70	0.90	3.0	70	145	—

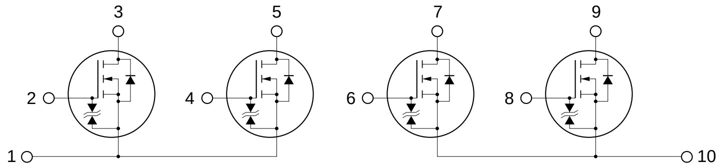
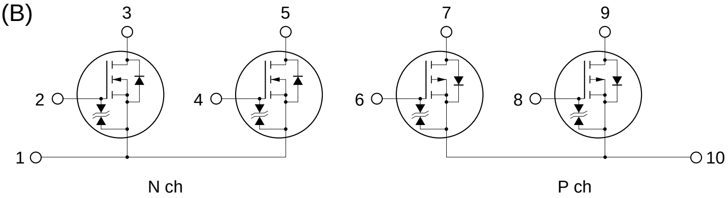
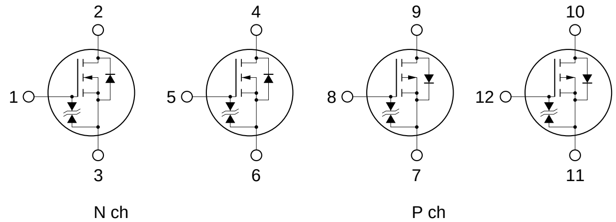
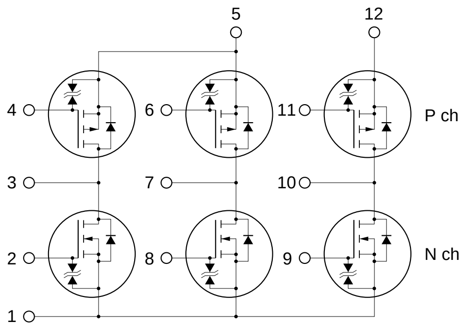
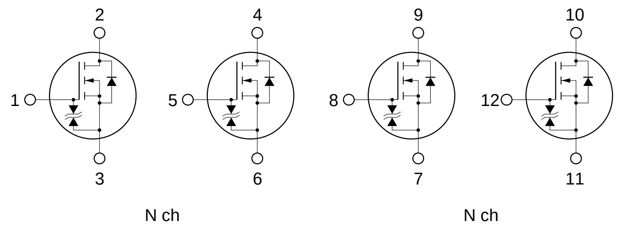
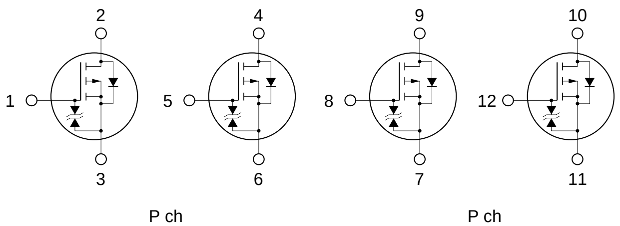
Note: * Allowable value at T_C = 25°C

Maximum channel dissipation ambient temperature curve



Maximum channel dissipation case temperature curve



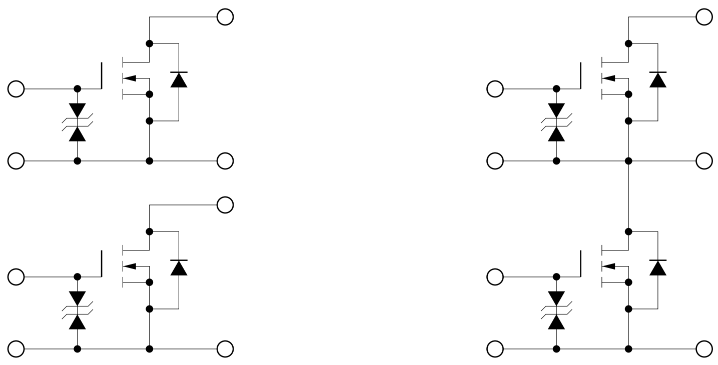
Type		Equivalent Circuit
SP-10	N ch 4-element (A)	
	N/P complementary (B)	
SP-12 • SP-12TA	(E)	
	(D)	
	(F)	
	(G)	

2.8 Power MOS FET Modules

Table 2-10 Typical Characteristics of Power MOS FET Modules

Package	Part Number	Maximum Ratings* V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch} (W)	Electrical Characteristics (typ) $R_{DS(on)}$ (Ω) Typ	$R_{DS(on)}$ (Ω) Max	$\lvert y_{fs}\rvert$ (S)	t_{on} (ns)	t_{off} (ns)	t_{rr} (ns)	Equivalent Circuit
F	PM45302F	450	±20	30	200	0.13	0.2	25	580	900	200	A
	PM50302F	500				0.15	0.2					
C	PM45502C	450	±20	50	300	0.08	0.12	40	850	1400	200	A
	PM50502C	500				0.09	0.12					
J	PM4550J	450	±30	50	250	0.14	0.18	30	315	390	130	B
	PM5050J	500				0.14	0.18					
	PM4575J	450	±30	75	300	0.1	0.12	45	410	685	130	B
	PM5075J	500				0.1	0.12					
K	PM50100K	500	±30	100	400	0.08	0.10	55	890	1020	140	B
	PM50150K	500		150	500	0.06	0.08	80	1100	1590	140	
	PM45100K	450		100	400	0.08	0.10	55	890	1020	140	
	PM45150K	450		150	500	0.06	0.08	80	1100	1590	140	

Notes: * Per transistor
☐ : Type with built-in high-speed diode
Internal equivalent circuit



A B

2.9 Line-up of Each Package Outline for Same Die

1. DI Series

Maximum Ratings

V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) Typ	Max	Insertion Type TO-220AB	TO-220FM	TO-3P	TO-3PFM	Surface Mount Type LDPAK	HDPAK
1500	2.5	9	12			2SK1317	2SK2225		2SK2278

2. DII Series

Maximum Ratings

V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) Typ	Max	Insertion Type TO-220AB	TO-220FM	TO-3P	TO-3PFM	Surface Mount Type LDPAK	HDPAK
150	10	0.12	0.15	2SK740				2SK1620	
250	7	0.4	0.55	2SK741				2SK1621	

3. DIII-L Series

Maximum Ratings

V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) Typ	Max	Insertion Type TO-92	TO-92M	TO-220AB	TO-220FM	TO-3P	TO-3PFM	Surface Mount Type UPAK	DPAK	LDPAK
60	0.5	1.3	1.7	2SK1336						2SK1697		
60	1.5	0.3	0.4		2SK975					2SK1764		
60	10	0.12	0.15			2SK970	2SK1093				2SK974	
60	15	0.055	0.065			2SK971	2SK1094					2SK1648
60	25	0.033	0.04			2SK972	2SK1095					2SK1622
60	40	0.015	0.018					2SK1297	2SK1298			
100	0.3	3.5	4.5	2SK1337						2SK1698		
100	10	0.2	0.25			2SK1300	2SK1305					
100	15	0.1	0.13			2SK1301	2SK1306					
100	20	0.065	0.085			2SK1302	2SK1307					2SK1623
–60	–10	0.13	0.18			2SJ172	2SJ175					2SJ214
–60	–15	0.09	0.11			2SJ173	2SJ176					2SJ219
–60	–20	0.065	0.085			2SJ174	2SJ177					2SJ220
–60	–35	0.045	0.06					2SJ215	2SJ216			
–60	–45	0.033	0.042					2SJ217	2SJ218			
–100	–8	0.25	0.3			2SJ247	2SJ248					
–100	–20	0.12	0.16			2SJ221	2SJ222					2SJ409

4. DIII-H Series

Maximum Ratings				Insertion Type						Surface Mount Type		
V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω) Typ	Max	TO-220AB	TO-220FM	TO-220CFM	TO-3P	TO-3PFM	TO-3PL	DPAK	LDPAK	HDPAK
250	7	0.4	0.55	2SK1667	2SK1668	2SK2425						
250	12	0.23	0.35	2SK1761	2SK1762	2SK2426						
250	20	0.12	0.15				2SK2007	2SK2008				
250	30	0.075	0.095				2SK1669	2SK1670				
350	7	0.6	0.8	2SK1400A	2SK2345						2SK1869	
350	15	0.3	0.4	2SK2582			2SK1401A					
450	3	2	2.8	2SK1153	2SK1862	2SK2431						
500	3	2.2	3	2SK1154	2SK1863							
450	5	1	1.4	2SK1155	2SK1626	2SK2114					2SK1313	
500	5	1.2	1.5	2SK1156	2SK1627	2SK2115					2SK1314	
450	7	0.6	0.8	2SK1157	2SK1566	2SK2116	2SK1161	2SK1831			2SK1540	
500	7	0.7	0.9	2SK1158	2SK1567	2SK2117	2SK1162	2SK1832			2SK1541	
450	8	0.55	0.7	2SK1159		2SK2423	2SK1163				2SK1315	
500	8	0.6	0.8	2SK1160			2SK1164				2SK1316	
450	12	0.4	0.55			2SK2424	2SK1165	2SK1328				
500	12	0.45	0.6			2SK2591	2SK1166	2SK1329				
450	15	0.25	0.36				2SK1167					
500	15	0.3	0.4				2SK1168					2SK2330
450	20	0.2	0.25				2SK1169		2SK1628			
500	20	0.22	0.27				2SK1170		2SK1629			2SK2174
500	10	0.7	0.9	2SK2408			2SK1516					
600	3	3.8	5		2SK1572	2SK2144				2SK2059	2SK1618	
600	4	1.8	2.4	2SK1402	2SK1637	2SK2097					2SK1624	
600	5	1.1	1.5	2SK1809	2SK1404	2SK2118						
600	7	0.9	1.3				2SK1403				2SK1625	
650	4	2	2.6	2SK1402A	2SK2422							
650	7	1	1.4	2SK2328		2SK2416	2SK1403A					
900	3	5	7	2SK1338			2SK1339				2SK1647	
900	5	3	4	2SK1807	2SK1808		2SK1340				2SK1528	
900	6	2	3				2SK1341	2SK1859				
900	8	1.2	1.6				2SK1342	2SK1775				

5. DIV-L Series

Maximum Ratings

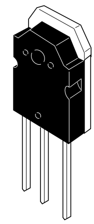
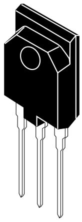
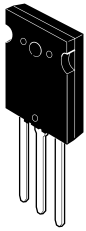
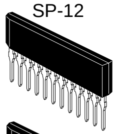
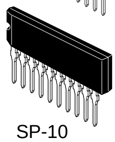
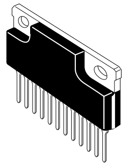
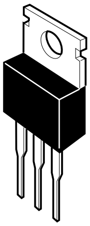
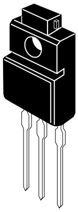
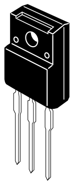
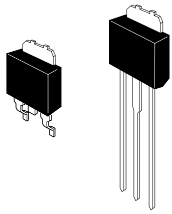
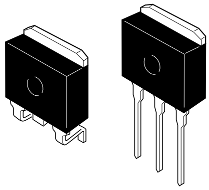
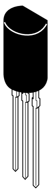
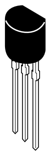
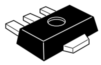
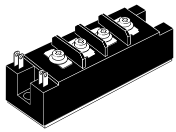
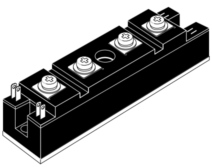
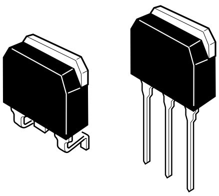
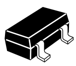
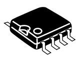
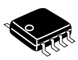
		$R_{DS(on)}$ (Ω)		Insertion Type						Surface Mount Type			
V_{DSS} (V)	I_D (A)	Typ	Max	TO-126 FM	TO-220 AB	TO-220 FM	TO-220 CFM	TO-3P	TO-3 PFM	(SOP-8)	DPAK	LDPAK	HDPAK
–20	–7	0.05	0.07							HAT1001F	2SJ387		
–60	–15	0.075	0.095		2SJ290	2SJ293	2SJ321					2SJ296	
–60	–20	0.05	0.065		2SJ291	2SJ294	2SJ322					2SJ297	
–60	–30	0.033	0.043		2SJ292	2SJ295	2SJ323					2SJ280	
30	10	0.03	0.04							HAT2001F	2SK2329		
30	45	0.011	0.015		2SK2205		2SK2206					2SK2204	
60	5	0.12	0.15		2SK2175						2SK1949		
60	25	0.03	0.04		2SK1910	2SK1951	2SK2119					2SK1918	
60	40	0.018	0.022		2SK1911	2SK1952	2SK2120	2SK2096				2SK1919	
60	50	0.007	0.01					2SK2121	2SK2203				

6. DV-L Series

Maximum Ratings

		$R_{DS(on)}$ (Ω)		Insertion Type						Surface Mount Type			
V_{DSS} (V)	I_D (A)	Typ	Max	TO-126 FM	TO-220 AB	TO-220 FM	TO-220 CFM	TO-3P	TO-3 PFM	(SOP-8)	DPAK	LDPAK	HDPAK
60	50	0.007				2SK2529		2SK2553				2SK2586	

Table 2-11 Power MOS FET Packages

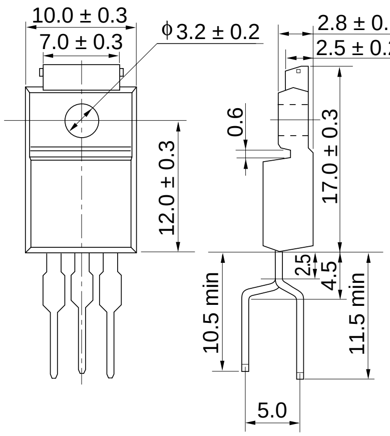
Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)	Package	V_{DSS} (V)	I_D (A)	$R_{DS(on)}$ (Ω)
TO-3P	60 to 1500	2.5 to 75	4.5 m to 9.0	TO-3P ·FM	60 to 1500	12 to 50	0.015 to 9.0	TO-3PL	250 to 1500	8 to 50	0.08 to 1.9	SP-10 SP-12 SP-12TA	60 100	2.5 to 10	0.033 to 0.25
												SP-12  SP-10  SP-12TA 			
TO-220	60 to 900	1 to 30	0.011 to 5.0	TO-220 FM/CFM	30 to 900	2 to 50	7 m to 5.0	DPAK	20 to 60	2 to 20	0.03 to 25	LDPAK	60 to 900	3 to 50	7 m to 3.0
				 TO-220FM  TO-220CFM											
TO-92M	30 60	1.5	0.3	TO-92	60 to 100	0.3	1.5 to 3.5	UPAK	12 to 200	0.5 to 2.0	0.28 to 8.0	F	450 to 500	30	0.13 to 0.15
															
C	450 to 500	50	0.08 to 0.09	HDPAK	60 to 1500	2.5 to 20	0.015 to 12	MPAK	20 to 50	0.2	1.4 to 5.0	SOP-8	20 to 60	2.5 to 10	0.012 to 0.2
												 FP-8D EIAJ SOP-8  FP-8DA JEDEC SOP-8			

Section 6. Standard Lead Forming Specification

TO-220FM

Unit : mm

B



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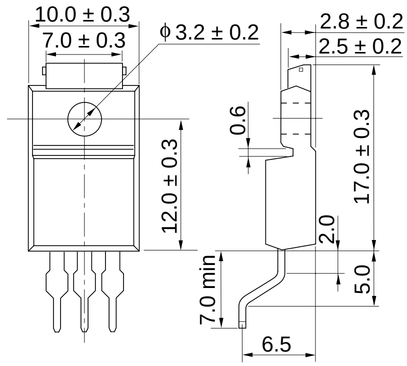

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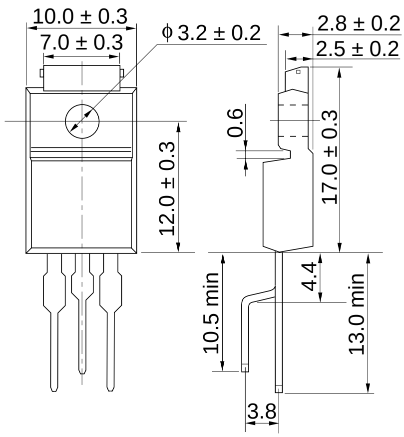

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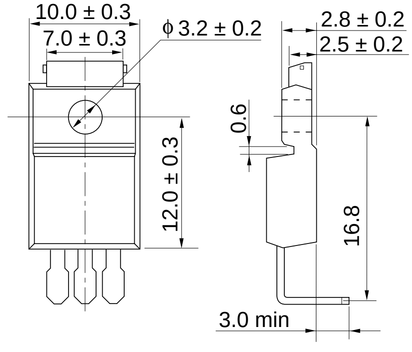

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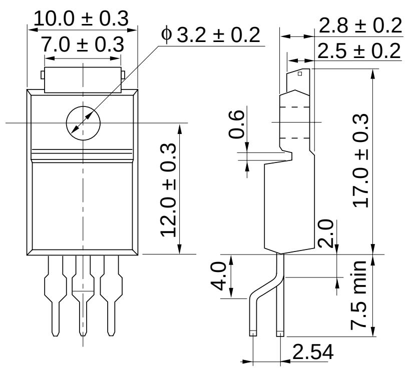
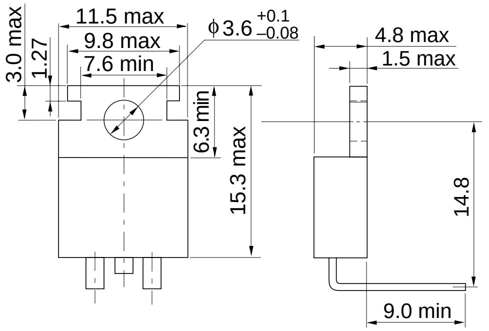


TO-220

Unit : mm

A



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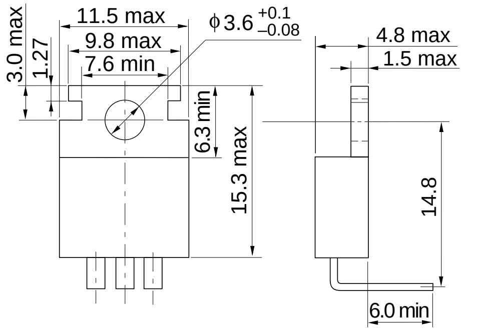

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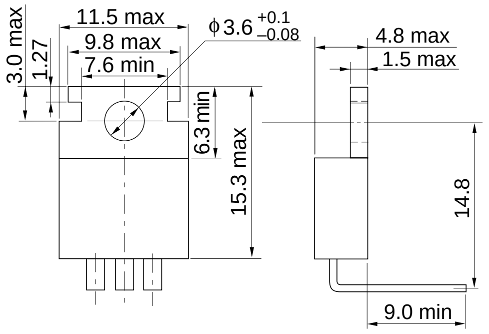

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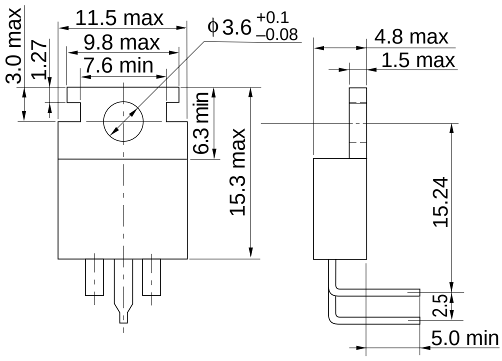

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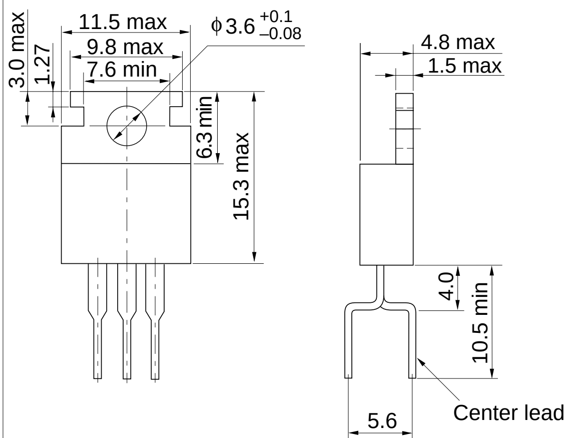

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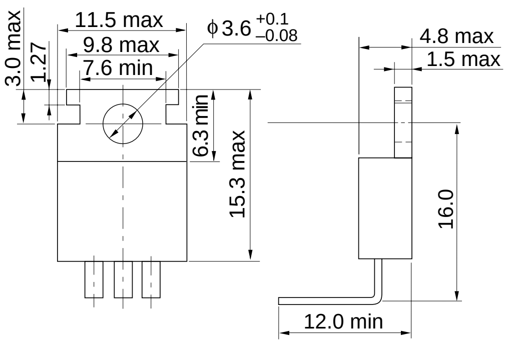
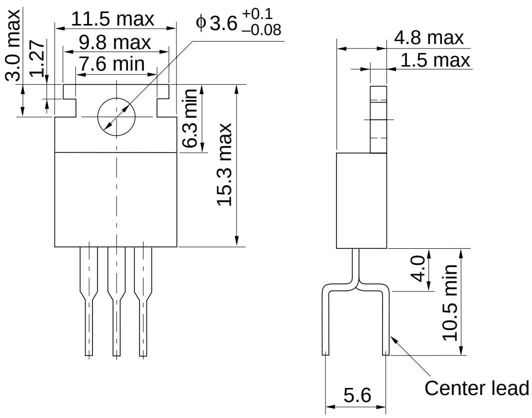


TO-220 (cont)

Unit :mm

E



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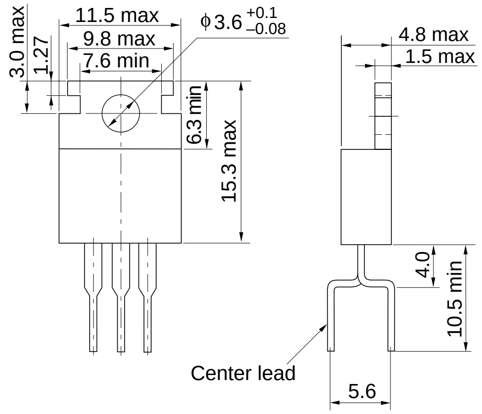

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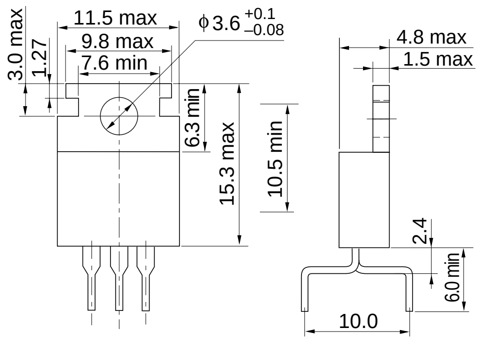

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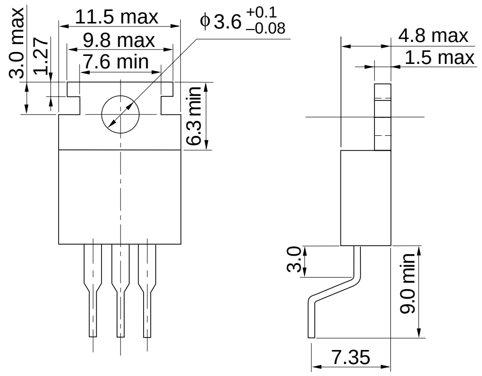

TO-3P

Unit : mm

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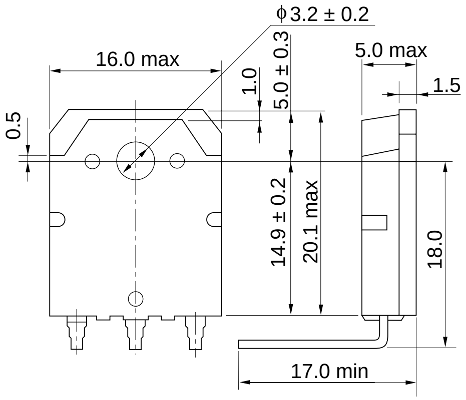
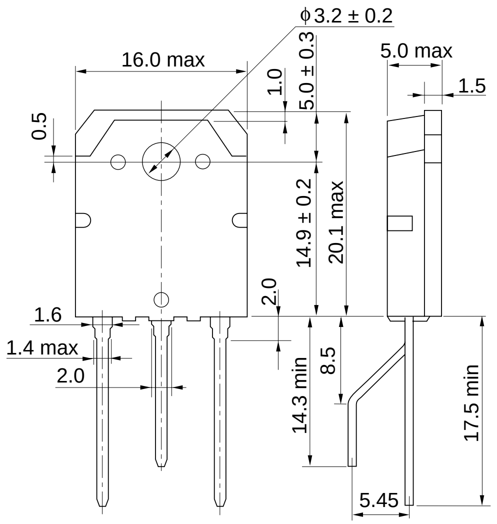
<tr><td>
</td><td>
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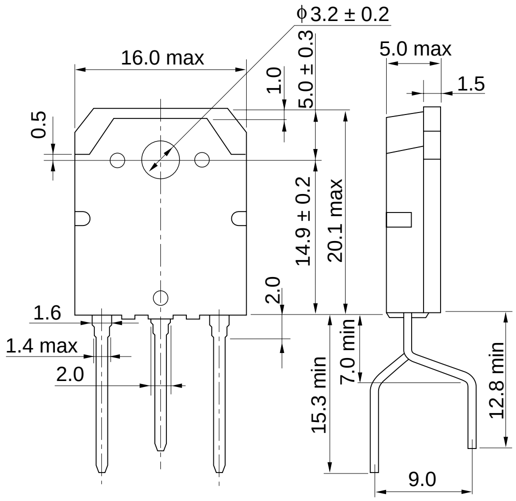
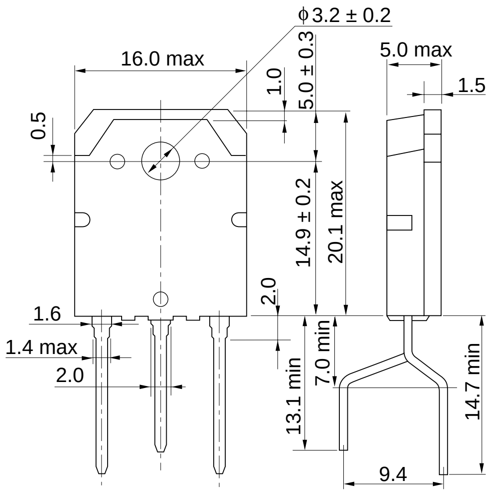
<tr><th>F</th><th>G</th></tr>
<tr><td>
</td><td>
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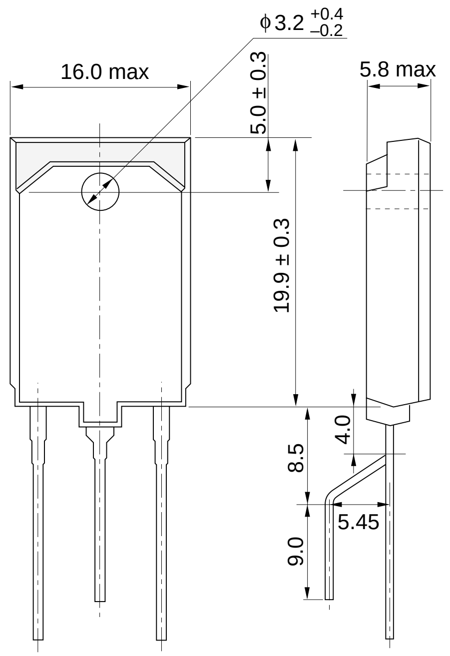
TO-3PFM

Unit : mm

F-1



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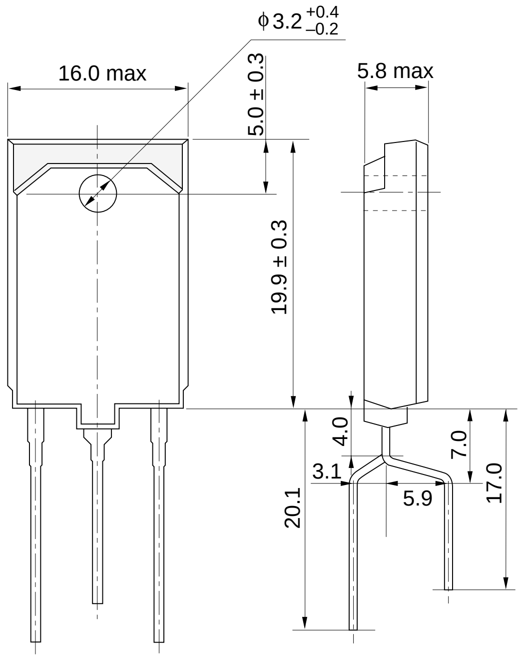
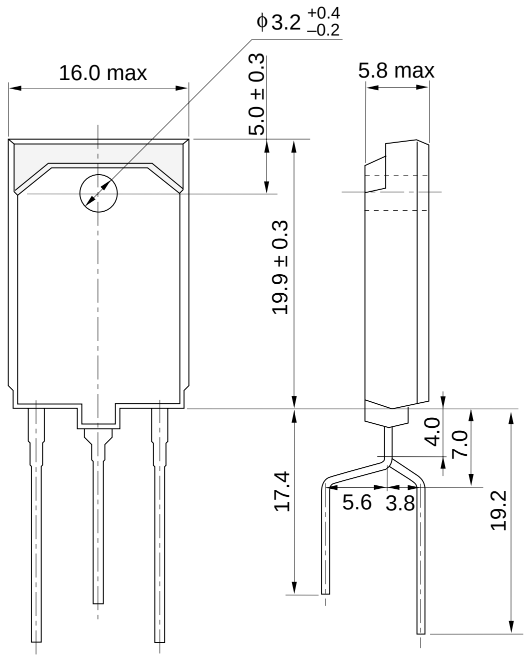


F-6

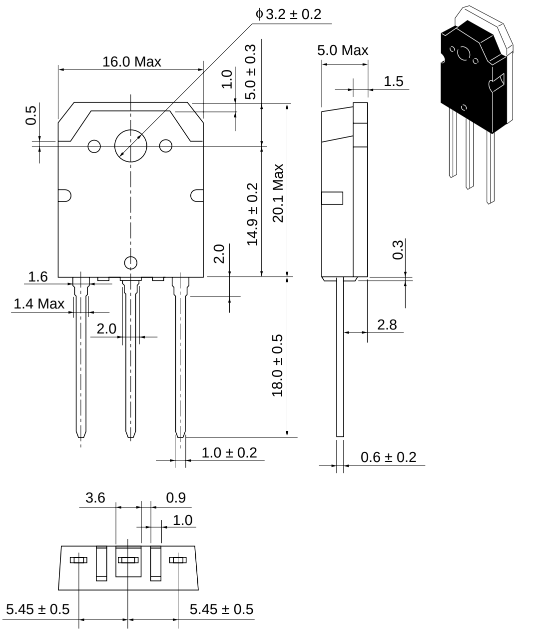


Section 7. Package Information

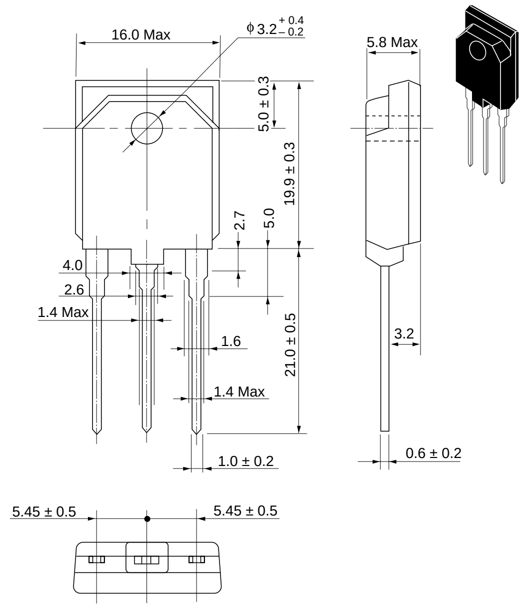
Outline Dimensions

Unit : mm

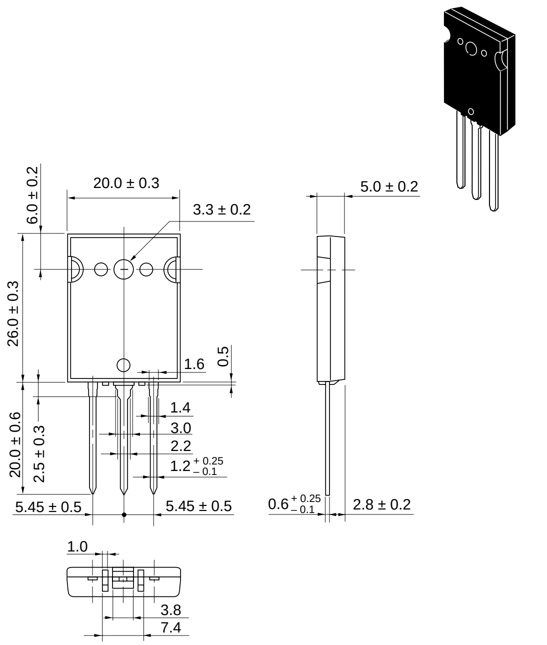
- **TO-3P**



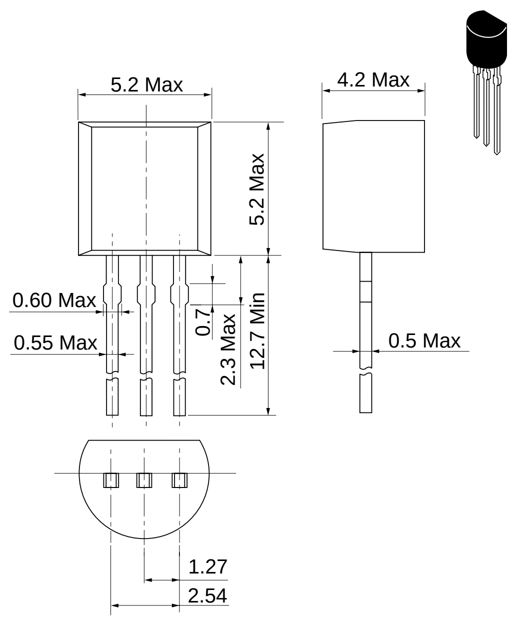
- **TO-3PFM**



- **TO-3PL**



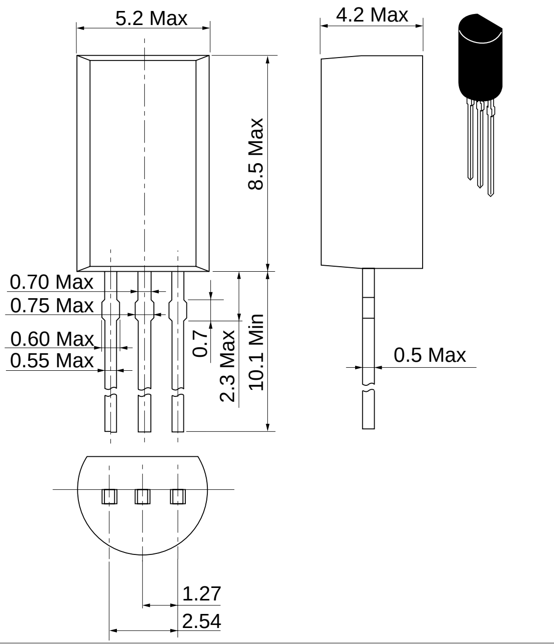
- **TO-92 (1)**



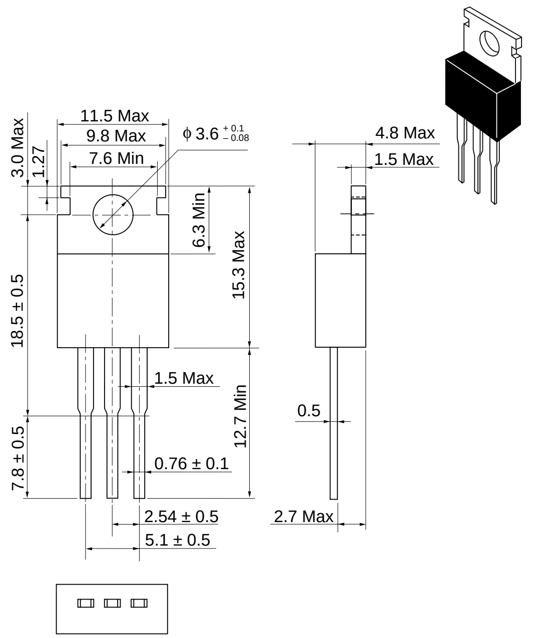
Outline Dimensions (cont)

Unit : mm

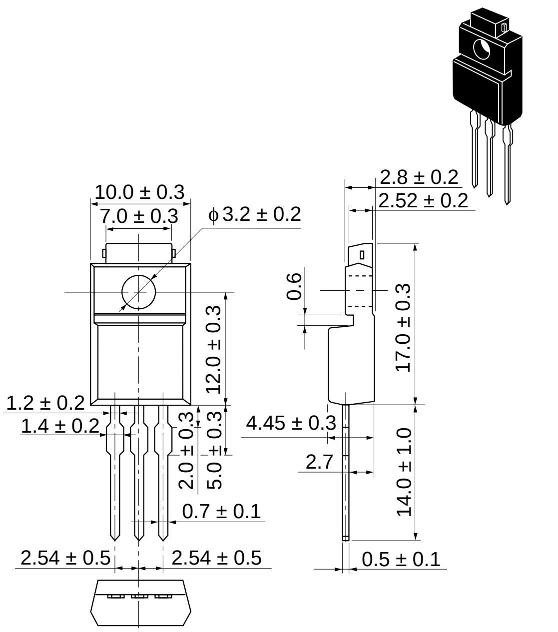
- **TO-92MOD**



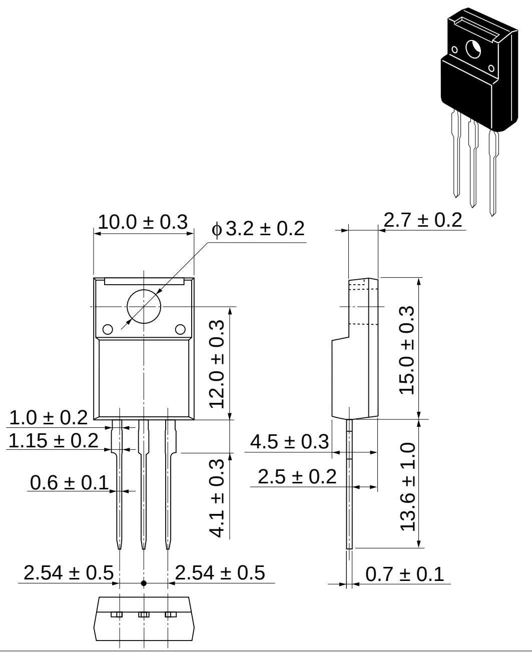
- **TO-220AB**



- **TO-220FM**



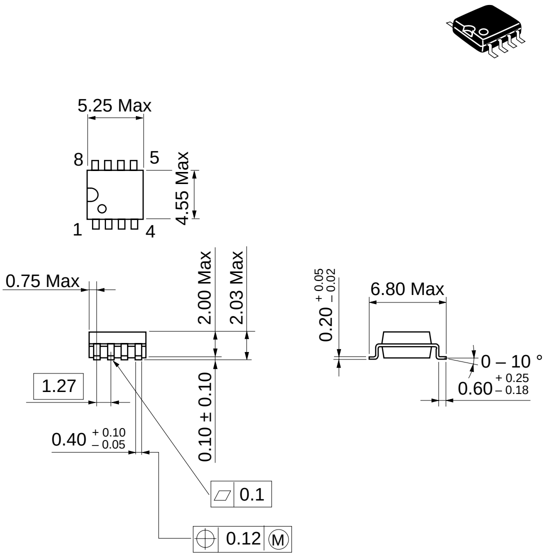
- **TO-220CFM**



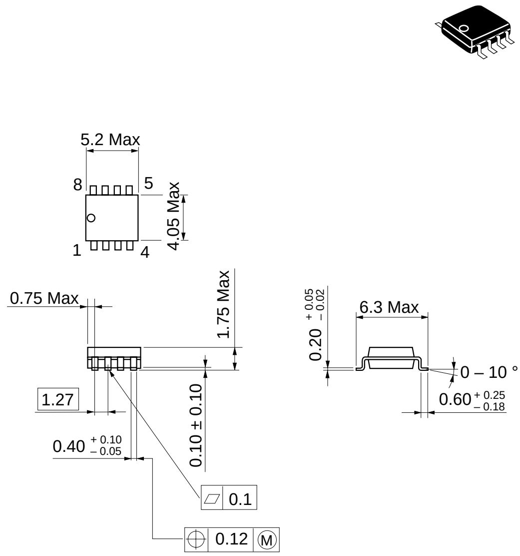
Outline Dimensions (cont)

Unit : mm

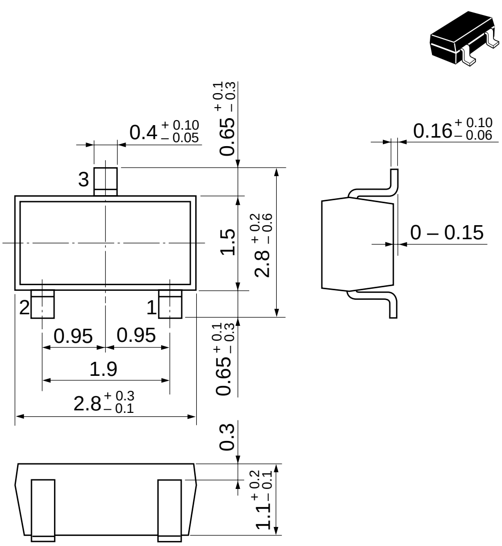
- **FP-8D (EIAJ SOP-8)**



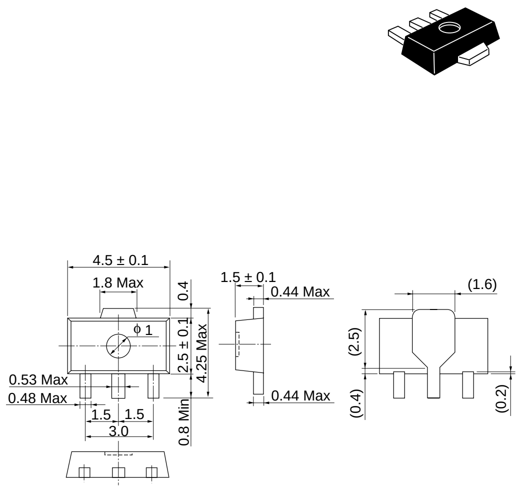
- **FP-8DA (JEDEC SOP-8)**



- **MPAK**



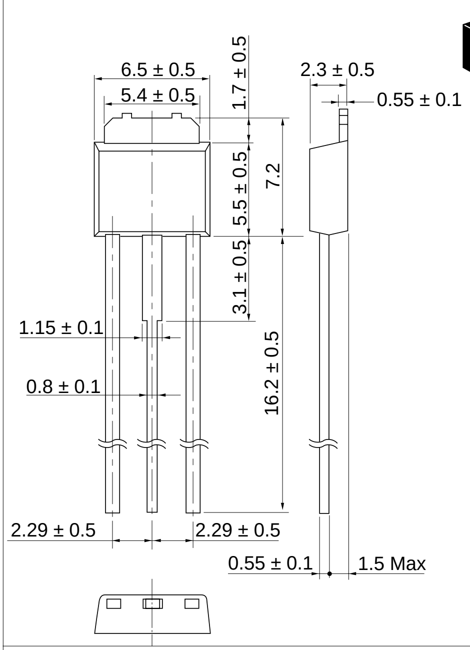
- **UPAK**



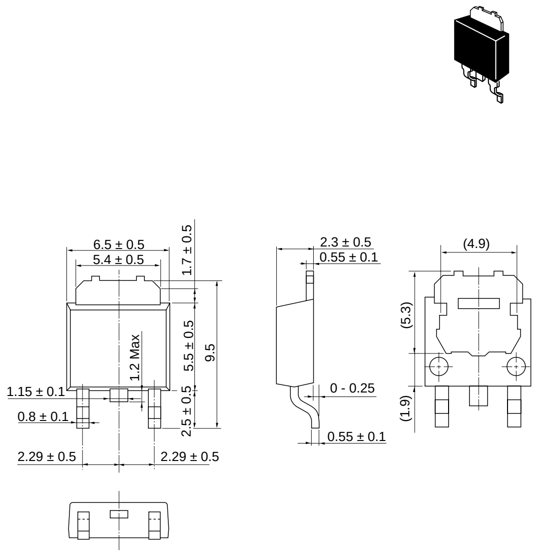
Outline Dimensions (cont)

Unit : mm

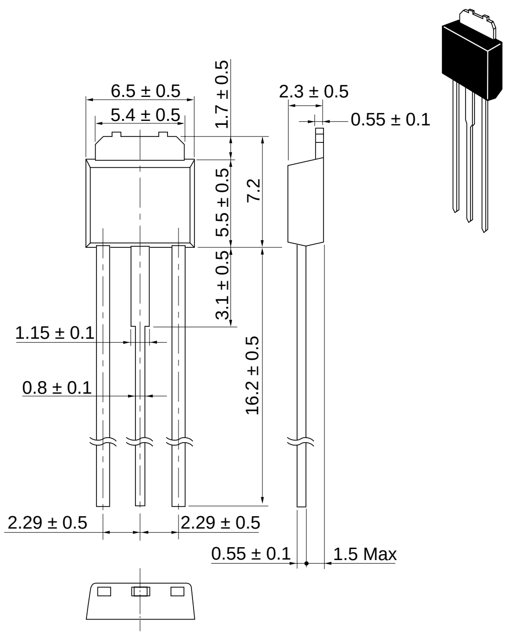
- **DPAK-1 (L)**



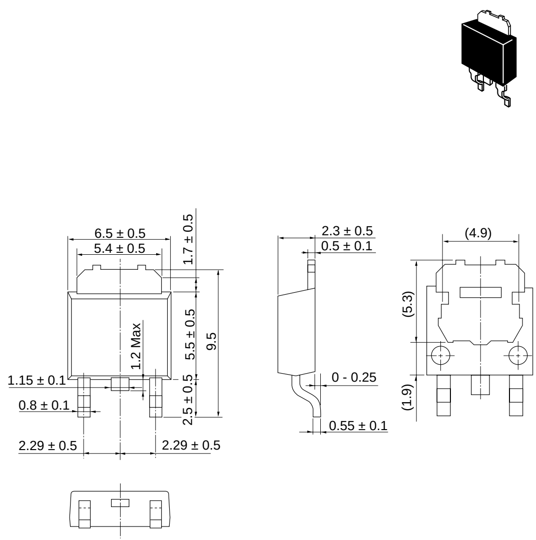
- **DPAK-1 (S)**



- **DPAK-2 (L)**



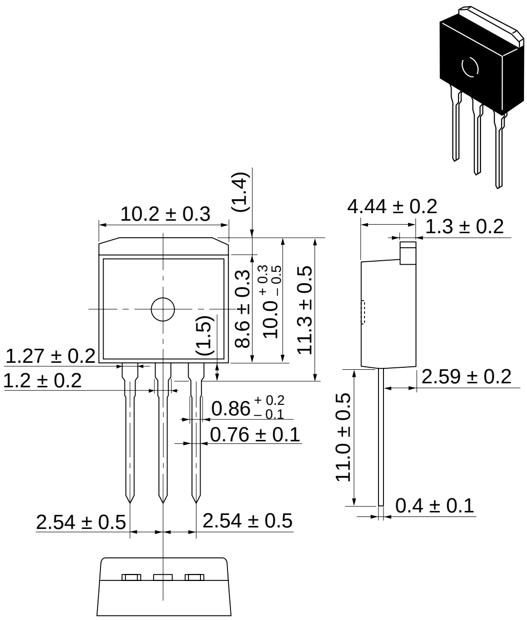
- **DPAK–2 (S)**



Outline Dimensions (cont)

Unit : mm

- **LDPAK (L)**



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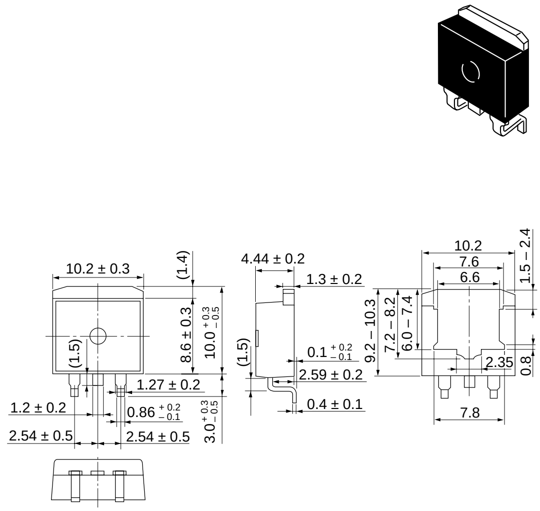
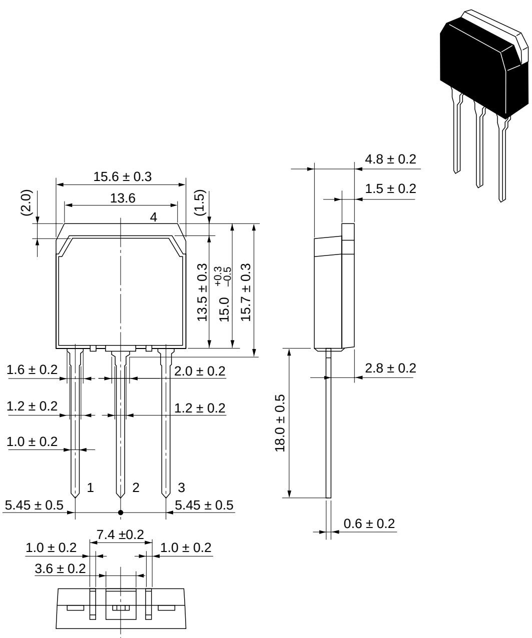
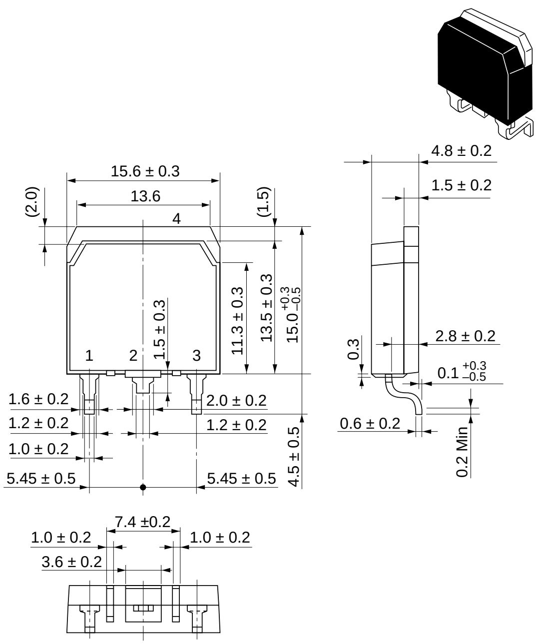


- **HDPAK (L)**



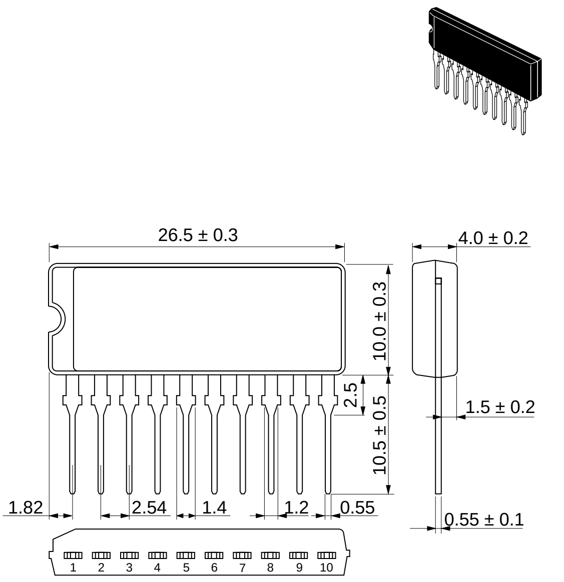
- **HDPAK (S)**



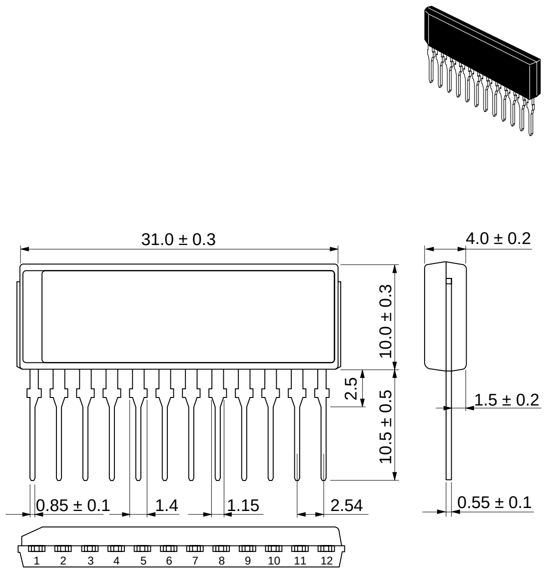
Outline Dimensions (cont)

Unit : mm

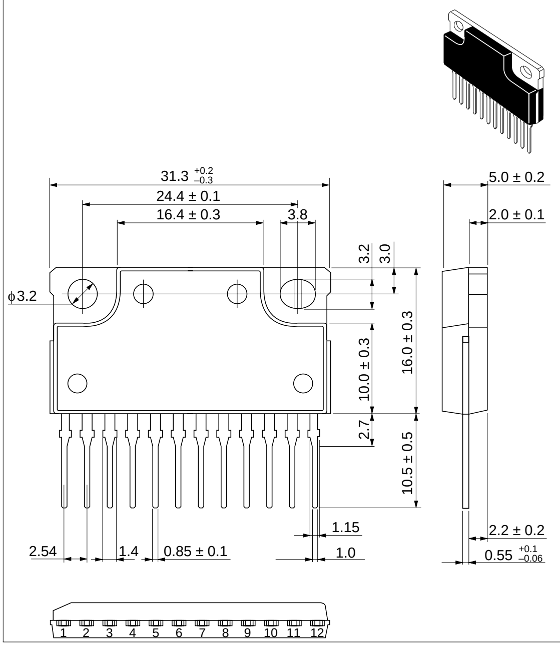
- **SP-10**



- **SP-12**



- **SP-12TA**



2SJ234(L), 2SJ234(S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source
- Suitable for DC – DC convertor, motor drive, power switch, solenoid drive

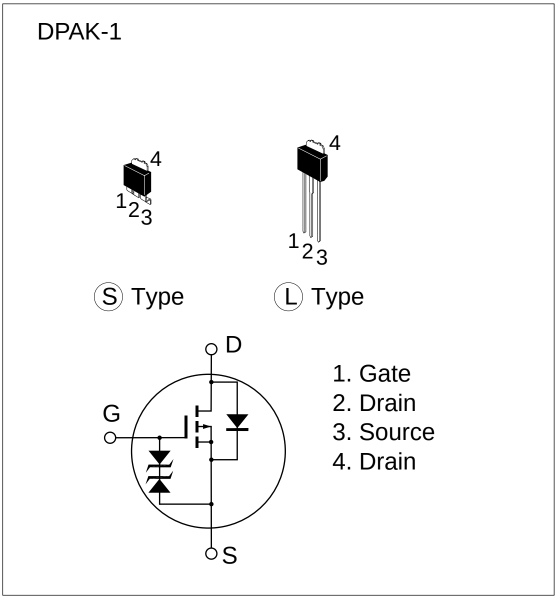


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2.5	A
Drain peak current	$I_{D(pulse)}$*	–10	A
Body–drain diode reverse drain current	I_{DR}	–2.5	A
Channel dissipation	Pch**	10	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

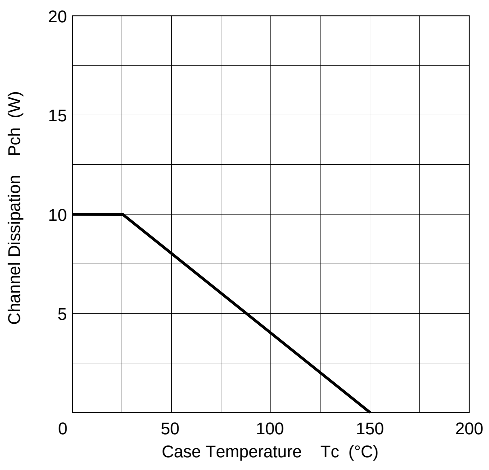
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

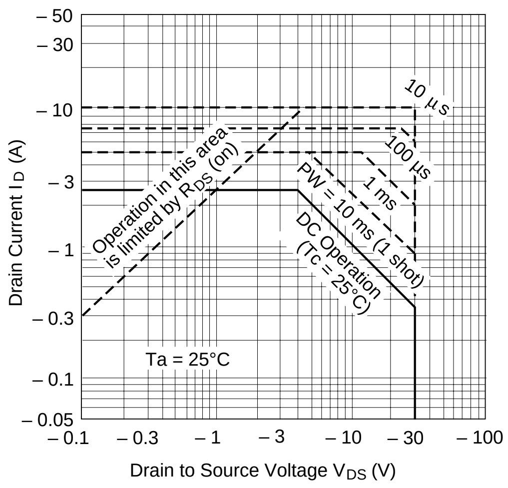
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.4	Ω	I_D = –1.5 A V_{GS} = –10 V *
		—	0.5	0.7		I_D = –1.5 A V_{GS} = –4 V *
Forward transfer admittance	$\lvert y_{fs} \rvert$	1.0	1.8	—	S	I_D = –1.5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	245	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	170	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	60	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	7	—	ns	I_D = –1.5 A
Rise time	t_r	—	25	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	85	—	ns	R_L = 20 Ω
Fall time	t_f	—	72	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –2.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	80	—	ns	I_F = –2.5 A, V_{GS} = 0, di_F / dt = 50 A / µs

* Pulse Test

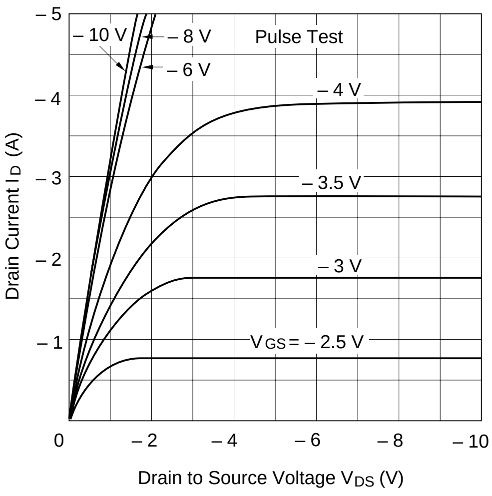
Power vs. Temperature Derating



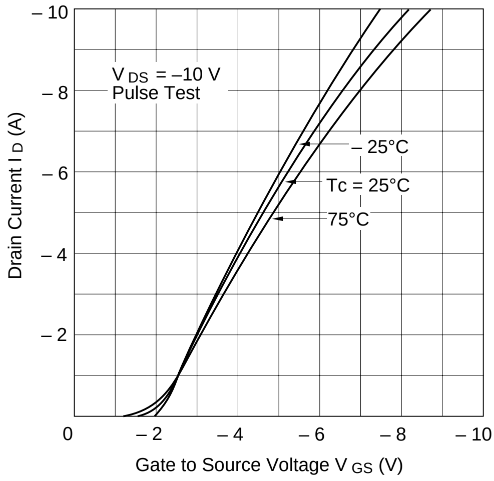
Maximum Safe Operation Area



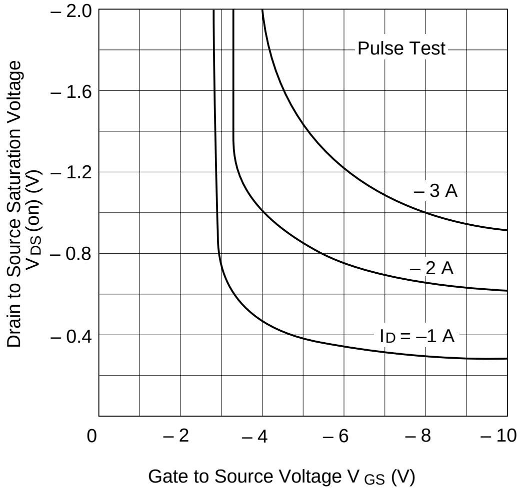
Typical Output Characteristics



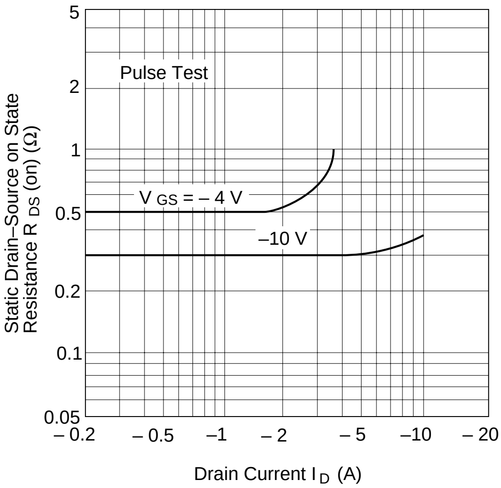
Typical Transfer Characteristics



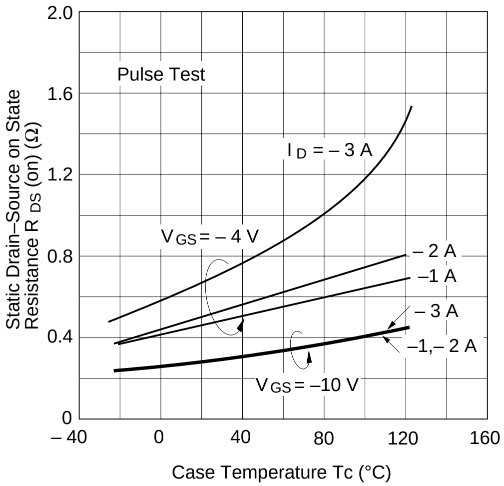
Drain to Source Saturation Voltage vs. Gage to Source Voltage



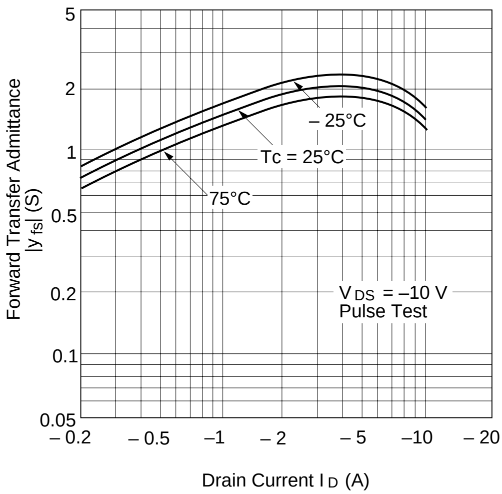
Static Drain to Source on State Resistance vs. Drain Current



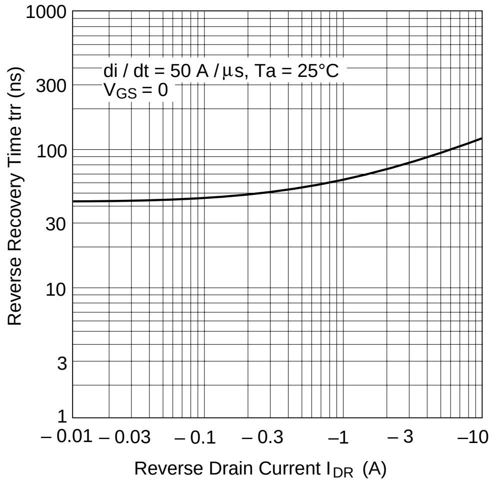
Static Drain to Source on State Resistance vs. Temperature



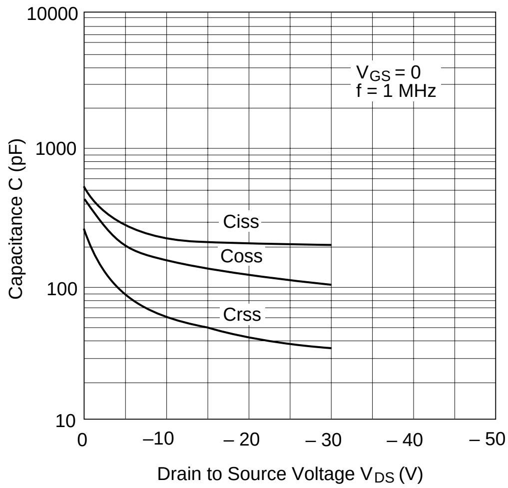
Forward Transfer Admittance vs. Drain Current



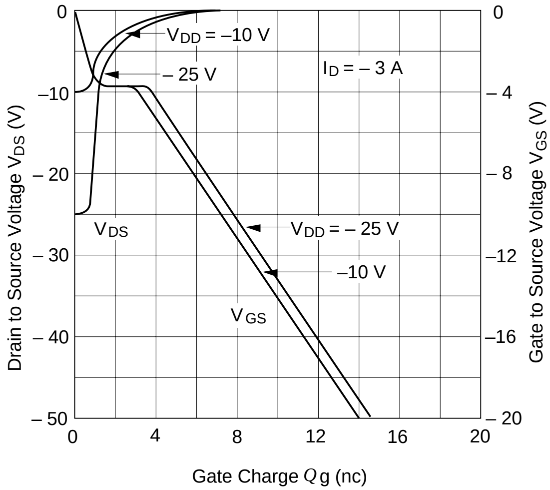
Body – Drain Diode Reverse Recovery Time



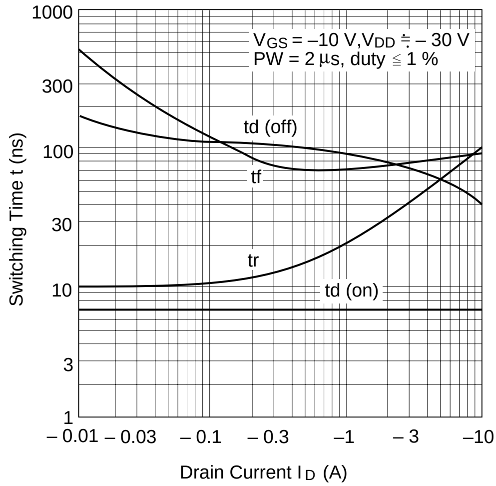
Typical Capacitance vs. Drain to Source Voltage



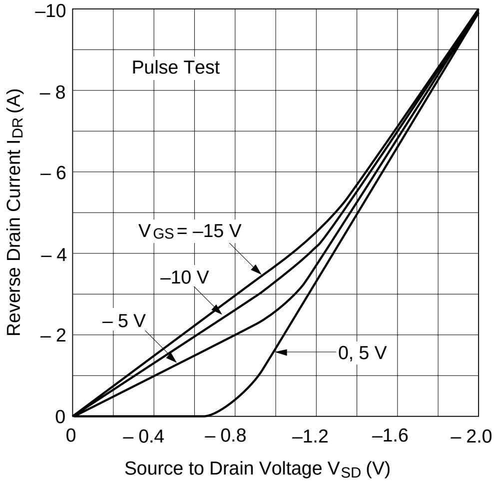
Dynamic Input Characteristics



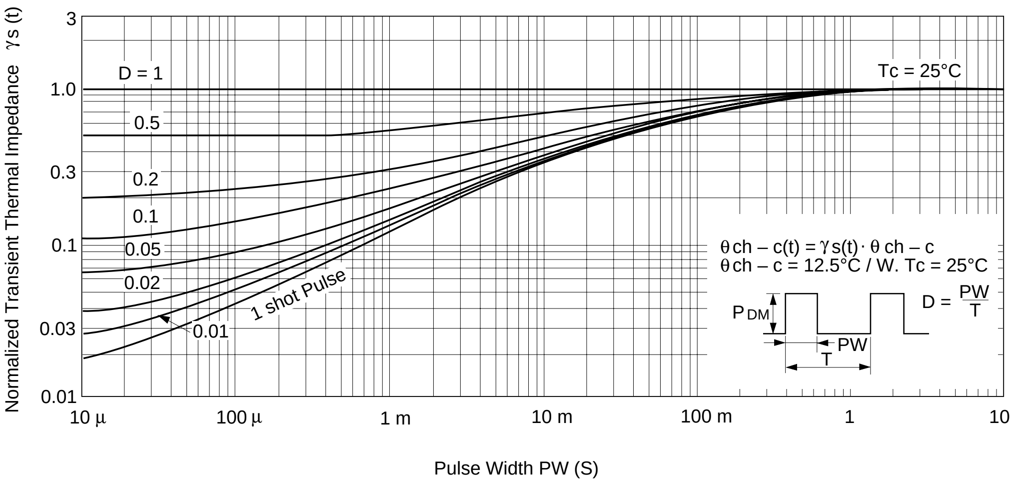
Switching Characteristics



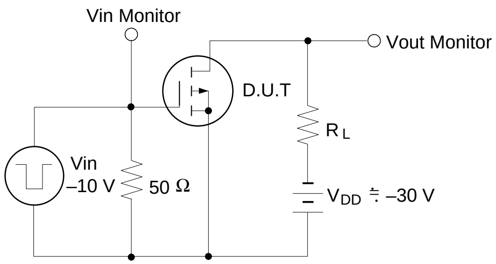
Reverse Drain Current vs.
Source to Drain Voltage



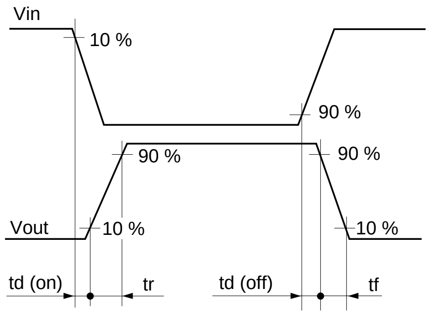
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveforms



2SJ244

Silicon P Channel MOS FET (DIII-L)

Application

High speed power switching
Low voltage operation

Features

- Very low on–resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

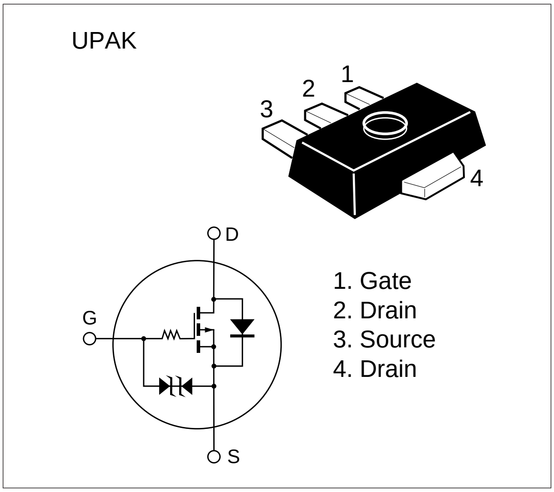


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–12	V
Gate to source voltage	V_{GSS}	±7	V
Drain current	I_D	±2	A
Drain peak current	$I_{D(pulse)}$*	±4	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

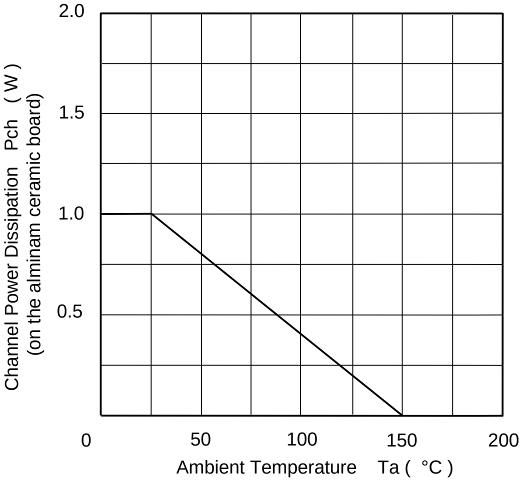
* PW < 100 µs, duty cycle < 10 %
** Value on the alumina ceramic board (12.5x20x0.7 mm)
*** Marking is "JY".

Table 2 Electrical Characteristics (Ta = 25°C)

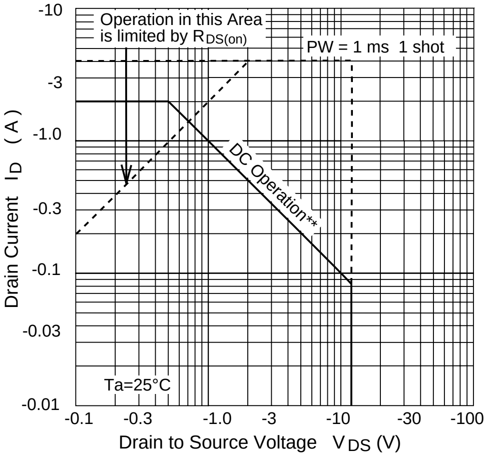
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–12	—	—	V	I_D = –1 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±7	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source cutoff current	I_{GSS}	—	—	±5	µA	V_{GS} = ±6 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –8 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.4	—	–1.4	V	I_D = –100 µA V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}1$	—	0.65	0.9	Ω	I_D = –0.5 A * V_{GS} = –2.5 V
Static drain to source on state resistance	$R_{DS(on)2}$	—	0.5	-–	Ω	I_D = –1 A * V_{GS} = –4 V
Forward transfer admittance	$\|y_{fs}\|$	—	1.8	—	S	I_D = –1 A * V_{DS} = –5 V
Input capacitance	Ciss	—	130	—	pF	V_{DS} = –5 V
Output capacitance	Coss	—	50	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	260	—	pF	f = 1 MHz
Turn–on time	$t_{(on)}$	—	365	—	ns	I_D = –0.2 A*, Vin = –4 V
Turn–off delay time	$t_{(off)}$	—	1450	—	ns	R_L = 51 Ω
Body–drain diode forward voltage	V_{DF}	—	—	7	V	I_F = 4 A*, V_{GS} = 0

* Pulse Test

Maximum Channel Power Dissipation Curve

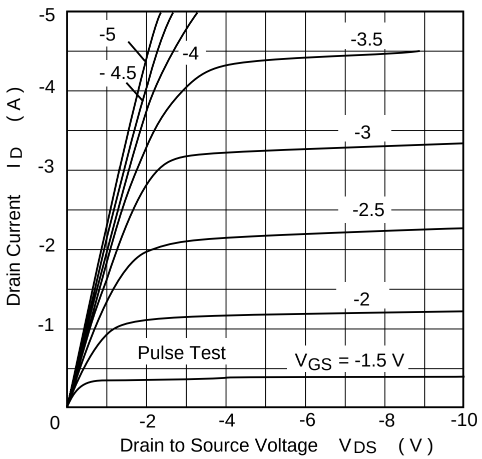


Safe Operation Area

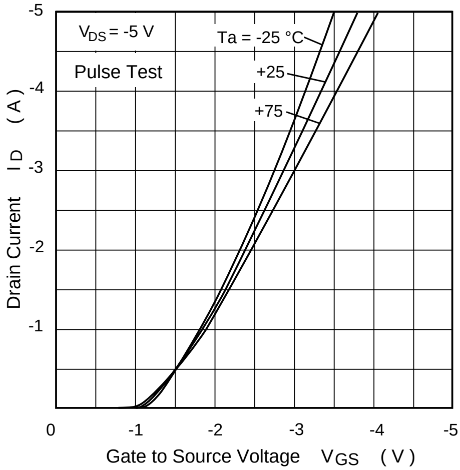


**ON the almina
ceramic board

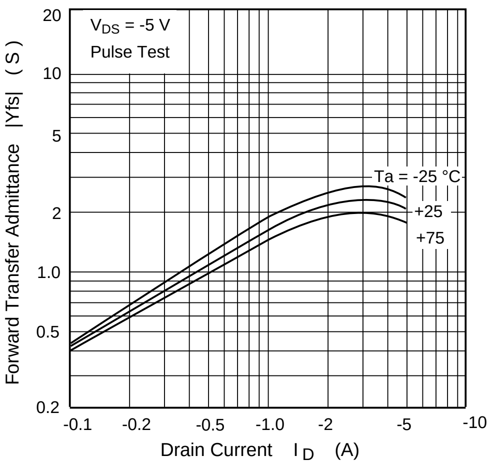
Typical Output Characteristics



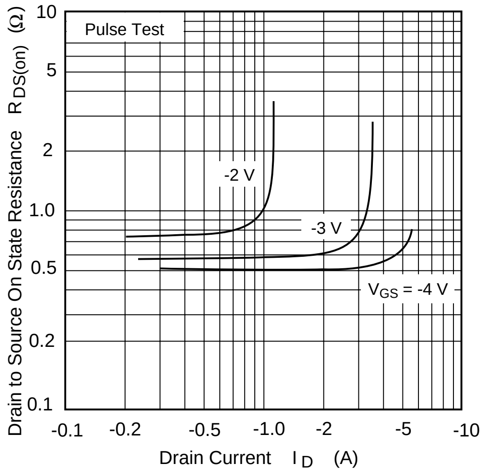
Typical Forward Transfer Characteristics



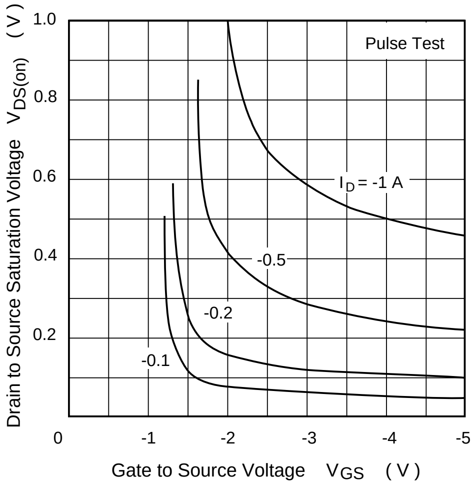
Forward Transfer Admittance vs. Drain Current



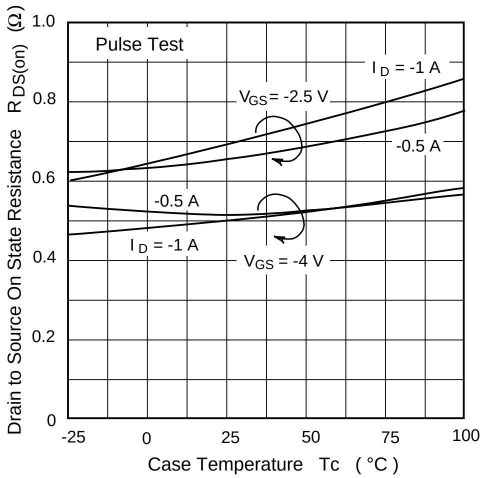
Drain to Source On State Resistance vs. Drain Current



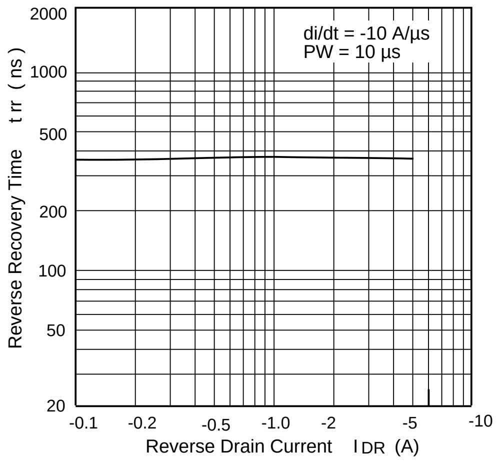
Drain to Source Saturation Voltage vs. Gate to Source Voltage



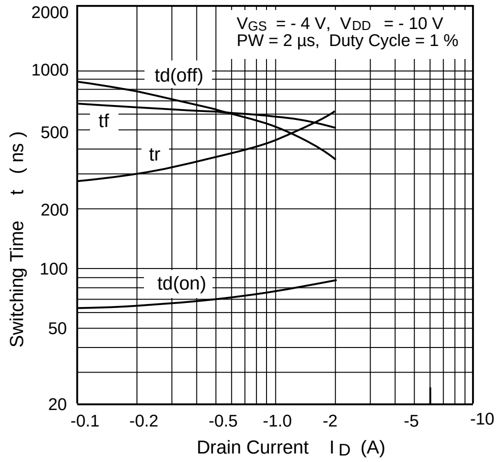
Drain to Source On State Resistance vs. Case Temperature



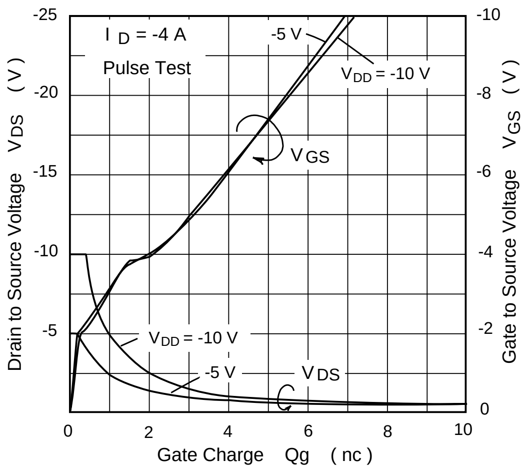
Reverse Recovery Time vs.
Reverse Drain Current



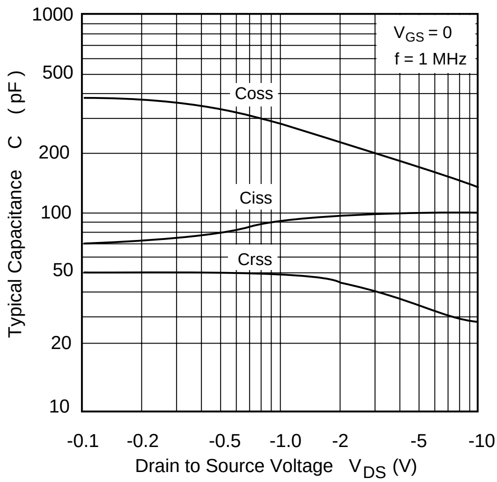
Switching Time vs. Drain Current



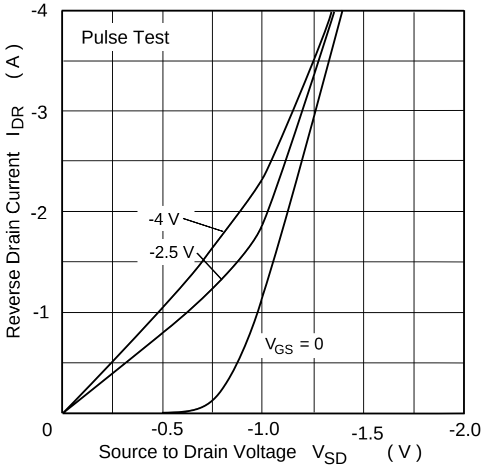
Dynamic Input Characteristics



Typical Capacitance vs.
Drain to Source Voltage



Reverse Drain Current vs.
Source to Drain Voltage



2SJ245(L), 2SJ245(S)

SILICON P-CHANNEL MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V Gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

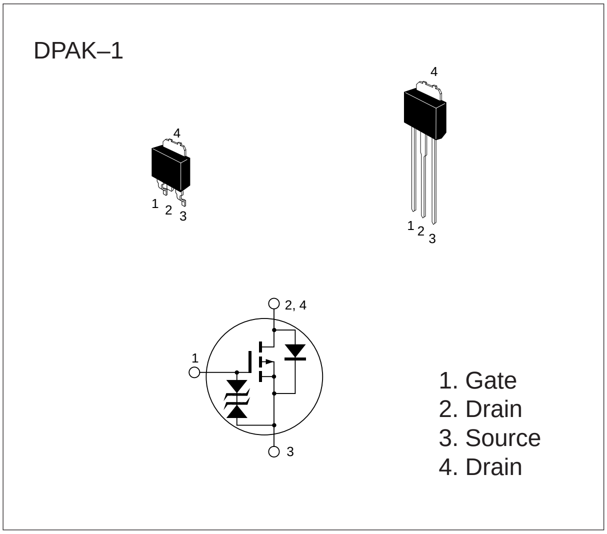


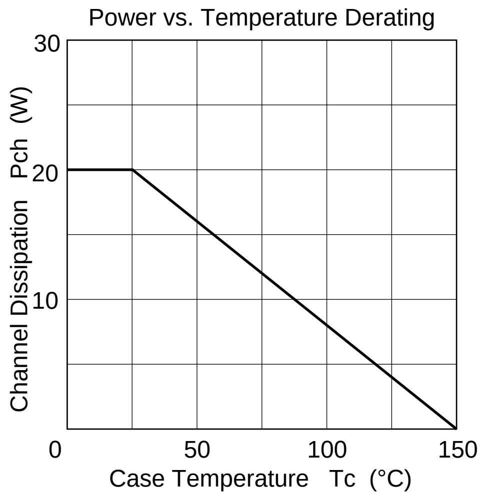
Table 1 Absolute Maximum Ratings (Ta = 25°C)

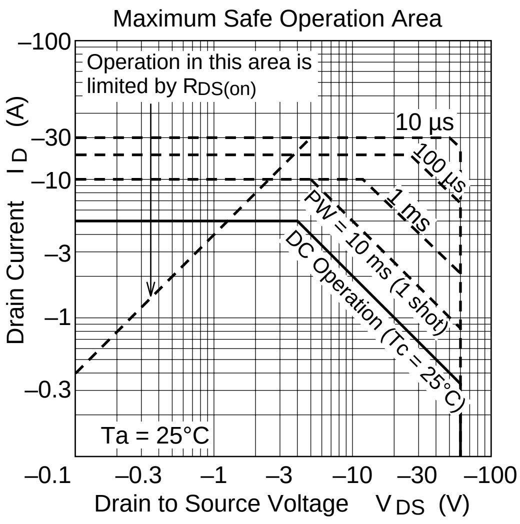
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–5	A
Drain peak current	$I_{D(pulse)}$*	–20	A
Body–drain diode reverse drain current	I_{DR}	–5	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

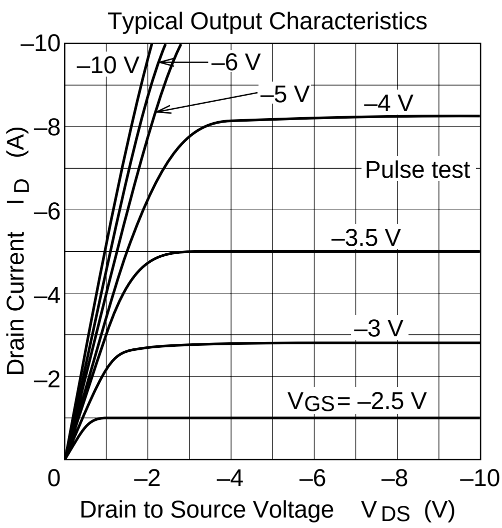
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc=25°C

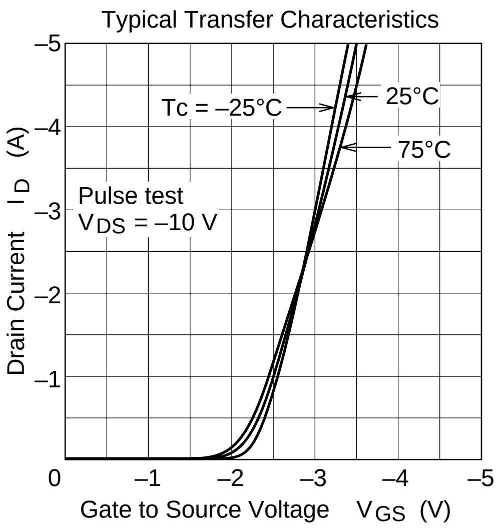
Table 2 Electrical Characteristics (Ta = 25°C)

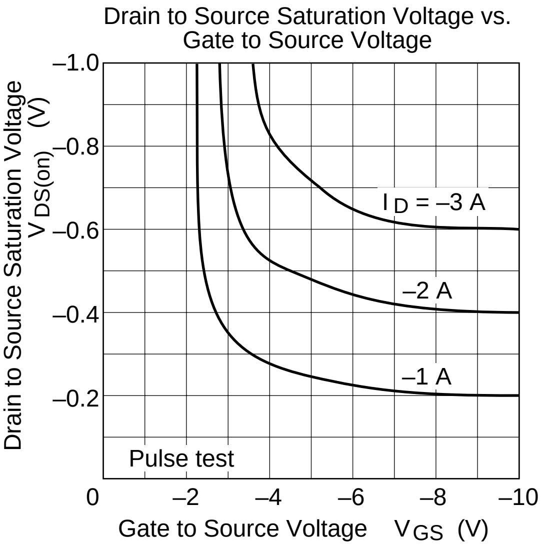
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.25	Ω	I_D = –3 A V_{GS} = –10 V *
		—	0.28	0.38	Ω	I_D = –3 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	2.2	3.7	—	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance	Ciss	—	610	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	315	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	95	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	12	—	ns	I_D = –3 A
Rise time	t_r	—	45	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	170	—	ns	R_L = 10 Ω
Fall time	t_f	—	90	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –5 A, V_{GS} = 0, diF / dt = 50 A / µs

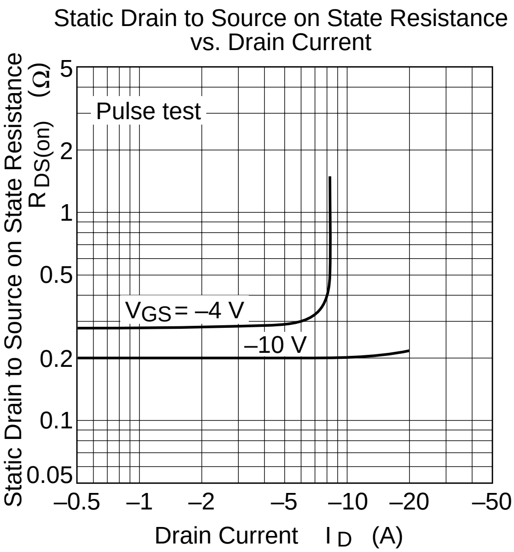

Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature Tc (°C)

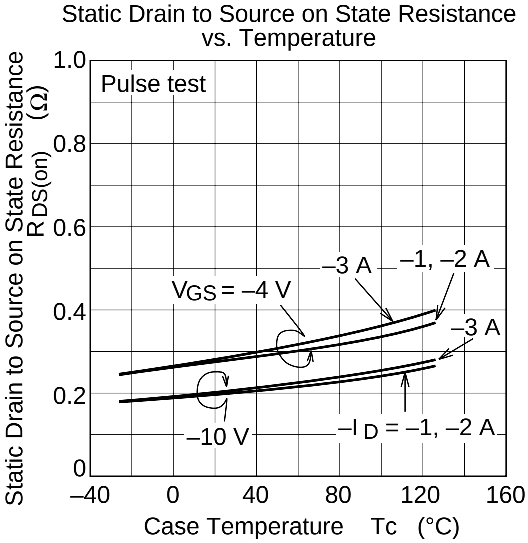

Maximum Safe Operation Area
Operation in this area is limited by $R_{DS(on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25°C
Drain Current I_D (A)
–100
–30
–10
–3
–1
–0.3
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V_{DS} (V)

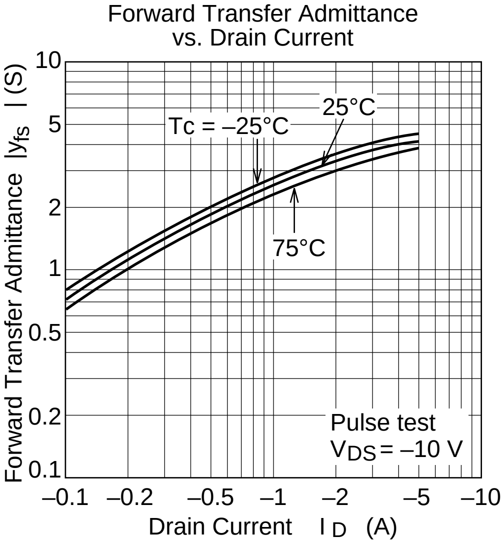

Typical Output Characteristics
–10 V
–6 V
–5 V
–4 V
Pulse test
–3.5 V
–3 V
V_{GS} = –2.5 V
Drain Current I_D (A)
–10
–8
–6
–4
–2
0
–2
–4
–6
–8
–10
Drain to Source Voltage V_{DS} (V)

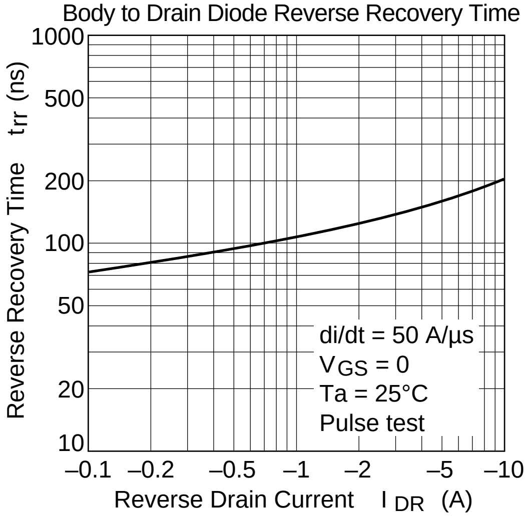

Typical Transfer Characteristics
Tc = –25°C
25°C
75°C
Pulse test
V_{DS} = –10 V
Drain Current I_D (A)
–5
–4
–3
–2
–1
0
–1
–2
–3
–4
–5
Gate to Source Voltage V_{GS} (V)

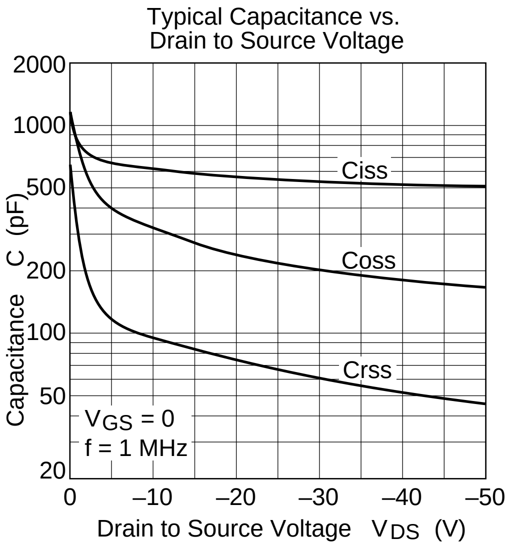

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage
V DS(on) (V)
–1.0
–0.8
–0.6
–0.4
–0.2
0
–2
–4
–6
–8
–10
I D = –3 A
–2 A
–1 A
Pulse test
Gate to Source Voltage V GS (V)

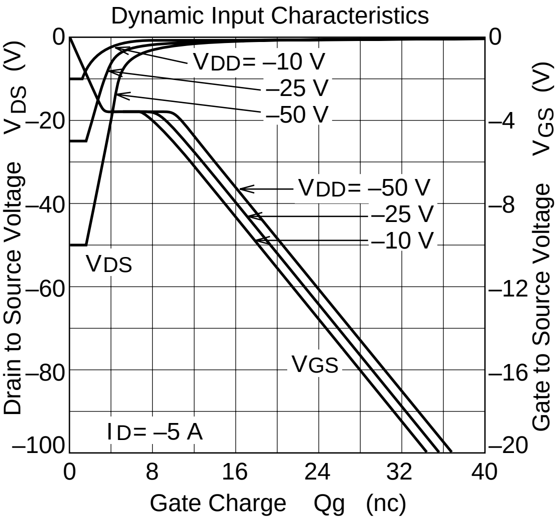

Static Drain to Source on State Resistance
vs. Drain Current
Static Drain to Source on State Resistance
R DS(on) (Ω)
5
2
1
0.5
0.2
0.1
0.05
Pulse test
VGS = –4 V
–10 V
–0.5
–1
–2
–5
–10
–20
–50
Drain Current I D (A)

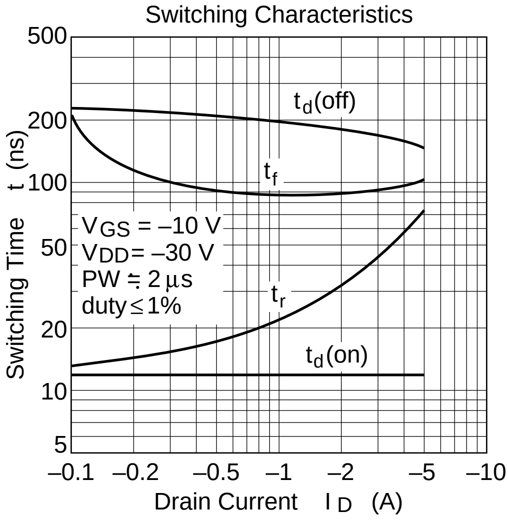

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance
R DS(on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
Pulse test
–3 A
–1, –2 A
VGS = –4 V
–3 A
–10 V
–I D = –1, –2 A
–40
0
40
80
120
160
Case Temperature Tc (°C)

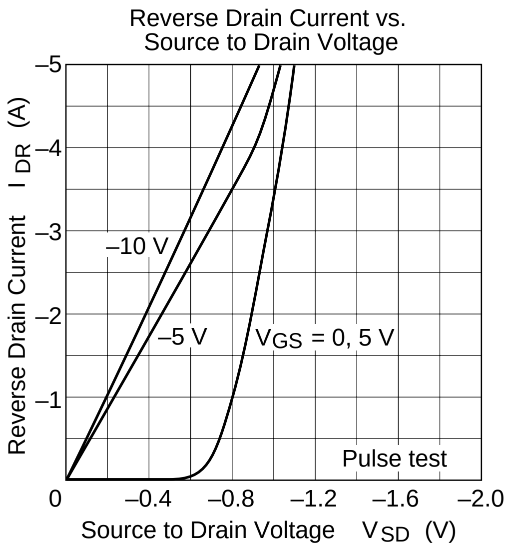

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
10
5
2
1
0.5
0.2
0.1
25°C
Tc = –25°C
75°C
Pulse test
VDS = –10 V
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

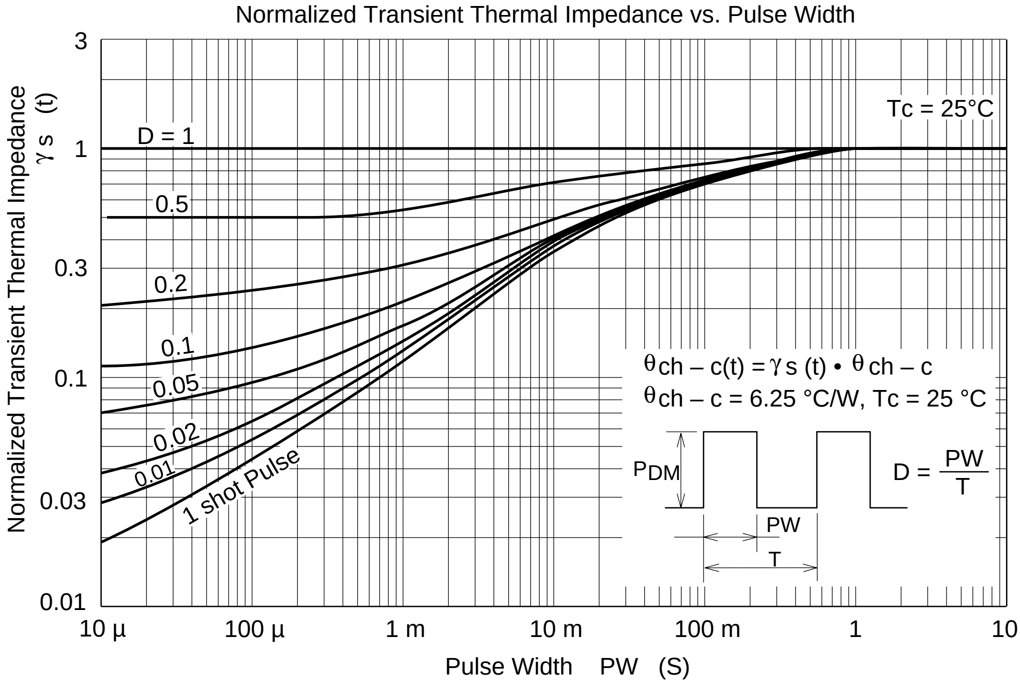

Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
1000
500
200
100
50
20
10
di/dt = 50 A/µs
V_{GS} = 0
Ta = 25°C
Pulse test
–0.1
–0.2
–0.5
–1
–2
–5
–10
Reverse Drain Current I_{DR} (A)

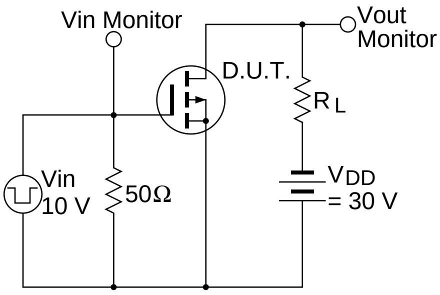

Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
2000
1000
500
200
100
50
20
Ciss
Coss
Crss
V_{GS} = 0
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage V_{DS} (V)

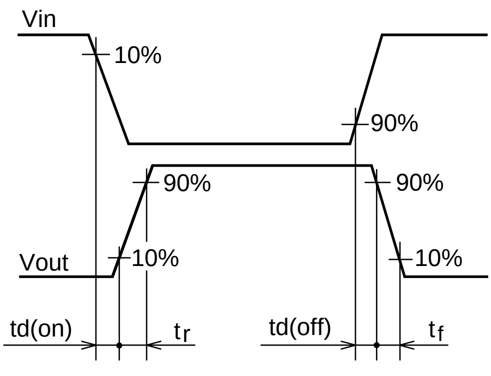

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
0
–20
–40
–60
–80
–100
0
–4
–8
–12
–16
–20
V_{DD}= –10 V
–25 V
–50 V
V_{DD}= –50 V
–25 V
–10 V
V_{DS}
V_{GS}
I_D= –5 A
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t_d(off)
t_f
t_r
t_d(on)
V_{GS} = –10 V
V_{DD}= –30 V
PW ≒ 2 µs
duty ≤ 1%
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I_D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
–5
–4
–3
–2
–1
–10 V
–5 V
VGS = 0, 5 V
Pulse test
0
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage VSD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10


Vin Monitor
Vout Monitor
D.U.T.
RL
Vin 10 V
50Ω
VDD = 30 V


Vin
10%
90%
Vout
90%
90%
10%
10%
td(on)
tr
td(off)
tf

2SJ246(L), 2SJ246(S)

SILICON P-CHANNEL MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4V gate drive device can be driven from 5V source.
- Suitable for Switching regulator, DC – DC converter

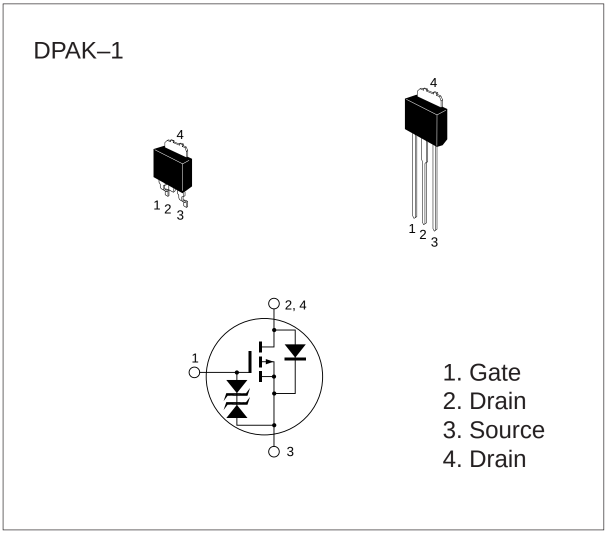


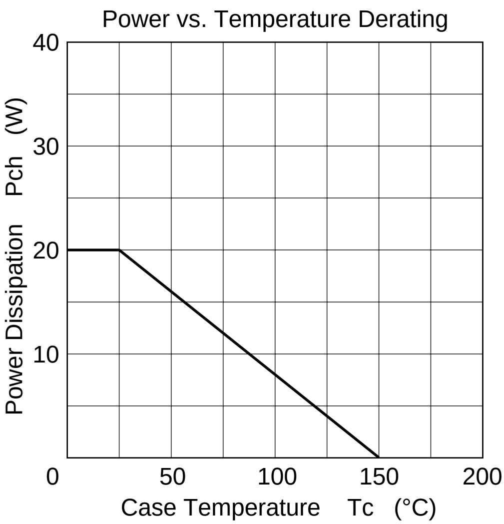
Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–7	A
Drain peak current	$I_{D(pulse)}$*	–28	A
Body–drain diode reverse drain current	I_{DR}	–7	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

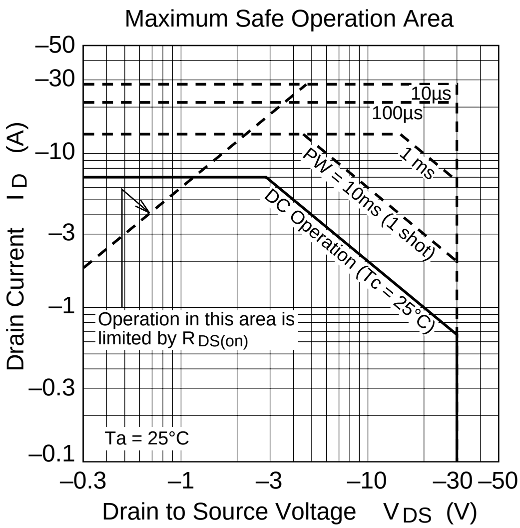
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

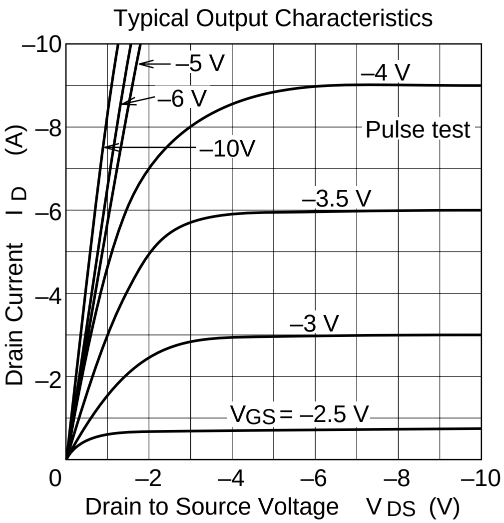
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.17	Ω	I_D = –4 A V_{GS} = –10 V
		—	0.21	0.31	Ω	I_D = –4 A V_{GS} = –4 V
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	V_{DS} = –10 V I_D = –4 A
Input capacitance	Ciss	—	660	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	465	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	180	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = –10 V
Rise time	t_r	—	55	—	ns	I_D = –4 V
Turn–off delay time	$t_{d(off)}$	—	135	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	135	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.2	—	V	I_F = –7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	µs	I_F = –7 A, V_{GS} = 0, di_F / dt = 50 A / µs



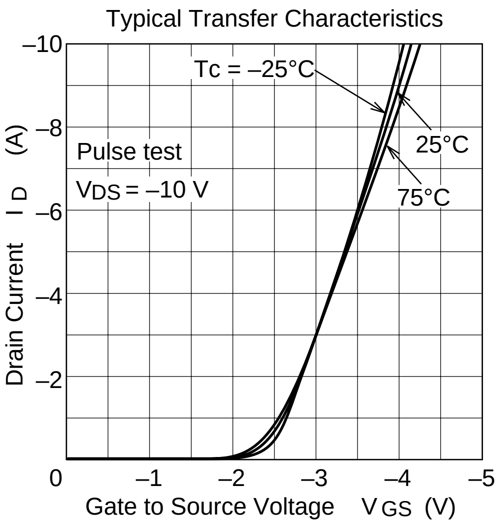
Power vs. Temperature Derating
Power Dissipation Pch (W)
Case Temperature Tc (°C)
0
10
20
30
40
50
100
150
200



Maximum Safe Operation Area
Drain Current I D (A)
Drain to Source Voltage V DS (V)
10µs
100µs
1 ms
PW = 10ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R DS(on)
Ta = 25°C
–50
–30
–10
–3
–1
–0.3
–0.1
–0.3
–1
–3
–10
–30
–50

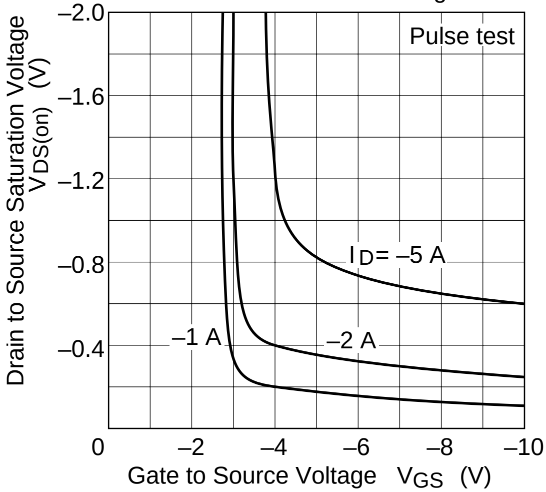


Typical Output Characteristics
Drain Current I D (A)
Drain to Source Voltage V DS (V)
–5 V
–6 V
–10V
–4 V
Pulse test
–3.5 V
–3 V
VGS = –2.5 V
–10
–8
–6
–4
–2
0
–2
–4
–6
–8
–10

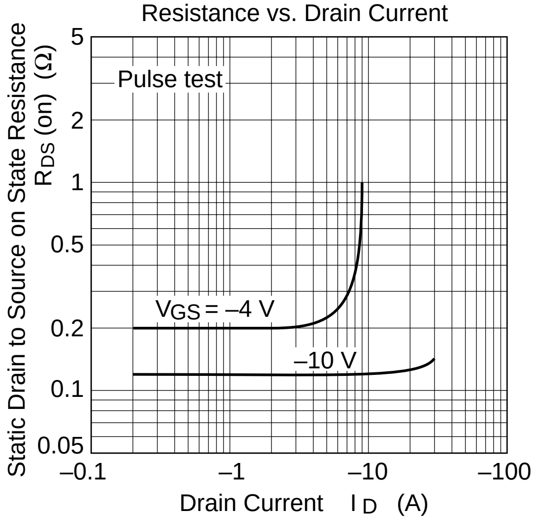


Typical Transfer Characteristics
Drain Current I D (A)
Gate to Source Voltage V GS (V)
Tc = –25°C
25°C
75°C
Pulse test
VDS = –10 V
–10
–8
–6
–4
–2
0
–1
–2
–3
–4
–5

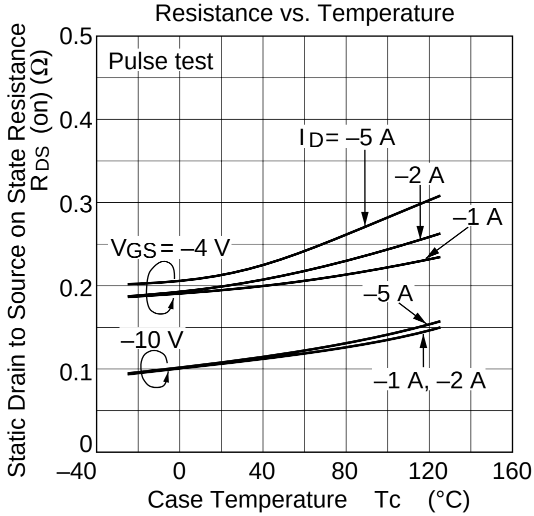
Drain to Source Saturation Voltage vs. Gate to Source Voltage



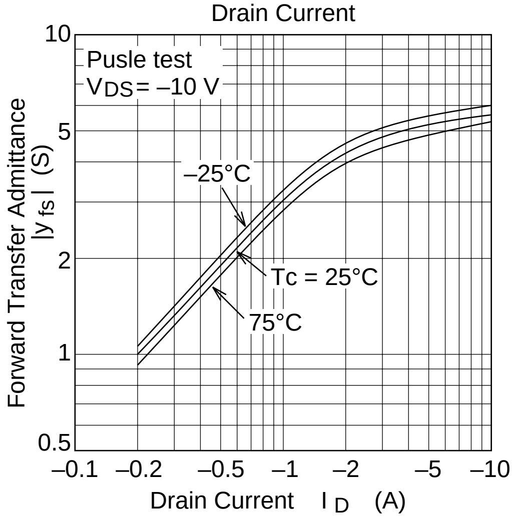
Static Drain to Source on State Resistance vs. Drain Current



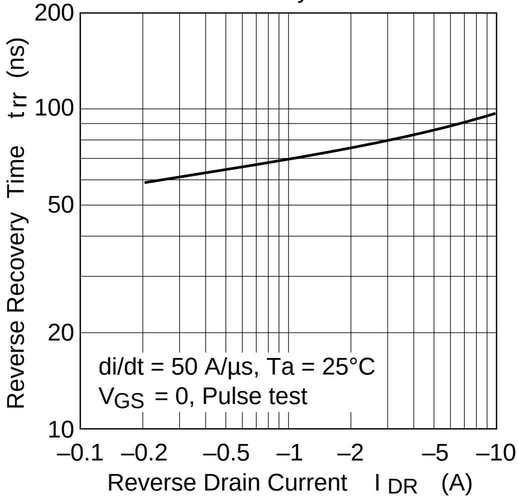
Static Drain to Source on State Resistance vs. Temperature



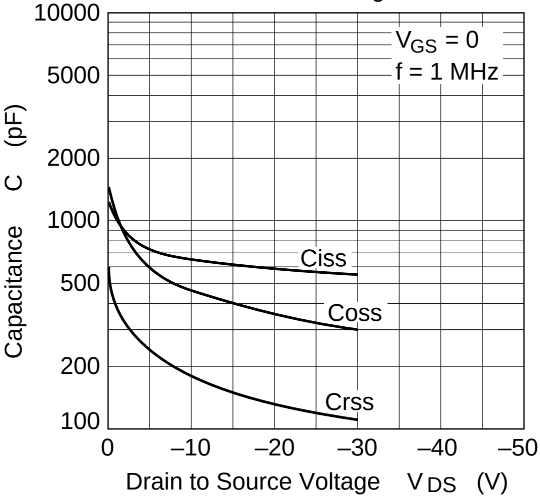
Forward Transfer Admittance vs. Drain Current



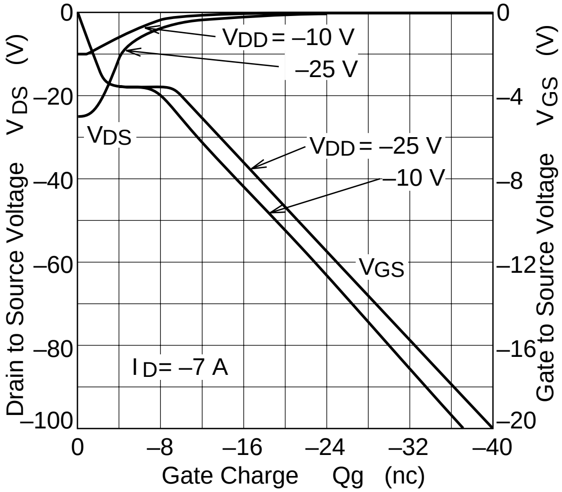
Body to Drain Diode Reverse Recovery Time



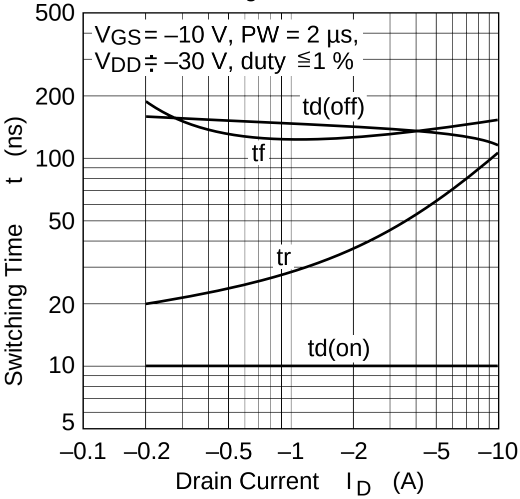
Typical Capacitance vs. Drain to Source Voltage

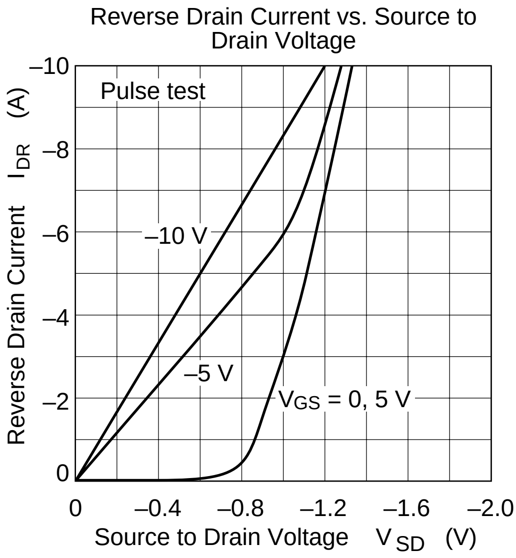


Dynamic Input Characteristics

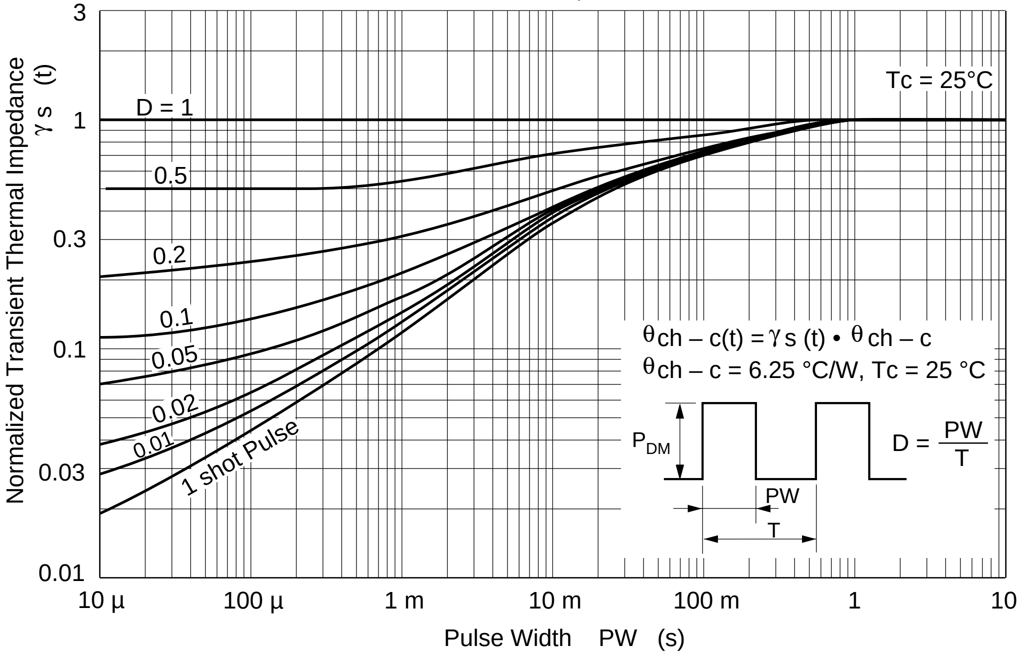


Switching Characteristics

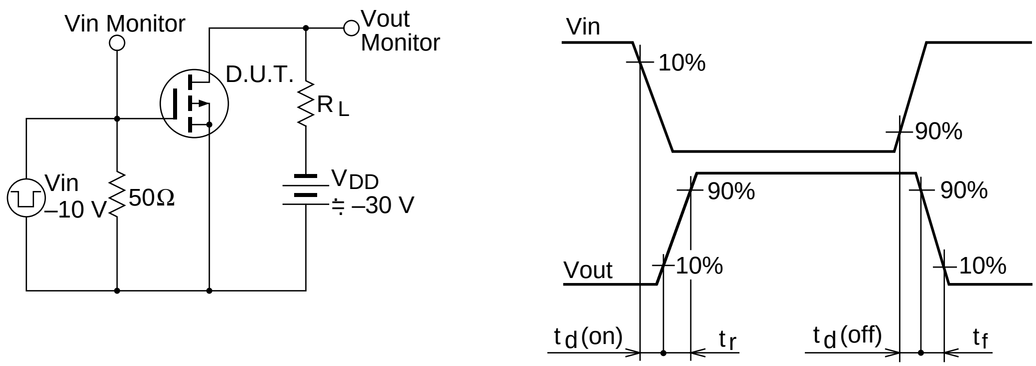



Reverse Drain Current vs. Source to Drain Voltage
Pulse test
–10 V
–5 V
V_{GS} = 0, 5 V
Reverse Drain Current I_{DR} (A)
–10
–8
–6
–4
–2
0
0
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage V_{SD} (V)

Normal Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit Waveform



2SJ247

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V Gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

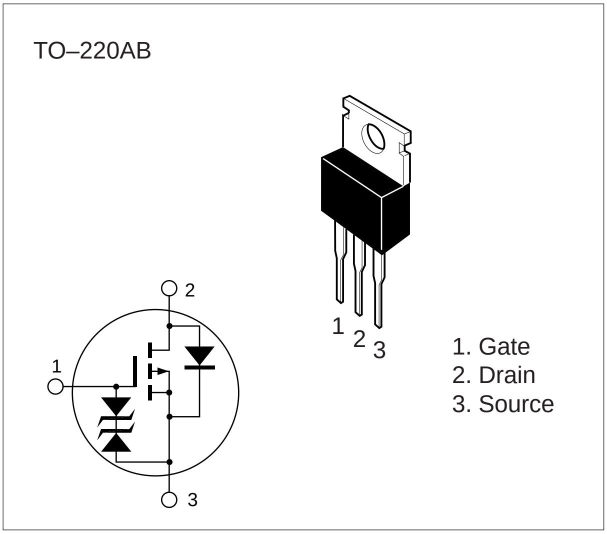


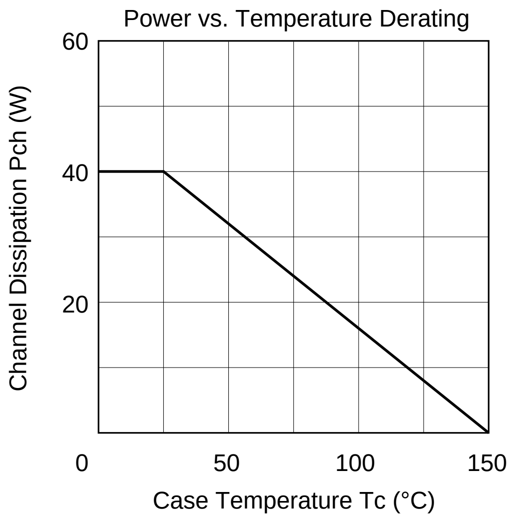
Table 1 Absolute Maximum Ratings (Ta = 25°C)

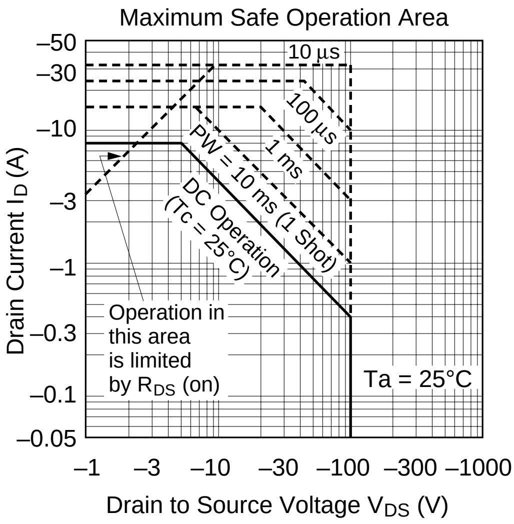
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–8	A
Drain peak current	$I_{D(pulse)}$*	–32	A
Body–drain diode reverse drain current	I_{DR}	–8	A
Channel dissipation	Pch**	40	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

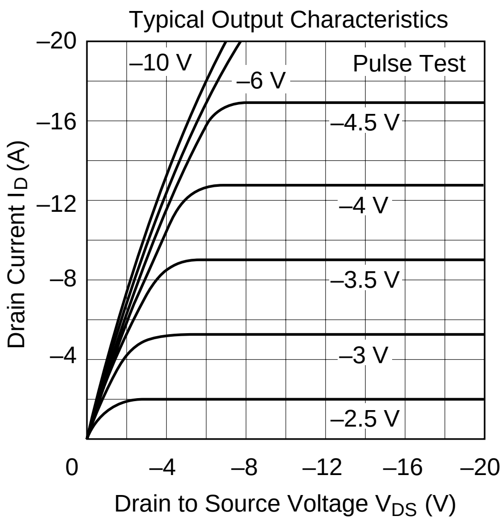
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc=25°C

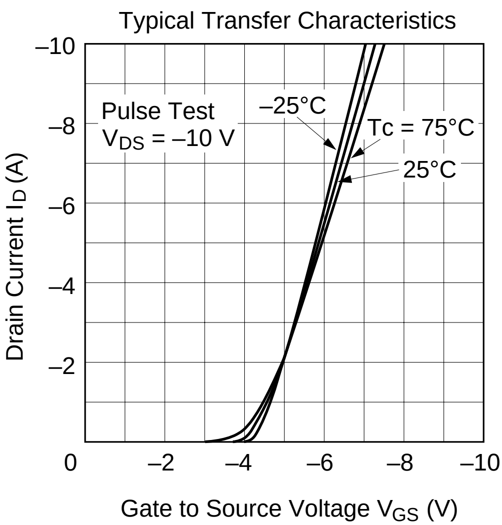
Table 2 Electrical Characteristics (Ta = 25°C)

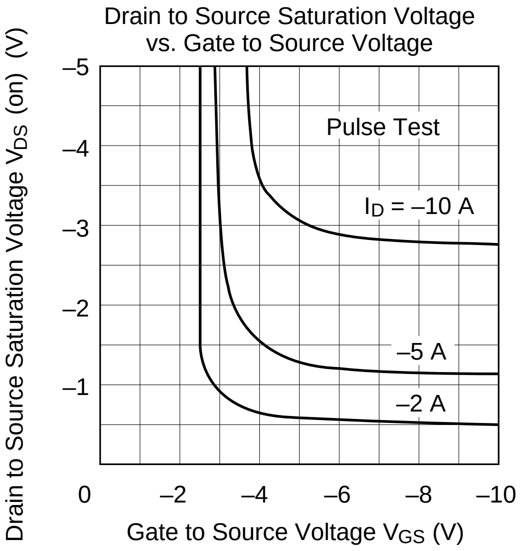
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–100	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.3	Ω	I_D = –4A V_{GS} = –10 V *
		—	0.3	0.45	Ω	I_D = –4 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.5	—	S	I_D = –4A V_{DS} = –10 V *
Input capacitance	Ciss	—	880	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	325	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	80	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	12	—	ns	I_D = –4A
Rise time	t_r	—	47	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	150	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	75	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	170	—	ns	I_F = –8 A, V_{GS} = 0, diF / dt = 50 A / µs


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)

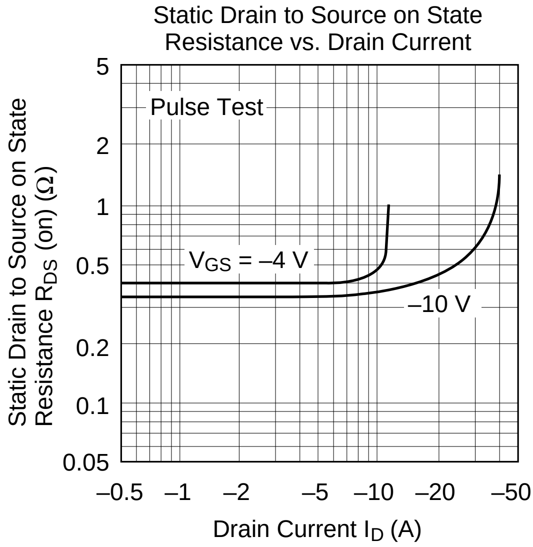

Maximum Safe Operation Area
Drain Current I_D (A)
–50
–30
–10
–3
–1
–0.3
–0.1
–0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation
(Tc = 25°C)
Operation in
this area
is limited
by R_{DS} (on)
Ta = 25°C
–1
–3
–10
–30
–100
–300
–1000
Drain to Source Voltage V_{DS} (V)


Typical Output Characteristics
Drain Current I_D (A)
–20
–16
–12
–8
–4
–10 V
–6 V
Pulse Test
–4.5 V
–4 V
–3.5 V
–3 V
–2.5 V
0
–4
–8
–12
–16
–20
Drain to Source Voltage V_{DS} (V)

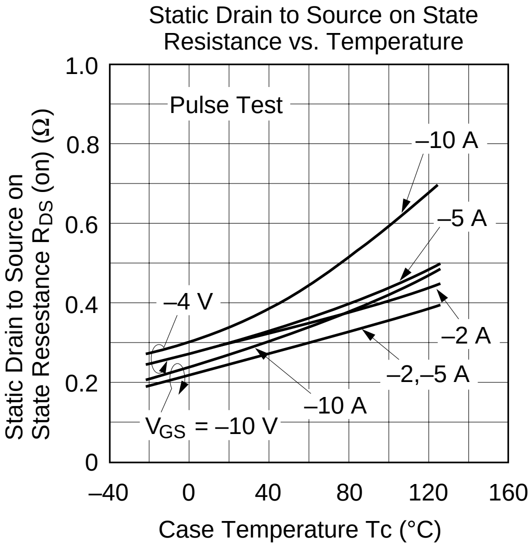

Typical Transfer Characteristics
Drain Current I_D (A)
–10
–8
–6
–4
–2
Pulse Test
V_{DS} = –10 V
–25°C
Tc = 75°C
25°C
0
–2
–4
–6
–8
–10
Gate to Source Voltage V_{GS} (V)



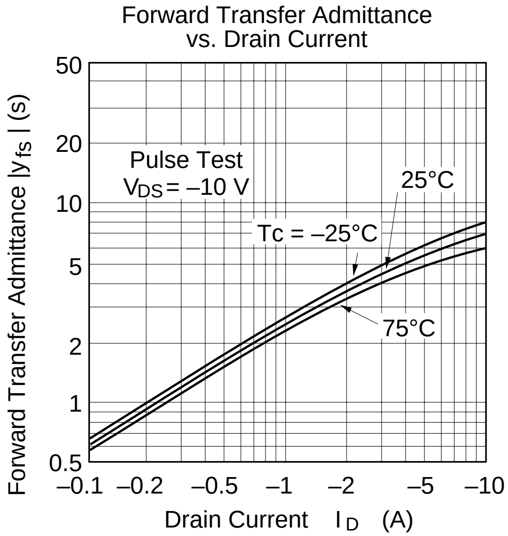
Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = –10 A
–5 A
–2 A
Drain to Source Saturation Voltage V_{DS} (on) (V)
–5
–4
–3
–2
–1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V_{GS} (V)



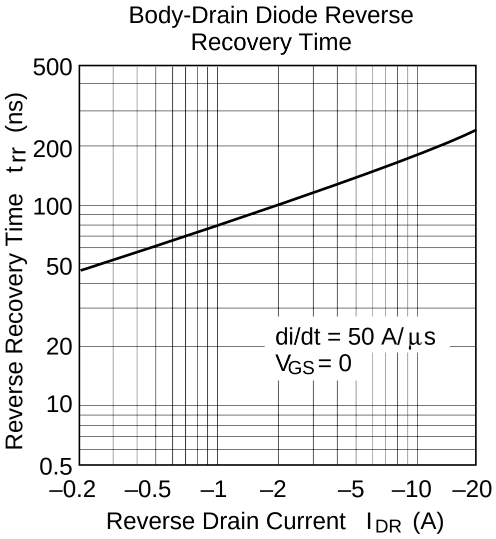
Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = –4 V
–10 V
Static Drain to Source on State Resistance R_{DS} (on) (Ω)
5
2
1
0.5
0.2
0.1
0.05
–0.5
–1
–2
–5
–10
–20
–50
Drain Current I_D (A)

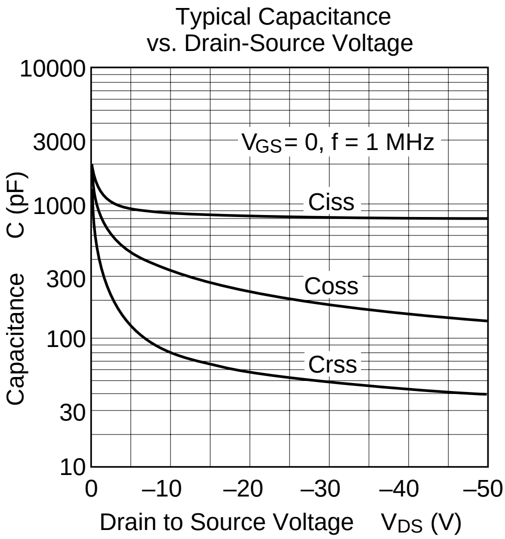


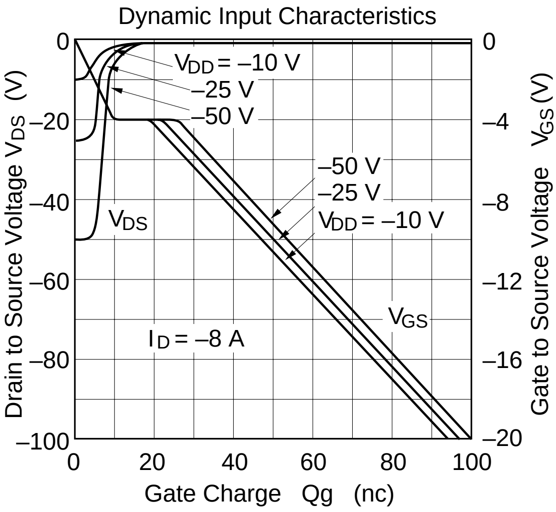
Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
–10 A
–5 A
–4 V
–2 A
–2,–5 A
–10 A
V_{GS} = –10 V
Static Drain to Source on State Resestance R_{DS} (on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

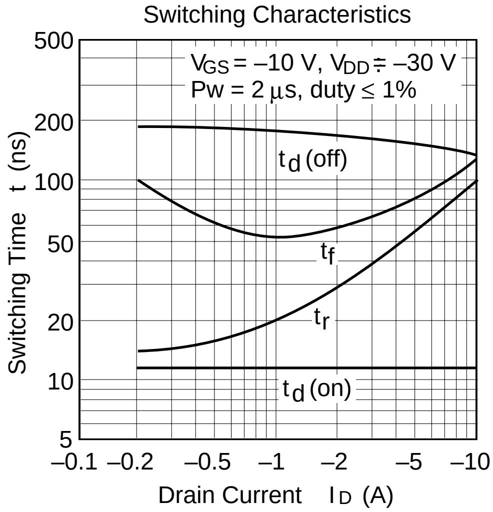


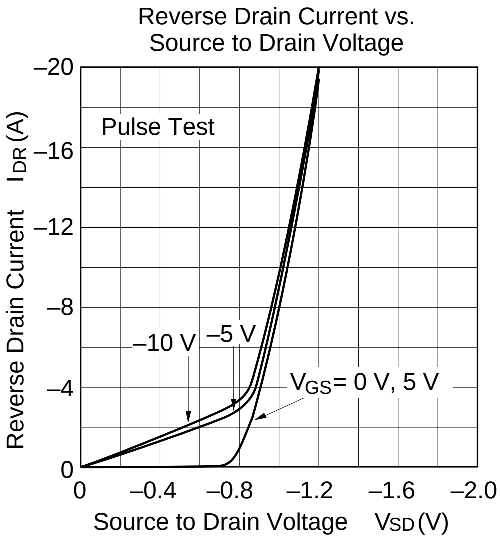
Forward Transfer Admittance
vs. Drain Current
Pulse Test
V_{DS} = –10 V
25°C
Tc = –25°C
75°C
Forward Transfer Admittance $|y_{fs}|$ (s)
50
20
10
5
2
1
0.5
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I_D (A)


Body-Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
Reverse Drain Current IDR (A)
di/dt = 50 A/µs
VGS = 0
500
200
100
50
20
10
0.5
–0.2
–0.5
–1
–2
–5
–10
–20


Typical Capacitance
vs. Drain-Source Voltage
Capacitance C (pF)
Drain to Source Voltage VDS (V)
VGS = 0, f = 1 MHz
Ciss
Coss
Crss
10000
3000
1000
300
100
30
10
0
–10
–20
–30
–40
–50


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
VDD = –10 V
–25 V
–50 V
–50 V
–25 V
VDD = –10 V
VDS
VGS
ID = –8 A
0
–20
–40
–60
–80
–100
0
–4
–8
–12
–16
–20
0
20
40
60
80
100


Switching Characteristics
Switching Time t (ns)
Drain Current ID (A)
VGS = –10 V, VDD ≒ –30 V
Pw = 2 µs, duty ≤ 1%
td (off)
tf
tr
td (on)
500
200
100
50
20
10
5
–0.1
–0.2
–0.5
–1
–2
–5
–10


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
–20
–16
–12
–8
–4
0
0
–0.4
–0.8
–1.2
–1.6
–2.0
–10 V
–5 V
VGS = 0 V, 5 V
Reverse Drain Current IDR (A)
Source to Drain Voltage VSD (V)

2SJ278

Silicon P Channel MOS FET

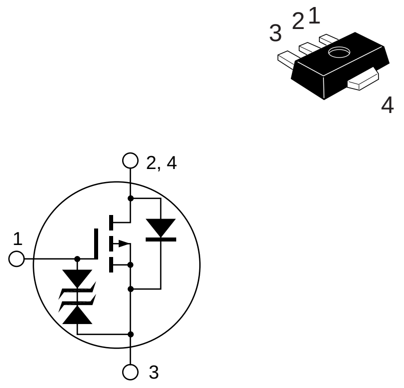
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

UPAK



1. Gate
2. Drain
3. Source
4. Drain

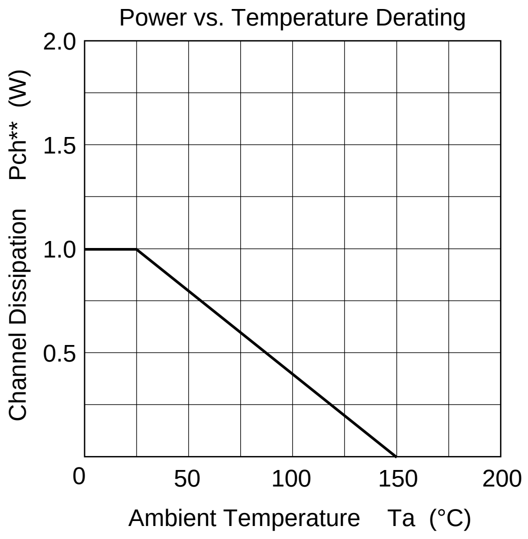
Table 1 Absolute Maximum Ratings (Ta = 25°C)

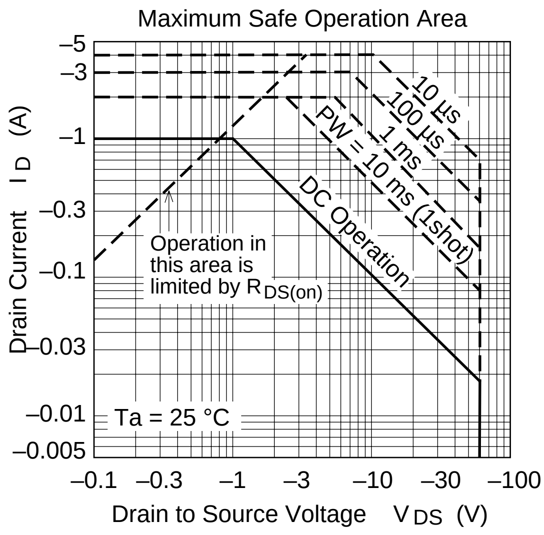
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–1	A
Drain peak current	$I_{D(pulse)}$*	–4	A
Body–drain diode reverse drain current	I_{DR}	–1	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

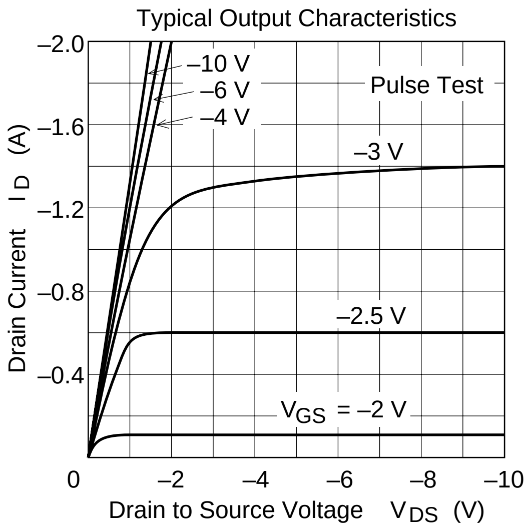
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value on the alumina ceramic board (12.5 x 20 x 0.7mm)
*** Marking is "MY".

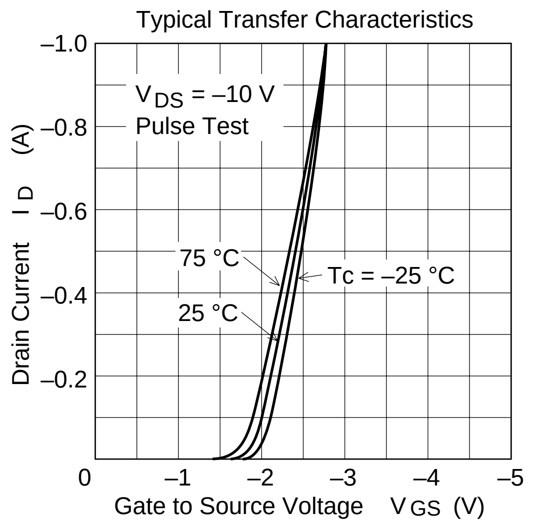
Table 2 Electrical Characteristics (Ta = 25°C)

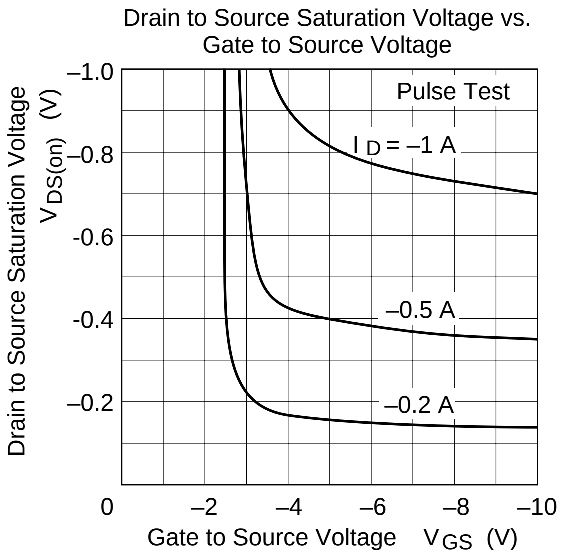
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.83	Ω	I_D = –0.5 A V_{GS} = –10 V *
		—	0.9	1.2	Ω	I_D = –0.5 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.6	1.0	—	S	I_D = –0.5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	160	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	80	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	28	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	7	—	ns	I_D = –0.5 A
Rise time	t_r	—	8	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	30	—	ns	R_L = 60 Ω
Fall time	t_f	—	25	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –1 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	µs	I_F = –1 A, V_{GS} = 0, diF / dt = 50 A / µs

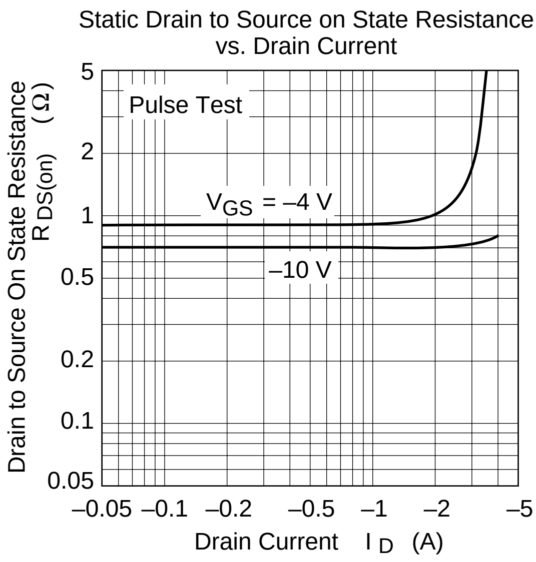

Power vs. Temperature Derating
Channel Dissipation Pch** (W)
2.0
1.5
1.0
0.5
0
50
100
150
200
Ambient Temperature Ta (°C)

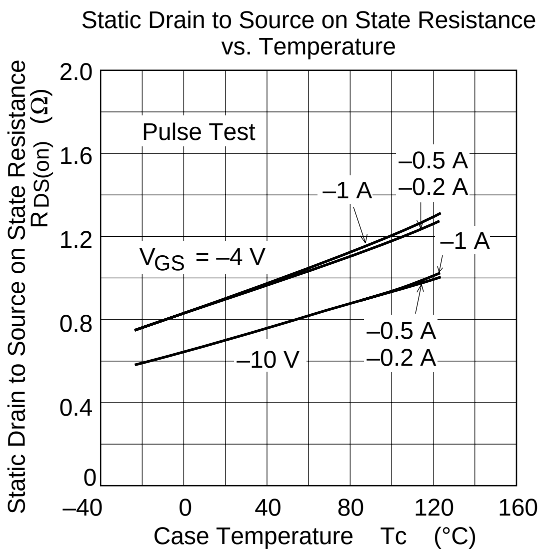

Maximum Safe Operation Area
Drain Current I D (A)
–5
–3
–1
–0.3
–0.1
–0.03
–0.01
–0.005
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation
Operation in this area is limited by R DS(on)
Ta = 25 °C
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

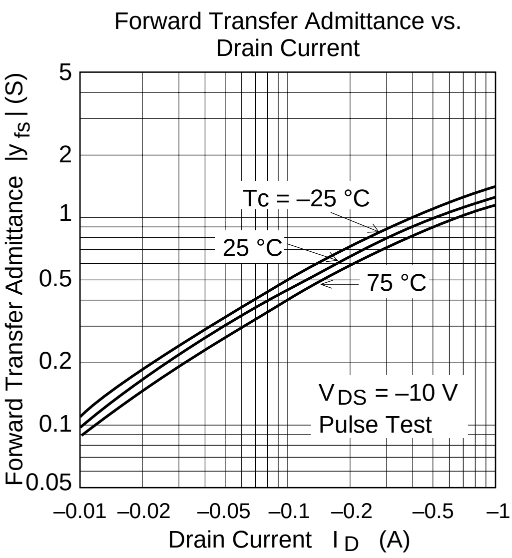

Typical Output Characteristics
Drain Current I D (A)
–2.0
–1.6
–1.2
–0.8
–0.4
–10 V
–6 V
–4 V
Pulse Test
–3 V
–2.5 V
VGS = –2 V
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
–1.0
–0.8
–0.6
–0.4
–0.2
V DS = –10 V
Pulse Test
75 °C
25 °C
Tc = –25 °C
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

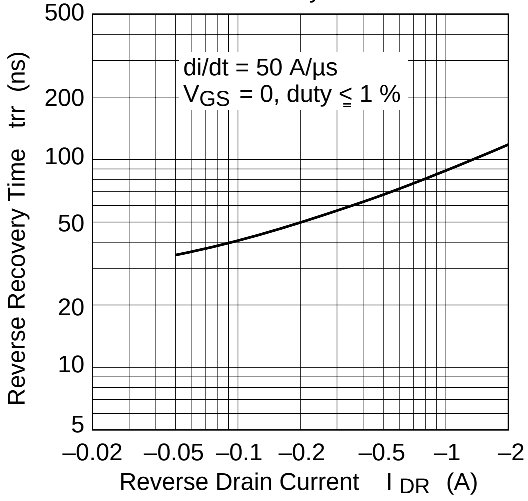

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –1 A
–0.5 A
–0.2 A
Drain to Source Saturation Voltage
V DS(on) (V)
–1.0
–0.8
-0.6
-0.4
–0.2
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)


Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –4 V
–10 V
Drain to Source On State Resistance
R DS(on) (Ω)
5
2
1
0.5
0.2
0.1
0.05
–0.05
–0.1
–0.2
–0.5
–1
–2
–5
Drain Current I D (A)

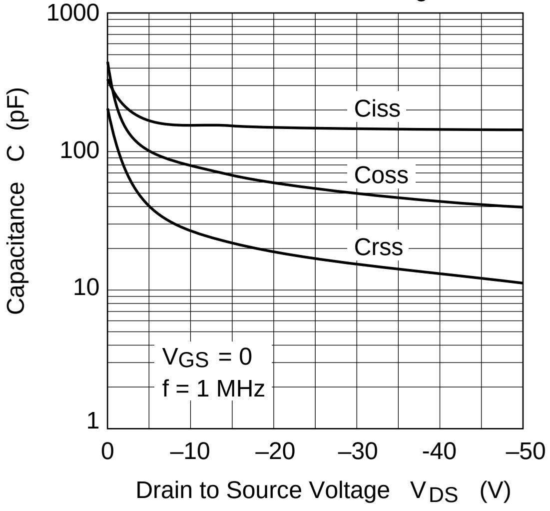

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
–0.5 A
–0.2 A
–1 A
V GS = –4 V
–1 A
–0.5 A
–0.2 A
–10 V
Static Drain to Source on State Resistance
R DS(on) (Ω)
2.0
1.6
1.2
0.8
0.4
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs | (S)
5
2
1
0.5
0.2
0.1
0.05
–0.01
–0.02
–0.05
–0.1
–0.2
–0.5
–1
Drain Current I D (A)

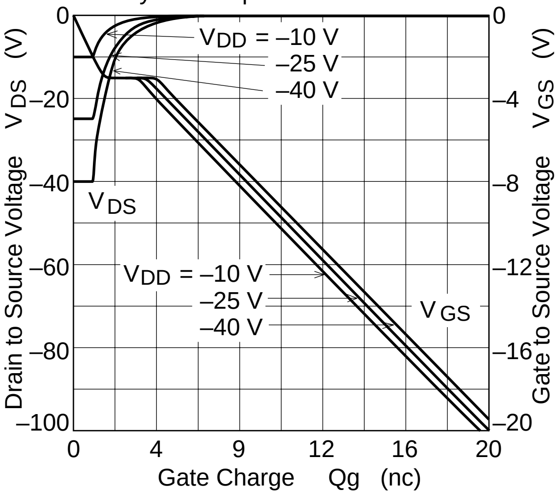
Body–Drain Diode Reverse Recovery Time



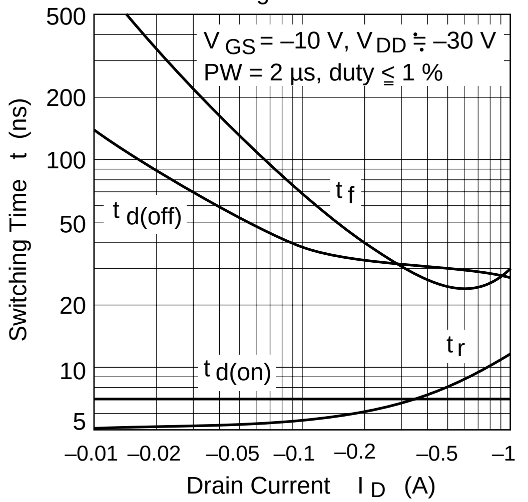
Typical Capacitance vs. Drain to Source Voltage



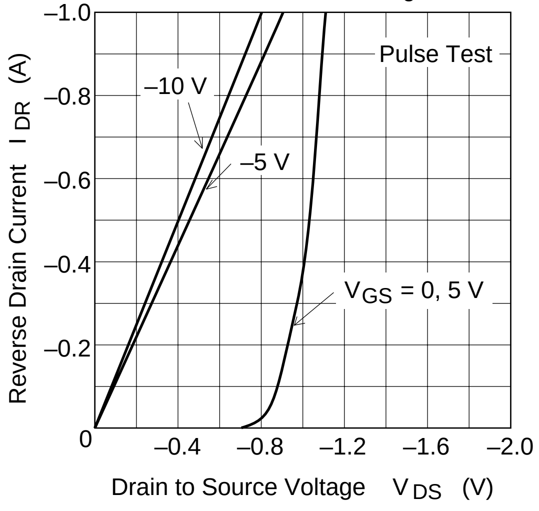
Dynamic Input Characteristics



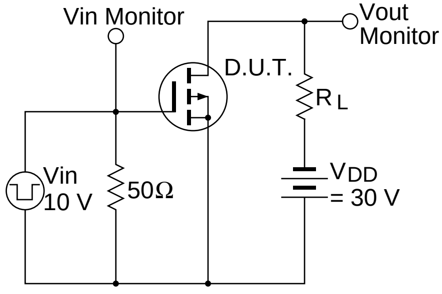
Switching Characteristics



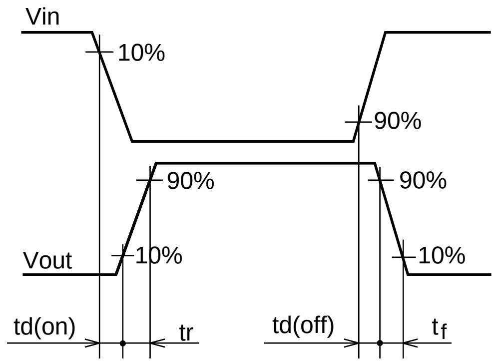
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit



Waveforms



2SJ279 (L) , 2SJ279 (S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

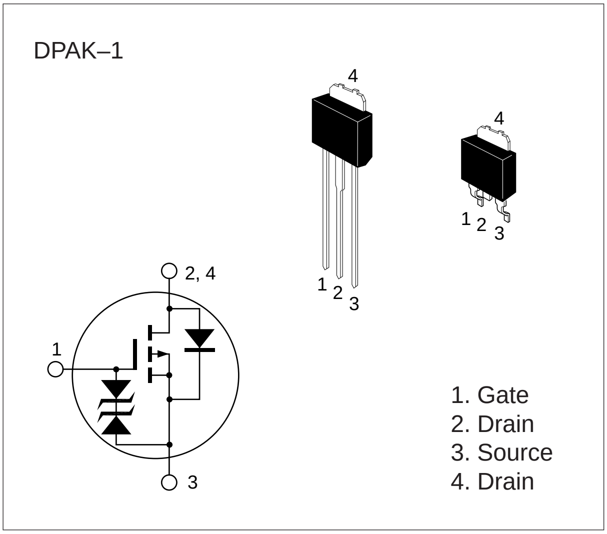


Table 1 Absolute Maximum Ratings (Ta = 25°C)

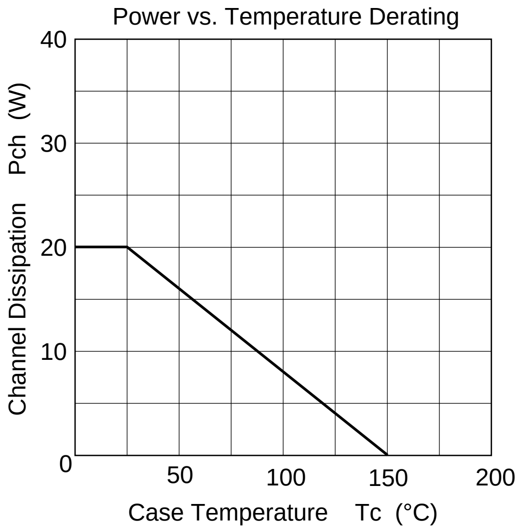
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–5	A
Drain peak current	$I_{D(pulse)}$*	–20	A
Body–drain diode reverse drain current	I_{DR}	–5	A
Avalanche current	I_{AP}***	–5	A
Avalanche energy	E_{AR}***	2.1	mJ
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

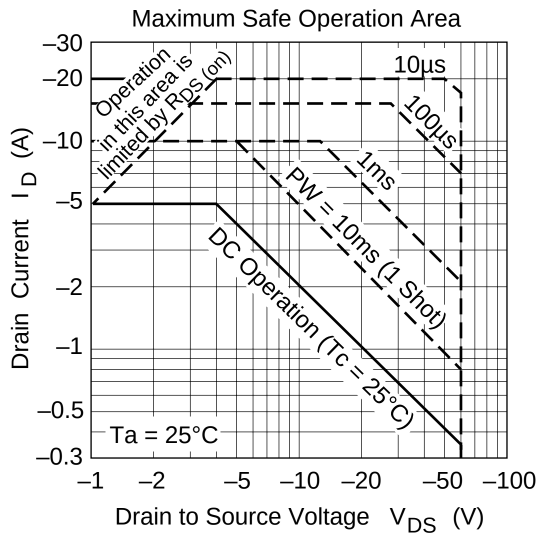
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

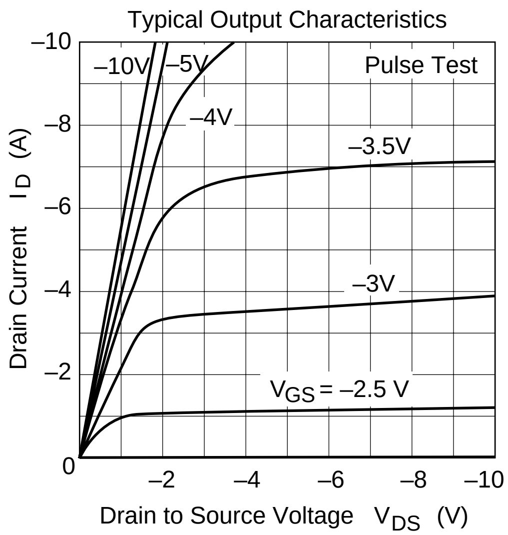
Table 2 Electrical Characteristics (Ta = 25°C)

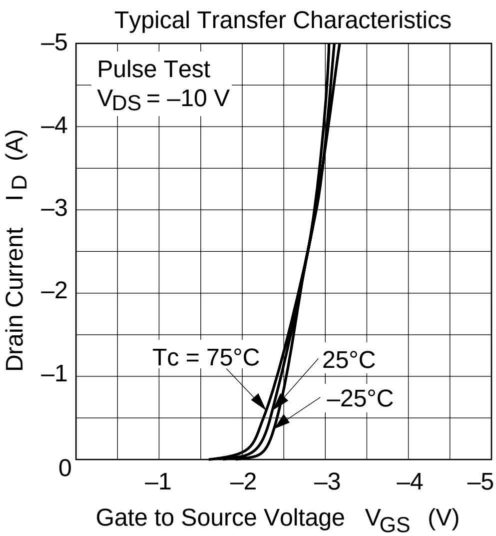
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.18	0.20	Ω	I_D = –3 A V_{GS} = –10 V *
		—	0.23	0.27	Ω	I_D = –3 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5	—	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance	Ciss	—	690	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	340	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	110	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = –3 A
Rise time	t_r	—	35	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	125	—	ns	R_L = 10 Ω
Fall time	t_f	—	75	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.2	—	V	I_F = –5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	140	—	µs	I_F = –5 A, V_{GS} = 0, diF / dt = 50 A / µs

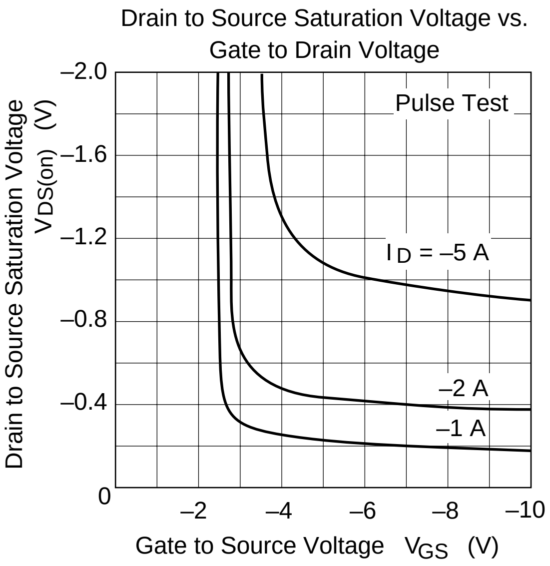
* Pulse Test

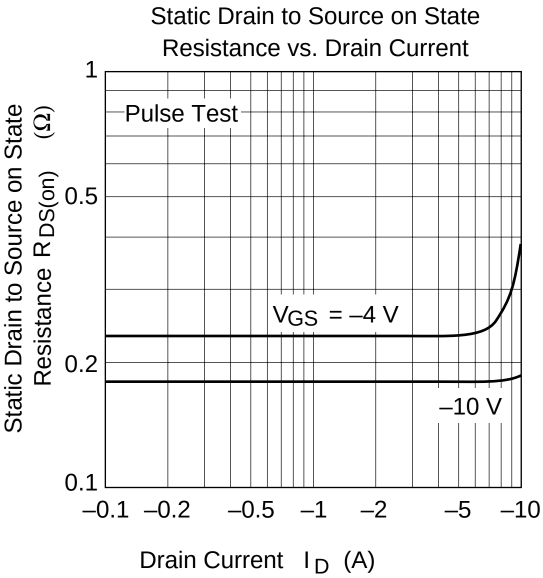

Power vs. Temperature Derating
40
30
20
10
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

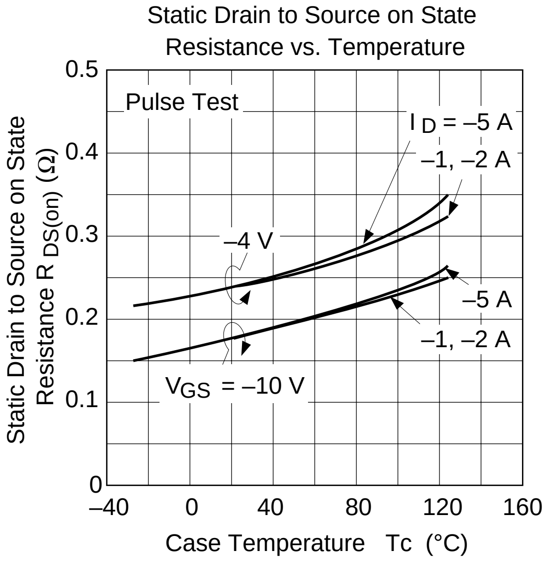

Maximum Safe Operation Area
–30
–20
–10
–5
–2
–1
–0.5
–0.3
Operation in this area is limited by RDS (on)
10µs
100µs
1ms
PW = 10ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C
Drain Current I D (A)
–1
–2
–5
–10
–20
–50
–100
Drain to Source Voltage VDS (V)

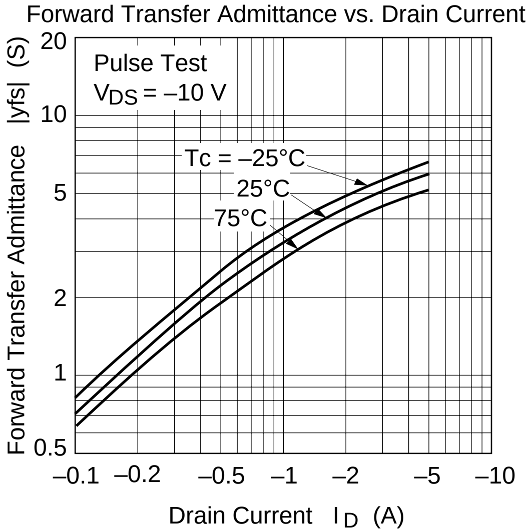

Typical Output Characteristics
–10
–8
–6
–4
–2
0
–10V
–5V
–4V
Pulse Test
–3.5V
–3V
VGS = –2.5 V
Drain Current I D (A)
–2
–4
–6
–8
–10
Drain to Source Voltage VDS (V)

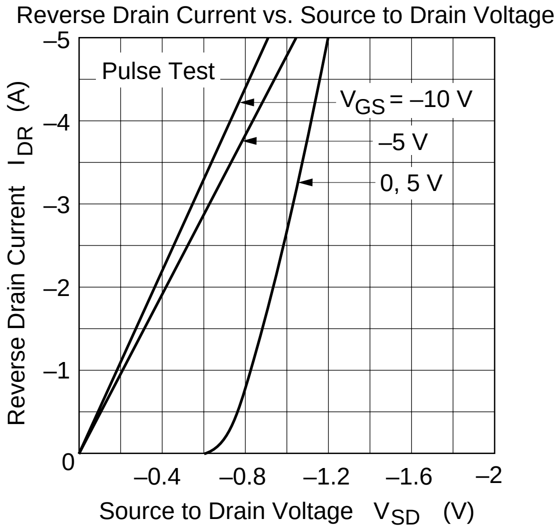

Typical Transfer Characteristics
–5
–4
–3
–2
–1
0
Pulse Test
VDS = –10 V
Tc = 75°C
25°C
–25°C
Drain Current I D (A)
–1
–2
–3
–4
–5
Gate to Source Voltage VGS (V)

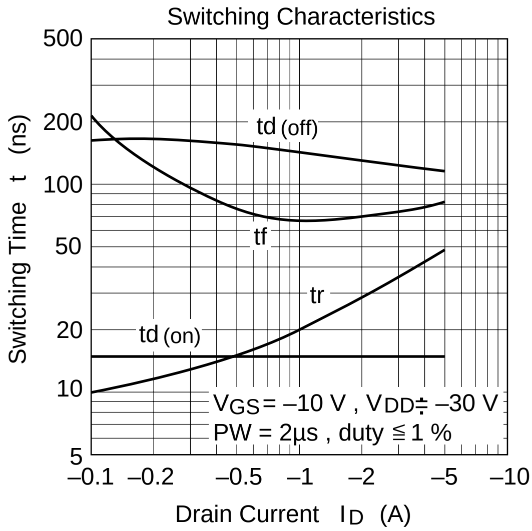

Drain to Source Saturation Voltage vs.
Gate to Drain Voltage
Pulse Test
I D = –5 A
–2 A
–1 A
–2.0
–1.6
–1.2
–0.8
–0.4
0
–2
–4
–6
–8
–10
Drain to Source Saturation Voltage
VDS(on) (V)
Gate to Source Voltage VGS (V)

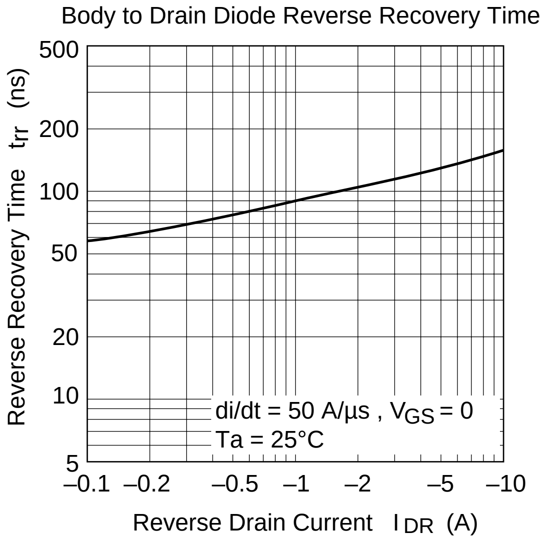

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
VGS = –4 V
–10 V
1
0.5
0.2
0.1
–0.1
–0.2
–0.5
–1
–2
–5
–10
Static Drain to Source on State
Resistance RDS(on) (Ω)
Drain Current I D (A)

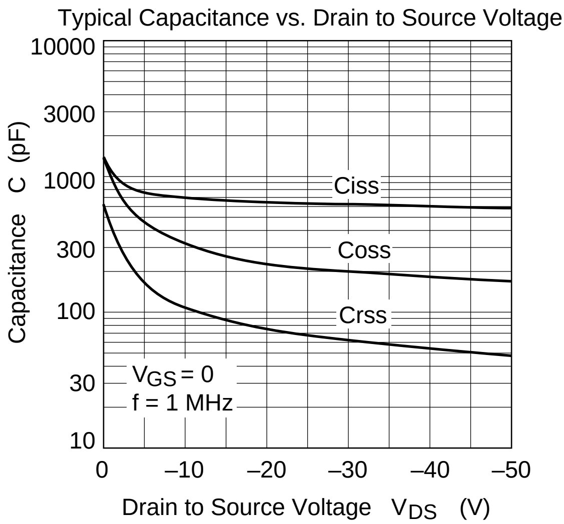

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I D = –5 A
–1, –2 A
–4 V
–5 A
–1, –2 A
VGS = –10 V
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Static Drain to Source on State
Resistance R DS(on) (Ω)
Case Temperature Tc (°C)


Forward Transfer Admittance vs. Drain Current
Pulse Test
VDS = –10 V
Tc = –25°C
25°C
75°C
20
10
5
2
1
0.5
–0.1
–0.2
–0.5
–1
–2
–5
–10
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)

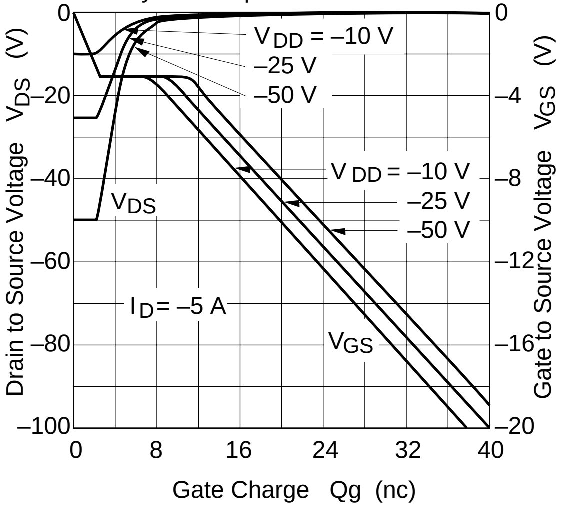

Reverse Drain Current vs. Source to Drain Voltage
Pulse Test
VGS = –10 V
–5 V
0, 5 V
Reverse Drain Current IDR (A)
–5
–4
–3
–2
–1
0
–0.4
–0.8
–1.2
–1.6
–2
Source to Drain Voltage VSD (V)


Switching Characteristics
td (off)
tf
tr
td (on)
VGS = –10 V , VDD ≒ –30 V
PW = 2µs , duty ≦ 1 %
Switching Time t (ns)
500
200
100
50
20
10
5
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current ID (A)

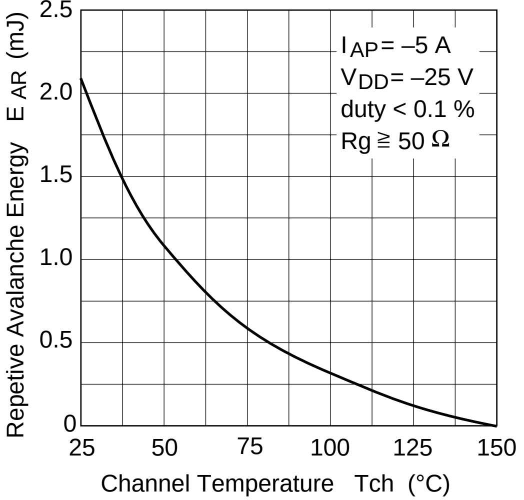

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs , VGS = 0
Ta = 25°C
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
–0.1
–0.2
–0.5
–1
–2
–5
–10
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)

Dynamic Input Characteristics

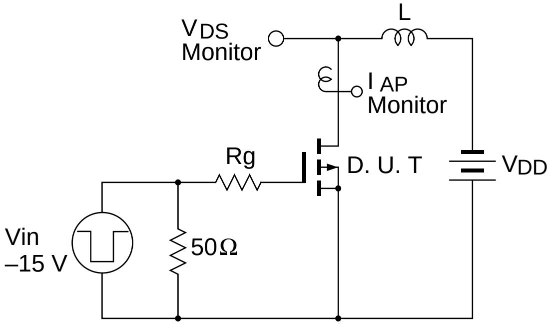


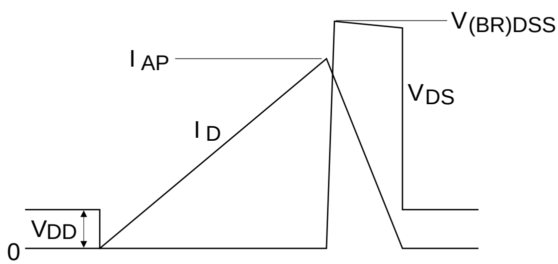
Maximum Avalanche Energy vs.
Channel Temperature Derationg

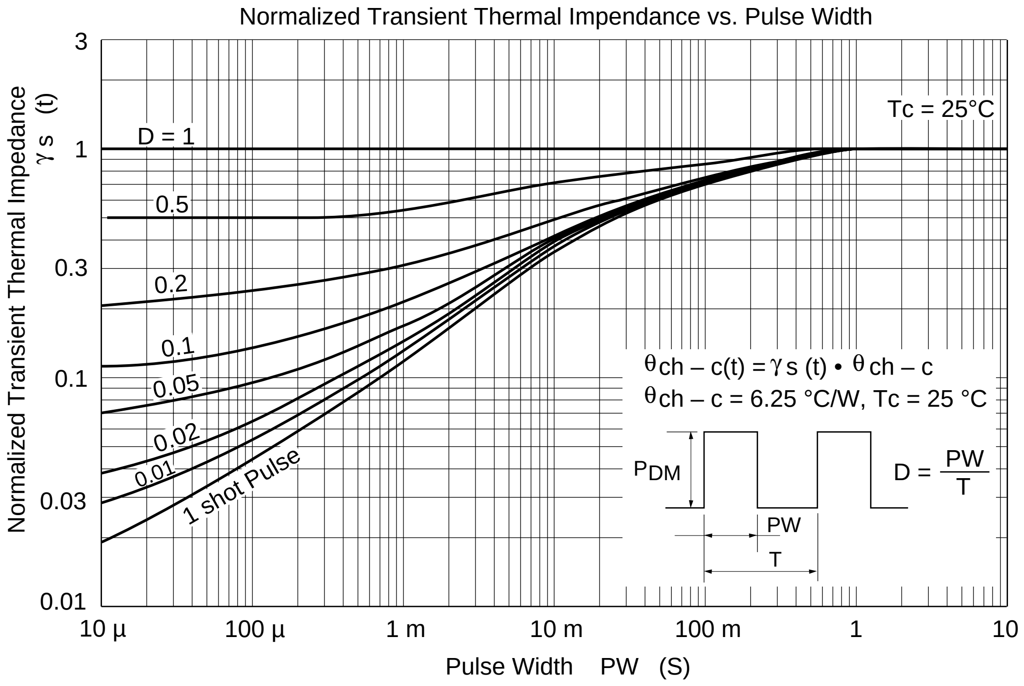


Avalanche Test Circuit and Waveform

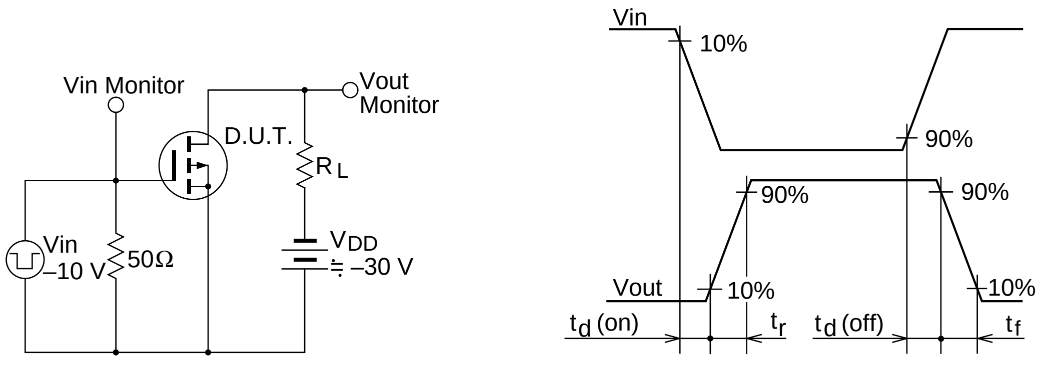
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$







Switching Time Test Circuit and Waveform



2SJ280(L), 2SJ280(S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

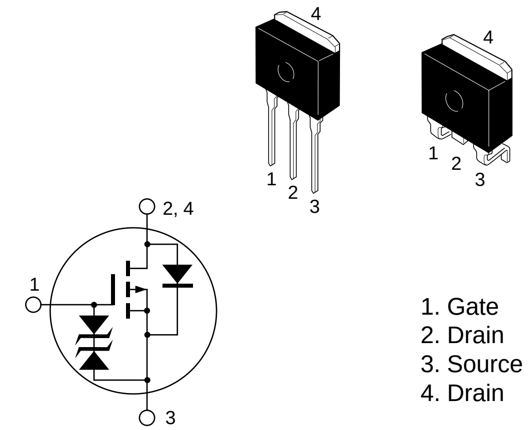


Table 1 Absolute Maximum Ratings (Ta = 25°C)

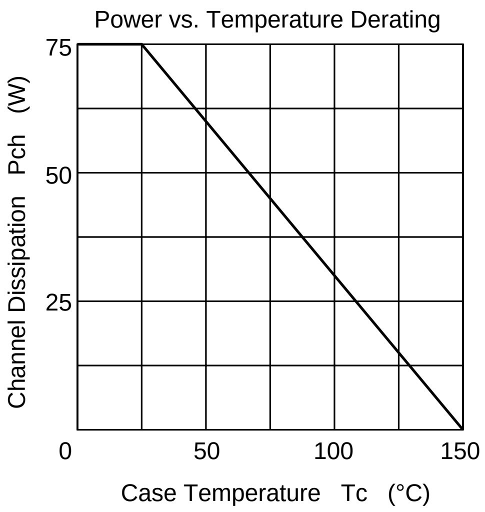
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–30	A
Drain peak current	$I_{D(pulse)}$*	–120	A
Body–drain diode reverse drain current	I_{DR}	–30	A
Avalanche current	I_{AP}***	–30	A
Avalanche energy	E_{AR}***	77	mJ
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

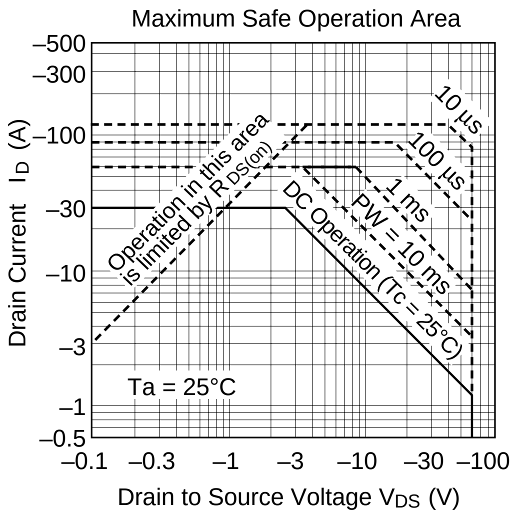
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

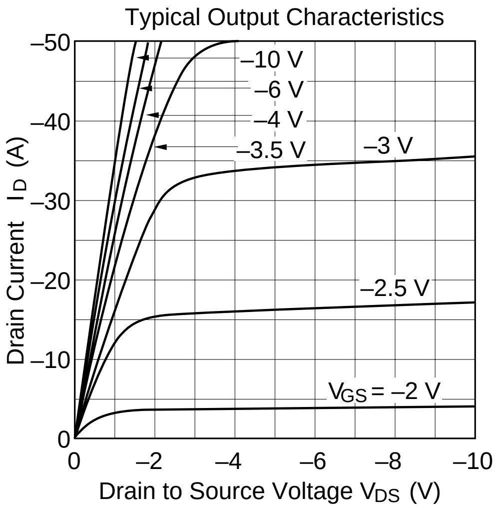
Table 2 Electrical Characteristics (Ta = 25°C)

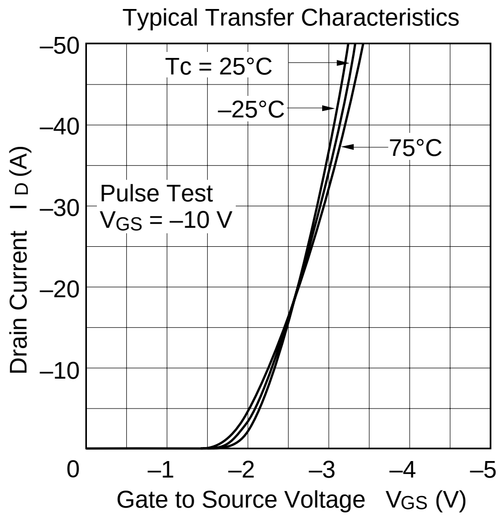
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.043	Ω	I_D = –15 A V_{GS} = –10 V *
		—	0.045	0.06	Ω	I_D = –15 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	17	25	—	S	I_D = –15 A V_{DS} = –10 V *
Input capacitance	Ciss	—	3300	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1500	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	480	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = –15 A
Rise time	t_r	—	170	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	500	—	ns	R_L = 2 Ω
Fall time	t_f	—	390	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.5	—	V	I_F = –30 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = –30 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

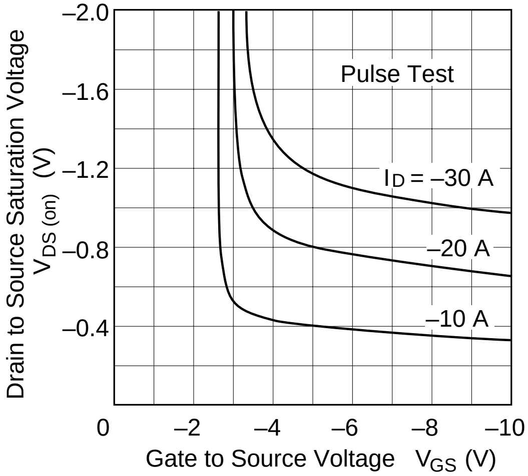

Power vs. Temperature Derating
Channel Dissipation Pch (W)
75
50
25
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
–500
–300
–100
–30
–10
–3
–1
–0.5
Operation in this area is limited by R DS(on)
10 µs
100 µs
1 ms
PW = 10 ms
DC Operation (Tc = 25°C)
Ta = 25°C
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage VDS (V)

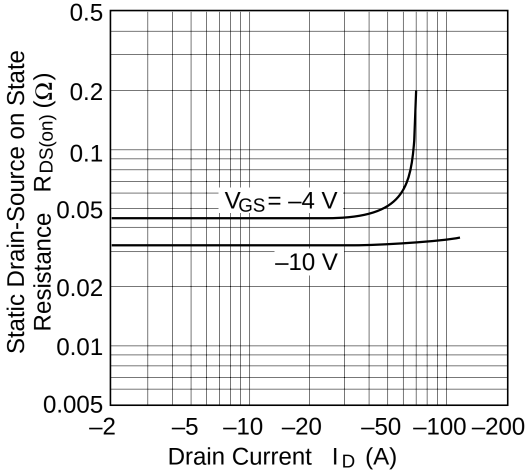

Typical Output Characteristics
Drain Current I D (A)
–50
–40
–30
–20
–10
0
–10 V
–6 V
–4 V
–3.5 V
–3 V
–2.5 V
VGS = –2 V
0
–2
–4
–6
–8
–10
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
Drain Current I D (A)
–50
–40
–30
–20
–10
Tc = 25°C
–25°C
75°C
Pulse Test
VGS = –10 V
0
–1
–2
–3
–4
–5
Gate to Source Voltage VGS (V)

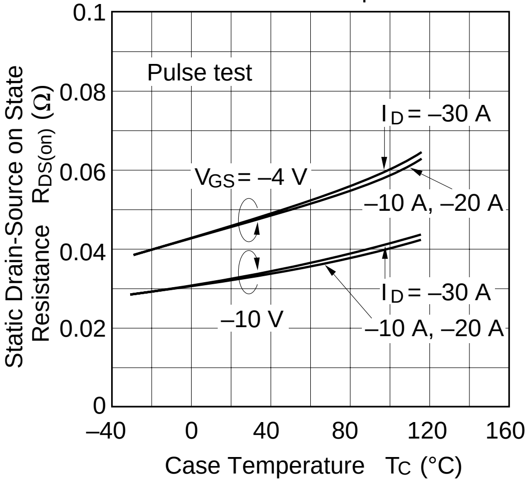
Drain-Source Saturation Voltage vs. Gate-Source Voltage



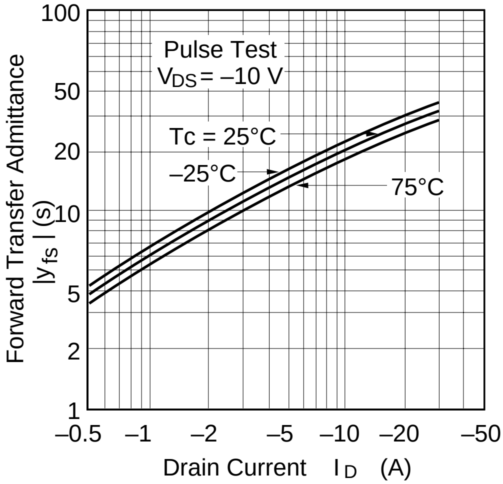
Static Drain-Source on State Resistance vs. Drain Current

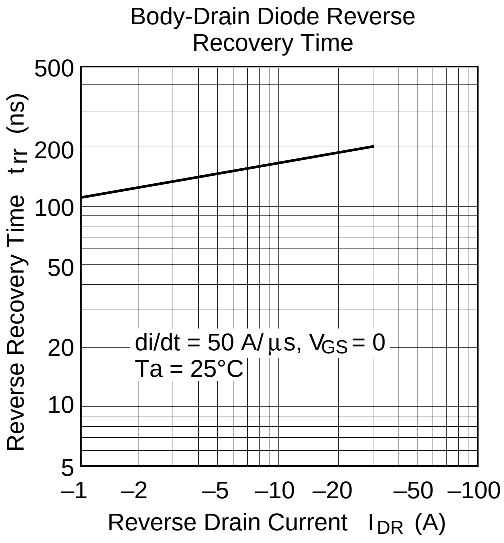


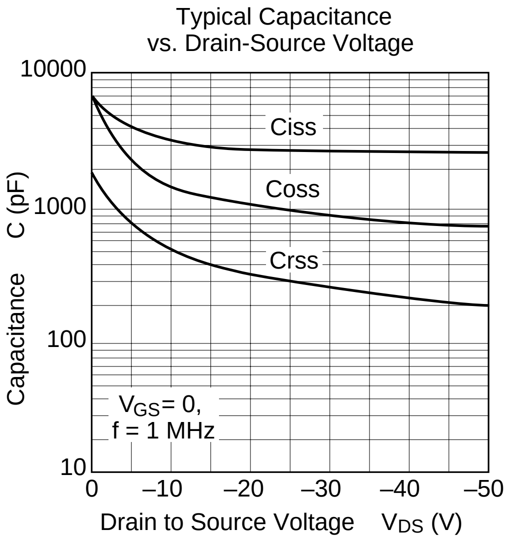
Static Drain-Source on State Resistance vs. Temperature

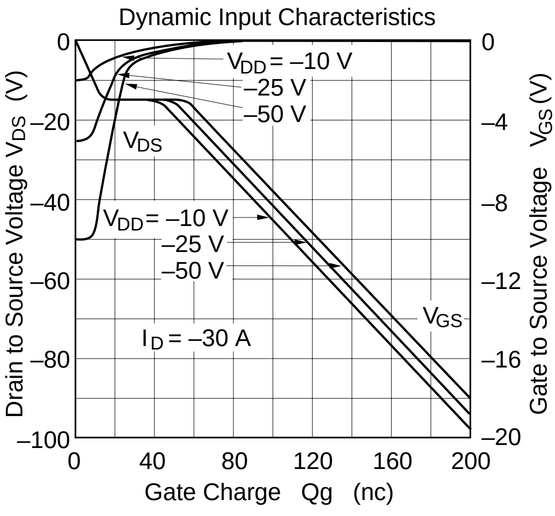


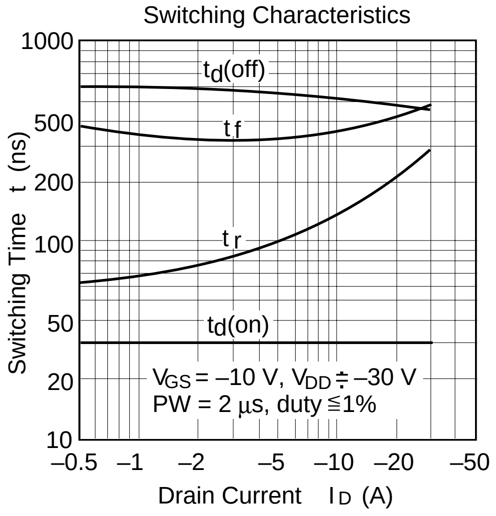
Forward Transfer Admittance vs. Drain Current

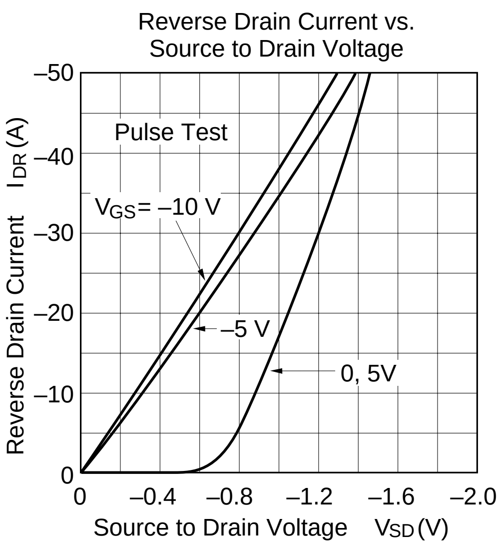


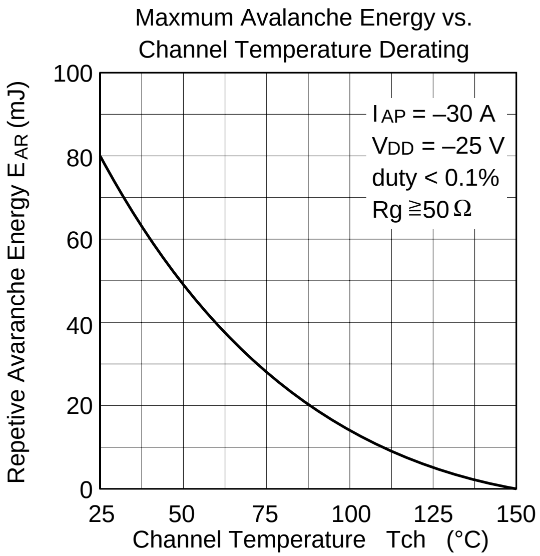

Body-Drain Diode Reverse Recovery Time
500
200
100
50
20
10
5
Reverse Recovery Time trr (ns)
di/dt = 50 A/μs, VGS = 0
Ta = 25°C
–1
–2
–5
–10
–20
–50
–100
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain-Source Voltage
10000
1000
100
10
Capacitance C (pF)
Ciss
Coss
Crss
VGS= 0,
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)

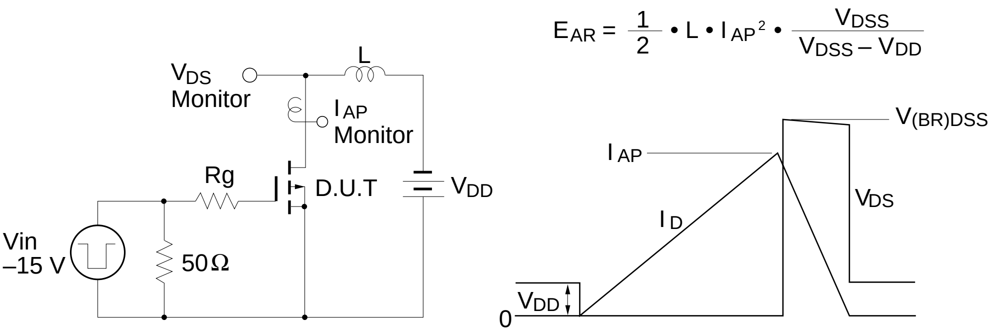

Dynamic Input Characteristics
0
–20
–40
–60
–80
–100
Drain to Source Voltage VDS (V)
VDD = –10 V
–25 V
–50 V
VDS
VDD = –10 V
–25 V
–50 V
VGS
ID = –30 A
0
–4
–8
–12
–16
–20
Gate to Source Voltage VGS (V)
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
1000
500
200
100
50
20
10
Switching Time t (ns)
td(off)
tf
tr
td(on)
VGS = –10 V, VDD ≒ –30 V
PW = 2 μs, duty ≦ 1%
–0.5
–1
–2
–5
–10
–20
–50
Drain Current ID (A)





Avalanche Test Circuit and Waveform

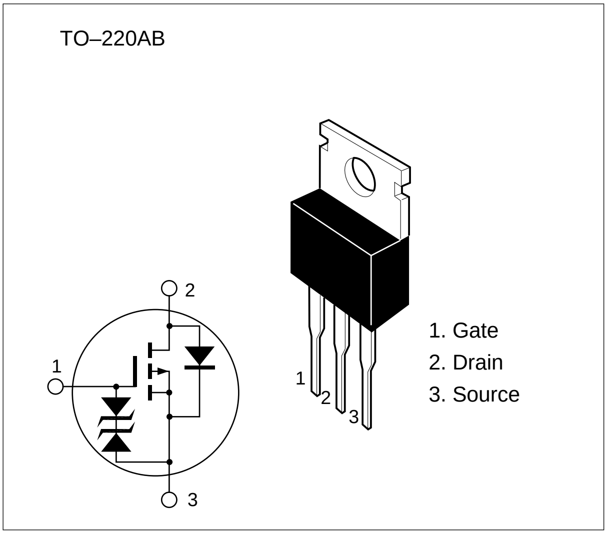


2SJ291

Silicon P Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven form 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

Table 1 Absolute Maximum Ratings (Ta = 25°C)

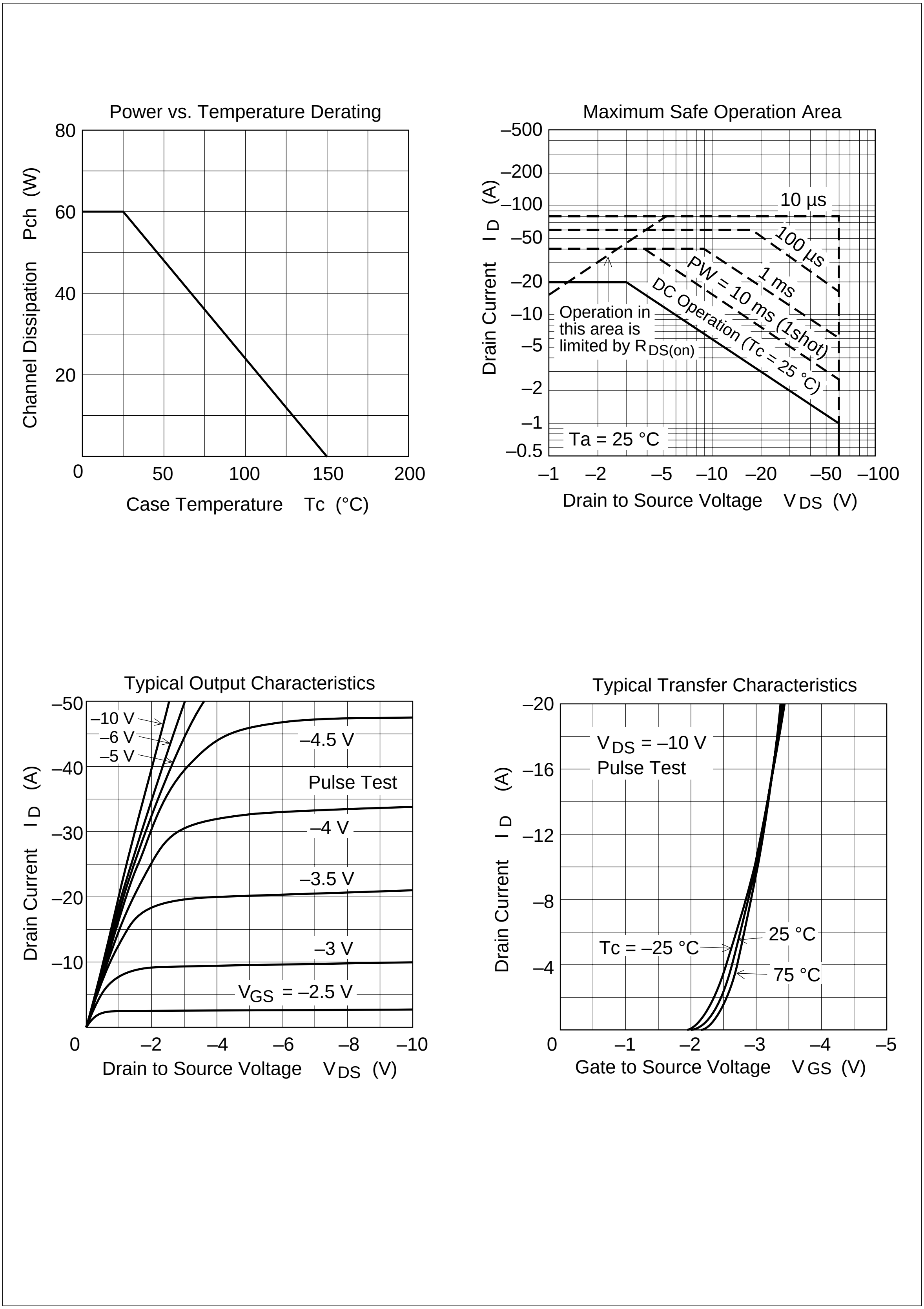
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–20	A
Drain peak current	$I_{D(pulse)}$*	–80	A
Body–drain diode reverse drain current	I_{DR}	–20	A
Avalanche current	I_{AP}***	–20	A
Avalanche energy	E_{AR}***	34	mJ
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

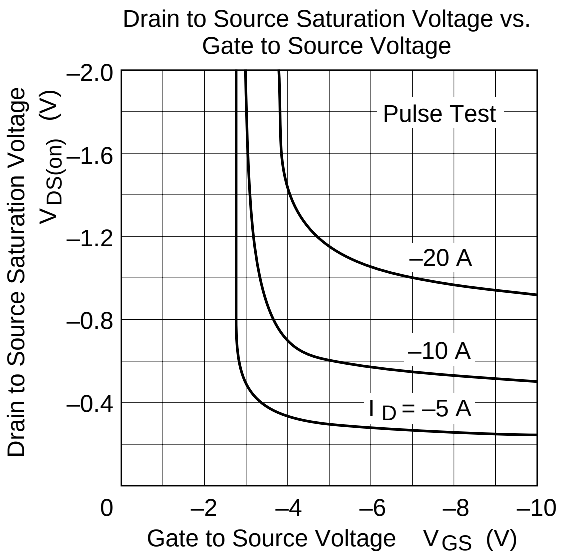
Table 2 Electrical Characteristics (Ta = 25°C)

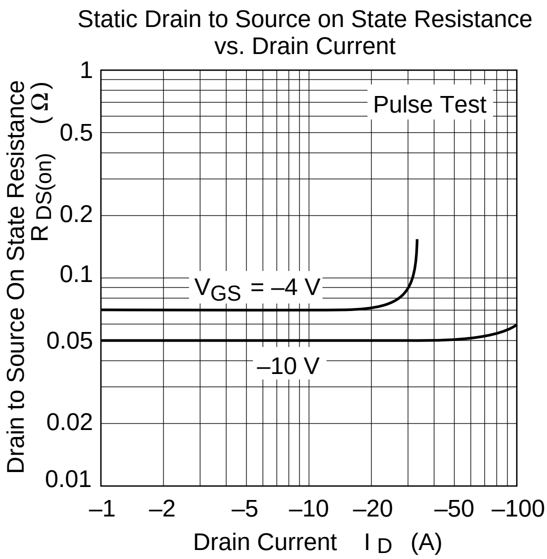
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.065	Ω	I_D = –10 A V_{GS} = –10 V *
		—	0.07	0.095	Ω	I_D = –10 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	16	—	S	I_D = –10 A V_{DS} = –10 V *
Input capacitance	Ciss	—	2200	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	1000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	I_D = –10 A
Rise time	t_r	—	130	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	320	—	ns	R_L = 3 Ω
Fall time	t_f	—	210	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –20 A, V_{GS} = 0, diF / dt = 50 A / µs

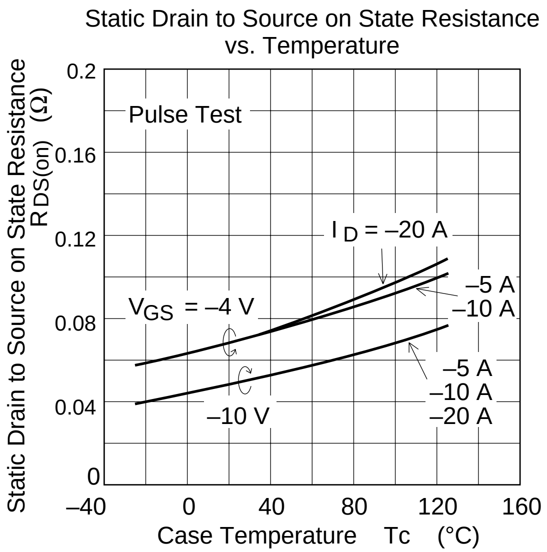
* Pulse Test

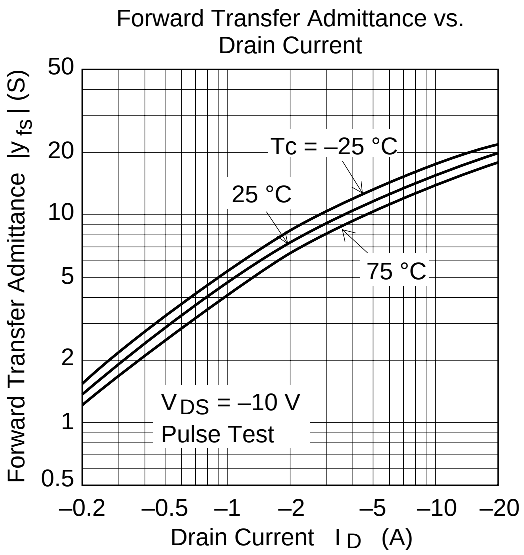


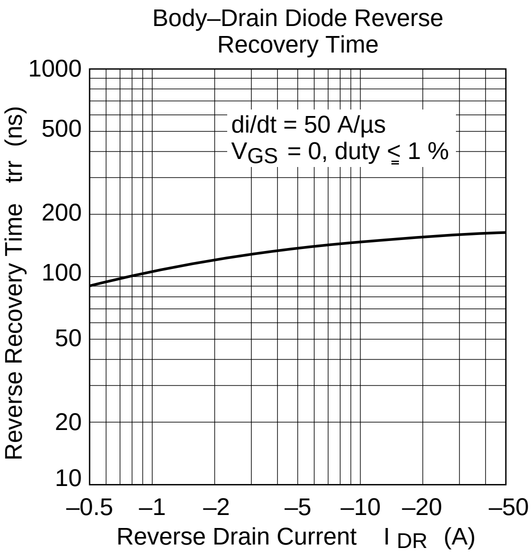
Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)
Maximum Safe Operation Area
Drain Current I D (A)
–500
–200
–100
–50
–20
–10
–5
–2
–1
–0.5
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
–1
–2
–5
–10
–20
–50
–100
Drain to Source Voltage V DS (V)
Typical Output Characteristics
Drain Current I D (A)
–50
–40
–30
–20
–10
–10 V
–6 V
–5 V
–4.5 V
Pulse Test
–4 V
–3.5 V
–3 V
VGS = –2.5 V
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)
Typical Transfer Characteristics
Drain Current I D (A)
–20
–16
–12
–8
–4
V DS = –10 V
Pulse Test
25 °C
Tc = –25 °C
75 °C
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

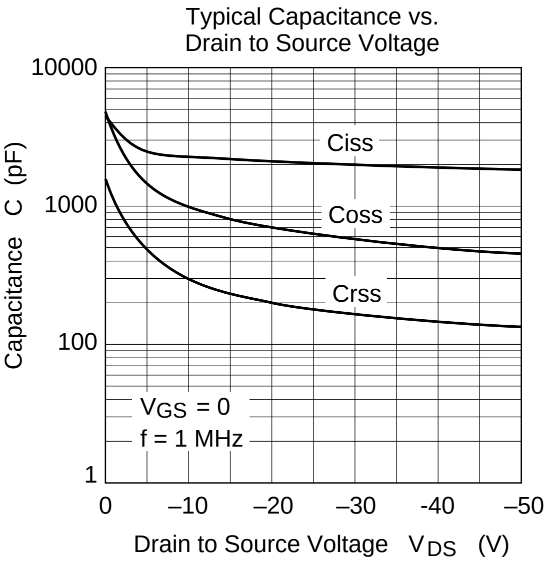

Drain to Source Saturation Voltage vs. Gate to Source Voltage
Pulse Test
–20 A
–10 A
I D = –5 A
Drain to Source Saturation Voltage V DS(on) (V)
–2.0
–1.6
–1.2
–0.8
–0.4
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

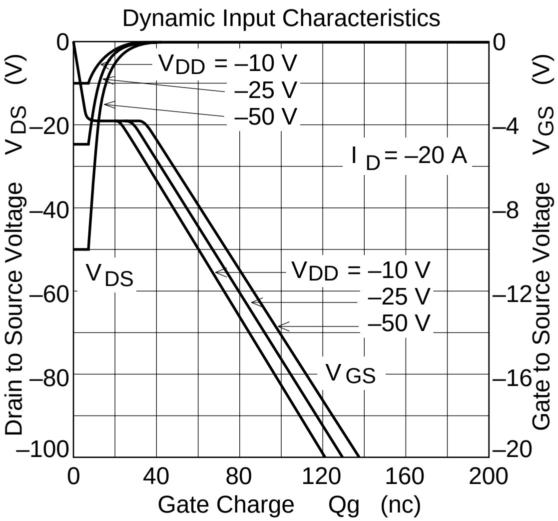

Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
V GS = –4 V
–10 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–1
–2
–5
–10
–20
–50
–100
Drain Current I D (A)

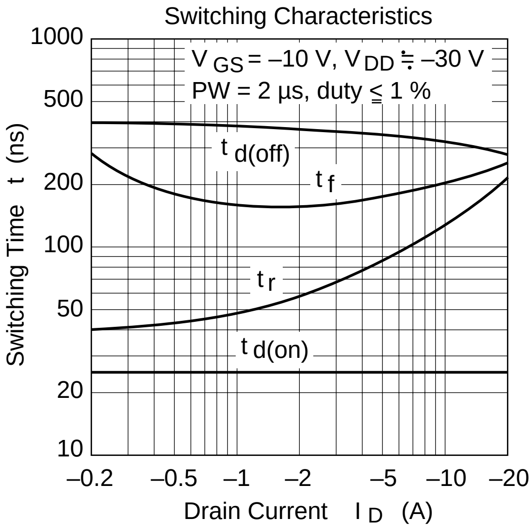

Static Drain to Source on State Resistance vs. Temperature
Pulse Test
I D = –20 A
–5 A
–10 A
V GS = –4 V
–5 A
–10 A
–20 A
–10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.2
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs. Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs| (S)
50
20
10
5
2
1
0.5
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)

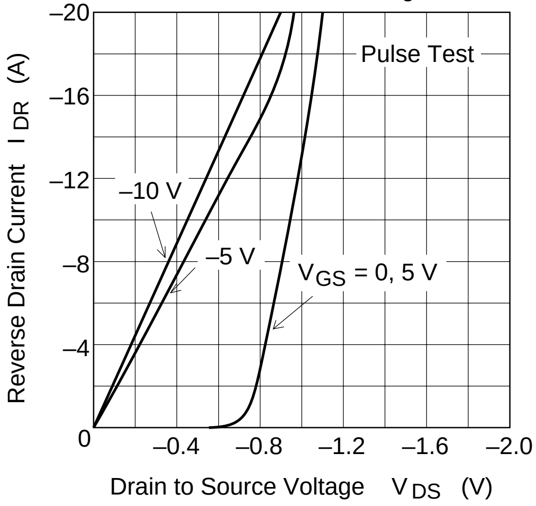

Body–Drain Diode Reverse Recovery Time
di/dt = 50 A/µs
VGS = 0, duty ≦ 1 %
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
–0.5
–1
–2
–5
–10
–20
–50
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
1
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
–10
–20
–30
-40
–50
Drain to Source Voltage VDS (V)

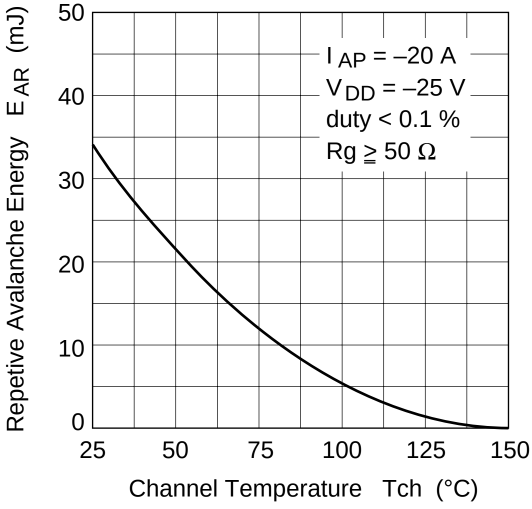

Dynamic Input Characteristics
Drain to Source Voltage V DS (V)
Gate to Source Voltage V GS (V)
VDD = –10 V
–25 V
–50 V
I D = –20 A
VDS
VDD = –10 V
–25 V
–50 V
V GS
0
–20
–40
–60
–80
–100
0
–4
–8
–12
–16
–20
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
V GS = –10 V, V DD ≒ –30 V
PW = 2 µs, duty ≦ 1 %
Switching Time t (ns)
1000
500
200
100
50
20
10
t d(off)
t f
t r
t d(on)
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)

Reverse Drain Current vs.
Source to Drain Voltage

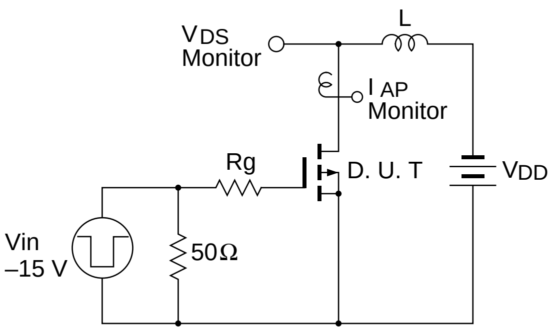


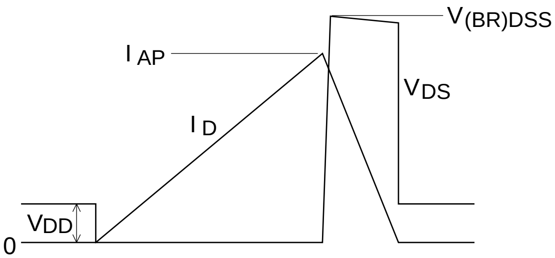
Maximun Avalanche Energy vs.
Channel Temperature Derating

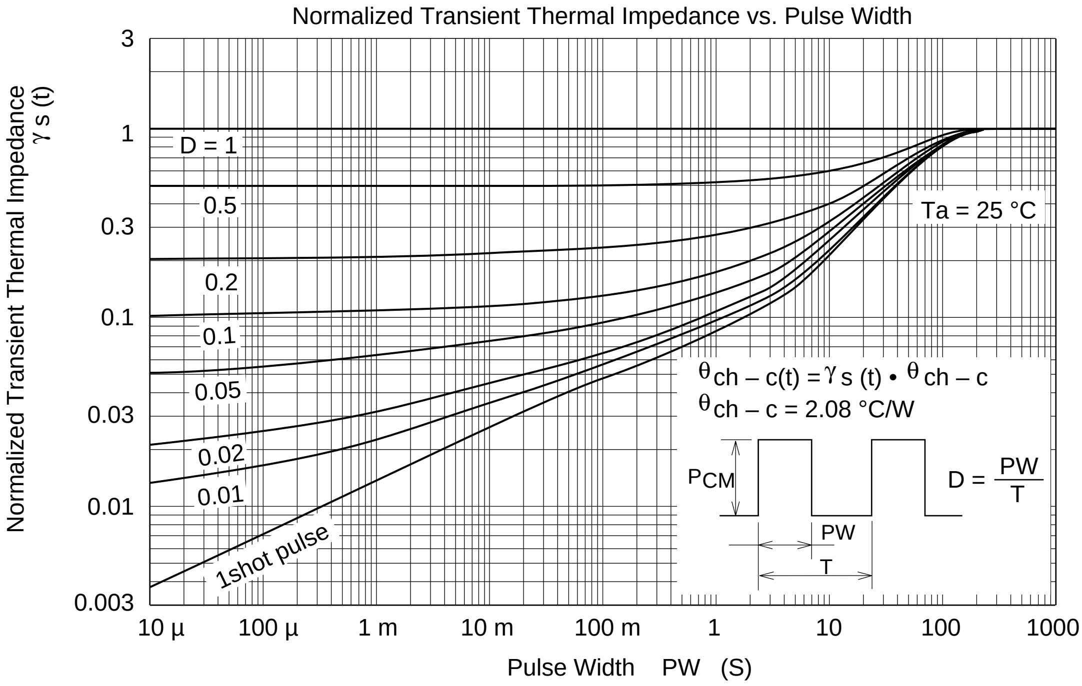


Avalanche Test Circuit and Waveform

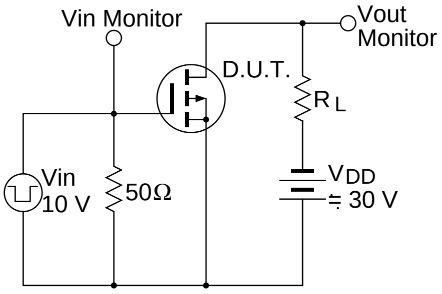
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



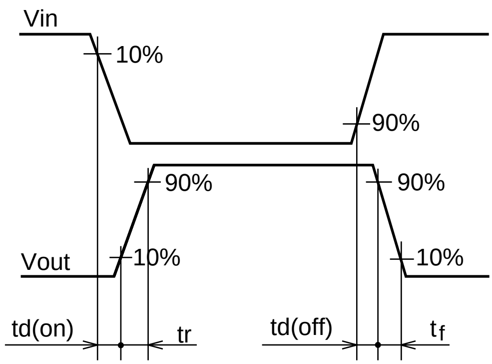




Switching Time Test Circuit



Waveforms



2SJ292

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

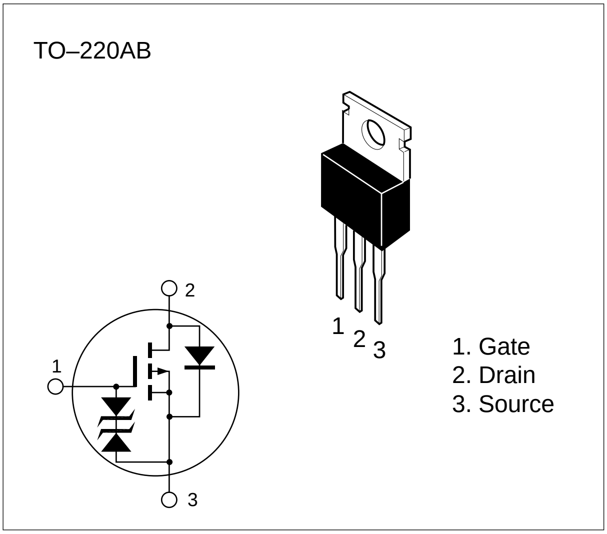


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–30	A
Drain peak current	$I_{D(pulse)}$*	–120	A
Body–drain diode reverse drain current	I_{DR}	–30	A
Avalanche current	I_{AP}***	–30	A
Avalanche energy	E_{AR}***	77	mJ
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.043	Ω	I_D = –15 A V_{GS} = –10 V *
		—	0.045	0.06	Ω	I_D = –15 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	17	25	—	S	I_D = –15 A V_{DS} = –10 V *
Input capacitance	Ciss	—	3300	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	1500	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	480	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = –15 A
Rise time	t_r	—	170	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	500	—	ns	R_L = 2 Ω
Fall time	t_f	—	390	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.5	—	V	I_F = –30 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = –30 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curves of 2SJ280

2SJ293

Silicon P Channel MOS FET

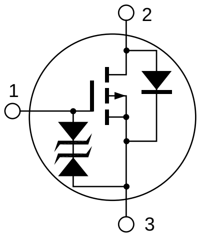
Application

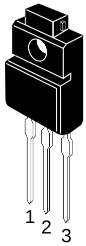
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

TO–220FM





1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–15	A
Drain peak current	$I_{D(pulse)}$*	–60	A
Body–drain diode reverse drain current	I_{DR}	–15	A
Avalanche current	I_{AP}***	–15	A
Avalanche energy	E_{AR}***	19	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

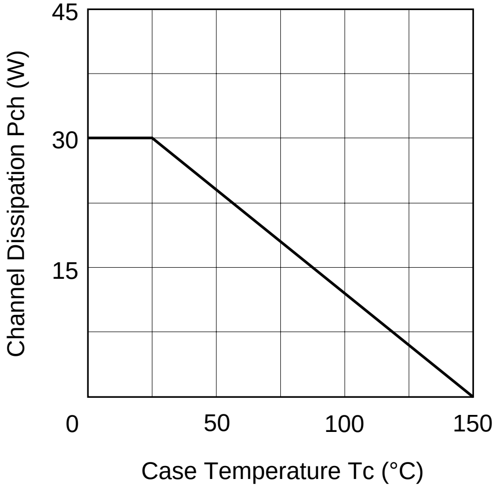
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.095	Ω	I_D = –8 A V_{GS} = –10 V *
		—	0.09	0.12	Ω	I_D = –8 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	8	12	—	S	I_D = –8 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	670	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	240	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = –8 A
Rise time	t_r	—	95	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	230	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	160	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.5	—	V	I_F = –15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –15 A, V_{GS} = 0, diF / dt = 50 A / µs

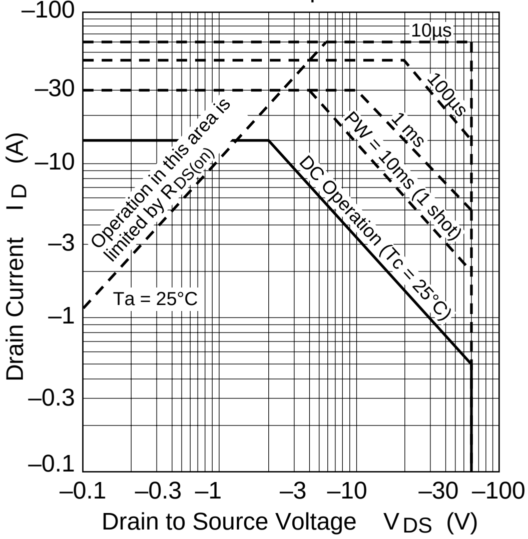
* Pulse Test

See characteristic curves of 2SJ290

Power vs. Temperature Derating



Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width

2SJ296(L), 2SJ296(S)

Silicon P-Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

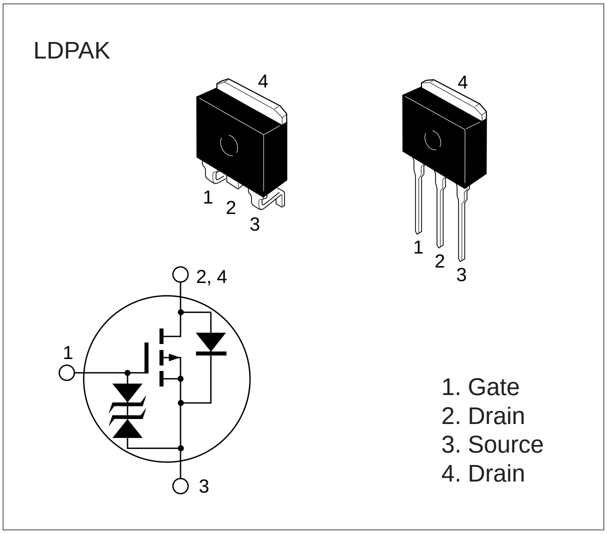


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–15	A
Drain peak current	$I_{D(pulse)}$*	–60	A
Body–drain diode reverse drain current	I_{DR}	–15	A
Avalanche current	I_{AP}***	–15	A
Avalanche energy	E_{AR}***	19	mJ
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.095	Ω	I_D = –8 A V_{GS} = –10 V *
		—	0.09	0.15	Ω	I_D = –8 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	8	12	—	S	I_D = –8 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	670	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	240	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = –8 A
Rise time	t_r	—	95	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	230	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	160	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.5	—	V	I_F = –15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –15 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curves of 2SJ290

2SJ297(L), 2SJ297(S)

Silicon P-Channel MOS FET

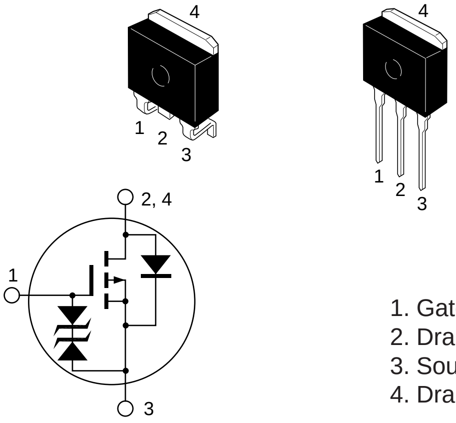
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–20	A
Drain peak current	$I_{D(pulse)}$*	–80	A
Body–drain diode reverse drain current	I_{DR}	–20	A
Avalanche current	I_{AP}***	–20	A
Avalanche energy	E_{AR}***	34	mJ
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.065	Ω	I_D = –10 A V_{GS} = –10 V *
		—	0.07	0.095	Ω	I_D = –10 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	16	—	S	I_D = –10 A V_{DS} = –10 V *
Input capacitance	Ciss	—	2200	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	1000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	I_D = –10 A
Rise time	t_r	—	130	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	320	—	ns	R_L = 3 Ω
Fall time	t_f	—	210	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –20 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See charactristics curves of 2SJ291

2SJ317

Silicon P Channel MOSFET

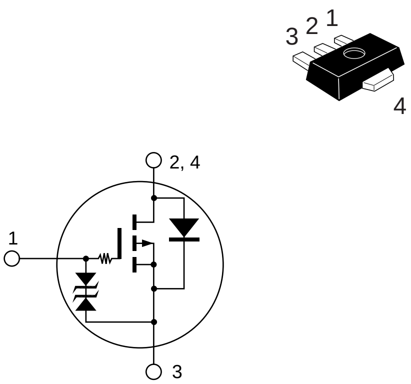
Application

High speed power switching
Low voltage operation

Features

- Very low on–resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

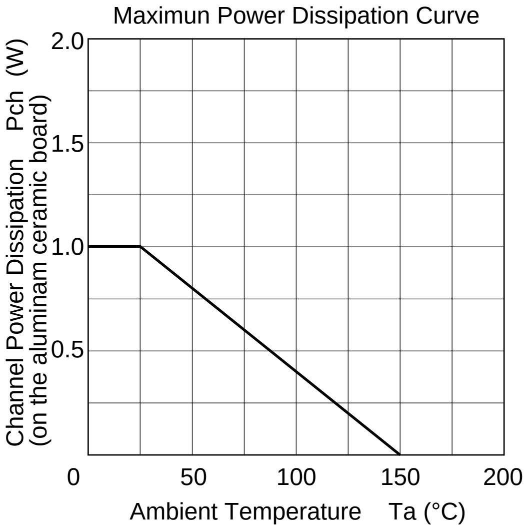
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–12	V
Gate to source voltage	V_{GSS}	±7	V
Drain current	I_D	±2	A
Drain peak current	$I_{D(pulse)}$*	±4	A
Body–drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

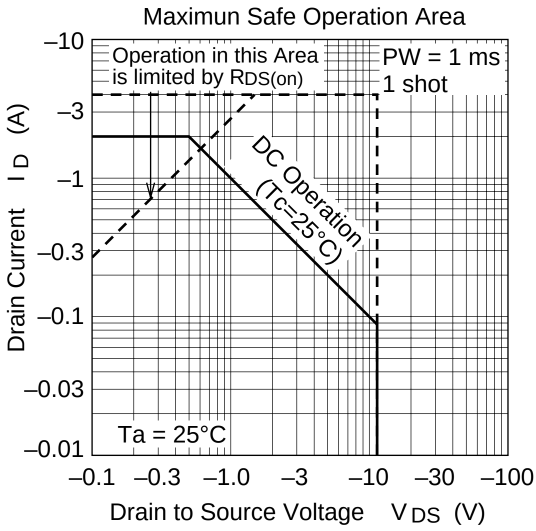
* PW < 100 µs, duty cycle < 10 %
** Value on the alumina ceramic board (12.5 x 20 x 0.7 mm).
*** Marking is "NY".

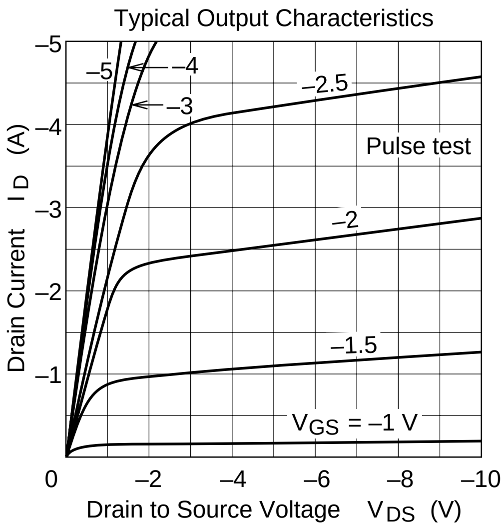
Table 2 Electrical Characteristics (Ta = 25°C)

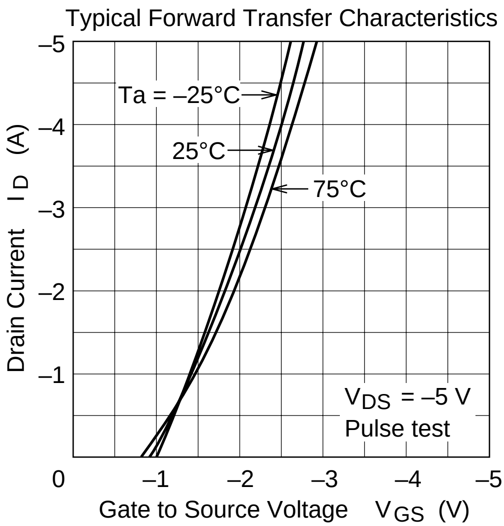
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–12	—	—	V	I_D = –1 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±7	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source cutoff current	I_{GSS}	—	—	±5	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –8 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.4	—	–1.4	V	I_D = –100 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)1}$	—	0.4	0.7	Ω	I_D = –0.5 A*, V_{GS} = –2.2 V
Static drain to source on state resistance	$R_{DS(on)2}$	—	0.28	0.35	Ω	I_D = –1 A*, V_{GS} = –4 V
Forward transfer admittance	$\|y_{fs}\|$	1.0	2.3	—	S	I_D = –1 A*, V_{DS} = –5 V
Input capcitance	Ciss	—	63	—	pF	V_{DS} = –5 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	180	—	pF	
Reverse transfer capacitance	Crss	—	23	—	pF	
Turn–on time	t_{on}	—	500	—	ns	I_D = –0.2 A*, Vin = –4 V, R_L = 51 Ω
Turn–off delay time	t_{off}	—	2860	—	ns	

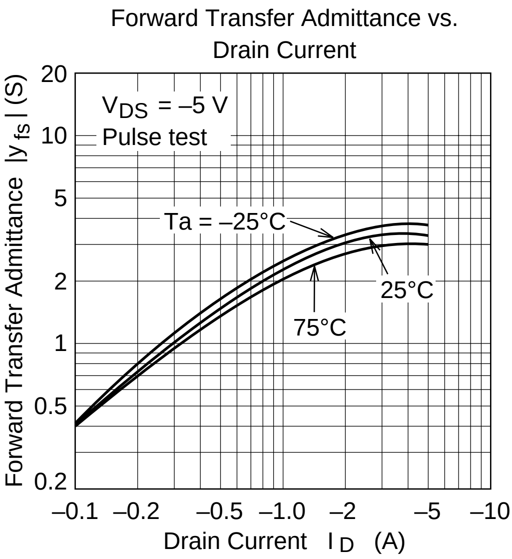
* Pulse test

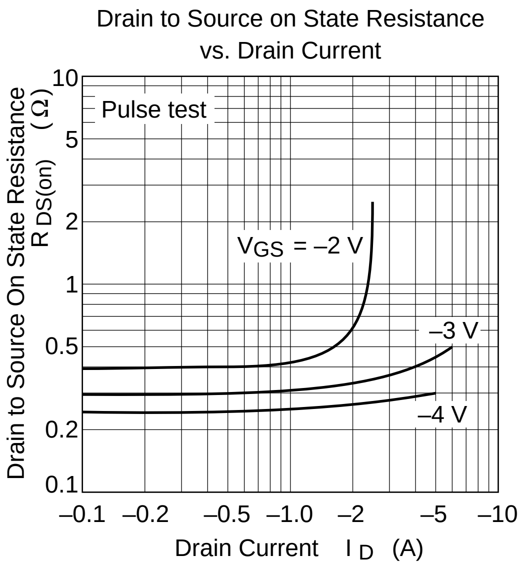

Maximun Power Dissipation Curve
Channel Power Dissipation Pch (W)
(on the aluminam ceramic board)
2.0
1.5
1.0
0.5
0
50
100
150
200
Ambient Temperature Ta (°C)

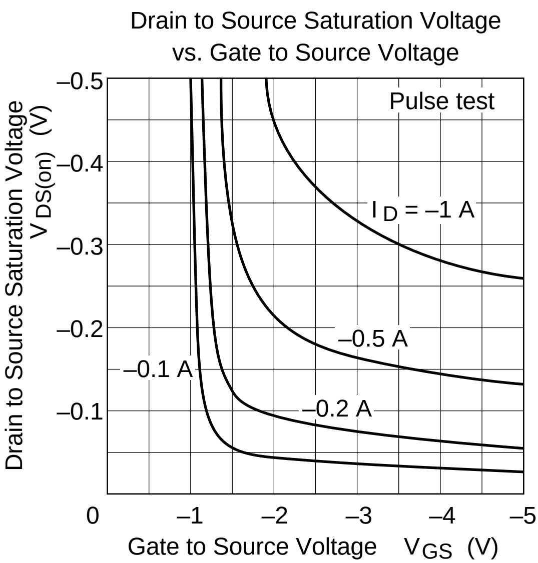

Maximun Safe Operation Area
Operation in this Area
is limited by RDS(on)
PW = 1 ms
1 shot
DC Operation
(Tc=25°C)
Ta = 25°C
Drain Current I D (A)
–10
–3
–1
–0.3
–0.1
–0.03
–0.01
–0.1
–0.3
–1.0
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

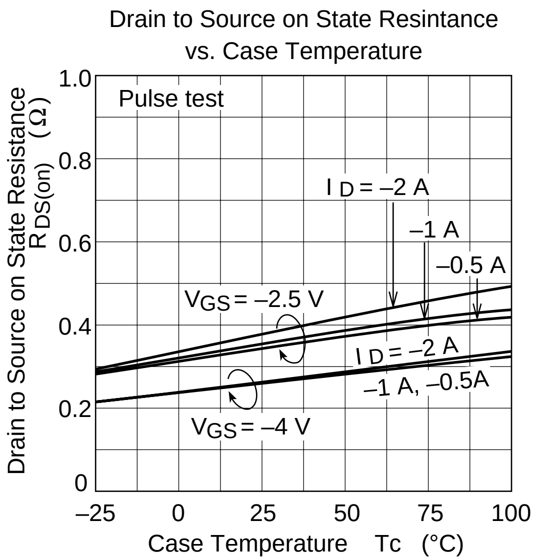

Typical Output Characteristics
–5
–4
–3
–2.5
Pulse test
–2
–1.5
VGS = –1 V
Drain Current I D (A)
–5
–4
–3
–2
–1
0
–2
–4
–6
–8
–10
Drain to Source Voltage VDS (V)

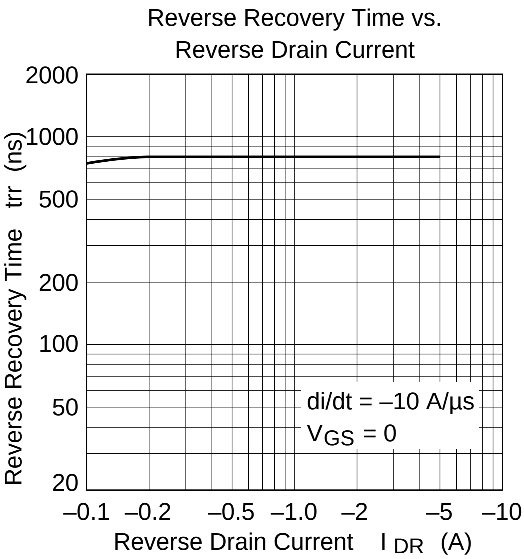

Typical Forward Transfer Characteristics
Ta = –25°C
25°C
75°C
VDS = –5 V
Pulse test
Drain Current I D (A)
–5
–4
–3
–2
–1
0
–1
–2
–3
–4
–5
Gate to Source Voltage VGS (V)

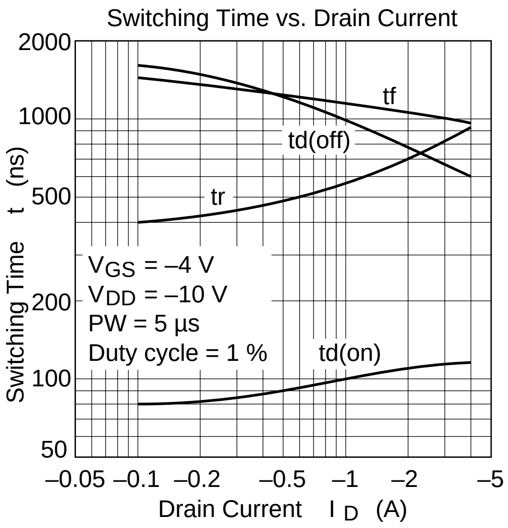

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |y fs | (S)
VDS = –5 V
Pulse test
Ta = –25°C
25°C
75°C
20
10
5
2
1
0.5
0.2
–0.1
–0.2
–0.5
–1.0
–2
–5
–10
Drain Current I D (A)

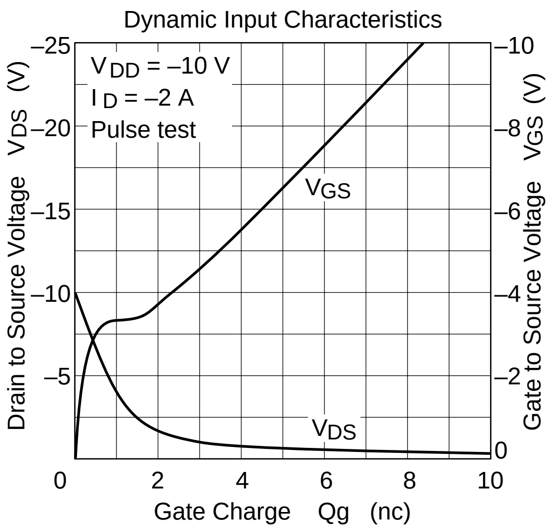

Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
Pulse test
VGS = –2 V
–3 V
–4 V
10
5
2
1
0.5
0.2
0.1
–0.1
–0.2
–0.5
–1.0
–2
–5
–10
Drain Current I D (A)

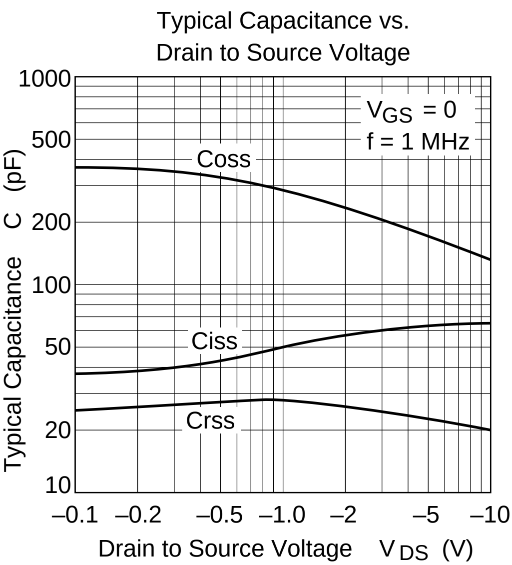

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage V DS(on) (V)
Pulse test
I D = –1 A
–0.5 A
–0.1 A
–0.2 A
–0.5
–0.4
–0.3
–0.2
–0.1
0
–1
–2
–3
–4
–5
Gate to Source Voltage VGS (V)

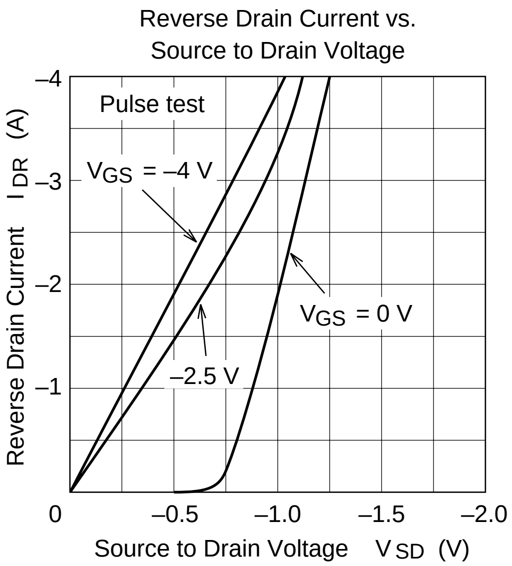

Drain to Source on State Resintance
vs. Case Temperature
Drain to Source on State Resistance R DS(on) (Ω)
Pulse test
I D = –2 A
–1 A
–0.5 A
VGS = –2.5 V
I D = –2 A
–1 A, –0.5A
VGS = –4 V
1.0
0.8
0.6
0.4
0.2
0
–25
0
25
50
75
100
Case Temperature Tc (°C)


Reverse Recovery Time vs.
Reverse Drain Current
Reverse Recovery Time trr (ns)
2000
1000
500
200
100
50
20
di/dt = –10 A/µs
V GS = 0
–0.1 –0.2 –0.5 –1.0 –2 –5 –10
Reverse Drain Current I DR (A)


Switching Time vs. Drain Current
Switching Time t (ns)
2000
1000
500
200
100
50
tf
td(off)
tr
V GS = –4 V
V DD = –10 V
PW = 5 µs
Duty cycle = 1 %
td(on)
–0.05 –0.1 –0.2 –0.5 –1 –2 –5
Drain Current I D (A)


Dynamic Input Characteristics
Drain to Source Voltage V DS (V)
Gate to Source Voltage V GS (V)
–25
–20
–15
–10
–5
–10
–8
–6
–4
–2
0
V DD = –10 V
I D = –2 A
Pulse test
V GS
V DS
0 2 4 6 8 10
Gate Charge Qg (nc)


Typical Capacitance vs.
Drain to Source Voltage
Typical Capacitance C (pF)
1000
500
200
100
50
20
10
V GS = 0
f = 1 MHz
Coss
Ciss
Crss
–0.1 –0.2 –0.5 –1.0 –2 –5 –10
Drain to Source Voltage V DS (V)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse test
VGS = –4 V
–2.5 V
VGS = 0 V
Reverse Drain Current I DR (A)
–4
–3
–2
–1
0
–0.5
–1.0
–1.5
–2.0
Source to Drain Voltage V SD (V)

2SJ318(L), 2SJ318(S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

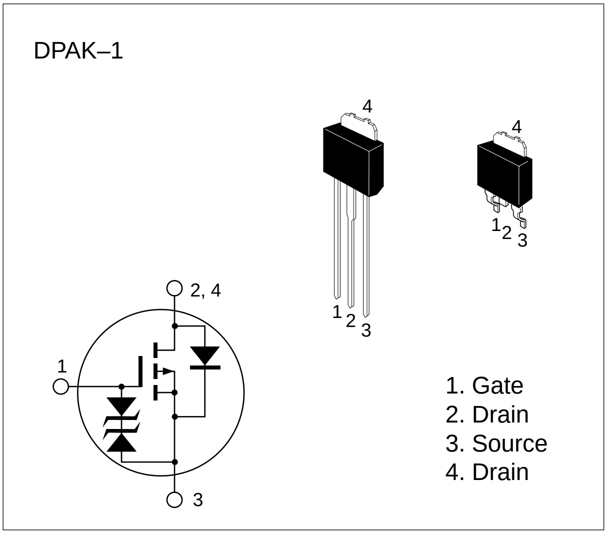


Table 1 Absolute Maximum Ratings (Ta = 25°C)

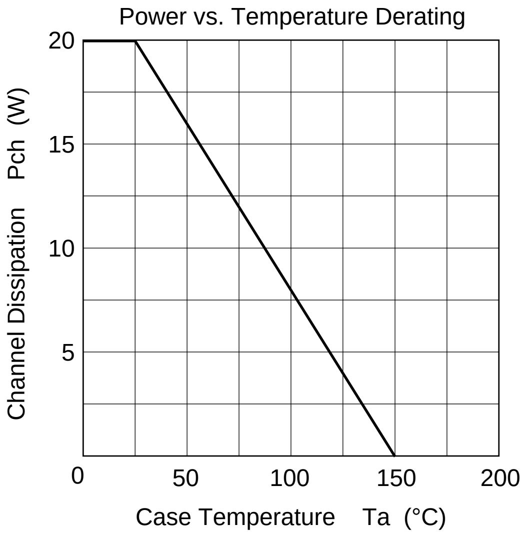
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–5	A
Drain peak current	$I_{D(pulse)}$*	–20	A
Body–drain diode reverse drain current	I_{DR}	–5	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

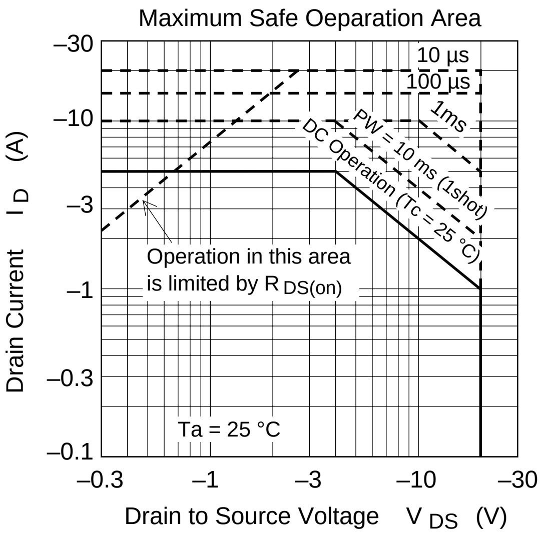
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C

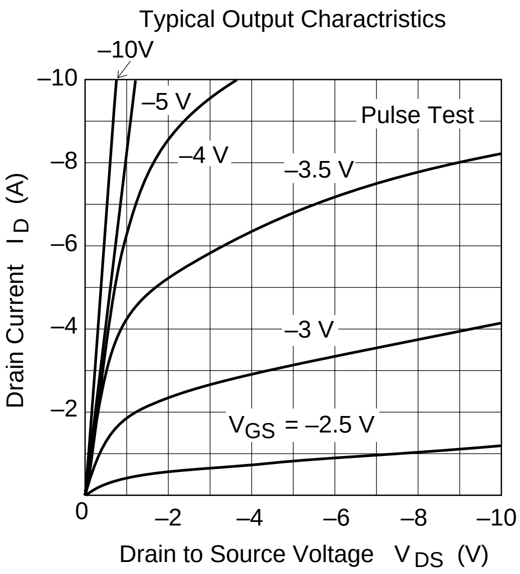
Table 2 Electrical Characteristics (Ta = 25°C)

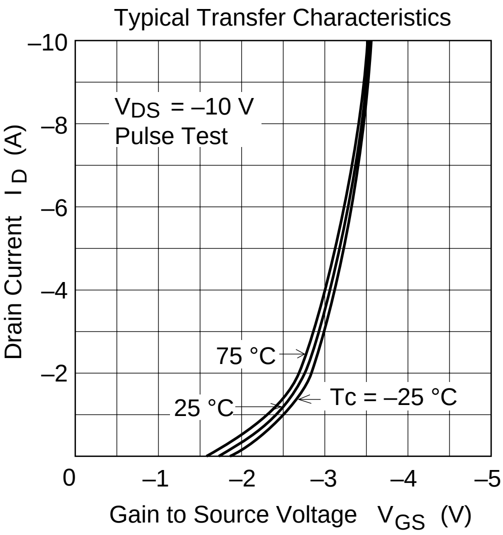
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.09	0.13	Ω	I_D = –3 A V_{GS} = –10 V *
		—	0.14	0.19	Ω	I_D = –3 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	5.5	—	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance	Ciss	—	580	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	520	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	215	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = –3 A
Rise time	t_r	—	60	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	75	—	ns	R_L = 3.3 Ω
Fall time	t_f	—	75	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	65	—	µs	I_F = –5 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

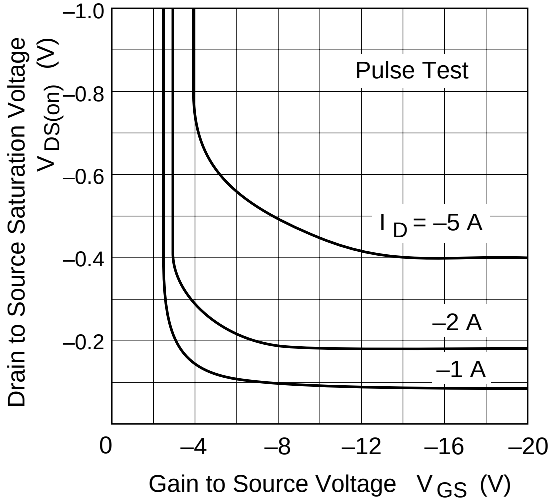

Power vs. Temperature Derating
Channel Dissipation Pch (W)
20
15
10
5
0
50
100
150
200
Case Temperature Ta (°C)


Maximum Safe Oeparation Area
Drain Current I D (A)
–30
–10
–3
–1
–0.3
–0.1
10 µs
100 µs
1ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area
is limited by R DS(on)
Ta = 25 °C
–0.3
–1
–3
–10
–30
Drain to Source Voltage V DS (V)

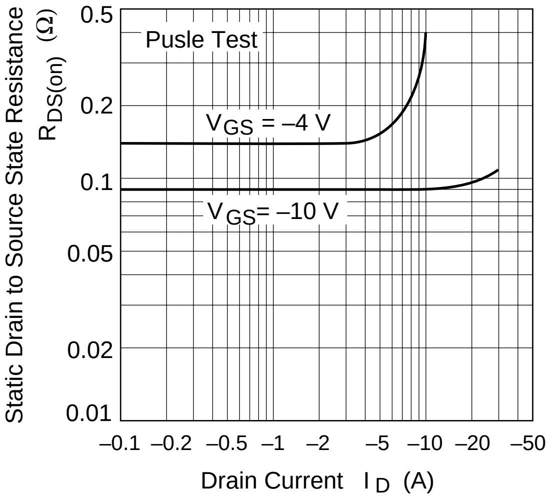

Typical Output Charactristics
–10V
–5 V
–4 V
–3.5 V
Pulse Test
–3 V
VGS = –2.5 V
Drain Current I D (A)
–10
–8
–6
–4
–2
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
VDS = –10 V
Pulse Test
75 °C
25 °C
Tc = –25 °C
Drain Current I D (A)
–10
–8
–6
–4
–2
0
–1
–2
–3
–4
–5
Gain to Source Voltage VGS (V)

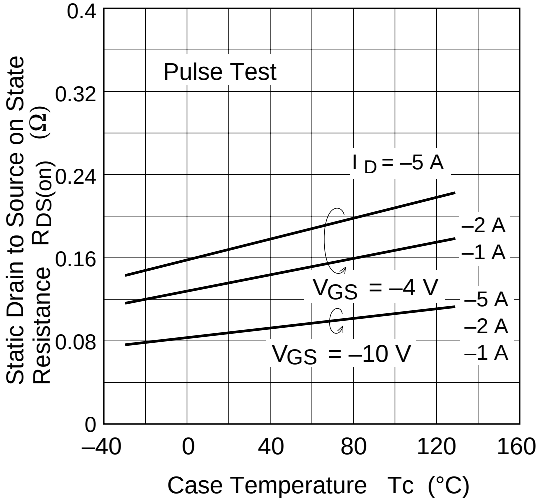
Drain to Source Saturation Voltage vs. Gate to Source Voltage



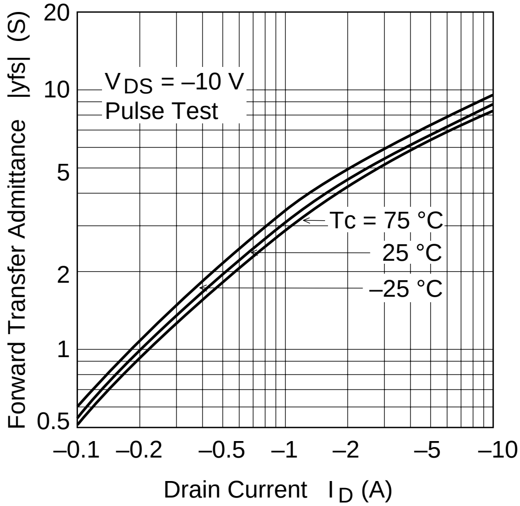
Static Drain to Source on State Resistance vs. Drain Current



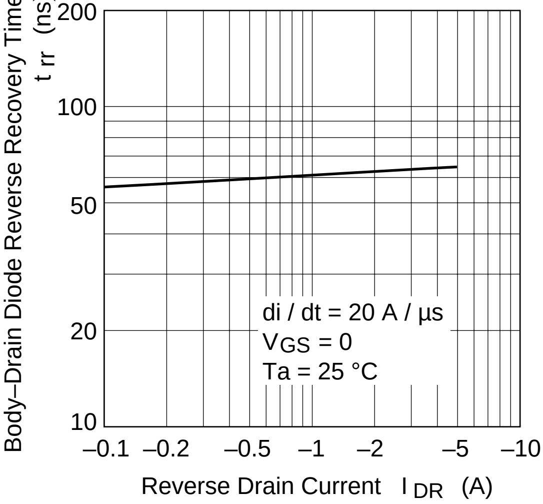
Static Drain to Source on State Resistance vs. Temperature



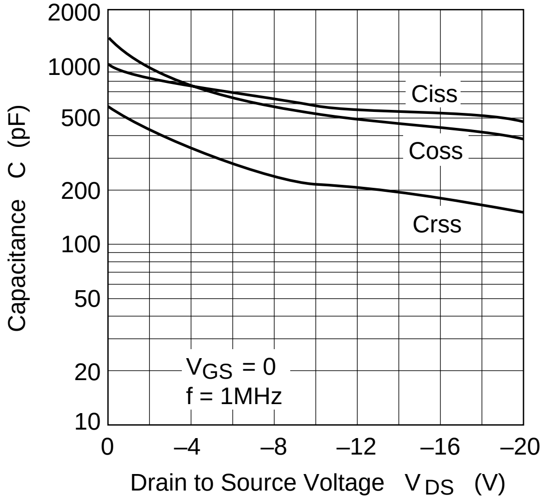
Foeward Transfer Admittance vs. Drain Current



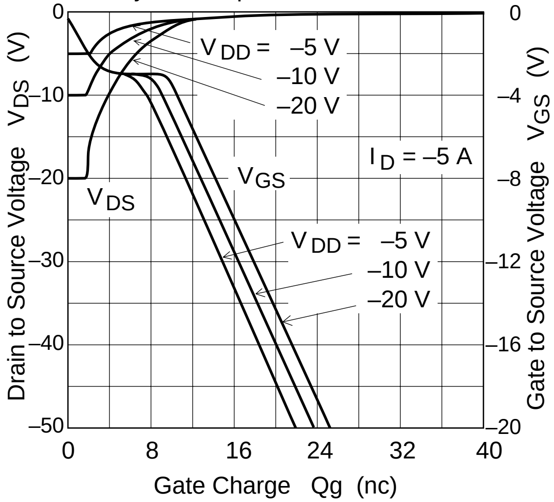
Body–Drain Diode Reverse Recovery Time



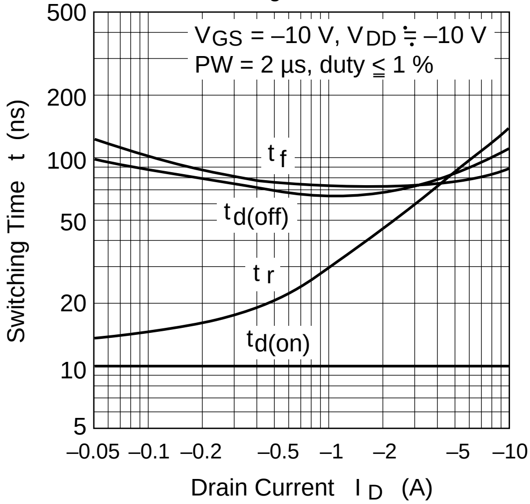
Typical Capacitance vs. Drain to Source Voltage

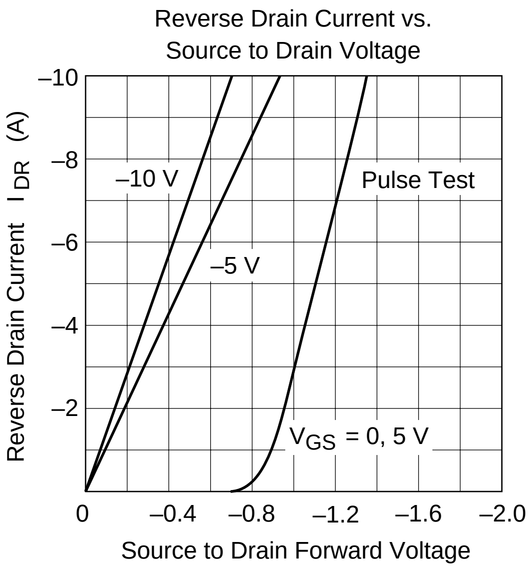


Dynamic Input Characteristics

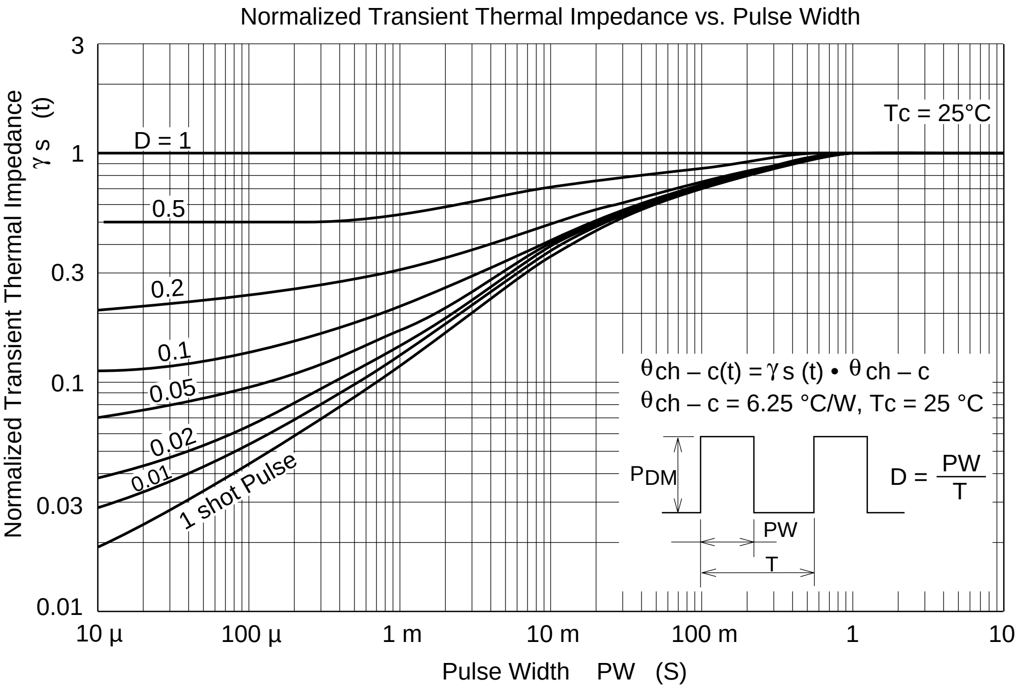


Switching Characteristics

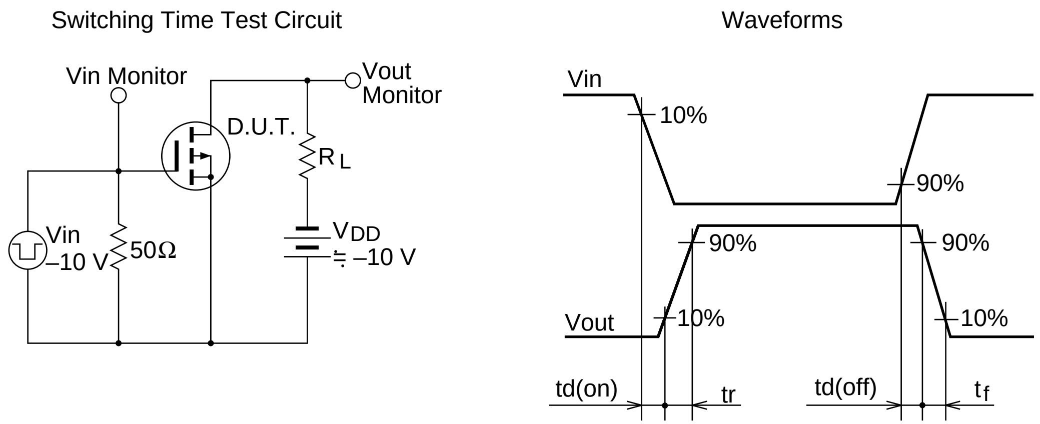




Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
–10
–8
–6
–4
–2
0
–0.4
–0.8
–1.2
–1.6
–2.0
–10 V
–5 V
Pulse Test
VGS = 0, 5 V
Source to Drain Forward Voltage



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
D = PW/T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)


Switching Time Test Circuit
Vin Monitor
Vout
Monitor
D.U.T.
R L
Vin
–10 V
50Ω
VDD
≒ –10 V
Waveforms
Vin
10%
90%
90%
90%
Vout
10%
10%
td(on)
tr
td(off)
tf

2SJ319(L), 2SJ319(S)

Silicon P Channel MOS FET

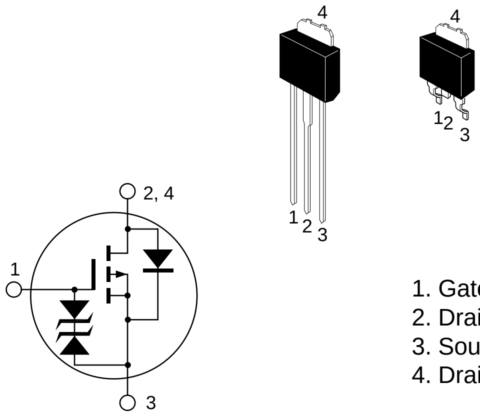
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for Switching regulator, DC – DC converter

DPAK–1



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

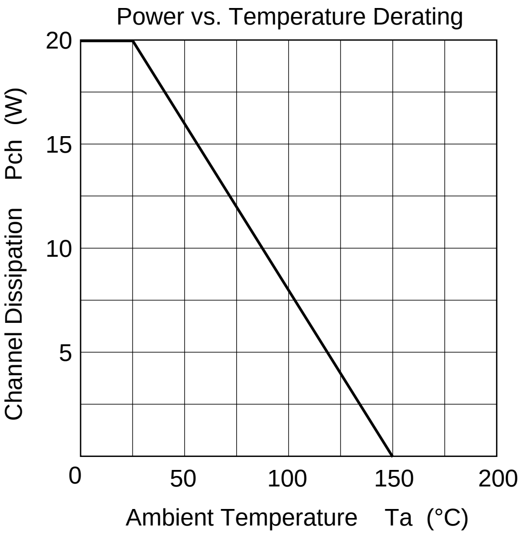
Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	–200	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–3	A
Drain peak current	$I_{D(pulse)}$*	–12	A
Body–drain diode reverse drain current	I_{DR}	–3	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

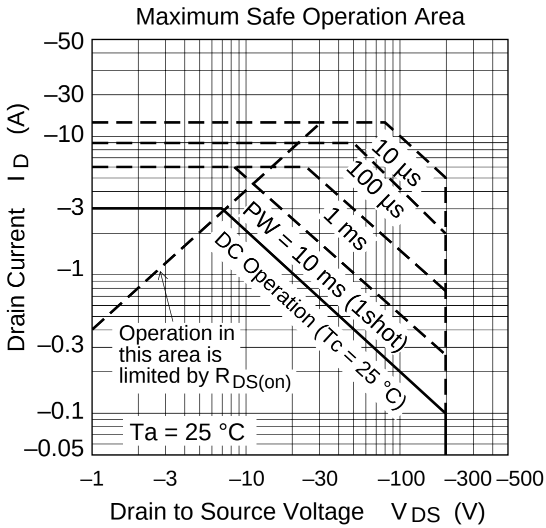
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

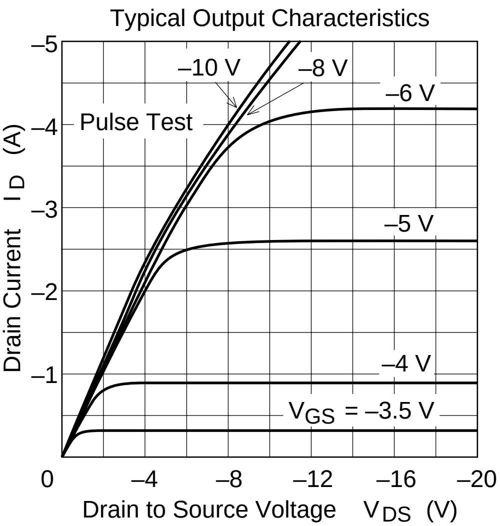
Table 2 Electrical Characteristics (Ta = 25°C)

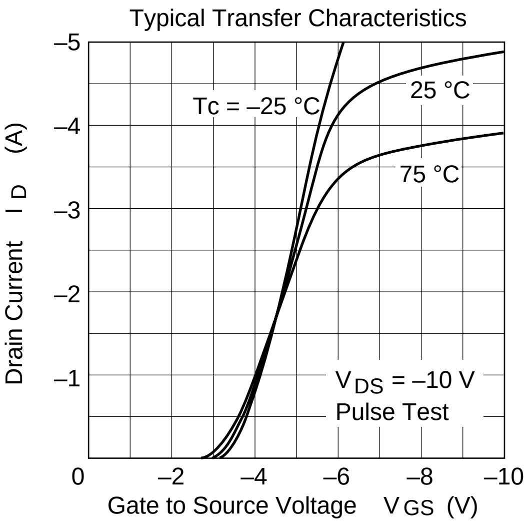
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–200	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–2.0	—	–4.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.7	2.3	Ω	I_D = –2 A V_{GS} = –10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.0	1.7	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	330	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	130	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	25	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = –2 A
Rise time	t_r	—	30	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	40	—	ns	R_L = 10 Ω
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.15	—	V	I_F = –3 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	180	—	µs	I_F = –3 A, V_{GS} = 0, diF / dt = 50 A / µs

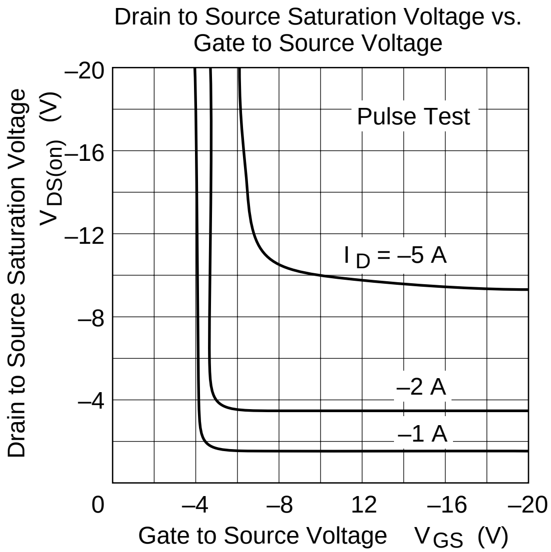
* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
20
15
10
5
0
50
100
150
200
Ambient Temperature Ta (°C)

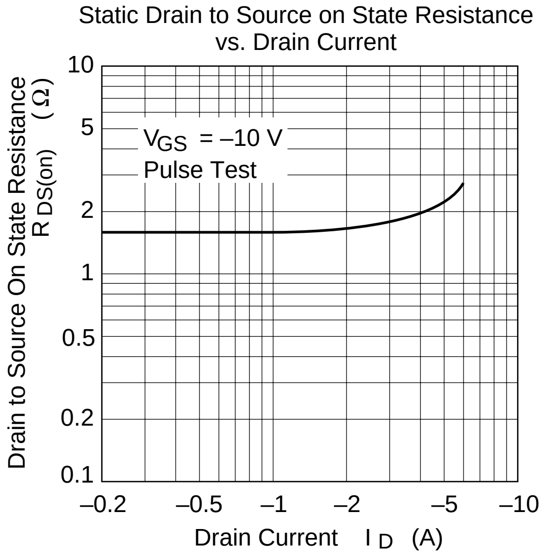

Maximum Safe Operation Area
Drain Current I D (A)
–50
–30
–10
–3
–1
–0.3
–0.1
–0.05
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
–1
–3
–10
–30
–100
–300
–500
Drain to Source Voltage V DS (V)


Typical Output Characteristics
Drain Current I D (A)
–5
–4
–3
–2
–1
0
–10 V
–8 V
–6 V
Pulse Test
–5 V
–4 V
V GS = –3.5 V
–4
–8
–12
–16
–20
Drain to Source Voltage V DS (V)

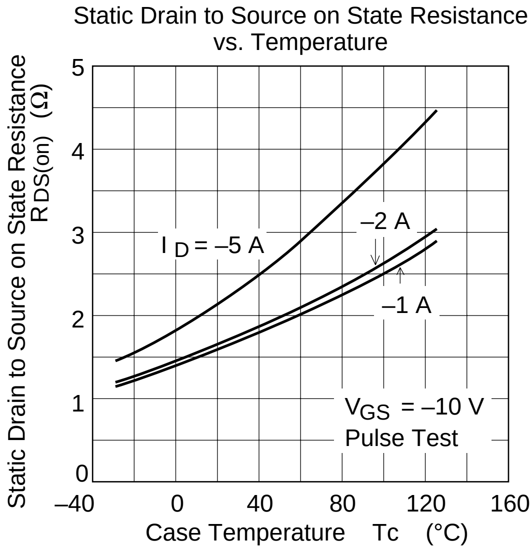

Typical Transfer Characteristics
Drain Current I D (A)
–5
–4
–3
–2
–1
0
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)



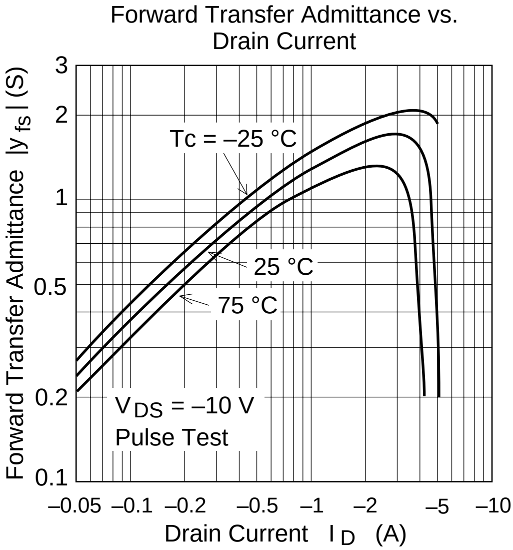
Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage V DS(on) (V)
–20
–16
–12
–8
–4
0
–4
–8
12
–16
–20
Gate to Source Voltage V GS (V)
Pulse Test
I D = –5 A
–2 A
–1 A



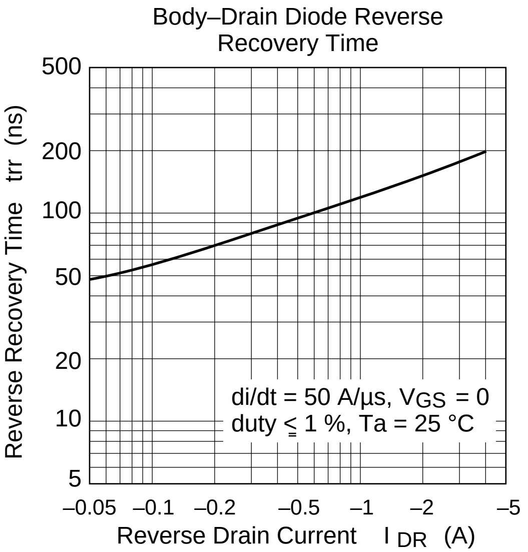
Static Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
10
5
2
1
0.5
0.2
0.1
V GS = –10 V
Pulse Test
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

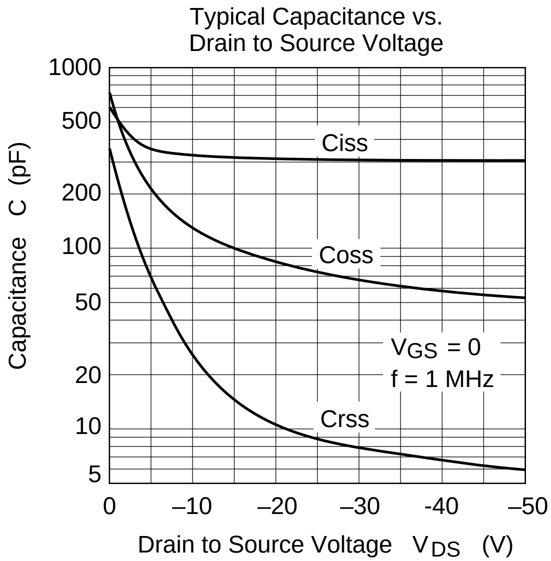


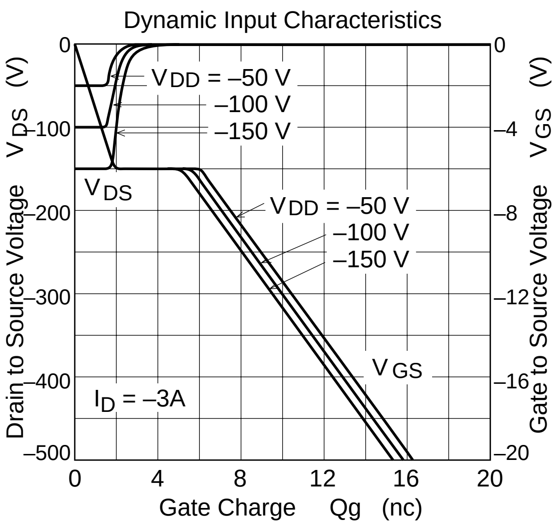
Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance R DS(on) (Ω)
5
4
3
2
1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)
I D = –5 A
–2 A
–1 A
V GS = –10 V
Pulse Test

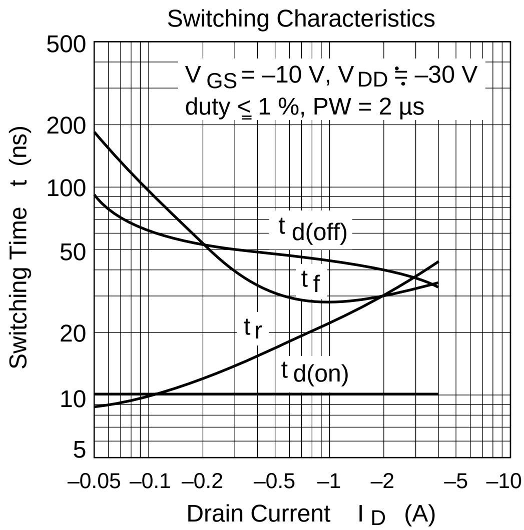


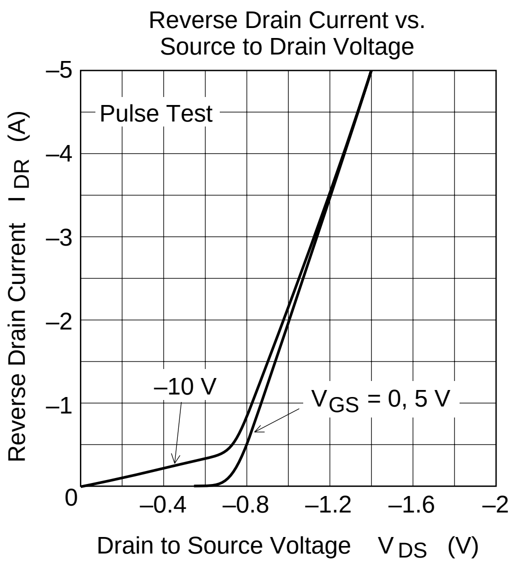
Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |y fs| (S)
3
2
1
0.5
0.2
0.1
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
–0.05
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
di/dt = 50 A/µs, VGS = 0
duty ≦ 1 %, Ta = 25 °C
–0.05 –0.1 –0.2 –0.5 –1 –2 –5
Reverse Drain Current I DR (A)

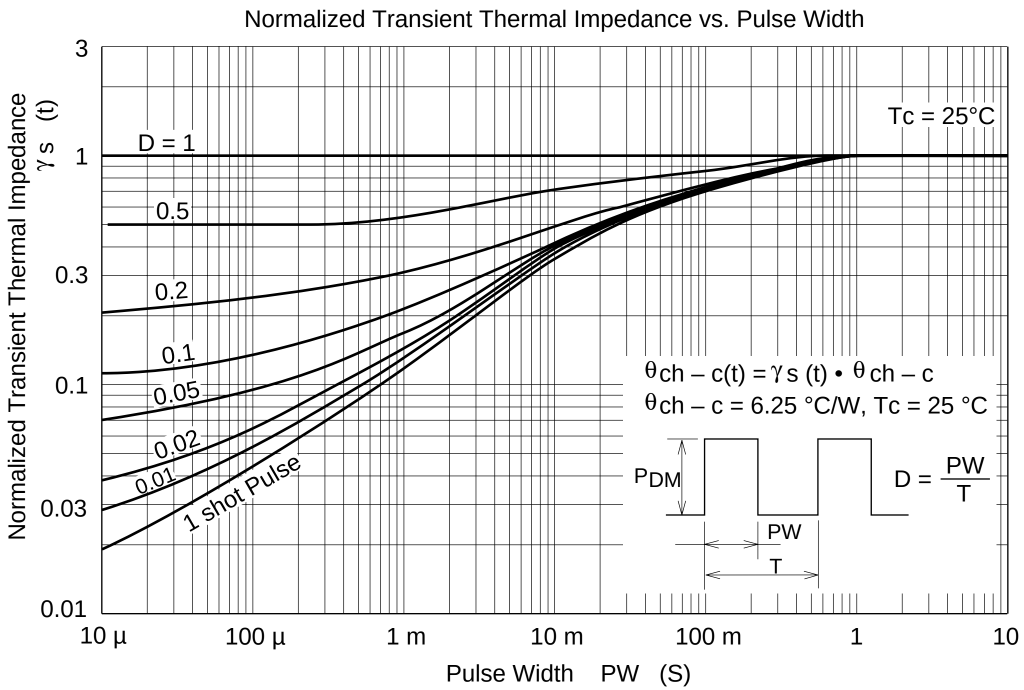

Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
1000
500
200
100
50
20
10
5
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 -40 –50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–100
–200
–300
–400
–500
VDD = –50 V
–100 V
–150 V
VDS
VDD = –50 V
–100 V
–150 V
VGS
ID = –3A
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
0 4 8 12 16 20
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
V GS = –10 V, V DD ≒ –30 V
duty ≦ 1 %, PW = 2 µs
t d(off)
t f
t r
t d(on)
–0.05 –0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)

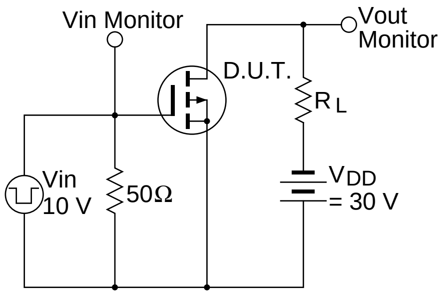


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
–10 V
V_GS = 0, 5 V
Reverse Drain Current I_DR (A)
Drain to Source Voltage V_DS (V)
0
–1
–2
–3
–4
–5
–0.4
–0.8
–1.2
–1.6
–2

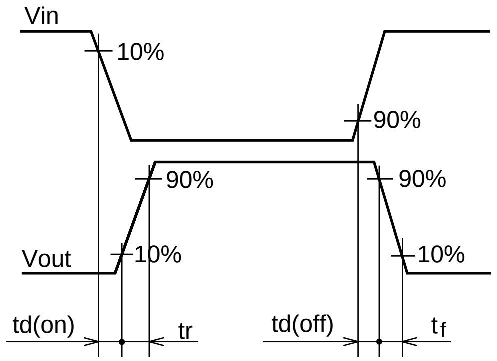


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
P_DM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Waveforms



2SJ321

Silicon P Channel MOS FET

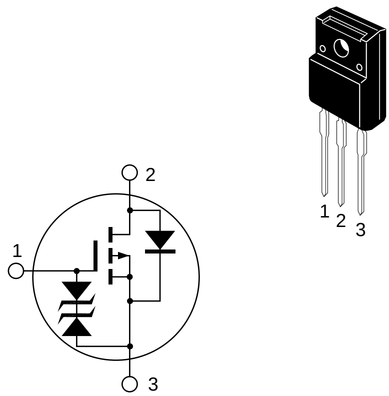
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1   Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–15	A
Drain peak current	$I_{D(pulse)}$*	–60	A
Body–drain diode reverse drain current	I_{DR}	–15	A
Avalanche current	I_{AP}***	–15	A
Avalanche energy	E_{AR}***	19	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

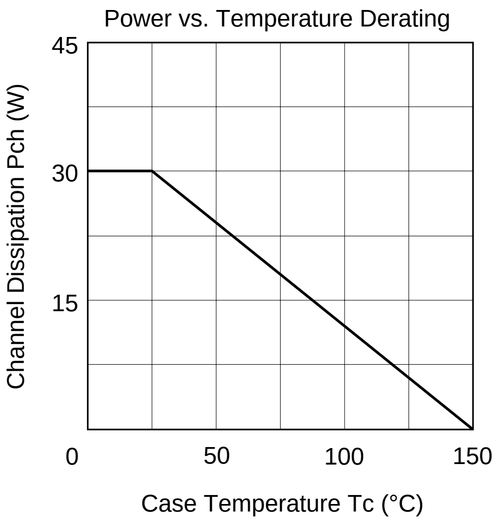
*   PW ≤ 10 µs, duty cycle ≤ 1 %
**   Value at Tc = 25 °C
***   Value at Tch = 25 °C, Rg ≥ 50 Ω

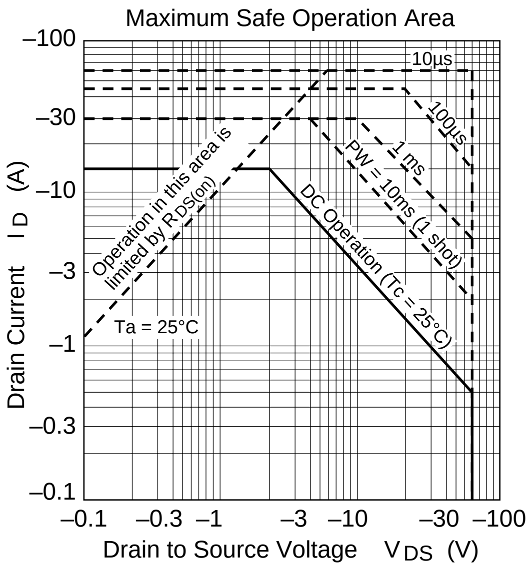
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.095	Ω	I_D = –8 A V_{GS} = –10 V *
		—	0.09	0.12	Ω	I_D = –8 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	8	12	—	S	I_D = –8 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	670	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	240	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = –8 A
Rise time	t_r	—	95	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	230	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	160	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.5	—	V	I_F = –15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –15 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curve of 2SJ290


Power vs. Temperature Derating
45
30
15
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
–100
–30
–10
–3
–1
–0.3
–0.1
10µs
100µs
1 ms
PW = 10ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by RDS(on)
Ta = 25°C
Drain Current I D (A)
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

2SJ322

Silicon P Channel MOS FET

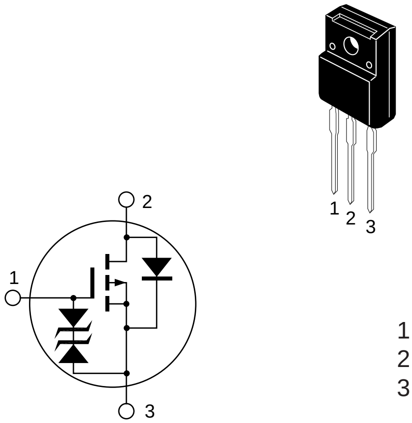
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–20	A
Drain peak current	$I_{D(pulse)}$*	–80	A
Body–drain diode reverse drain current	I_{DR}	–20	A
Avalanche current	I_{AP}***	–20	A
Avalanche energy	E_{AR}***	34	mJ
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

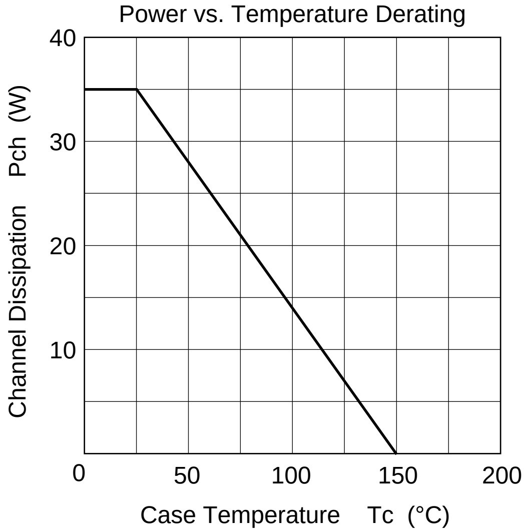
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

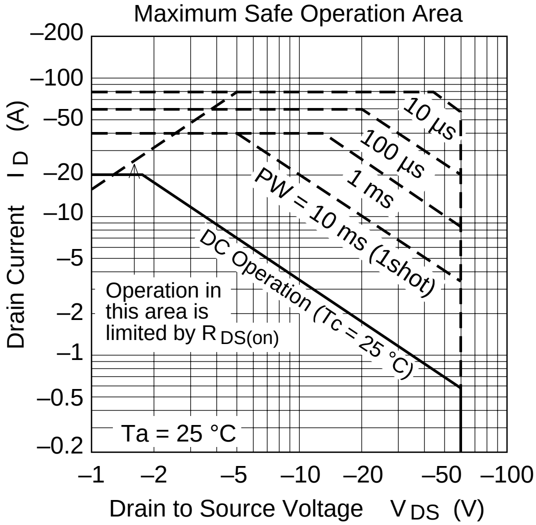
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.065	Ω	I_D = –10 A V_{GS} = –10 V *
		—	0.07	0.095	Ω	I_D = –10 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	16	—	S	I_D = –10 A V_{DS} = –10 V *
Input capacitance	Ciss	—	2200	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	1000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	I_D = –10 A
Rise time	t_r	—	130	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	320	—	ns	R_L = 3 Ω
Fall time	t_f	—	210	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –20 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

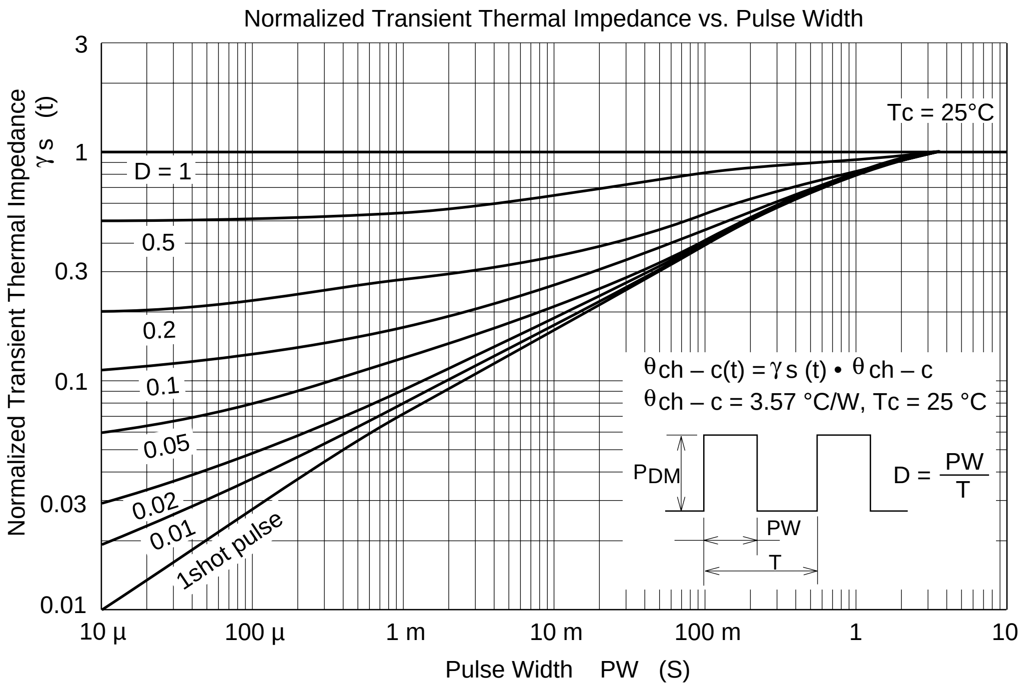
See characteristic curve of 2SJ291.



Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)



Maximum Safe Operation Area
Drain Current I D (A)
–200
–100
–50
–20
–10
–5
–2
–1
–0.5
–0.2
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
–1
–2
–5
–10
–20
–50
–100
Drain to Source Voltage V DS (V)



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 3.57 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

2SJ323

Silicon P Channel MOS FET

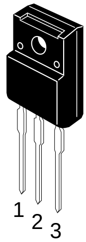
Application

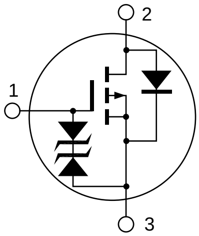
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

TO–220CFM





1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–30	A
Drain peak current	$I_{D(pulse)}{}^{*}$	–120	A
Body–drain diode reverse drain current	I_{DR}	–30	A
Avalanche current	$I_{AP}{}^{***}$	–30	A
Avalanche energy	$E_{AR}{}^{***}$	77	mJ
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

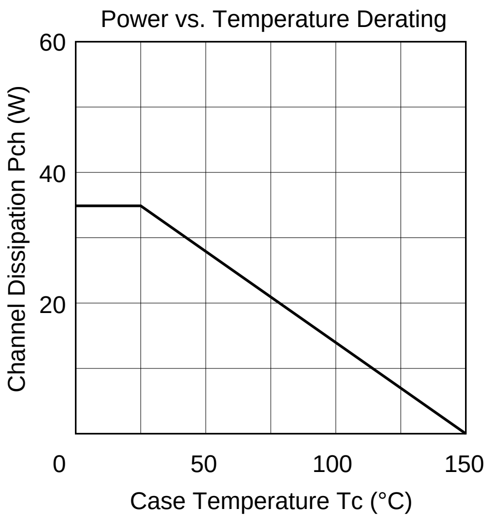
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

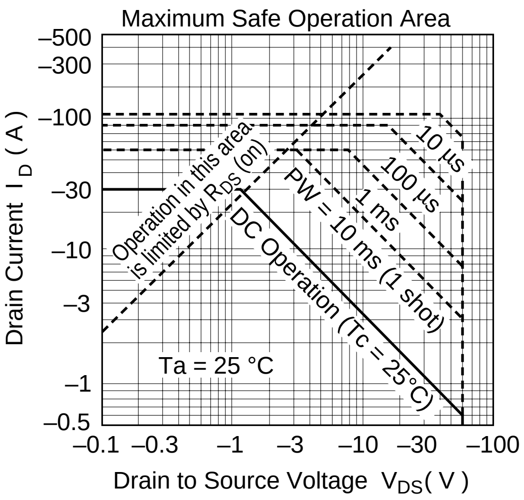
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.043	Ω	I_D = –15 A V_{GS} = –10 V *
		—	0.045	0.06	Ω	I_D = –15 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	17	25	—	S	I_D = –15 A V_{DS} = –10 V *
Input capacitance	Ciss	—	3300	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	1500	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	480	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = –15 A
Rise time	t_r	—	170	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	500	—	ns	R_L = 2 Ω
Fall time	t_f	—	390	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.5	—	V	I_F = –30 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = –30 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curve of 2SJ280.



Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)



Maximum Safe Operation Area
Drain Current I D (A)
–500
–300
–100
–30
–10
–3
–1
–0.5
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)
Operation in this area is limited by R DS (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25 °C

2SJ332L, 2SJ332S

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V Gate drive device can be driven from 5 V Source
- Suitable for Switching regulator, DC – DC converter

DPAK–2

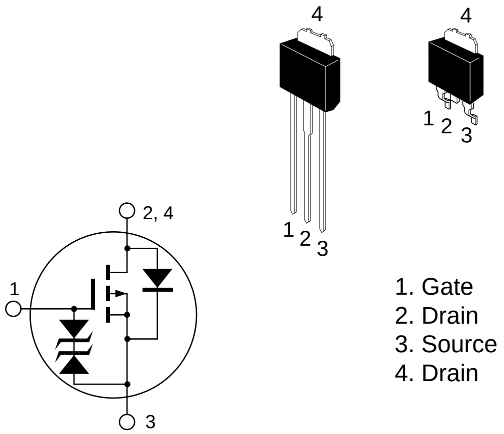


Table 1 Absolute Maximum Ratings (Ta = 25°C)

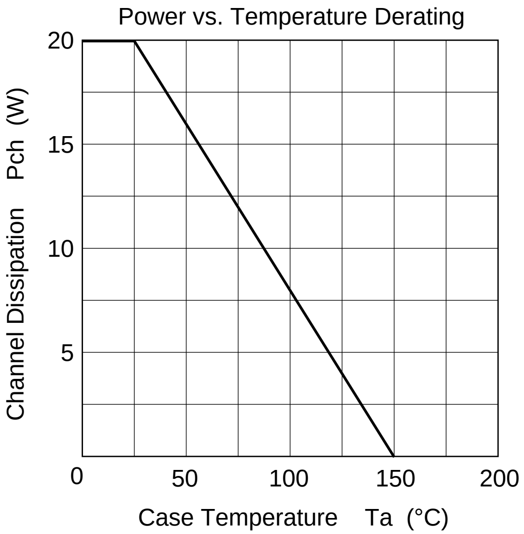
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–10	A
Drain peak current	$I_{D(pulse)}$*	–40	A
Body–drain diode reverse drain current	I_{DR}	–10	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

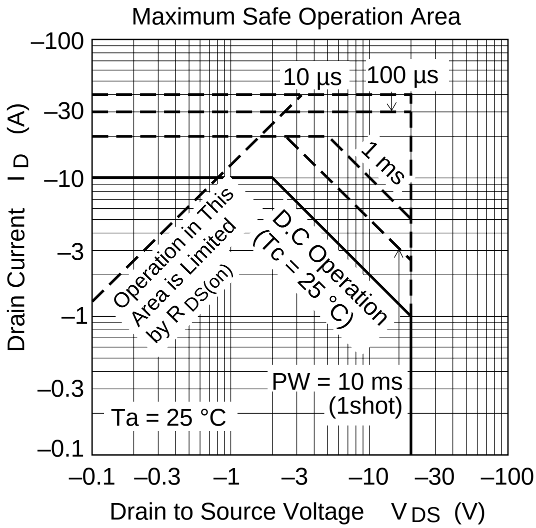
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C

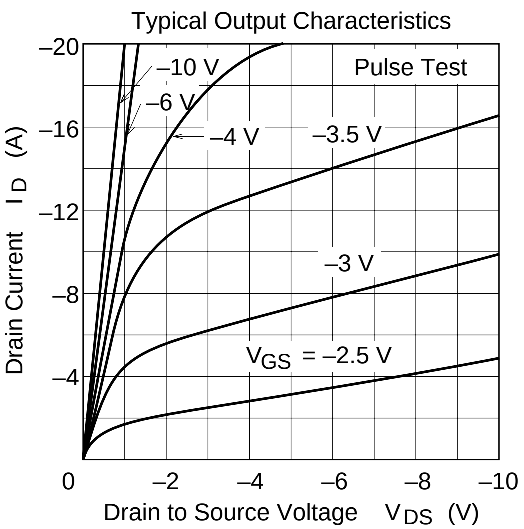
Table 2 Electrical Characteristics (Ta = 25°C)

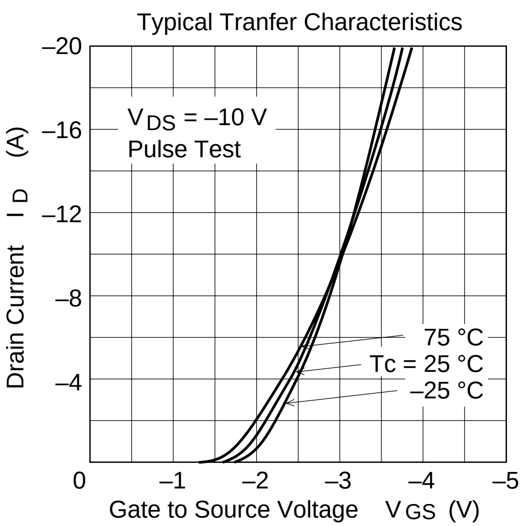
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.08	Ω	I_D = –5 A V_{GS} = –10 V *
		—	0.09	0.14	Ω	I_D = –5 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	6	9	—	S	I_D = –5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	730	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	680	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	260	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	13	—	ns	I_D = –5 A
Rise time	t_r	—	110	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	90	—	ns	R_L = 2 Ω
Fall time	t_f	—	110	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.2	—	V	I_F = –10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	50	—	µs	I_F = –10 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

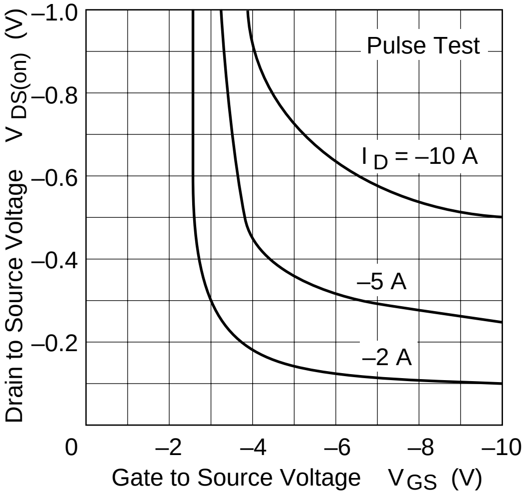

Power vs. Temperature Derating
Channel Dissipation Pch (W)
20
15
10
5
0
50
100
150
200
Case Temperature Ta (°C)


Maximum Safe Operation Area
Drain Current I D (A)
–100
–30
–10
–3
–1
–0.3
–0.1
10 µs
100 µs
1 ms
D.C Operation (Tc = 25 °C)
Operation in This Area is Limited by R DS(on)
PW = 10 ms (1shot)
Ta = 25 °C
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

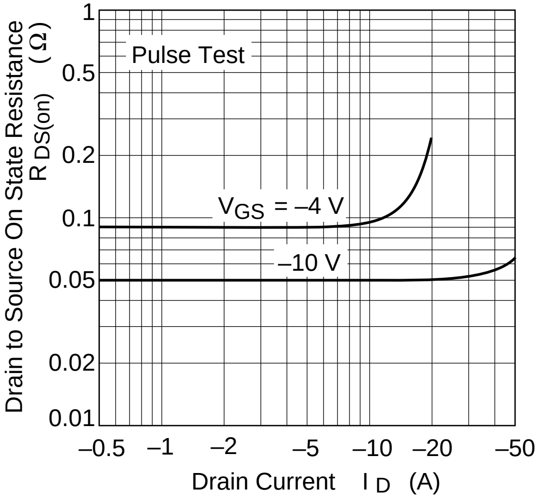

Typical Output Characteristics
Drain Current I D (A)
–20
–16
–12
–8
–4
0
–10 V
–6 V
–4 V
–3.5 V
–3 V
VGS = –2.5 V
Pulse Test
–2
–4
–6
–8
–10
Drain to Source Voltage VDS (V)


Typical Tranfer Characteristics
Drain Current I D (A)
–20
–16
–12
–8
–4
VDS = –10 V
Pulse Test
75 °C
Tc = 25 °C
–25 °C
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

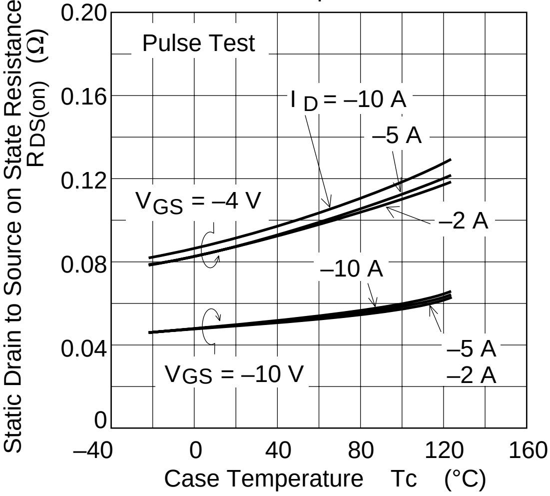
Drain to Source Saturation Voltage vs. Gate to Source Voltage



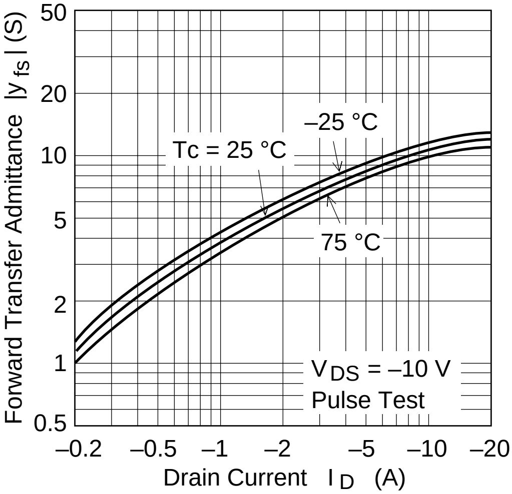
Static Drain to Source on State Resistance vs. Drain Current



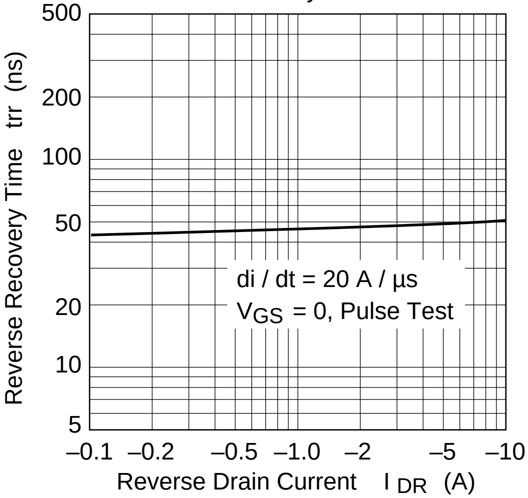
Static Drain to Source on State Resistance vs. Temperature



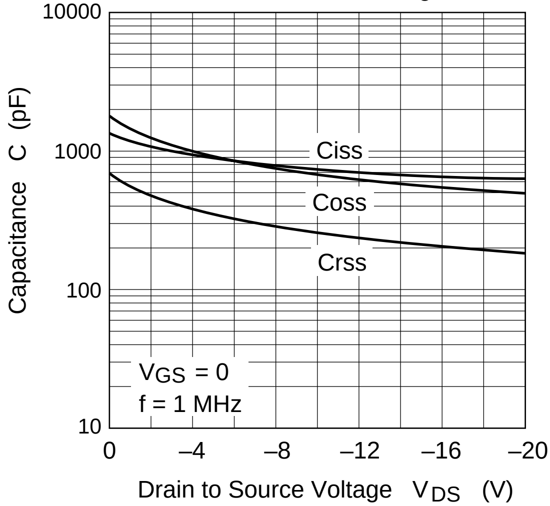
Forward Transfer Admittance vs. Drain Current



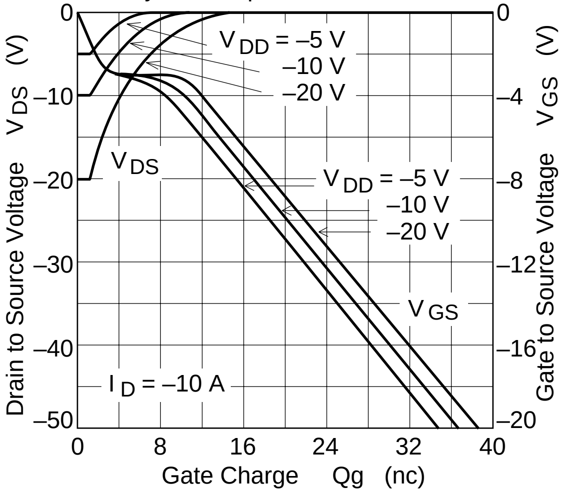
Body–Drain Diode Reverse Recovery Time



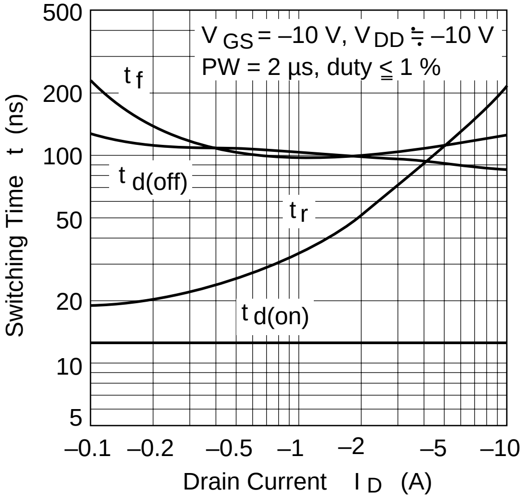
Typical Capacitance vs. Drain to Source Voltage

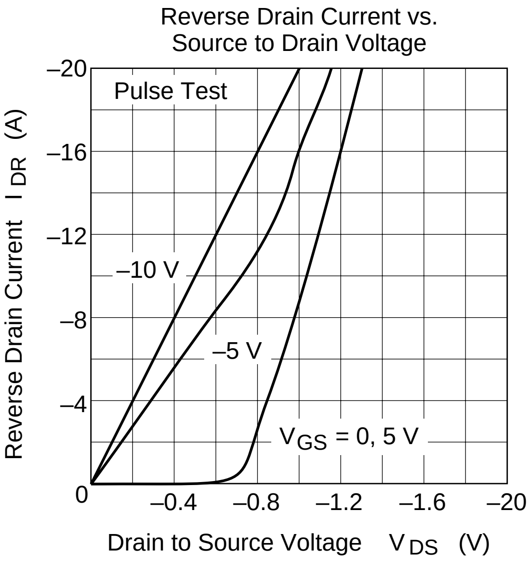


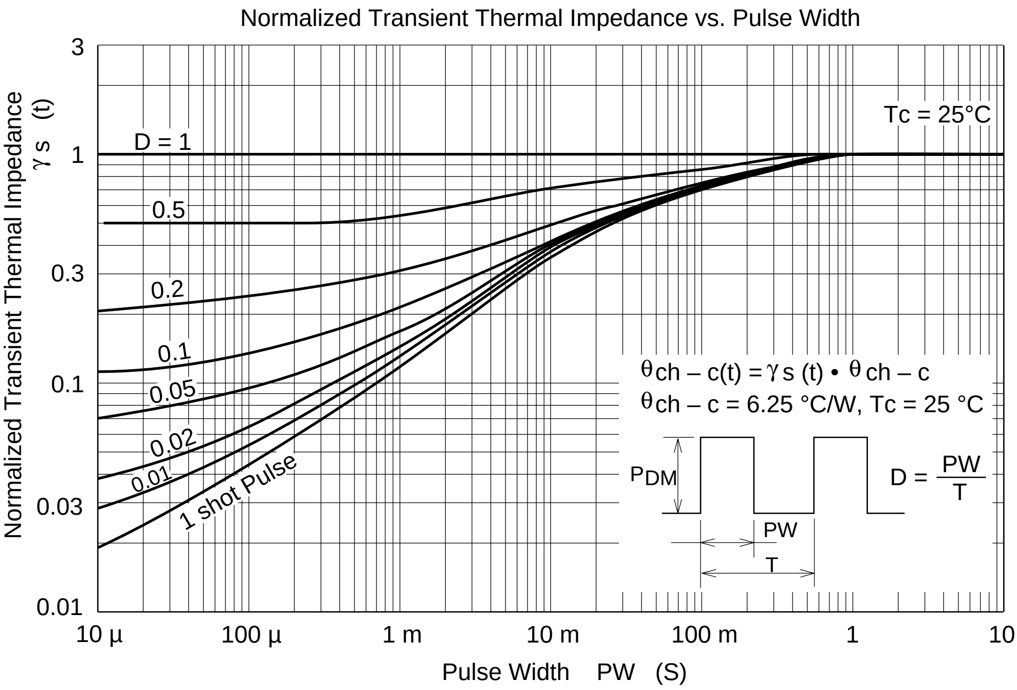
Dynamic Input Characteristics



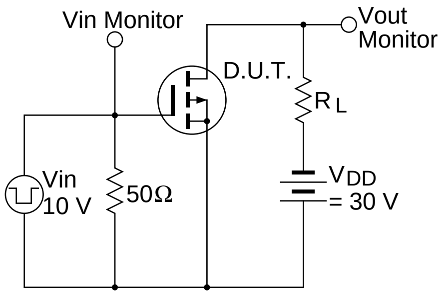
Switching Characteristics



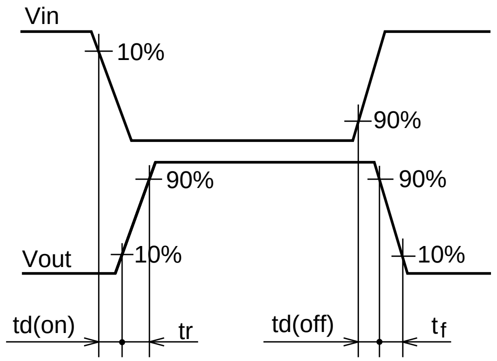

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
–10 V
–5 V
VGS = 0, 5 V
–20
–16
–12
–8
–4
0
–0.4
–0.8
–1.2
–1.6
–20
Reverse Drain Current I DR (A)
Drain to Source Voltage V DS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)

Switching Time Test Circuit



Waveforms



2SJ333(L), 2SJ333(S)

Silicon P-Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V Gate drive device can be driven from 5 V Source
- Suitable for Switching regulator, DC – DC converter

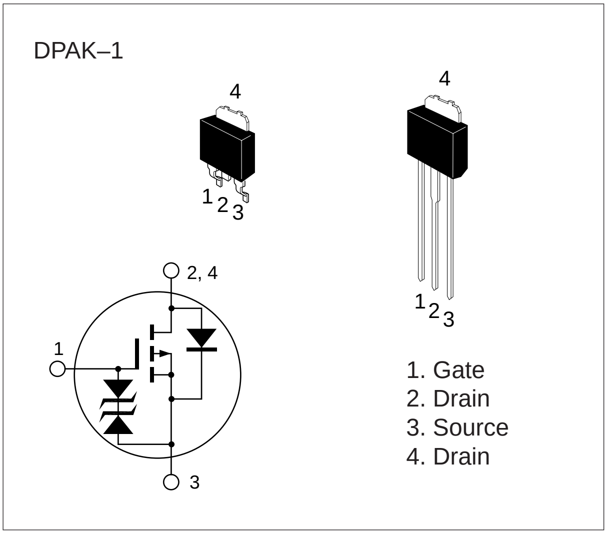


Table 1 Absolute Maximum Ratings (Ta = 25°C)

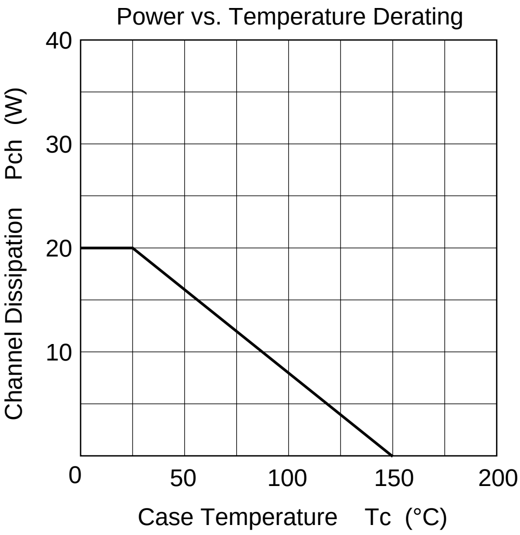
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–7	A
Drain peak current	$I_{D(pulse)}$*	–28	A
Body–drain diode reverse drain current	I_{DR}	–7	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

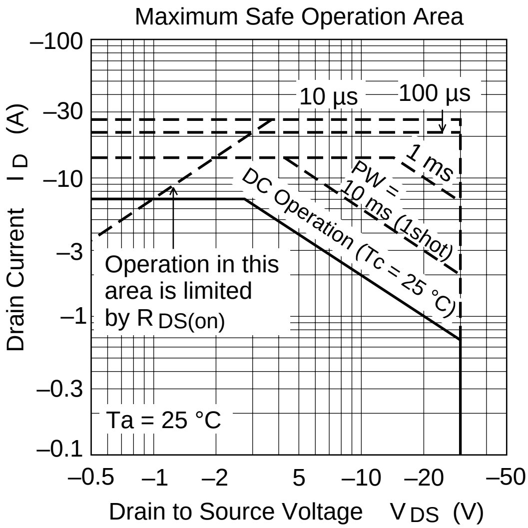
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C

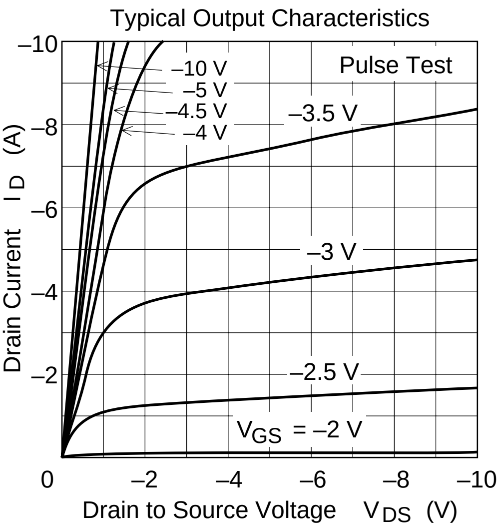
Table 2 Electrical Characteristics (Ta = 25°C)

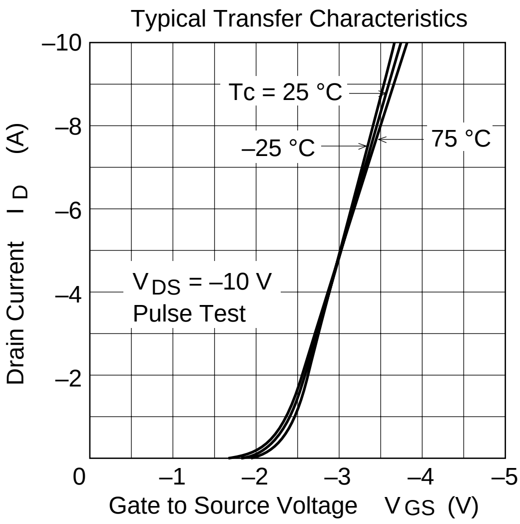
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.14	Ω	I_D = –4 A V_{GS} = –10 V *
		—	0.15	0.22	Ω	I_D = –4 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	4	6	—	S	I_D = –4 A V_{DS} = –10 V *
Input capacitance	Ciss	—	755	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	495	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	210	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	12	—	ns	I_D = –4 A
Rise time	t_r	—	50	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	120	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	120	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	µs	I_F = –7 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

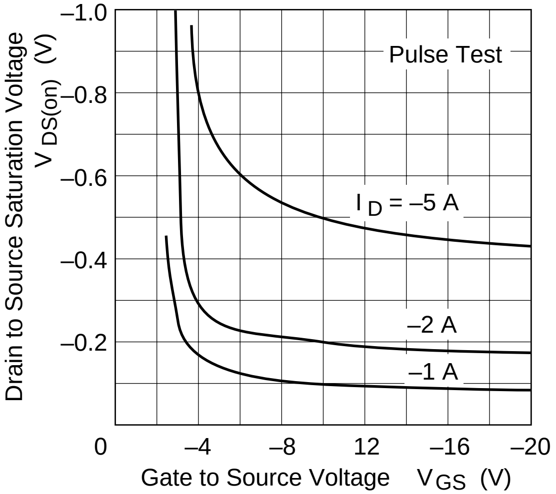

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
–100
–30
–10
–3
–1
–0.3
–0.1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
–0.5
–1
–2
5
–10
–20
–50
Drain to Source Voltage V DS (V)

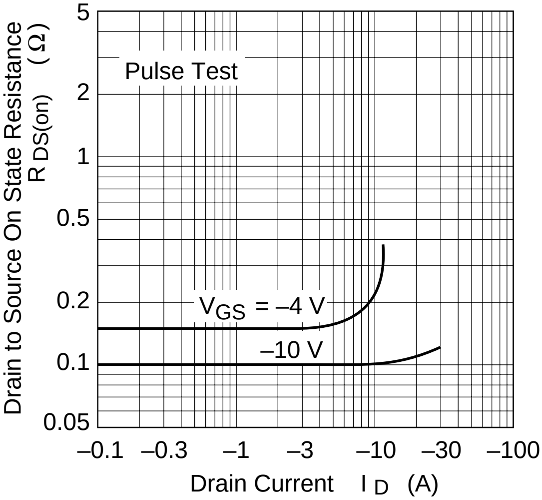

Typical Output Characteristics
Drain Current I D (A)
–10
–8
–6
–4
–2
0
–10 V
–5 V
–4.5 V
–4 V
–3.5 V
–3 V
–2.5 V
VGS = –2 V
Pulse Test
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
–10
–8
–6
–4
–2
0
Tc = 25 °C
–25 °C
75 °C
V DS = –10 V
Pulse Test
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

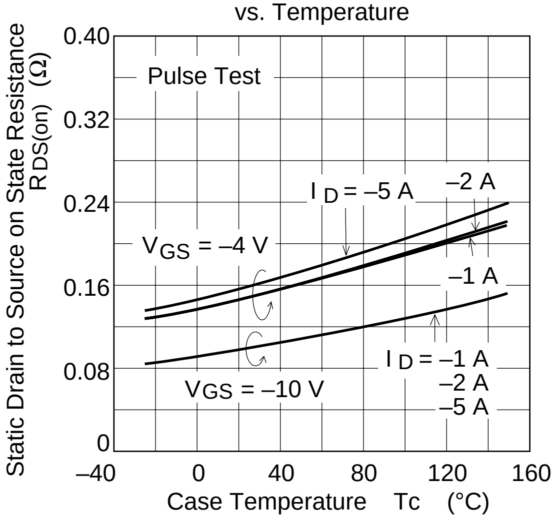
Drain to Source Saturation Voltage vs. Gate to Source Voltage



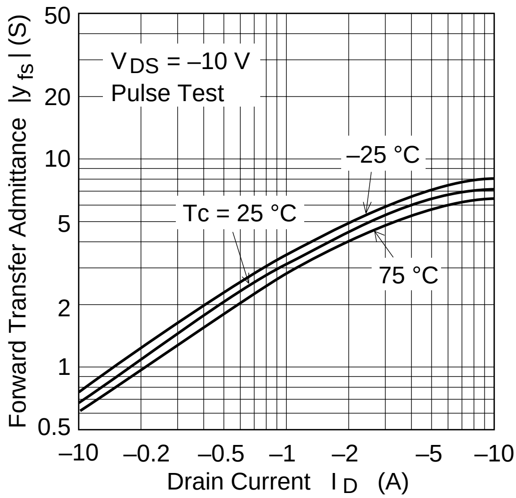
Static Drain to Source on State Resistance vs. Drain Current

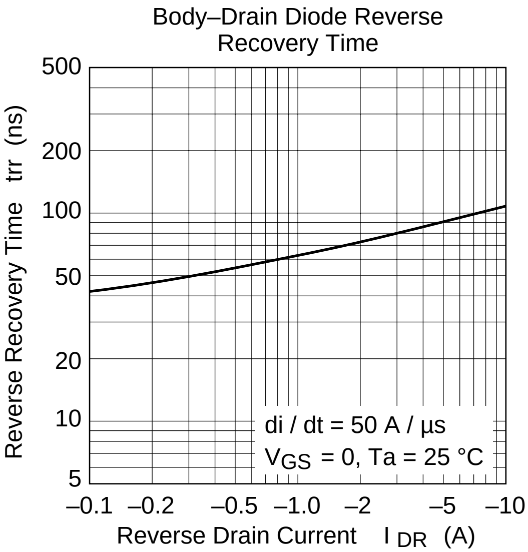


Static Drain to Source on State Resistance vs. Temperature

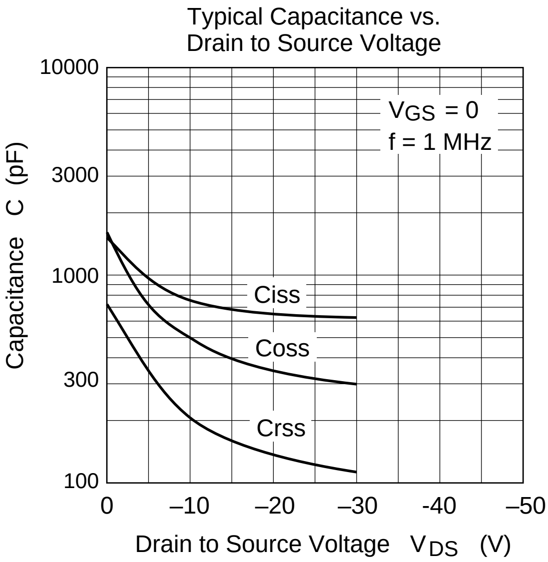


Forward Transfer Admittance vs. Drain Current

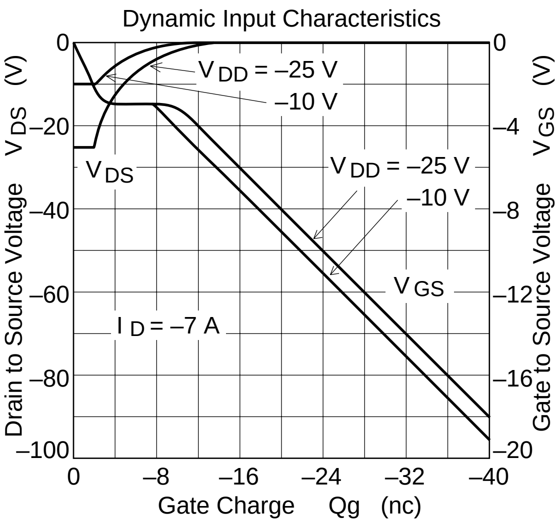




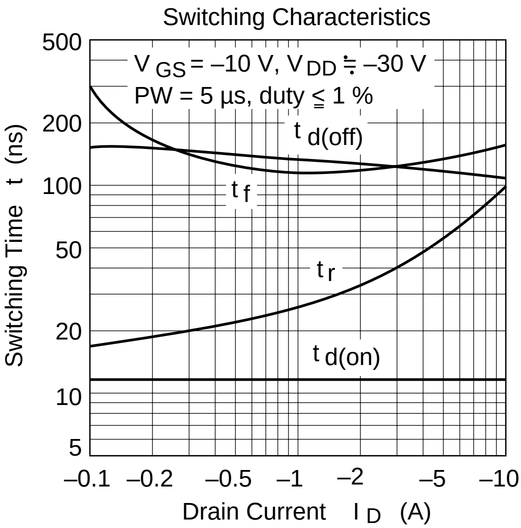
Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.2 –0.5 –1.0 –2 –5 –10
Reverse Drain Current I DR (A)



Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0 –10 –20 –30 -40 –50
Drain to Source Voltage VDS (V)

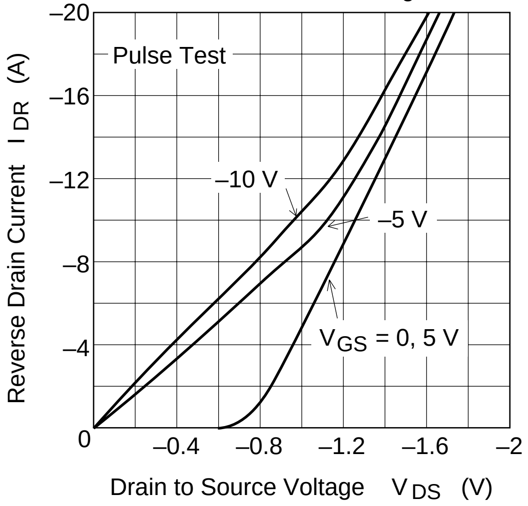


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–20
–40
–60
–80
–100
V DD = –25 V
–10 V
VDS
V DD = –25 V
–10 V
VGS
I D = –7 A
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
0 –8 –16 –24 –32 –40
Gate Charge Qg (nc)

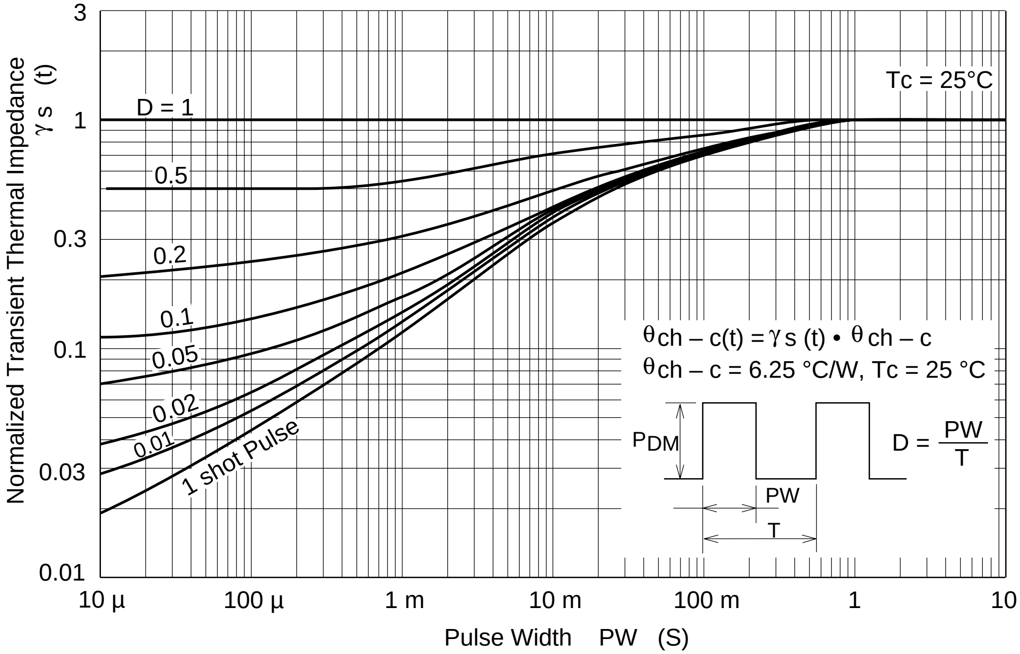


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
V GS = –10 V, V DD ≒ –30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)

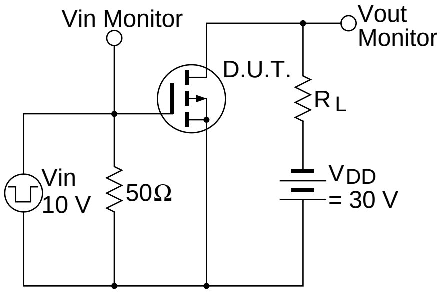
Reverse Drain Current vs. Source to Drain Voltage



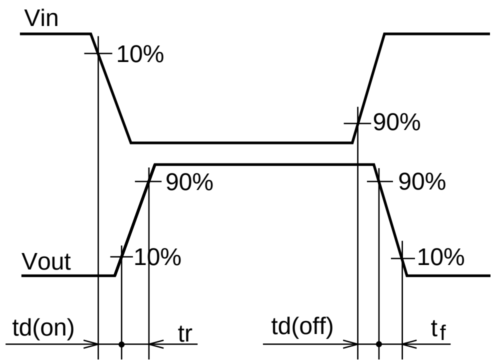
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveforms



2SJ350

Silicon P-Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

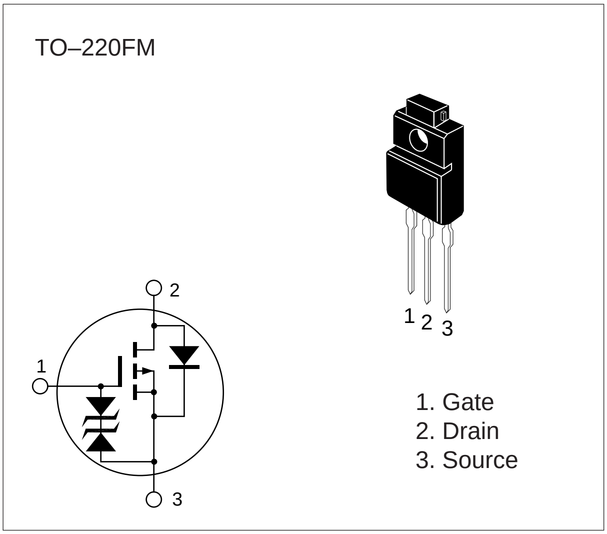
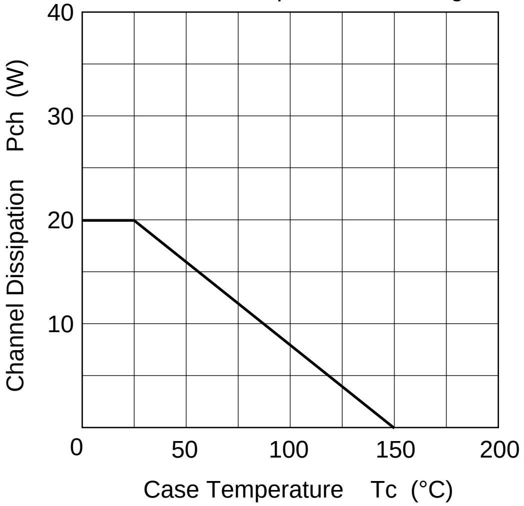


Table 1 Absolute Maximum Ratings (Ta = 25°C)

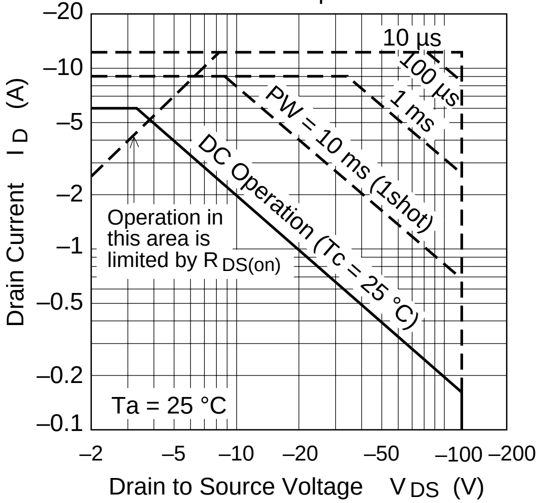
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–120	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–6	A
Drain peak current	$I_{D(pulse)}$*	–12	A
Body–drain diode reverse drain current	I_{DR}	–6	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

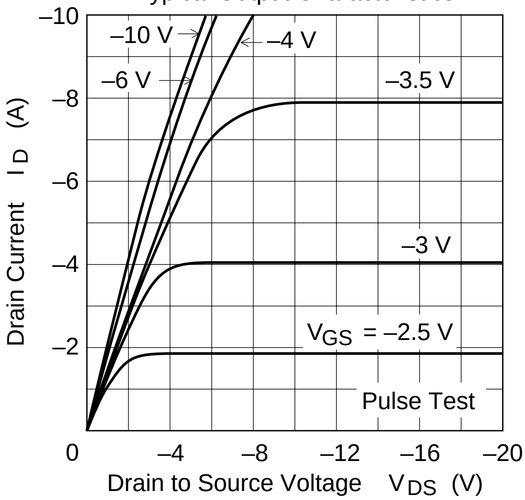
Power vs. Temperature Derating



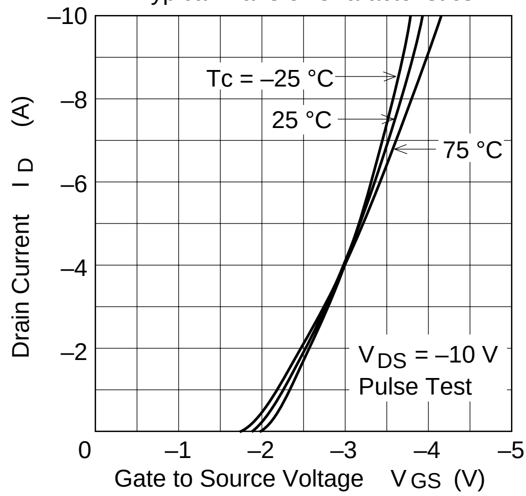
Maximum Safe Operation Area

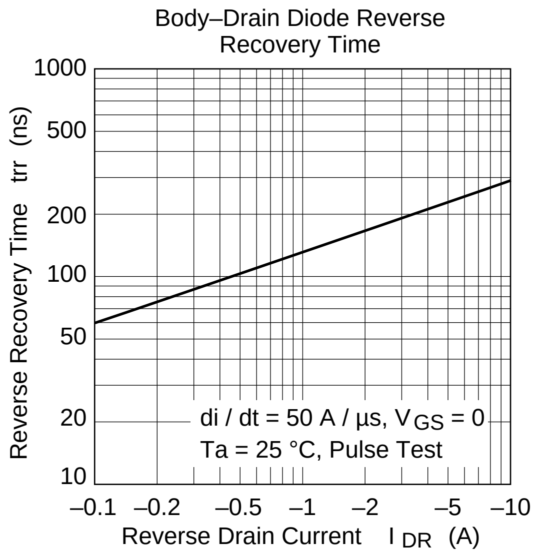


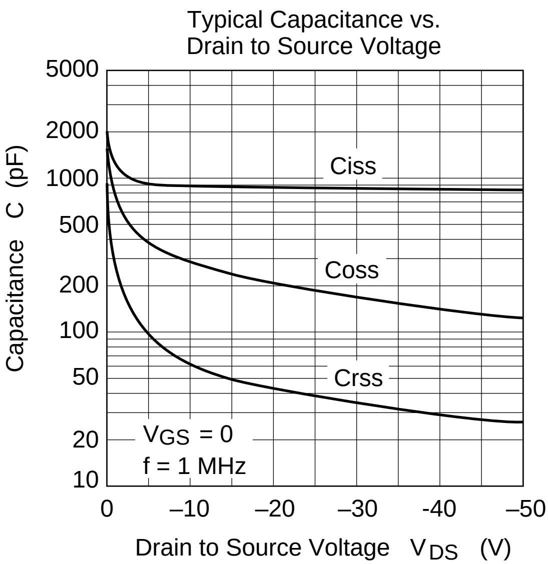
Typical Output Characteristics

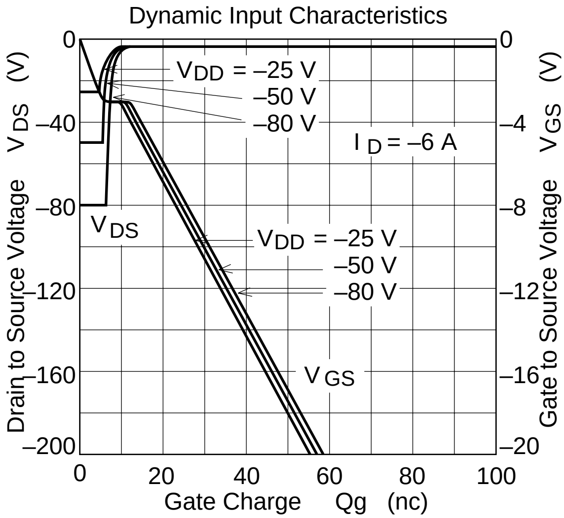


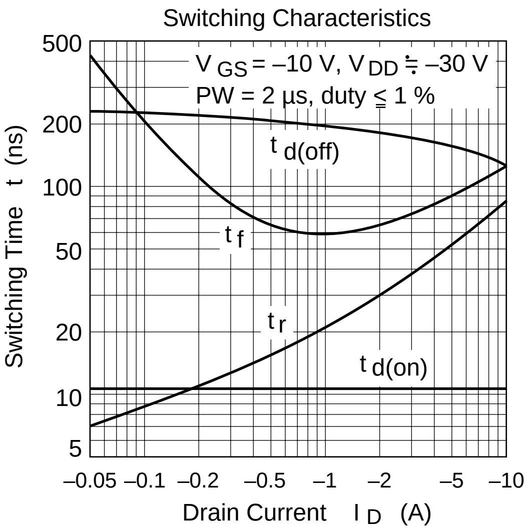
Typical Transfer Characteristics



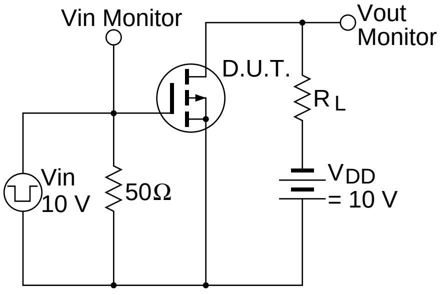

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 50 A / μs, VGS = 0
Ta = 25 °C, Pulse Test
–0.1 –0.2 –0.5 –1 –2 –5 –10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
20
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 -40 –50
Drain to Source Voltage VDS (V)

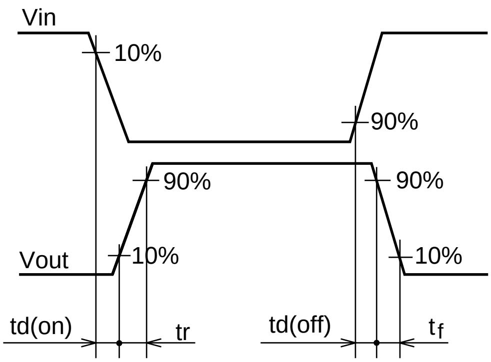

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–40
–80
–120
–160
–200
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
VDD = –25 V
–50 V
–80 V
I D = –6 A
VDS
VDD = –25 V
–50 V
–80 V
VGS
0 20 40 60 80 100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
V GS = –10 V, V DD ≒ –30 V
PW = 2 μs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
–0.05 –0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)

Switching Time Test Circuit



Waveforms

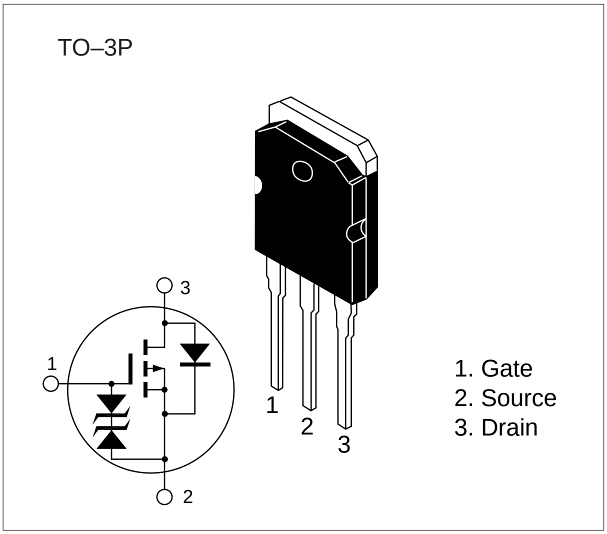


2SJ351, 2SJ352

Silicon P-Channel MOS FET

Application

Low frequency power amplifier
Complementary pair with 2SK2220
2SK2221



Features

- High power gain
- Excellent frequency response
- High speed switching
- Wide area of safe operation
- Enhancement–mode
- Good complementary characteristics
- Equipped with gate protection diodes

Table 1 Ordering Information

Type No.	V_{DSS}
2SJ351	–180 V
2SJ352	–200 V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

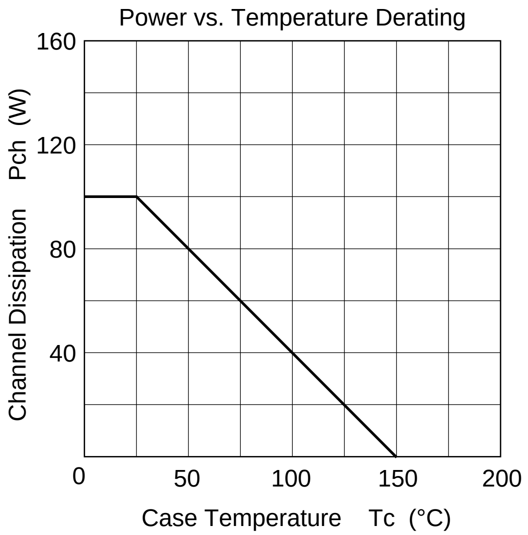
Item		Symbol	Ratings	Unit
Drain to source voltage	2SJ351	V_{DSX}	–180	V
	2SJ352		–200	
Gate to source voltage		V_{GSS}	±20	V
Drain current		I_D	–8	A
Body–drain diode reverse drain current		I_{DR}	–8	A
Channel dissipation		Pch*	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

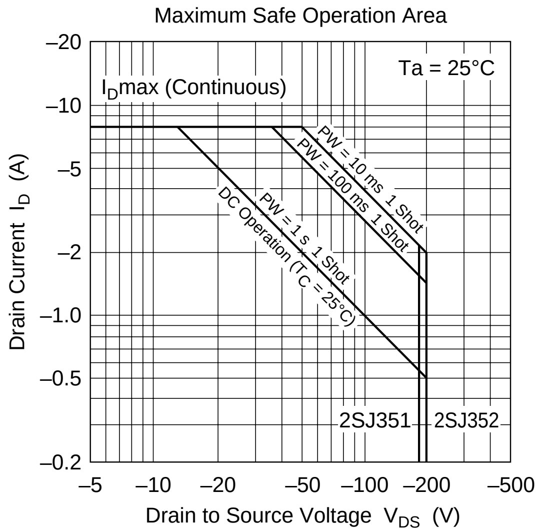
* Value at Tc = 25 °C

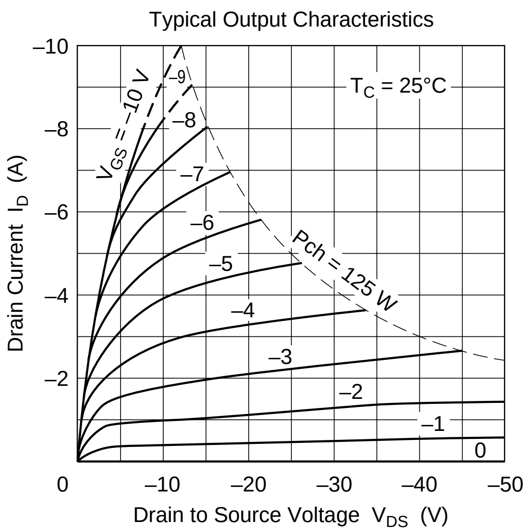
Table 3 Electrical Characteristics (Ta = 25°C)

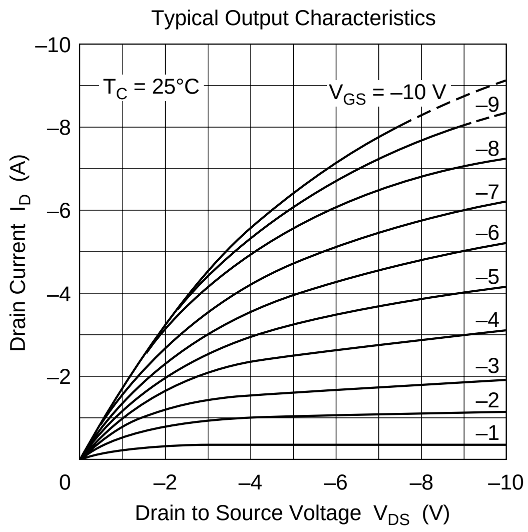
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SJ351	$V_{(BR)DSX}$	–180	—	—	V	I_D = –10 mA, V_{GS} = 10 V
	2SJ352		–200	—	—		
Gate to source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	–0.15	—	–1.45	V	I_D = –100 mA V_{DS} = –10 V
Drain to source saturation voltage		$V_{DS(sat)}$	—	—	–12	V	I_D = –8 A, V_{GD} = 0 V*
Forward transfer admittance		$\|y_{fs}\|$	0.7	1.0	1.4	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance		Ciss	—	800	—	pF	V_{GS} = 5 V
Output capacitance		Coss	—	1000	—	pF	V_{DS} = –10 V
Reverse transfer capacitance		Crss	—	18	—	pF	f = 1 MHz
Turn–on time		t_{on}	—	320	—	ns	V_{DD} = –30 V
Turn–off time		t_{off}	—	120	—	ns	I_D = –4 A

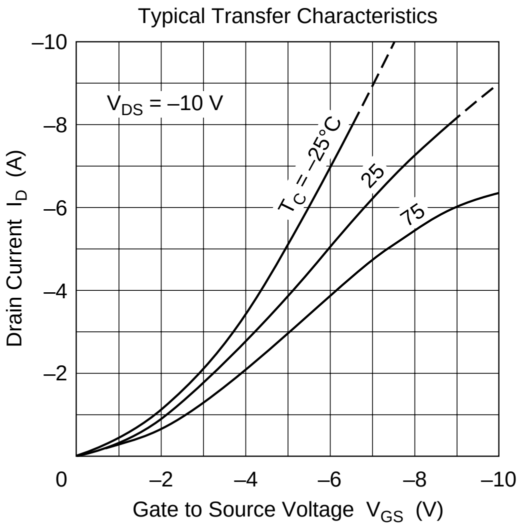
* Pulse Test

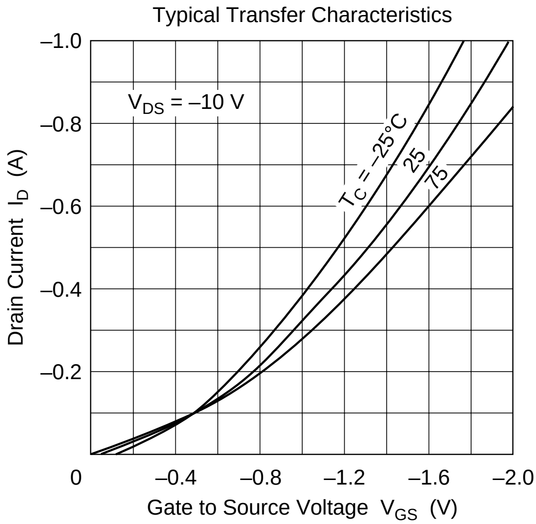

Power vs. Temperature Derating
Channel Dissipation Pch (W)
160
120
80
40
0
50
100
150
200
Case Temperature Tc (°C)

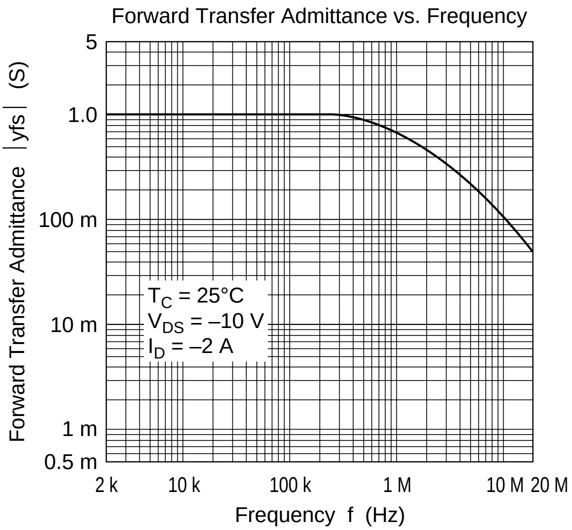

Maximum Safe Operation Area
Ta = 25°C
IDmax (Continuous)
PW = 10 ms 1 Shot
PW = 100 ms 1 Shot
PW = 1 s 1 Shot
DC Operation (TC = 25°C)
2SJ351
2SJ352
Drain Current ID (A)
–20
–10
–5
–2
–1.0
–0.5
–0.2
–5
–10
–20
–50
–100
–200
–500
Drain to Source Voltage VDS (V)

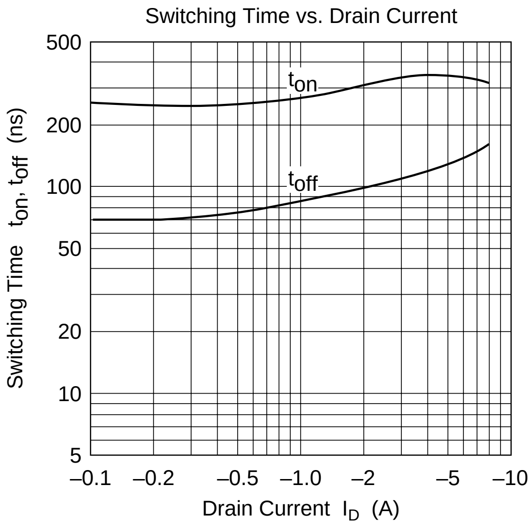

Typical Output Characteristics
TC = 25°C
VGS = –10 V
–9
–8
–7
–6
–5
–4
–3
–2
–1
0
Pch = 125 W
Drain Current ID (A)
–10
–8
–6
–4
–2
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)

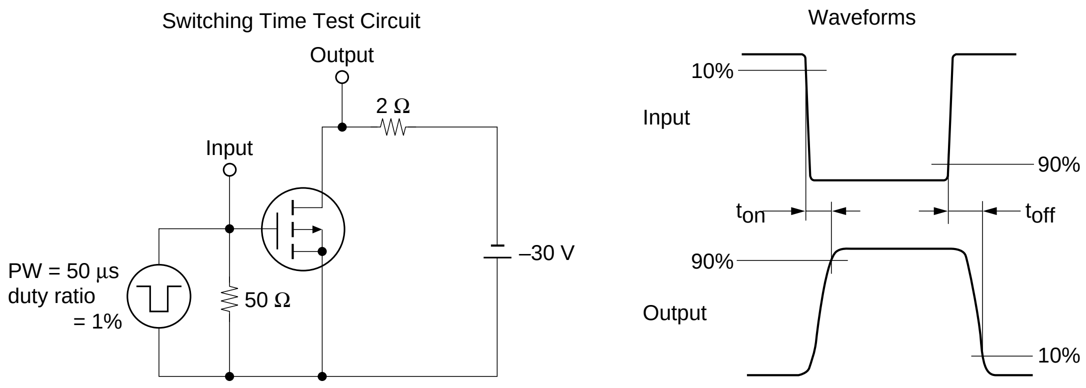

Typical Output Characteristics
TC = 25°C
VGS = –10 V
–9
–8
–7
–6
–5
–4
–3
–2
–1
Drain Current ID (A)
–10
–8
–6
–4
–2
0
–2
–4
–6
–8
–10
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
V_{DS} = –10 V
T_C = –25°C
25
75
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)


Typical Transfer Characteristics
V_{DS} = –10 V
T_C = –25°C
25
75
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)


Forward Transfer Admittance vs. Frequency
T_C = 25°C
V_{DS} = –10 V
I_D = –2 A
Forward Transfer Admittance |yfs| (S)
Frequency f (Hz)


Switching Time vs. Drain Current
t_{on}
t_{off}
Switching Time t_{on}, t_{off} (ns)
Drain Current I_D (A)


Switching Time Test Circuit
Output
2 Ω
Input
PW = 50 μs
duty ratio
= 1%
50 Ω
–30 V
Waveforms
10%
Input
90%
t_{on}
t_{off}
90%
Output
10%

2SJ361

Silicon P-Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device can be driven from 3 V source

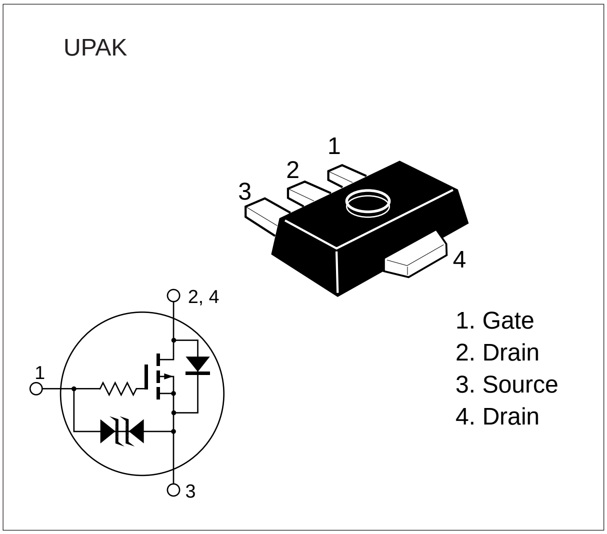


Table 1   Absolute Maximum Ratings (Ta = 25°C)

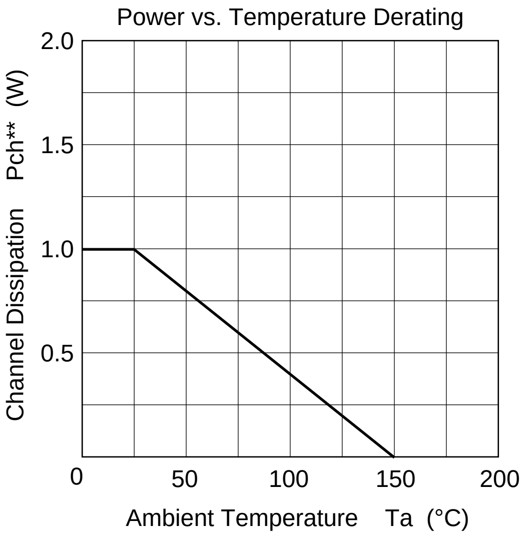
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2	A
Drain peak current	$I_{D(pulse)}$*	–4	A
Body–drain diode reverse drain current	I_{DR}	–2	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

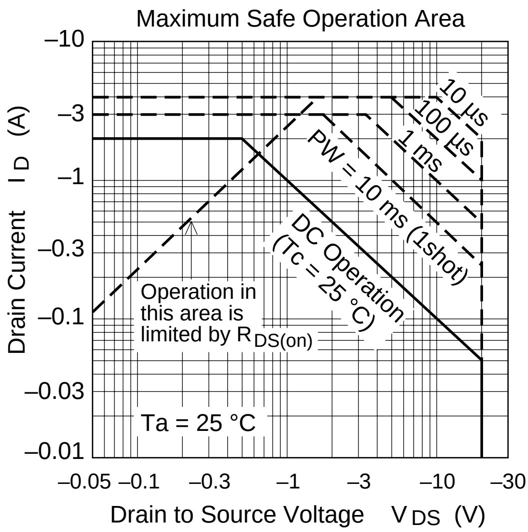
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value on the alumina ceramic board (12.5 x 20 x 0.7mm)
*** Marking is “RY”.

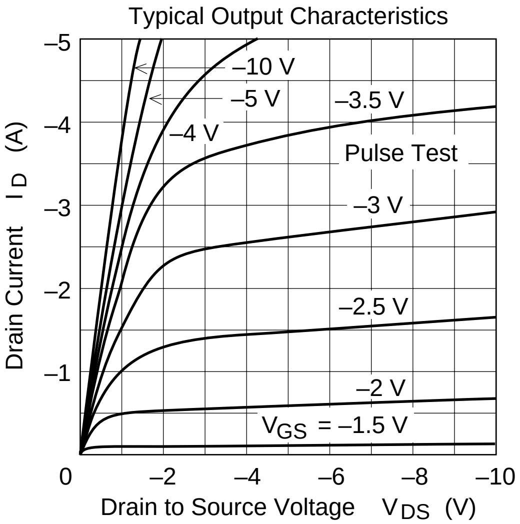
Table 2 Electrical Characteristics (Ta = 25°C)

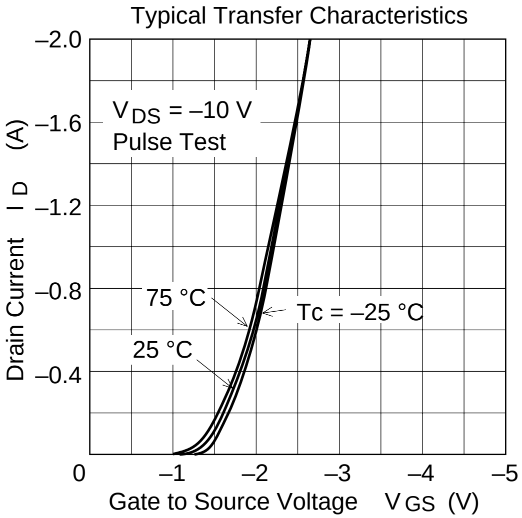
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.28	0.4	Ω	I_D = –1 A V_{GS} = –10 V
		—	0.85	1.5	Ω	I_D = –0.4 A V_{GS} = –2.5 V
Forward transfer admittance	$\|y_{fs}\|$	0.15	0.3	—	S	I_D = –10 A V_{DS} = –10 V
Input capacitance	Ciss	—	3.2	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	130	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.6	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	350	—	ns	I_D = –1 A
Rise time	t_r	—	1650	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	7280	—	ns	R_L = 10 Ω
Fall time	t_f	—	6950	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –2 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	530	—	µs	I_F = –2 A, V_{GS} = 0, diF / dt = 20 A / µs

* Pulse Test

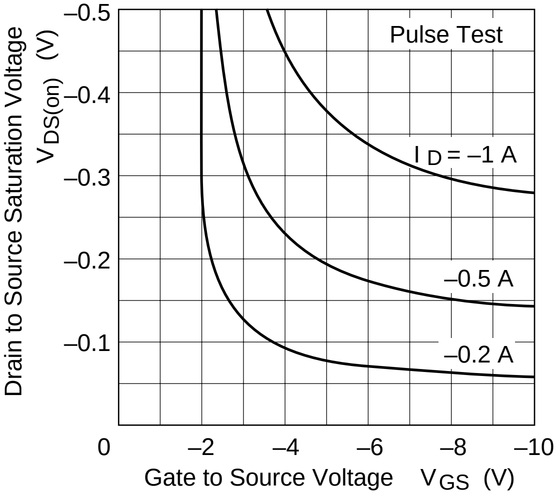

Power vs. Temperature Derating
Channel Dissipation Pch** (W)
2.0
1.5
1.0
0.5
0
50
100
150
200
Ambient Temperature Ta (°C)


Maximum Safe Operation Area
Drain Current I D (A)
–10
–3
–1
–0.3
–0.1
–0.03
–0.01
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation
(Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
–0.05
–0.1
–0.3
–1
–3
–10
–30
Drain to Source Voltage V DS (V)

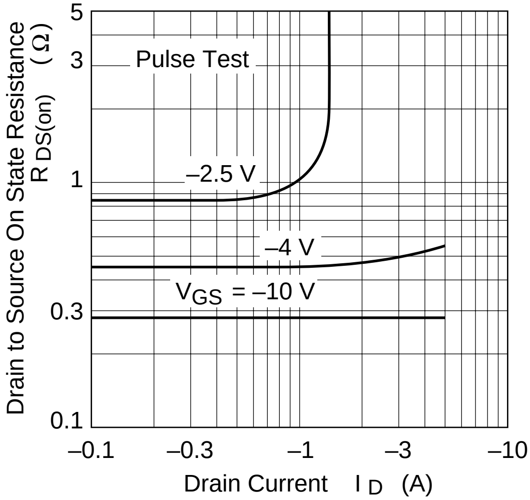

Typical Output Characteristics
Drain Current I D (A)
–5
–4
–3
–2
–1
–10 V
–5 V
–4 V
–3.5 V
Pulse Test
–3 V
–2.5 V
–2 V
VGS = –1.5 V
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
–2.0
–1.6
–1.2
–0.8
–0.4
VDS = –10 V
Pulse Test
75 °C
Tc = –25 °C
25 °C
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

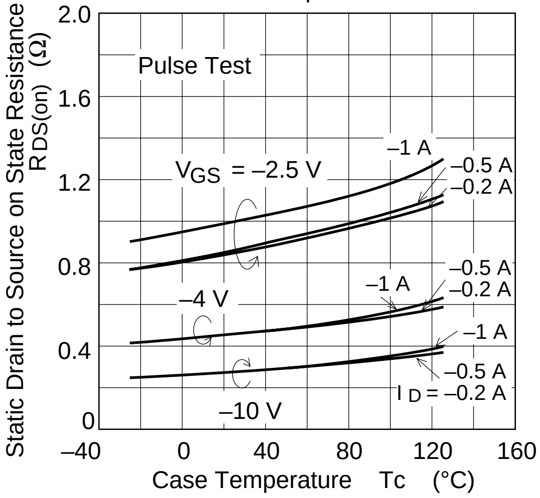
Drain to Source Saturation Voltage vs. Gate to Source Voltage



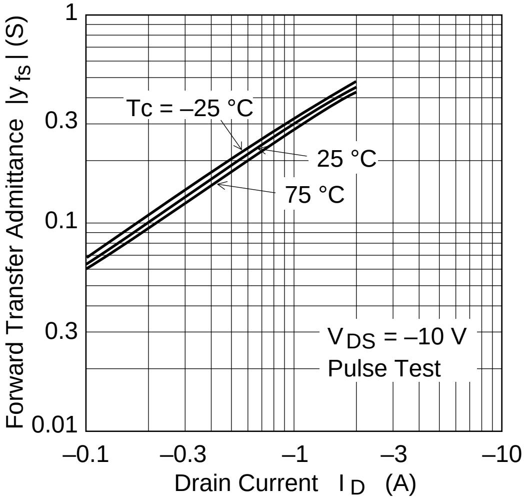
Static Drain to Source on State Resistance vs. Drain Current

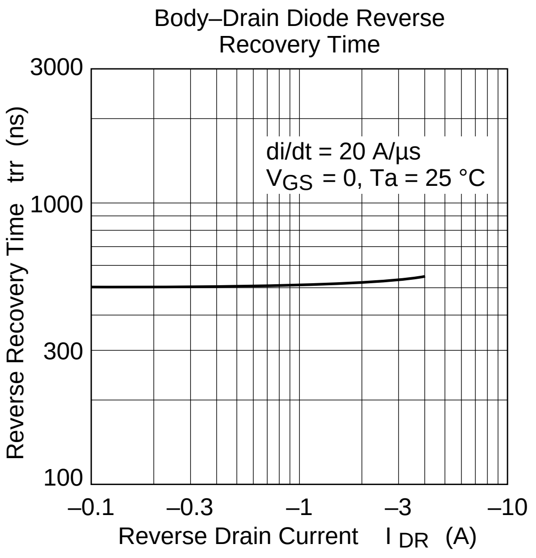


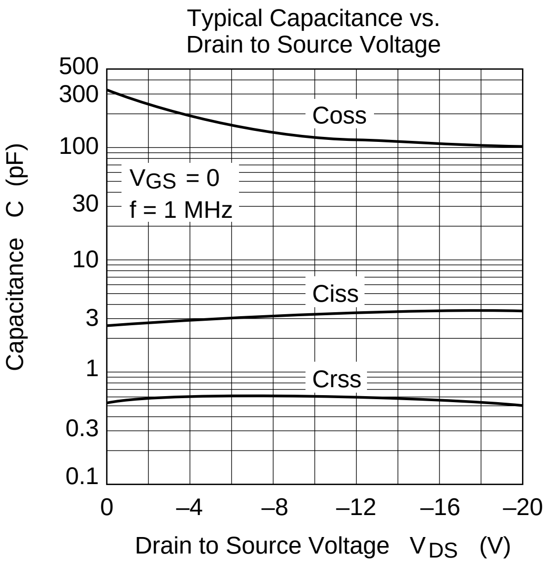
Static Drain to Source on State Resistance vs. Temperature

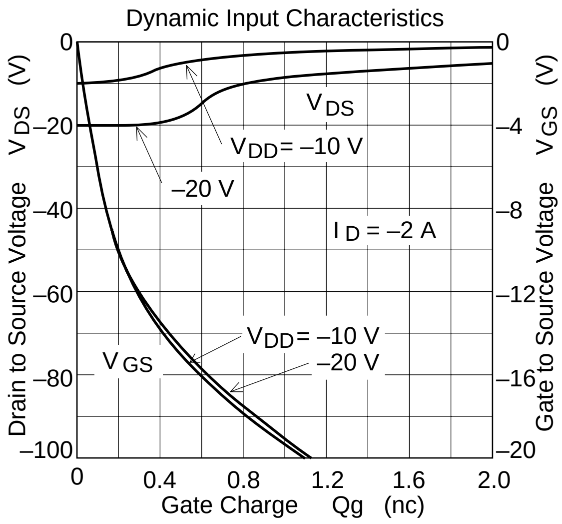


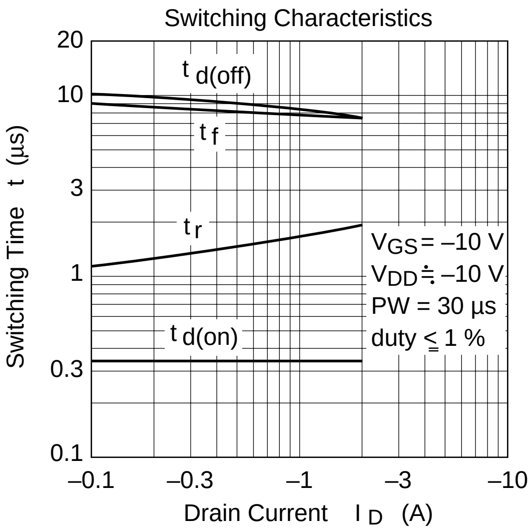
Forward Transfer Admittance vs. Drain Current

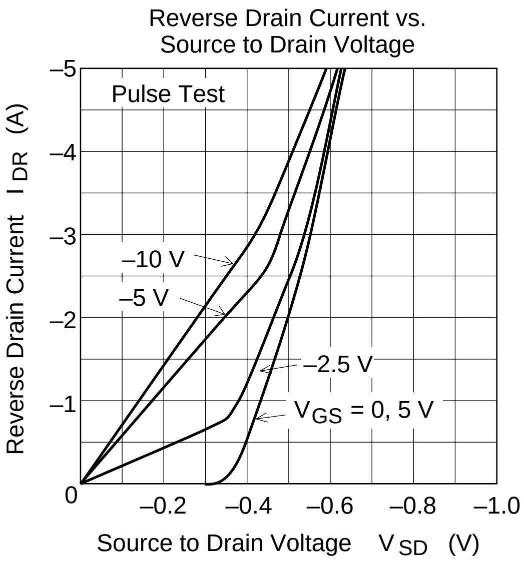



Body–Drain Diode Reverse
Recovery Time
di/dt = 20 A/μs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
3000
1000
300
100
–0.1
–0.3
–1
–3
–10
Reverse Drain Current I DR (A)

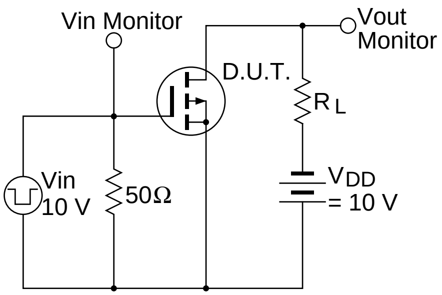

Typical Capacitance vs.
Drain to Source Voltage
Coss
Ciss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
500
300
100
30
10
3
1
0.3
0.1
0
–4
–8
–12
–16
–20
Drain to Source Voltage V DS (V)


Dynamic Input Characteristics
Drain to Source Voltage V DS (V)
Gate to Source Voltage V GS (V)
V DS
V DD = –10 V
–20 V
I D = –2 A
V GS
V DD = –10 V
–20 V
0
–20
–40
–60
–80
–100
0
–4
–8
–12
–16
–20
0
0.4
0.8
1.2
1.6
2.0
Gate Charge Qg (nc)

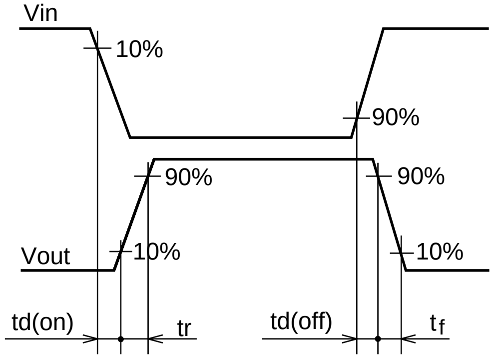

Switching Characteristics
t d(off)
t f
t r
t d(on)
VGS = –10 V
VDD ≒ –10 V
PW = 30 μs
duty ≦ 1 %
Switching Time t (μs)
20
10
3
1
0.3
0.1
–0.1
–0.3
–1
–3
–10
Drain Current I D (A)



Switching Time Test Circuit



Waveforms



2SJ363

Silicon P Channel MOS FET

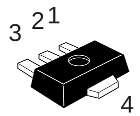
Application

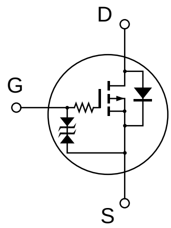
Low frequency power switching

Features

- Low on–resistance
- Low drive current
- 4 V gate drive device can be driven from 5 V source

UPAK





1. Gate
2. Drain
3. Source
4. Drain

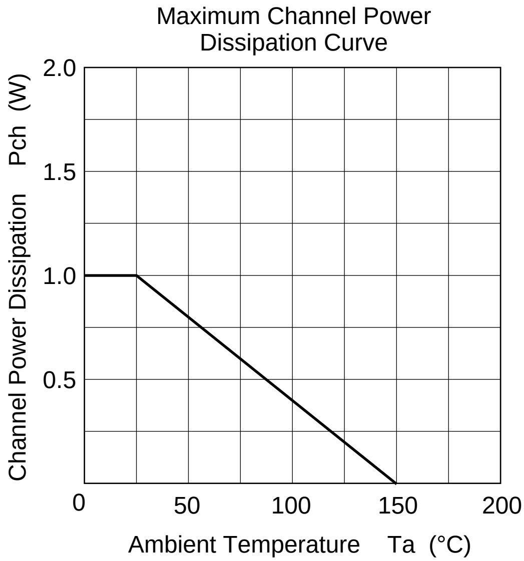
Table 1 Absolute Maximum Ratings (Ta = 25°C)

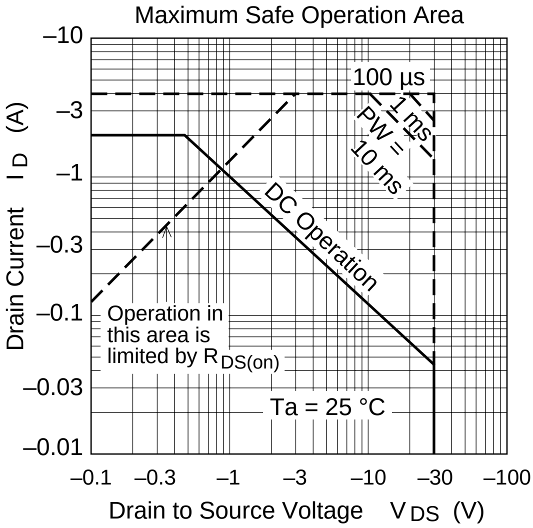
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2	A
Drain peak current	$I_{D(pulse)}$*	–4	A
Body–drain diode reverse drain current	I_{DR}	–2	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

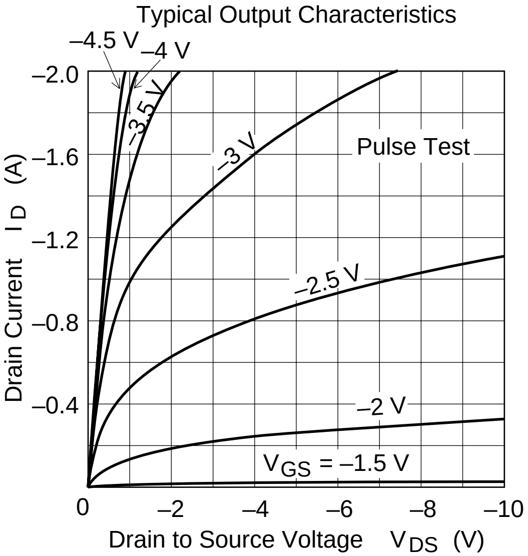
* PW ≤ 100 µs, duty cycle ≤ 10 %
** Value on the alumina ceramic board (12.5 x 20 x 0.7mm)
*** Marking is “PY”.

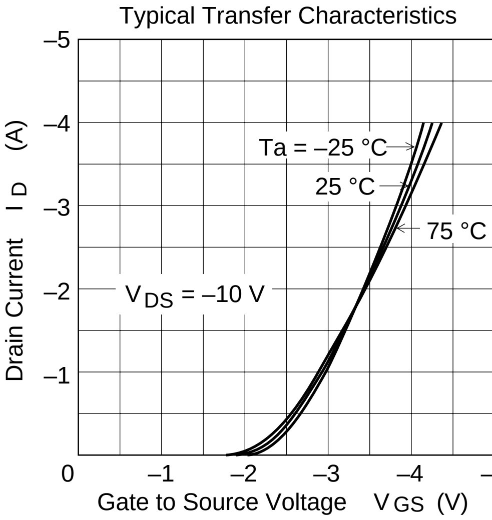
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –24 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D=–100 µA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.6	0.75	Ω	I_D = –1 A V_{GS} = –4 V *
		—	0.35	0.45	Ω	I_D = –1 A V_{GS} = –10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.4	2.0	—	S	I_D = –1 A V_{DS} = –10 V *
Input capacitance	Ciss	—	2.1	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	100	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.25	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	1.65	—	µs	I_D = –1 A
Rise time	t_r	—	8	—	µs	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	25.9	—	µs	R_L = 30 Ω
Fall time	t_f	—	14.9	—	µs	

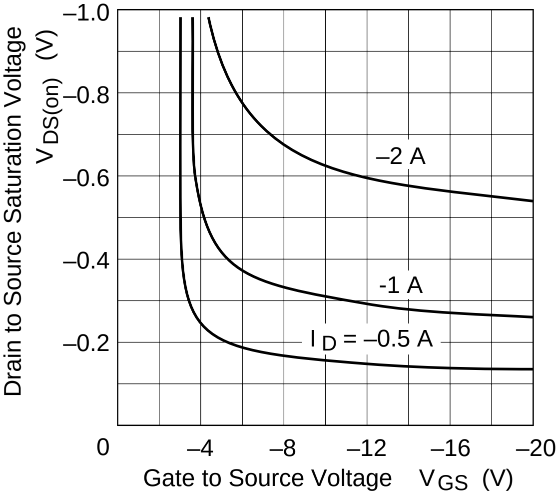

Maximum Channel Power
Dissipation Curve
Channel Power Dissipation Pch (W)
2.0
1.5
1.0
0.5
0
50
100
150
200
Ambient Temperature Ta (°C)


Maximum Safe Operation Area
Drain Current I D (A)
–10
–3
–1
–0.3
–0.1
–0.03
–0.01
100 µs
1 ms
PW =
10 ms
DC Operation
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

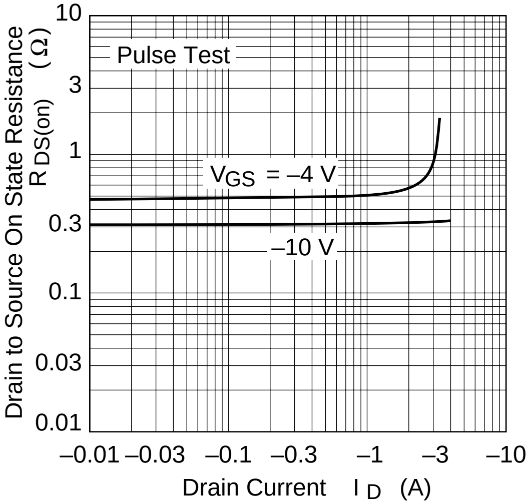

Typical Output Characteristics
–4.5 V
–4 V
–3.5 V
–3 V
–2.5 V
–2 V
V GS = –1.5 V
Pulse Test
Drain Current I D (A)
–2.0
–1.6
–1.2
–0.8
–0.4
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
–5
–4
–3
–2
–1
Ta = –25 °C
25 °C
75 °C
V DS = –10 V
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

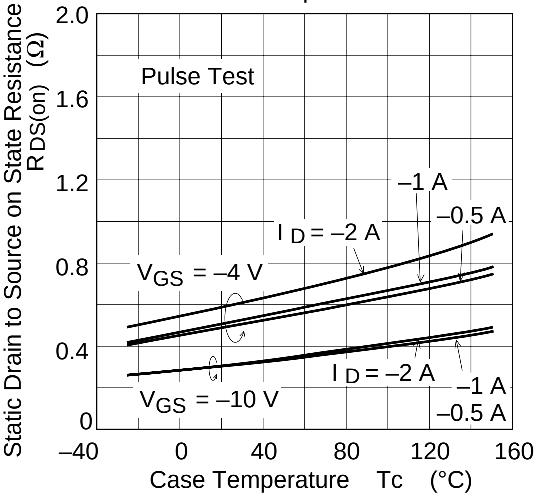
Drain to Source Saturation Voltage vs. Gate to Source Voltage



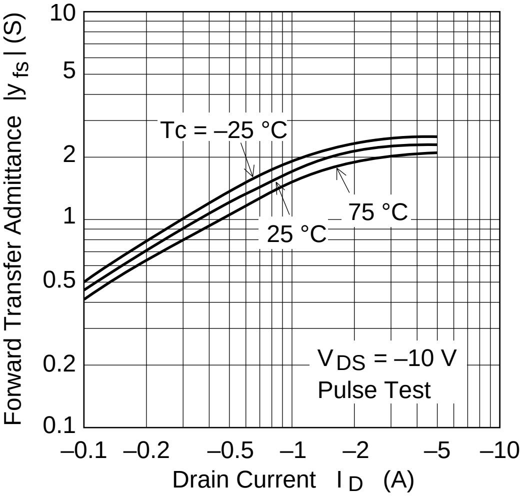
Static Drain to Source on State Resistance vs. Drain Current

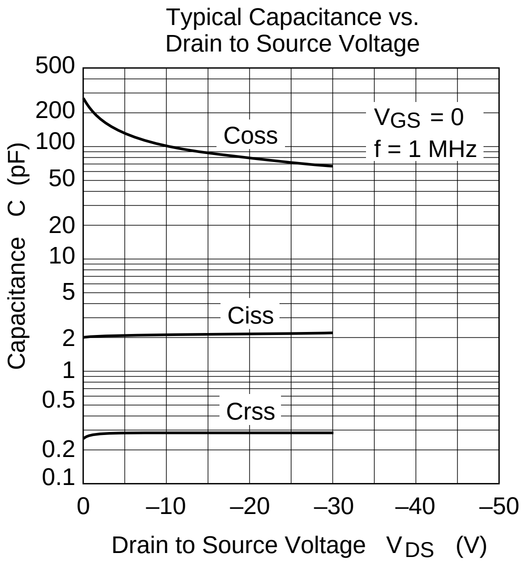


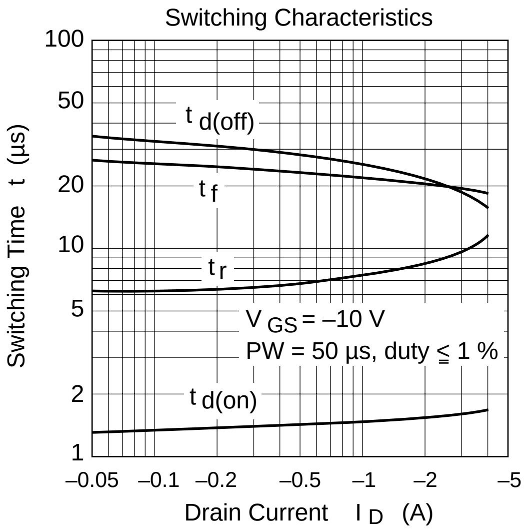
Static Drain to Source on State Resistance vs. Temperature

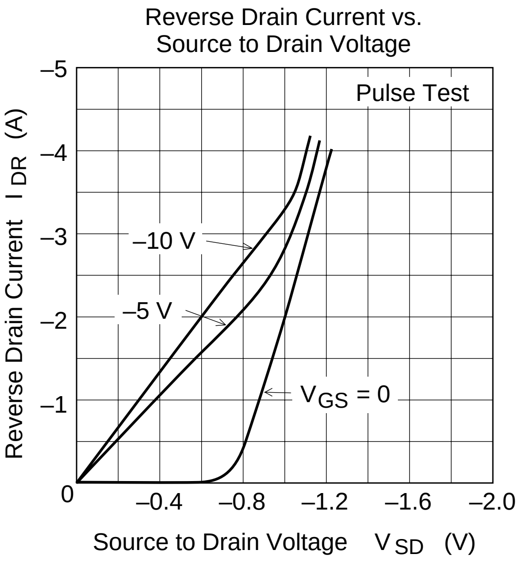


Forward Transfer Admittance vs. Drain Current




Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
500
200
100
50
20
10
5
2
1
0.5
0.2
0.1
VGS = 0
f = 1 MHz
Coss
Ciss
Crss
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)


Switching Characteristics
Switching Time t (µs)
100
50
20
10
5
2
1
t d(off)
t f
t r
V GS = –10 V
PW = 50 µs, duty ≦ 1 %
t d(on)
–0.05
–0.1
–0.2
–0.5
–1
–2
–5
Drain Current I D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
–5
–4
–3
–2
–1
0
Pulse Test
–10 V
–5 V
VGS = 0
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage V SD (V)

2SJ384(L), 2SJ384(S)

Silicon P-Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device can be driven from 3 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

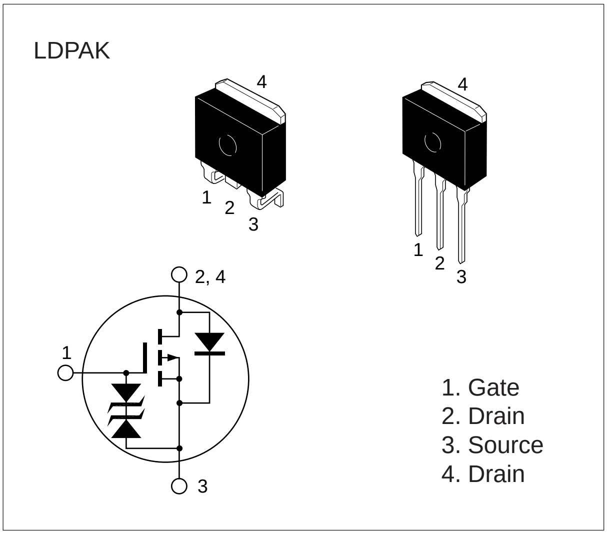


Table 1 Absolute Maximum Ratings (Ta = 25°C)

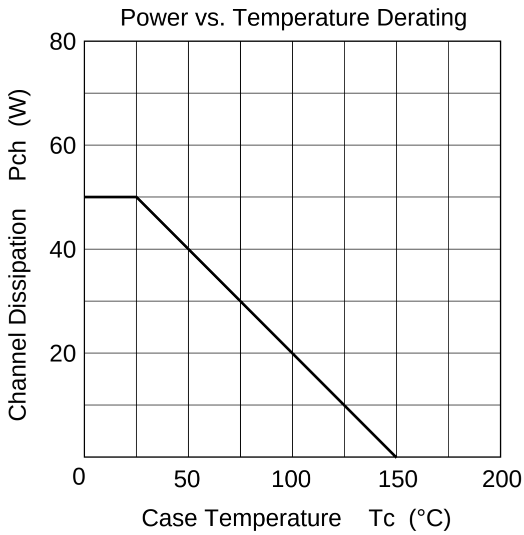
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–15	A
Drain peak current	$I_{D(pulse)}$*	–60	A
Body–drain diode reverse drain current	I_{DR}	–15	A
Avalanche current	I_{AP}***	–15	A
Avalanche energy	E_{AR}***	19	mJ
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

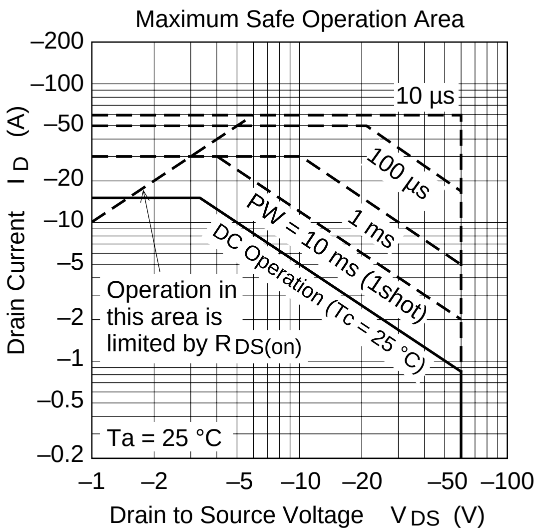
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

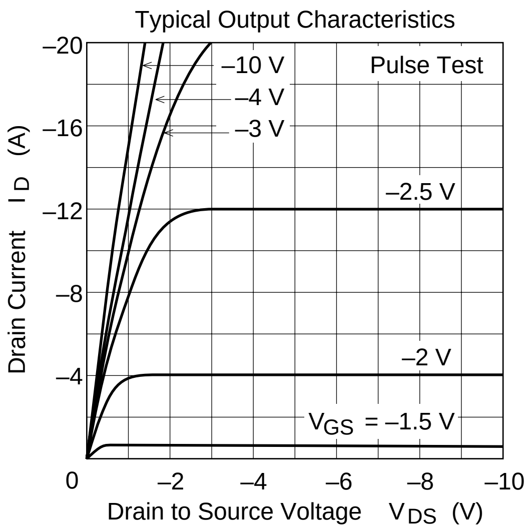
Table 2 Electrical Characteristics (Ta = 25°C)

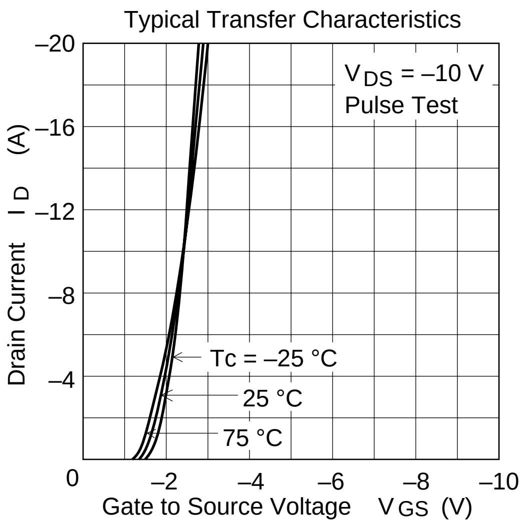
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.07	0.01	Ω	I_D = –8 A V_{GS} = –10 V *
		—	0.12	0.19	Ω	I_D = –3 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	8	14	—	S	I_D = –8 A V_{DS} = –10 V *
Input capacitance	Ciss	—	2170	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	830	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	130	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	16	—	ns	I_D = –8 A
Rise time	t_r	—	75	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	360	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	180	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = –15 A, V_{GS} = 0, diF / dt = 50 A / µs

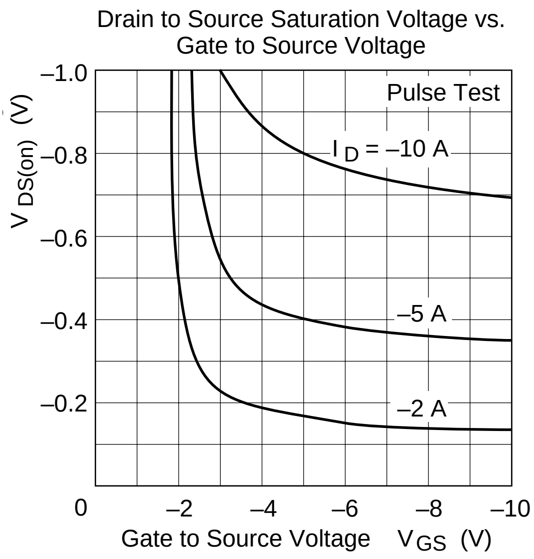
* Pulse Test

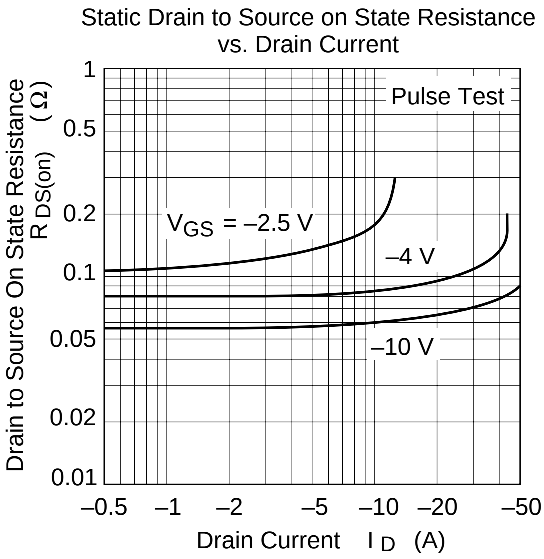

Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)

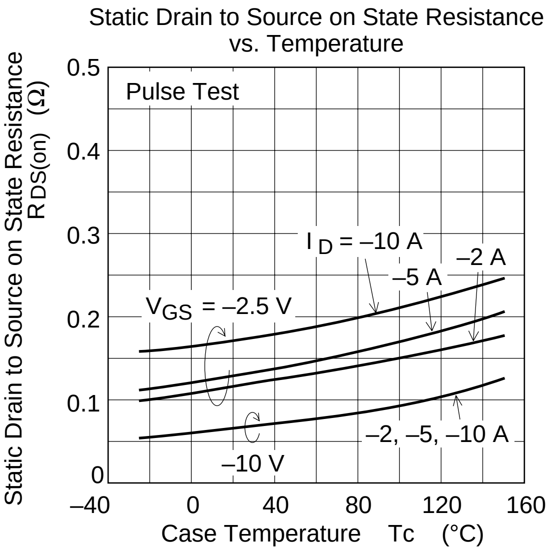

Maximum Safe Operation Area
Drain Current I D (A)
–200
–100
–50
–20
–10
–5
–2
–1
–0.5
–0.2
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
–1
–2
–5
–10
–20
–50
–100
Drain to Source Voltage V DS (V)

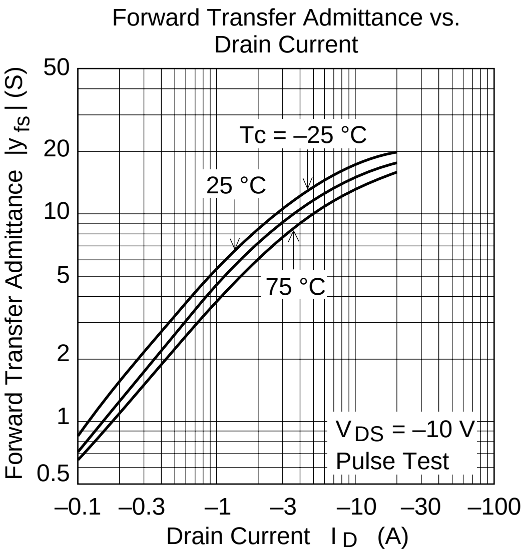

Typical Output Characteristics
Drain Current I D (A)
–20
–16
–12
–8
–4
0
–10 V
–4 V
–3 V
Pulse Test
–2.5 V
–2 V
VGS = –1.5 V
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
–20
–16
–12
–8
–4
0
V DS = –10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

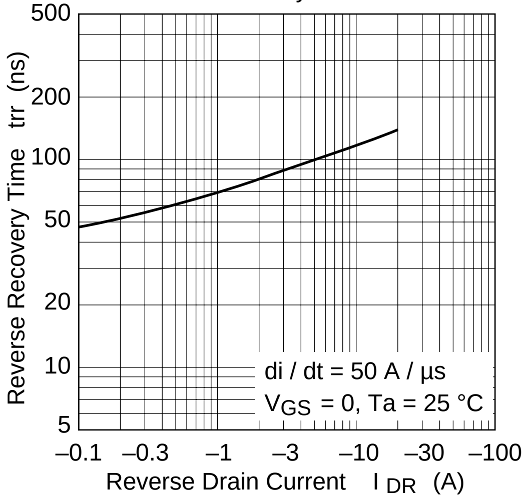

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –10 A
–5 A
–2 A
V DS(on) (V)
–1.0
–0.8
–0.6
–0.4
–0.2
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)


Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –2.5 V
–4 V
–10 V
Drain to Source On State Resistance
R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.5
–1
–2
–5
–10
–20
–50
Drain Current I D (A)

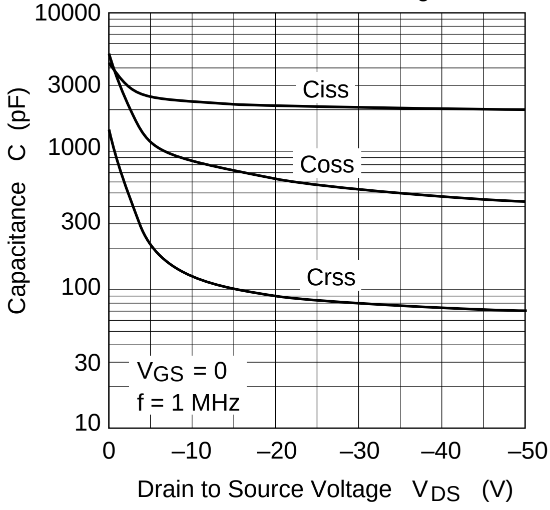

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –10 A
–5 A
–2 A
V GS = –2.5 V
–2, –5, –10 A
–10 V
Static Drain to Source on State Resistance
R DS(on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs | (S)
50
20
10
5
2
1
0.5
–0.1
–0.3
–1
–3
–10
–30
–100
Drain Current I D (A)

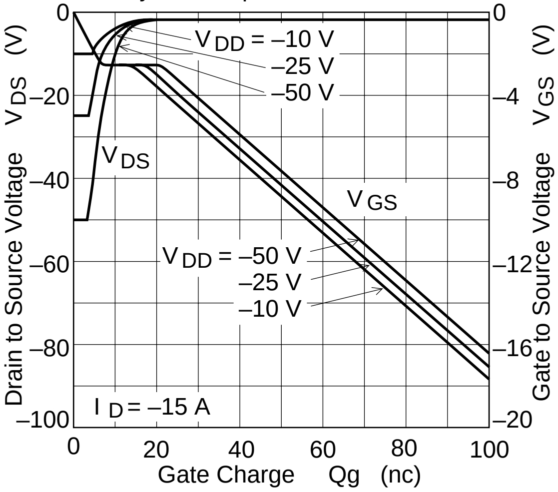
Body–Drain Diode Reverse Recovery Time



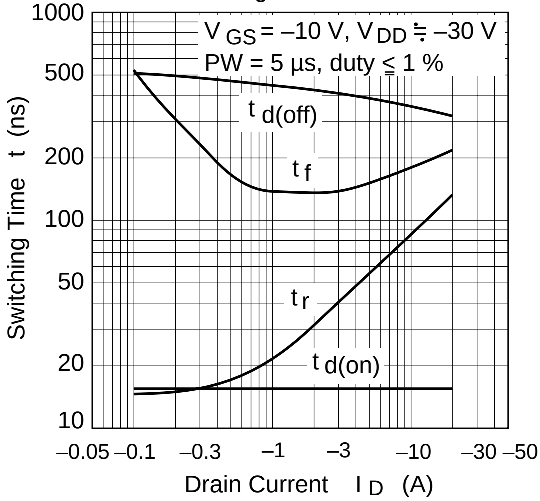
Typical Capacitance vs. Drain to Source Voltage



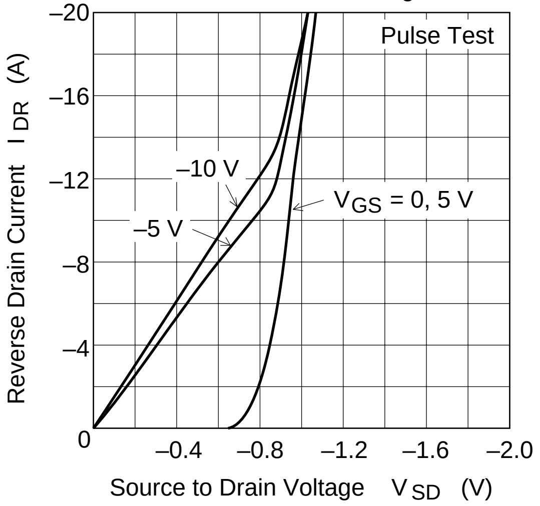
Dynamic Input Characteristics



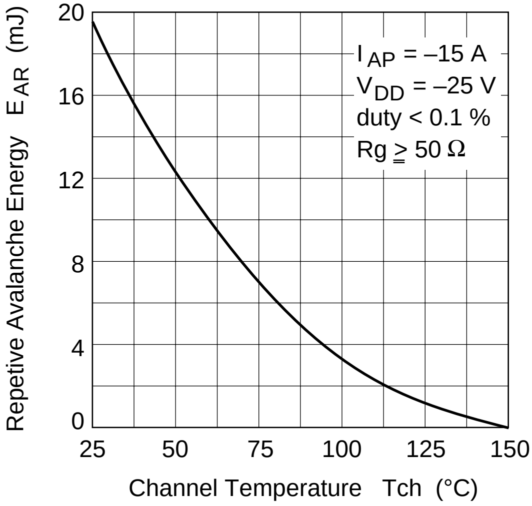
Switching Characteristics



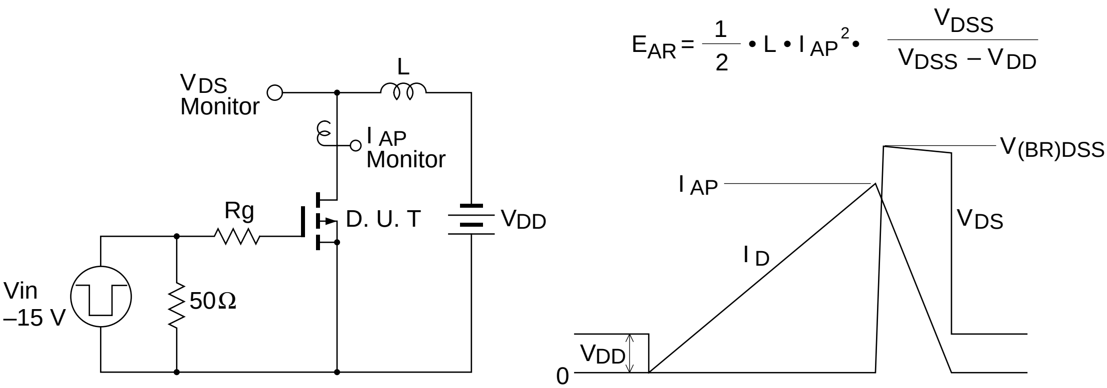
Reverse Drain Current vs.
Source to Drain Voltage

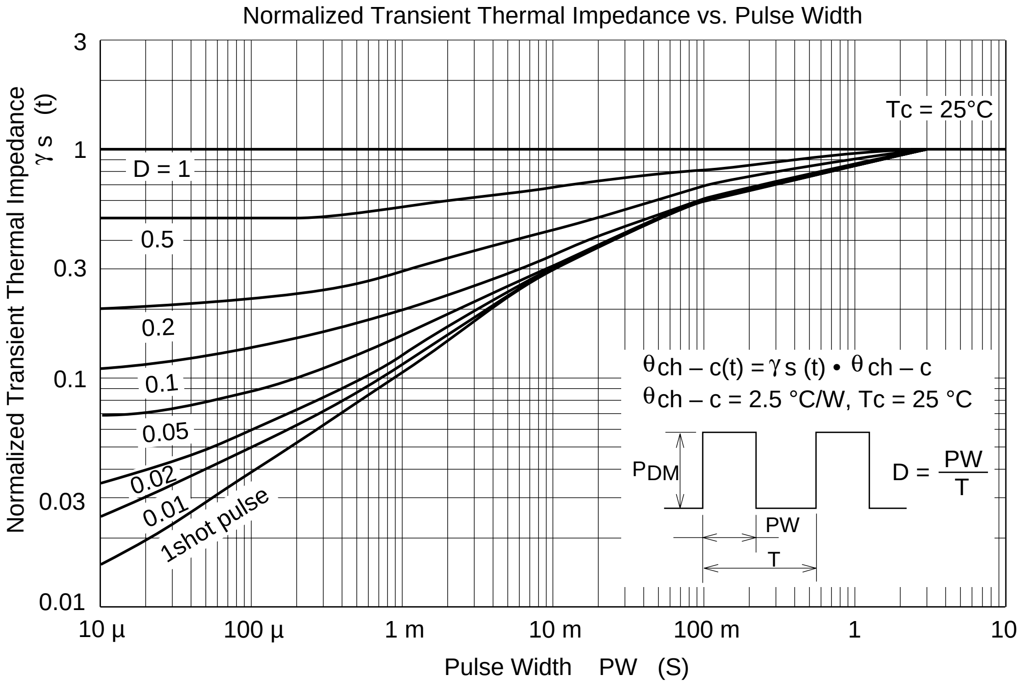


Maximun Avalanche Energy vs.
Channel Temperature Derating

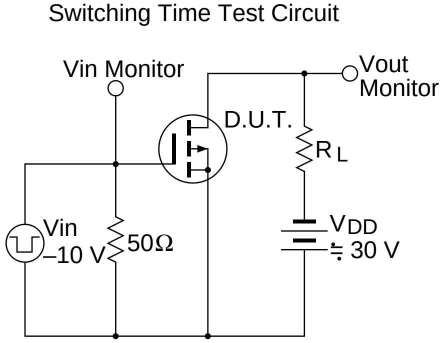


Avalanche Test Circuit and Waveform

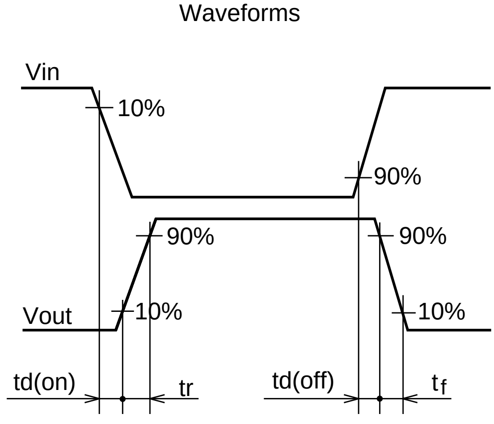




Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 2.5 °C/W, Tc = 25 °C
PDM
D = PW/T
PW
T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)



Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T.
RL
Vin –10 V
50Ω
VDD ≒ 30 V



Waveforms
Vin
10%
90%
90%
90%
Vout
10%
10%
td(on)
tr
td(off)
tf

2SJ386

Silicon P Channel MOS FET

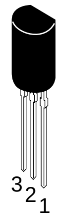
Application

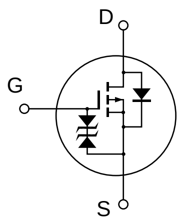
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

TO-92Mod.





1. Gate
2. Drain
3. Source

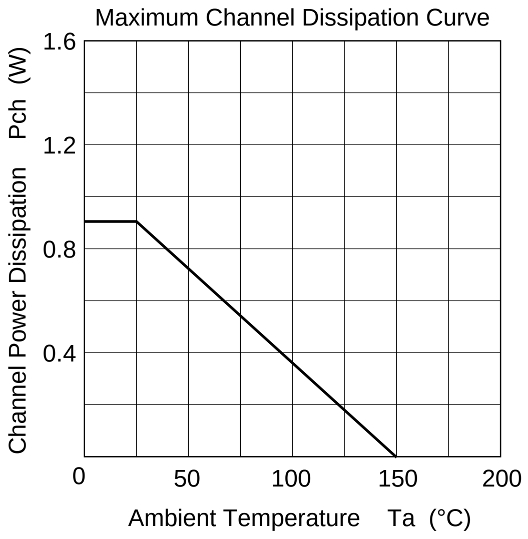
Table 1 Absolute Maximum Ratings (Ta = 25°C)

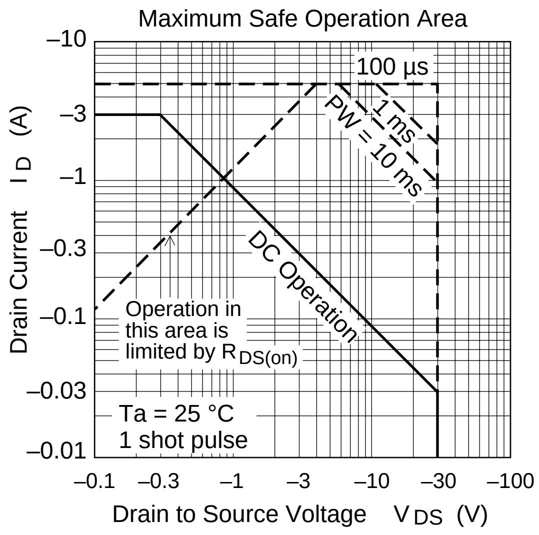
Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–3	A
Drain peak current	$I_{D(pulse)}$*	–5	A
Body–drain diode reverse drain current	I_{DR}	–3	A
Channel dissipation	Pch	0.9	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

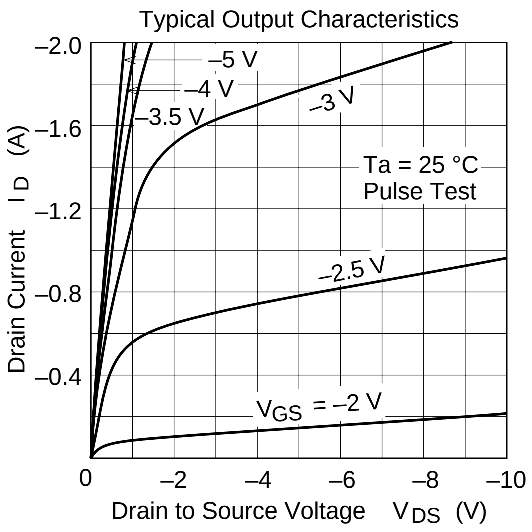
* PW ≤ 10 µs, duty cycle ≤ 1 %

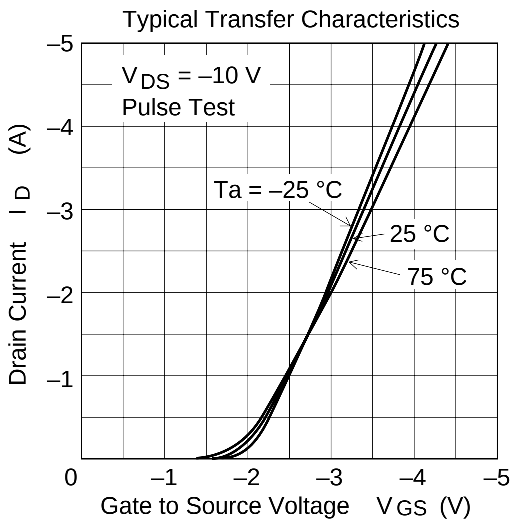
Table 2 Electrical Characteristics (Ta = 25°C)

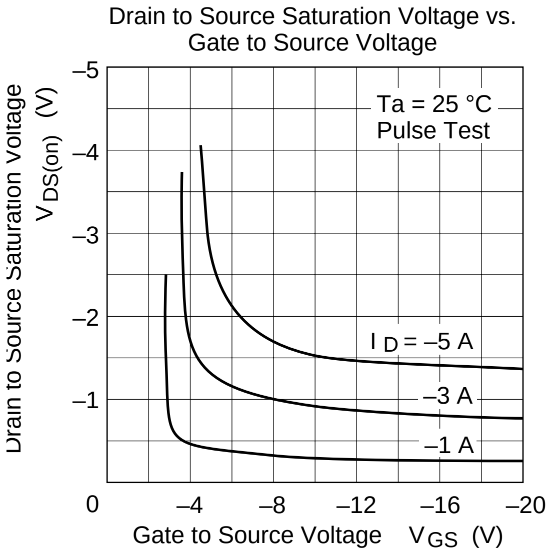
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –24 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.4	Ω	I_D = –2 A V_{GS} = –10 V *
		—	0.55	0.8	Ω	I_D = –2 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	1.0	1.7	—	S	I_D = –1 A V_{DS} = –10 V *
Input capacitance	Ciss	—	177	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	120	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	59	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = –2 A
Rise time	t_r	—	28	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	45	—	ns	R_L = 15 Ω
Fall time	t_f	—	60	—	ns	

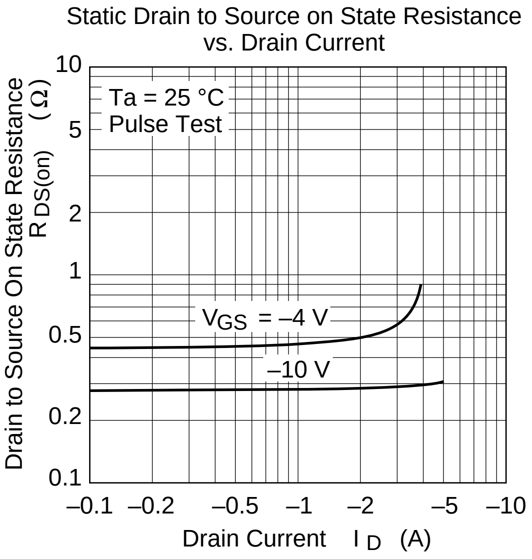

Maximum Channel Dissipation Curve
Channel Power Dissipation Pch (W)
1.6
1.2
0.8
0.4
0
50
100
150
200
Ambient Temperature Ta (°C)

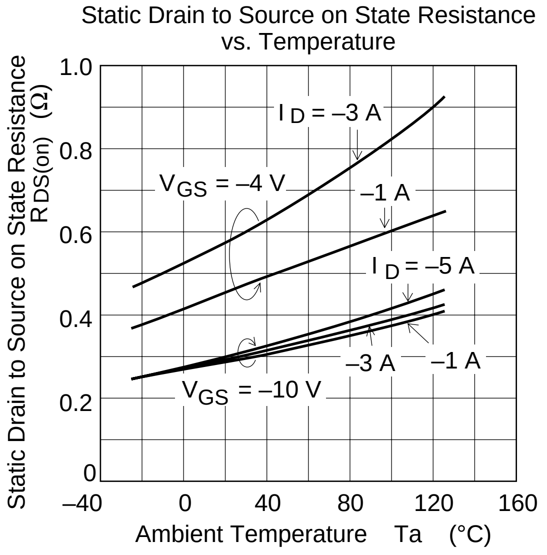

Maximum Safe Operation Area
Drain Current I D (A)
–10
–3
–1
–0.3
–0.1
–0.03
–0.01
100 μs
1 ms
PW = 10 ms
DC Operation
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1 shot pulse
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

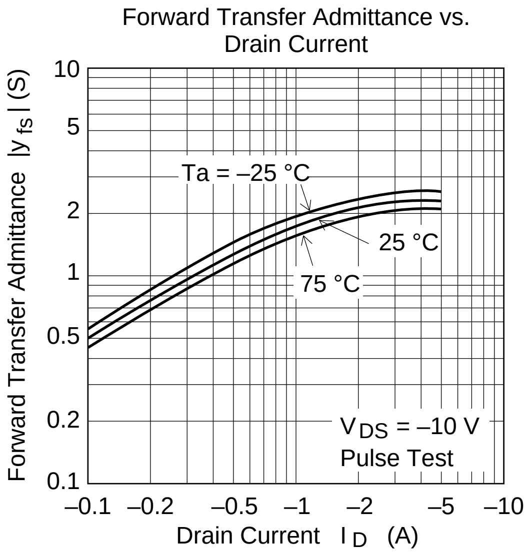

Typical Output Characteristics
Drain Current I D (A)
–2.0
–1.6
–1.2
–0.8
–0.4
–5 V
–4 V
–3.5 V
–3 V
Ta = 25 °C
Pulse Test
–2.5 V
V GS = –2 V
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)

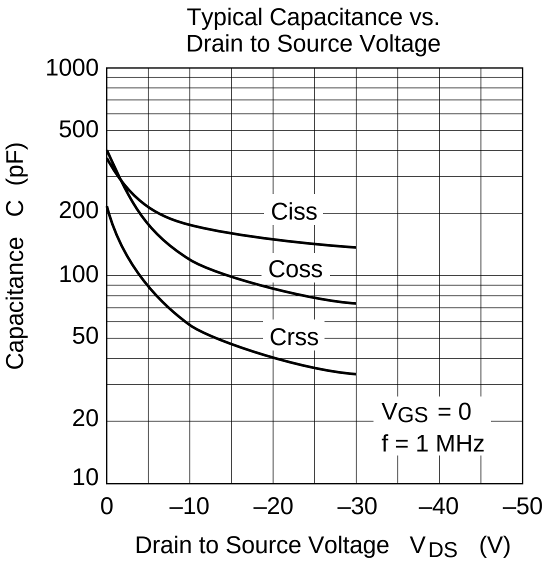

Typical Transfer Characteristics
Drain Current I D (A)
–5
–4
–3
–2
–1
V DS = –10 V
Pulse Test
Ta = –25 °C
25 °C
75 °C
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

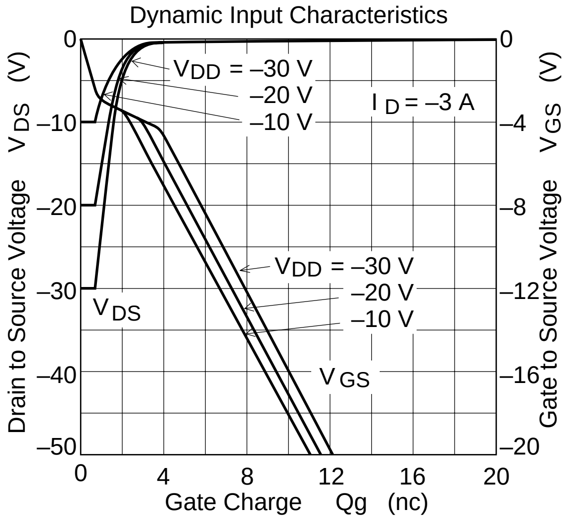

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Ta = 25 °C
Pulse Test
I D = –5 A
–3 A
–1 A
Drain to Source Saturation Voltage V DS(on) (V)
–5
–4
–3
–2
–1
0
–4
–8
–12
–16
–20
Gate to Source Voltage V GS (V)

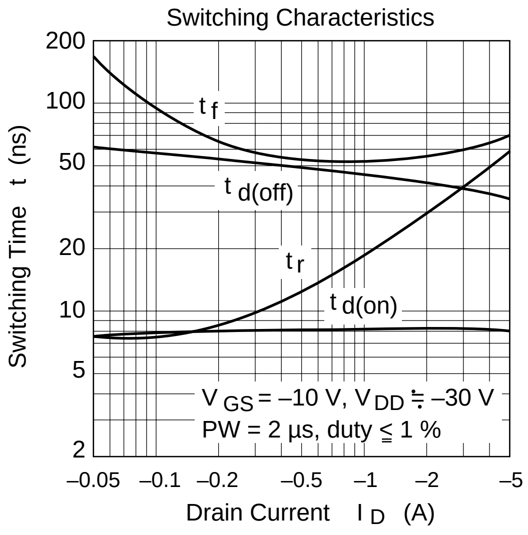

Static Drain to Source on State Resistance
vs. Drain Current
Ta = 25 °C
Pulse Test
V GS = –4 V
–10 V
Drain to Source On State Resistance R DS(on) (Ω)
10
5
2
1
0.5
0.2
0.1
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

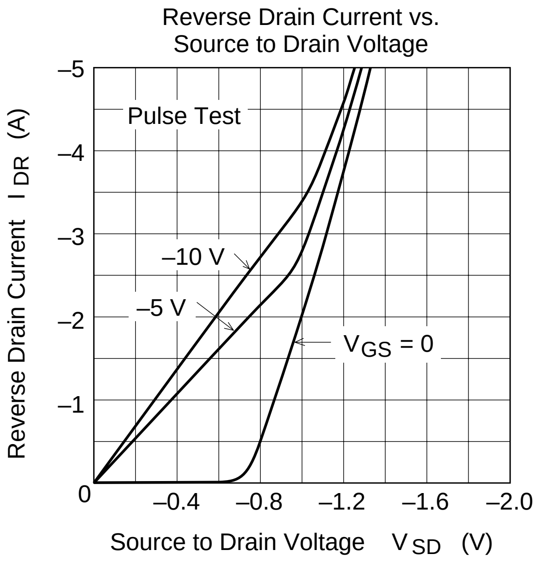

Static Drain to Source on State Resistance
vs. Temperature
I D = –3 A
V GS = –4 V
–1 A
I D = –5 A
–3 A
–1 A
V GS = –10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160
Ambient Temperature Ta (°C)


Forward Transfer Admittance vs.
Drain Current
Ta = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs| (S)
10
5
2
1
0.5
0.2
0.1
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
1000
500
200
100
50
20
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
VDD = –30 V
–20 V
–10 V
ID = –3 A
VDS
VGS
VDD = –30 V
–20 V
–10 V
0
–10
–20
–30
–40
–50
0
–4
–8
–12
–16
–20
0
4
8
12
16
20
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
200
100
50
20
10
5
2
tf
td(off)
tr
td(on)
VGS = –10 V, VDD ≒ –30 V
PW = 2 µs, duty ≦ 1 %
–0.05
–0.1
–0.2
–0.5
–1
–2
–5
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current IDR (A)
–5
–4
–3
–2
–1
0
Pulse Test
–10 V
–5 V
VGS = 0
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage VSD (V)

2SJ387(L), 2SJ387(S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- Low drive current
- 2.5 V Gate drive device can be driven from 3 V Source
- Suitable for Switching regulator, DC – DC converter

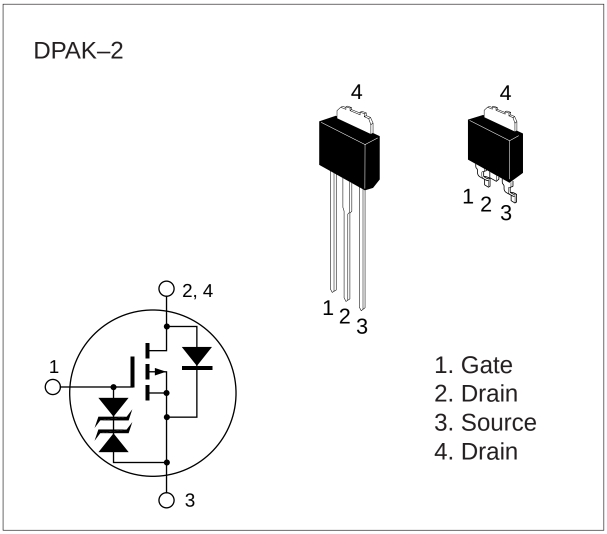


Table 1 Absolute Maximum Ratings (Ta = 25°C)

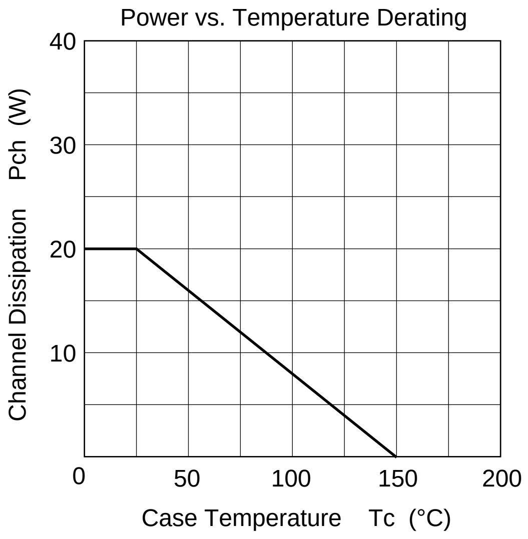
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–10	A
Drain peak current	$I_{D(pulse)}$*	–40	A
Body–drain diode reverse drain current	I_{DR}	–10	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

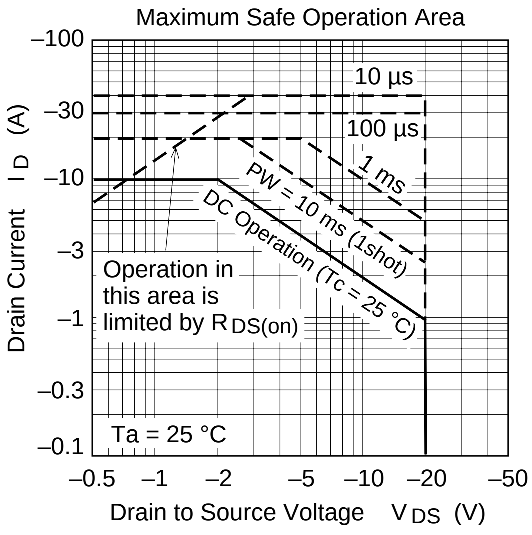
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C

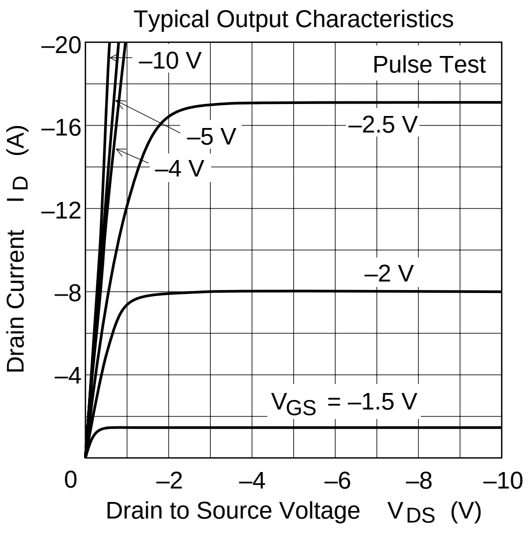
Table 2 Electrical Characteristics (Ta = 25°C)

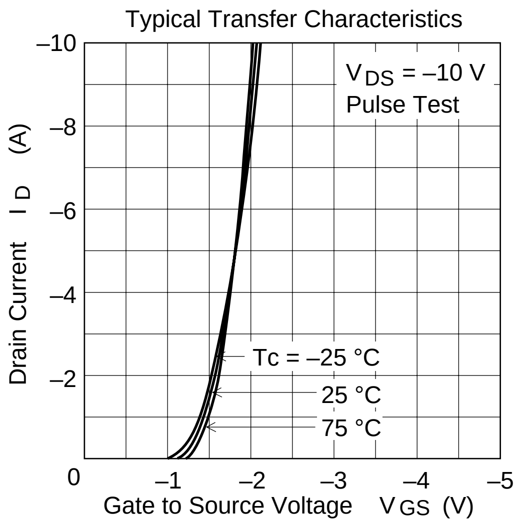
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.07	Ω	I_D = –5 A V_{GS} = –4 V *
		—	0.07	0.1	Ω	I_D = –5 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = –5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1170	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	860	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	310	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = –5 A
Rise time	t_r	—	325	—	ns	V_{GS} = –4 V
Turn–off delay time	$t_{d(off)}$	—	350	—	ns	R_L = 2 Ω
Fall time	t_f	—	425	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	240	—	µs	I_F = –10 A, V_{GS} = 0, diF / dt = 20 A / µs

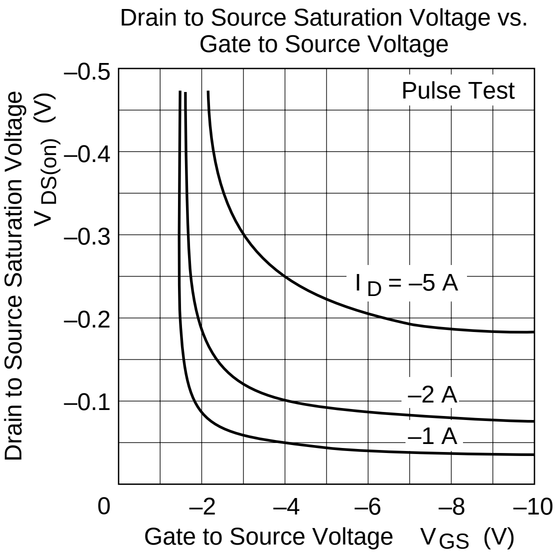
* Pulse Test

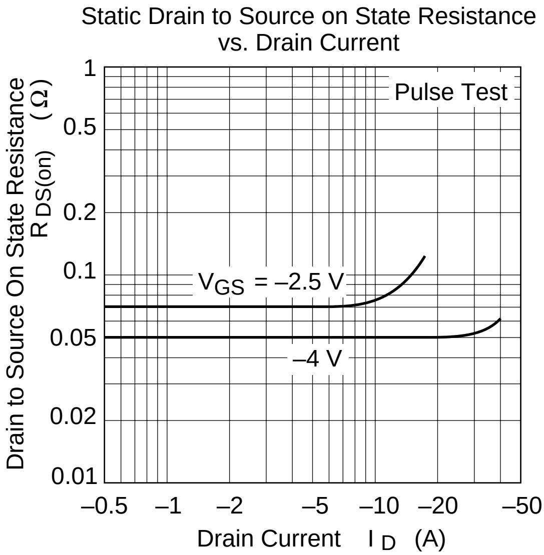

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

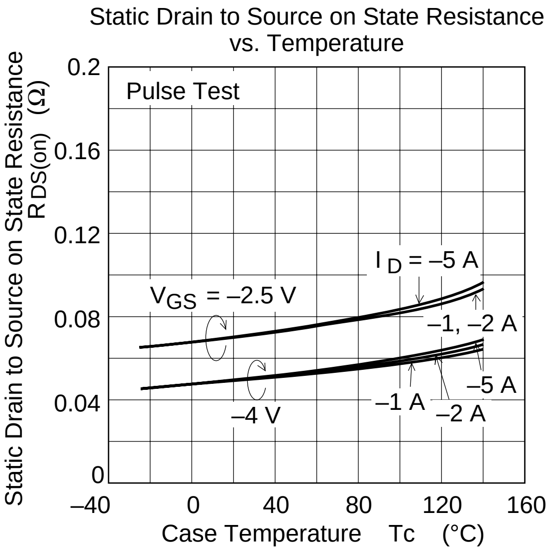

Maximum Safe Operation Area
–100
–30
–10
–3
–1
–0.3
–0.1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
Drain Current I D (A)
–0.5
–1
–2
–5
–10
–20
–50
Drain to Source Voltage V DS (V)

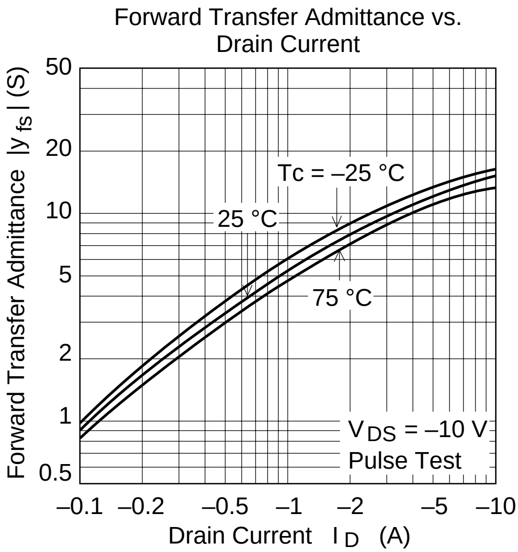

Typical Output Characteristics
–20
–16
–12
–8
–4
0
–10 V
–5 V
–4 V
Pulse Test
–2.5 V
–2 V
VGS = –1.5 V
Drain Current I D (A)
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)

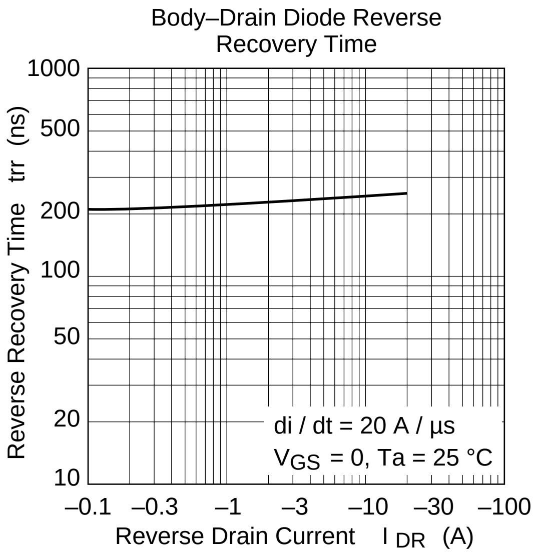

Typical Transfer Characteristics
–10
–8
–6
–4
–2
0
V DS = –10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
Drain Current I D (A)
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

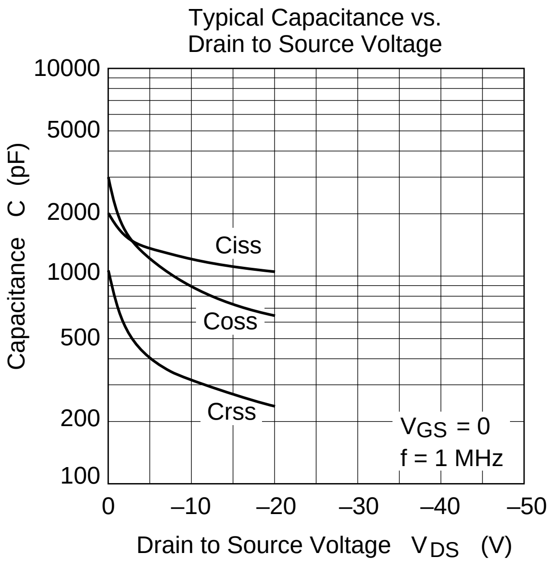

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –5 A
–2 A
–1 A
Drain to Source Saturation Voltage
V DS(on) (V)
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

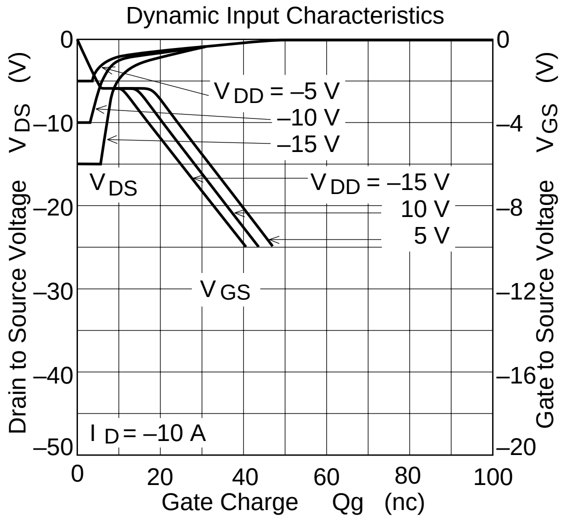

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –2.5 V
–4 V
Drain to Source On State Resistance
R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.5
–1
–2
–5
–10
–20
–50
Drain Current I D (A)

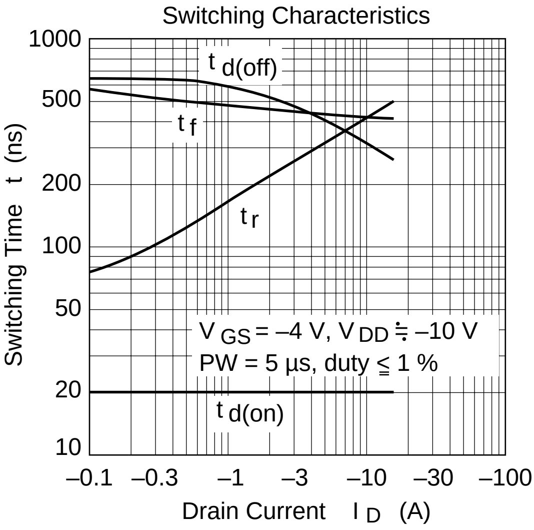

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –5 A
V GS = –2.5 V
–1, –2 A
–5 A
–1 A
–2 A
–4 V
Static Drain to Source on State Resistance
R DS(on) (Ω)
0.2
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

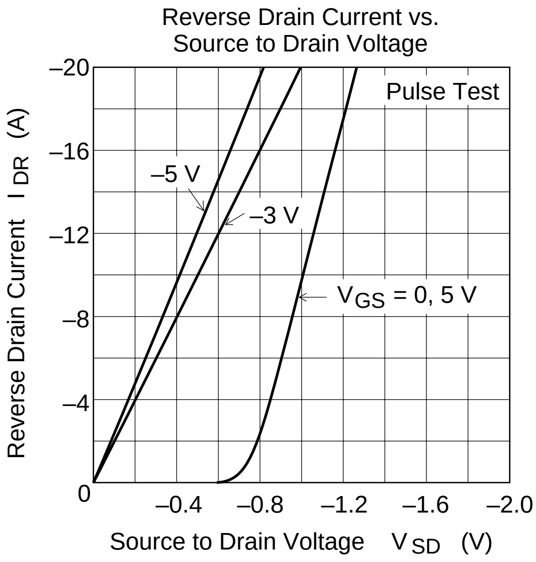

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs| (S)
50
20
10
5
2
1
0.5
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

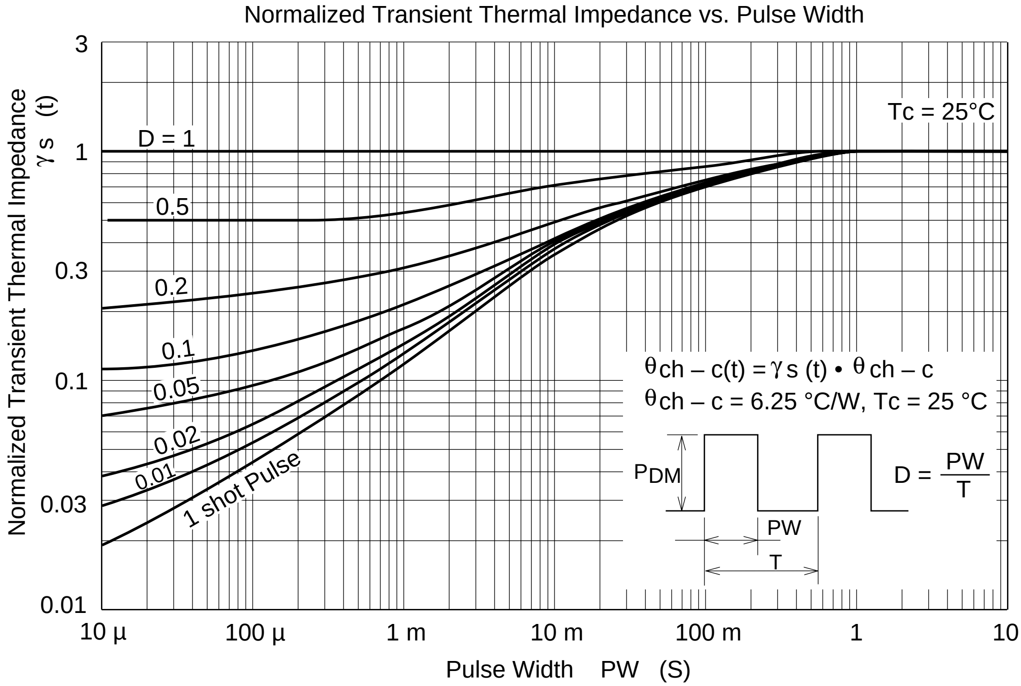

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.1
–0.3
–1
–3
–10
–30
–100
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
5000
2000
1000
500
200
100
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)

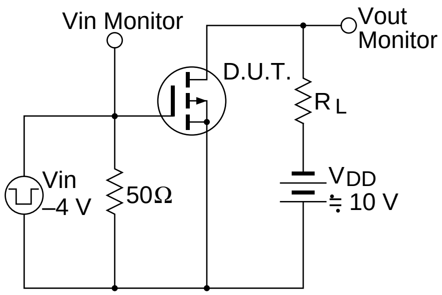

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–10
–20
–30
–40
–50
VDD = –5 V
–10 V
–15 V
VDS
VDD = –15 V
10 V
5 V
VGS
I D = –10 A
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
t d(off)
t f
t r
V GS = –4 V, V DD ≒ –10 V
PW = 5 µs, duty ≦ 1 %
t d(on)
–0.1
–0.3
–1
–3
–10
–30
–100
Drain Current I D (A)

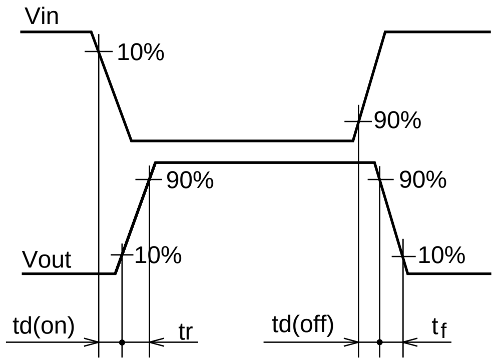

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
–5 V
–3 V
VGS = 0, 5 V
Reverse Drain Current I DR (A)
–20
–16
–12
–8
–4
0
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage V SD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Switching Time Test Circuit



Waveforms



2SJ388(L), 2SJ388(S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V Gate drive device can be driven from 3 V Source
- Suitable for Switching regulator, DC – DC converter

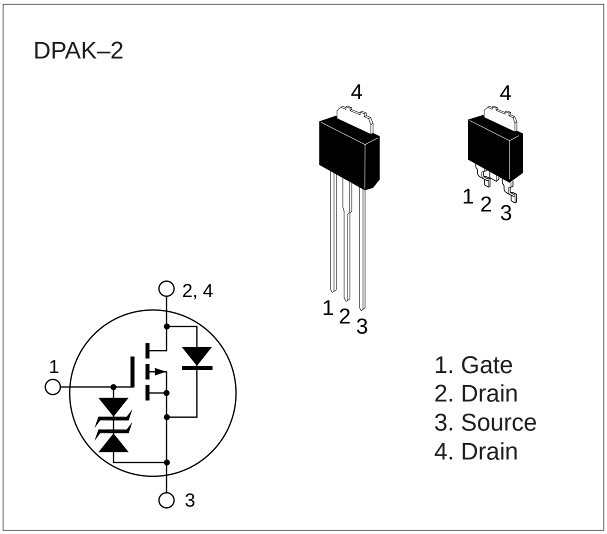


Table 1 Absolute Maximum Ratings (Ta = 25°C)

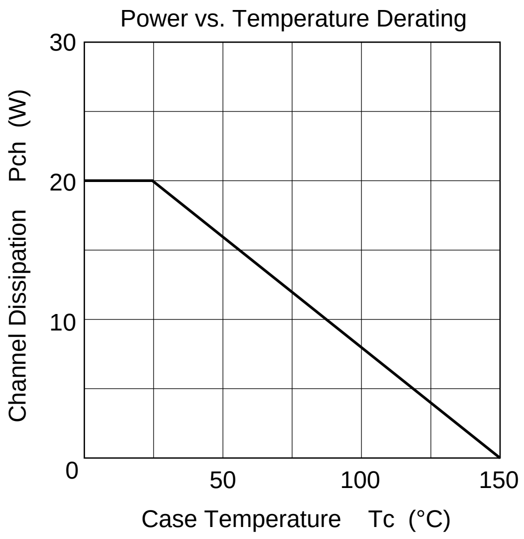
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–10	A
Drain peak current	$I_{D(pulse)}$*	–40	A
Body–drain diode reverse drain current	I_{DR}	–10	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.08	Ω	I_D = –5 A V_{GS} = –10 V *
		—	0.12	0.2	Ω	I_D = –5 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	4.5	8	—	S	I_D = –5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	970	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	620	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	250	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = –5 A
Rise time	t_r	—	65	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	250	—	ns	R_L = 6 Ω
Fall time	t_f	—	240	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	85	—	µs	I_F = –10 A, V_{GS} = 0, diF / dt = 20 A / µs

* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature Tc (°C)

2SJ389(L), 2SJ389(S)

Silicon P Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

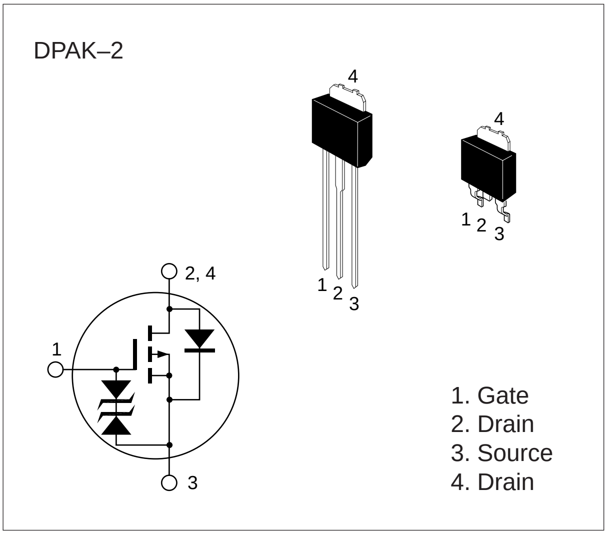


Table 1 Absolute Maximum Ratings (Ta = 25°C)

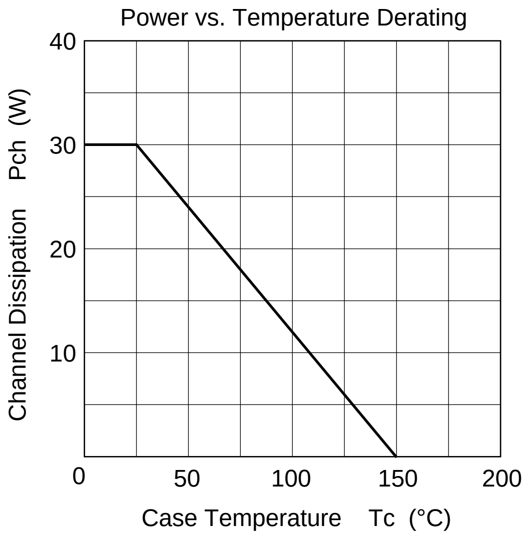
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–10	A
Drain peak current	$I_{D(pulse)}$*	–40	A
Body–drain diode reverse drain current	I_{DR}	–10	A
Avalanche current	I_{AP}***	–10	A
Avalanche energy	E_{AR}***	8.5	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

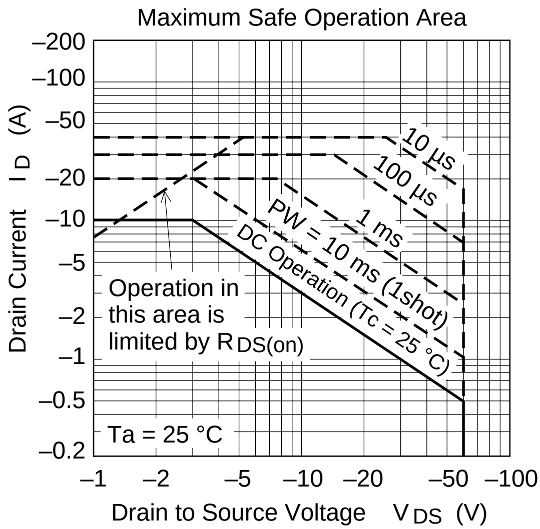
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

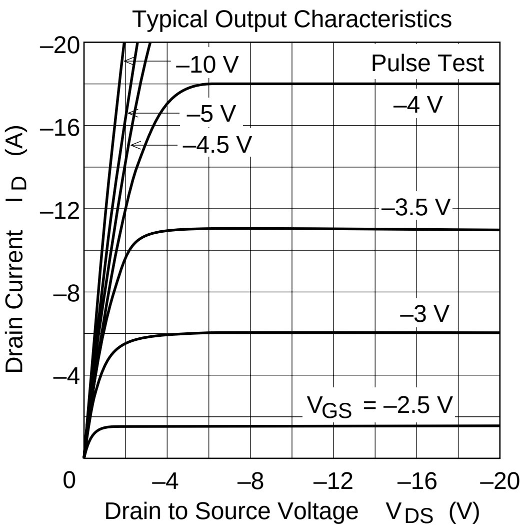
Table 2 Electrical Characteristics (Ta = 25°C)

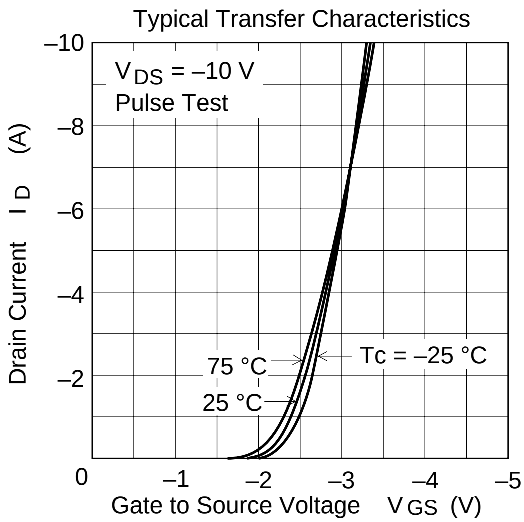
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.135	Ω	I_D = –5 A V_{GS} = –10 V *
		—	0.14	0.2	Ω	I_D = –5 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	4	8	—	S	I_D = –5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	910	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	170	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = –5 A
Rise time	t_r	—	85	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	220	—	ns	R_L = 6 Ω
Fall time	t_f	—	145	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	170	—	µs	I_F = –10 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

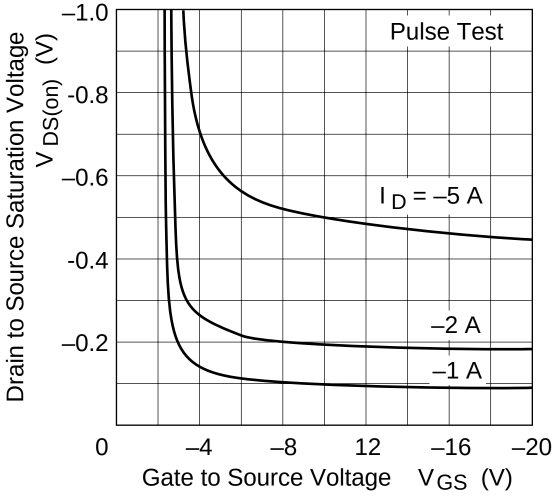

Power vs. Temperature Derating
40
30
20
10
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
–200
–100
–50
–20
–10
–5
–2
–1
–0.5
–0.2
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
–1
–2
–5
–10
–20
–50
–100
Drain Current I D (A)
Drain to Source Voltage V DS (V)

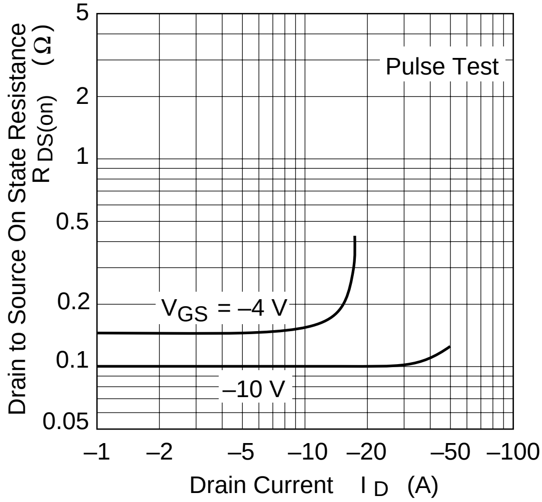

Typical Output Characteristics
–20
–16
–12
–8
–4
0
–10 V
–5 V
–4.5 V
Pulse Test
–4 V
–3.5 V
–3 V
VGS = –2.5 V
–4
–8
–12
–16
–20
Drain Current I D (A)
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
–10
–8
–6
–4
–2
0
VDS = –10 V
Pulse Test
75 °C
25 °C
Tc = –25 °C
–1
–2
–3
–4
–5
Drain Current I D (A)
Gate to Source Voltage V GS (V)

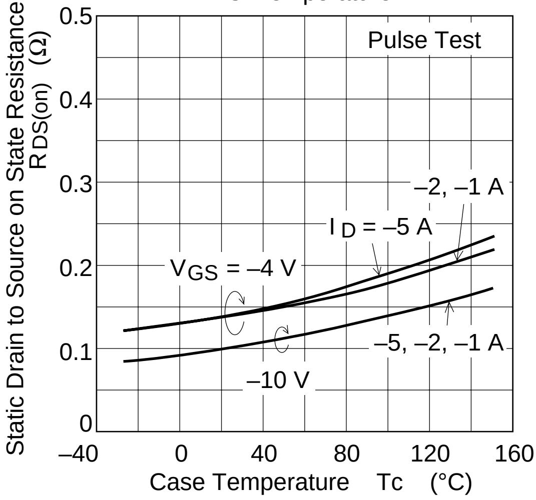
Drain to Source Saturation Voltage vs. Gate to Source Voltage



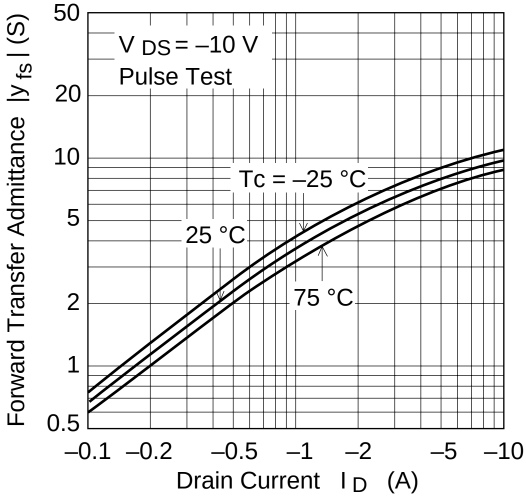
Static Drain to Source on State Resistance vs. Drain Current

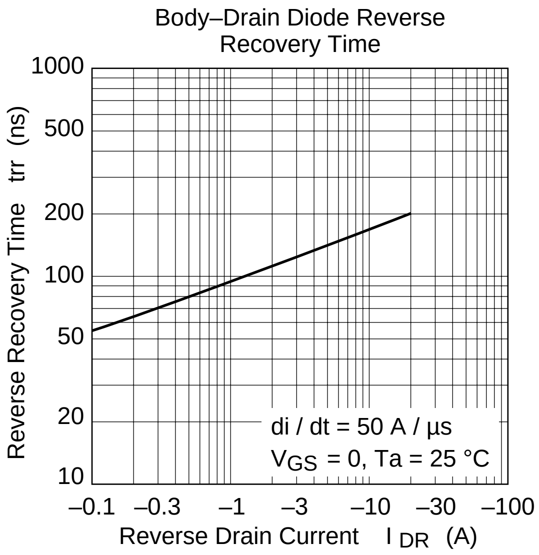


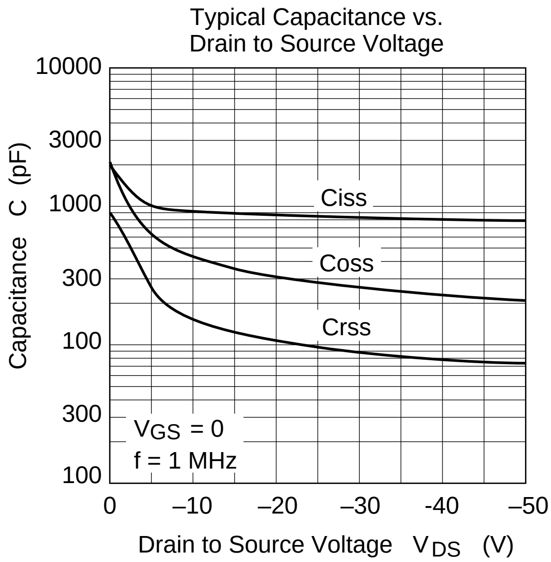
Static Drain to Source on State Resistance vs. Temperature

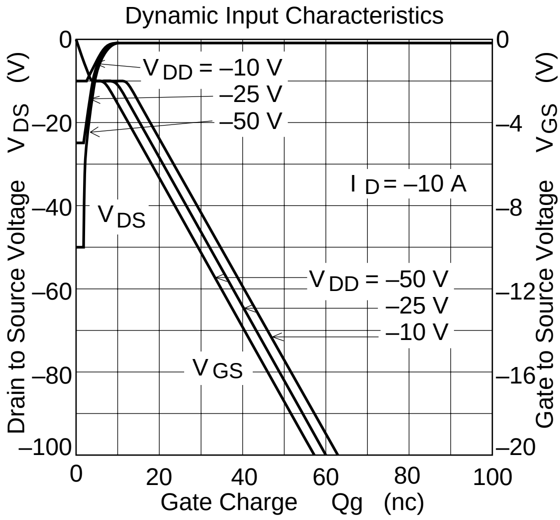


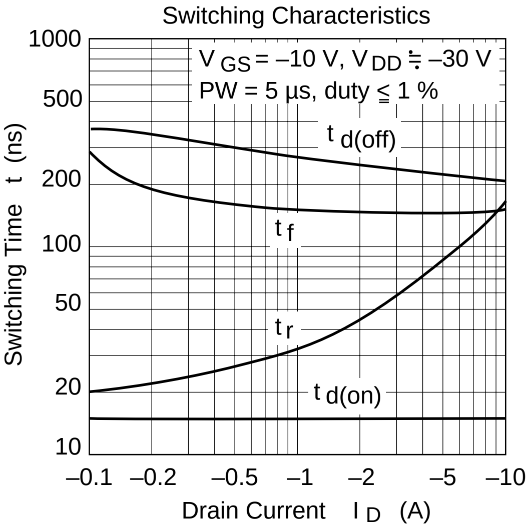
Forward Transfer Admittance vs. Drain Current



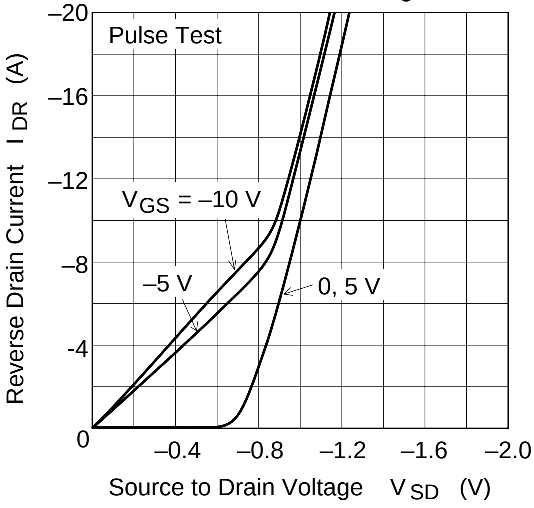

Body–Drain Diode Reverse Recovery Time
1000
500
200
100
50
20
10
Reverse Recovery Time trr (ns)
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.3 –1 –3 –10 –30 –100
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
10000
3000
1000
300
100
300
100
Capacitance C (pF)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 -40 –50
Drain to Source Voltage VDS (V)

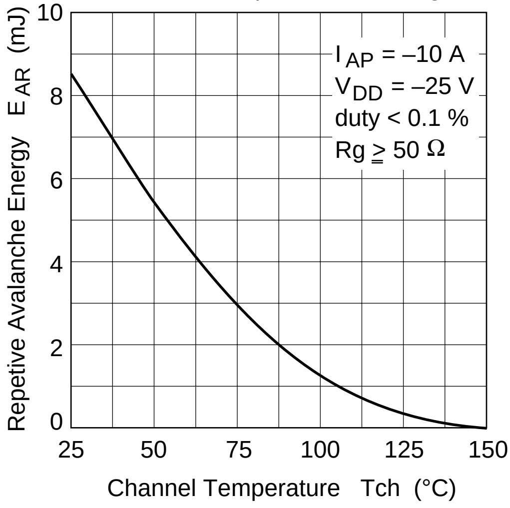

Dynamic Input Characteristics
0
–20
–40
–60
–80
–100
Drain to Source Voltage VDS (V)
V DD = –10 V
–25 V
–50 V
I D = –10 A
VDS
V DD = –50 V
–25 V
–10 V
V GS
0
–4
–8
–12
–16
–20
Gate to Source Voltage VGS (V)
0 20 40 60 80 100
Gate Charge Qg (nc)


Switching Characteristics
1000
500
200
100
50
20
10
Switching Time t (ns)
V GS = –10 V, V DD ≒ –30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)

Reverse Drain Current vs.
Source to Drain Voltage

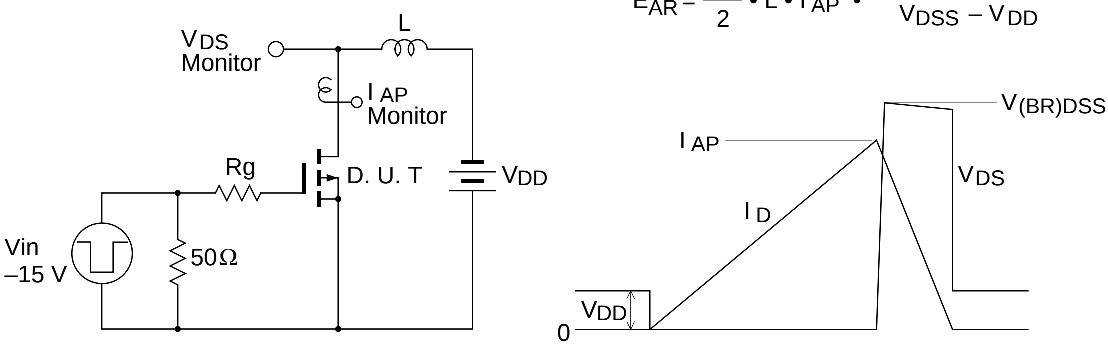


Maximun Avalanche Energy vs.
Channel Temperature Derating

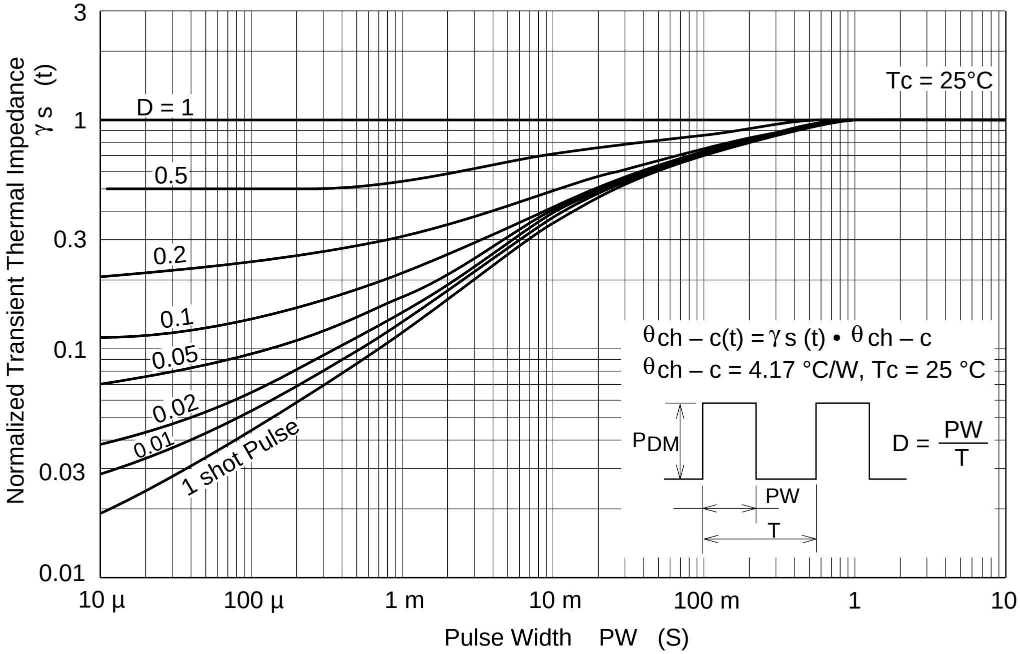


Avalanche Test Circuit and Waveform

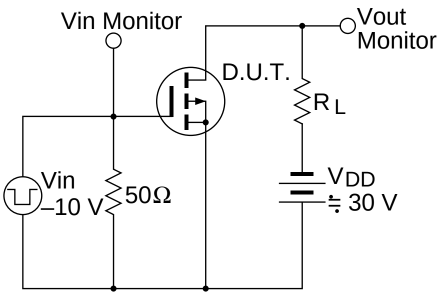
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



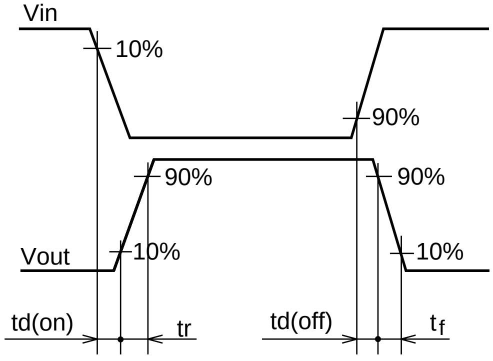
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveforms



2SJ390

Silicon P Channel MOS FET

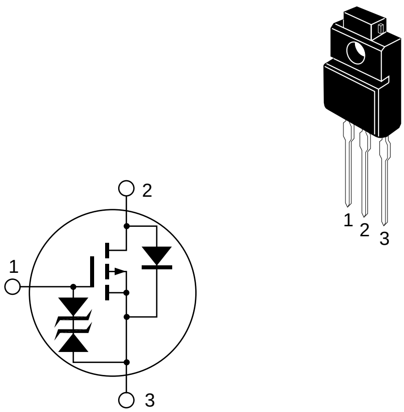
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

TO–220FM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

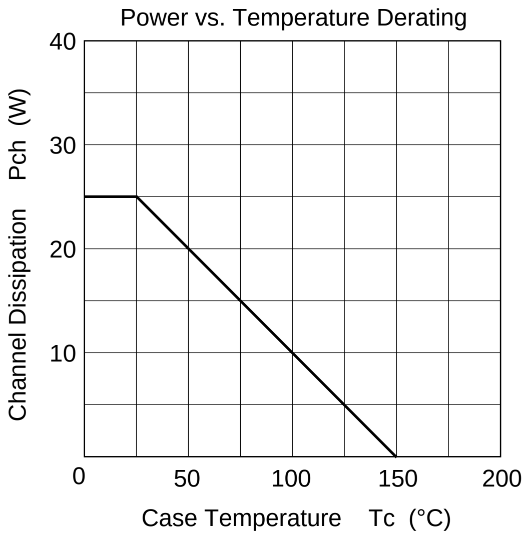
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–10	A
Drain peak current	$I_{D(pulse)}$*	–40	A
Body–drain diode reverse drain current	I_{DR}	–10	A
Avalanche current	I_{AP}***	–10	A
Avalanche energy	E_{AR}***	8.5	mJ
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

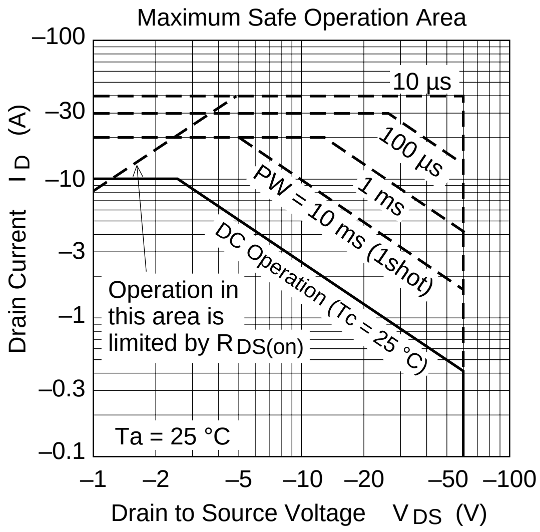
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.09	0.12	Ω	I_D = –5 A V_{GS} = –10 V *
		—	0.13	0.19	Ω	I_D = –5 A V_{GS} = –4 V *
Forward transfer admittance	$\lvert y_{fs} \rvert$	5	9	—	S	I_D = –5 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1060	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	520	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	190	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	13	—	ns	I_D = –5 A
Rise time	t_r	—	65	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	175	—	ns	R_L = 6 Ω
Fall time	t_f	—	110	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = –10 A, V_{GS} = 0, diF / dt = 50 A / µs

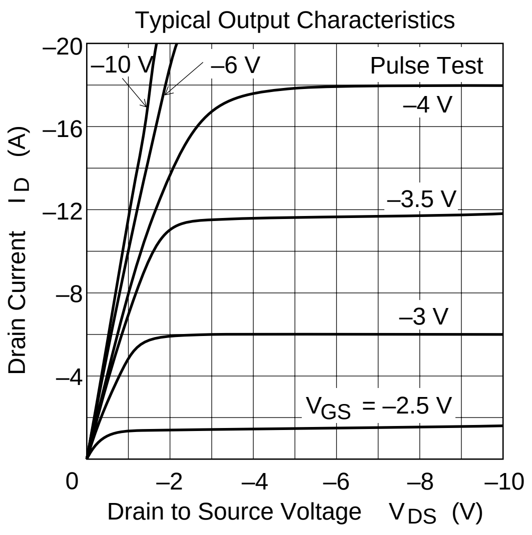
* Pulse Test



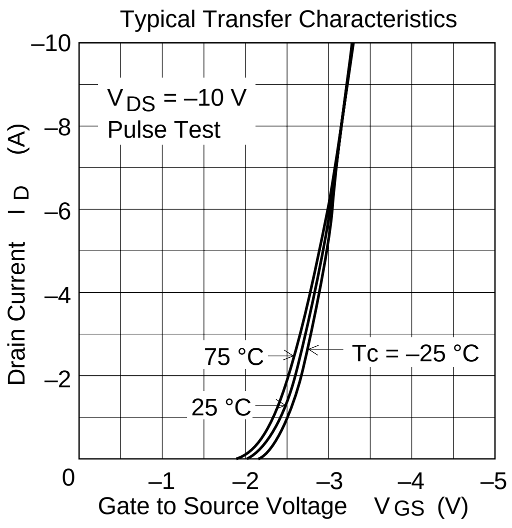
Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)



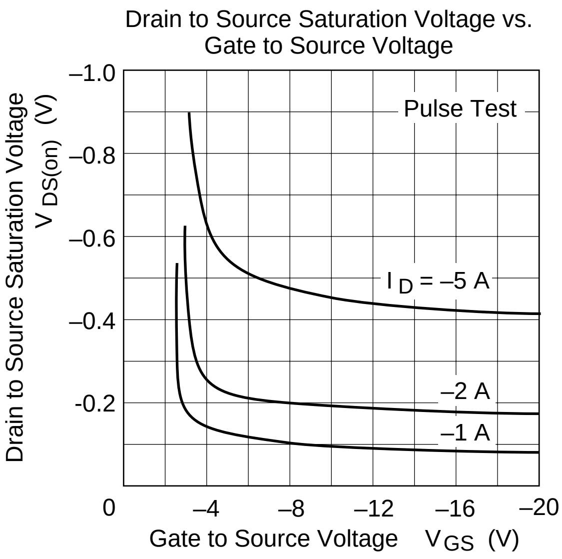
Maximum Safe Operation Area
Drain Current I D (A)
–100
–30
–10
–3
–1
–0.3
–0.1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
–1
–2
–5
–10
–20
–50
–100
Drain to Source Voltage V DS (V)

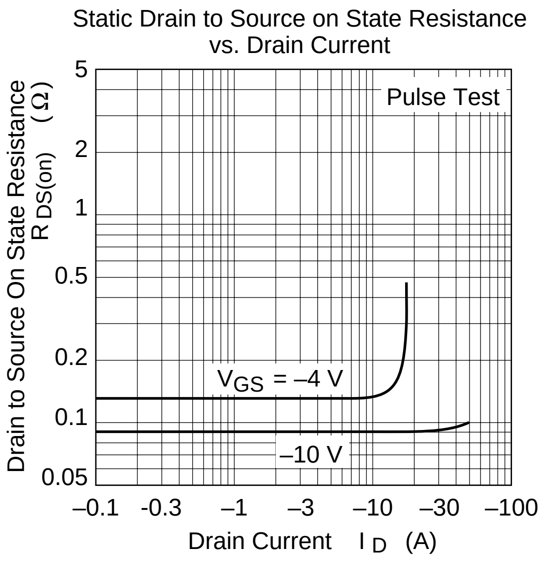


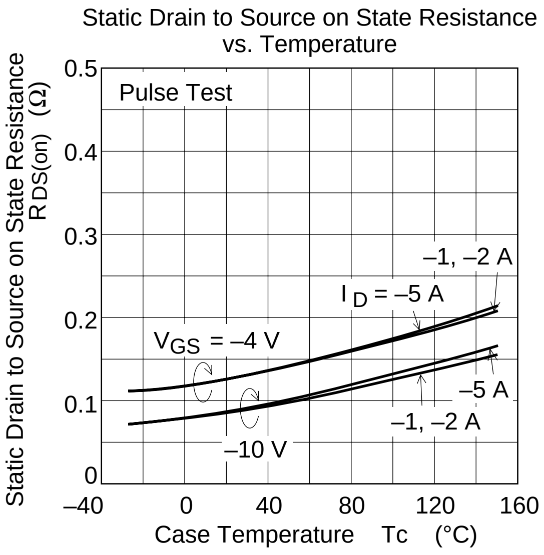
Typical Output Characteristics
Drain Current I D (A)
–20
–16
–12
–8
–4
0
–10 V
–6 V
Pulse Test
–4 V
–3.5 V
–3 V
VGS = –2.5 V
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)

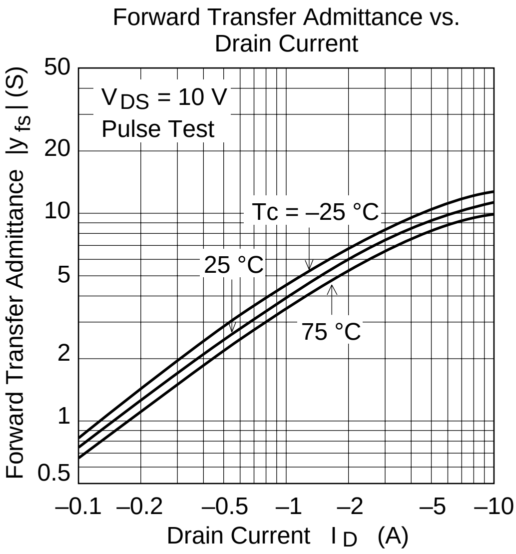


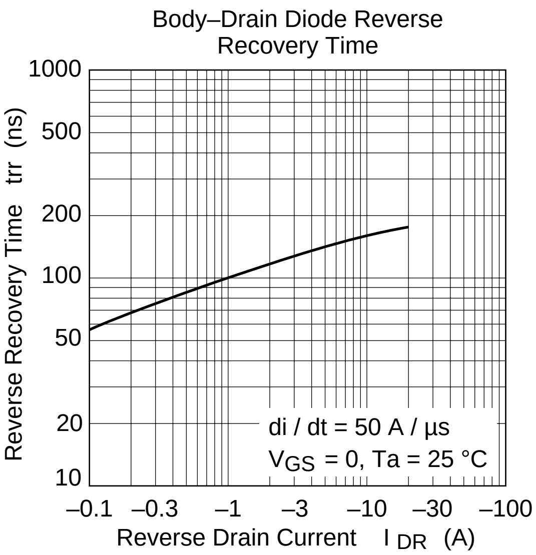
Typical Transfer Characteristics
Drain Current I D (A)
–10
–8
–6
–4
–2
0
V DS = –10 V
Pulse Test
75 °C
Tc = –25 °C
25 °C
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

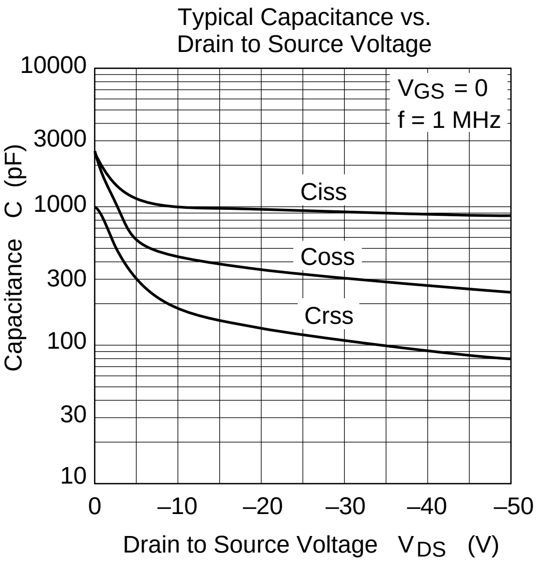

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –5 A
–2 A
–1 A
Drain to Source Saturation Voltage V DS(on) (V)
–1.0
–0.8
–0.6
–0.4
-0.2
0
–4
–8
–12
–16
–20
Gate to Source Voltage V GS (V)

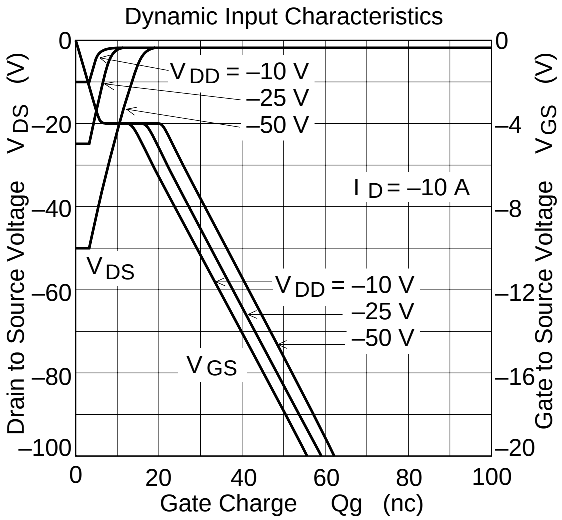

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –4 V
–10 V
Drain to Source On State Resistance R DS(on) (Ω)
5
2
1
0.5
0.2
0.1
0.05
–0.1
-0.3
–1
–3
–10
–30
–100
Drain Current I D (A)

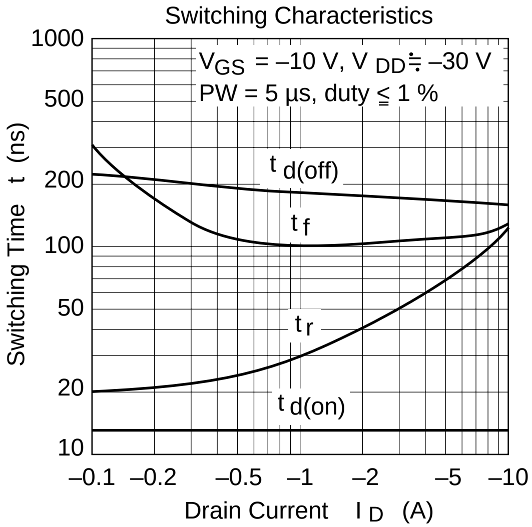

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
–1, –2 A
I D = –5 A
V GS = –4 V
–5 A
–1, –2 A
–10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

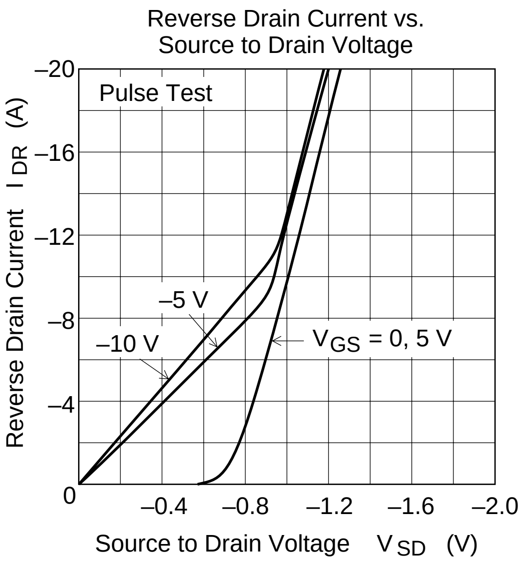

Forward Transfer Admittance vs.
Drain Current
V DS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
Forward Transfer Admittance |y fs | (S)
50
20
10
5
2
1
0.5
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

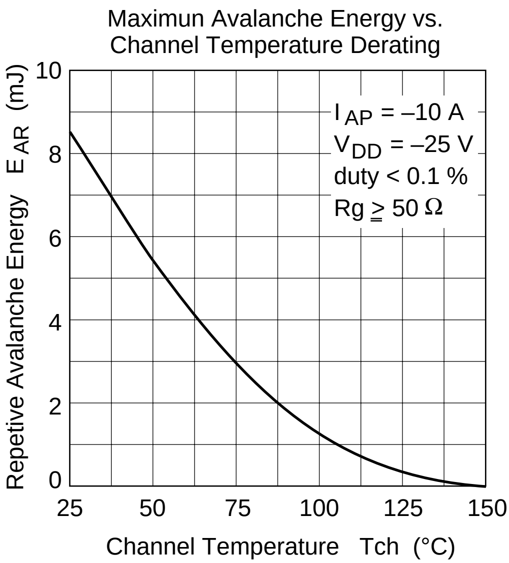

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.3 –1 –3 –10 –30 –100
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0 –10 –20 –30 –40 –50
Drain to Source Voltage VDS (V)

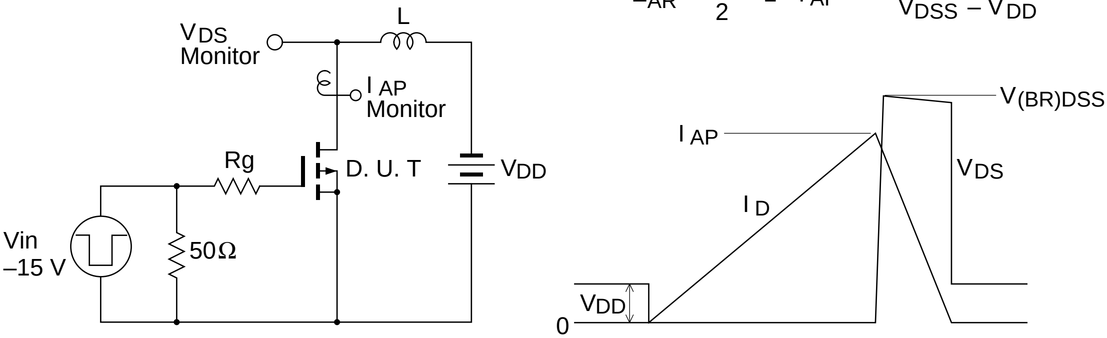

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–20
–40
–60
–80
–100
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
VDD = –10 V
–25 V
–50 V
I D = –10 A
VDS
VDD = –10 V
–25 V
–50 V
VGS
0 20 40 60 80 100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
VGS = –10 V, VDD ≒ –30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)

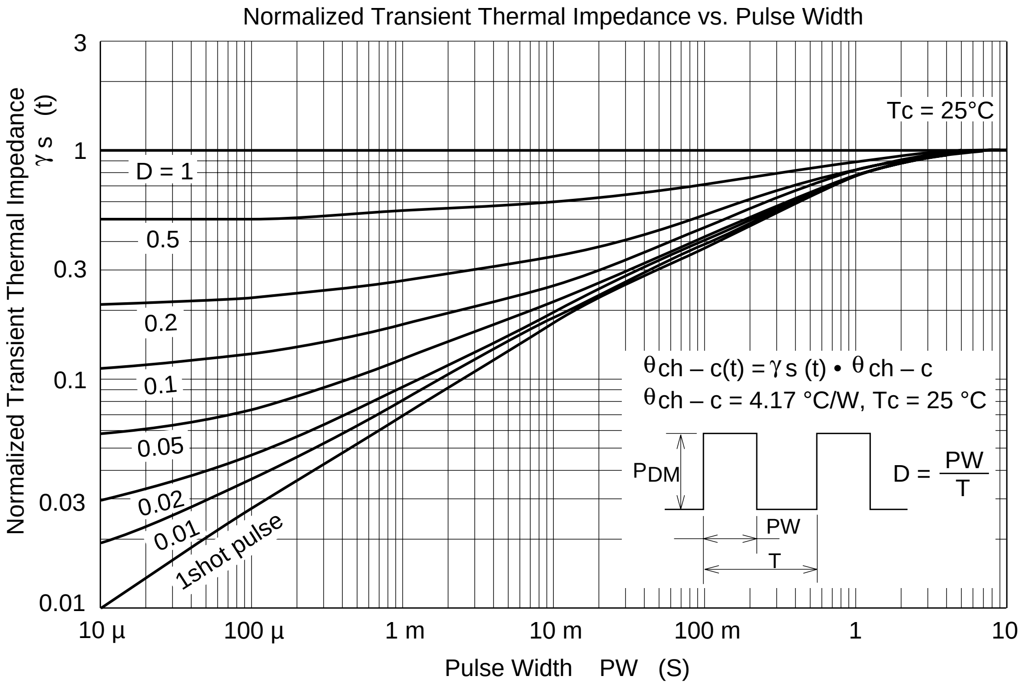




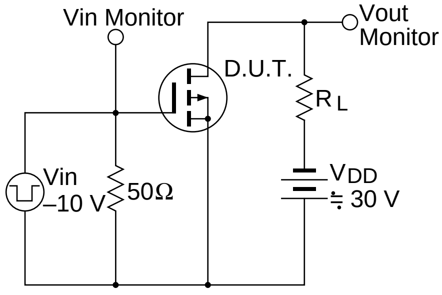
Avalanche Test Circuit and Waveform



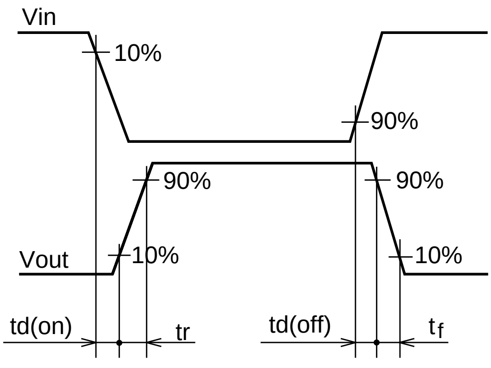
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



Waveforms



2SJ399

Silicon P Channel MOS FET

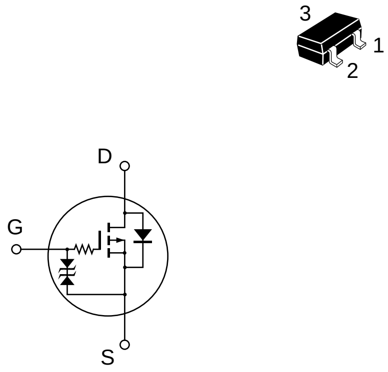
Application

Low frequency power switching

Features

- Low on–resistance
- Small package
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for low signal load switch.

MPAK



1. Source
2. Gate
3. Drain

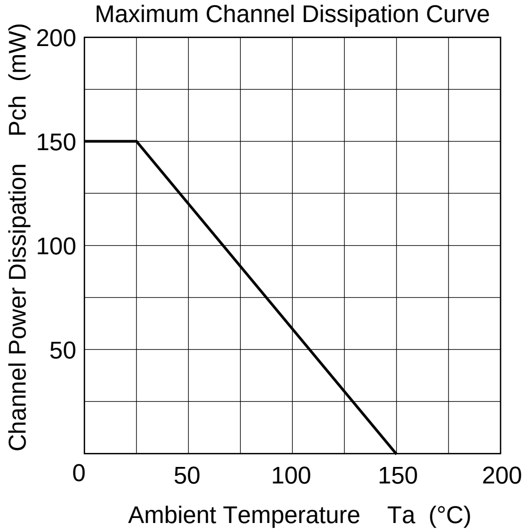
Table 1 Absolute Maximum Ratings (Ta = 25°C)

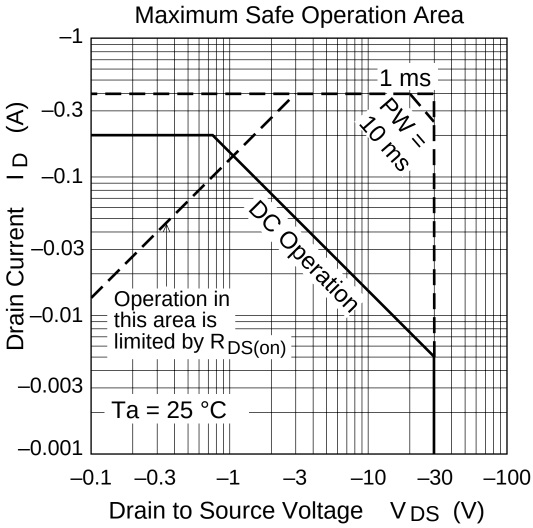
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–0.2	A
Drain peak current	$I_{D(pulse)}{}^*$	–0.4	A
Body–drain diode reverse drain current	I_{DR}	–0.2	A
Channel dissipation	Pch**	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

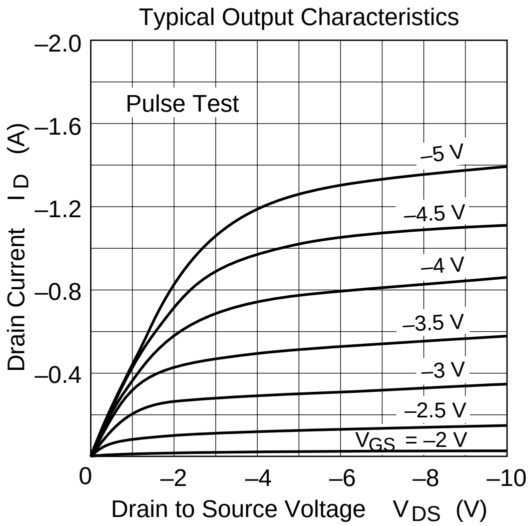
* PW ≤ 100 µs, duty cycle ≤ 10 %
** Marking is “ZF–”

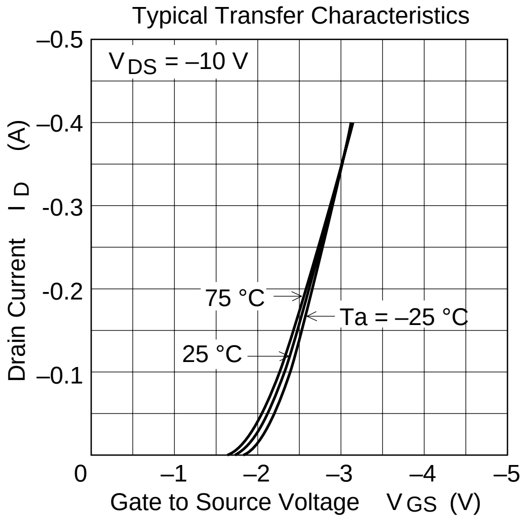
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±2	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	2.7	7.5	Ω	I_D = –20 mA V_{GS} = –4 V *
		—	2.0	7	Ω	I_D = –10 mA V_{GS} = –10 V *
Input capacitance	Ciss	—	1.1	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	22.3	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.17	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	530	—	ns	I_D = –0.1 A
Rise time	t_r	—	2170	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	7640	—	ns	R_L = 100 Ω
Fall time	t_f	—	7690	—	ns	PW = 5 µs

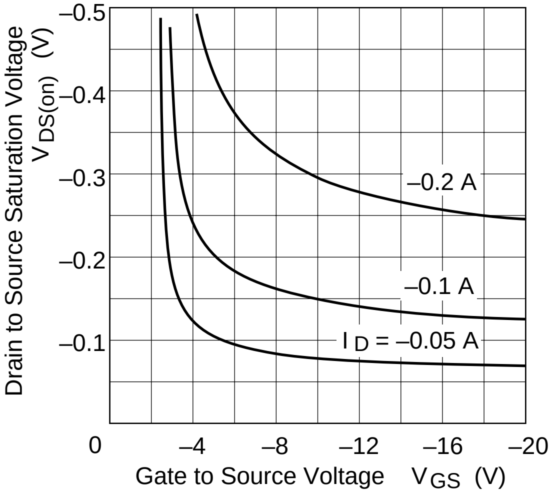

Maximum Channel Dissipation Curve
Channel Power Dissipation Pch (mW)
200
150
100
50
0
50
100
150
200
Ambient Temperature Ta (°C)


Maximum Safe Operation Area
–1
–0.3
–0.1
–0.03
–0.01
–0.003
–0.001
Drain Current I D (A)
1 ms
PW = 10 ms
DC Operation
Operation in this area is limited by R DS(on)
Ta = 25 °C
–0.1
–0.3
–1
–3
–10
–30
–100
Drain to Source Voltage V DS (V)

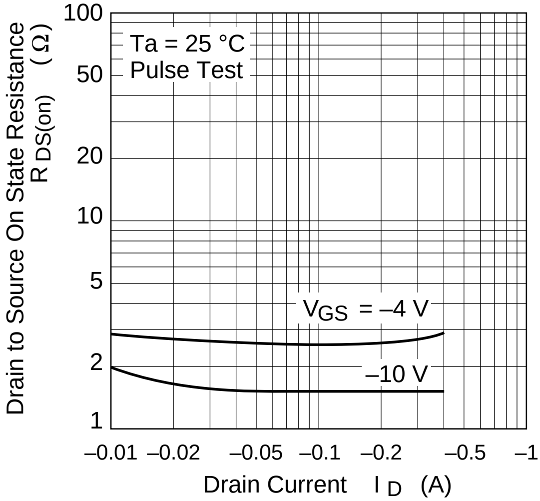

Typical Output Characteristics
–2.0
–1.6
–1.2
–0.8
–0.4
Drain Current I D (A)
Pulse Test
–5 V
–4.5 V
–4 V
–3.5 V
–3 V
–2.5 V
VGS = –2 V
0
–2
–4
–6
–8
–10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
–0.5
–0.4
-0.3
-0.2
–0.1
Drain Current I D (A)
V DS = –10 V
75 °C
25 °C
Ta = –25 °C
0
–1
–2
–3
–4
–5
Gate to Source Voltage V GS (V)

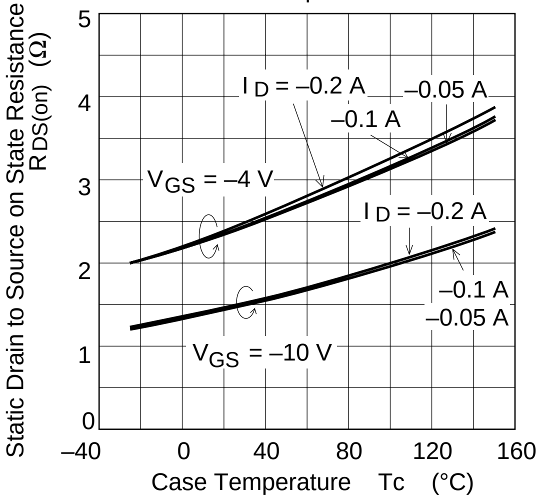
Drain to Source Saturation Voltage vs. Gate to Source Voltage



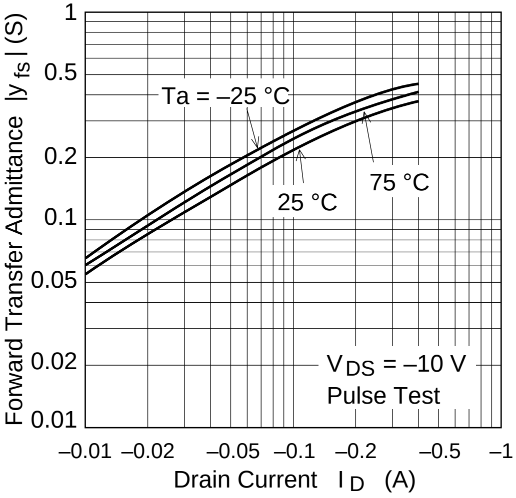
Static Drain to Source on State Resistance vs. Drain Current

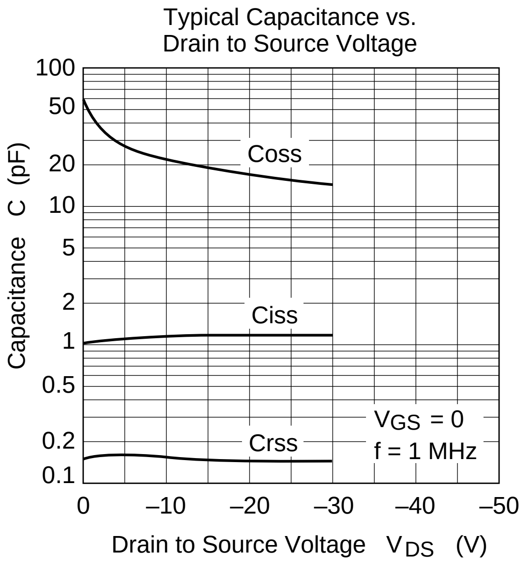


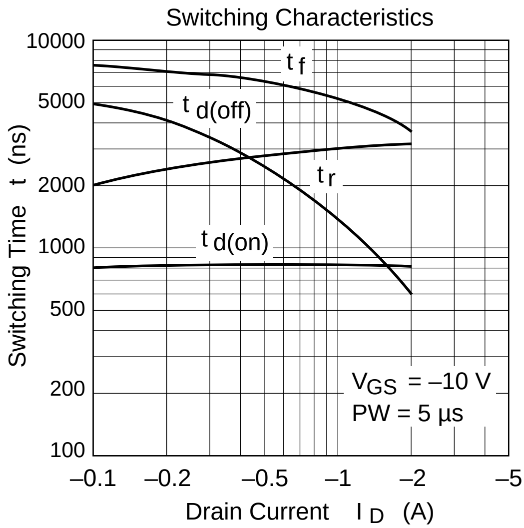
Static Drain to Source on State Resistance vs. Temperature

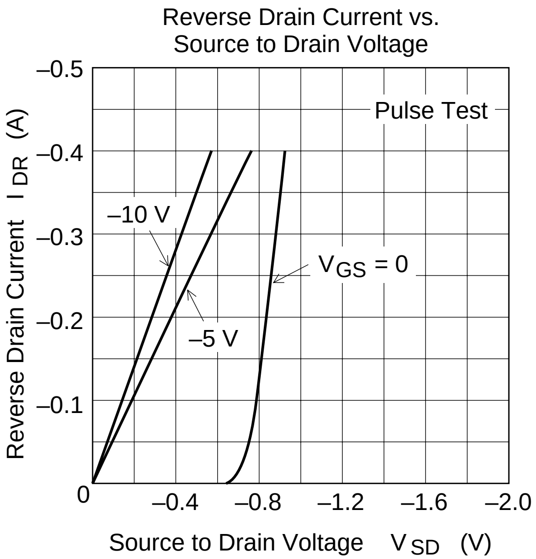


Forward Transfer Admittance vs. Drain Current




Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
100
50
20
10
5
2
1
0.5
0.2
0.1
Coss
Ciss
Crss
VGS = 0
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)


Switching Characteristics
Switching Time t (ns)
10000
5000
2000
1000
500
200
100
t f
t d(off)
t r
t d(on)
VGS = –10 V
PW = 5 µs
–0.1
–0.2
–0.5
–1
–2
–5
Drain Current I D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
–0.5
–0.4
–0.3
–0.2
–0.1
0
Pulse Test
–10 V
–5 V
VGS = 0
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage VSD (V)

2SJ408(L), 2SJ408(S)

Silicon P-Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

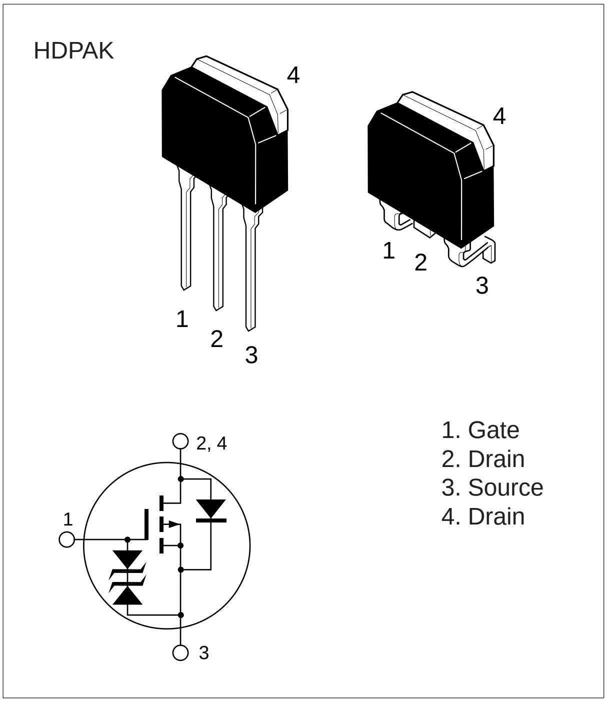


Table 1 Absolute Maximum Ratings (Ta = 25°C)

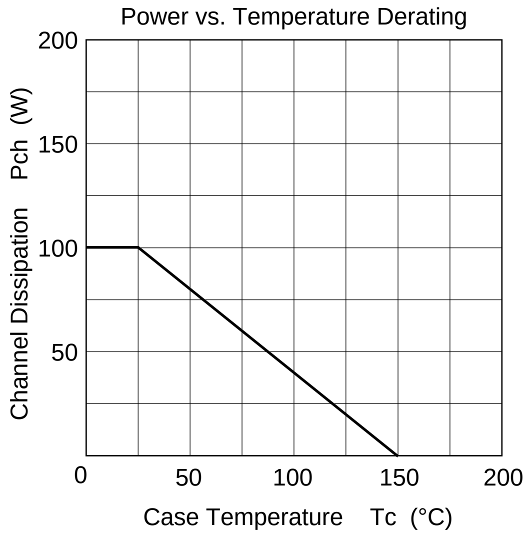
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–50	A
Drain peak current	$I_{D(pulse)}$*	–200	A
Body–drain diode reverse drain current	I_{DR}	–50	A
Avalanche current	I_{AP}***	–50	A
Avalanche energy	E_{AR}***	214	mJ
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

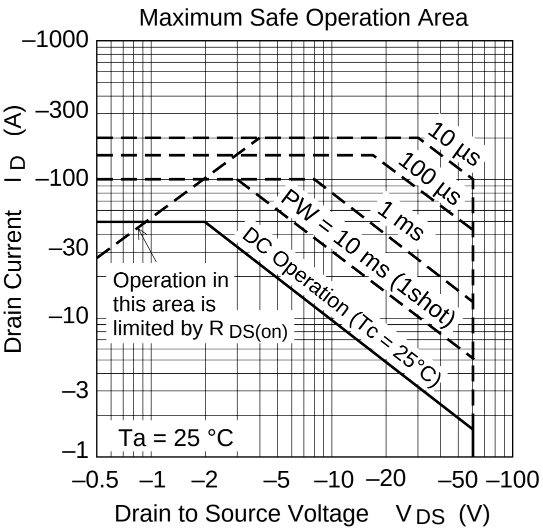
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.015	0.02	Ω	I_D = –25 A V_{GS} = –10 V *
		—	0.02	0.028	Ω	I_D = –25 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	30	50	—	S	I_D = –25 A V_{DS} = –10 V *
Input capacitance	Ciss	—	8200	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	3650	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	750	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	55	—	ns	I_D = –25 A
Rise time	t_r	—	340	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	1150	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	620	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	250	—	ns	I_F = –50 A, V_{GS} = 0, diF / dt = 50 A / µs

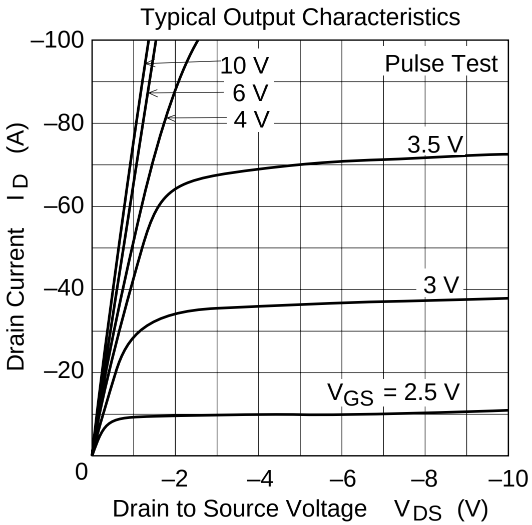
* Pulse Test



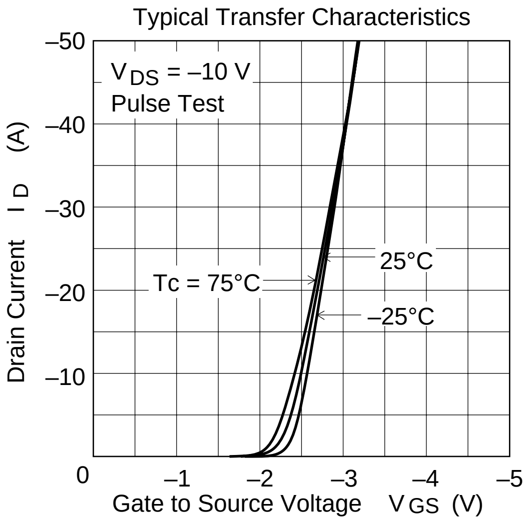
Power vs. Temperature Derating
Channel Dissipation Pch (W)
200
150
100
50
0
50
100
150
200
Case Temperature Tc (°C)



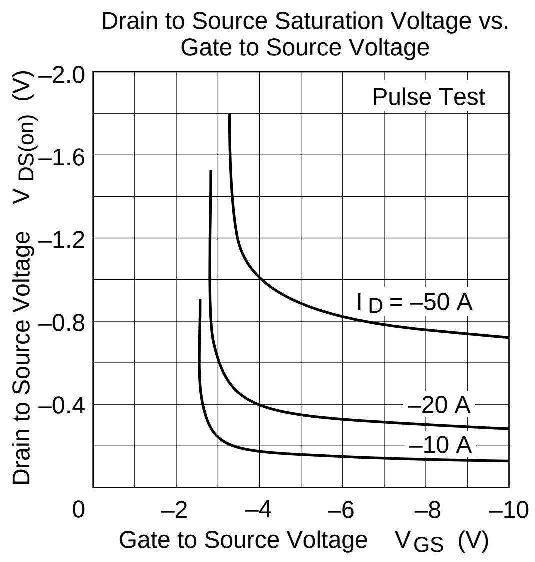
Maximum Safe Operation Area
Drain Current I D (A)
–1000
–300
–100
–30
–10
–3
–1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
–0.5 –1 –2 –5 –10 –20 –50 –100
Drain to Source Voltage V DS (V)

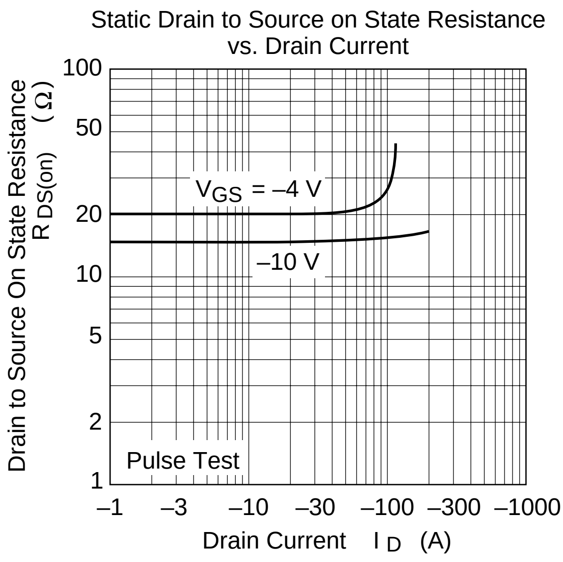


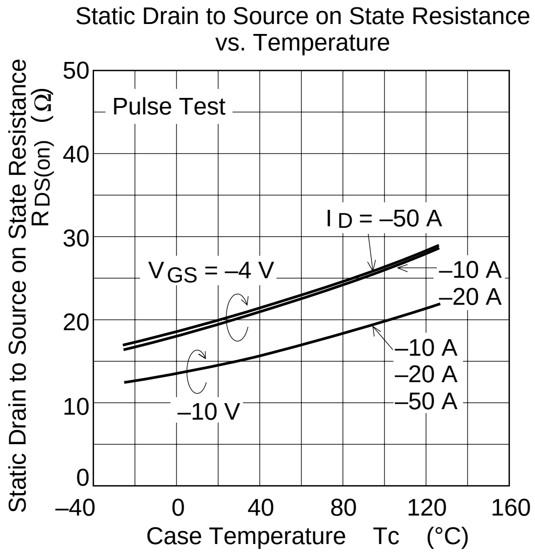
Typical Output Characteristics
Drain Current I D (A)
–100
–80
–60
–40
–20
0
10 V
6 V
4 V
Pulse Test
3.5 V
3 V
VGS = 2.5 V
–2 –4 –6 –8 –10
Drain to Source Voltage V DS (V)

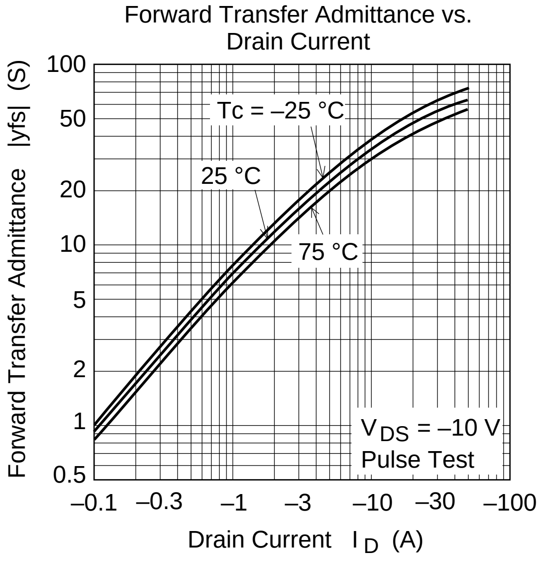


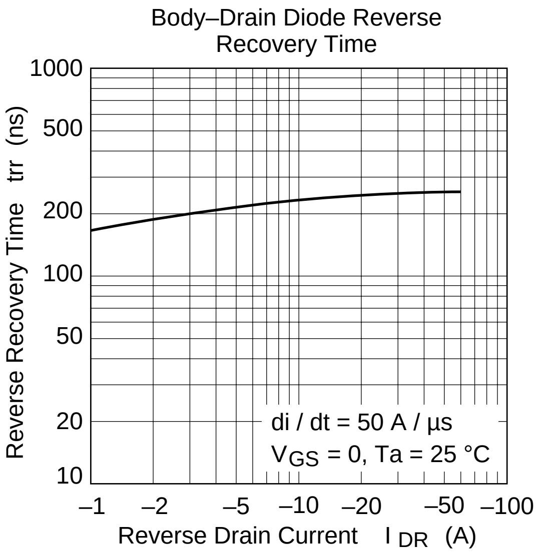
Typical Transfer Characteristics
Drain Current I D (A)
–50
–40
–30
–20
–10
0
VDS = –10 V
Pulse Test
25°C
Tc = 75°C
–25°C
–1 –2 –3 –4 –5
Gate to Source Voltage V GS (V)


Drain to Source Saturation Voltage vs. Gate to Source Voltage
Pulse Test
I D = –50 A
–20 A
–10 A
Drain to Source Voltage V DS(on) (V)
–2.0
–1.6
–1.2
–0.8
–0.4
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

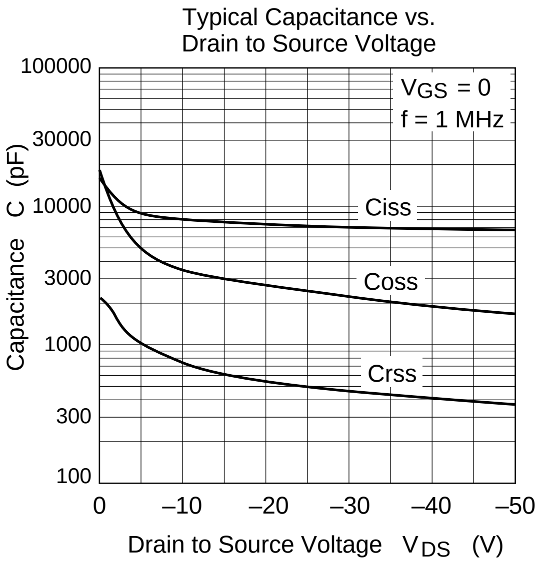

Static Drain to Source on State Resistance vs. Drain Current
V GS = –4 V
–10 V
Pulse Test
Drain to Source On State Resistance R DS(on) (Ω)
100
50
20
10
5
2
1
–1
–3
–10
–30
–100
–300
–1000
Drain Current I D (A)


Static Drain to Source on State Resistance vs. Temperature
Pulse Test
I D = –50 A
V GS = –4 V
–10 A
–20 A
–10 A
–20 A
–50 A
–10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
50
40
30
20
10
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

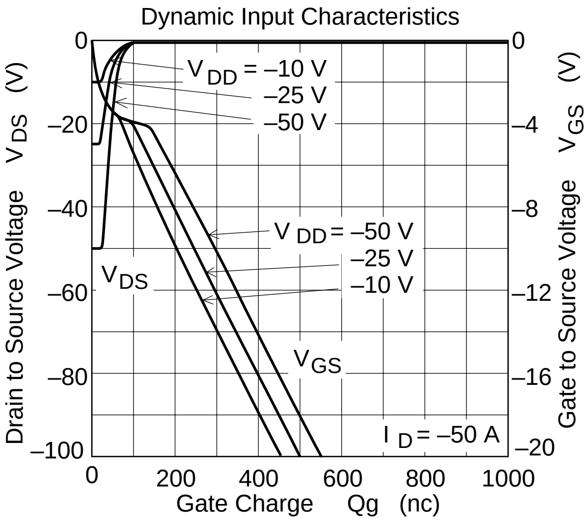

Forward Transfer Admittance vs. Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
100
50
20
10
5
2
1
0.5
–0.1
–0.3
–1
–3
–10
–30
–100
Drain Current I D (A)



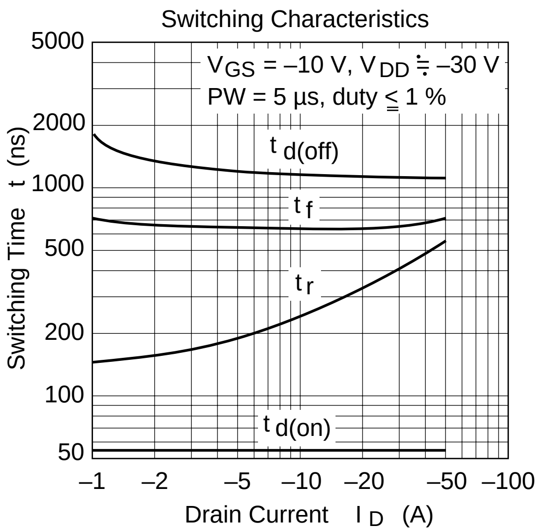
Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
–1 –2 –5 –10 –20 –50 –100
Reverse Drain Current I DR (A)



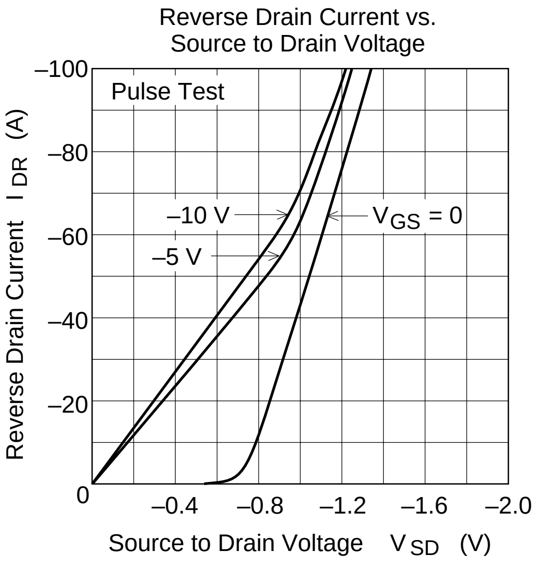
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
100000
30000
10000
3000
1000
300
100
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0 –10 –20 –30 –40 –50
Drain to Source Voltage VDS (V)

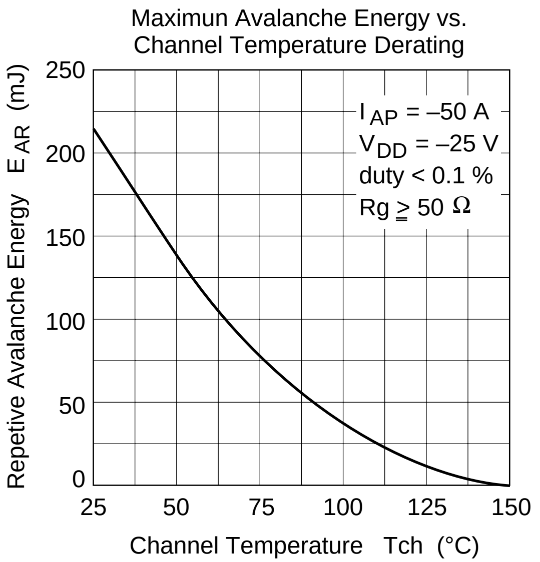


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–20
–40
–60
–80
–100
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
VDD = –10 V
–25 V
–50 V
VDD = –50 V
–25 V
–10 V
VDS
VGS
I D = –50 A
0 200 400 600 800 1000
Gate Charge Qg (nc)

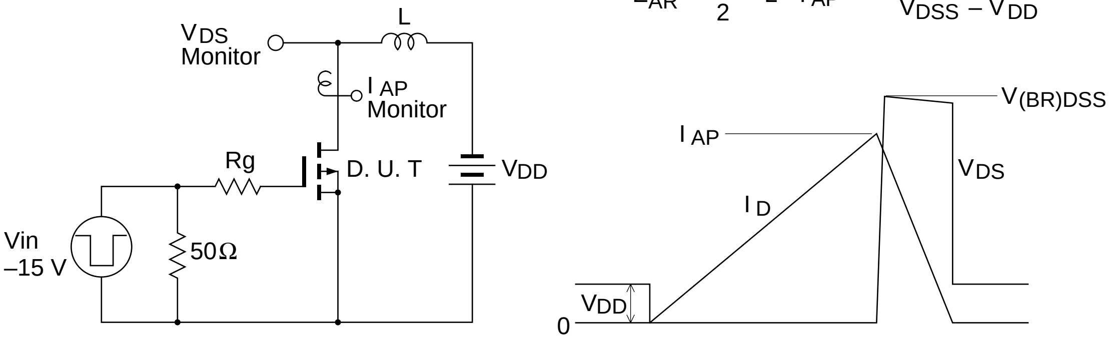


Switching Characteristics
Switching Time t (ns)
5000
2000
1000
500
200
100
50
VGS = –10 V, VDD ≒ –30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
–1 –2 –5 –10 –20 –50 –100
Drain Current I D (A)

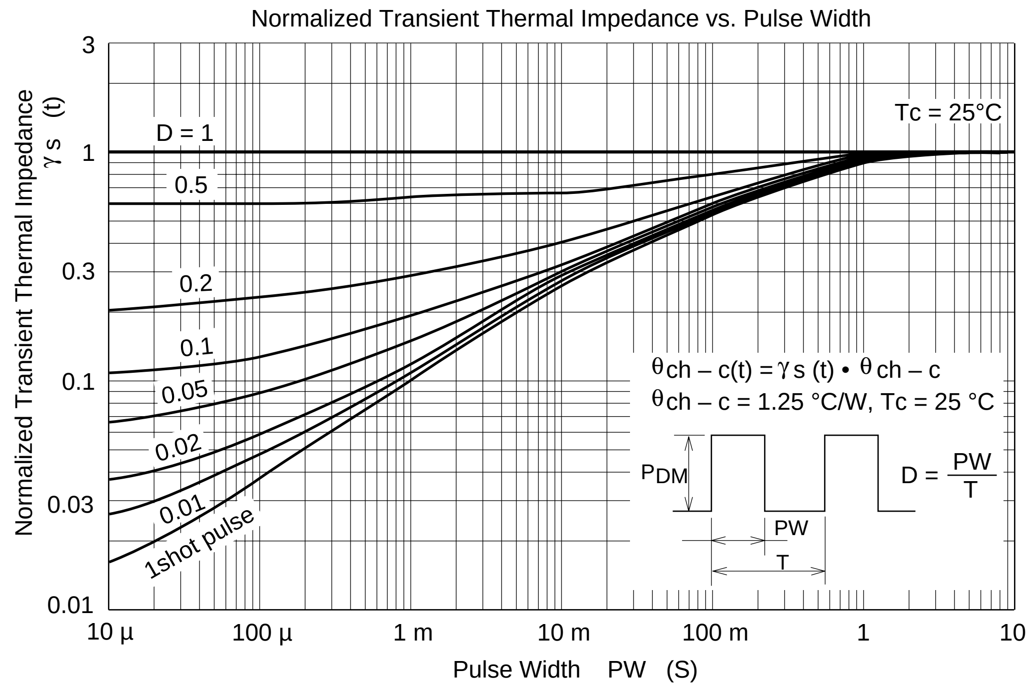




Avalanche Test Circuit and Waveform



$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
3
1
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 1.25 °C/W, Tc = 25 °C
PDM
D = PW / T
PW
T

2SJ409(L), 2SJ409(S)

SILICON P-CHANNEL MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V Gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

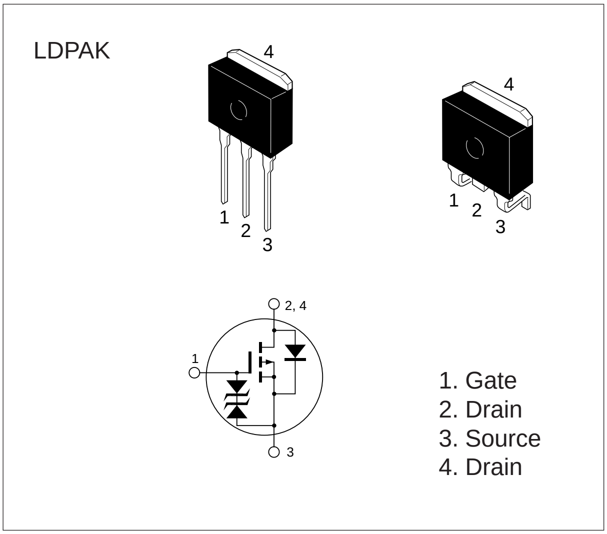


Table 1 Absolute Maximum Ratings (Ta = 25°C)

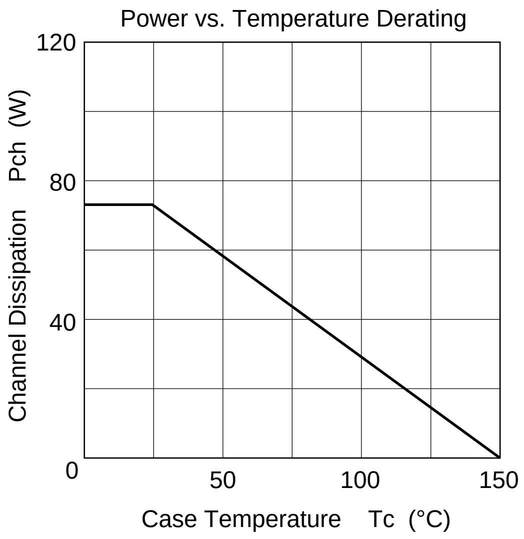
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–20	A
Drain peak current	$I_{D(pulse)}$*	–80	A
Body–drain diode reverse drain current	I_{DR}	–20	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc=25°C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–100	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	I_D = –10 A V_{GS} = –10 V *
		—	0.16	0.22	Ω	I_D = –10 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	7.5	12	—	S	I_D = –10 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1860	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	680	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	145	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = –10 A
Rise time	t_r	—	115	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	320	—	ns	R_L = 3 Ω
Fall time	t_f	—	170	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.05	—	V	I_F = –20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	280	—	ns	I_F = –20 A, V_{GS} = 0, diF / dt = 50 A / µs

See characteristics curves of 2SJ221



Power vs. Temperature Derating
120
80
40
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

2SJ410

Silicon P Channel MOS FET

HITACHI

1st. Edition
Jun. 1995
Preliminary

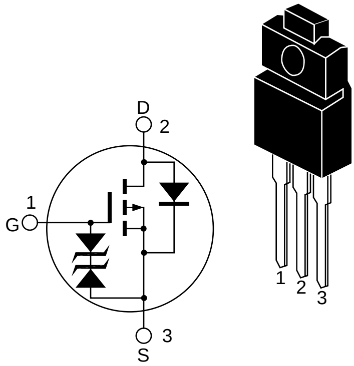
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC–DC converter and motor driver

TO–220FM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–200	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–6	A
Drain peak current	$I_{D(pulse)}$*	–24	A
Body–drain diode reverse drain current	I_{DR}	–6	A
Channel dissipation	Pch**	–30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

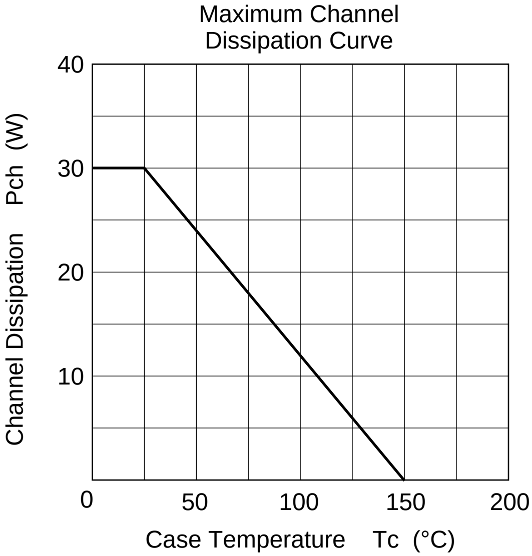
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

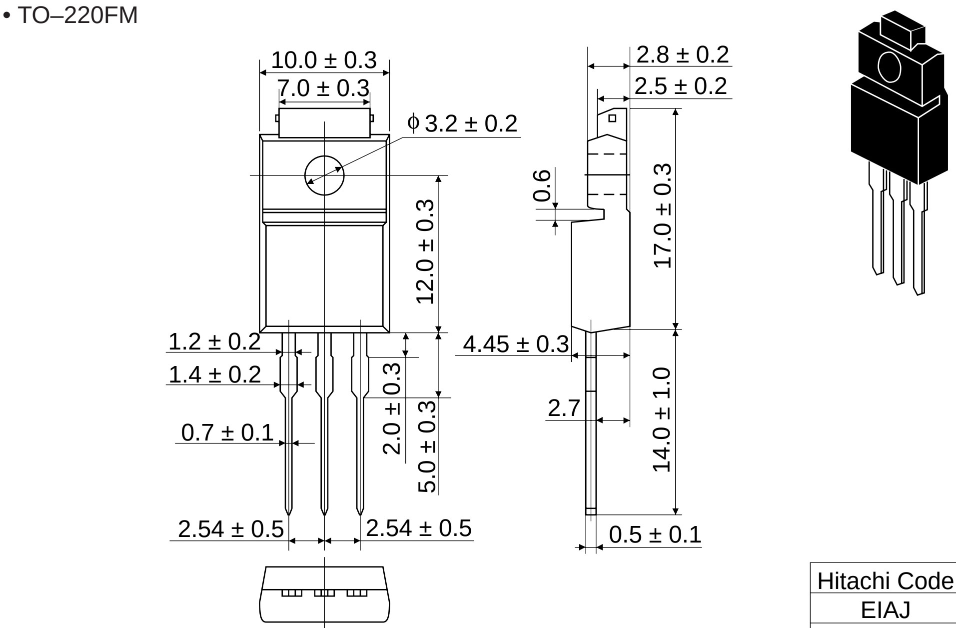
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–200	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} =–160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–2.0	—	–4.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.9	Ω	I_D = –3 A V_{GS} = –10 V *
Forward transfer admittance	$\|y_{fs}\|$	2.0	3.5	—	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(920)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(190)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(70)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(17)	—	ns	I_D = –3 A
Rise time	t_r	—	(40)	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(85)	—	ns	R_L = 6Ω
Fall time	t_f	—	(45)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –6 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(170)	—	ns	I_F = –6 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test



Package Dimensions

Unit : mm



Hitachi Code	TO–220FM
EIAJ	SC–72
JEDEC	—

2SJ443

Silicon P Channel MOS FET

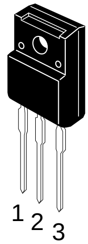
Application

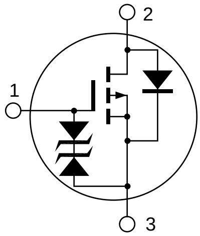
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V Gate drive can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

TO–220CFM





1. Gate
2. Drain
3. Source

Table 1   Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–10	A
Drain peak current	$I_{D(pulse)}$*	–40	A
Body–drain diode reverse drain current	I_{DR}	–10	A
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

*   PW ≤ 10 µs, duty cycle ≤ 1 %
**   Value at Tc=25°C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.18	Ω	I_D = –5A V_{GS} = –10 V *
		—	0.18	0.25	Ω	I_D = –5A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	6.5	—	S	I_D = –5A V_{DS} = –10 V *
Input capacitance	Ciss	—	900	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	460	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	130	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = –5A
Rise time	t_r	—	65	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	170	—	ns	R_L =6 Ω
Fall time	t_f	—	105	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –10A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = –10 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curves of 2SJ172, 2SJ175

2SJ450
Silicon P Channel MOS FET

1st. Edition
Jun. 1995

HITACHI

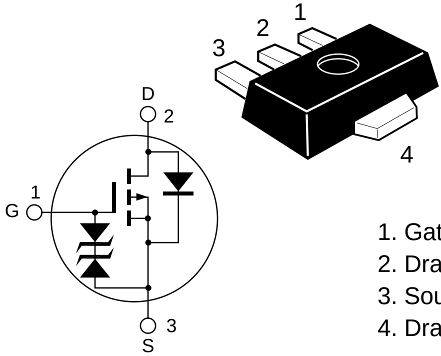
Application

High speed power switching

Features

- Low on-resistance.
- Low drive power
- High speed switching
- 2.5V gate drive device.

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–1	A
Drain peak current	$I_{D(pulse)}$*	–2	A
Drain peak current	I_{DR}	–1	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

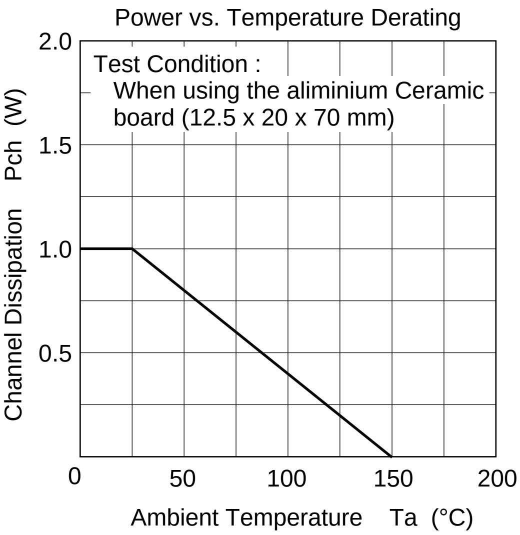
* PW ≤ 100 µs, duty cycle ≤ 10 %
** When using aluminium ceramic board (12.5 x 20 x 70 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–50	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.85	1.2	Ω	I_D = –0.5 A V_{GS} = –4 V *
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.9	Ω	I_D = –0.3 A V_{GS} = –2.5 V *
Fowerd transfer admittance	$\|y_{fs}\|$	0.6	1.0	—	S	I_D = –0.5 A V_{DS} = –10 V
Input capacitance	Ciss	—	150	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	72	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	24	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	6	—	µs	V_{GS} = –10 V, I_D = –0.5 A
Rise time	t_r	—	9	—	µs	R_L = 60 Ω
Turn–off delay time	$t_{d(off)}$	—	50	—	µs	
Fall time	t_f	—	35	—	µs	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –1 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	100	—	ns	I_F = –1 A, V_{GS} = 0 diF / dt = 50A / µs

* Pulse Test

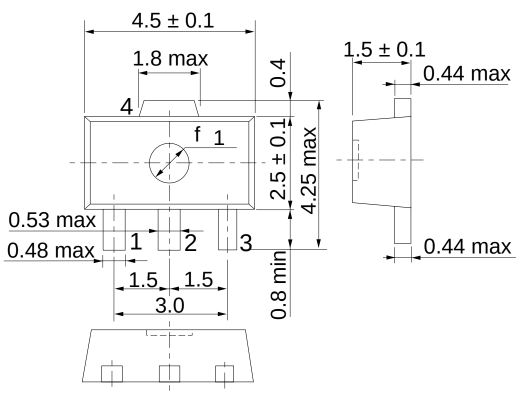
Marking is "UY".

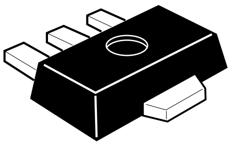


Package Dimensions

Unit : mm

• UPAK





Hitachi Code	UPAK
EIAJ	SC–62
JEDEC	UPAK

2SJ451
Silicon P Channel MOS FET

HITACHI

1st. Edition
Jun. 1995

Application

Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5V gate drive device.
- Small package (MPAK).

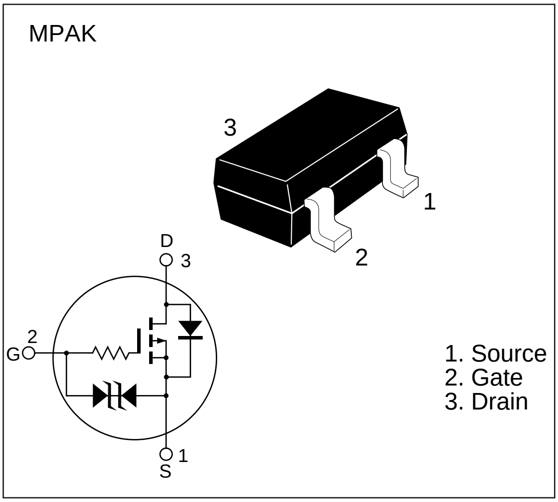


Table 1 Absolute Maximum Ratings (Ta = 25°C)

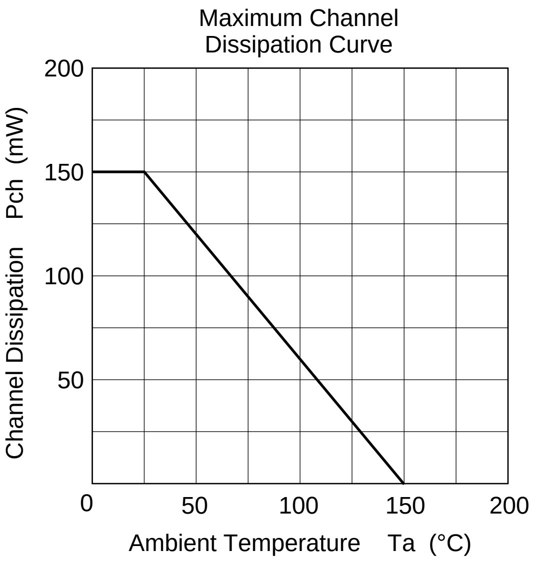
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–0.2	A
Drain peak current	$I_{D(pulse)}$*	–0.4	A
Channel dissipation	Pch**	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
Marking is "ZK–".

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1.0	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±2.0	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}1$	—	2.3	3.5	Ω	I_D = –100 mA V_{GS} = –4 V *
Static drain to source on state resistance	$R_{DS(on)}2$	—	5.0	9.0	Ω	I_D = –40 mA V_{GS} = –2.5 V *
Foward transfer admittance	$\|y_{fs}\|$	0.13	0.23	—	S	I_D = –100 mA V_{DS} = –10 V
Input capacitance	Ciss	—	2.4	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	31	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.6	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	0.17	—	µs	V_{GS} = –10 V, I_D = –0.1 A
Rise time	t_r	—	0.68	—	µs	R_L = 100 Ω
Turn–off delay time	$t_{d(off)}$	—	3.0	—	µs	
Fall time	t_f	—	2.8	—	µs	

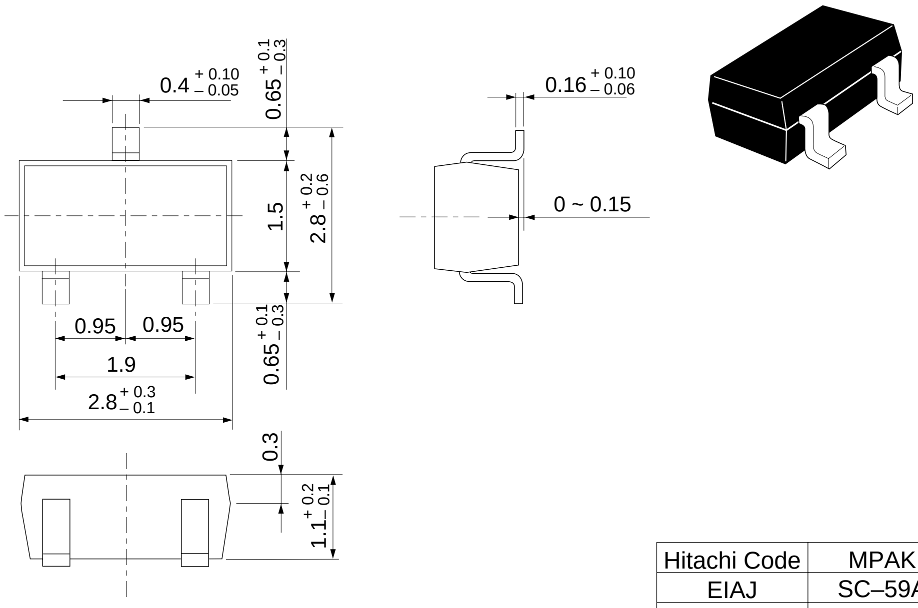
* Pulse Test



Package Dimensions

Unit : mm

• MPAK



Hitachi Code	MPAK
EIAJ	SC–59A
JEDEC	—

2SJ452

Silicon P Channel MOS FET

HITACHI

2nd. Edition
Jun. 1995

Application

Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5V gate drive device.
- Small package (MPAK).

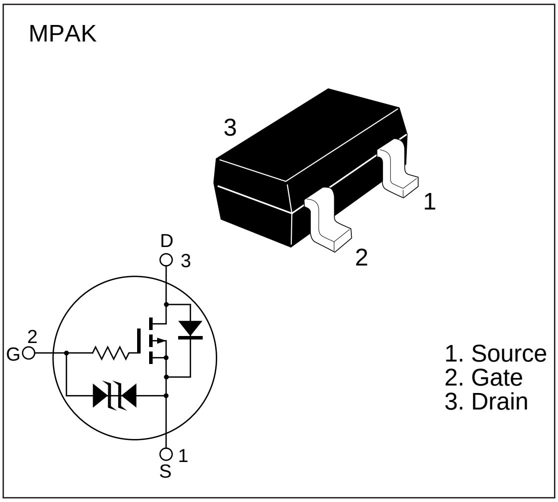


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–50	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–0.2	A
Drain peak current	$I_{D(pulse)}$*	–0.4	A
Channel dissipation	Pch**	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
Marking is "ZM–".

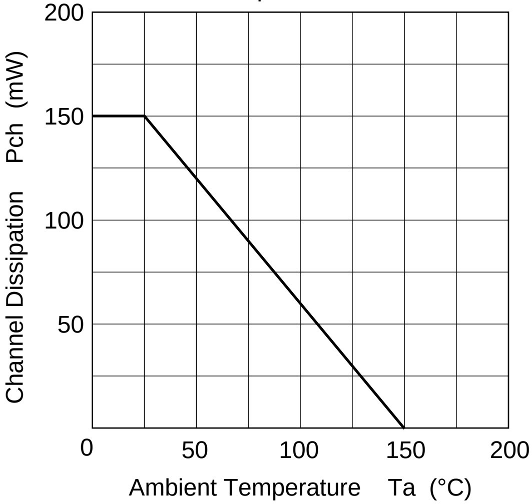
Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–50	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1.0	µA	V_{DS} = –40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±2.0	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}1$	—	5.0	7.0	Ω	I_D = –100 mA V_{GS} = –4 V *
Static drain to source on state resistance	$R_{DS(on)}2$	—	7.5	12.0	Ω	I_D = –40 mA V_{GS} = –2.5 V *
Foward transfer admittance	$\|y_{fs}\|$	0.1	0.19	—	S	I_D = –100 mA V_{DS} = –10 V
Input capacitance	Ciss	—	1.1	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	15.7	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.12	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	0.45	—	µs	V_{GS} = –10 V, I_D = –0.1 A
Rise time	t_r	—	1.3	—	µs	R_L = 300 Ω
Turn–off delay tiem	$t_{d(off)}$	—	8.4	—	µs	
Fall time	t_f	—	5.6	—	µs	

* Pulse Test

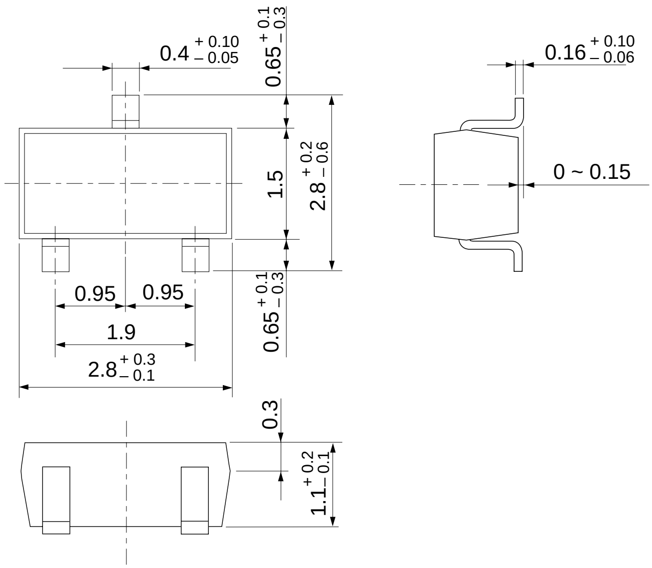
Maximum Channel Dissipation Curve

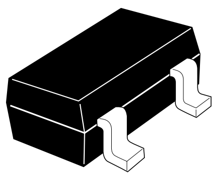


Package Dimensions

Unit : mm

• MPAK





Hitachi Code	MPAK
EIAJ	SC–59A
JEDEC	—

2SK213, 2SK214, 2SK215, 2SK216

Silicon N-Channel MOS FET

Application

High frequency and low frequency power amplifier, high speed switching.
Complementary pair with 2SJ76, J77, J78, J79

Features

- Suitable for direct mounting
- High forward transfer admittance
- Excellent frequency response
- Enhancement-mode

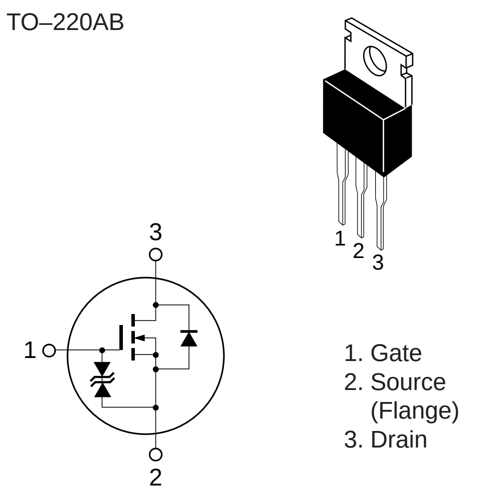


Table 1 Absolute Maximum Ratings (Ta = 25°C)

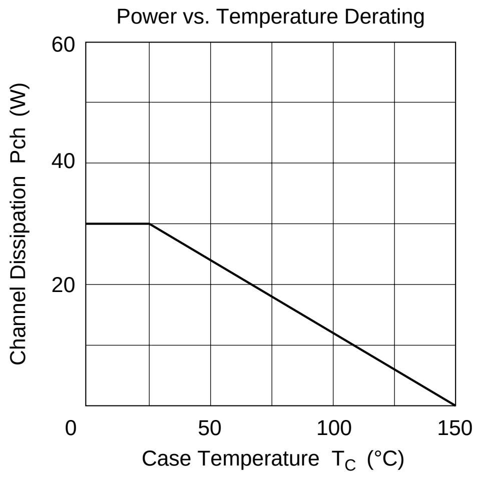
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK213	V_{DSX}	140	V
	2SK214		160	
	2SK215		180	
	2SK216		200	
Gate to source voltage		V_{GSS}	±15	V
Drain current		I_D	500	mA
Body to drain diode reverse drain current		I_{DR}	500	mA
Channel dissipation		Pch	1.75	W
		Pch*	30	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–45 to +150	°C

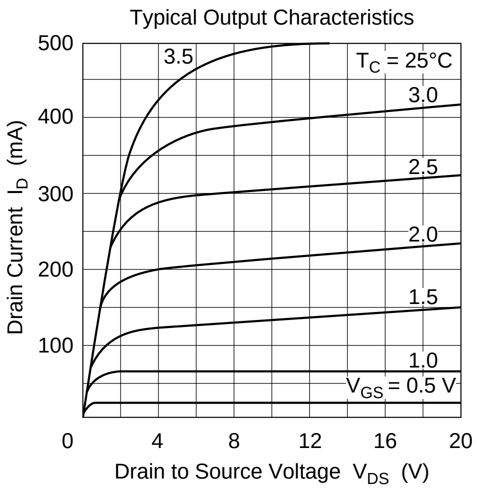
* Value at T_C = 25 °C

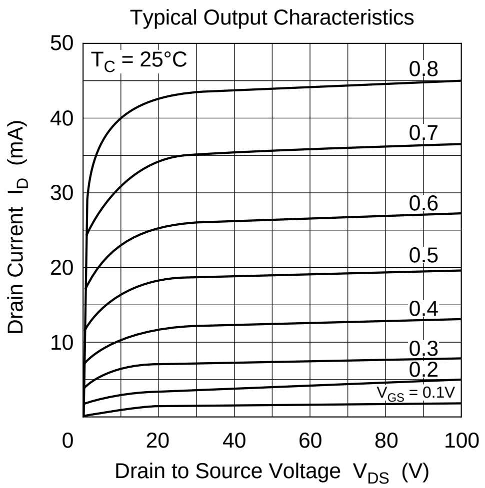
Table 2 Electrical Characteristics (Ta = 25°C)

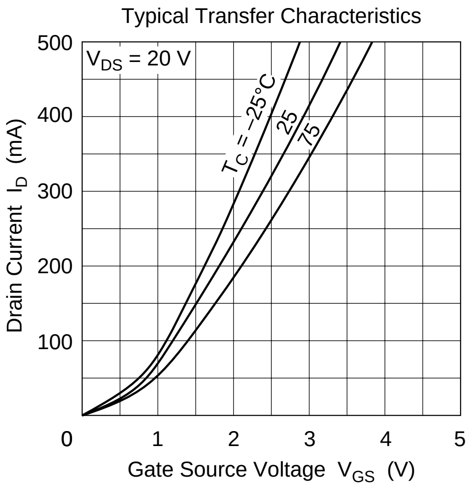
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK213	$V_{(BR)DSX}$	140	—	—	V	I_D = 1 mA, V_{GS} = –2 V
	2SK214		160	—	—	V	
	2SK215		180	—	—	V	
	2SK216		200	—	—	V	
Gate to source breakdown voltage		$V_{(BR)GSS}$	±15	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source voltage		$V_{GS(on)}$	0.2	—	1.5	V	I_D = 10 mA, V_{DS} = 10 V *
Drain to source saturation voltage		$V_{DS(sat)}$	—	—	2.0	V	I_D = 10 mA, V_{GD} = 0 *
Forward transfer admittance		$\|y_{fs}\|$	20	40	—	mS	I_D = 10 mA, V_{DS} = 20 V *
Input capacitance		Ciss	—	90	—	pF	I_D = 10 mA, V_{DS} = 10 V,
Reverse transfer capacitance		Crss	—	2.2	—	pF	f = 1 MHz

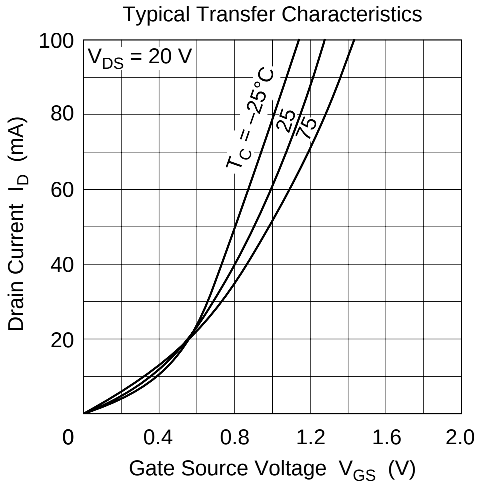
* Pulse Test

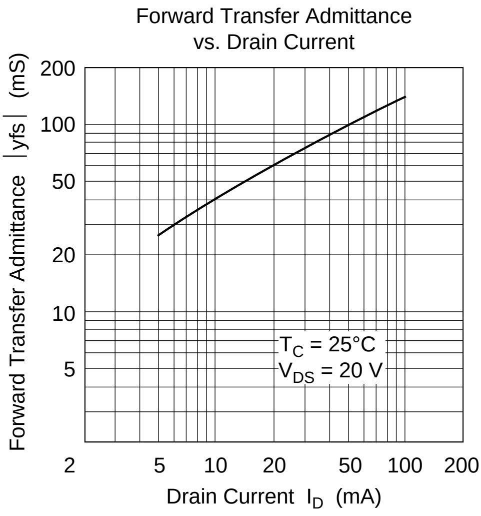

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

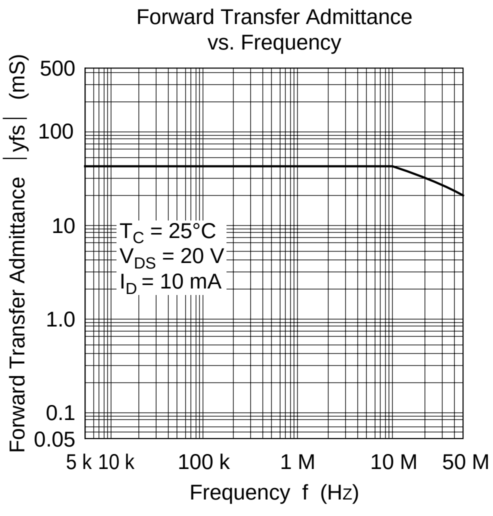

Typical Output Characteristics
T_C = 25°C
Drain Current I_D (mA)
500
400
300
200
100
3.5
3.0
2.5
2.0
1.5
1.0
V_{GS} = 0.5 V
0
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)


Typical Output Characteristics
T_C = 25°C
Drain Current I_D (mA)
50
40
30
20
10
0.8
0.7
0.6
0.5
0.4
0.3
0.2
V_{GS} = 0.1V
0
20
40
60
80
100
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
V_{DS} = 20 V
T_C = –25°C
25
75
Drain Current I_D (mA)
500
400
300
200
100
0
1
2
3
4
5
Gate Source Voltage V_{GS} (V)


Typical Transfer Characteristics
V_{DS} = 20 V
T_C = –25°C
25
75
Drain Current I_D (mA)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Gate Source Voltage V_{GS} (V)


Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (mS)
200
100
50
20
10
5
T_C = 25°C
V_{DS} = 20 V
2
5
10
20
50
100
200
Drain Current I_D (mA)


Forward Transfer Admittance
vs. Frequency
Forward Transfer Admittance |yfs| (mS)
500
100
10
1.0
0.1
0.05
T_C = 25°C
V_{DS} = 20 V
I_D = 10 mA
5 k
10 k
100 k
1 M
10 M
50 M
Frequency f (Hz)

2SK740

Silicon N-Channel MOS FET

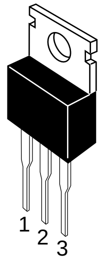
Application

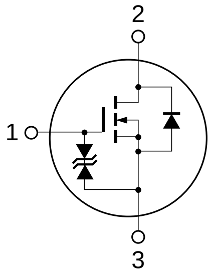
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

TO–220AB





1. Gate
2. Drain (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

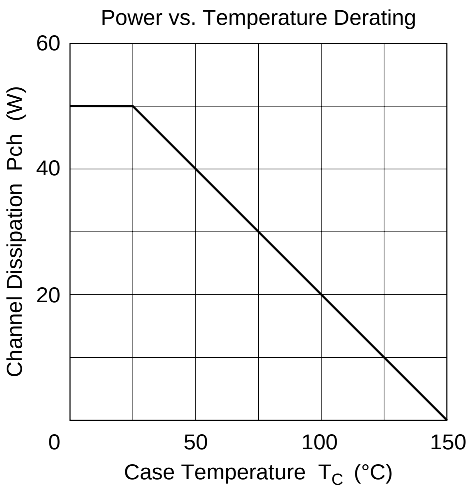
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	150	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch*	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

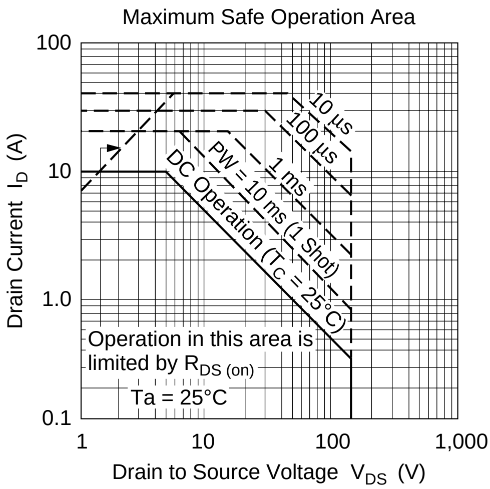
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

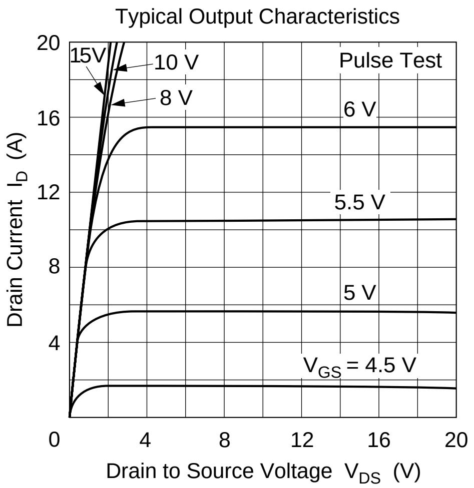
Table 2 Electrical Characteristics (Ta = 25°C)

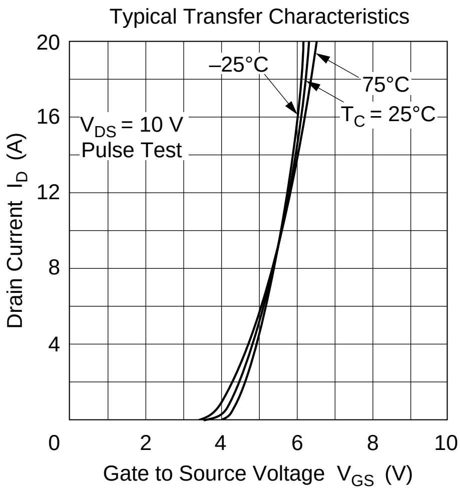
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	150	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 120 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 5 A, V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	7.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1200	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	550	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	85	—	pF	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time	t_r	—	50	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	t_f	—	40	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

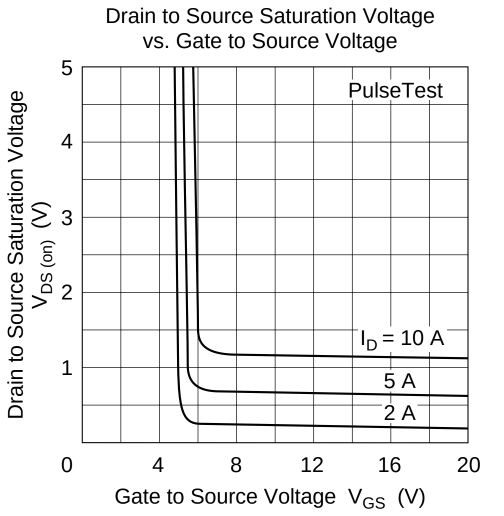
* Pulse Test

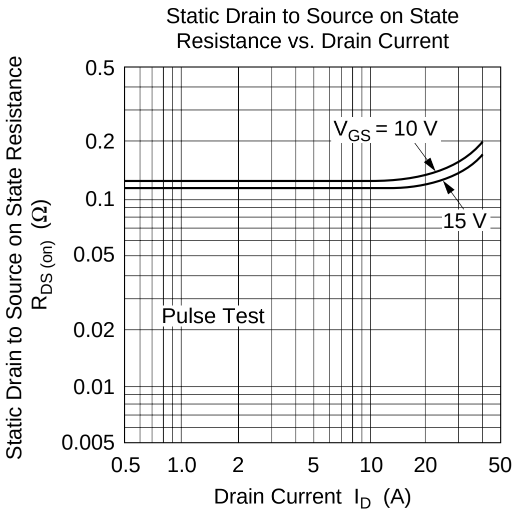

Power vs. Temperature Derating
60
40
20
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

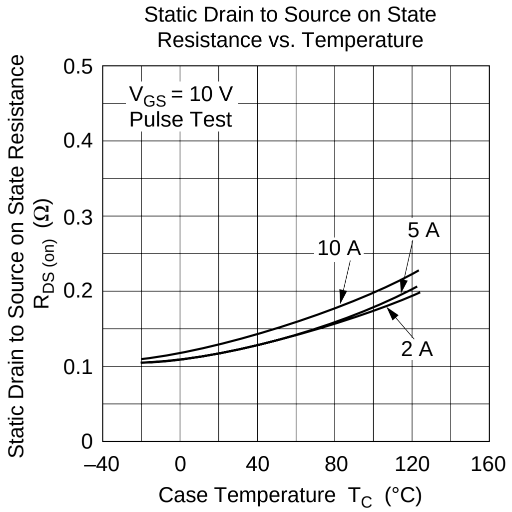

Maximum Safe Operation Area
100
10
1.0
0.1
1
10
100
1,000
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this area is limited by $R_{DS\ (on)}$
Ta = 25°C
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

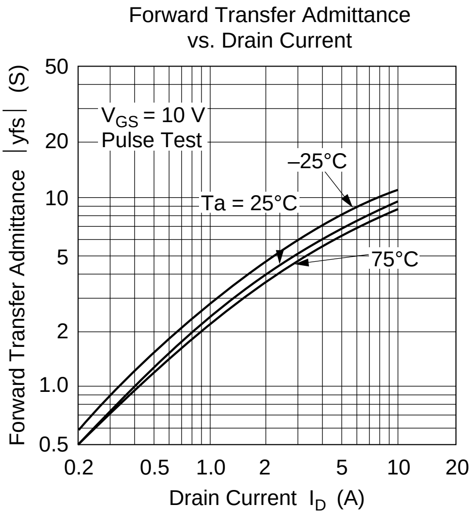

Typical Output Characteristics
20
16
12
8
4
0
4
8
12
16
20
15V
10 V
8 V
Pulse Test
6 V
5.5 V
5 V
V_{GS} = 4.5 V
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
20
16
12
8
4
0
2
4
6
8
10
–25°C
75°C
T_C = 25°C
V_{DS} = 10 V
Pulse Test
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

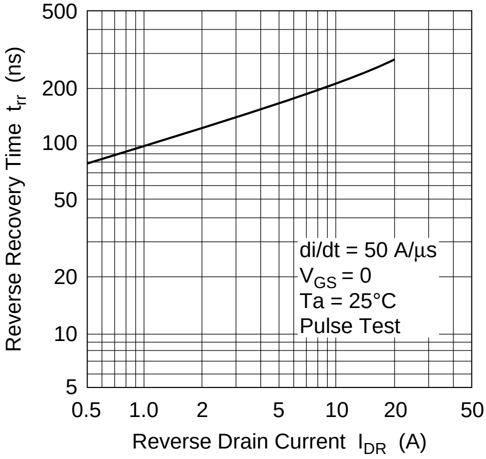

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
$V_{DS\ (on)}$ (V)
Pulse Test
I_D = 10 A
5 A
2 A
0
1
2
3
4
5
4
8
12
16
20
Gate to Source Voltage V_{GS} (V)


Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
V_{GS} = 10 V
15 V
Pulse Test
0.5
0.2
0.1
0.05
0.02
0.01
0.005
1.0
2
5
10
20
50
Drain Current I_D (A)

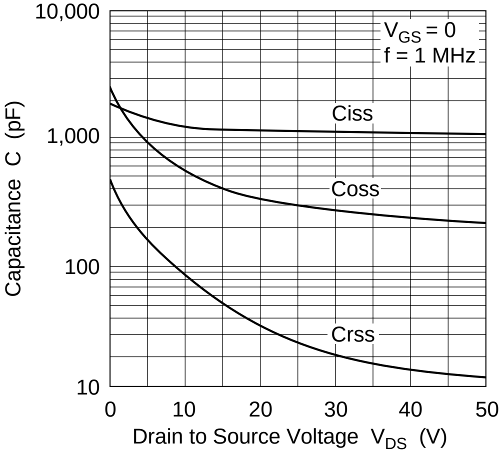

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
V_{GS} = 10 V
Pulse Test
10 A
5 A
2 A
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature T_C (°C)


Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
V_{GS} = 10 V
Pulse Test
–25°C
Ta = 25°C
75°C
50
20
10
5
2
1.0
0.5
0.2
0.5
1.0
2
5
10
20
Drain Current I_D (A)

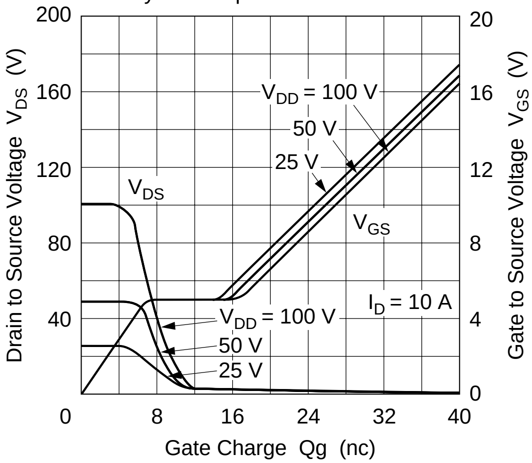
Body to Drain Diode Reverse Recovery Time



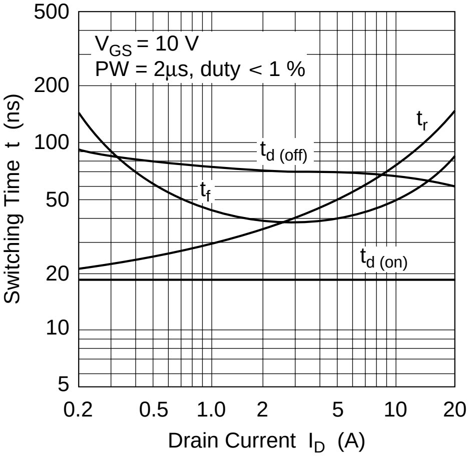
Typical Capacitance vs. Drain to Source Voltage

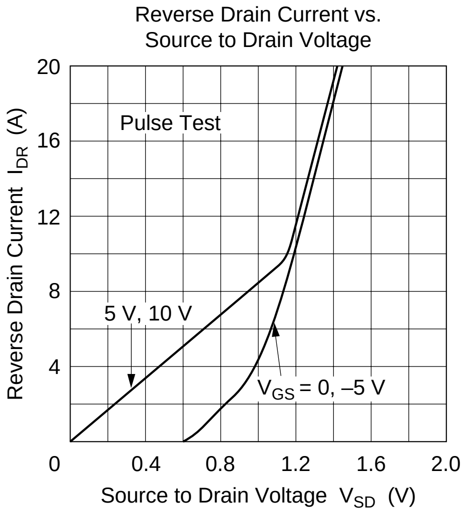


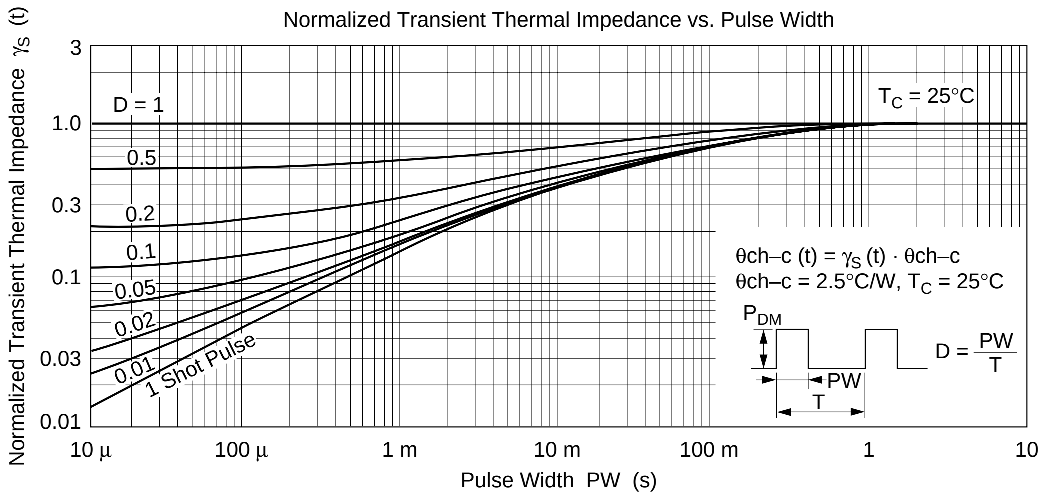
Dynamic Input Characteristics



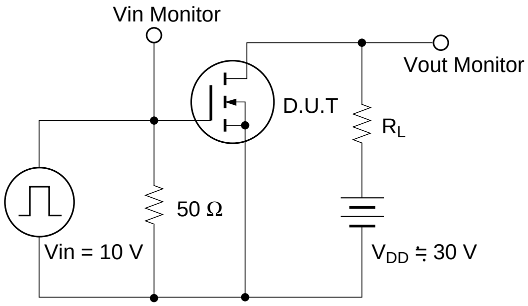
Switching Characteristics



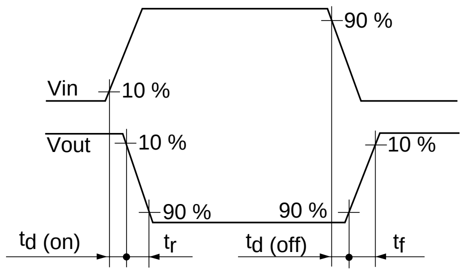

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5 V, 10 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
20
16
12
8
4
0
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
θch–c (t) = γ_S (t) · θch–c
θch–c = 2.5°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK741

Silicon N-Channel MOS FET

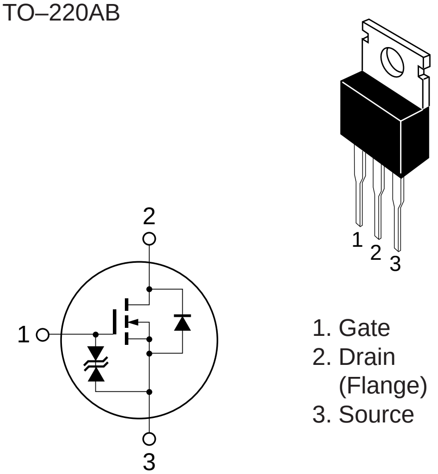
Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

TO–220AB



1. Gate
2. Drain (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body to drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %

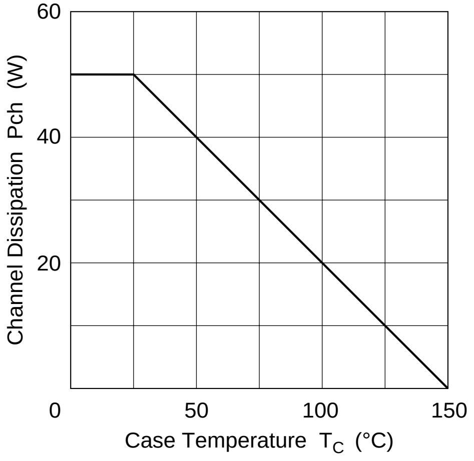
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

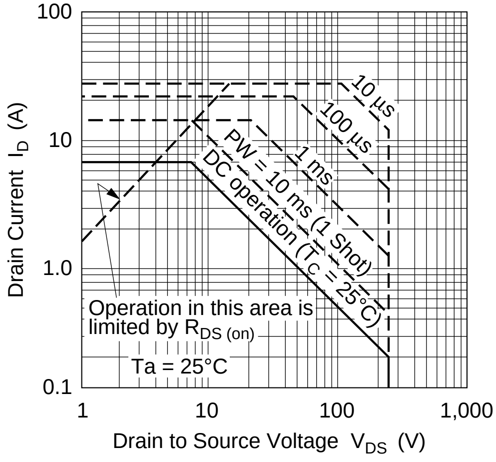
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.40	0.55	Ω	I_D = 4 A, V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	2.7	4.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	820	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	370	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	115	—	pF	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	I_D = 4 A, V_{GS} = 10 V,
Rise time	t_r	—	48	—	ns	R_L = 7.5 Ω
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	t_f	—	50	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 7 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	400	—	ns	I_F = 7 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

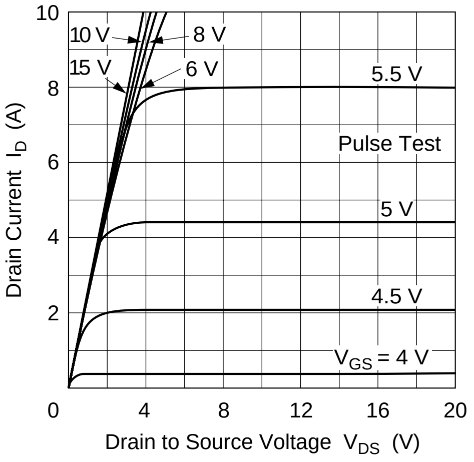
Power vs. Temperature Derating



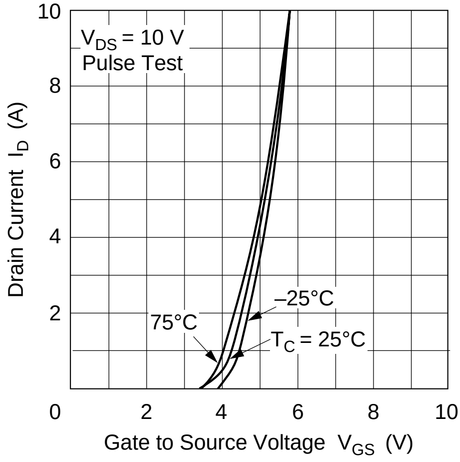
Maximum Safe Operation Area



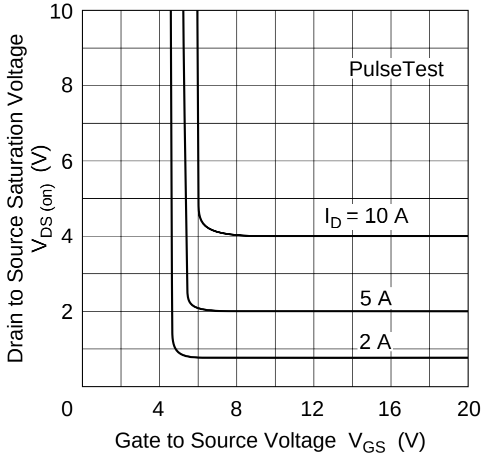
Typical Output Characteristics



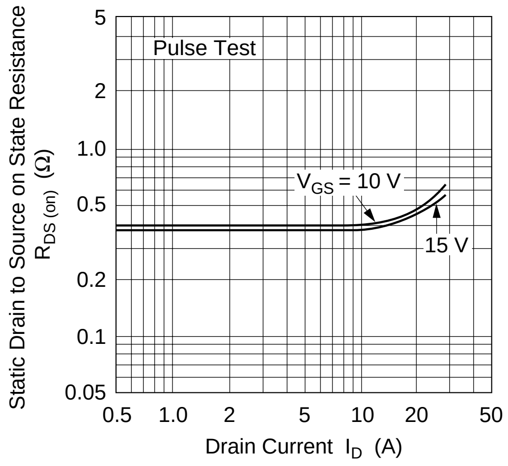
Typical Transfer Characteristics



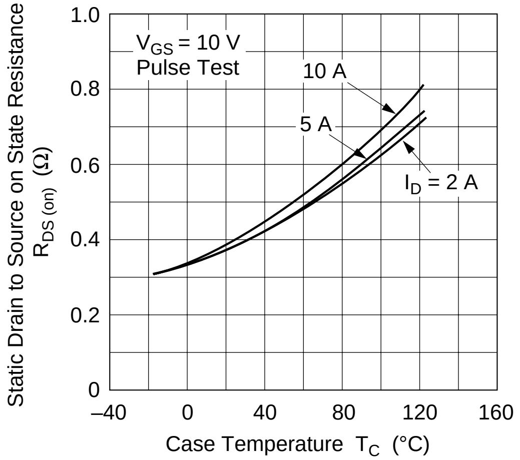
Drain to Source Saturation Voltage vs. Gate to Source Voltage



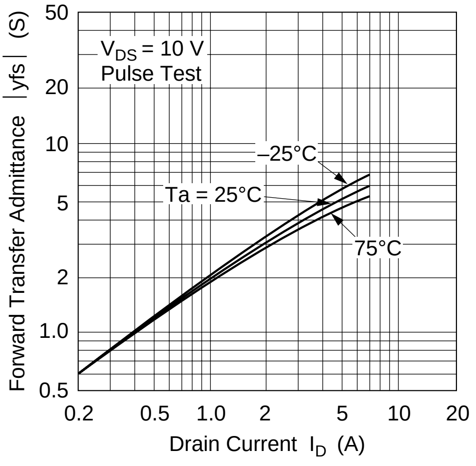
Static Drain to Source on State Resistance vs. Drain Current

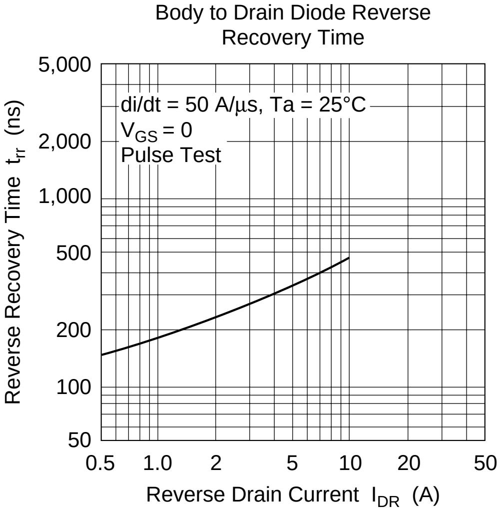


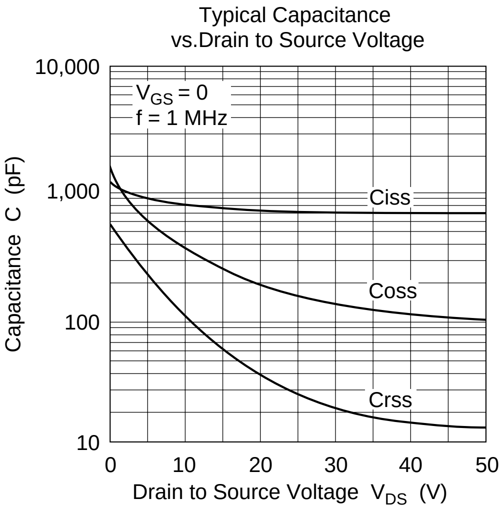
Static Drain to Source on State Resistance vs. Temperature

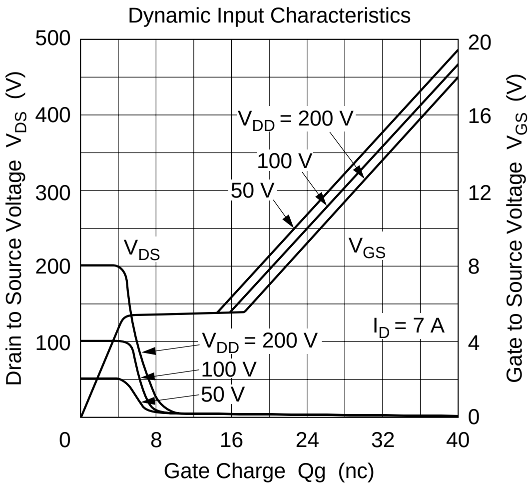


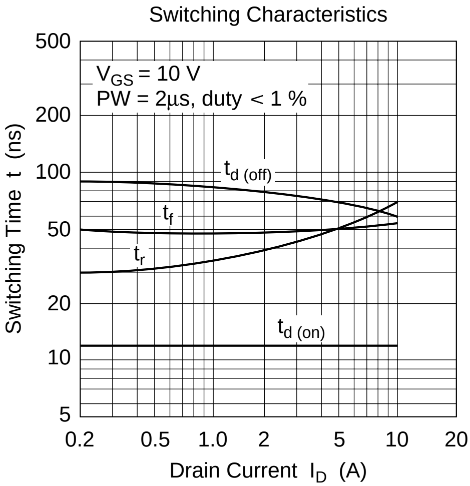
Forward Transfer Admittance vs. Drain Current

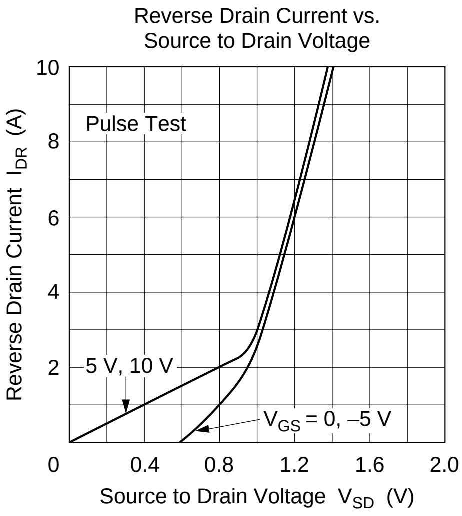


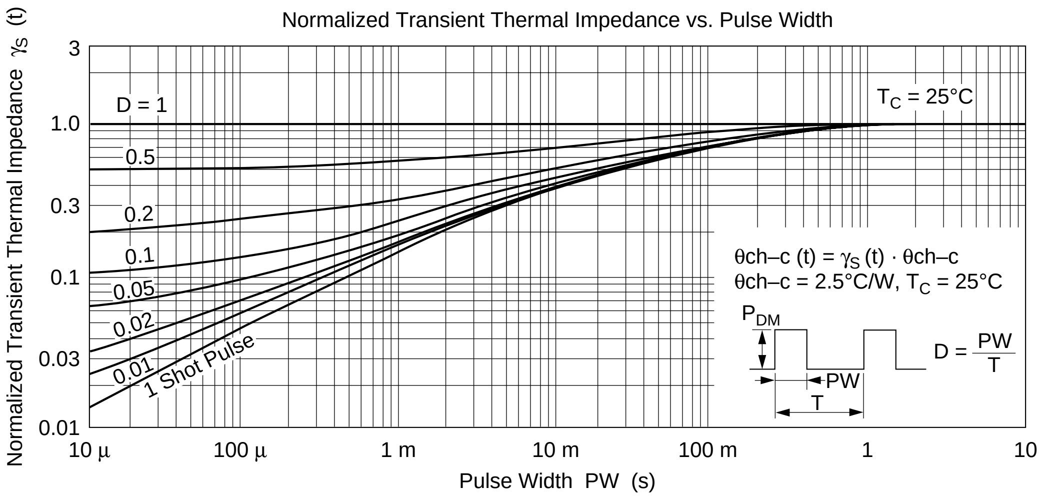

Body to Drain Diode Reverse
Recovery Time
di/dt = 50 A/μs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
5,000
2,000
1,000
500
200
100
50
0.5
1.0
2
5
10
20
50
Reverse Drain Current IDR (A)


Typical Capacitance
vs.Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10,000
1,000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

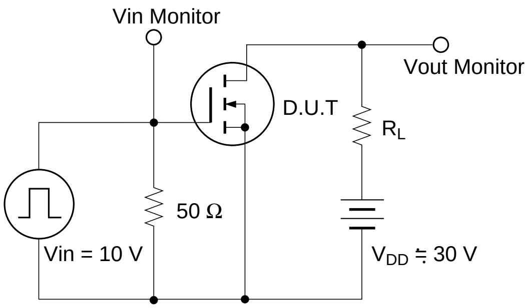

Dynamic Input Characteristics
VDD = 200 V
100 V
50 V
VDS
VGS
ID = 7 A
VDD = 200 V
100 V
50 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
500
400
300
200
100
20
16
12
8
4
0
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
VGS = 10 V
PW = 2μs, duty < 1 %
td (off)
tf
tr
td (on)
Switching Time t (ns)
500
200
100
50
20
10
5
0.2
0.5
1.0
2
5
10
20
Drain Current ID (A)

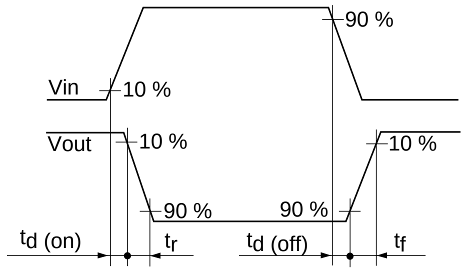

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5 V, 10 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
10
8
6
4
2
0
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 2.5°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK970

Silicon N-Channel MOS FET

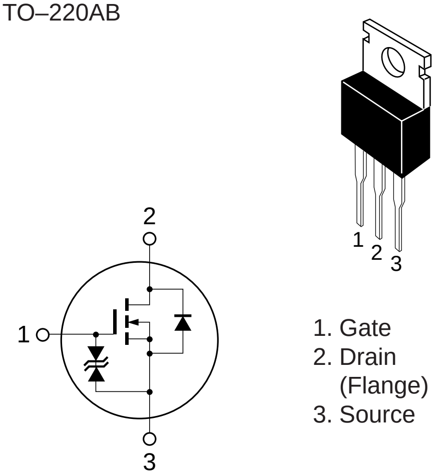
Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

TO–220AB



1. Gate
2. Drain (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

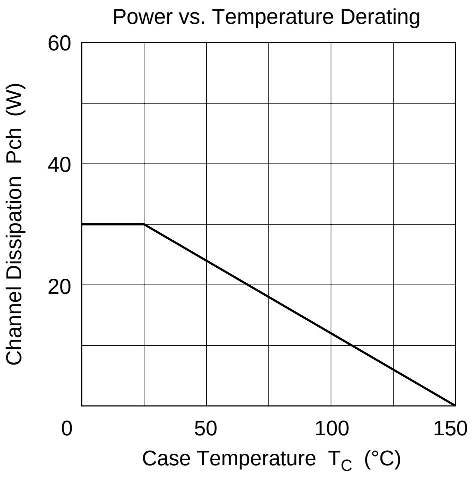
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

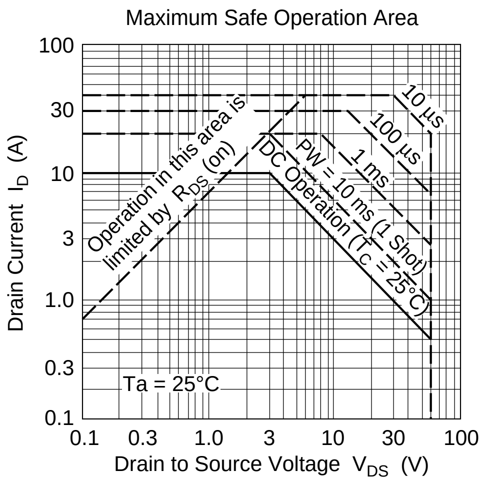
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

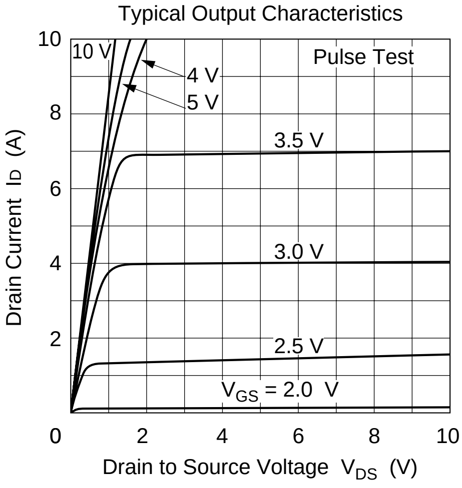
Table 2 Electrical Characteristics (Ta = 25°C)

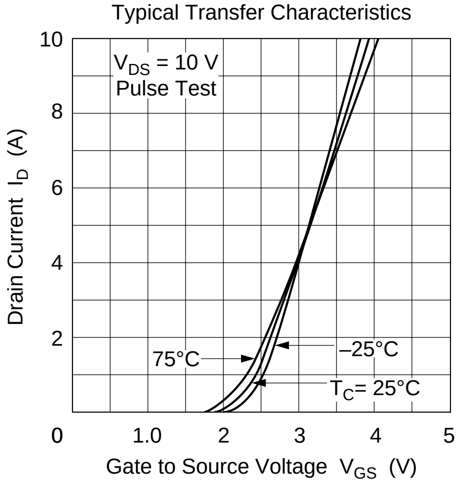
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 5 A, V_{GS} = 10 V *
			0.17	0.22		I_D = 5 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	6.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	220	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	60	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time	t_r	—	55	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	140	—	ns	
Fall time	t_f	—	90	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	125	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

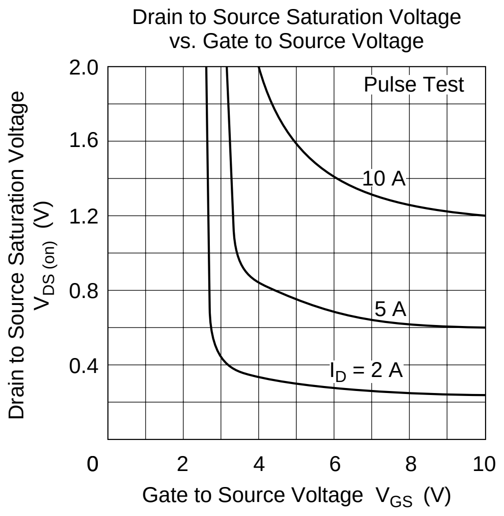
* Pulse Test

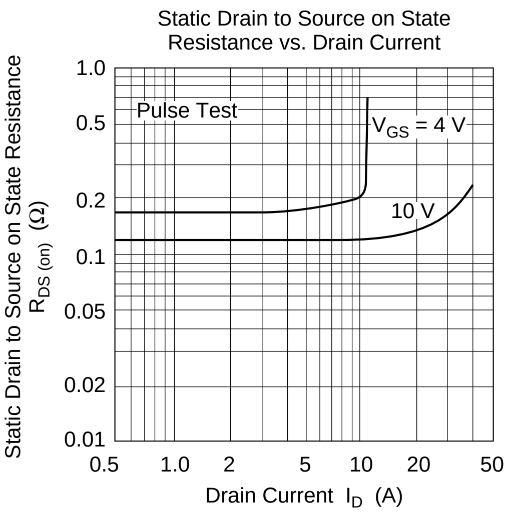

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

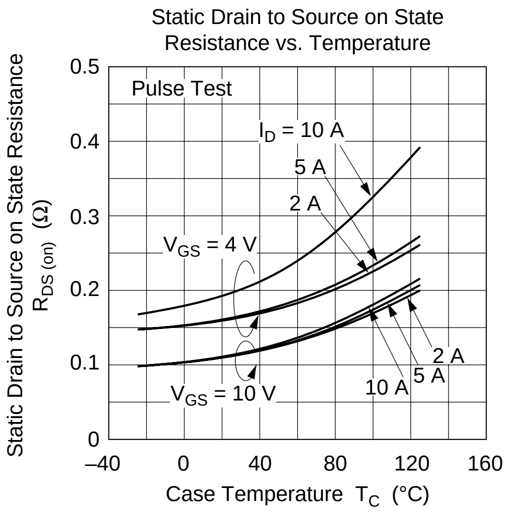

Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
Operation in this area is limited by R_{DS} (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)

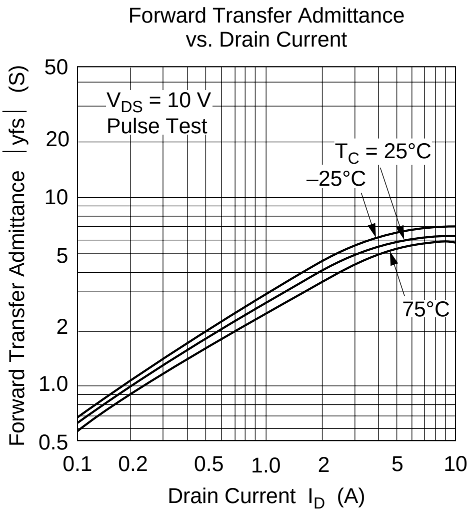

Typical Output Characteristics
Drain Current I_D (A)
10
8
6
4
2
0
10 V
4 V
5 V
Pulse Test
3.5 V
3.0 V
2.5 V
V_{GS} = 2.0 V
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)

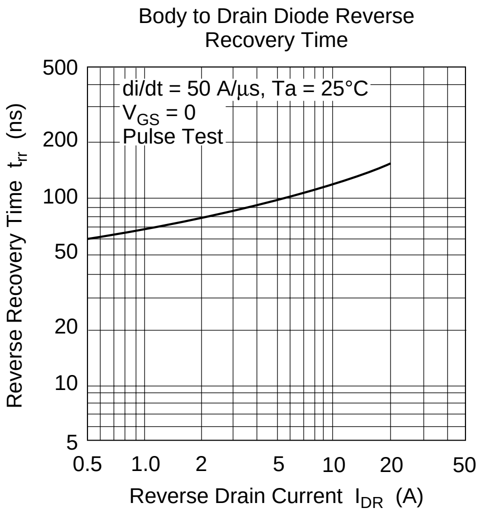

Typical Transfer Characteristics
Drain Current I_D (A)
10
8
6
4
2
0
V_{DS} = 10 V
Pulse Test
75°C
–25°C
T_C= 25°C
1.0
2
3
4
5
Gate to Source Voltage V_{GS} (V)

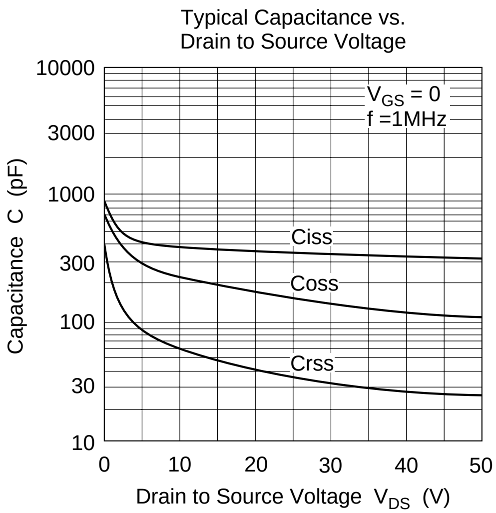

Drain to Source Saturation Voltage vs. Gate to Source Voltage
Pulse Test
10 A
5 A
I_D = 2 A
Drain to Source Saturation Voltage $V_{DS\,(on)}$ (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

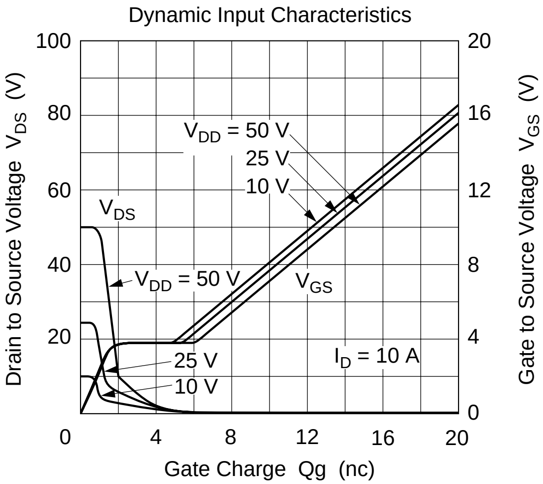

Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
V_{GS} = 4 V
10 V
Static Drain to Source on State Resistance $R_{DS\,(on)}$ (Ω)
1.0
0.5
0.2
0.1
0.05
0.02
0.01
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)

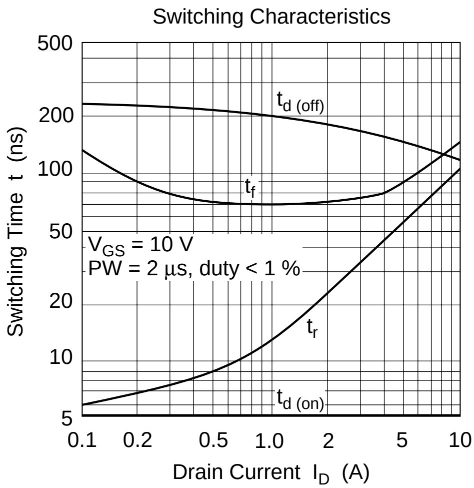

Static Drain to Source on State Resistance vs. Temperature
Pulse Test
I_D = 10 A
5 A
2 A
V_{GS} = 4 V
V_{GS} = 10 V
10 A
5 A
2 A
Static Drain to Source on State Resistance $R_{DS\,(on)}$ (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature T_C (°C)

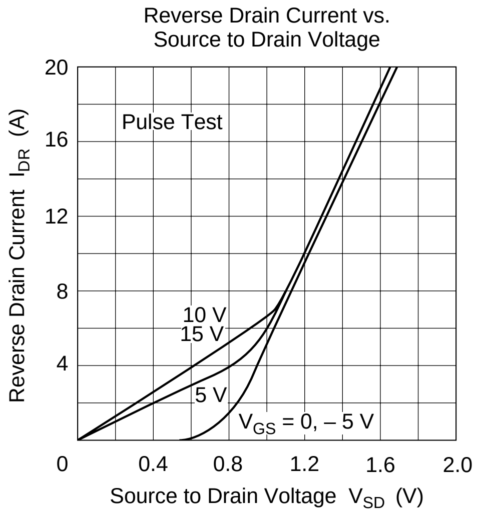

Forward Transfer Admittance vs. Drain Current
V_{DS} = 10 V
Pulse Test
T_C = 25°C
–25°C
75°C
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1.0
0.5
0.1
0.2
0.5
1.0
2
5
10
Drain Current I_D (A)

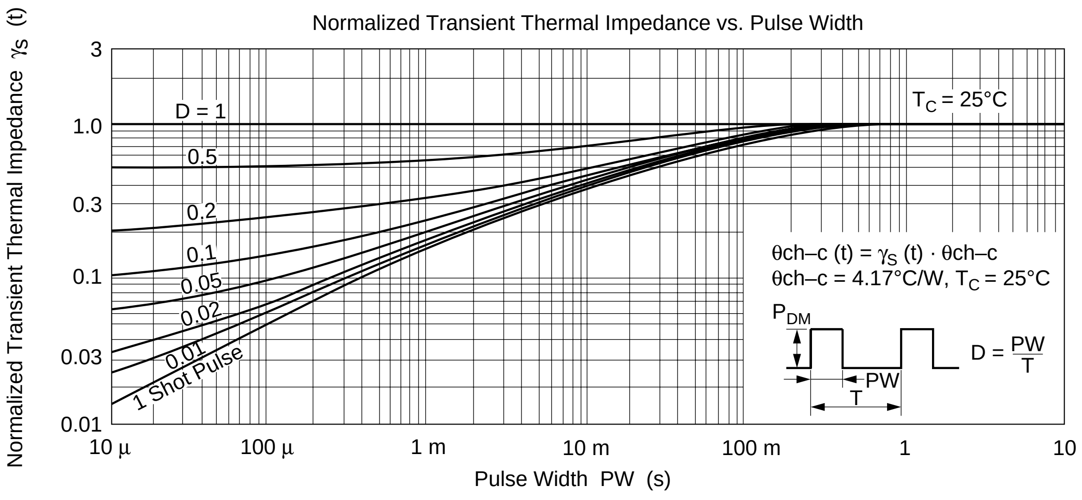

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/μs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.5
1.0
2
5
10
20
50
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f =1MHz
Ciss
Coss
Crss
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

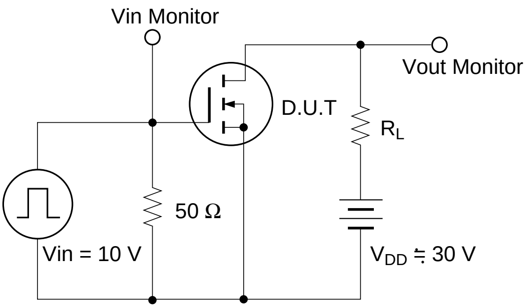

Dynamic Input Characteristics
VDD = 50 V
25 V
10 V
VDS
VDD = 50 V
VGS
25 V
10 V
ID = 10 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
4
8
12
16
20
Gate Charge Qg (nc)


Switching Characteristics
td (off)
tf
VGS = 10 V
PW = 2 μs, duty < 1 %
tr
td (on)
Switching Time t (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1.0
2
5
10
Drain Current ID (A)

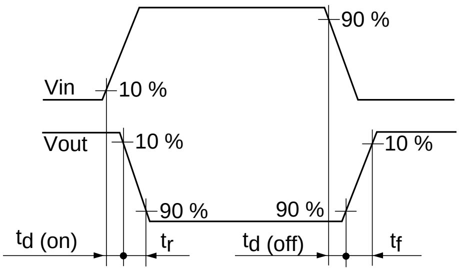

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
V_{GS} = 0, – 5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
4
8
12
16
20


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 4.17°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



Silicon N-Channel MOS FET

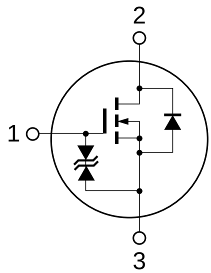
Application

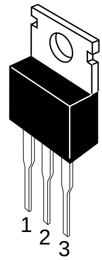
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

TO–220AB





1. Gate
2. Drain
   (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

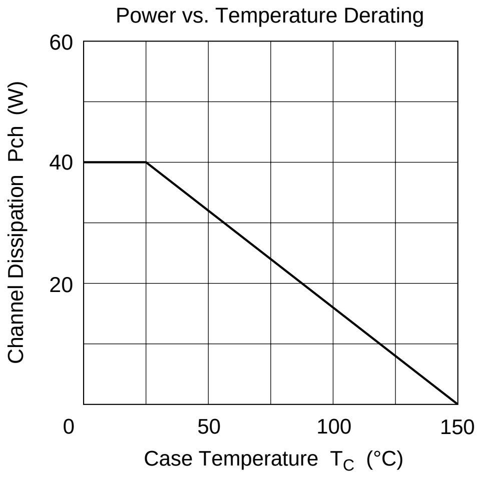
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body to drain diode reverse drain current	I_{DR}	15	A
Channel dissipation	Pch**	40	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

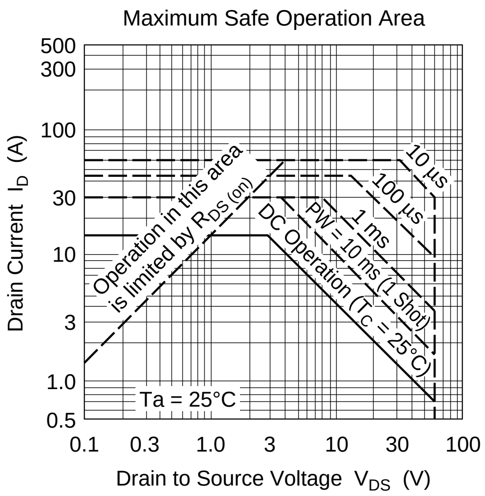
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.055	0.065	Ω	I_D = 8 A, V_{GS} = 10 V *
			0.075	0.095		I_D = 8 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = 8 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	450	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	140	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 8 A, V_{GS} = 10 V,
Rise time	t_r	—	70	—	ns	R_L = 3.75 Ω
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	
Fall time	t_f	—	120	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 15 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 50 A/µs

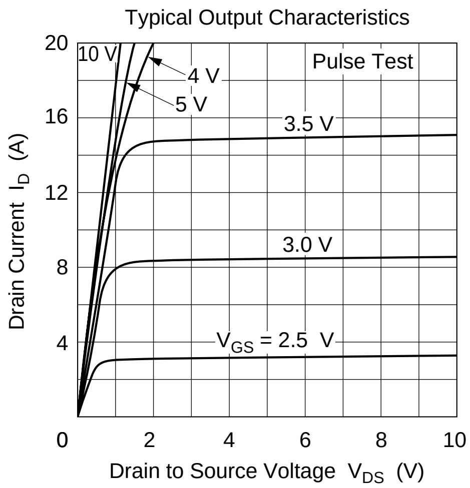
* Pulse Test



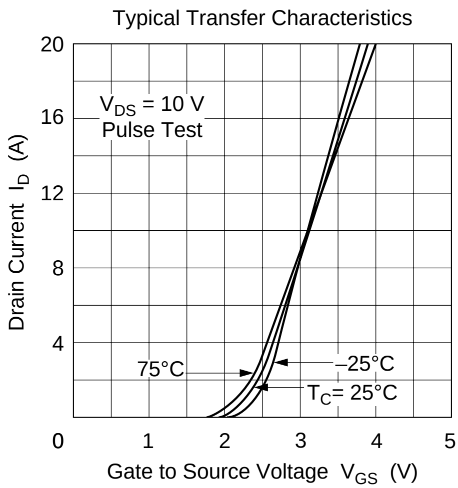
Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)



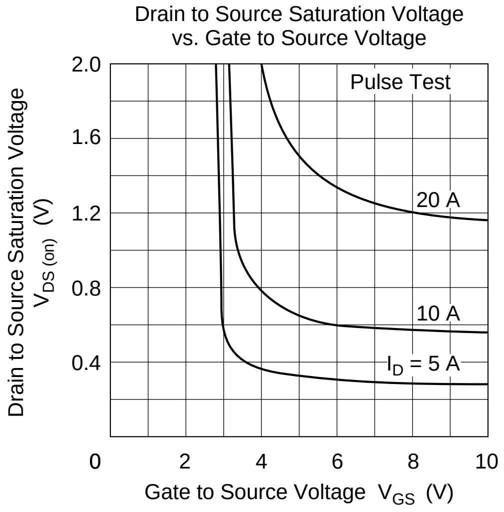
Maximum Safe Operation Area
Drain Current I_D (A)
500
300
100
30
10
3
1.0
0.5
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)
Operation in this area is limited by $R_{DS (on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C

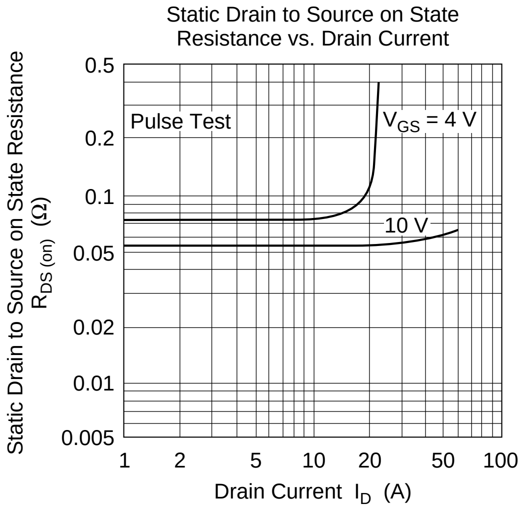


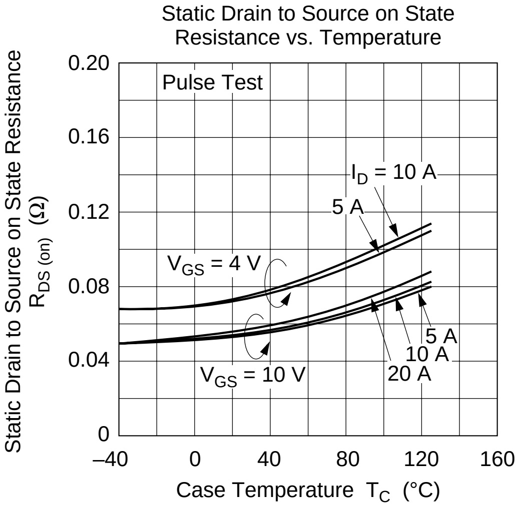
Typical Output Characteristics
Drain Current I_D (A)
20
16
12
8
4
0
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)
10 V
4 V
5 V
Pulse Test
3.5 V
3.0 V
V_{GS} = 2.5 V

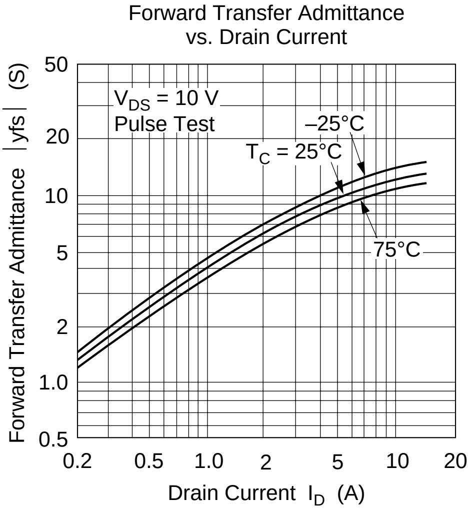


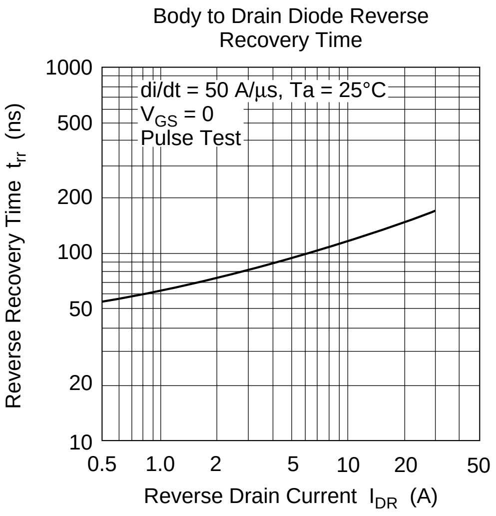
Typical Transfer Characteristics
Drain Current I_D (A)
20
16
12
8
4
0
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
75°C
–25°C
T_C= 25°C

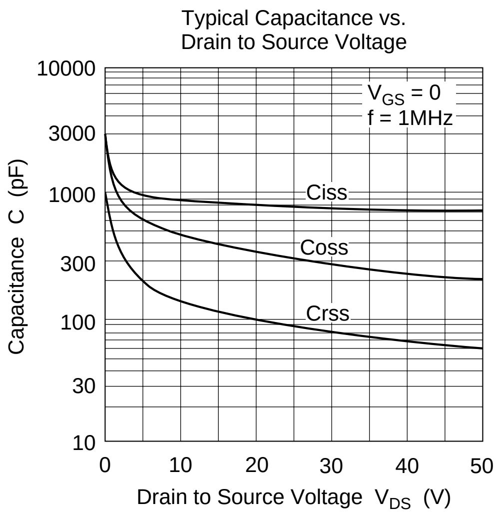

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
20 A
10 A
I_D = 5 A
Drain to Source Saturation Voltage
$V_{DS (on)}$ (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

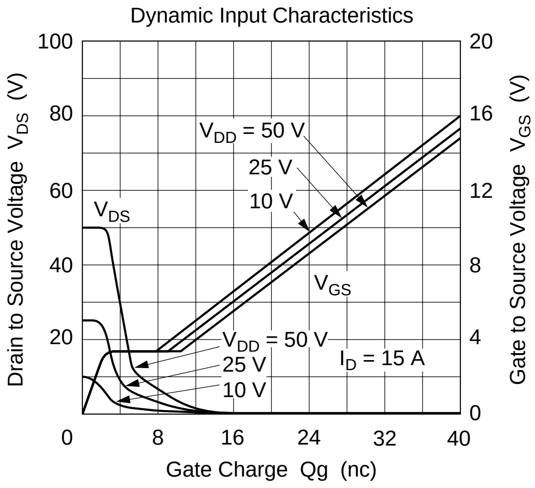

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 4 V
10 V
Static Drain to Source on State Resistance
$R_{DS (on)}$ (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
1
2
5
10
20
50
100
Drain Current I_D (A)

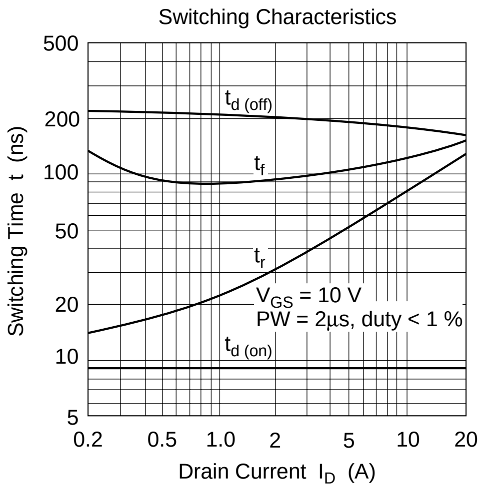

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 10 A
5 A
V_{GS} = 4 V
V_{GS} = 10 V
5 A
10 A
20 A
Static Drain to Source on State Resistance
$R_{DS (on)}$ (Ω)
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature T_C (°C)

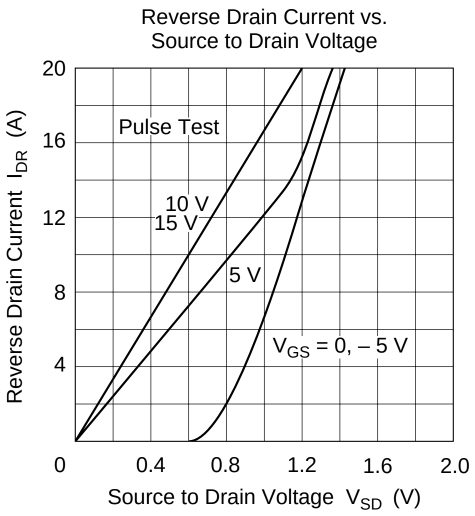

Forward Transfer Admittance
vs. Drain Current
V_{DS} = 10 V
Pulse Test
–25°C
T_C = 25°C
75°C
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1.0
0.5
0.2
0.5
1.0
2
5
10
20
Drain Current I_D (A)

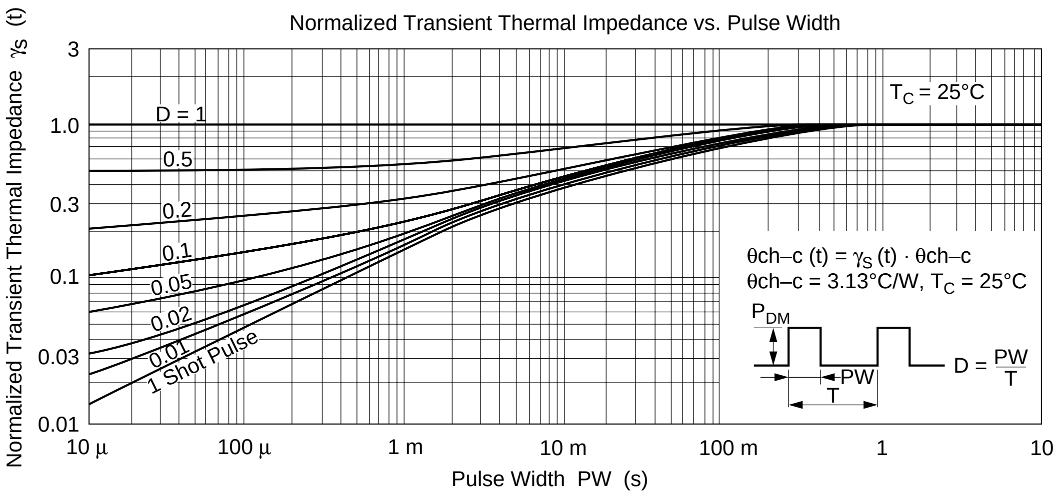

Body to Drain Diode Reverse
Recovery Time
di/dt = 50 A/µs, Ta = 25°C
V_{GS} = 0
Pulse Test
Reverse Recovery Time t_{rr} (ns)
1000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Reverse Drain Current I_{DR} (A)

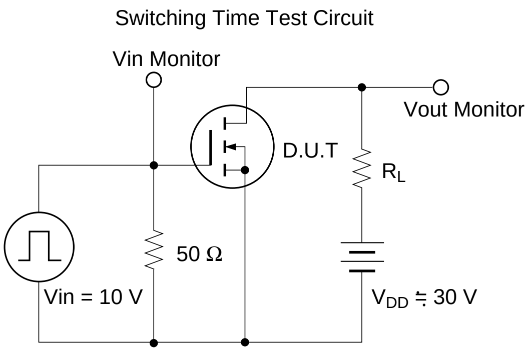

Typical Capacitance vs.
Drain to Source Voltage
V_{GS} = 0
f = 1MHz
Ciss
Coss
Crss
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)

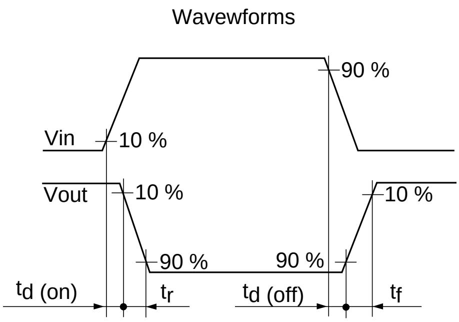

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
100
80
60
40
20
0
20
16
12
8
4
0
V_{DD} = 50 V
25 V
10 V
V_{DS}
V_{GS}
V_{DD} = 50 V
25 V
10 V
I_D = 15 A
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
$t_{d\ (off)}$
t_f
t_r
V_{GS} = 10 V
PW = 2µs, duty < 1 %
$t_{d\ (on)}$
0.2
0.5
1.0
2
5
10
20
Drain Current I_D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
V_{GS} = 0, – 5 V
Reverse Drain Current I_{DR} (A)
20
16
12
8
4
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 3.13°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T
RL
50 Ω
Vin = 10 V
VDD ≒ 30 V


Wavewforms
90 %
Vin
10 %
Vout
10 %
10 %
90 %
90 %
td (on)
tr
td (off)
tf

2SK972

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

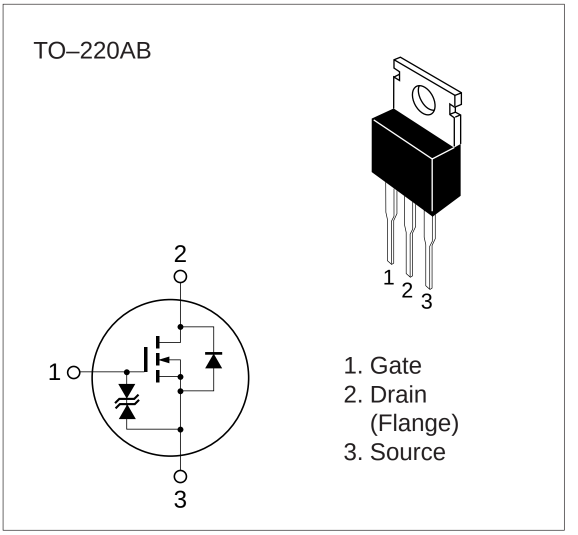


Table 1 Absolute Maximum Ratings (Ta = 25°C)

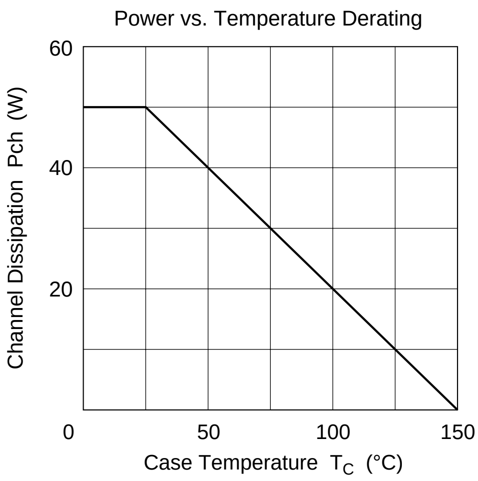
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$*	100	A
Body to drain diode reverse drain current	I_{DR}	25	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

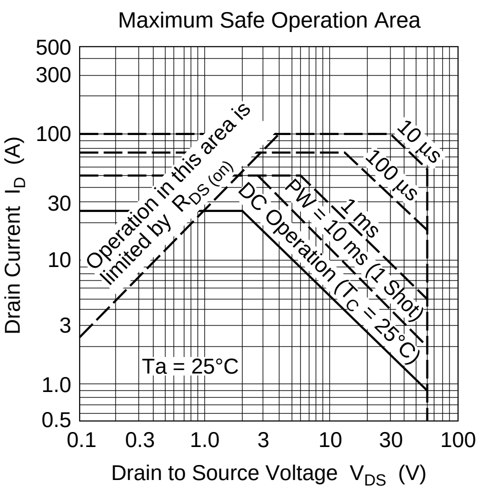
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

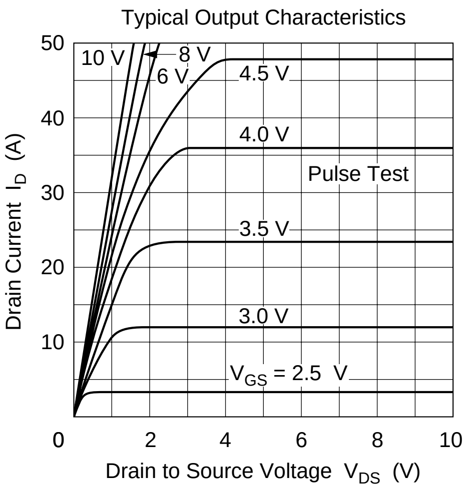
Table 2 Electrical Characteristics (Ta = 25°C)

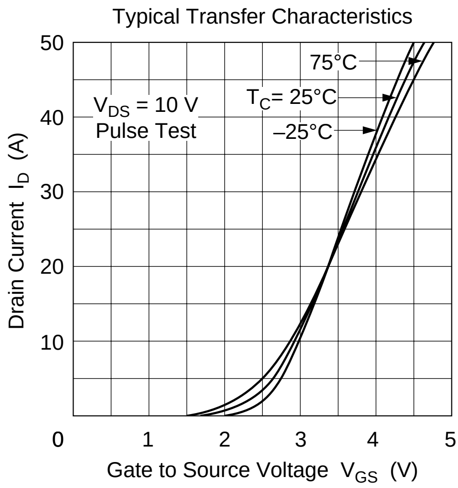
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.04	Ω	I_D = 15 A, V_{GS} = 10 V *
			0.05	0.06		I_D = 15 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	20	—	S	I_D = 15 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	720	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	220	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 15 A, V_{GS} = 10 V,
Rise time	t_r	—	130	—	ns	R_L = 2 Ω
Turn-off delay time	$t_{d(off)}$	—	270	—	ns	
Fall time	t_f	—	180	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 25 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 25 A, V_{GS} = 0, di_F/dt = 50 A/µs

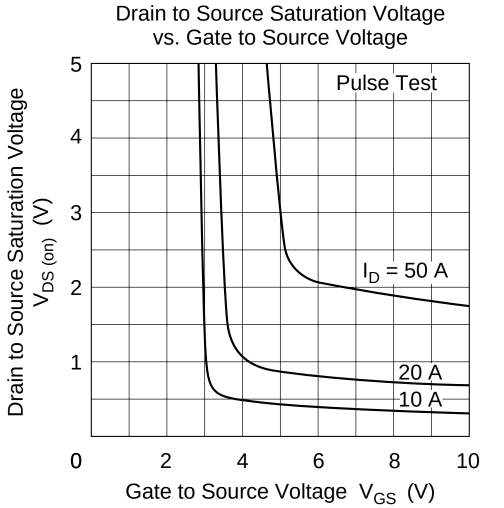
* Pulse Test

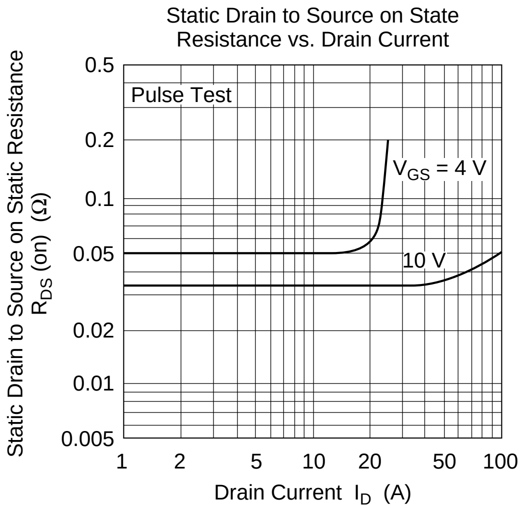

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

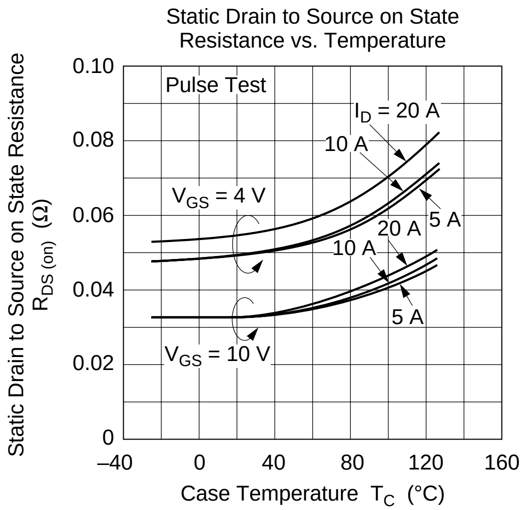

Maximum Safe Operation Area
Drain Current I_D (A)
500
300
100
30
10
3
1.0
0.5
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)
Operation in this area is limited by $R_{DS(on)}$
10 µs
100 µs
PW = 1 ms
10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C

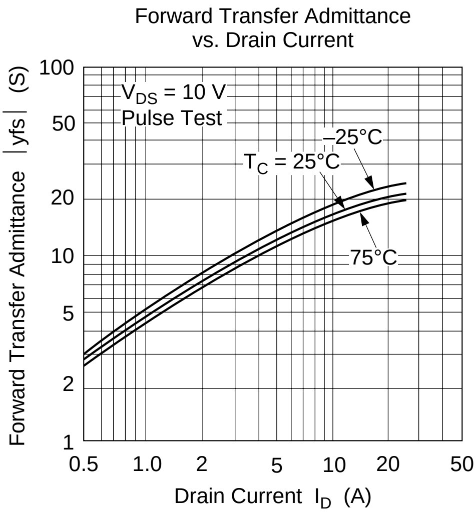

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)
10 V
8 V
6 V
4.5 V
4.0 V
Pulse Test
3.5 V
3.0 V
V_{GS} = 2.5 V

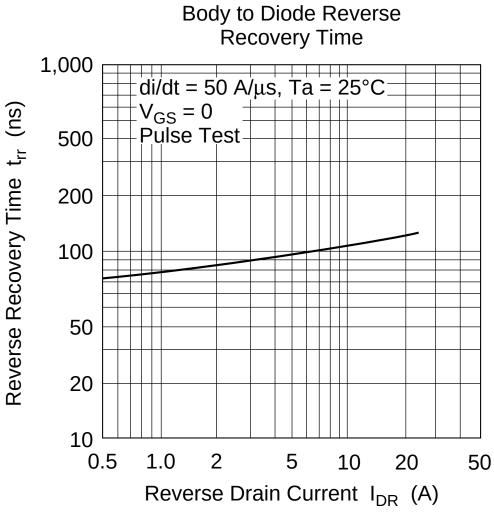

Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
75°C
T_C= 25°C
–25°C

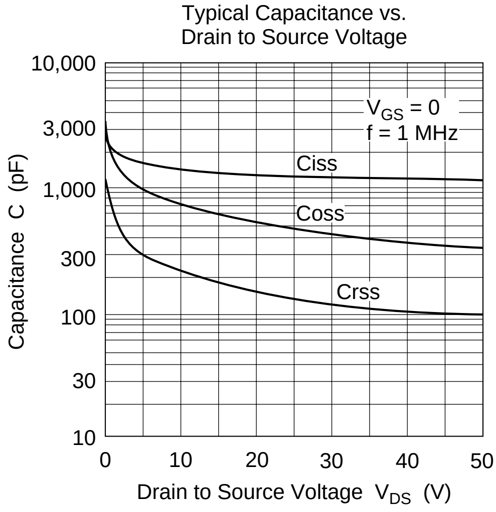

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 50 A
20 A
10 A
Drain to Source Saturation Voltage V_DS (on) (V)
Gate to Source Voltage V_GS (V)
0
1
2
3
4
5
6
8
10

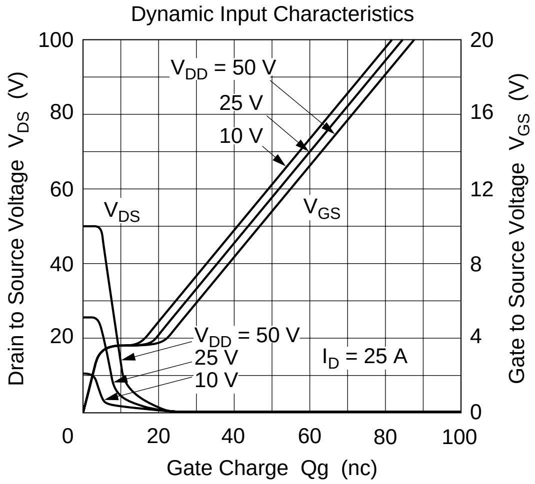

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_GS = 4 V
10 V
Static Drain to Source on Static Resistance R_DS (on) (Ω)
Drain Current I_D (A)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
1
2
5
10
20
50
100

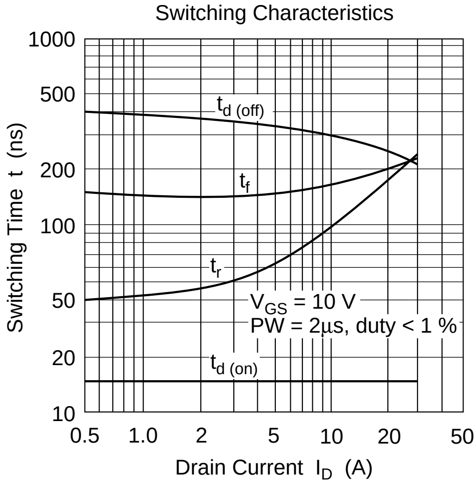

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 20 A
10 A
5 A
V_GS = 4 V
20 A
10 A
5 A
V_GS = 10 V
Static Drain to Source on State Resistance R_DS (on) (Ω)
Case Temperature T_C (°C)
0.10
0.08
0.06
0.04
0.02
0
–40
40
80
120
160

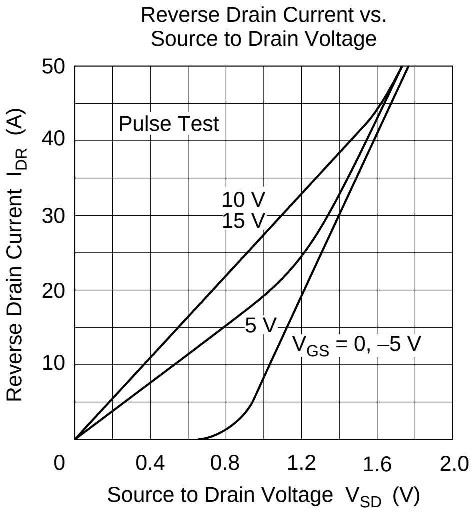

Forward Transfer Admittance
vs. Drain Current
V_DS = 10 V
Pulse Test
–25°C
T_C = 25°C
75°C
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
100
50
20
10
5
2
1
0.5
1.0
2
5
10
20
50

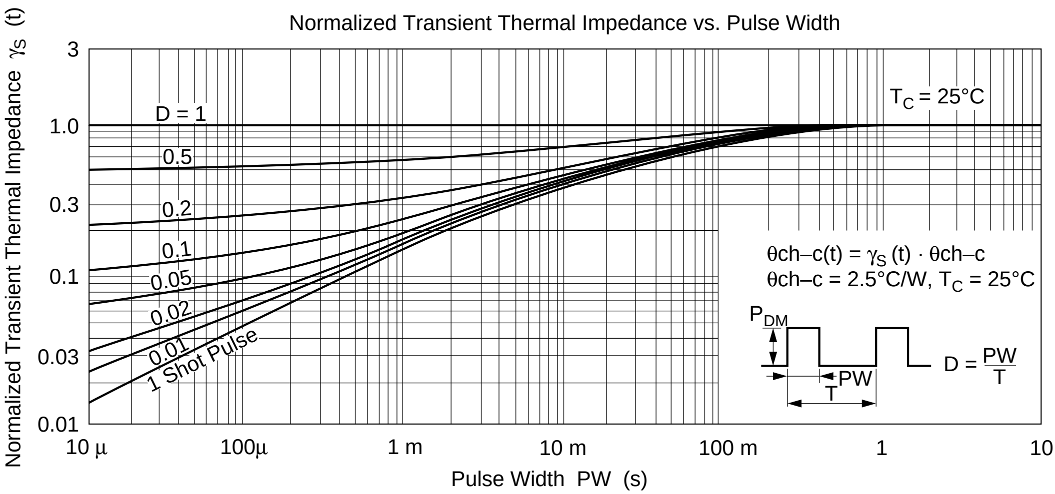

Body to Diode Reverse Recovery Time
di/dt = 50 A/µs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
1,000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10,000
3,000
1,000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

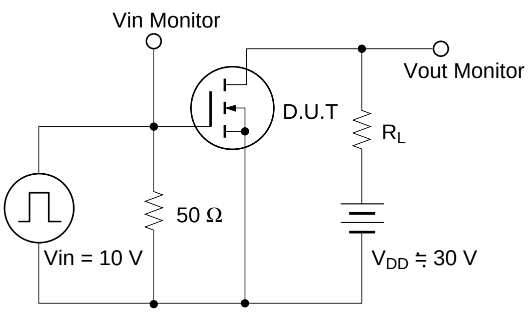

Dynamic Input Characteristics
VDD = 50 V
25 V
10 V
VDS
VGS
VDD = 50 V
25 V
10 V
ID = 25 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
td (off)
tf
tr
VGS = 10 V
PW = 2µs, duty < 1 %
td (on)
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Drain Current ID (A)

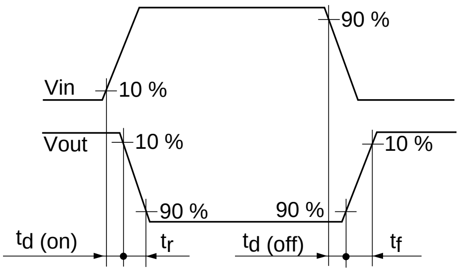

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
VGS = 0, –5 V
Reverse Drain Current IDR (A)
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage VSD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
TC = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c(t) = γS (t) · θch–c
θch–c = 2.5°C/W, TC = 25°C
PDM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γS (t)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit



Wavewforms



2SK973(L), 2SK973(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

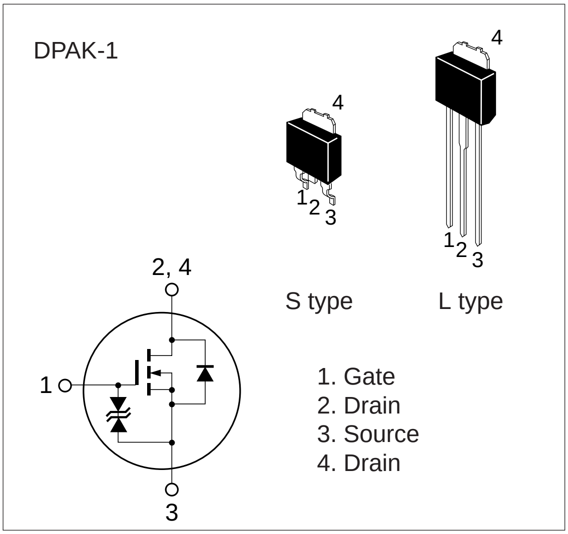


Table 1 Absolute Maximum Ratings (Ta = 25°C)

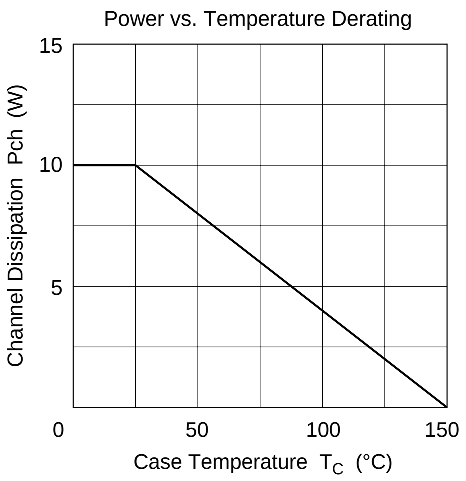
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	2	A
Drain peak current	$I_{D(peak)}$*	8	A
Body to drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch**	10	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

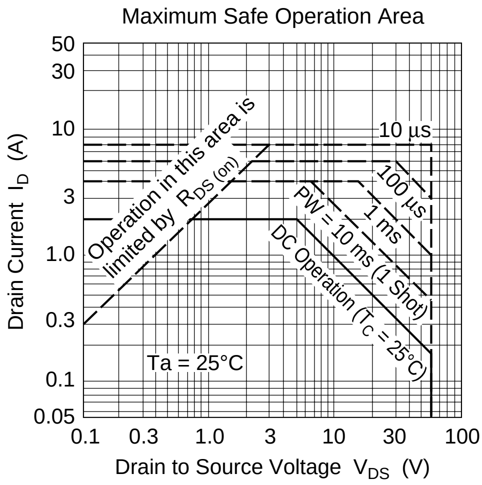
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

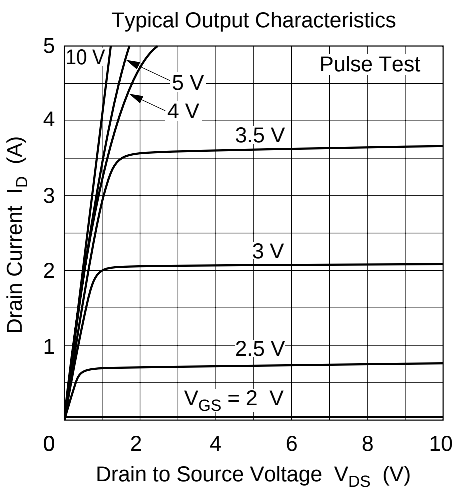
Table 2 Electrical Characteristics (Ta = 25°C)

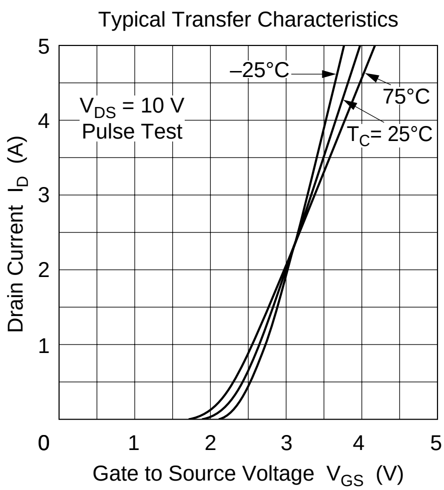
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.35	Ω	I_D = 1 A, V_{GS} = 10 V *
			0.40	0.50		I_D = 1 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = 1 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	240	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	115	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	35	—	pF	
Turn-on delay time	$t_{d(on)}$	—	4	—	ns	I_D = 1 A, V_{GS} = 10 V,
Rise time	t_r	—	15	—	ns	R_L = 30 Ω
Turn-off delay time	$t_{d(off)}$	—	80	—	ns	
Fall time	t_f	—	40	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 2 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	70	—	ns	I_F = 2 A, V_{GS} = 0, di_F/dt = 50 A/µs

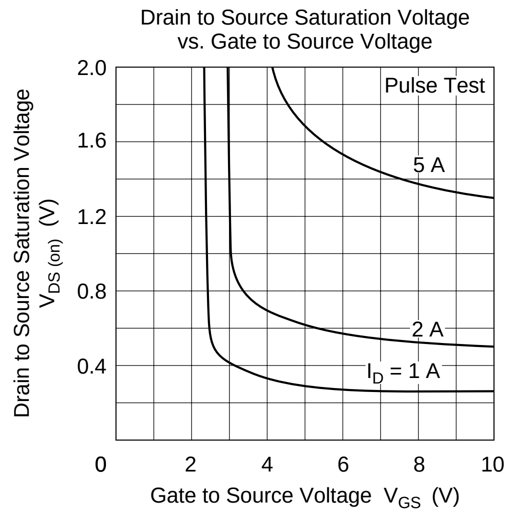
* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
15
10
5
0
50
100
150
Case Temperature T_C (°C)

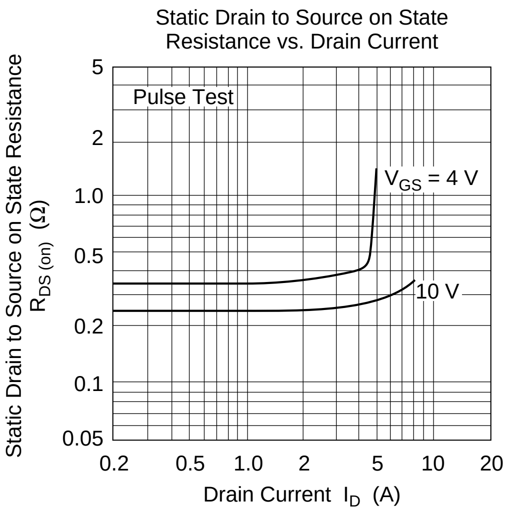

Maximum Safe Operation Area
Drain Current I_D (A)
50
30
10
3
1.0
0.3
0.1
0.05
Operation in this area is limited by $R_{DS (on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)


Typical Output Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
10 V
5 V
4 V
Pulse Test
3.5 V
3 V
2.5 V
V_{GS} = 2 V
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)

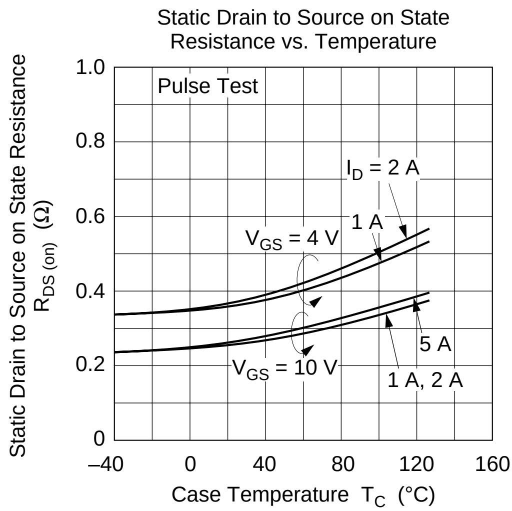

Typical Transfer Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
–25°C
75°C
V_{DS} = 10 V
Pulse Test
T_C= 25°C
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)



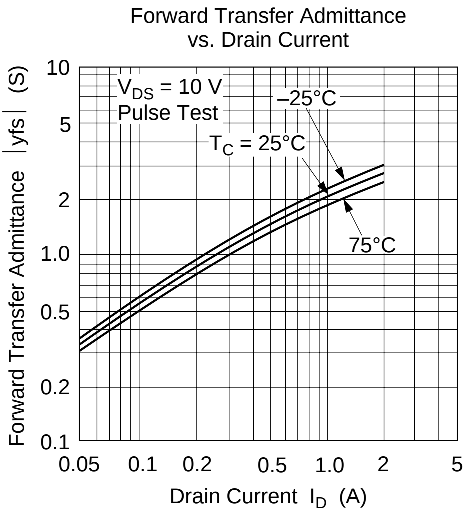
Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
V_DS (on) (V)
Gate to Source Voltage V_GS (V)
Pulse Test
5 A
2 A
I_D = 1 A
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10



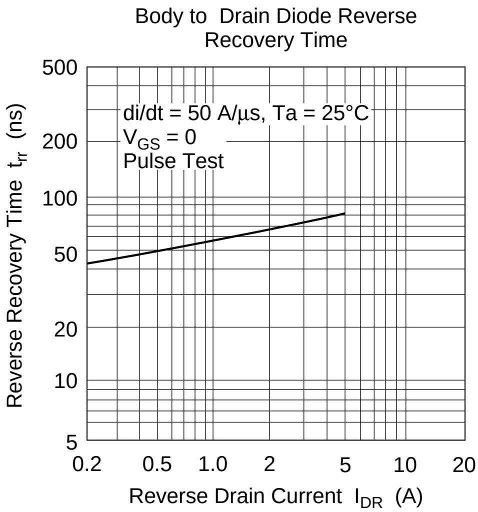
Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
R_DS (on) (Ω)
Drain Current I_D (A)
Pulse Test
V_GS = 4 V
10 V
5
2
1.0
0.5
0.2
0.1
0.05
0.2
0.5
1.0
2
5
10
20

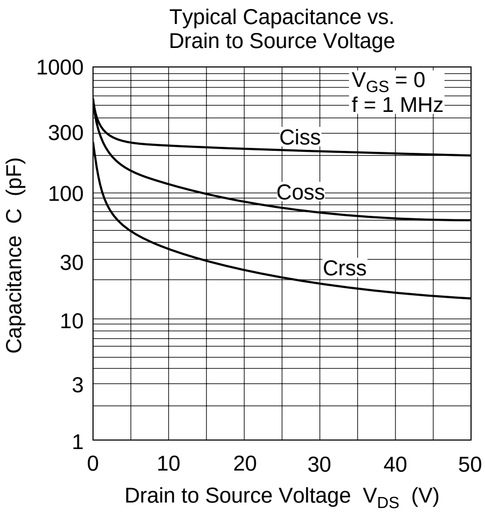


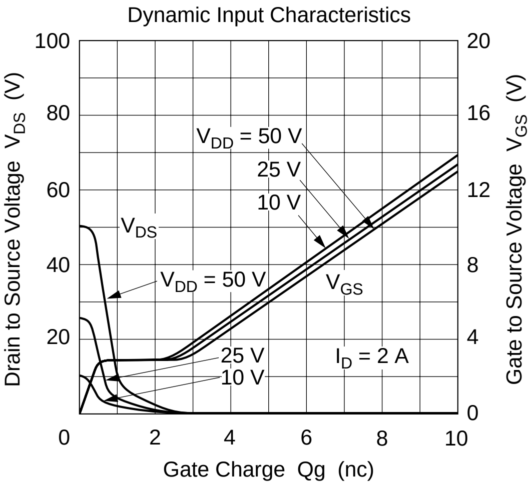
Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
R_DS (on) (Ω)
Case Temperature T_C (°C)
Pulse Test
I_D = 2 A
1 A
V_GS = 4 V
5 A
V_GS = 10 V
1 A, 2 A
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160

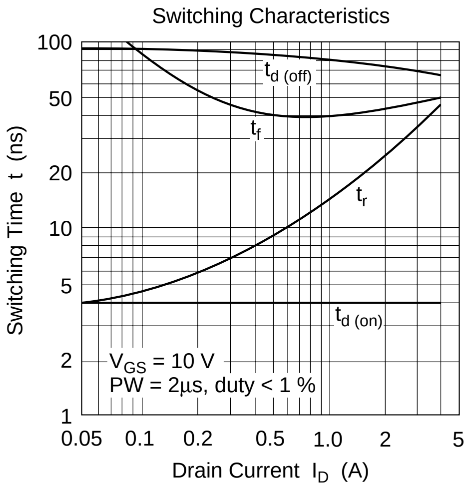


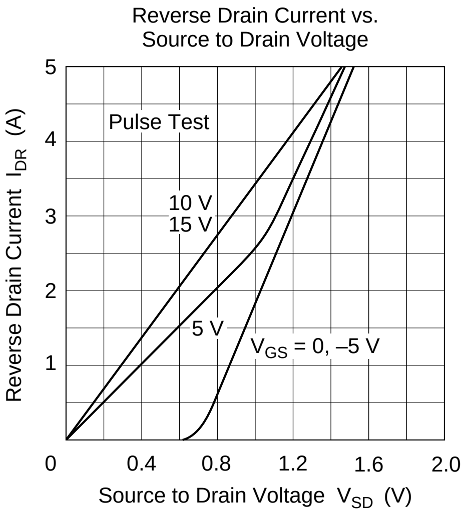
Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
V_DS = 10 V
Pulse Test
–25°C
T_C = 25°C
75°C
10
5
2
1.0
0.5
0.2
0.1
0.05
0.1
0.2
0.5
1.0
2
5

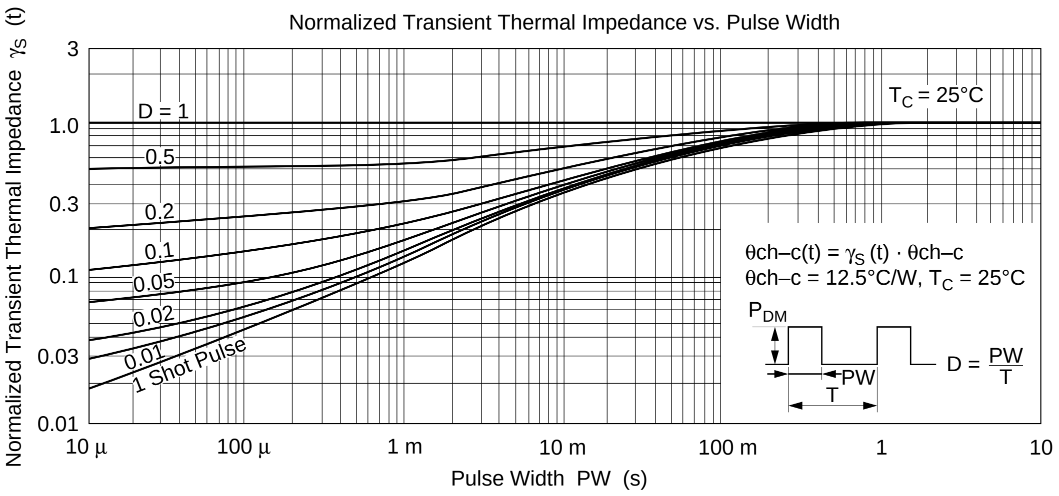

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/μs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.2
0.5
1.0
2
5
10
20
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
1000
300
100
30
10
3
1
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

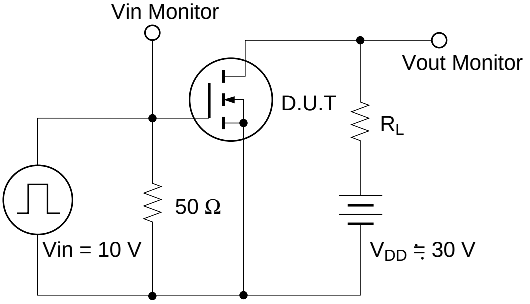

Dynamic Input Characteristics
VDD = 50 V
25 V
10 V
VDS
VDD = 50 V
VGS
25 V
10 V
ID = 2 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
20
16
12
8
4
0
0
2
4
6
8
10
Gate Charge Qg (nc)


Switching Characteristics
td (off)
tf
tr
td (on)
VGS = 10 V
PW = 2μs, duty < 1 %
Switching Time t (ns)
100
50
20
10
5
2
1
0.05
0.1
0.2
0.5
1.0
2
5
Drain Current ID (A)

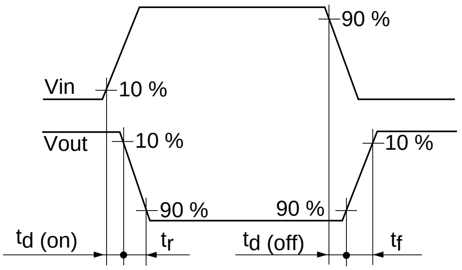

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
0
1
2
3
4
5
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c(t) = γ_S (t) · θch–c
θch–c = 12.5°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit



Wavewforms



2SK974L, 2SK974S

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

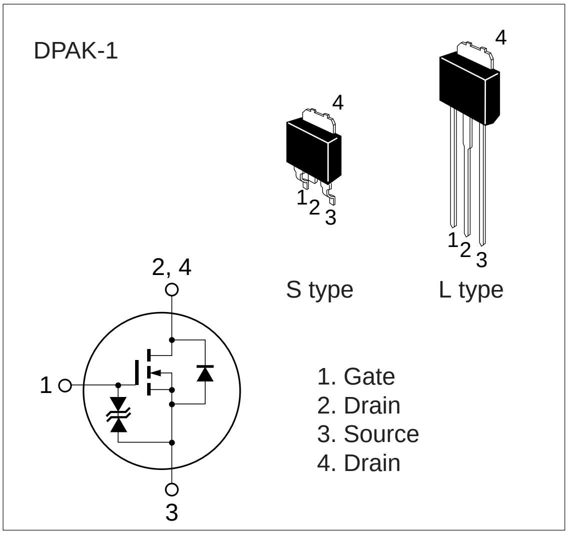


Table 1 Absolute Maximum Ratings (Ta = 25°C)

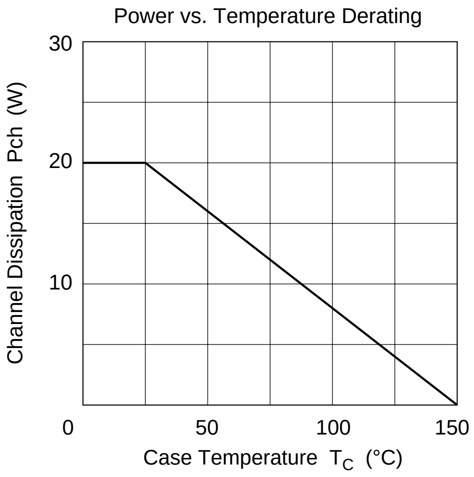
Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	3	A
Drain peak current	$I_{D(peak)}$*	12	A
Body to drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

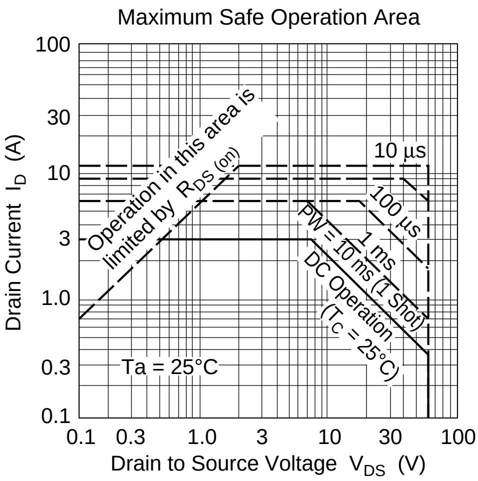
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

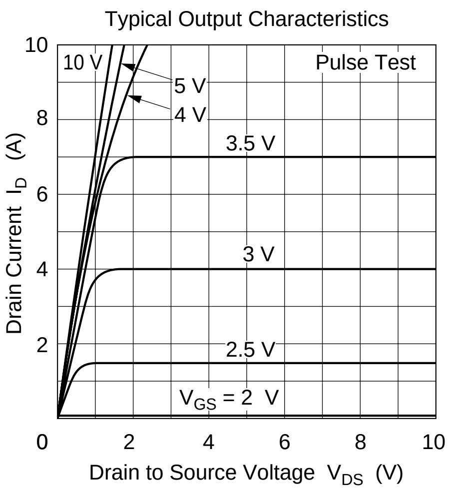
Table 2 Electrical Characteristics (Ta = 25°C)

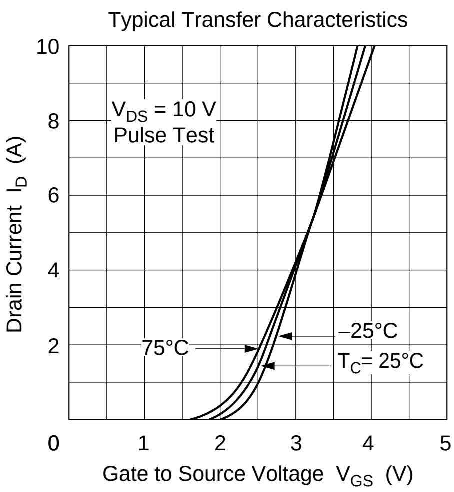
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.15	0.18	Ω	I_D = 2 A, V_{GS} = 10 V *
			0.20	0.25		I_D = 2 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	2.4	4.0	—	S	I_D = 2 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	230	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	60	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 2 A, V_{GS} = 10 V,
Rise time	t_r	—	25	—	ns	R_L = 15 Ω
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	
Fall time	t_f	—	75	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 3 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	85	—	ns	I_F = 3 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

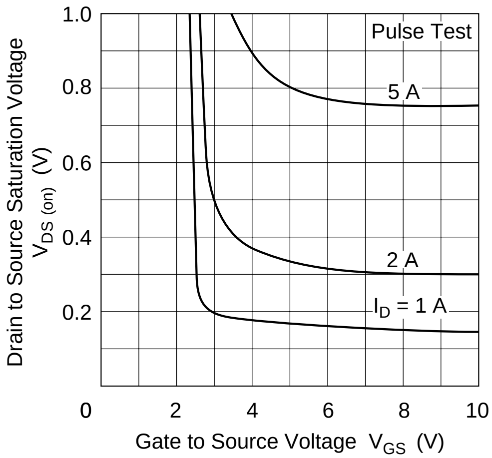

Power vs. Temperature Derating
30
20
10
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)


Maximum Safe Operation Area
100
30
10
3
1.0
0.3
0.1
Operation in this area is limited by $R_{DS\,(on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C
0.1
0.3
1.0
3
10
30
100
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

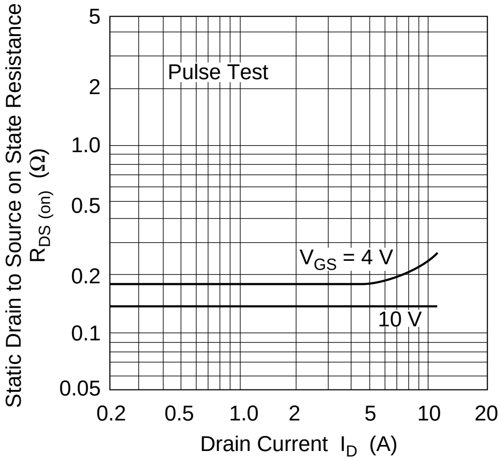

Typical Output Characteristics
10
8
6
4
2
0
10 V
5 V
4 V
Pulse Test
3.5 V
3 V
2.5 V
V_{GS} = 2 V
2
4
6
8
10
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
10
8
6
4
2
0
V_{DS} = 10 V
Pulse Test
75°C
–25°C
T_C= 25°C
1
2
3
4
5
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

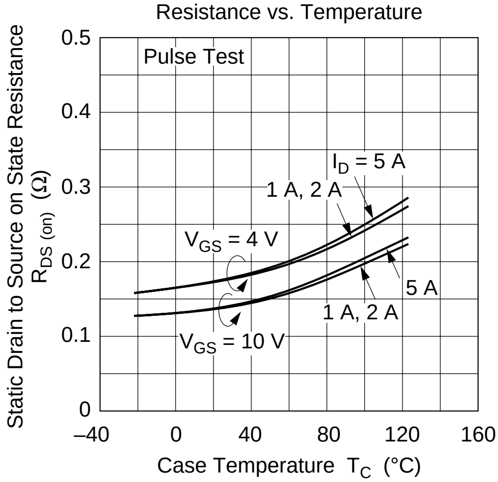
Drain to Source Saturation Voltage vs. Gate to Source Voltage



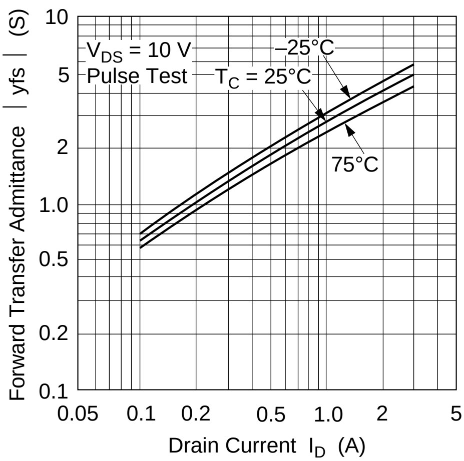
Static Drain to Source on State Resistance vs. Drain Current

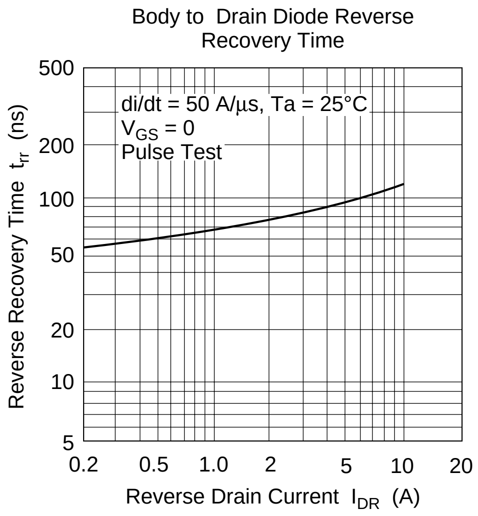


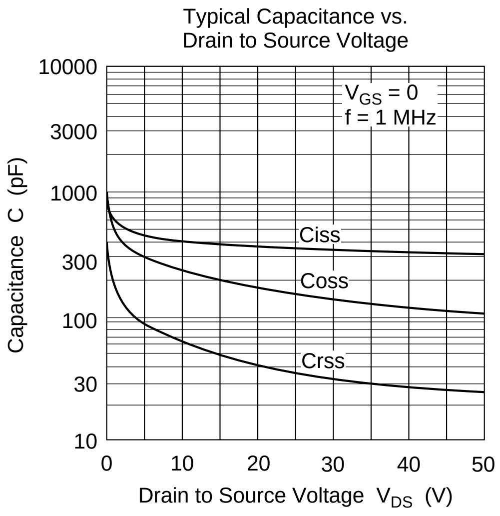
Static Drain to Source on State Resistance vs. Temperature

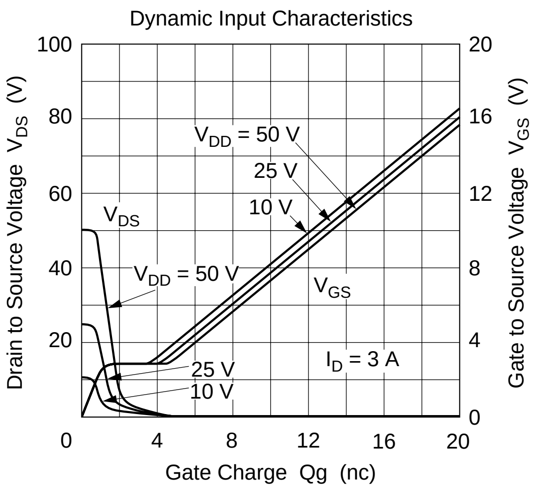


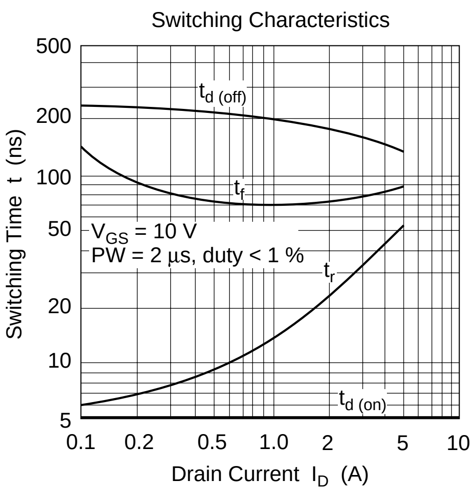
Forward Transfer Admittance vs. Drain Current

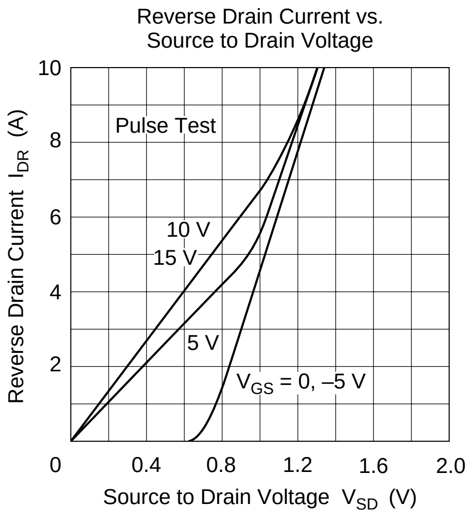


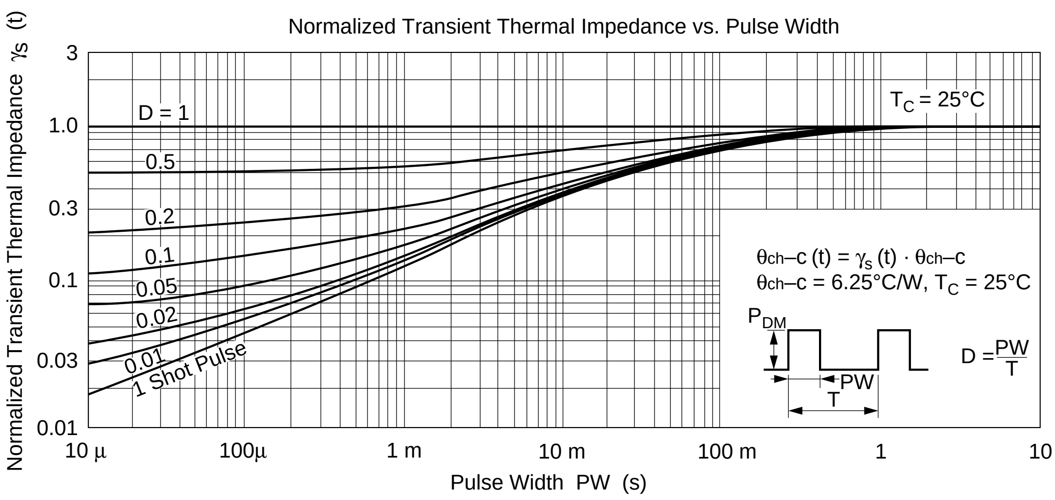

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.2
0.5
1.0
2
5
10
20
Reverse Drain Current IDR (A)

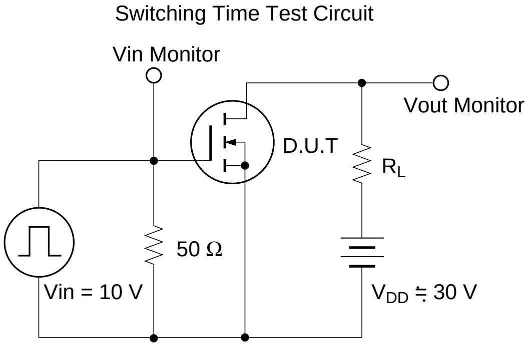

Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

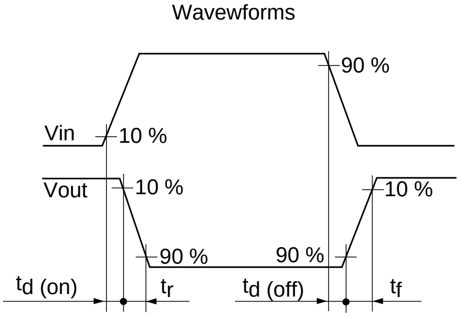

Dynamic Input Characteristics
VDD = 50 V
25 V
10 V
VDS
VDD = 50 V
25 V
10 V
VGS
ID = 3 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
0
4
8
12
16
20
Gate Charge Qg (nc)


Switching Characteristics
td (off)
tf
VGS = 10 V
PW = 2 µs, duty < 1 %
tr
td (on)
Switching Time t (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1.0
2
5
10
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
V_GS = 0, –5 V
Reverse Drain Current I_DR (A)
Source to Drain Voltage V_SD (V)
0
0.4
0.8
1.2
1.6
2.0
2
4
6
8
10


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γs (t) · θch–c
θch–c = 6.25°C/W, T_C = 25°C
P_DM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (s)
10 µ
100µ
1 m
10 m
100 m
1
10
3
1.0
0.3
0.1
0.03
0.01


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T
RL
50 Ω
Vin = 10 V
VDD ≒ 30 V

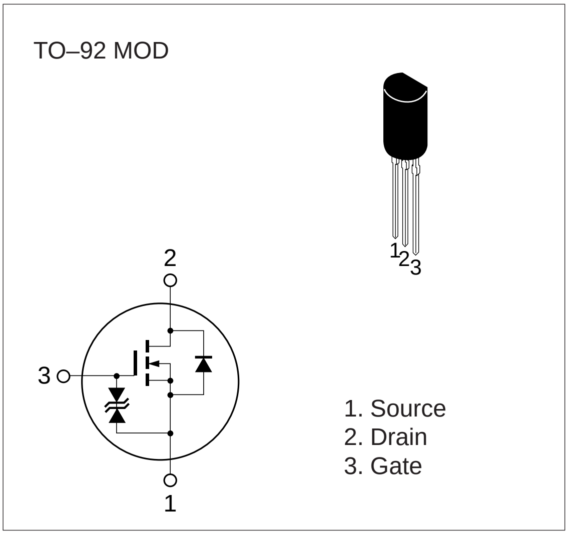

Wavewforms
Vin
Vout
90 %
10 %
10 %
10 %
90 %
90 %
td (on)
tr
td (off)
tf

2SK975

Silicon N-Channel MOS FET

Application

High speed power switching



Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

Table 1 Absolute Maximum Ratings (Ta = 25°C)

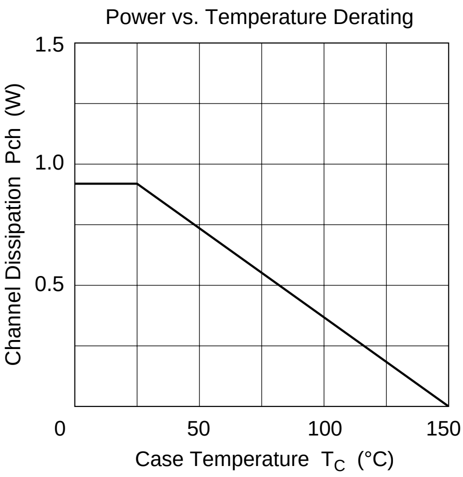
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	1.5	A
Drain peak current	$I_{D(pulse)}$*	4.5	A
Body to drain diode reverse drain current	I_{DR}	1.5	A
Channel dissipation	Pch	900	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

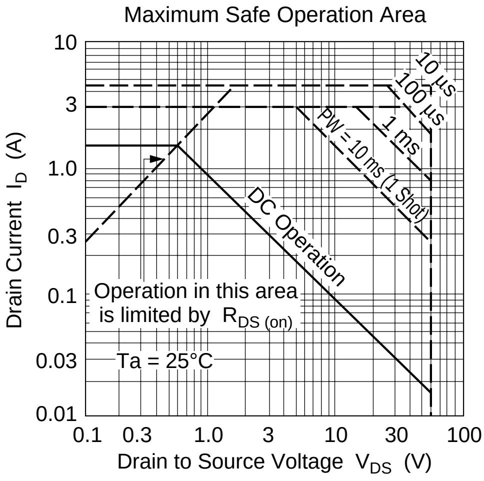
* PW ≤ 10 µs, duty cycle ≤ 1 %

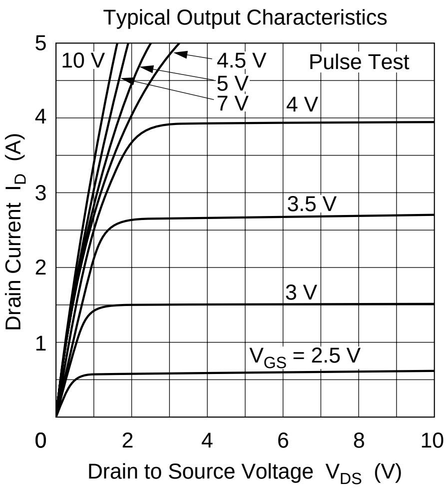
Table 2 Electrical Characteristics (Ta = 25°C)

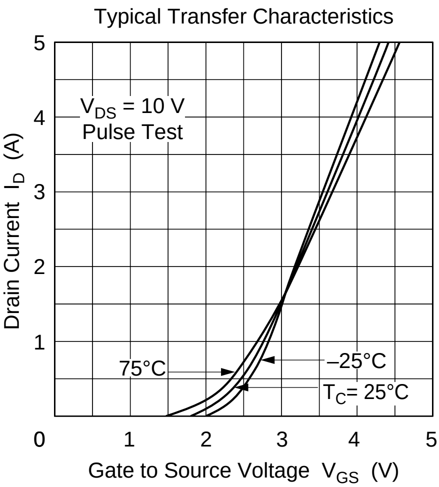
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(off)}$	—	0.3	0.4	Ω	I_D = 1 A, V_{GS} = 10 V *
			0.4	0.55		I_D = 1 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.9	1.5	—	S	I_D = 1 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	140	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	70	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	20	—	pF	
Turn-on delay time	$t_{d(on)}$	—	3	—	ns	I_D = 1 A, V_{GS} = 10 V,
Rise time	t_r	—	12	—	ns	R_L = 30 Ω
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	30	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 1.5 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = 1.5 A, V_{GS} = 0, di_F/dt = 50 A/µs

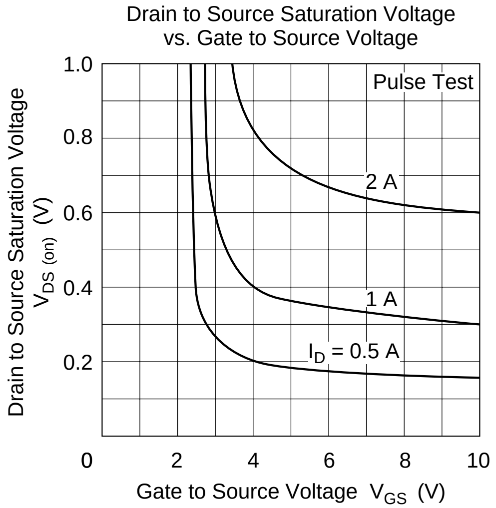
* Pulse Test

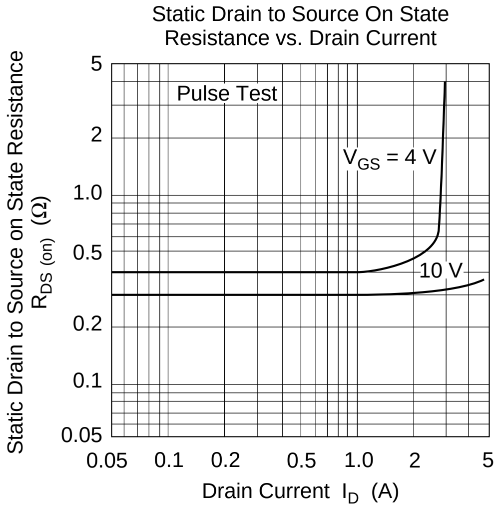

Power vs. Temperature Derating
Channel Dissipation Pch (W)
1.5
1.0
0.5
0
50
100
150
Case Temperature T_C (°C)

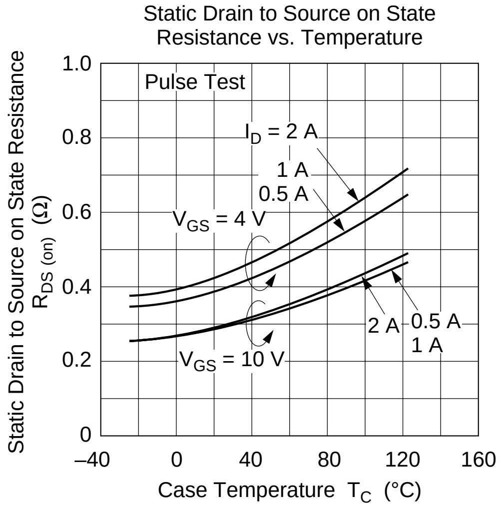

Maximum Safe Operation Area
Drain Current I_D (A)
10
3
1.0
0.3
0.1
0.03
0.01
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation
Operation in this area is limited by $R_{DS (on)}$
Ta = 25°C
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)

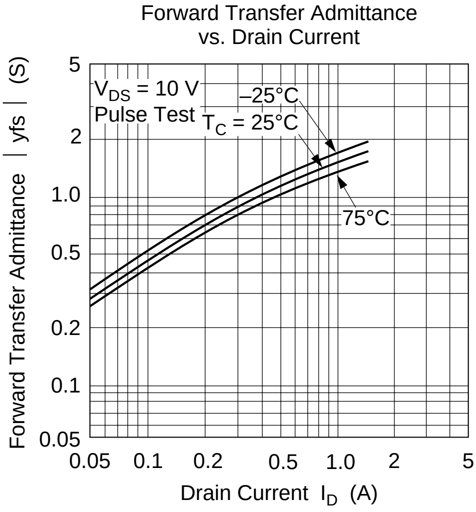

Typical Output Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
10 V
4.5 V
5 V
7 V
Pulse Test
4 V
3.5 V
3 V
V_{GS} = 2.5 V
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)

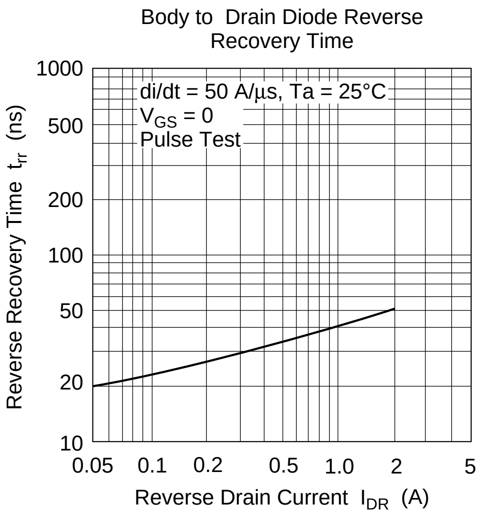

Typical Transfer Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
V_{DS} = 10 V
Pulse Test
75°C
–25°C
T_C= 25°C
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)

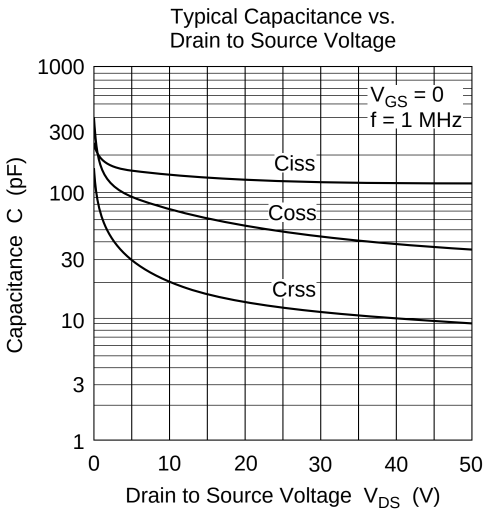

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
2 A
1 A
I_D = 0.5 A
Drain to Source Saturation Voltage
V_DS (on) (V)
Gate to Source Voltage V_GS (V)
1.0
0.8
0.6
0.4
0.2
0
2
4
6
8
10

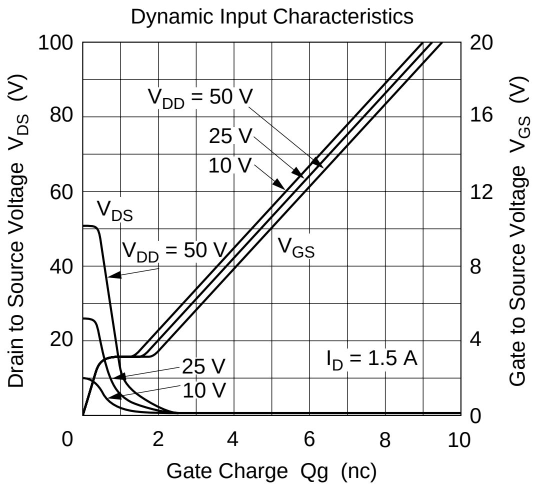

Static Drain to Source On State
Resistance vs. Drain Current
Pulse Test
V_GS = 4 V
10 V
Static Drain to Source on State Resistance
R_DS (on) (Ω)
Drain Current I_D (A)
5
2
1.0
0.5
0.2
0.1
0.05
0.05
0.1
0.2
0.5
1.0
2
5

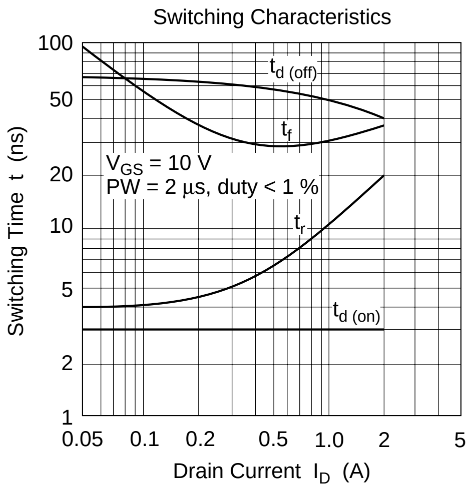

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 2 A
1 A
0.5 A
V_GS = 4 V
2 A
0.5 A
1 A
V_GS = 10 V
Static Drain to Source on State Resistance
R_DS (on) (Ω)
Case Temperature T_C (°C)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160

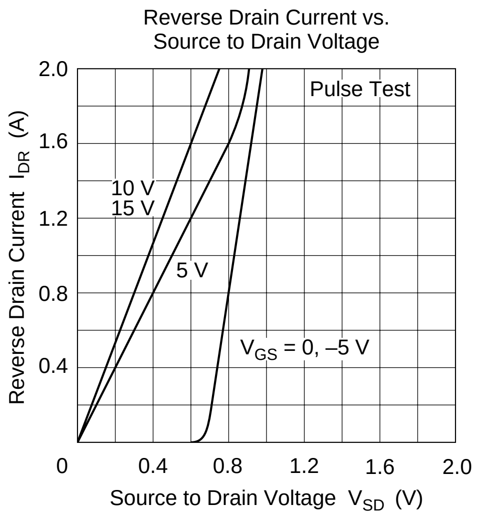

Forward Transfer Admittance
vs. Drain Current
V_DS = 10 V
Pulse Test
–25°C
T_C = 25°C
75°C
Forward Transfer Admittance | yfs | (S)
Drain Current I_D (A)
5
2
1.0
0.5
0.2
0.1
0.05
0.05
0.1
0.2
0.5
1.0
2
5


Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/μs, Ta = 25°C
V_GS = 0
Pulse Test
Reverse Recovery Time t_rr (ns)
1000
500
200
100
50
20
10
0.05
0.1
0.2
0.5
1.0
2
5
Reverse Drain Current I_DR (A)


Typical Capacitance vs. Drain to Source Voltage
V_GS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
1000
300
100
30
10
3
1
0
10
20
30
40
50
Drain to Source Voltage V_DS (V)


Dynamic Input Characteristics
V_DD = 50 V
25 V
10 V
V_DS
V_DD = 50 V
V_GS
25 V
10 V
I_D = 1.5 A
Drain to Source Voltage V_DS (V)
100
80
60
40
20
0
Gate to Source Voltage V_GS (V)
20
16
12
8
4
0
0
2
4
6
8
10
Gate Charge Qg (nc)


Switching Characteristics
t_d (off)
t_f
V_GS = 10 V
PW = 2 μs, duty < 1 %
t_r
t_d (on)
Switching Time t (ns)
100
50
20
10
5
2
1
0.05
0.1
0.2
0.5
1.0
2
5
Drain Current I_D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
5 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
2.0
1.6
1.2
0.8
0.4
0
0.4
0.8
1.2
1.6
2.0

2SK1056, 2SK1057, 2SK1058

Silicon N-Channel MOS FET

Application

Low frequency power amplifier
Complementary pair with 2SJ160, 2SJ161 and 2SJ162

Features

- Good frequency characteristic
- High speed switching
- Wide area of safe operation
- Enhancement-mode
- Good complementary characteristics
- Equipped with gate protection diodes
- Suitable for audio power amplifier

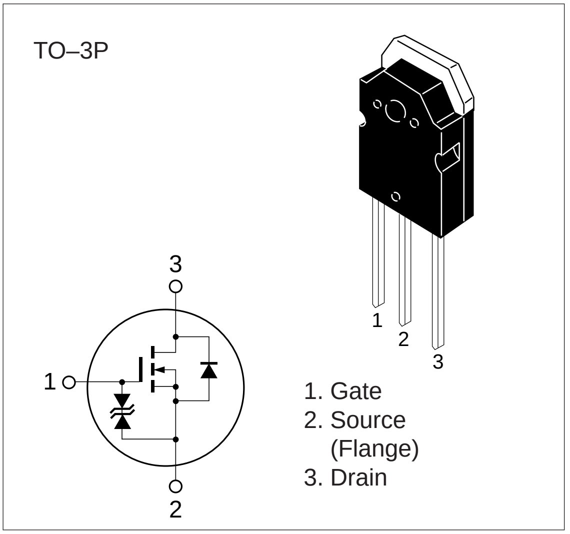


Table 1 Absolute Maximum Ratings (Ta = 25°C)

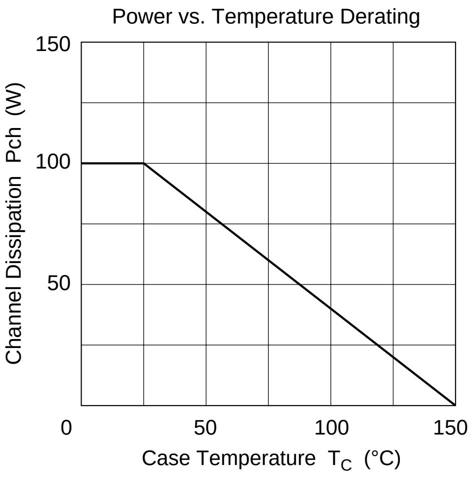
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1056	V_{DSX}	120	V
	2SK1057		140	
	2SK1058		160	
Gate to source voltage		V_{GSS}	±15	V
Drain current		I_D	7	A
Body to drain diode reverse drain current		I_{DR}	7	A
Channel dissipation		Pch*	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

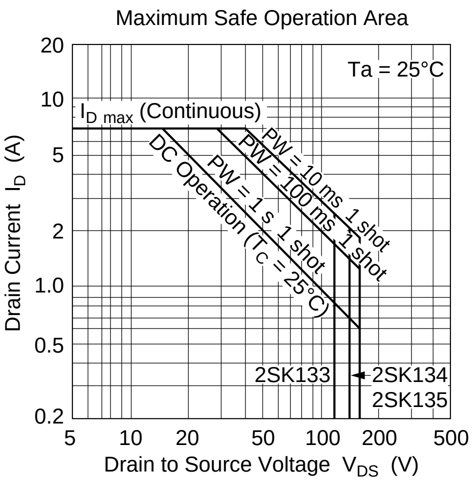
* Value at T_C = 25 °C

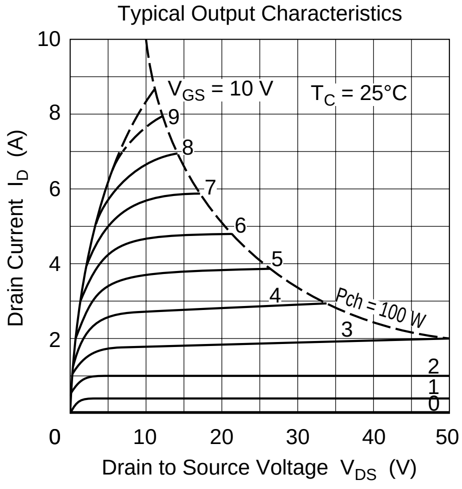
Table 2 Electrical Characteristics (Ta = 25°C)

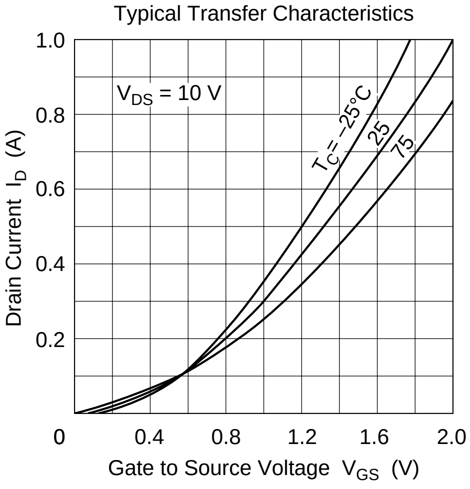
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1056	$V_{(BR)DSX}$	120	—	—	V	I_D = 10 mA, V_{GS} = –10 V
	2SK1057		140				
	2SK1058		160				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±15	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	0.15	—	1.45	V	I_D = 100 mA, V_{DS} = 10 V
Drain to source saturation voltage		$V_{DS(sat)}$	—	—	12	V	I_D = 7 A, V_{GD} = 0 *
Forward transfer admittance		$\|y_{fs}\|$	0.7	1.0	1.4	S	I_D = 3 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	600	—	pF	V_{GS} = –5 V, V_{DS} = 10 V,
Output capacitance		Coss	—	350	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	10	—	pF	
Turn-on time		t_{on}	—	180	—	ns	V_{DD} = 20 V, I_D = 4 A,
Turn-off time		t_{off}	—	60	—	ns	

* Pulse Test

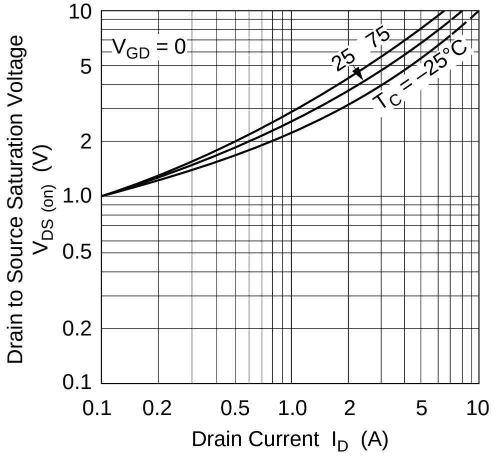

Power vs. Temperature Derating
150
100
50
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)


Maximum Safe Operation Area
Ta = 25°C
$I_{D\ max}$ (Continuous)
PW = 10 ms 1 shot
PW = 100 ms 1 shot
PW = 1 s 1 shot
DC Operation (T_C = 25°C)
2SK133
2SK134
2SK135
20
10
5
2
1.0
0.5
0.2
5
10
20
50
100
200
500
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

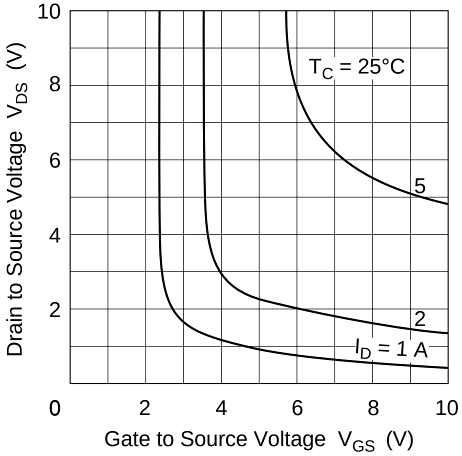

Typical Output Characteristics
V_{GS} = 10 V
T_C = 25°C
9
8
7
6
5
4
3
2
1
0
Pch = 100 W
10
8
6
4
2
0
10
20
30
40
50
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
V_{DS} = 10 V
T_C = –25°C
25
75
1.0
0.8
0.6
0.4
0.2
0
0.4
0.8
1.2
1.6
2.0
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

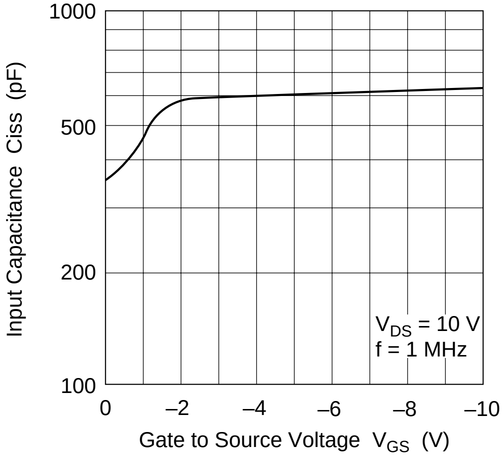
Drain to Source Saturation Voltage vs. Drain Current



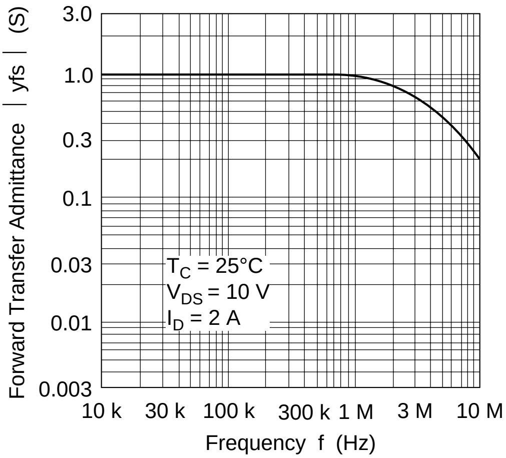
Drain to Source Voltage vs. Gate to Source Voltage



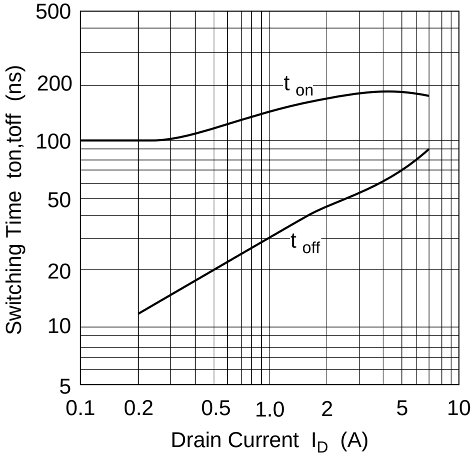
Input Capacitance vs. Gate Source Voltage



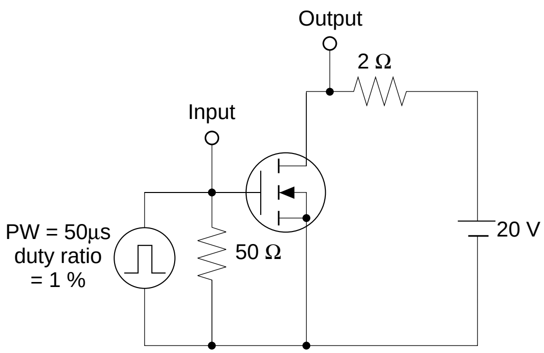
Forward Transfer Admittance vs. Frequency



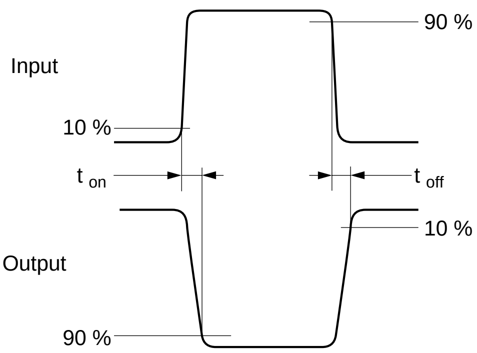
Switching Time vs. Drain Current



Switching Time Test Circuit



Waveforms



2SK1093

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

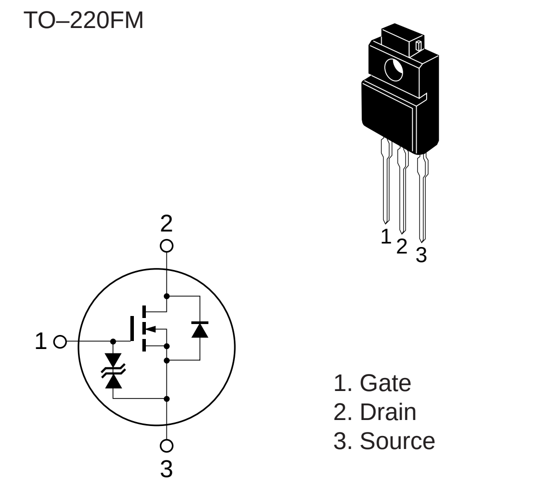


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %

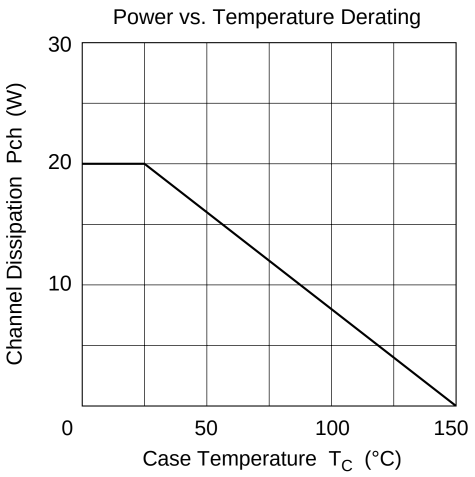
** Value at T_C = 25 °C

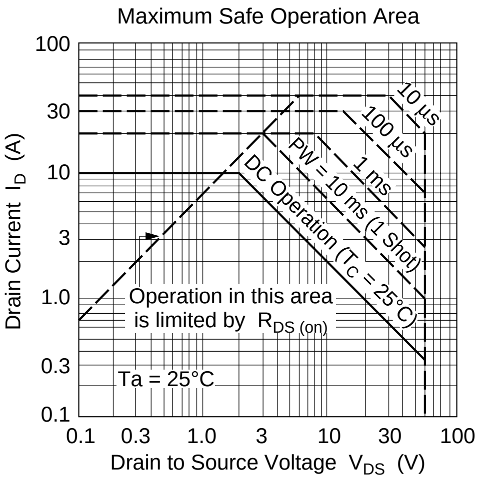
Table 2 Electrical Characteristics (Ta = 25°C)

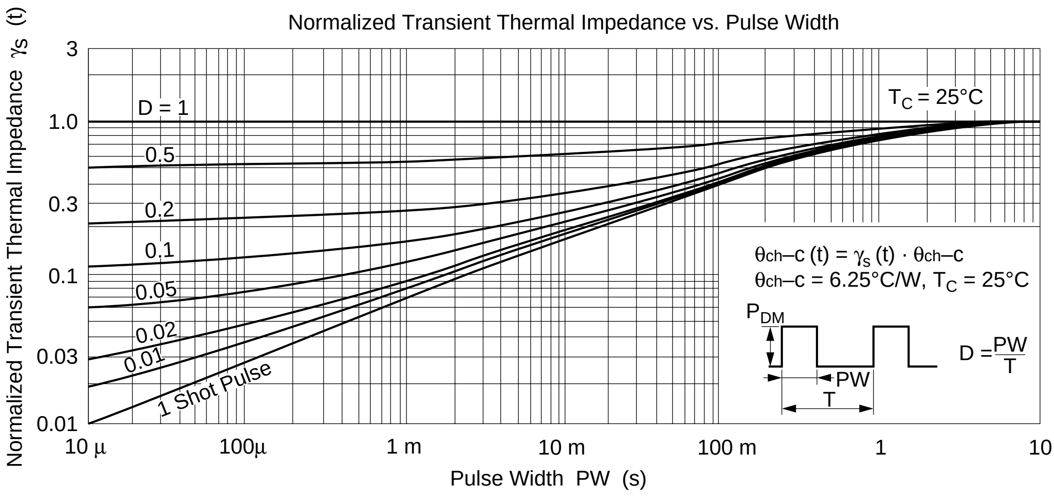
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 5 A, V_{GS} = 10 V *
			0.17	0.22		I_D = 5 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	6.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	220	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	60	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time	t_r	—	55	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	140	—	ns	
Fall time	t_f	—	90	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	125	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK970.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this area
is limited by $R_{DS (on)}$
Ta = 25°C
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
$\theta ch–c (t) = \gamma_S (t) \cdot \theta ch–c$
$\theta ch–c$ = 6.25°C/W, T_C = 25°C
P_{DM}
PW
T
$D = \frac{PW}{T}$
10 µ
100µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1094

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

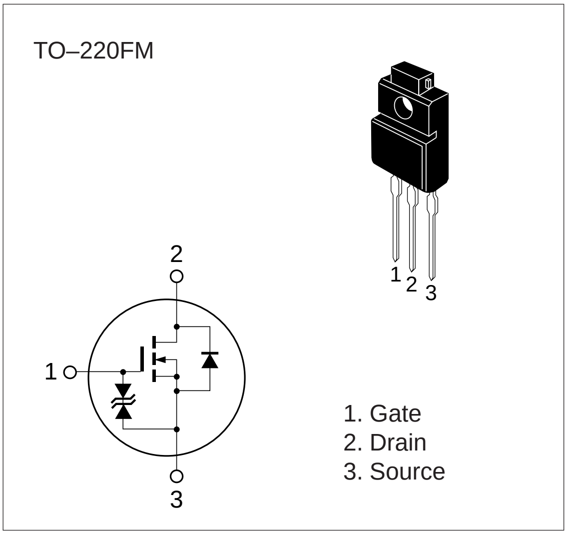


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body to drain diode reverse drain current	I_{DR}	15	A
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

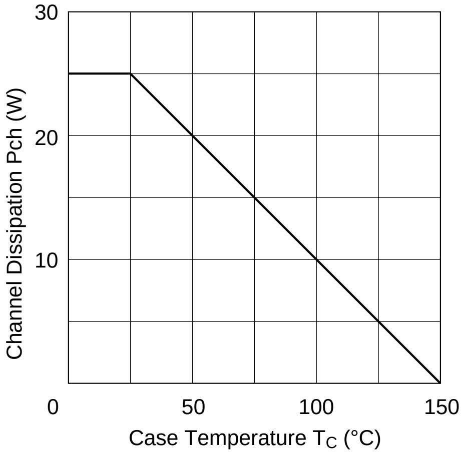
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.055	0.065	Ω	I_D = 8 A, V_{GS} = 10 V *
			0.075	0.095		I_D = 8 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = 8 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	450	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	140	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 8 A, V_{GS} = 10 V,
Rise time	t_r	—	70	—	ns	R_L = 3.75 Ω
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	
Fall time	t_f	—	120	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 15 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 50 A/µs

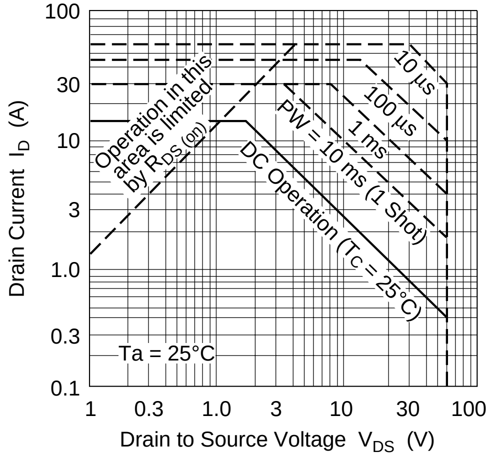
* Pulse Test

See characteristic curves of 2SK971.

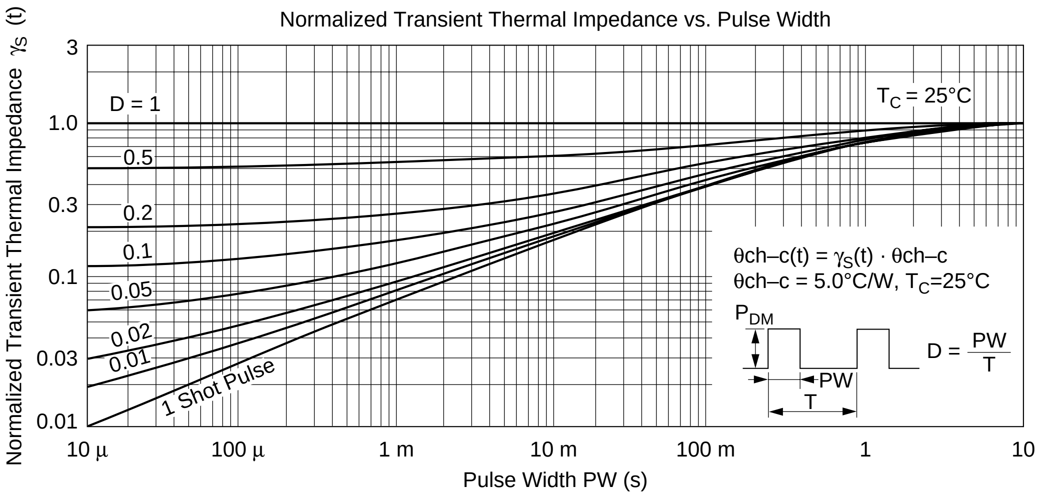
Power vs. Temperature Derating



Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width



2SK1095

Silicon N-Channel MOS FET

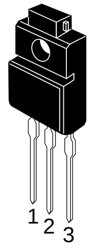
Application

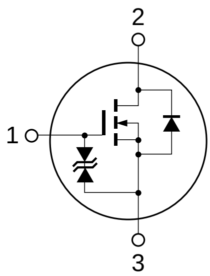
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

TO–220FM





1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$*	100	A
Body to drain diode reverse drain current	I_{DR}	25	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

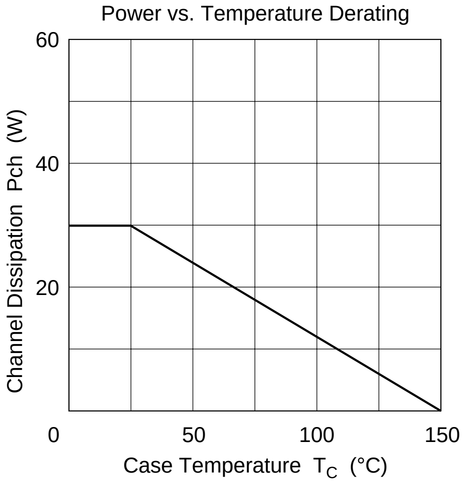
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

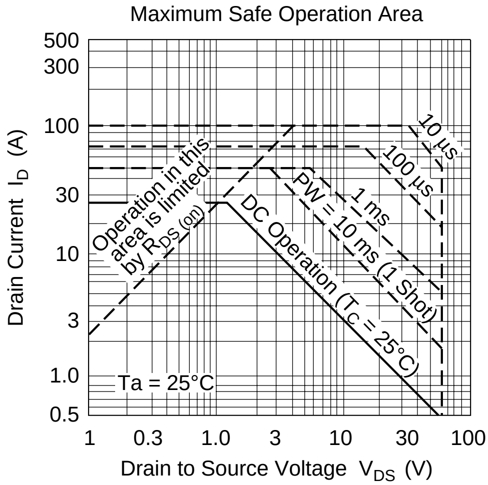
Table 2 Electrical Characteristics (Ta = 25°C)

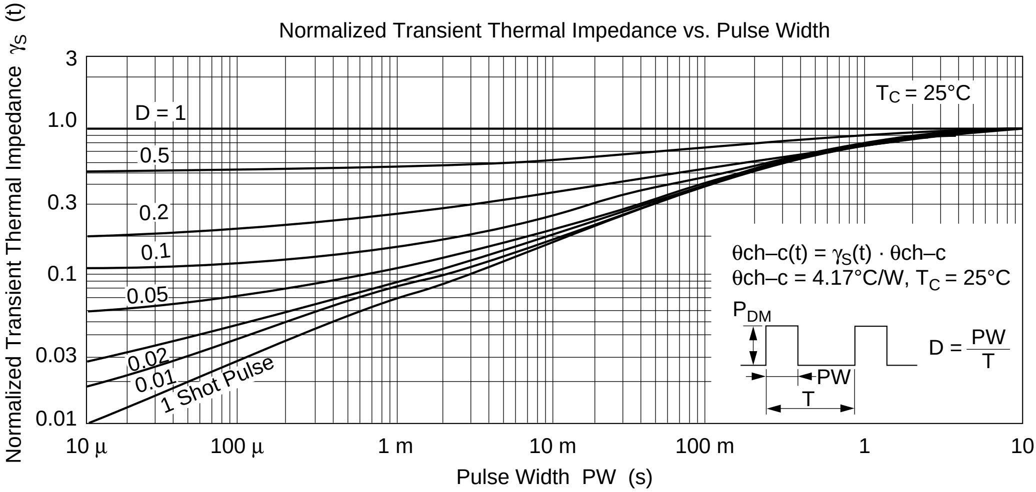
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V *
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.04	Ω	I_D = 15 A, V_{GS} = 10 V *
			0.05	0.06		I_D = 15 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	20	—	S	I_D = 15 A, V_{DS} = 10 V
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	720	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	220	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 15 A, V_{GS} = 10 V,
Rise time	t_r	—	130	—	ns	R_L = 2 Ω
Turn-off delay time	$t_{d(off)}$	—	270	—	ns	
Fall time	t_f	—	180	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 25 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 25 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characterist curves of 2SK972.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
500
300
100
30
10
3
1.0
0.5
Operation in this area is limited by $R_{DS(on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C
1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c(t) = γ_S(t) · θch–c
θch–c = 4.17°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1151Ⓛ, 2SK1152Ⓛ, 2SK1151Ⓢ, 2SK1152Ⓢ

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

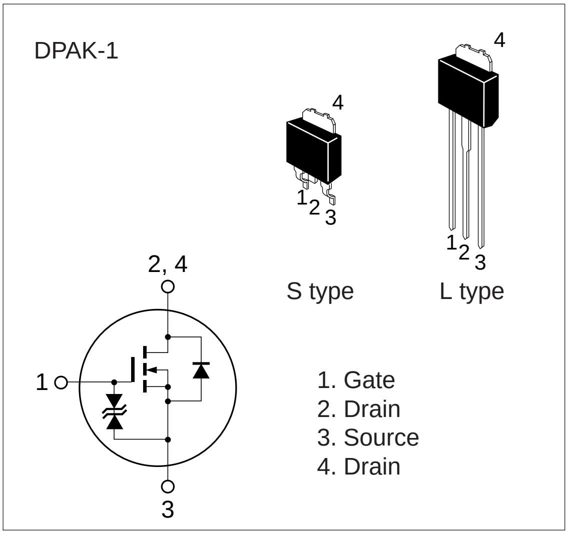


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1151	V_{DSS}	450	V
	2SK1152		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	1.5	A
Drain peak current		$I_{D(pulse)}$*	6	A
Body to drain diode reverse drain current		I_{DR}	1.5	A
Channel dissipation		Pch**	20	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

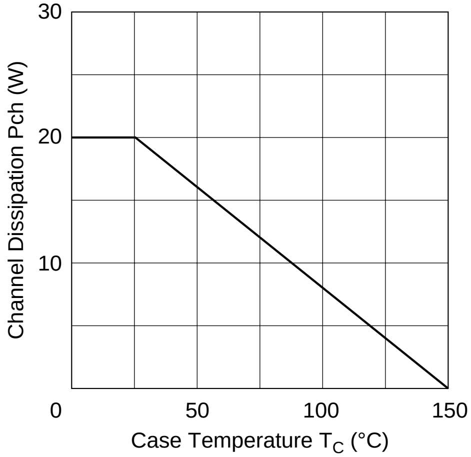
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

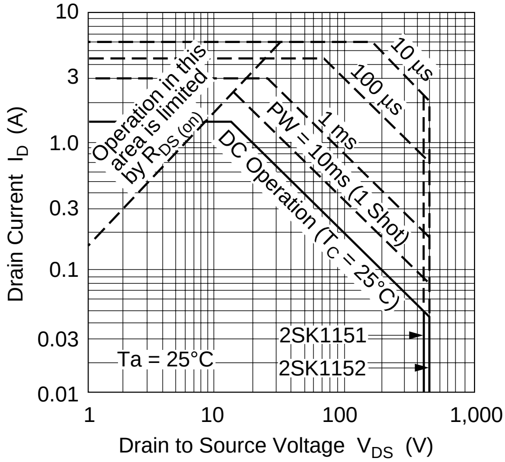
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	2SK1151	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1152		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1151	I_{DSS}	—	—	100	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1152						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1151	$R_{DS(on)}$	—	3.5	5.5	Ω	I_D = 1 A, V_{GS} = 10 V *
	2SK1152		—	4.0	6.0		
Forward transfer admittance		$\|y_{fs}\|$	0.6	1.1	—	S	I_D = 1 A, V_{DS} = 20 V *
Input capacitance		Ciss	—	160	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	45	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	5	—	pF	
Turn-on delay time		$t_{d(on)}$	—	5	—	ns	I_D = 1 A, V_{GS} = 10 V,
Rise time		t_r	—	10	—	ns	R_L = 30 Ω
Turn-off delay time		$t_{d(off)}$	—	20	—	ns	
Fall time		t_f	—	10	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 1.5 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	220	—	ns	I_F = 1.5 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

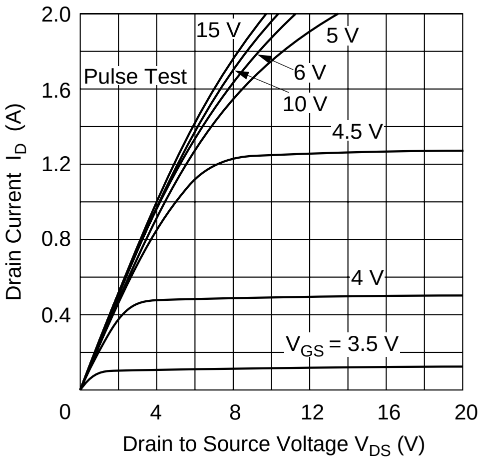
Power vs. Temperature Derating



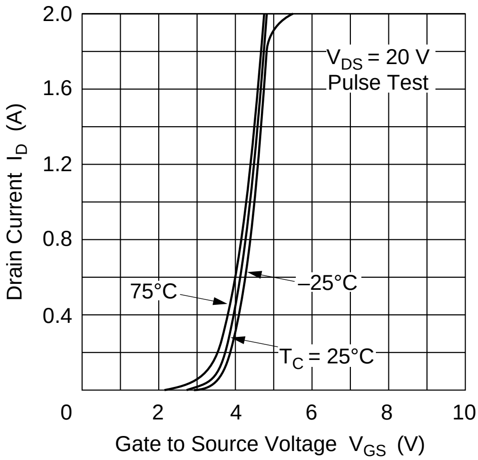
Maximum Safe Operation Area

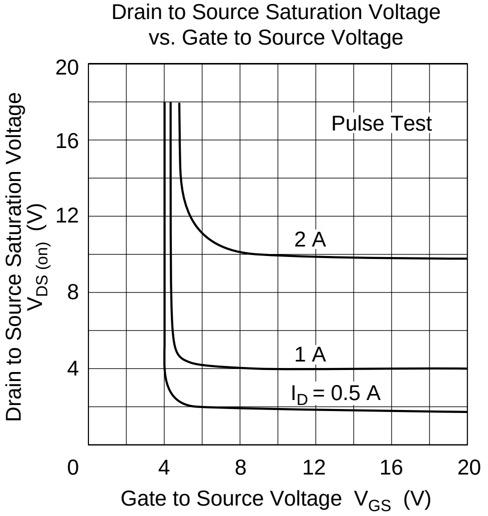


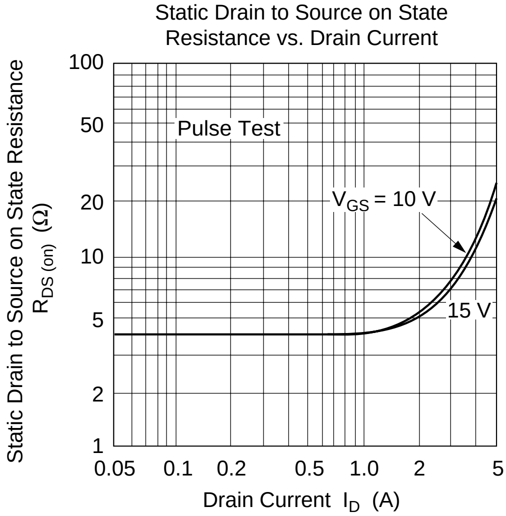
Typical Output Characteristics

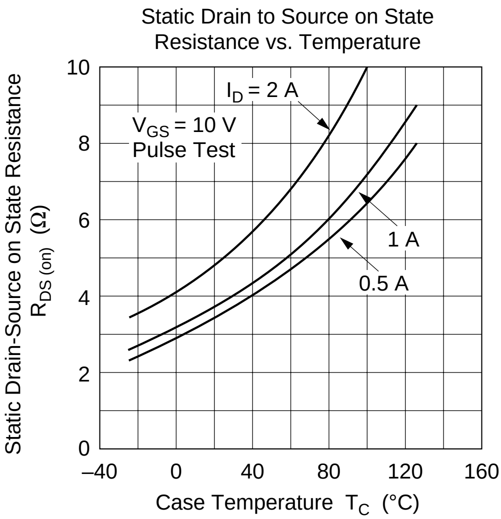


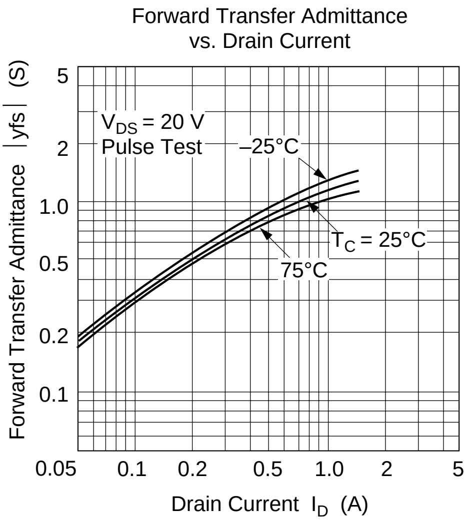
Typical Transfer Characteristics

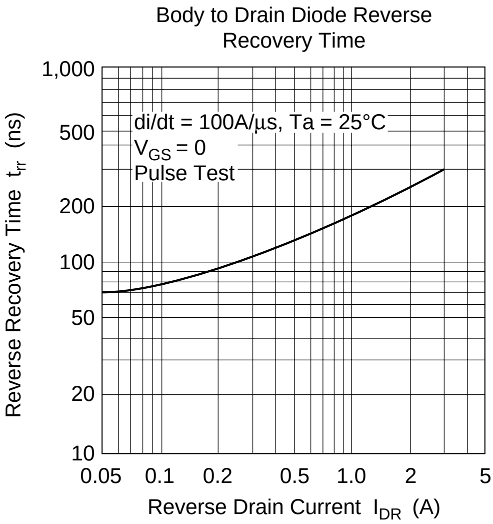


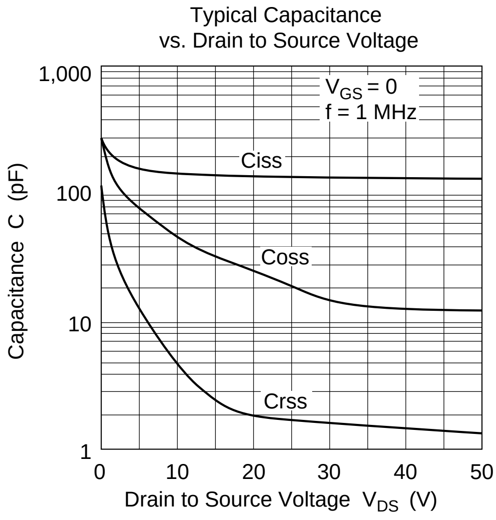

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS\,(on)}$ (V)
Pulse Test
2 A
1 A
I_D = 0.5 A
0
4
8
12
16
20
Gate to Source Voltage V_{GS} (V)

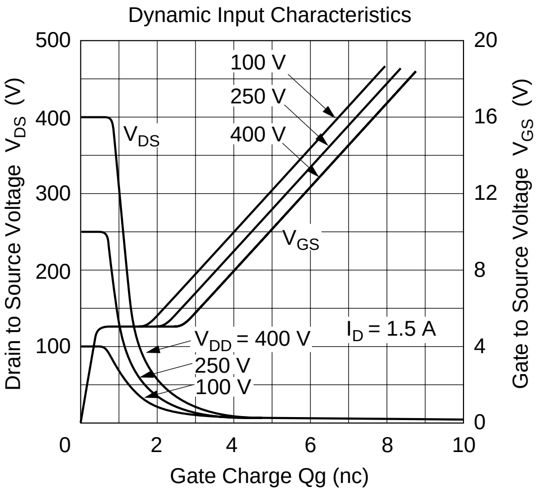

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance $R_{DS\,(on)}$ (Ω)
100
50
20
10
5
2
1
Pulse Test
V_{GS} = 10 V
15 V
0.05
0.1
0.2
0.5
1.0
2
5
Drain Current I_D (A)

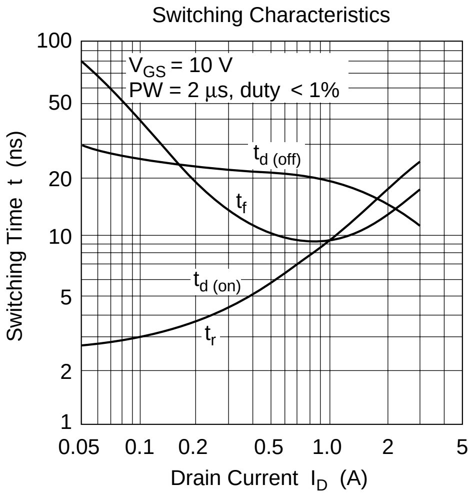

Static Drain to Source on State
Resistance vs. Temperature
Static Drain-Source on State Resistance $R_{DS\,(on)}$ (Ω)
10
8
6
4
2
0
I_D = 2 A
V_{GS} = 10 V
Pulse Test
1 A
0.5 A
–40
0
40
80
120
160
Case Temperature T_C (°C)

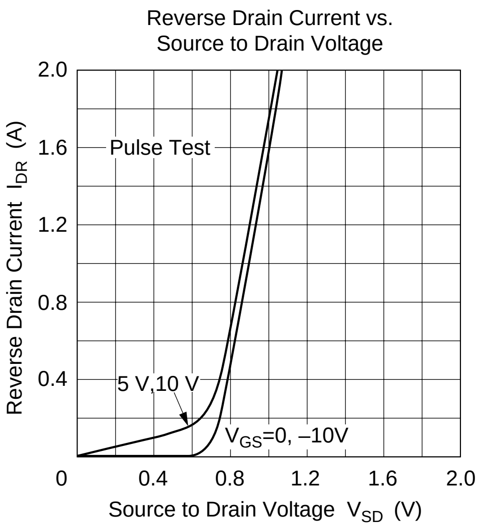

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
5
2
1.0
0.5
0.2
0.1
V_{DS} = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
0.05
0.1
0.2
0.5
1.0
2
5
Drain Current I_D (A)


Body to Drain Diode Reverse Recovery Time
di/dt = 100A/µs, Ta = 25°C
V_{GS} = 0
Pulse Test
Reverse Recovery Time t_{rr} (ns)
1,000
500
200
100
50
20
10
0.05
0.1
0.2
0.5
1.0
2
5
Reverse Drain Current I_{DR} (A)

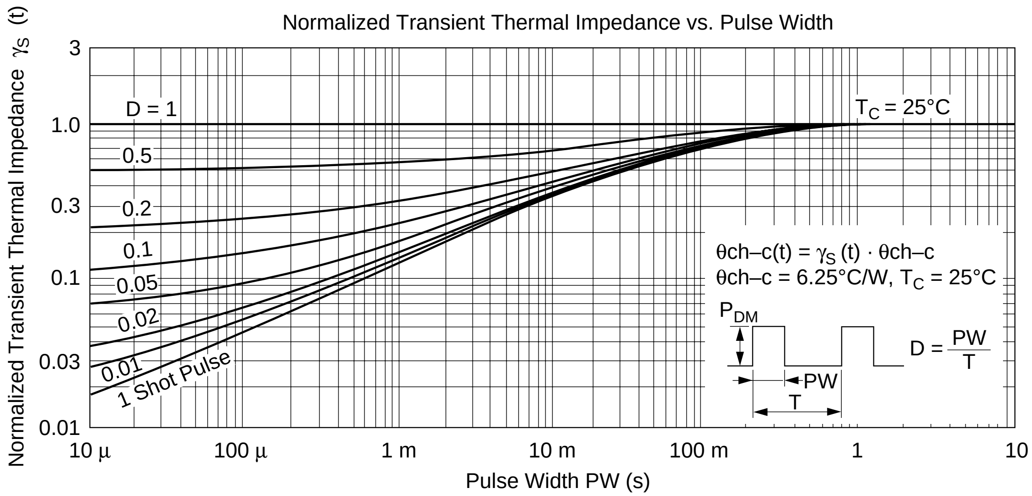

Typical Capacitance vs. Drain to Source Voltage
V_{GS} = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
1,000
100
10
1
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)


Dynamic Input Characteristics
100 V
250 V
400 V
V_{DS}
V_{GS}
V_{DD} = 400 V
250 V
100 V
I_D = 1.5 A
Drain to Source Voltage V_{DS} (V)
500
400
300
200
100
0
Gate to Source Voltage V_{GS} (V)
20
16
12
8
4
0
2
4
6
8
10
Gate Charge Qg (nc)


Switching Characteristics
V_{GS} = 10 V
PW = 2 µs, duty < 1%
t_{d (off)}
t_f
t_{d (on)}
t_r
Switching Time t (ns)
100
50
20
10
5
2
1
0.05
0.1
0.2
0.5
1.0
2
5
Drain Current I_D (A)

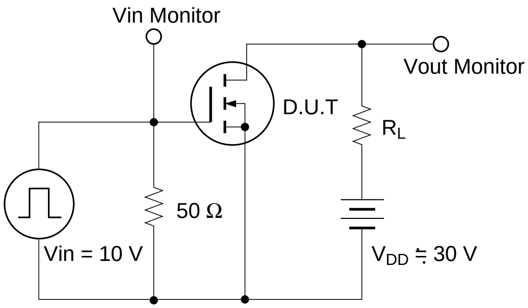


Reverse Drain Current vs.
Source to Drain Voltage
2.0
1.6
1.2
0.8
0.4
Pulse Test
5 V,10 V
V_GS=0, –10V
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_SD (V)
Reverse Drain Current I_DR (A)

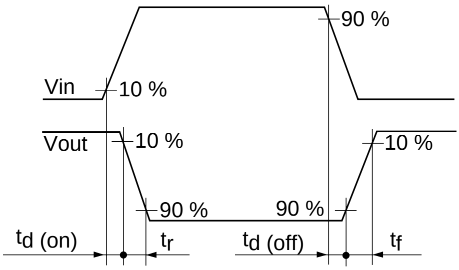


Normalized Transient Thermal Impedance vs. Pulse Width
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
θch–c(t) = γ_S (t) · θch–c
θch–c = 6.25°C/W, T_C = 25°C
P_DM
PW
T
D = PW/T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)
Normalized Transient Thermal Impedance γ_S (t)

Switching Time Test Circuit



Wavewforms



2SK1153, 2SK1154

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

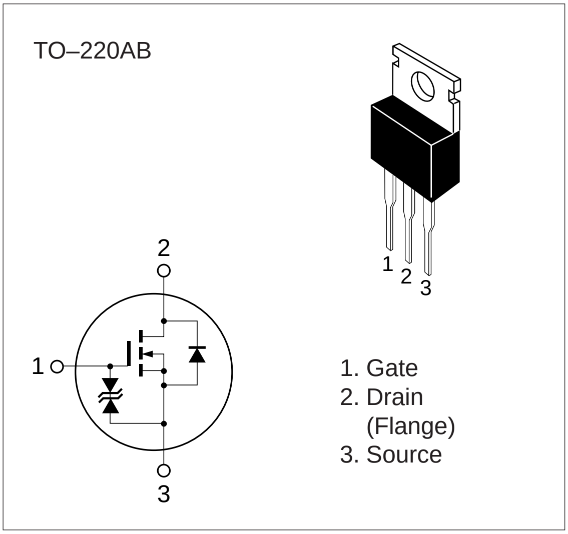


Table 1 Absolute Maximum Ratings (Ta = 25°C)

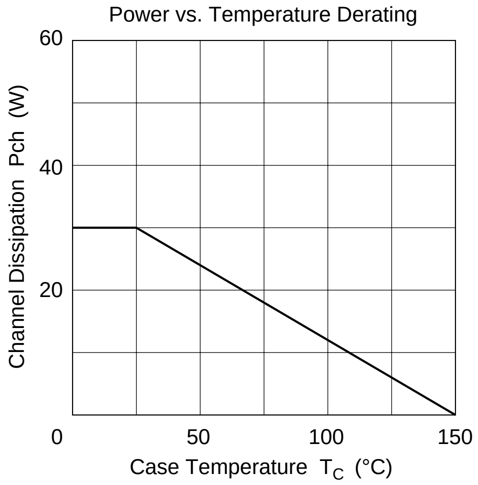
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1153	V_{DSS}	450	V
	2SK1154		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	3	A
Drain peak current		$I_{D(pulse)}$*	12	A
Body to drain diode reverse drain current		I_{DR}	3	A
Channel dissipation		Pch**	30	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

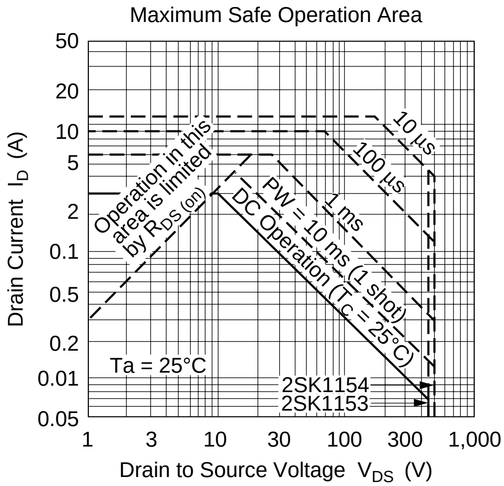
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

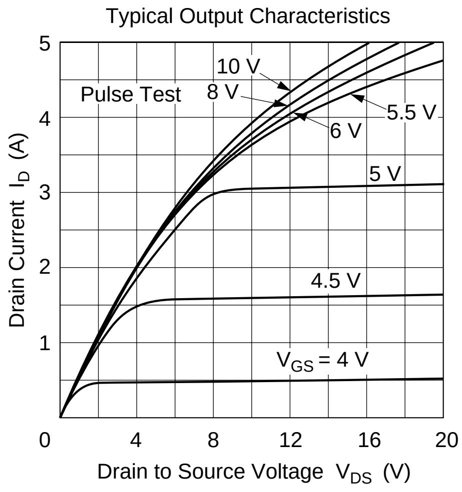
Table 2 Electrical Characteristics (Ta = 25°C)

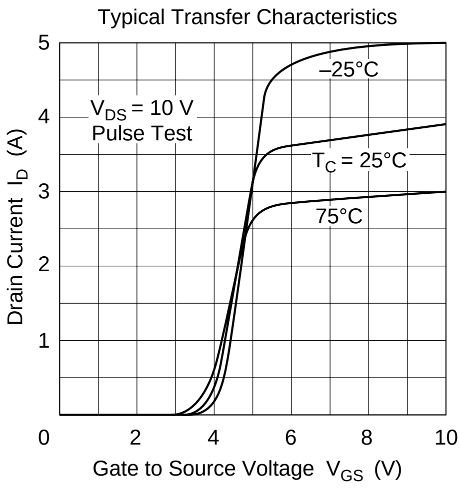
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1153	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1154		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1153	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1154						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1153	$R_{DS(on)}$	—	2.0	2.8	Ω	I_D = 2 A, V_{GS} = 10 V *
	2SK1154		—	2.2	3.0		
Forward transfer admittance		$\|y_{fs}\|$	1.5	2.5	—	S	I_D = 2 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	330	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	90	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	15	—	pF	
Turn-on delay time		$t_{d(on)}$	—	7	—	ns	I_D = 2 A, V_{GS} = 10 V,
Rise time		t_r	—	20	—	ns	R_L = 15 Ω
Turn-off delay time		$t_{d(off)}$	—	30	—	ns	
Fall time		t_f	—	20	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.9	—	V	I_F = 3 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	300	—	ns	I_F = 3 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

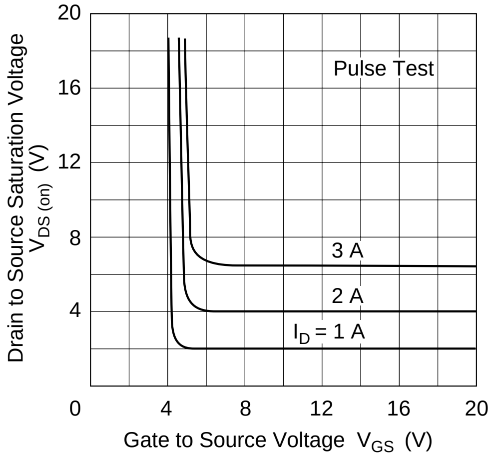

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
50
20
10
5
2
0.1
0.5
0.2
0.01
0.05
10 µs
100 µs
Operation in this area is limited by $R_{DS (on)}$
PW = 10 ms (1 shot)
1 ms
DC Operation (T_C = 25°C)
Ta = 25°C
2SK1154
2SK1153
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)

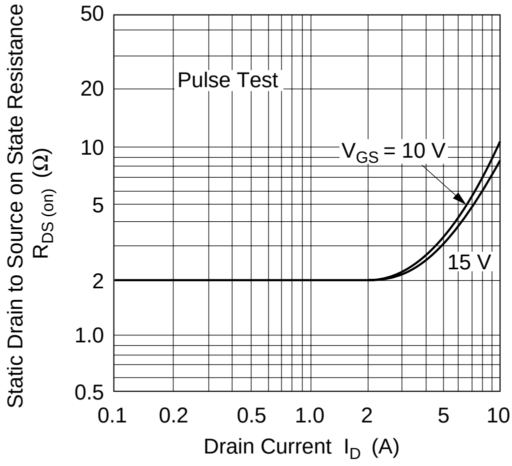

Typical Output Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
Pulse Test
10 V
8 V
6 V
5.5 V
5 V
4.5 V
V_{GS} = 4 V
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
V_{DS} = 10 V
Pulse Test
–25°C
T_C = 25°C
75°C
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

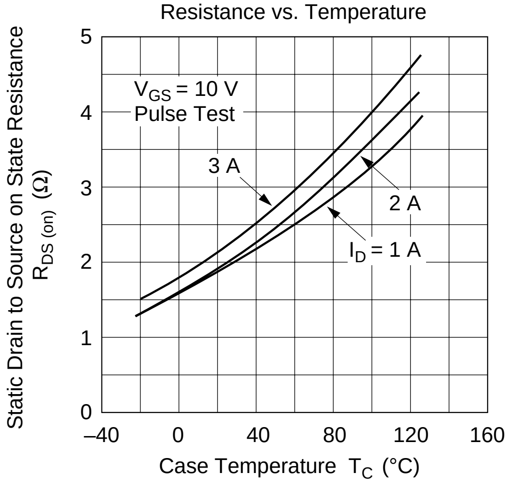
Drain to Source Saturation Voltage vs. Gate to Source Voltage



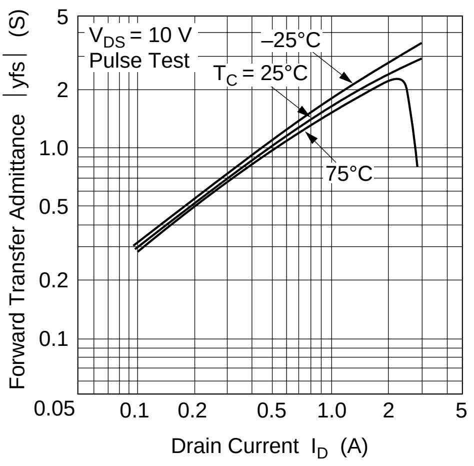
Static Drain to Source on State Resistance vs. Drain Current



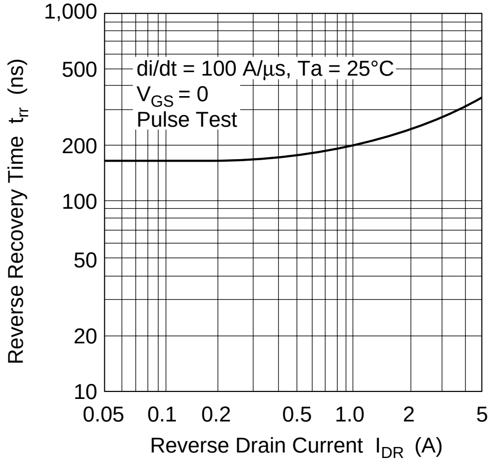
Static Drain to Source on State Resistance vs. Temperature



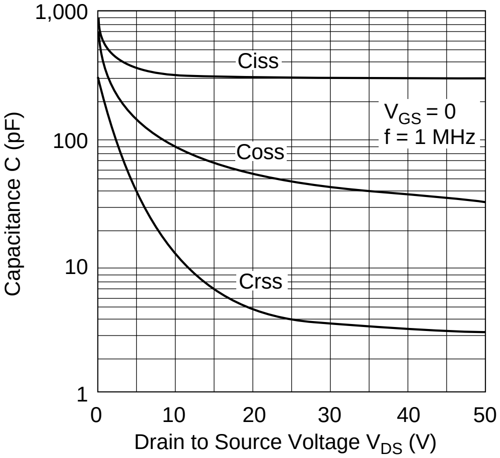
Forward Transfer Admittance vs. Drain Current



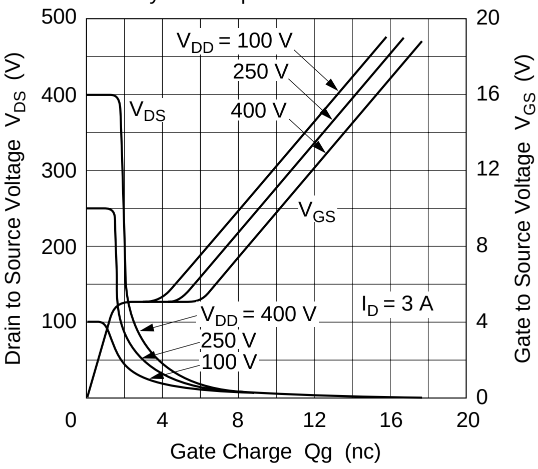
Body to Drain Diode Reverse Recovery Time



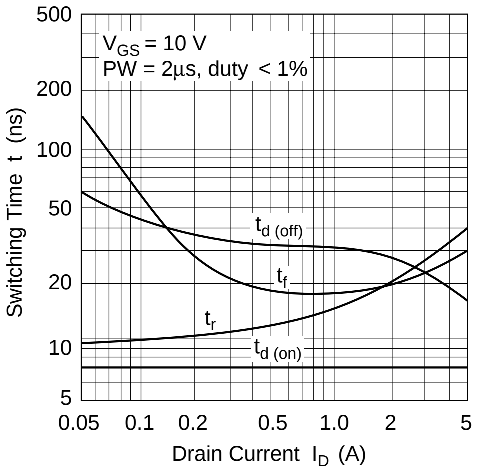
Typical Capacitance vs. Drain to Source Voltage

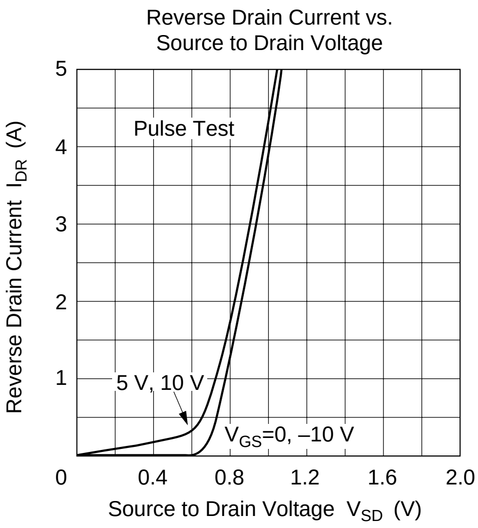


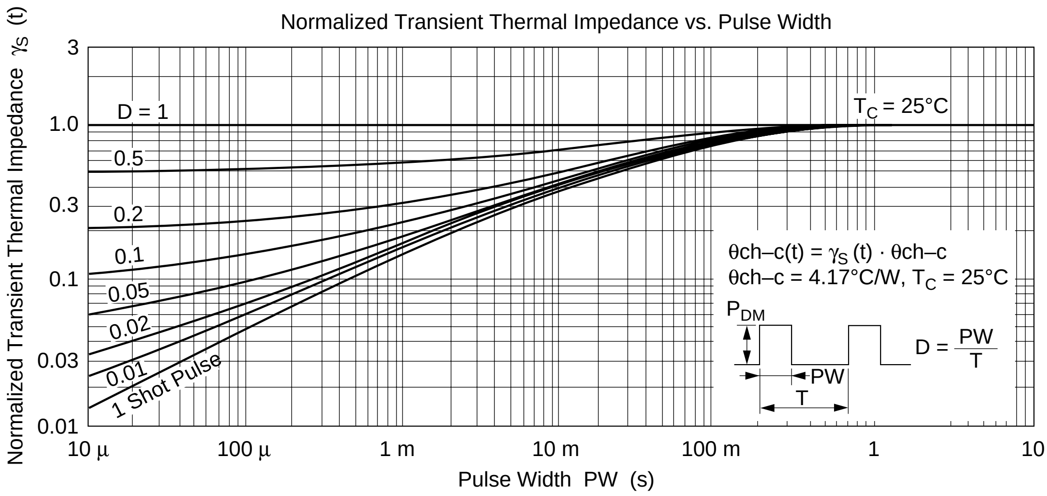
Dynamic Input Characteristics



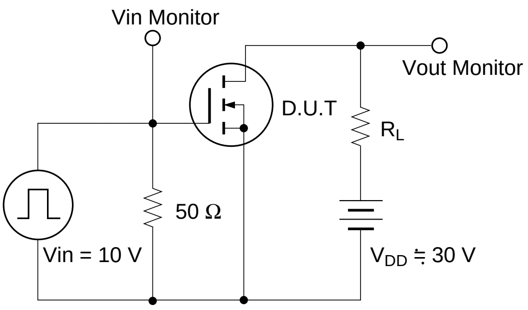
Switching Characteristics



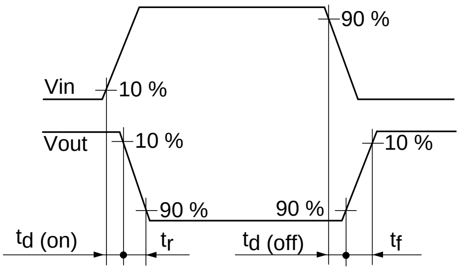

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5 V, 10 V
VGS=0, –10 V
Reverse Drain Current IDR (A)
Source to Drain Voltage VSD (V)
0
0.4
0.8
1.2
1.6
2.0
1
2
3
4
5


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
TC = 25°C
θch–c(t) = γS (t) · θch–c
θch–c = 4.17°C/W, TC = 25°C
PDM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γS (t)
Pulse Width PW (s)
10 μ
100 μ
1 m
10 m
100 m
1
10
3
1.0
0.3
0.1
0.03
0.01

Switching Time Test Circuit



Wavewforms



2SK1155, 2SK1156

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

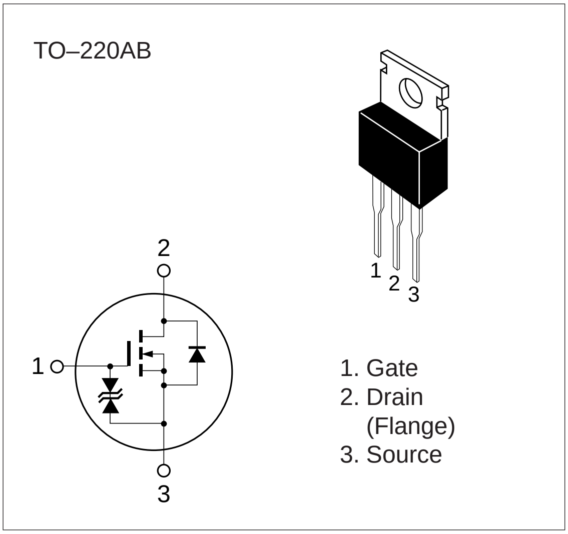


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1155	V_{DSS}	450	V
	2SK1156		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	5	A
Drain peak current		$I_{D(pulse)}$*	20	A
Body to drain diode reverse drain current		I_{DR}	5	A
Channel dissipation		Pch**	50	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

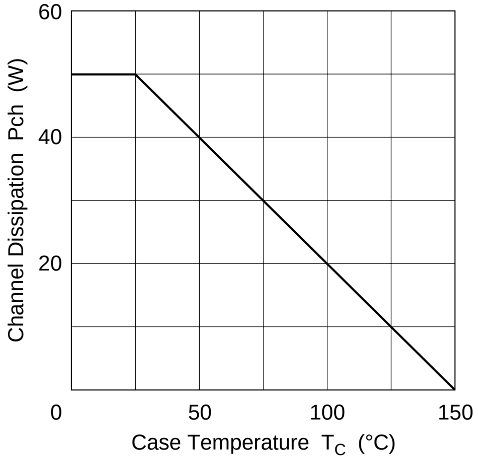
*	PW ≤ 10 µs, duty cycle ≤ 1 %
**	Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

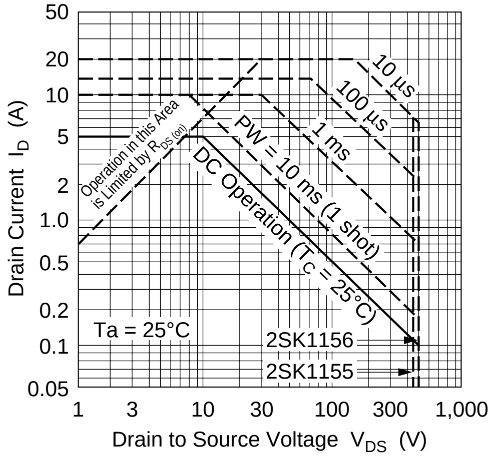
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1155	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1156		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1155	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1156						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1155	$R_{DS(on)}$	—	1.0	1.4	Ω	I_D = 2.5 A, V_{GS} = 10 V *
	2SK1156		—	1.2	1.5		
Forward transfer admittance		$\|y_{fs}\|$	2.5	4.0	—	S	I_D = 2.5 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	640	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	160	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	20	—	pF	
Turn-on delay time		$t_{d(on)}$	—	10	—	ns	I_D = 2.5 A, V_{GS} = 10 V,
Rise time		t_r	—	25	—	ns	R_L = 12 Ω
Turn-off delay time		$t_{d(off)}$	—	50	—	ns	
Fall time		t_f	—	30	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 5 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	300	—	ns	I_F = 5 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

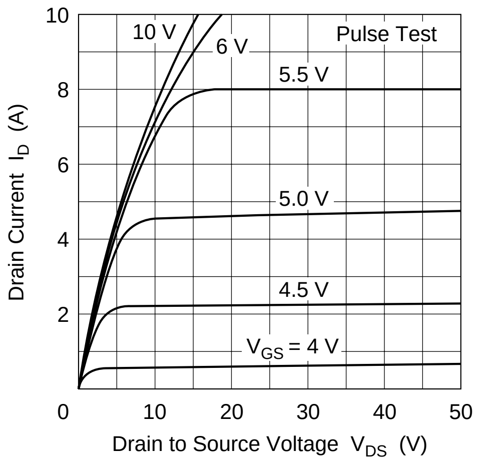
Power vs. Temperature Derating



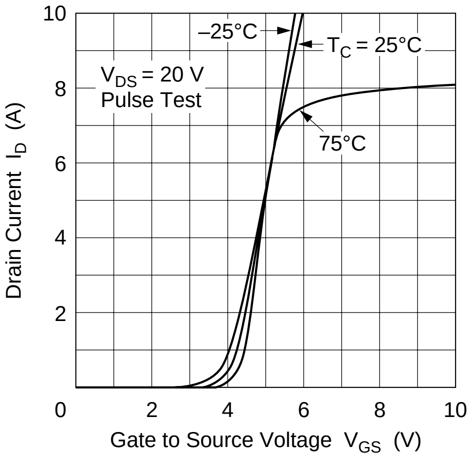
Maximum Safe Operation Area

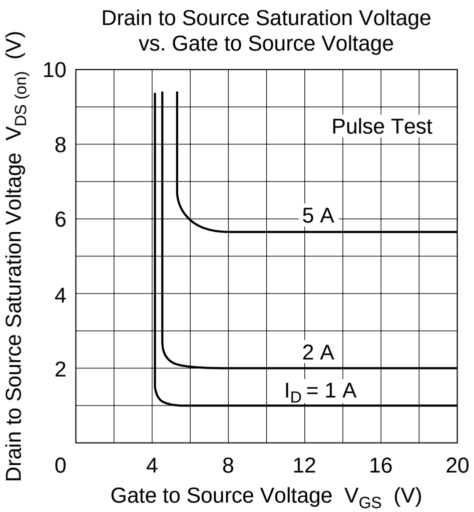


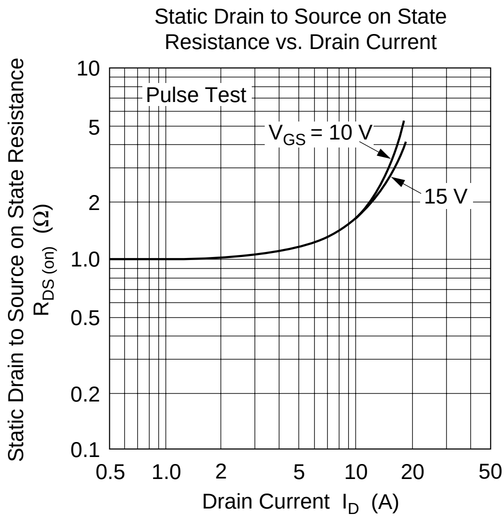
Typical Output Characteristics

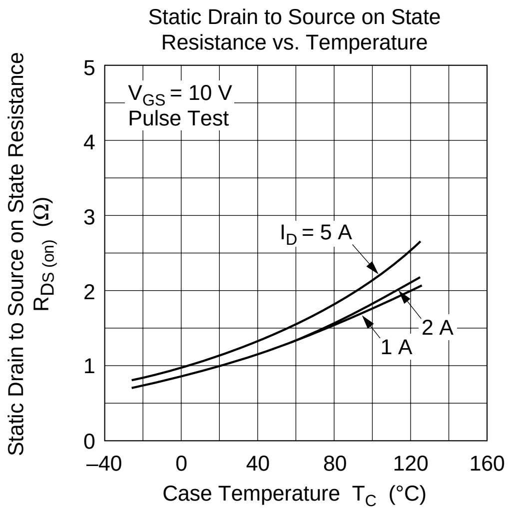


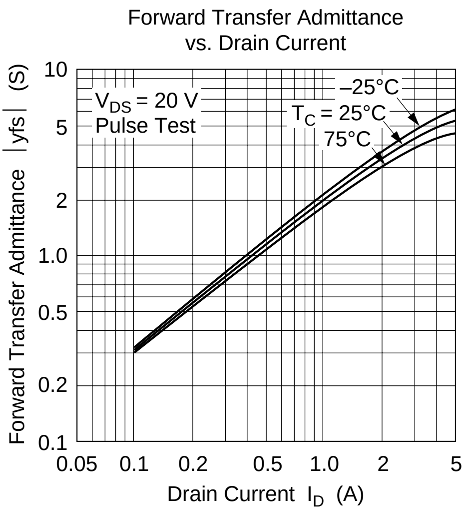
Typical Transfer Characteristics



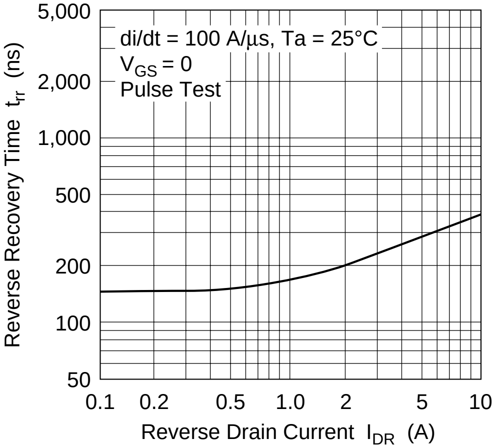

Drain to Source Saturation Voltage vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS\ (on)}$ (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
5 A
2 A
I_D = 1 A
0
2
4
6
8
10
0
4
8
12
16
20


Static Drain to Source on State Resistance vs. Drain Current
Static Drain to Source on State Resistance $R_{DS\ (on)}$ (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 10 V
15 V
0.1
0.2
0.5
1.0
2
5
10
0.5
1.0
2
5
10
20
50

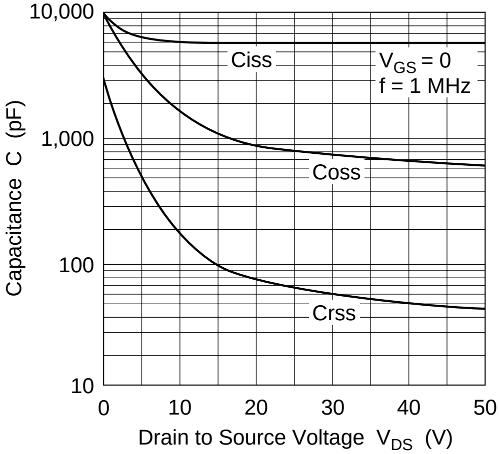

Static Drain to Source on State Resistance vs. Temperature
Static Drain to Source on State Resistance $R_{DS\ (on)}$ (Ω)
Case Temperature T_C (°C)
V_{GS} = 10 V
Pulse Test
I_D = 5 A
2 A
1 A
0
1
2
3
4
5
–40
0
40
80
120
160


Forward Transfer Admittance vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
V_{DS} = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
0.1
0.2
0.5
1.0
2
5
10
0.05
0.1
0.2
0.5
1.0
2
5

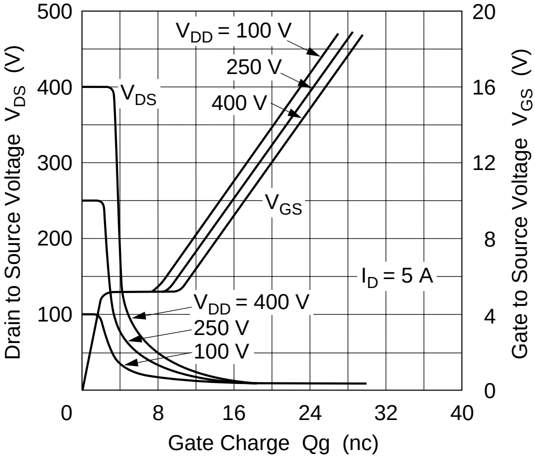
Body to Drain Diode Reverse Recovery Time



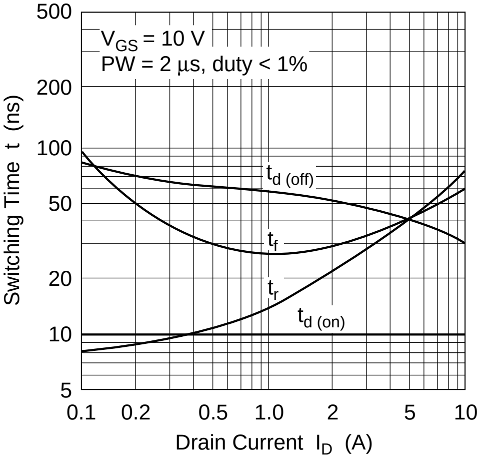
Typical Capacitance vs. Drain to Source Voltage

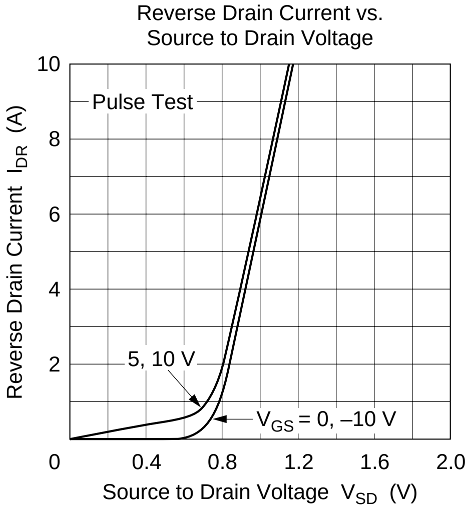


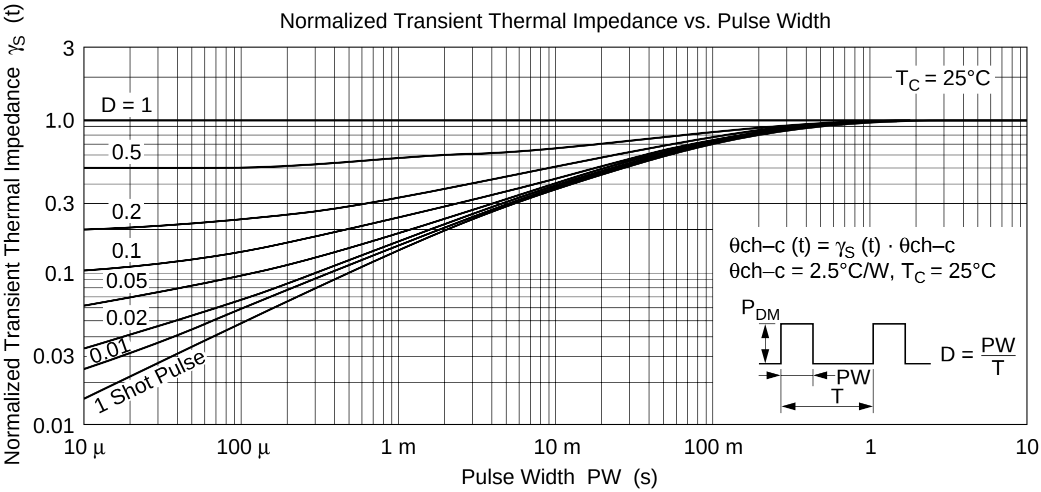
Dynamic Input Characteristics



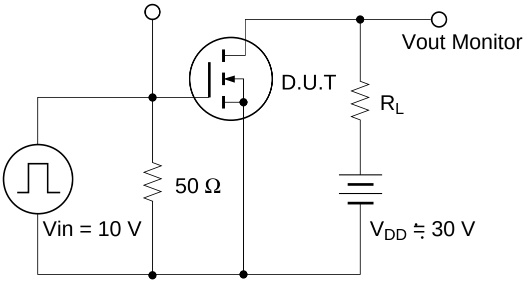
Switching Characteristics



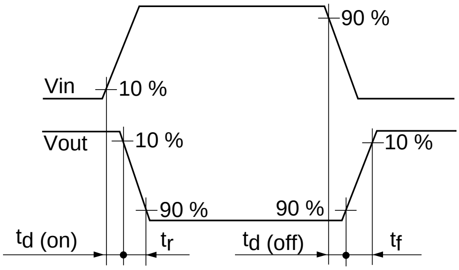

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5, 10 V
V_{GS} = 0, –10 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
2
4
6
8
10


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 2.5°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
10 µ
100 µ
1 m
10 m
100 m
1
10
0.01
0.03
0.1
0.3
1.0
3

Switching Time Test Circuit



Wavewforms



2SK1157, 2SK1158

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

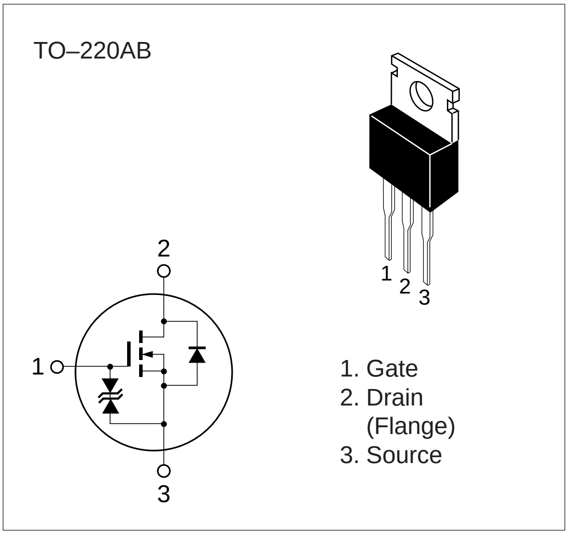


Table 1 Absolute Maximum Ratings (Ta = 25°C)

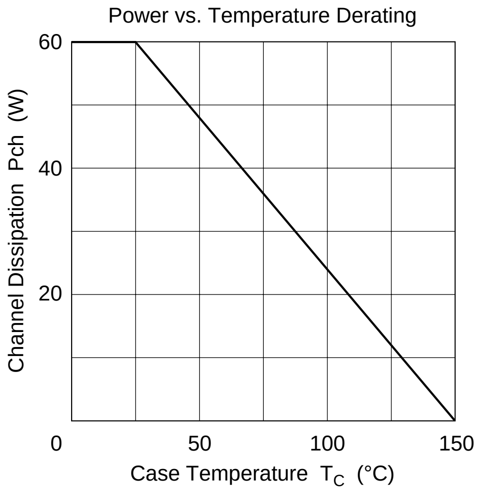
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1157	V_{DSS}	450	V
	2SK1158		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	7	A
Drain peak current		$I_{D(pulse)}$*	28	A
Body to drain diode reverse drain current		I_{DR}	7	A
Channel dissipation		Pch**	60	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

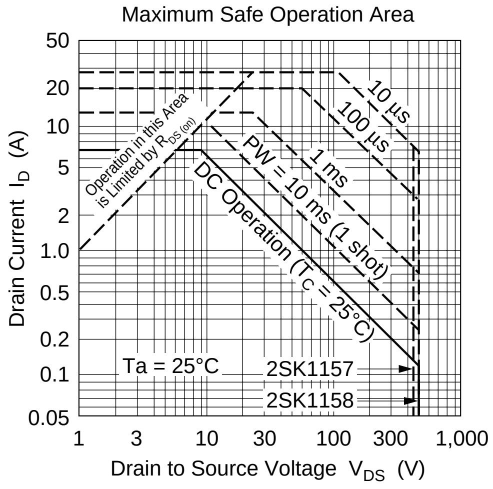
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

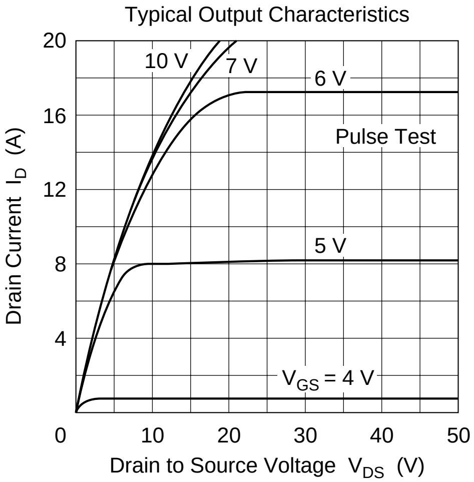
Table 2 Electrical Characteristics (Ta = 25°C)

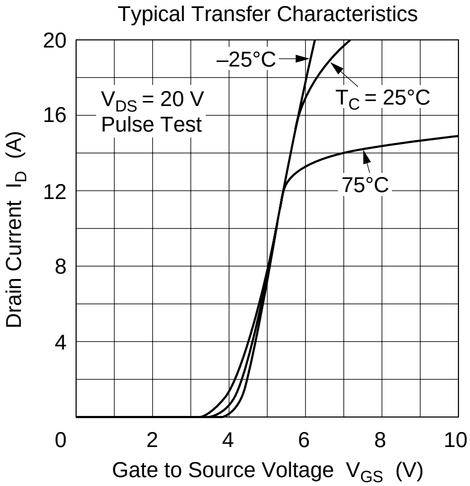
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1157	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1158		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1157	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1158						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1157	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 4 A, V_{GS} = 10 V *
	2SK1158		—	0.7	0.9		
Forward transfer admittance		$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1050	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	280	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	40	—	pF	
Turn-on delay time		$t_{d(on)}$	—	15	—	ns	I_D = 4 A, V_{GS} = 10 V,
Rise time		t_r	—	55	—	ns	R_L = 7.5 Ω
Turn-off delay time		$t_{d(off)}$	—	95	—	ns	
Fall time		t_f	—	40	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 7 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	320	—	ns	I_F = 7 A, V_{GS} = 0, di_F/dt = 100 A/µs

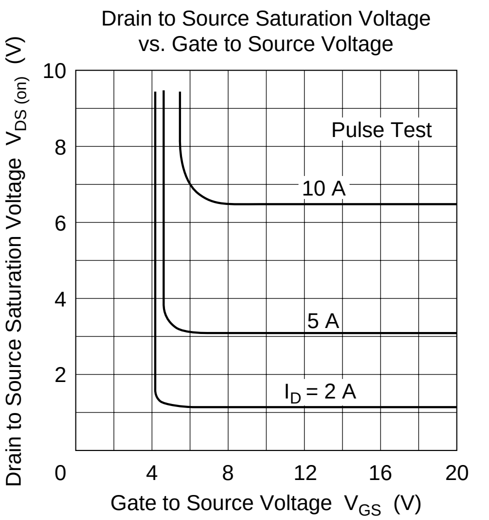
* Pulse Test

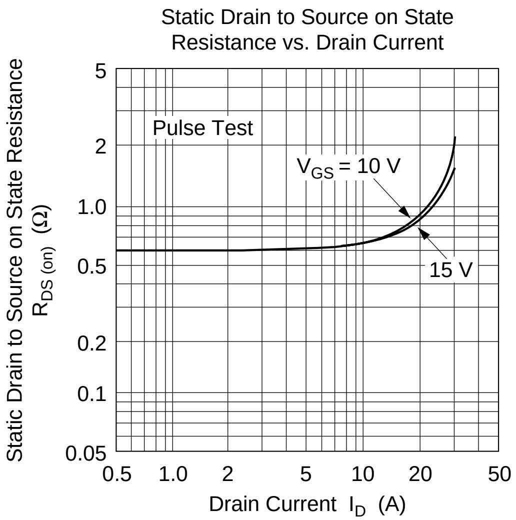

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

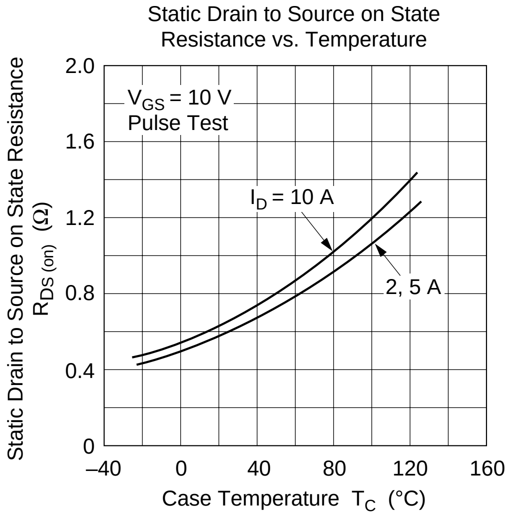

Maximum Safe Operation Area
Drain Current I_D (A)
50
20
10
5
2
1.0
0.5
0.2
0.1
0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS (on)}$
Ta = 25°C
2SK1157
2SK1158
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)

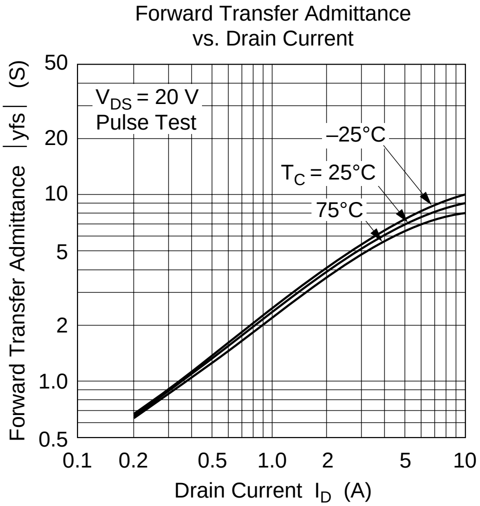

Typical Output Characteristics
Drain Current I_D (A)
20
16
12
8
4
0
10 V
7 V
6 V
Pulse Test
5 V
V_{GS} = 4 V
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)

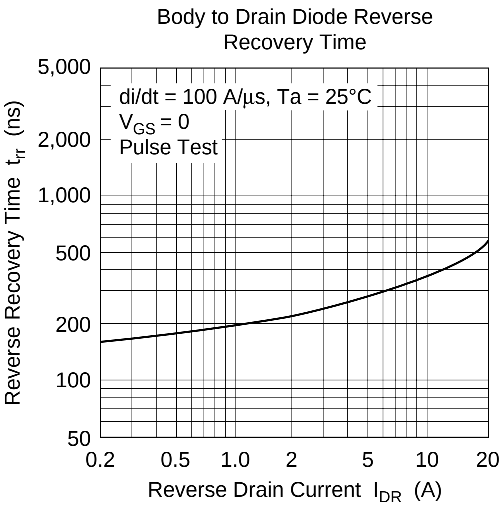

Typical Transfer Characteristics
Drain Current I_D (A)
20
16
12
8
4
0
V_{DS} = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

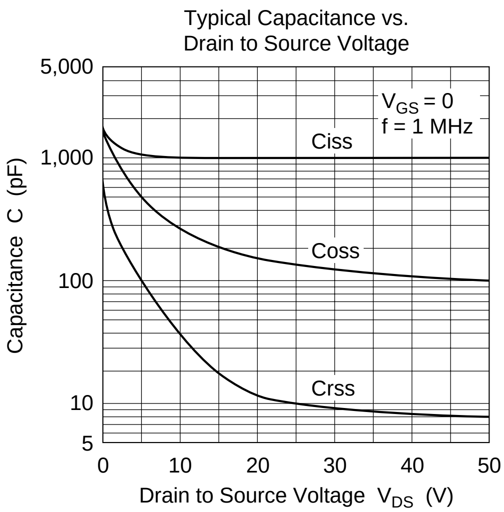

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS\ (on)}$ (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
10 A
5 A
I_D = 2 A
0
4
8
12
16
20
2
6
10

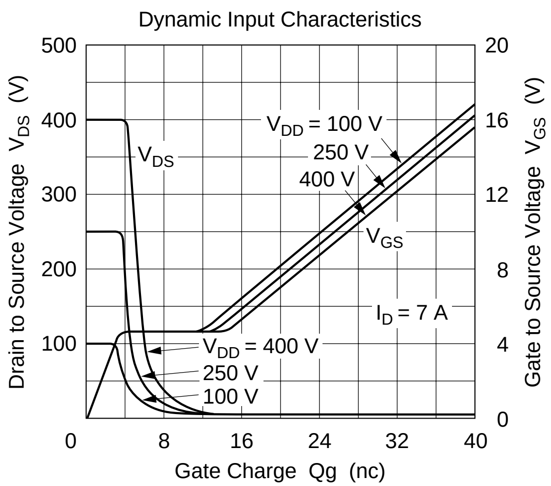

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 10 V
15 V
5
2
1.0
0.5
0.2
0.1
0.05
0.5
1.0
2
5
10
20
50

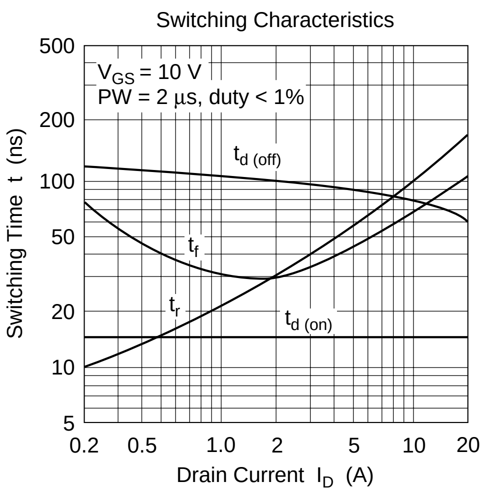

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
Case Temperature T_C (°C)
V_{GS} = 10 V
Pulse Test
I_D = 10 A
2, 5 A
2.0
1.6
1.2
0.8
0.4
0
–40
0
40
80
120
160

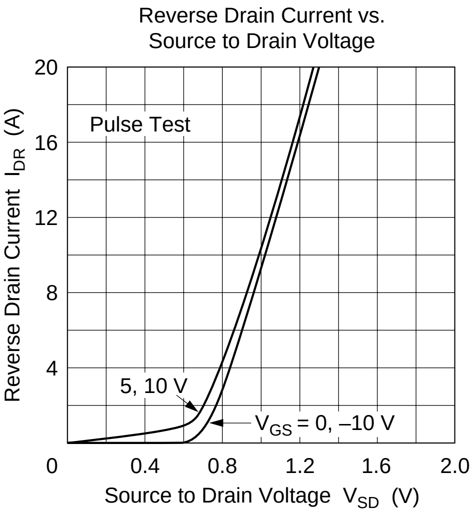

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
V_{DS} = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
50
20
10
5
2
1.0
0.5
0.1
0.2
0.5
1.0
2
5
10


Body to Drain Diode Reverse
Recovery Time
di/dt = 100 A/µs, Ta = 25°C
V_{GS} = 0
Pulse Test
Reverse Recovery Time t_{rr} (ns)
Reverse Drain Current I_{DR} (A)
5,000
2,000
1,000
500
200
100
50
0.2
0.5
1.0
2
5
10
20

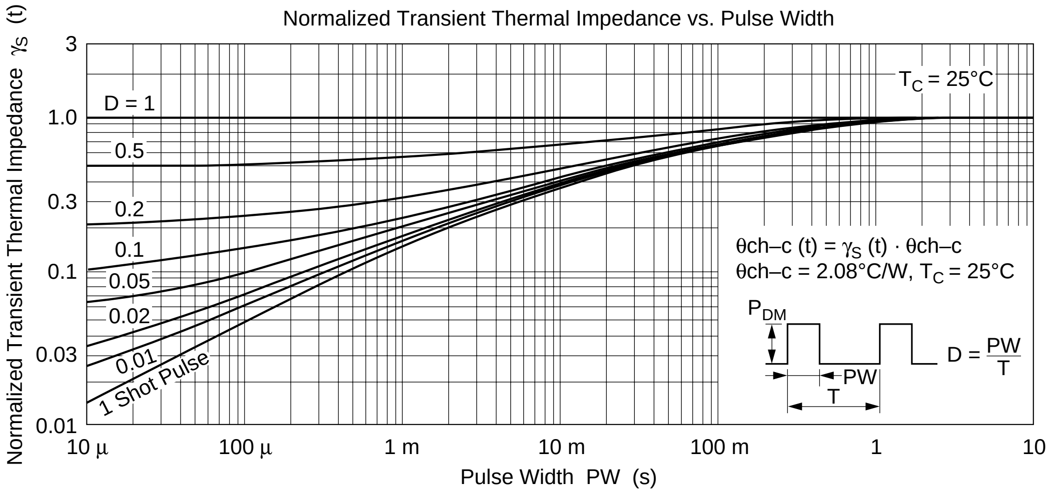

Typical Capacitance vs.
Drain to Source Voltage
V_{GS} = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
Drain to Source Voltage V_{DS} (V)
5,000
1,000
100
10
5
0
10
20
30
40
50


Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
V_{DS}
V_{DD} = 100 V
250 V
400 V
V_{GS}
I_D = 7 A
V_{DD} = 400 V
250 V
100 V
Gate Charge Qg (nc)
500
400
300
200
100
0
8
16
24
32
40
20
16
12
8
4
0


Switching Characteristics
V_{GS} = 10 V
PW = 2 µs, duty < 1%
$t_{d\ (off)}$
t_f
t_r
$t_{d\ (on)}$
Switching Time t (ns)
Drain Current I_D (A)
500
200
100
50
20
10
5
0.2
0.5
1.0
2
5
10
20

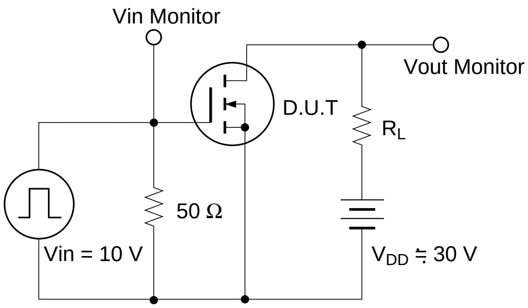


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5, 10 V
V_{GS} = 0, –10 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
4
8
12
16
20

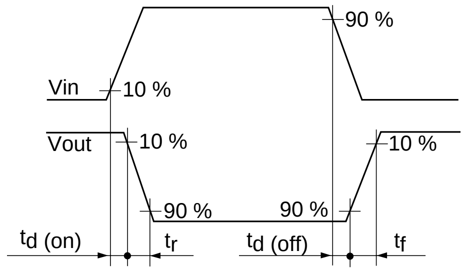


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 2.08°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1159, 2SK1160

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

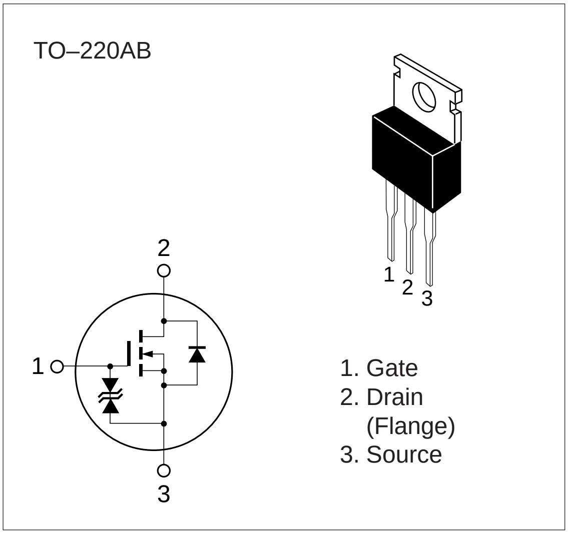


Table 1 Absolute Maximum Ratings (Ta = 25°C)

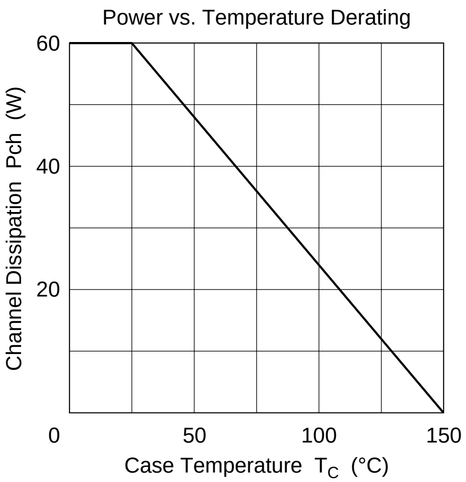
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1159	V_{DSS}	450	V
	2SK1160		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	8	A
Drain peak current		$I_{D(pulse)}$*	32	A
Body to drain diode reverse drain current		I_{DR}	8	A
Channel dissipation		Pch**	60	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

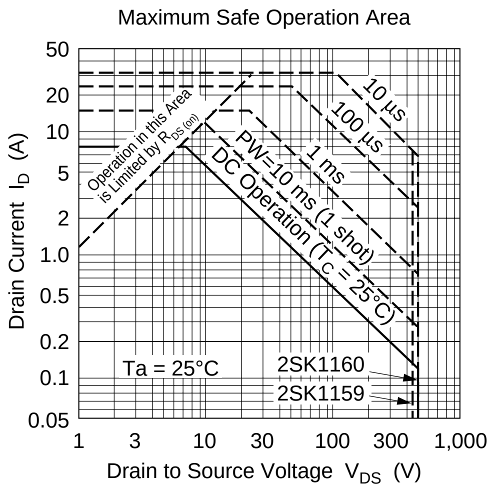
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

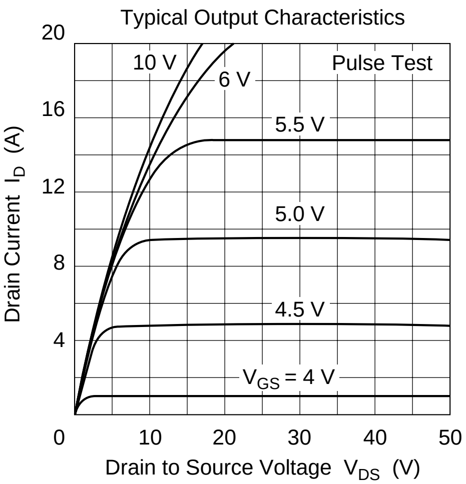
Table 2 Electrical Characteristics (Ta = 25°C)

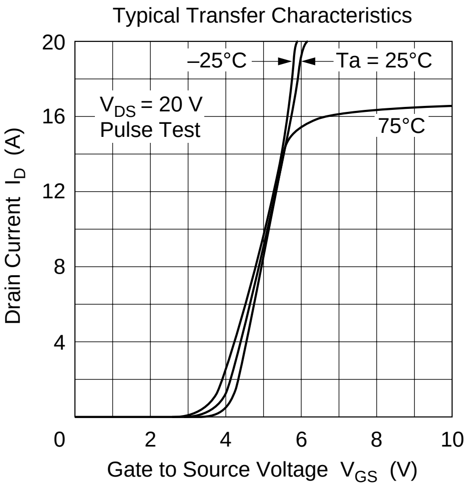
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1159	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1160		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1159	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1160						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1159	$R_{DS(on)}$	—	0.55	0.7	Ω	I_D = 4 A, V_{GS} = 10 V *
	2SK1160		—	0.60	0.8		
Forward transfer admittance		$\lvert y_{fs} \rvert$	4.5	7.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1150	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	340	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	55	—	pF	
Turn-on delay time		$t_{d(on)}$	—	17	—	ns	I_D = 4 A, V_{GS} = 10 V,
Rise time		t_r	—	55	—	ns	R_L = 7.5 Ω
Turn-off delay time		$t_{d(off)}$	—	100	—	ns	
Fall time		t_f	—	45	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body to drain diode forward voltage		t_{rr}	—	350	—	ns	I_F = 8 A, V_{GS} = 0, di_F/dt = 100 A/µs

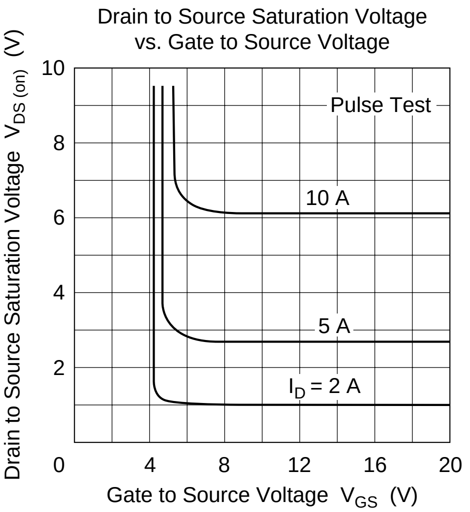
* Pulse Test

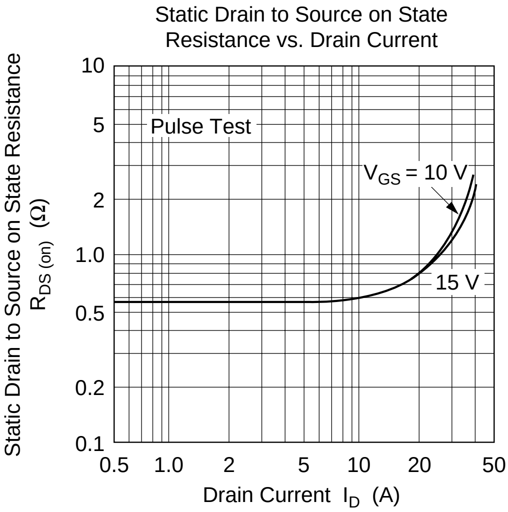

Power vs. Temperature Derating
60
40
20
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

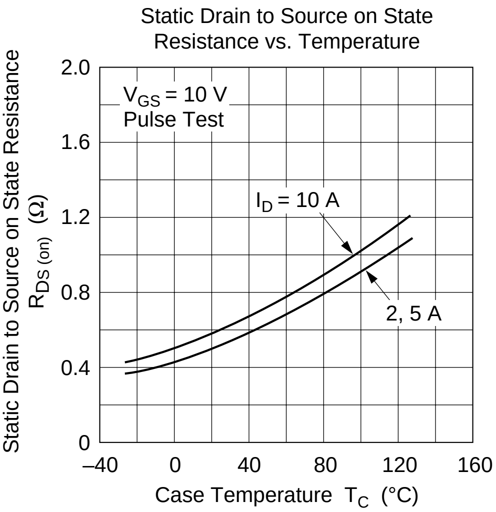

Maximum Safe Operation Area
50
20
10
5
2
1.0
0.5
0.2
0.1
0.05
1
3
10
30
100
300
1,000
Operation in this Area is Limited by $R_{DS(on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_C = 25°C)
Ta = 25°C
2SK1160
2SK1159
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

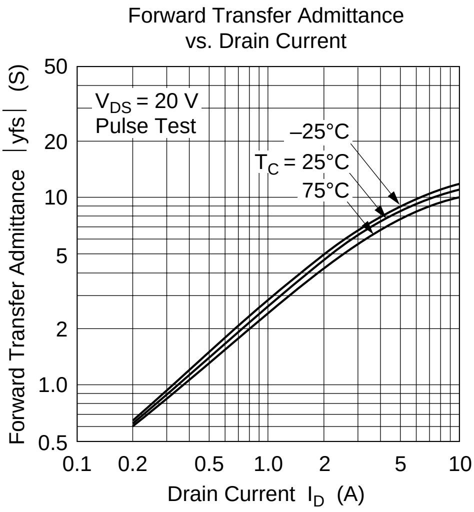

Typical Output Characteristics
20
16
12
8
4
0
10
20
30
40
50
10 V
6 V
Pulse Test
5.5 V
5.0 V
4.5 V
V_{GS} = 4 V
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

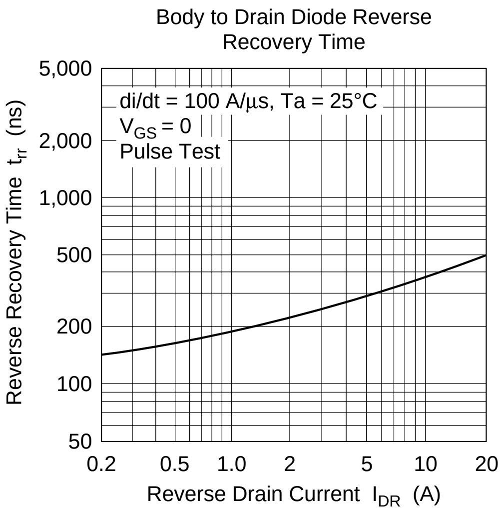

Typical Transfer Characteristics
20
16
12
8
4
0
2
4
6
8
10
–25°C
Ta = 25°C
V_{DS} = 20 V
Pulse Test
75°C
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

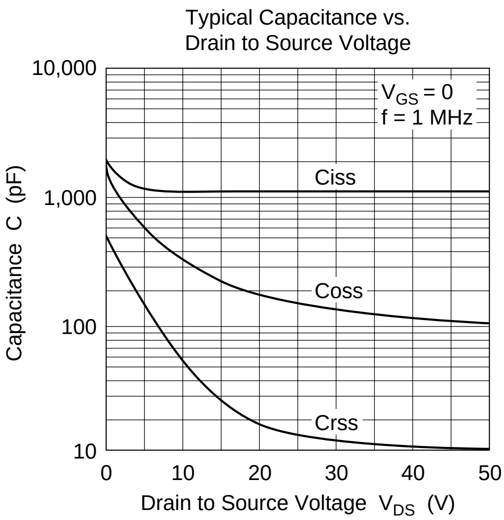

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage V DS (on) (V)
Gate to Source Voltage V GS (V)
Pulse Test
10 A
5 A
I D = 2 A
0
2
4
6
8
10
12
16
20

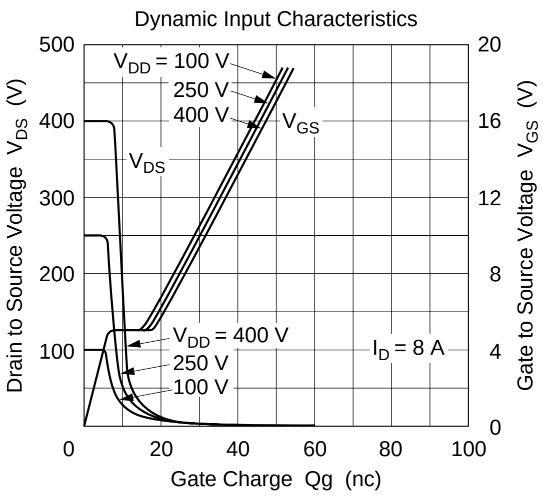

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
R DS (on) (Ω)
Drain Current I D (A)
Pulse Test
V GS = 10 V
15 V
0.1
0.2
0.5
1.0
2
5
10
20
50

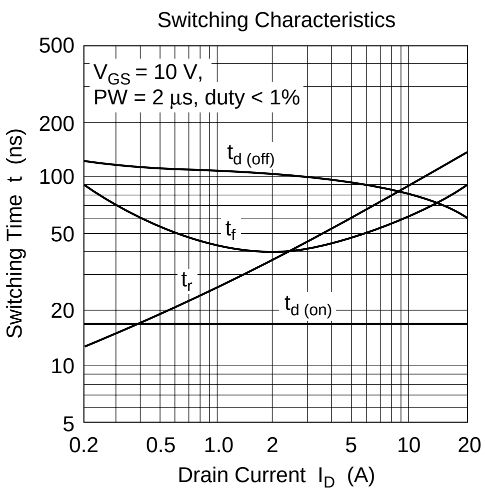

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
R DS (on) (Ω)
Case Temperature T C (°C)
V GS = 10 V
Pulse Test
I D = 10 A
2, 5 A
0
0.4
0.8
1.2
1.6
2.0
–40
0
40
80
120
160


Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
V DS = 20 V
Pulse Test
–25°C
T C = 25°C
75°C
0.5
1.0
2
5
10
20
50
0.1
0.2
0.5
1.0
2
5
10

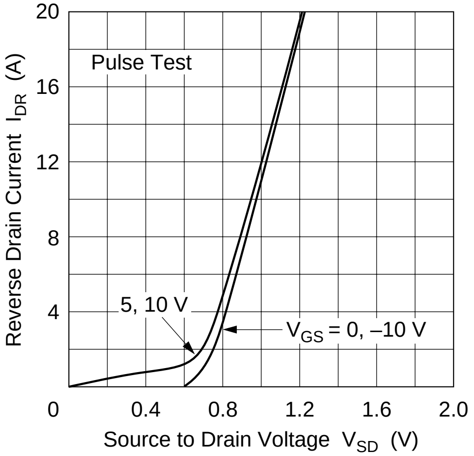

Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/µs, Ta = 25°C
V_GS = 0
Pulse Test
Reverse Recovery Time t_rr (ns)
5,000
2,000
1,000
500
200
100
50
0.2
0.5
1.0
2
5
10
20
Reverse Drain Current I_DR (A)


Typical Capacitance vs. Drain to Source Voltage
V_GS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10,000
1,000
100
10
0
10
20
30
40
50
Drain to Source Voltage V_DS (V)

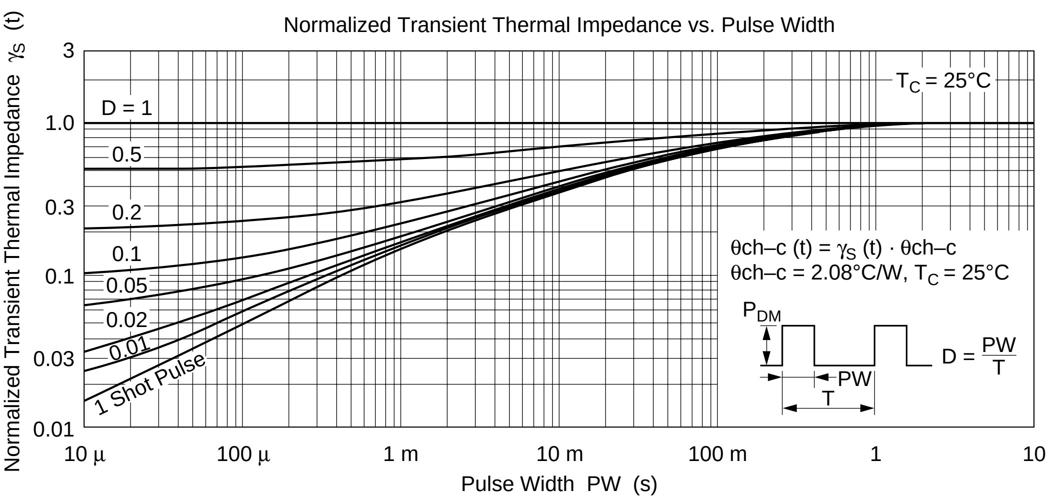

Dynamic Input Characteristics
V_DD = 100 V
250 V
400 V
V_GS
V_DS
V_DD = 400 V
250 V
100 V
I_D = 8 A
Drain to Source Voltage V_DS (V)
Gate to Source Voltage V_GS (V)
500
400
300
200
100
20
16
12
8
4
0
0
20
40
60
80
100
Gate Charge Qg (nc)

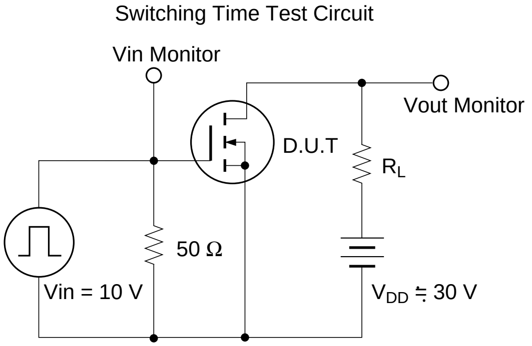

Switching Characteristics
V_GS = 10 V,
PW = 2 µs, duty < 1%
t_d (off)
t_f
t_r
t_d (on)
Switching Time t (ns)
500
200
100
50
20
10
5
0.2
0.5
1.0
2
5
10
20
Drain Current I_D (A)

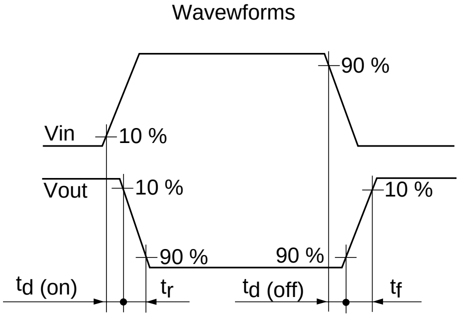
Reverse Drain Current vs.
Source to Drain Voltage



Normalized Transient Thermal Impedance vs. Pulse Width




Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T
RL
50 Ω
Vin = 10 V
VDD ≒ 30 V


Wavewforms
90 %
Vin
10 %
Vout
10 %
10 %
90 %
90 %
td (on)
tr
td (off)
tf

2SK1161, 2SK1162

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

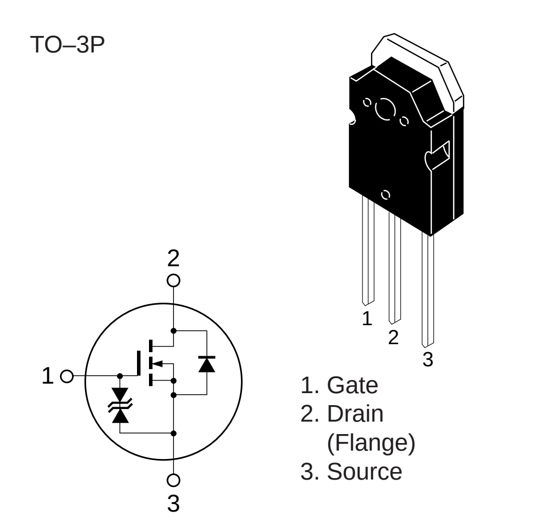


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1161	V_{DSS}	450	V
	2SK1162		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	10	A
Drain peak current		$I_{D(pulse)}$*	30	A
Body to drain diode reverse drain current		I_{DR}	10	A
Channel dissipation		Pch**	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

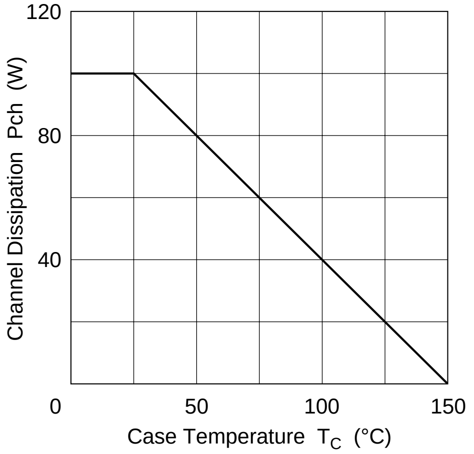
Table 2 Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1161	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1162		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1161	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1162						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1161	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 5 A, V_{GS} = 10 V *
	2SK1162		—	0.7	0.9		
Forward transfer admittance		$\|y_{fs}\|$	4.0	7.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1050	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance		Coss	—	280	—	pF	
Reverse transfer capacitance		Crss	—	40	—	pF	
Turn-on delay time		$t_{d(on)}$	—	15	—	ns	I_D = 5 A, V_{GS} = 10 V, R_L = 6 Ω
Rise time		t_r	—	60	—	ns	
Turn-off delay time		$t_{d(off)}$	—	90	—	ns	
Fall time		t_f	—	45	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	350	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 100 A/µs

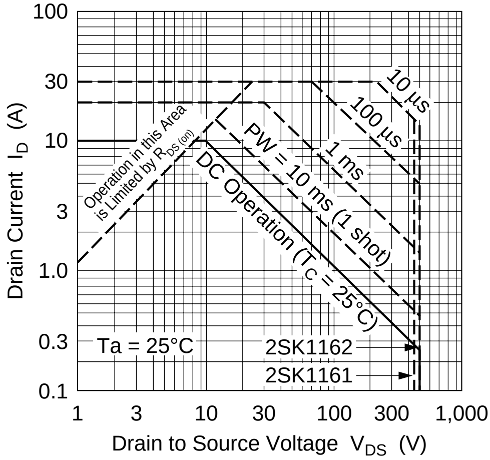
* Pulse Test

See characteristic curves of 2SK1157, 2SK1158.

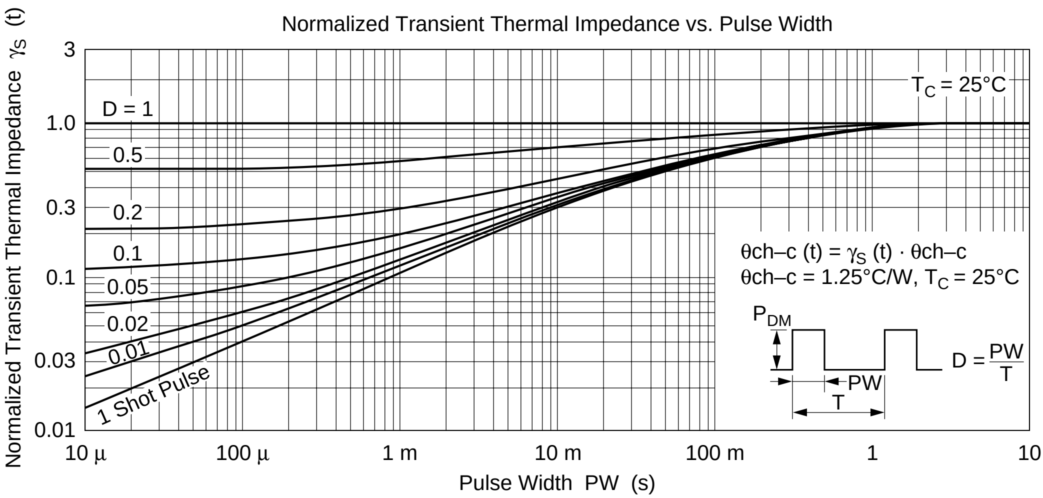
Power vs. Temperature Derating



Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width



2SK1163, 2SK1164

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

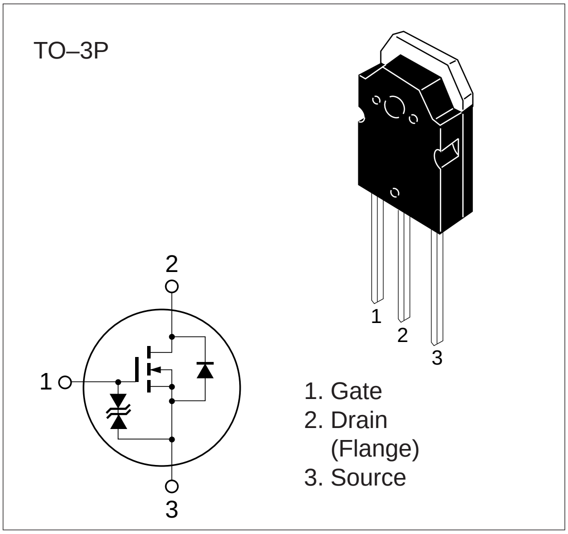


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1163	V_{DSS}	450	V
	2SK1164		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	11	A
Drain peak current		$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current		I_{DR}	11	A
Channel dissipation		Pch**	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

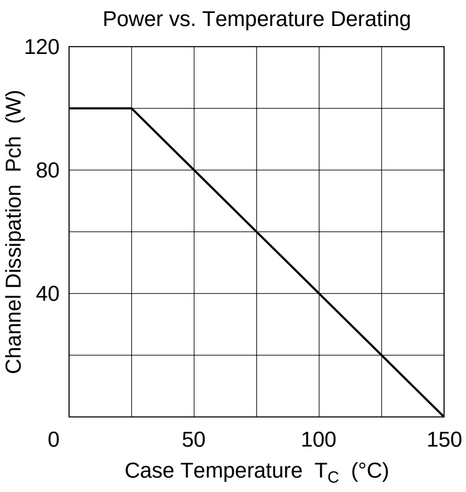
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

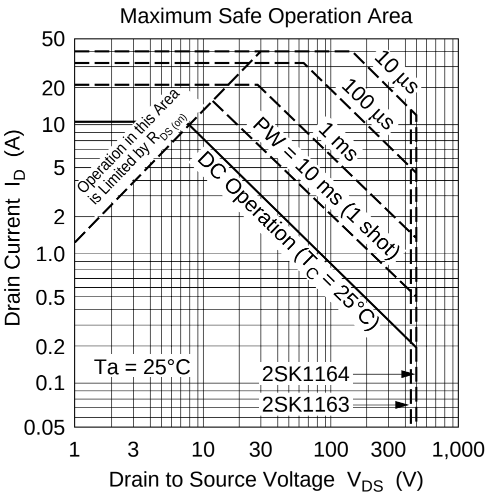
Table 2 Electrical Characteristics (Ta = 25°C)

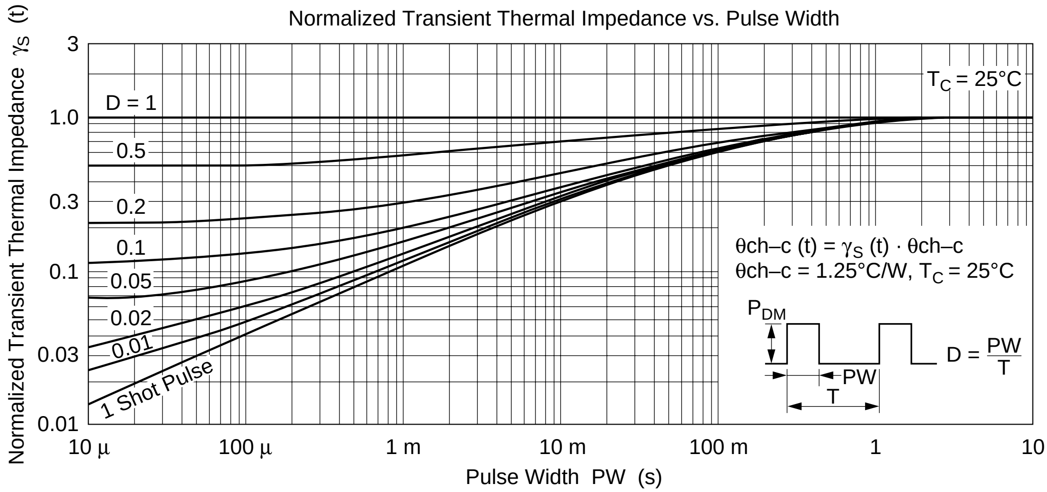
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1163	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1164		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1163	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1164						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1163	$R_{DS(on)}$	—	0.55	0.7	Ω	I_D = 5 A, V_{GS} = 10 V *
	2SK1164		—	0.60	0.8		
Forward transfer admittance		$\|y_{fs}\|$	5.0	8.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1150	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	340	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	55	—	pF	
Turn-on delay time		$t_{d(on)}$	—	17	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time		t_r	—	60	—	ns	R_L = 6 Ω
Turn-off delay time		$t_{d(off)}$	—	95	—	ns	
Fall time		t_f	—	50	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 11 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	400	—	ns	I_F = 11 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

See characteristic curves of 2SK1159, 2SK1160.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
120
80
40
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
50
20
10
5
2
1.0
0.5
0.2
0.1
0.05
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS(on)}$
Ta = 25°C
2SK1164
2SK1163


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 1.25°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$

2SK1165, 2SK1166

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

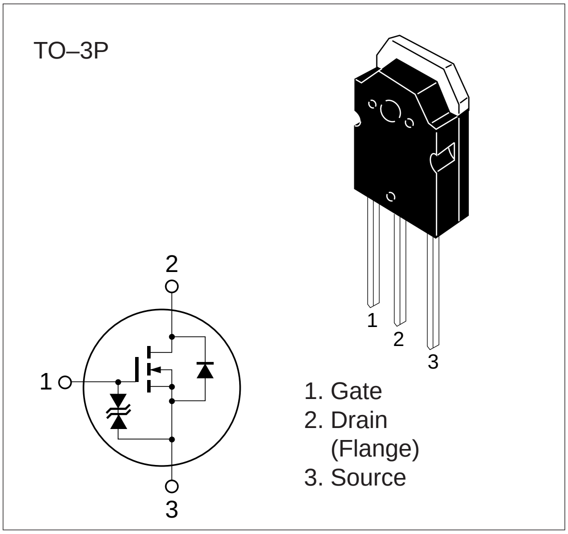


Table 1 Absolute Maximum Ratings (Ta = 25°C)

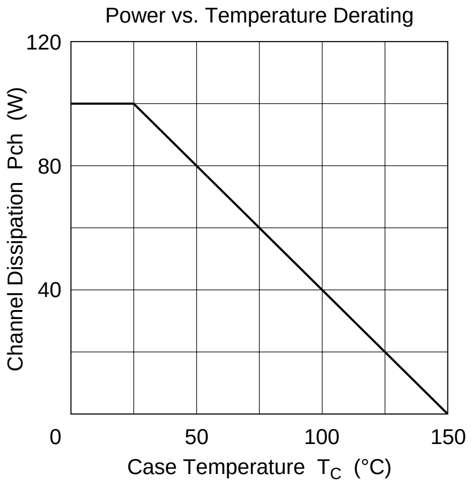
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1165	V_{DSS}	450	V
	2SK1166		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	12	A
Drain peak current		$I_{D(pulse)}$*	48	A
Body to drain diode reverse drain current		I_{DR}	12	A
Channel dissipation		Pch**	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

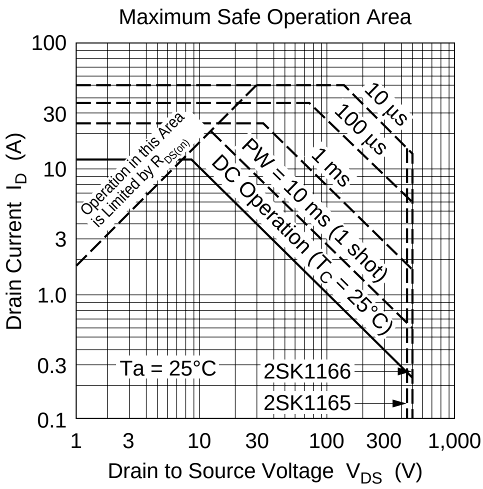
Table 2 Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1165	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1166		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1165	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1166						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1165	$R_{DS(on)}$	—	0.40	0.55	Ω	I_D = 6 A, V_{GS} = 10 V *
	2SK1166		—	0.45	0.60		
Forward transfer admittance		$\|y_{fs}\|$	6.0	10	—	S	I_D = 6 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1450	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	410	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	55	—	pF	
Turn-on delay time		$t_{d(on)}$	—	20	—	ns	I_D = 6 A, V_{GS} = 10 V,
Rise time		t_r	—	70	—	ns	R_L = 5 Ω
Turn-off delay time		$t_{d(off)}$	—	120	—	ns	
Fall time		t_f	—	60	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 12 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	450	—	ns	I_F = 12 A, V_{GS} = 0, di_F/dt = 100 A/µs

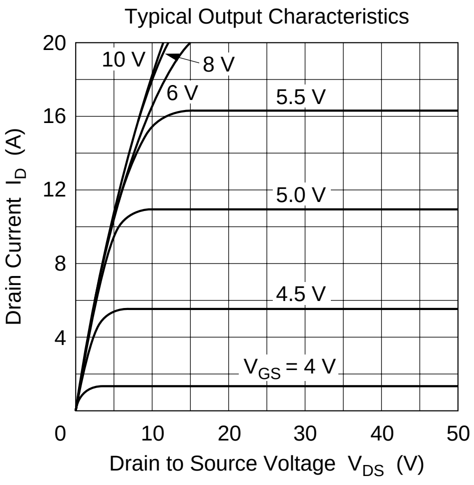
* Pulse Test



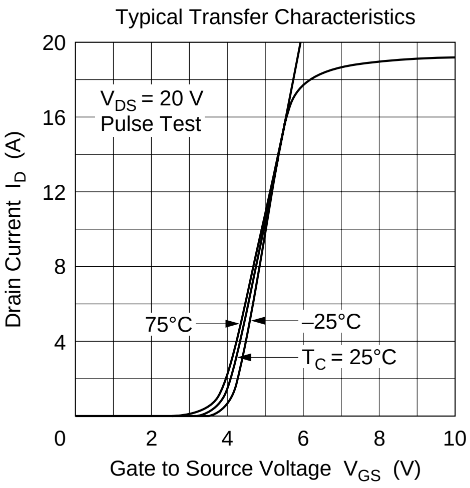
Power vs. Temperature Derating
120
80
40
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)



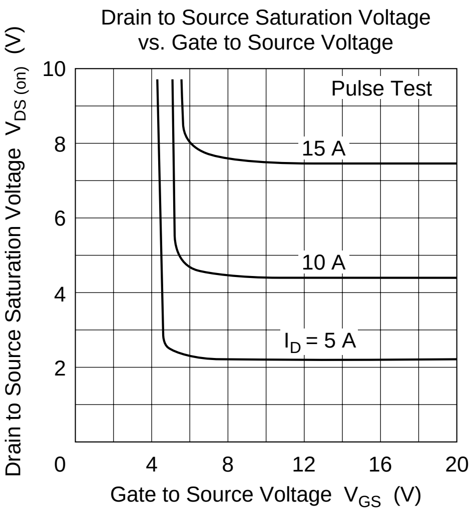
Maximum Safe Operation Area
100
30
10
3
1.0
0.3
0.1
1
3
10
30
100
300
1,000
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS(on)}$
Ta = 25°C
2SK1166
2SK1165
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

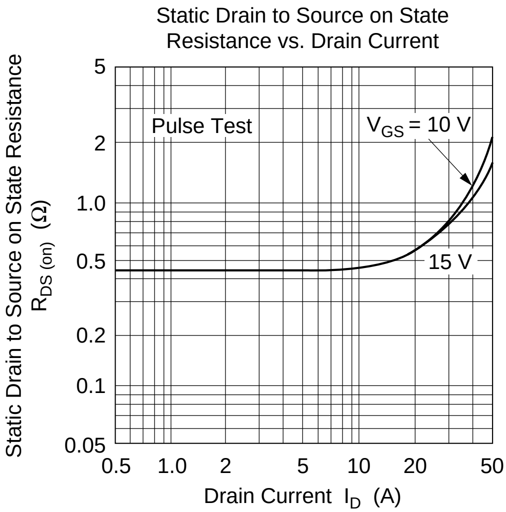


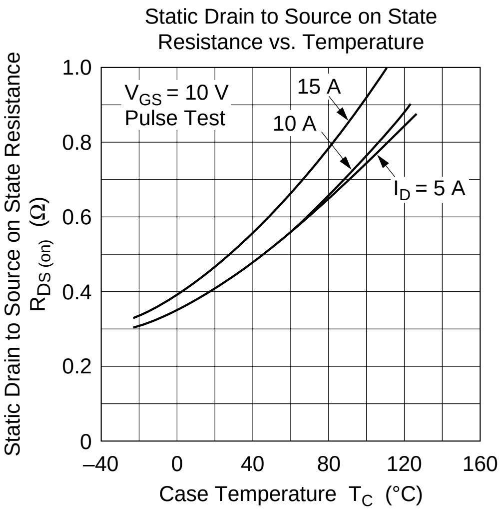
Typical Output Characteristics
20
16
12
8
4
0
10
20
30
40
50
10 V
8 V
6 V
5.5 V
5.0 V
4.5 V
V_{GS} = 4 V
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

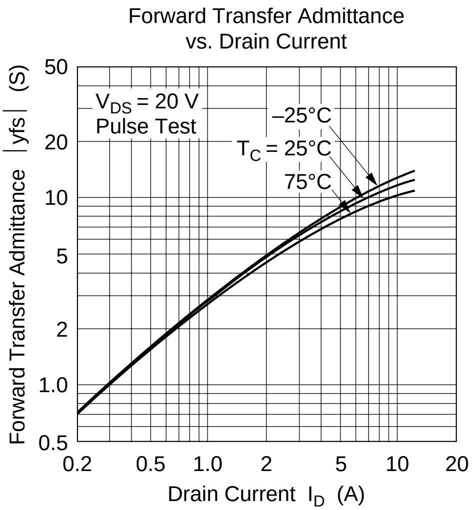


Typical Transfer Characteristics
20
16
12
8
4
0
2
4
6
8
10
V_{DS} = 20 V
Pulse Test
75°C
–25°C
T_C = 25°C
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

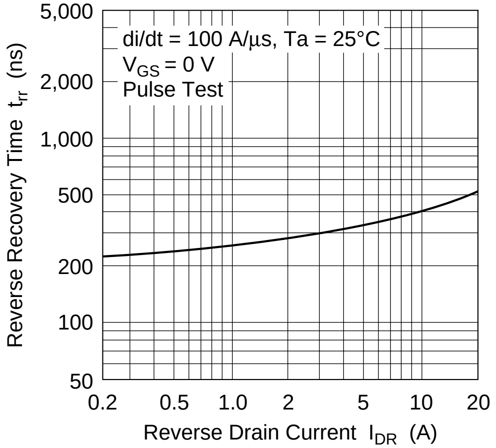

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage V_DS (on) (V)
Gate to Source Voltage V_GS (V)
Pulse Test
15 A
10 A
I_D = 5 A
0
2
4
6
8
10
4
8
12
16
20


Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
R_DS (on) (Ω)
Drain Current I_D (A)
Pulse Test
V_GS = 10 V
15 V
5
2
1.0
0.5
0.2
0.1
0.05
0.5
1.0
2
5
10
20
50

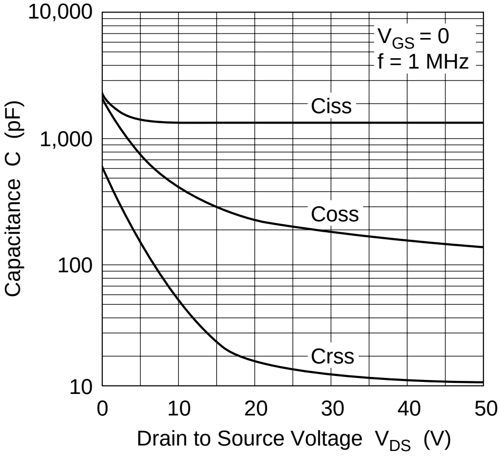

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
R_DS (on) (Ω)
Case Temperature T_C (°C)
V_GS = 10 V
Pulse Test
15 A
10 A
I_D = 5 A
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160


Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
V_DS = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
50
20
10
5
2
1.0
0.5
0.2
0.5
1.0
2
5
10
20

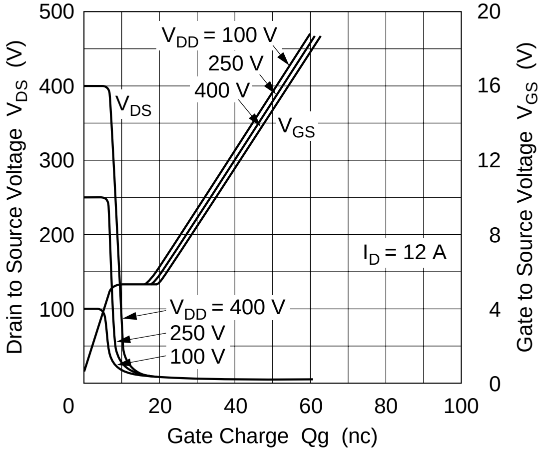
Body to Drain Diode Reverse Recovery Time



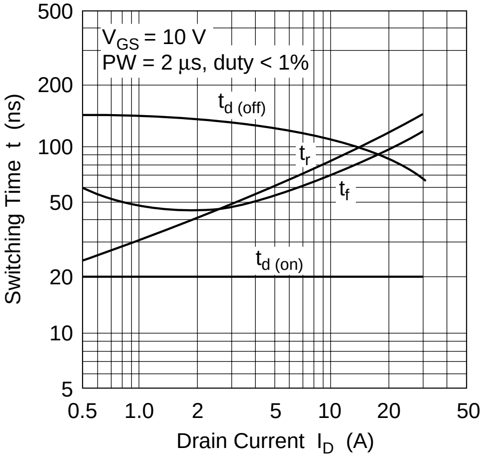
Typical Capacitance vs. Drain to Source Voltage

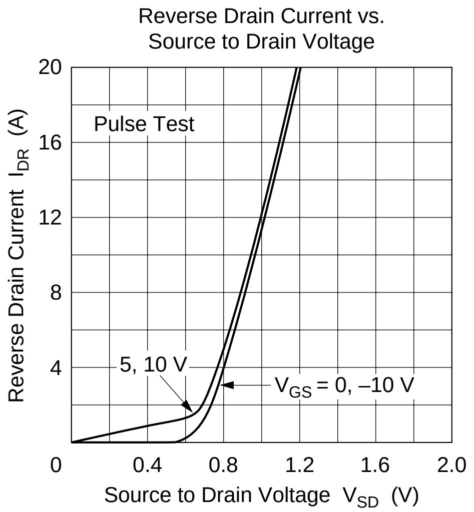


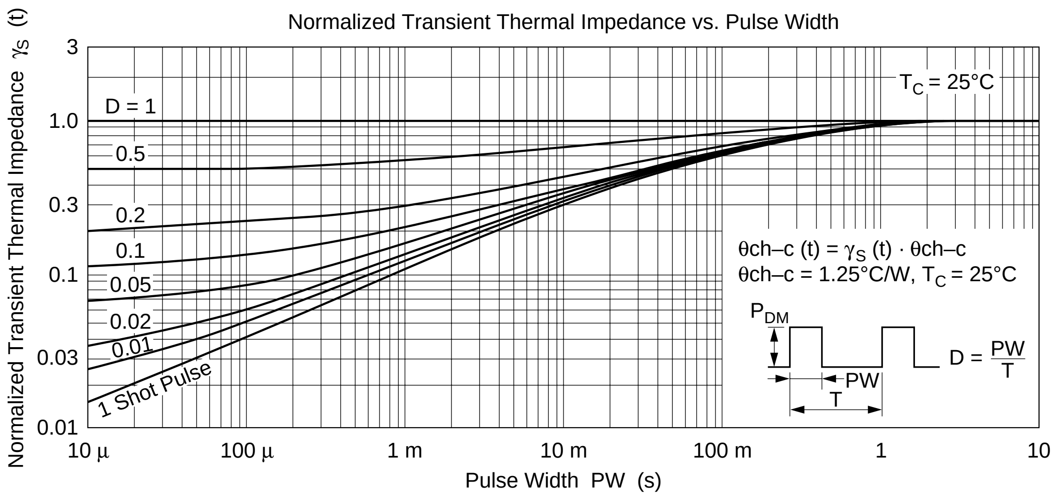
Dynamic Input Characteristics

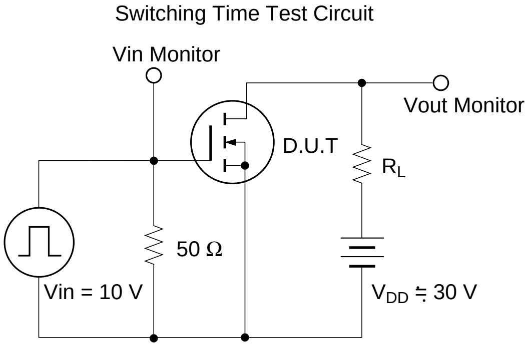


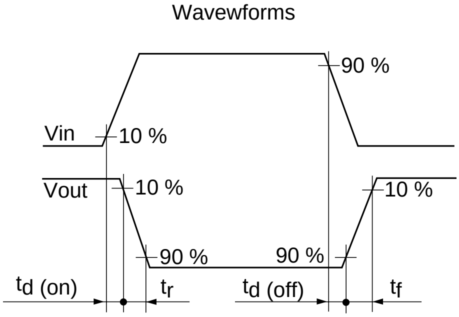
Switching Characteristics




Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5, 10 V
V_{GS} = 0, –10 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
4
8
12
16
20


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 1.25°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
10 µ
100 µ
1 m
10 m
100 m
1
10
3
1.0
0.3
0.1
0.03
0.01


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T
RL
50 Ω
Vin = 10 V
VDD ≒ 30 V


Wavewforms
90 %
Vin
10 %
Vout
10 %
10 %
90 %
90 %
td (on)
tr
td (off)
tf

2SK1167, 2SK1168

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

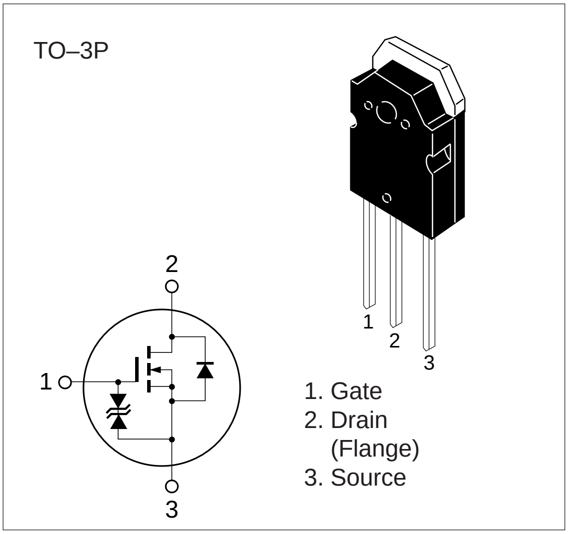


Table 1 Absolute Maximum Ratings (Ta = 25°C)

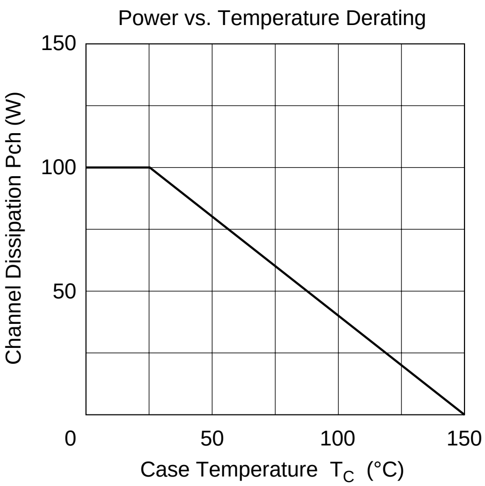
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1167	V_{DSS}	450	V
	2SK1168		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	15	A
Drain peak current		$I_{D(pulse)}$*	60	A
Body to drain diode reverse drain current		I_{DR}	15	A
Channel dissipation		Pch**	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

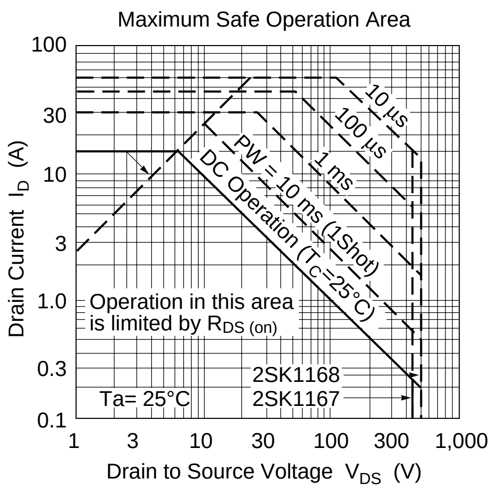
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

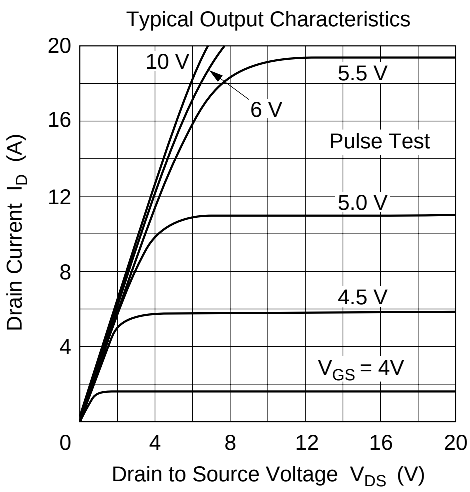
Table 2 Electrical Characteristics (Ta = 25°C)

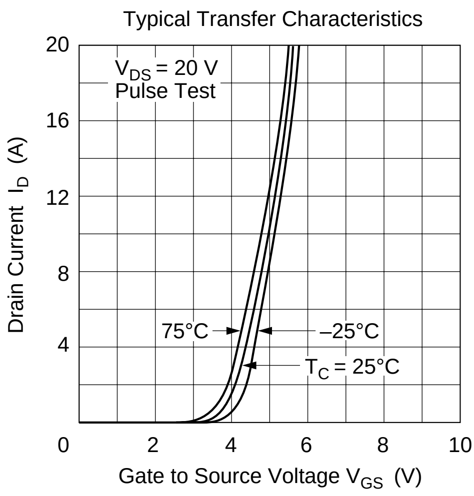
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1167	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1168		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1167	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1168						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1167	$R_{DS(on)}$	—	0.25	0.36	Ω	I_D = 8 A, V_{GS} = 10 V *
	2SK1168		—	0.30	0.40		
Forward transfer admittance		$\|y_{fs}\|$	8	13	—	S	I_D = 8 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	2050	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	600	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	75	—	pF	
Turn-on delay time		$t_{d(on)}$	—	30	—	ns	I_D = 8 A, V_{GS} = 10 V,
Rise time		t_r	—	110	—	ns	R_L = 3.75 Ω
Turn-off delay time		$t_{d(off)}$	—	150	—	ns	
Fall time		t_f	—	70	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 15 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	500	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 100 A/µs

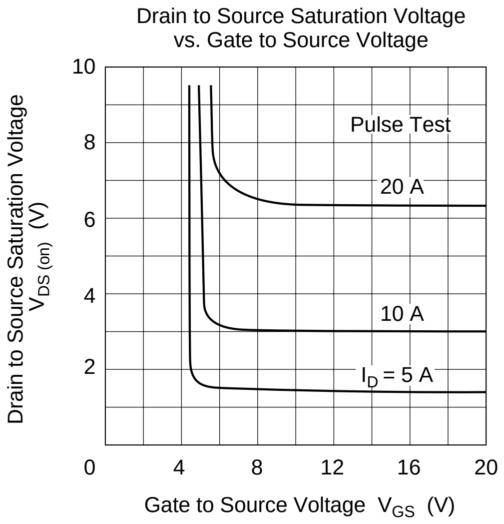
* Pulse Test

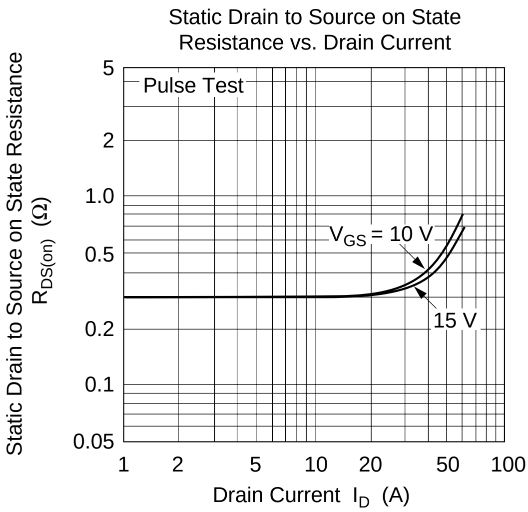

Power vs. Temperature Derating
150
100
50
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

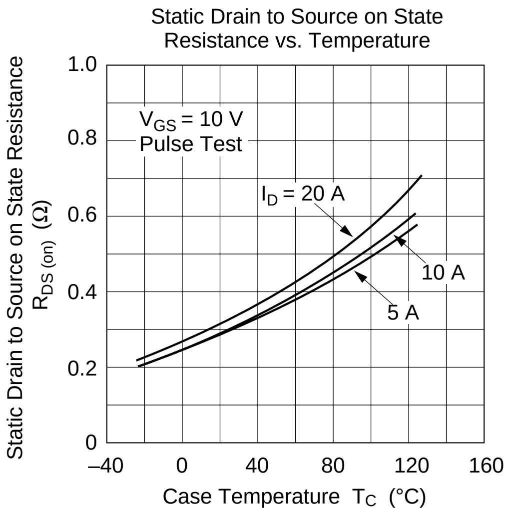

Maximum Safe Operation Area
100
30
10
3
1.0
0.3
0.1
1
3
10
30
100
300
1,000
10 µs
100 µs
1 ms
PW = 10 ms (1Shot)
DC Operation (T_C=25°C)
Operation in this area
is limited by $R_{DS (on)}$
2SK1168
2SK1167
Ta= 25°C
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

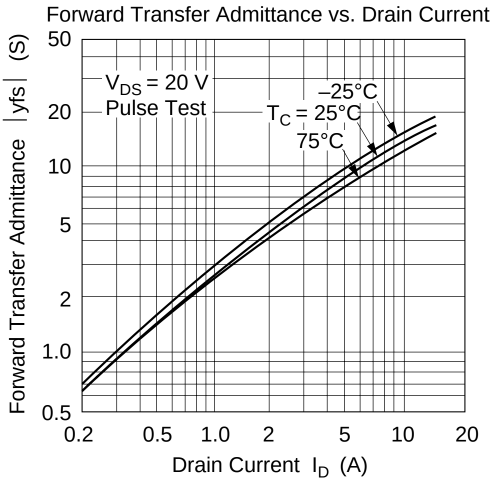

Typical Output Characteristics
20
16
12
8
4
0
4
8
12
16
20
10 V
6 V
5.5 V
Pulse Test
5.0 V
4.5 V
V_{GS} = 4V
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

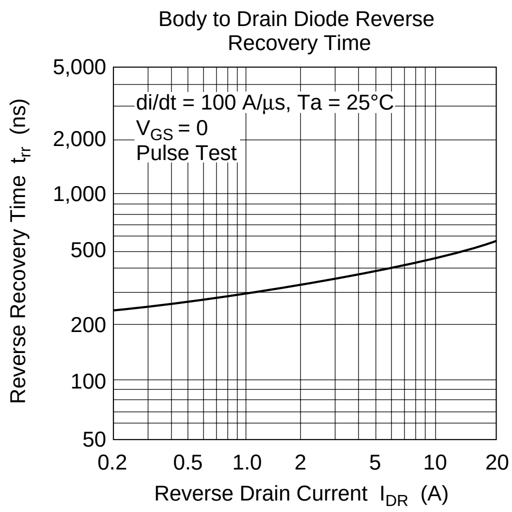

Typical Transfer Characteristics
20
16
12
8
4
0
2
4
6
8
10
V_{DS} = 20 V
Pulse Test
75°C
–25°C
T_C = 25°C
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)


Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS(on)}$ (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
20 A
10 A
I_D = 5 A
0
4
8
12
16
20
2
4
6
8
10

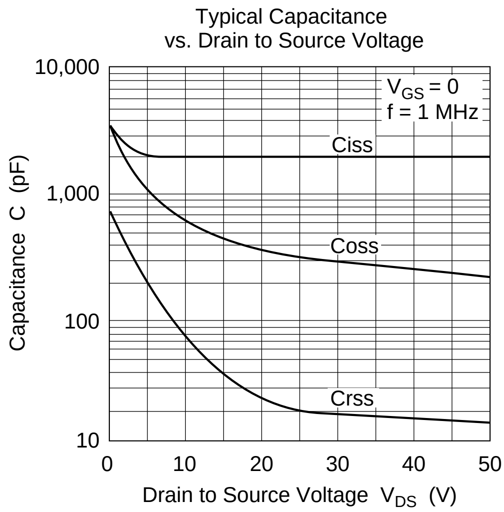

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 10 V
15 V
5
2
1.0
0.5
0.2
0.1
0.05
1
2
5
10
20
50
100


Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)
Case Temperature T_C (°C)
V_{GS} = 10 V
Pulse Test
I_D = 20 A
10 A
5 A
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160

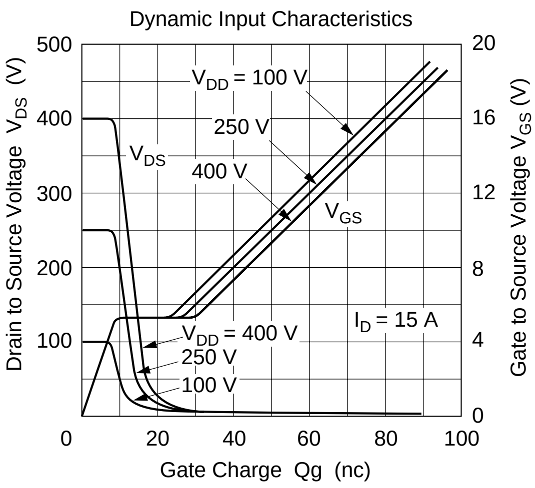

Forward Transfer Admittance vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
V_{DS} = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
50
20
10
5
2
1.0
0.5
0.2
0.5
1.0
2
5
10
20



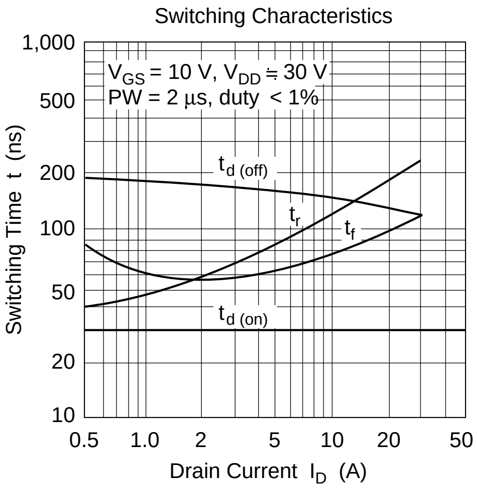
Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/µs, Ta = 25°C
V_GS = 0
Pulse Test
Reverse Recovery Time t_rr (ns)
5,000
2,000
1,000
500
200
100
50
0.2
0.5
1.0
2
5
10
20
Reverse Drain Current I_DR (A)



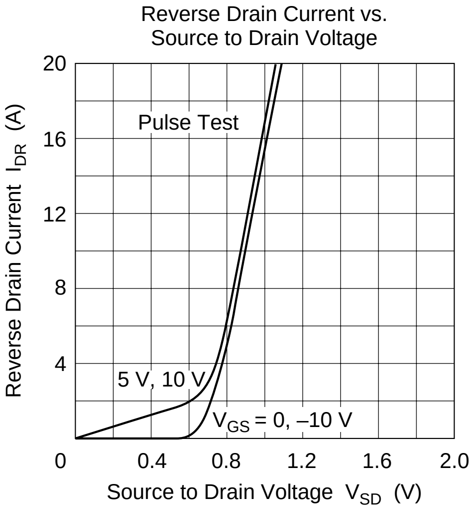
Typical Capacitance vs. Drain to Source Voltage
V_GS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10,000
1,000
100
10
0
10
20
30
40
50
Drain to Source Voltage V_DS (V)

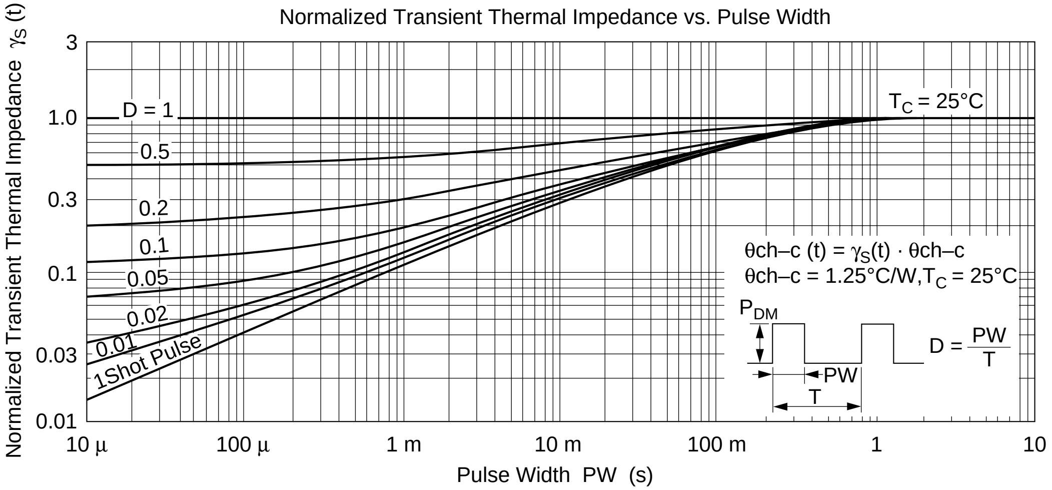


Dynamic Input Characteristics
V_DD = 100 V
250 V
400 V
V_DS
V_GS
V_DD = 400 V
250 V
100 V
I_D = 15 A
Drain to Source Voltage V_DS (V)
500
400
300
200
100
0
20
40
60
80
100
Gate to Source Voltage V_GS (V)
20
16
12
8
4
0
Gate Charge Qg (nc)

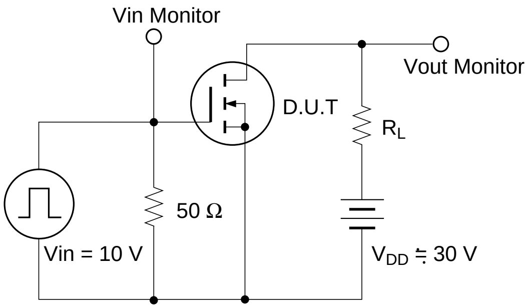


Switching Characteristics
V_GS = 10 V, V_DD ≒ 30 V
PW = 2 µs, duty < 1%
t_d (off)
t_r
t_f
t_d (on)
Switching Time t (ns)
1,000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)

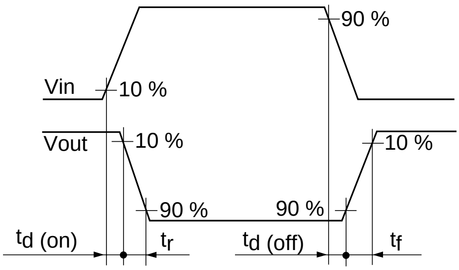

Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
20
16
12
8
4
0
Pulse Test
5 V, 10 V
V_{GS} = 0, –10 V
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1Shot Pulse
T_C = 25°C
θch–c (t) = γ_S(t) · θch–c
θch–c = 1.25°C/W,T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit



Wavewforms



2SK1169, 2SK1170

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

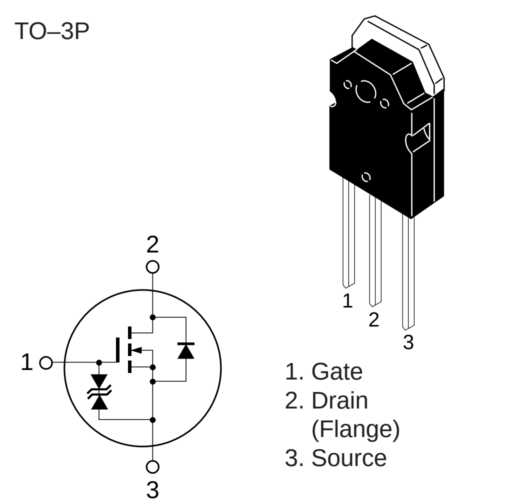


Table 1 Absolute Maximum Ratings (Ta = 25°C)

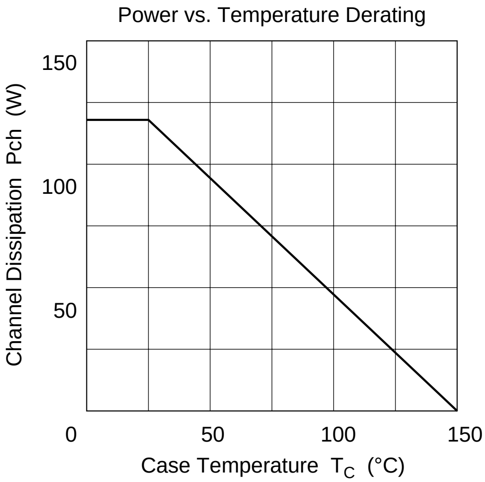
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1169	V_{DSS}	450	V
	2SK1170		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	20	A
Drain peak current		$I_{D(pulse)}{}^{*}$	80	A
Body to drain diode reverse drain current		I_{DR}	20	A
Channel dissipation		Pch**	120	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

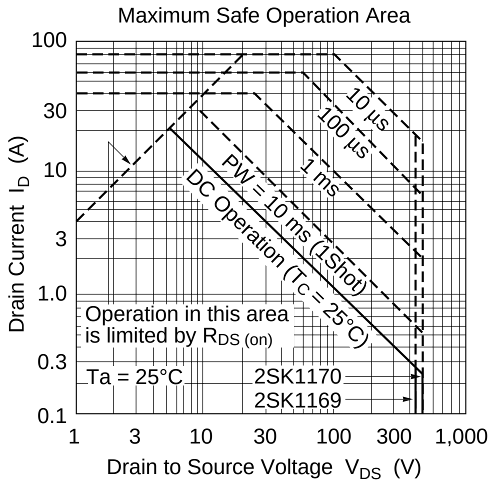
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

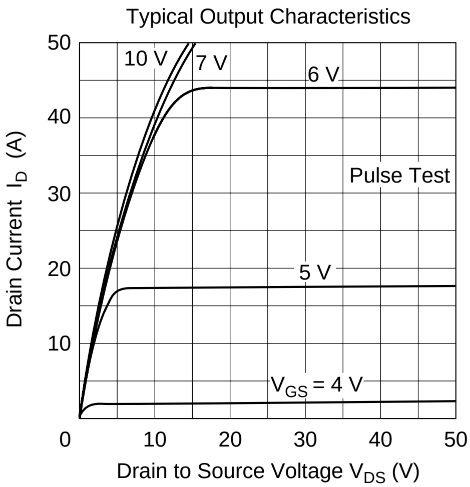
Table 2 Electrical Characteristics (Ta = 25°C)

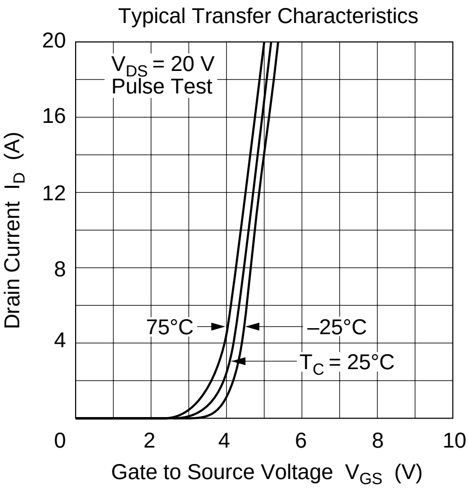
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1169	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1170		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1169	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1170						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1169	$R_{DS(on)}$	—	0.20	0.25	Ω	I_D = 10 A, V_{GS} = 10 V *
	2SK1170		—	0.22	0.27		
Forward transfer admittance		$\|y_{fs}\|$	10	16	—	S	I_D = 10 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	2800	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	780	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	90	—	pF	
Turn-on delay time		$t_{d(on)}$	—	32	—	ns	I_D = 10 A, V_{GS} = 10 V,
Rise time		t_r	—	115	—	ns	R_L = 3 Ω
Turn-off delay time		$t_{d(off)}$	—	200	—	ns	
Fall time		t_f	—	90	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 20 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	500	—	ns	I_F = 20 A, V_{GS} = 0, di_F/dt = 100 A/µs

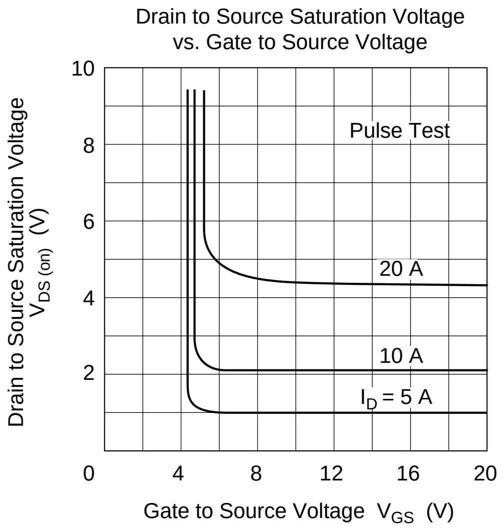
* Pulse Test

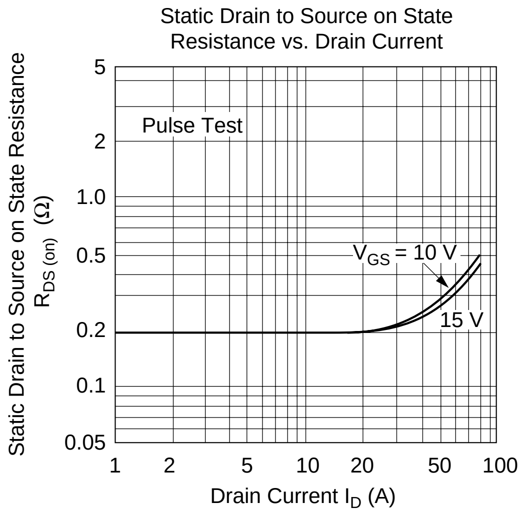

Power vs. Temperature Derating
Channel Dissipation Pch (W)
150
100
50
0
50
100
150
Case Temperature T_C (°C)

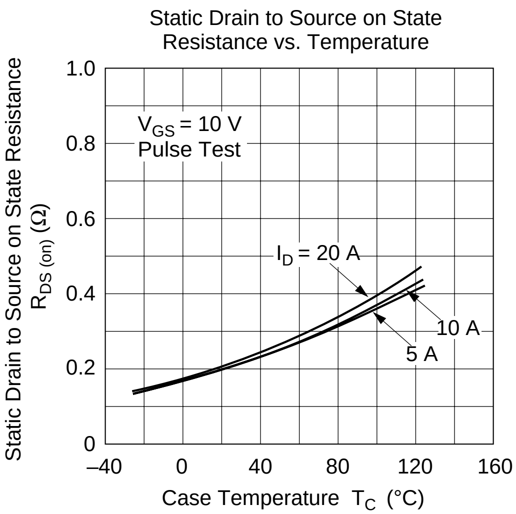

Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)
10 μs
100 μs
1 ms
PW = 10 ms (1Shot)
DC Operation (T_C = 25°C)
Operation in this area
is limited by $R_{DS (on)}$
Ta = 25°C
2SK1170
2SK1169

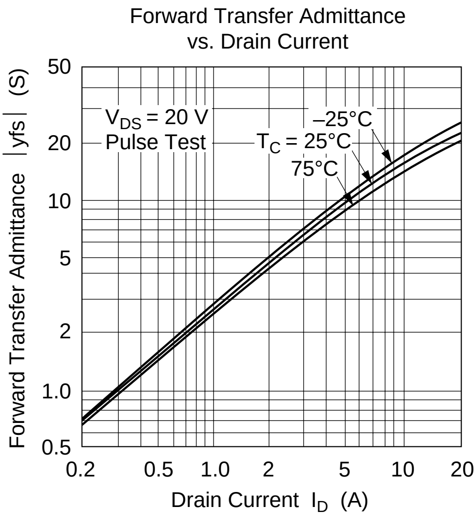

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)
10 V
7 V
6 V
Pulse Test
5 V
V_{GS} = 4 V

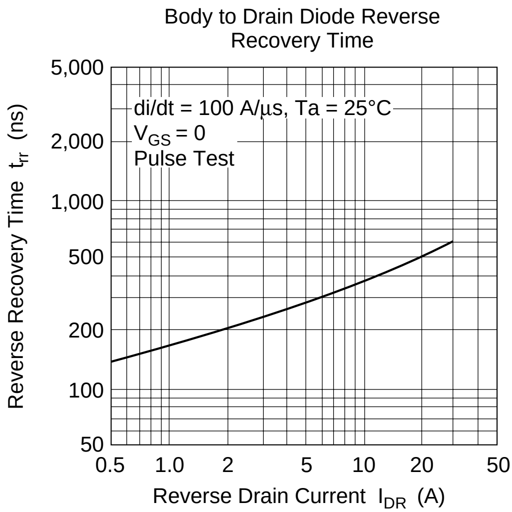

Typical Transfer Characteristics
Drain Current I_D (A)
20
16
12
8
4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)
V_{DS} = 20 V
Pulse Test
75°C
–25°C
T_C = 25°C

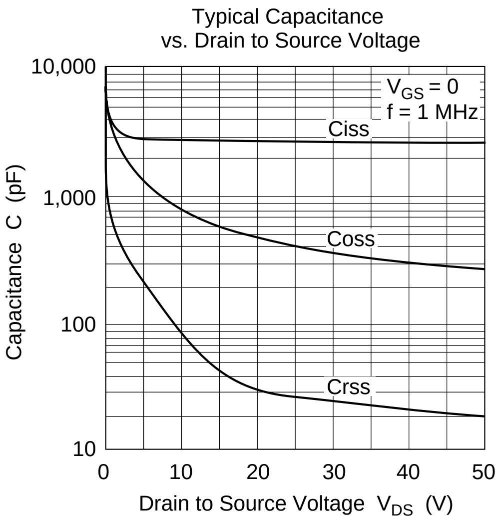

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
20 A
10 A
I_D = 5 A
Drain to Source Saturation Voltage V_DS (on) (V)
Gate to Source Voltage V_GS (V)
0
4
8
12
16
20
2
6
10

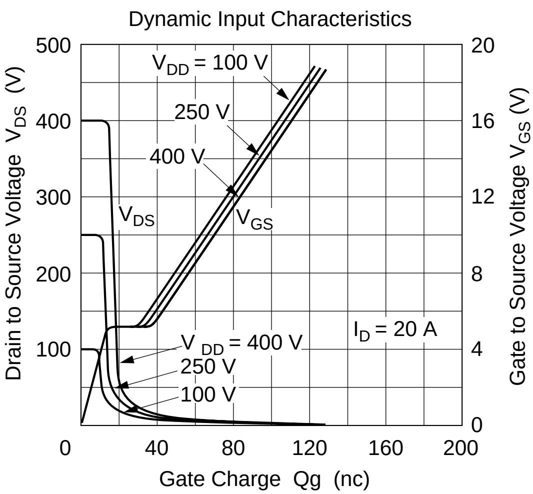

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_GS = 10 V
15 V
Static Drain to Source on State Resistance R_DS (on) (Ω)
Drain Current I_D (A)
5
2
1.0
0.5
0.2
0.1
0.05
1
2
5
10
20
50
100

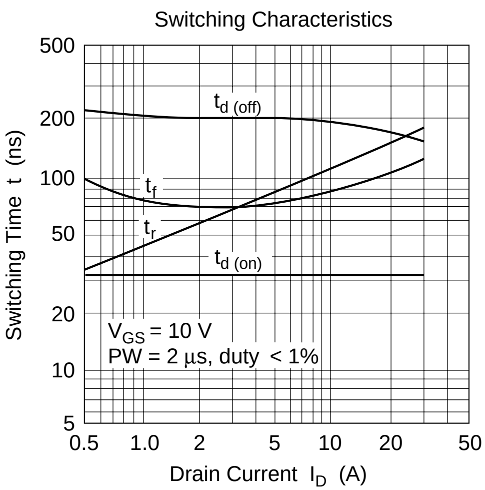

Static Drain to Source on State
Resistance vs. Temperature
V_GS = 10 V
Pulse Test
I_D = 20 A
10 A
5 A
Static Drain to Source on State Resistance R_DS (on) (Ω)
Case Temperature T_C (°C)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160

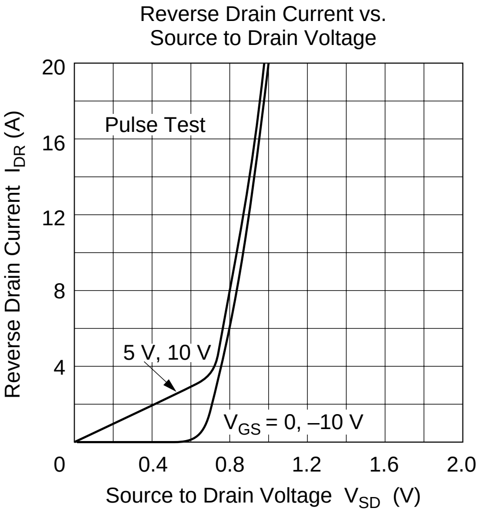

Forward Transfer Admittance
vs. Drain Current
V_DS = 20 V
Pulse Test
–25°C
T_C = 25°C
75°C
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
50
20
10
5
2
1.0
0.5
0.2
0.5
1.0
2
5
10
20


Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/μs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
5,000
2,000
1,000
500
200
100
50
0.5
1.0
2
5
10
20
50
Reverse Drain Current IDR (A)

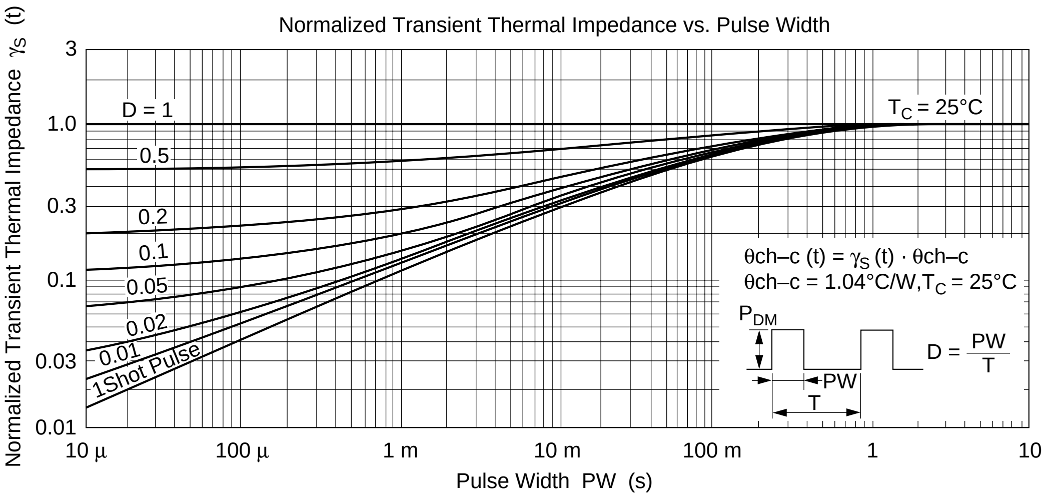

Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10,000
1,000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
VDD = 100 V
250 V
400 V
VDS
VGS
VDD = 400 V
250 V
100 V
ID = 20 A
Drain to Source Voltage VDS (V)
500
400
300
200
100
0
40
80
120
160
200
Gate Charge Qg (nc)
Gate to Source Voltage VGS (V)
20
16
12
8
4
0


Switching Characteristics
td (off)
tf
tr
td (on)
VGS = 10 V
PW = 2 μs, duty < 1%
Switching Time t (ns)
500
200
100
50
20
10
5
0.5
1.0
2
5
10
20
50
Drain Current ID (A)

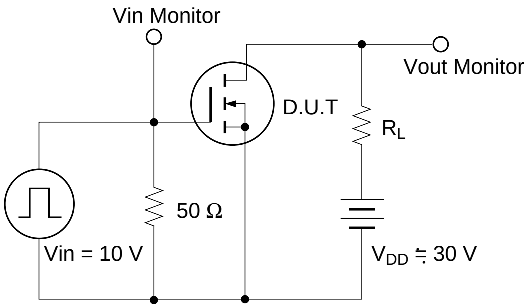


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I_DR (A)
Pulse Test
5 V, 10 V
V_GS = 0, –10 V
Source to Drain Voltage V_SD (V)
0
0.4
0.8
1.2
1.6
2.0
4
8
12
16
20

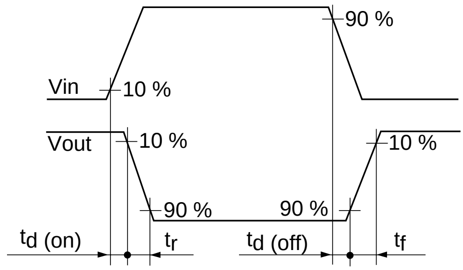


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γS (t)
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1Shot Pulse
θch–c (t) = γS (t) · θch–c
θch–c = 1.04°C/W, T_C = 25°C
P_DM
PW
T
D = PW / T
Pulse Width PW (s)
10 µ
100 µ
1 m
10 m
100 m
1
10
3
1.0
0.3
0.1
0.03
0.01

Switching Time Test Circuit



Wavewforms



2SK1254(L), 2SK1254(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

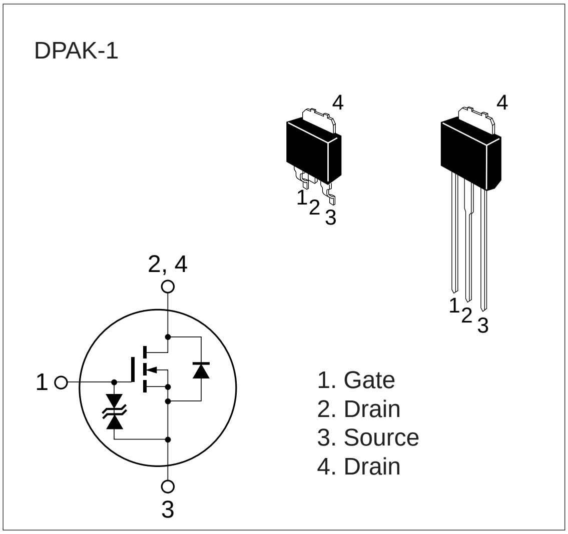


Table 1 Absolute Maximum Ratings (Ta = 25°C)

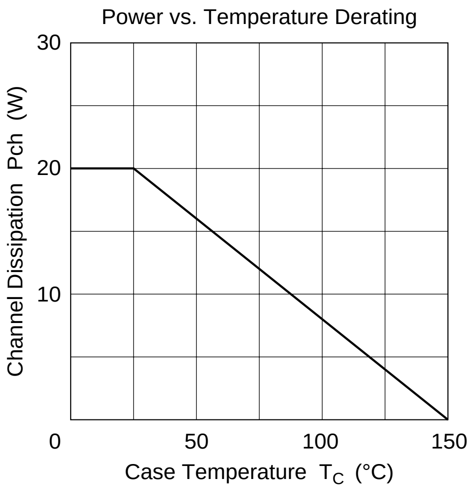
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	120	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$*	12	A
Body to drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

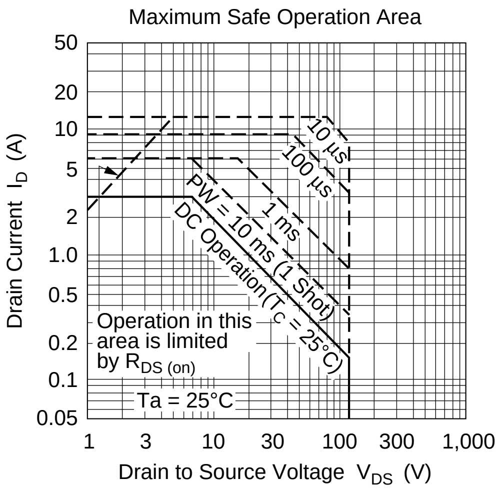
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

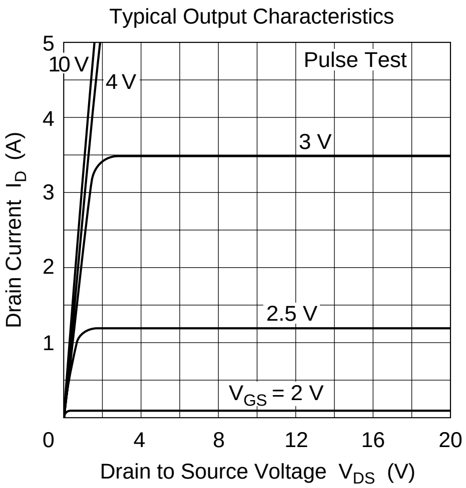
Table 2 Electrical Characteristics (Ta = 25°C)

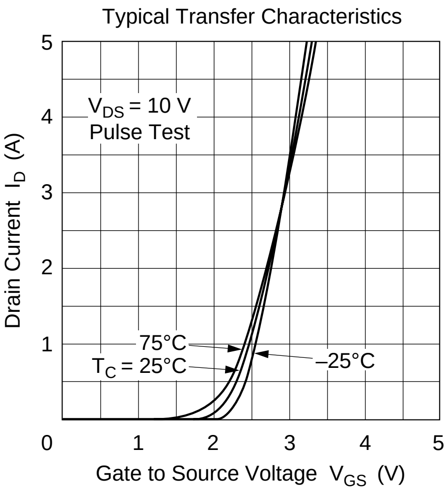
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	120	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.30	0.40	Ω	I_D = 2 A, V_{GS} = 10 V *
		—	0.35	0.55		I_D = 2 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	2.4	4.0	—	S	I_D = 2 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	420	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	190	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	25	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 2 A, V_{GS} = 10 V,
Rise time	t_r	—	20	—	ns	R_L = 15 Ω
Turn-off delay time	$t_{d(off)}$	—	150	—	ns	
Fall time	t_f	—	45	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 3 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = 3 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

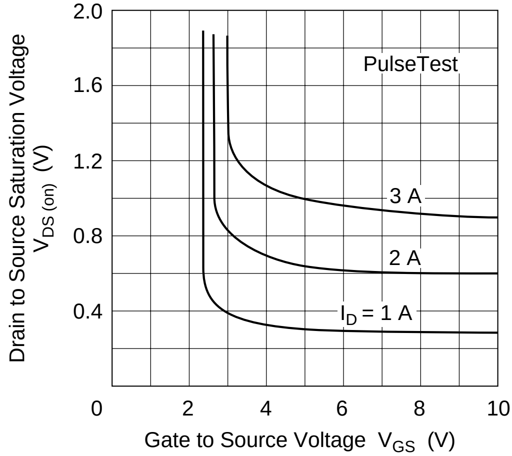

Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
50
20
10
5
2
1.0
0.5
0.2
0.1
0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this area is limited by $R_{DS\,(on)}$
Ta = 25°C
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)

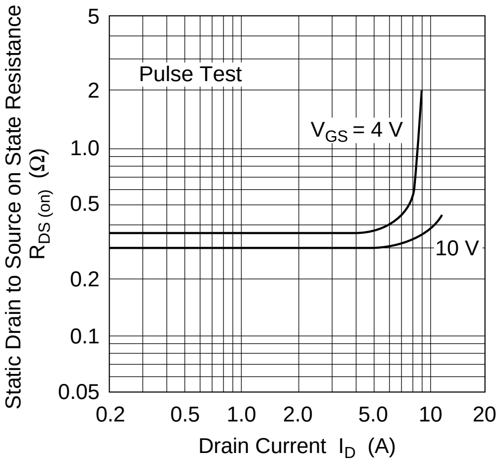

Typical Output Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
10 V
4 V
Pulse Test
3 V
2.5 V
V_{GS} = 2 V
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
Drain Current I_D (A)
5
4
3
2
1
0
V_{DS} = 10 V
Pulse Test
75°C
T_C = 25°C
–25°C
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)

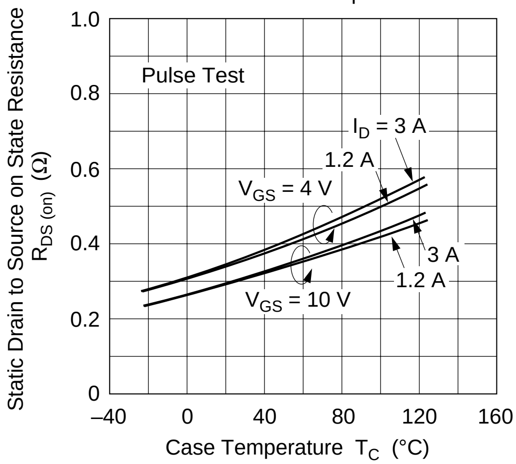
Drain to Source Saturation Voltage vs. Gate to Source Voltage



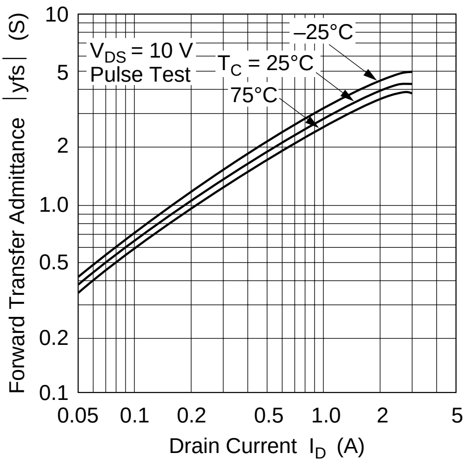
Static Drain to Source on State Resistance vs. Drain Current

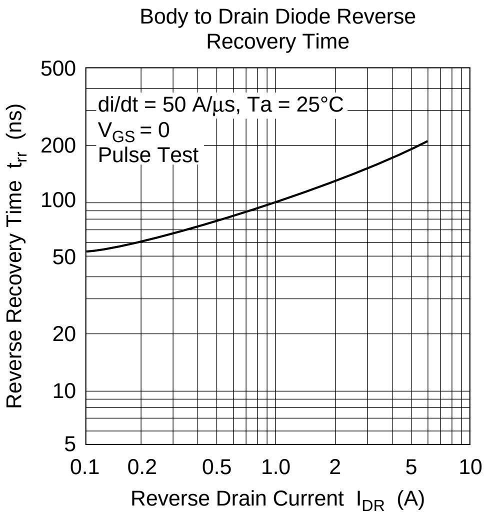


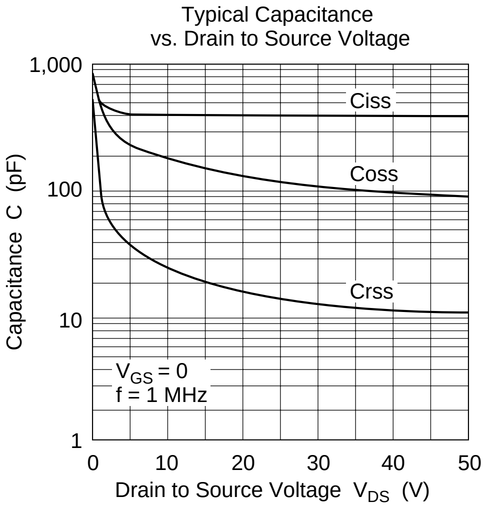
Static Drain to Source on State Resistance vs. Temperature

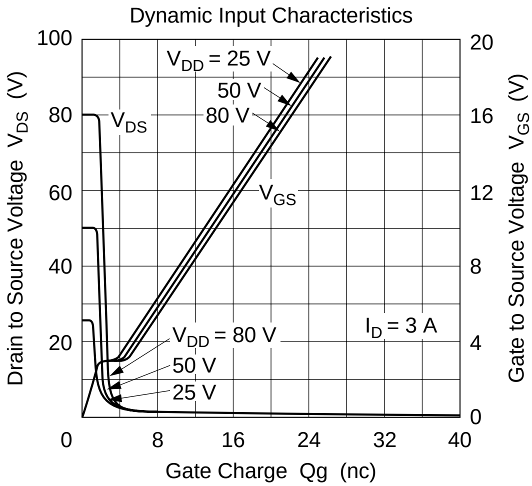


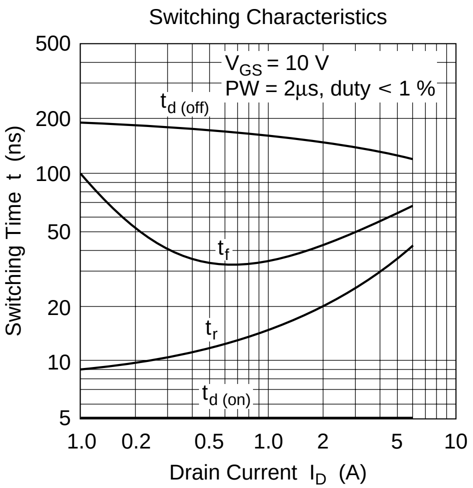
Forward Transfer Admittance vs. Drain Current

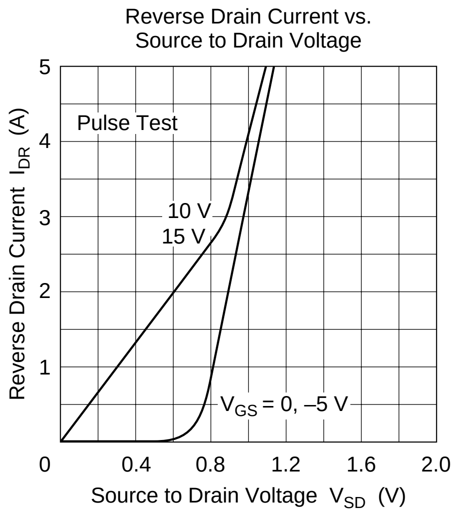



Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
Reverse Drain Current IDR (A)
500
200
100
50
20
10
5
0.1
0.2
0.5
1.0
2
5
10

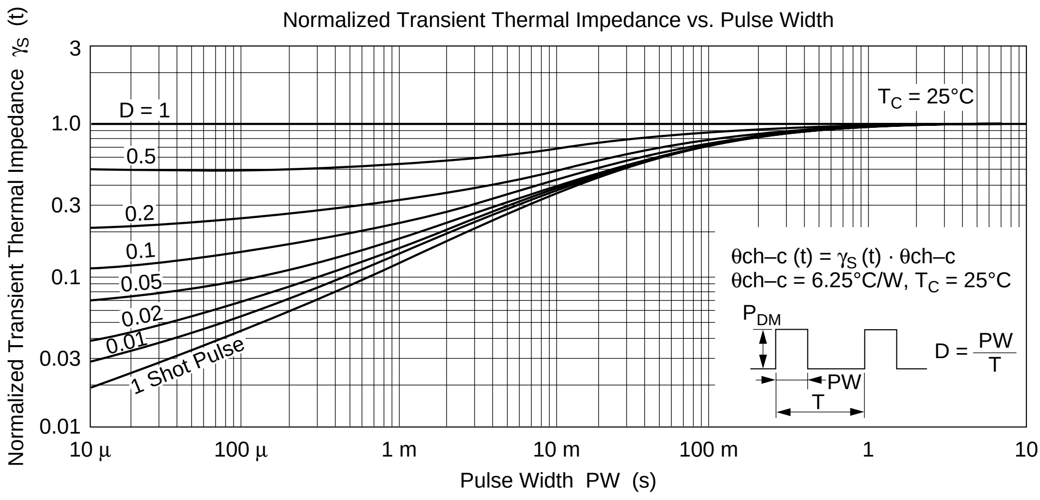

Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
Drain to Source Voltage VDS (V)
1,000
100
10
1
0
10
20
30
40
50


Dynamic Input Characteristics
VDD = 25 V
50 V
80 V
VDS
VGS
VDD = 80 V
50 V
25 V
ID = 3 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
100
80
60
40
20
0
8
16
24
32
40
20
16
12
8
4
0


Switching Characteristics
VGS = 10 V
PW = 2µs, duty < 1 %
td (off)
tf
tr
td (on)
Switching Time t (ns)
Drain Current ID (A)
500
200
100
50
20
10
5
1.0
0.2
0.5
1.0
2
5
10

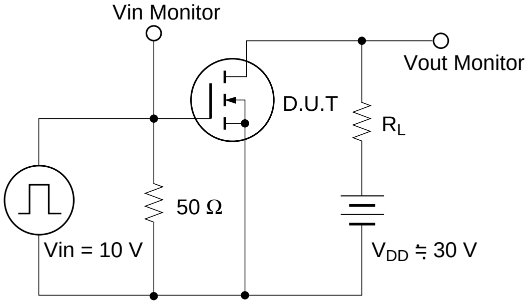


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
15 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
1
2
3
4
5

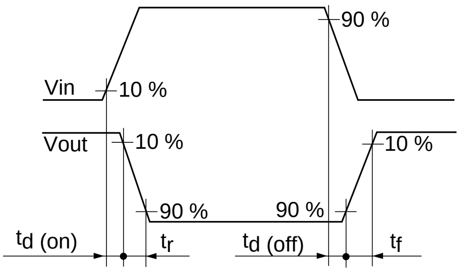


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 6.25°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1296

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

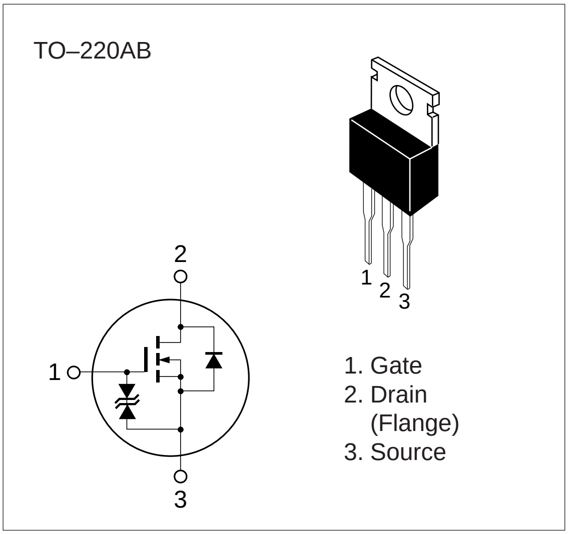


Table 1 Absolute Maximum Ratings (Ta = 25°C)

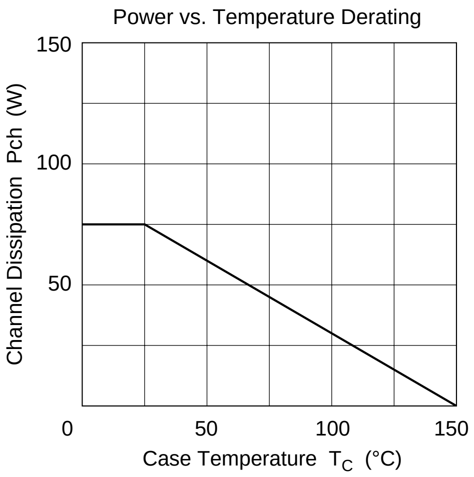
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$*	120	A
Body to drain diode reverse drain current	I_{DR}	30	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

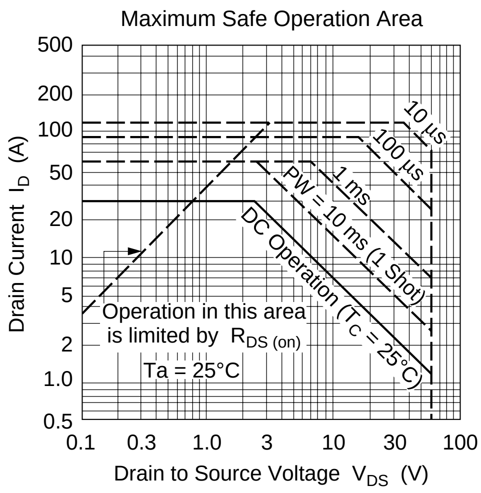
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

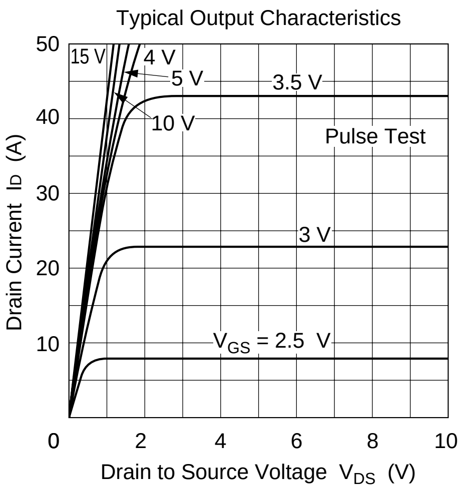
Table 2 Electrical Characteristics (Ta = 25°C)

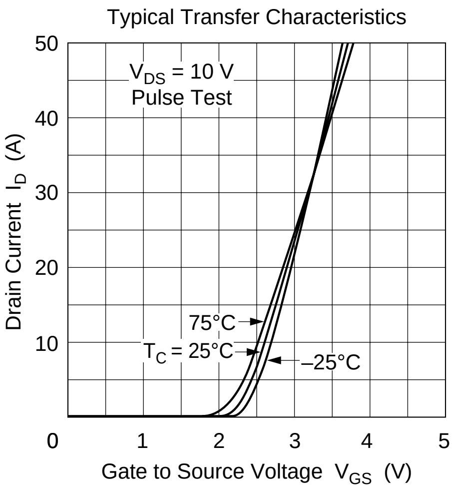
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.024	0.028	Ω	I_D = 15 A, V_{GS} = 10 V *
		—	0.030	0.040		I_D = 15 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	17	27	—	S	I_D = 15 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	2250	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	1230	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	300	—	pF	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 15 A, V_{GS} = 10 V,
Rise time	t_r	—	125	—	ns	R_L = 2 Ω
Turn-off delay time	$t_{d(off)}$	—	390	—	ns	
Fall time	t_f	—	225	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 30 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = 30 A, V_{GS} = 0, di_F/dt = 50 A/µs

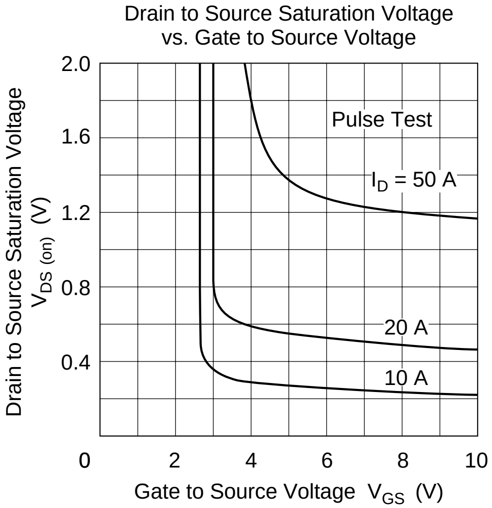
* Pulse Test

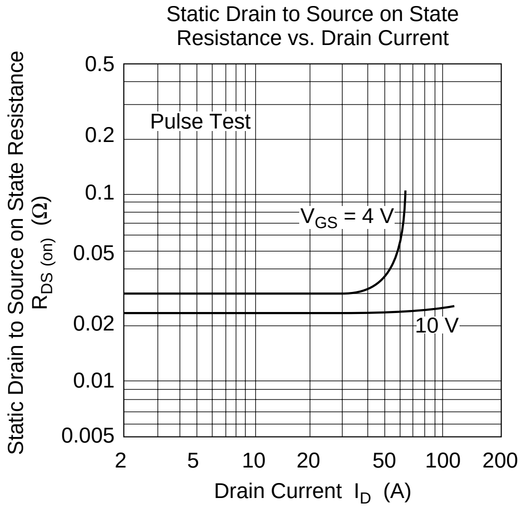

Power vs. Temperature Derating
Channel Dissipation Pch (W)
150
100
50
0
50
100
150
Case Temperature T_C (°C)

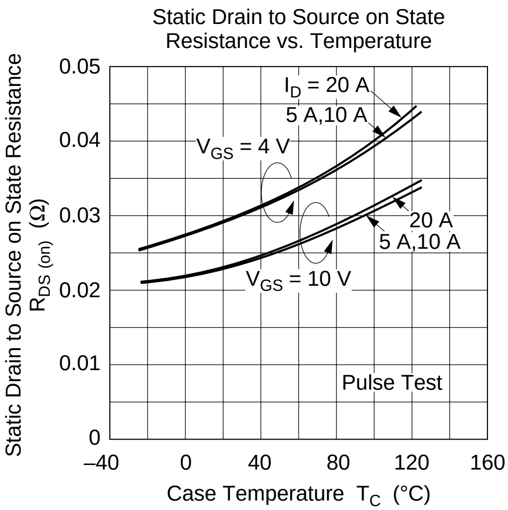

Maximum Safe Operation Area
Drain Current I_D (A)
500
200
100
50
20
10
5
2
1.0
0.5
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this area
is limited by $R_{DS (on)}$
Ta = 25°C

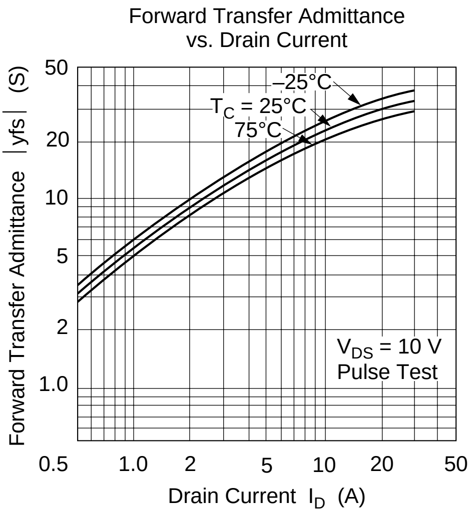

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)
15 V
4 V
5 V
3.5 V
10 V
Pulse Test
3 V
V_{GS} = 2.5 V


Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
75°C
T_C = 25°C
–25°C

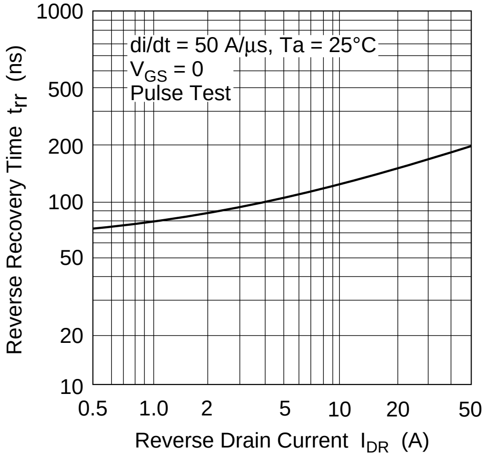

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 50 A
20 A
10 A
Drain to Source Saturation Voltage
$V_{DS\ (on)}$ (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)


Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 4 V
10 V
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I_D (A)

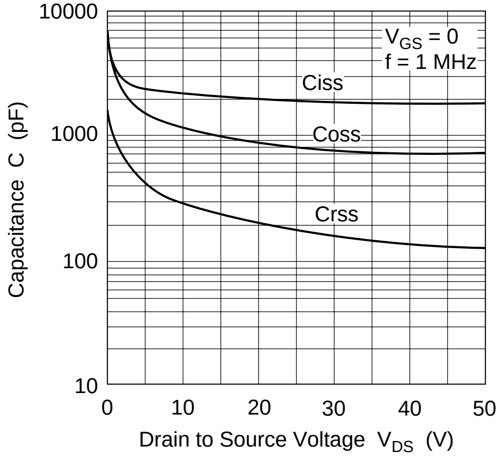

Static Drain to Source on State
Resistance vs. Temperature
I_D = 20 A
5 A,10 A
V_{GS} = 4 V
20 A
5 A,10 A
V_{GS} = 10 V
Pulse Test
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
0.05
0.04
0.03
0.02
0.01
0
–40
0
40
80
120
160
Case Temperature T_C (°C)


Forward Transfer Admittance
vs. Drain Current
–25°C
T_C = 25°C
75°C
V_{DS} = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1.0
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)

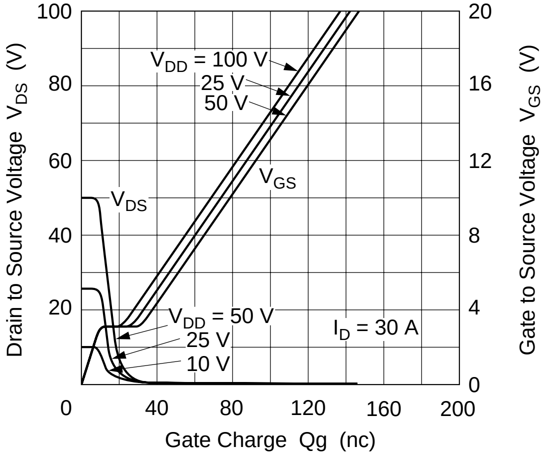
Body to Drain Diode Reverse Recovery Time



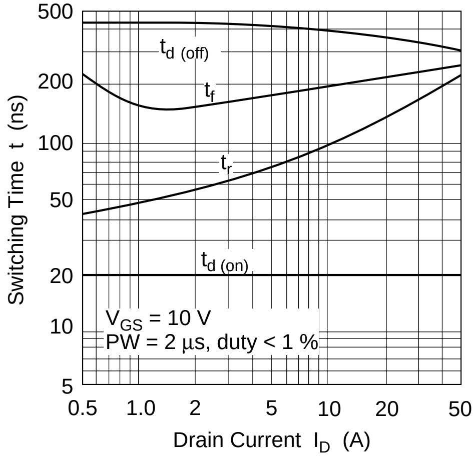
Typical Capacitance vs. Drain to Source Voltage

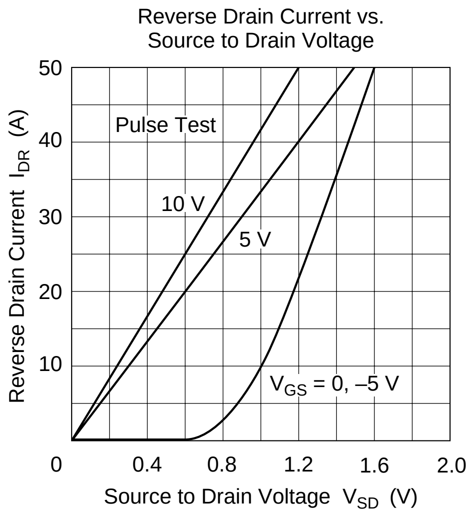


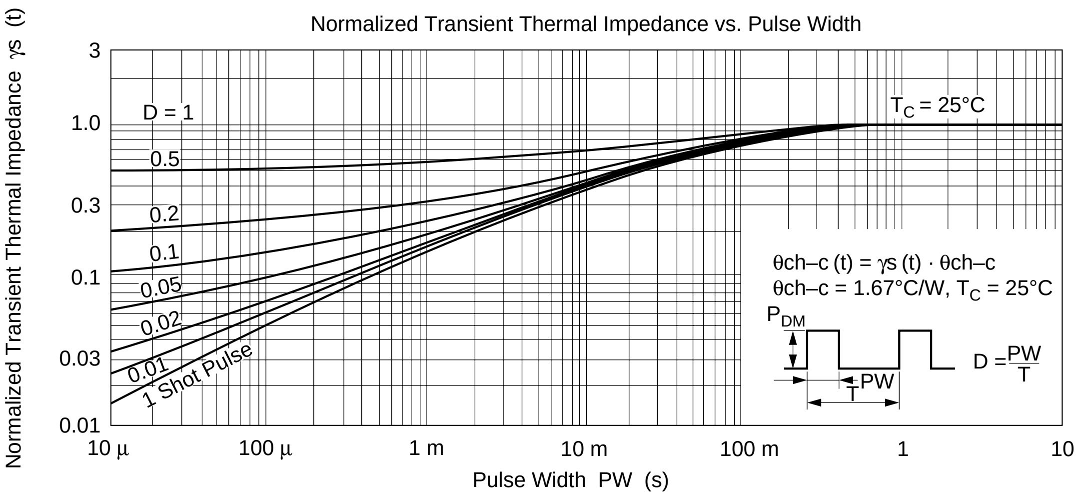
Dynamic Input Characteristics



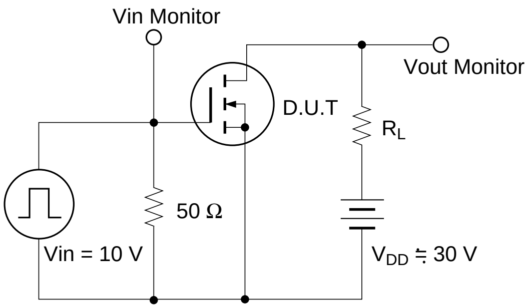
Switching Characteristics



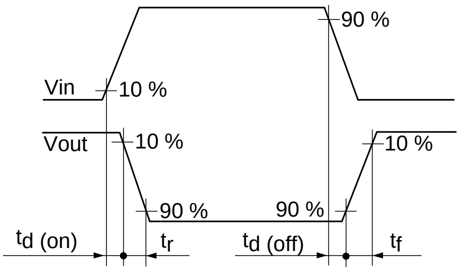

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
V_{GS} = 0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (s)
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γs (t) · θch–c
θch–c = 1.67°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1297

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

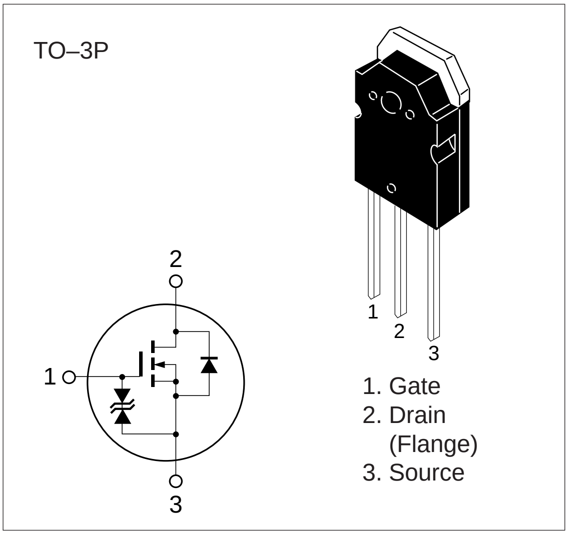


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*	160	A
Body to drain diode reverse drain current	I_{DR}	40	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

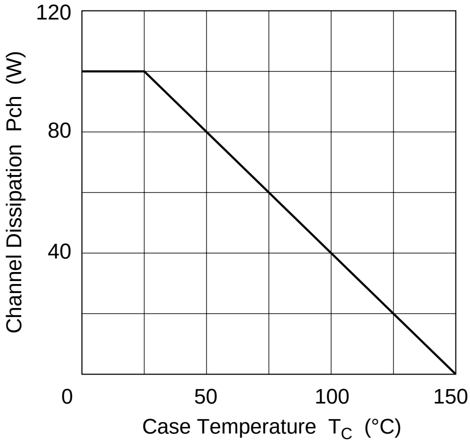
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

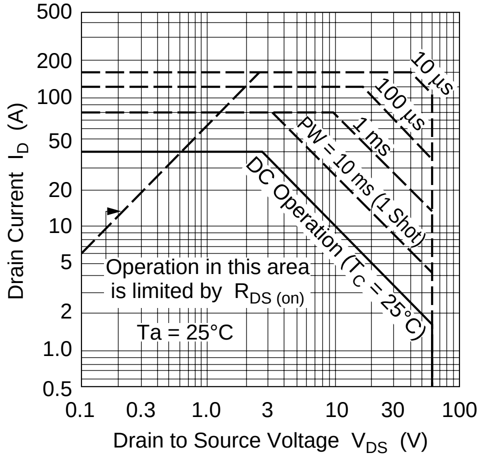
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.015	0.018	Ω	I_D = 20 A, V_{GS} = 10 V *
		—	0.02	0.025		I_D = 20 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	22	35	—	S	I_D = 20 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	3600	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	1850	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	450	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 20 A, V_{GS} = 10 V,
Rise time	t_r	—	170	—	ns	R_L = 1.5 Ω
Turn-off delay time	$t_{d(off)}$	—	700	—	ns	
Fall time	t_f	—	350	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	155	—	ns	I_F = 40 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

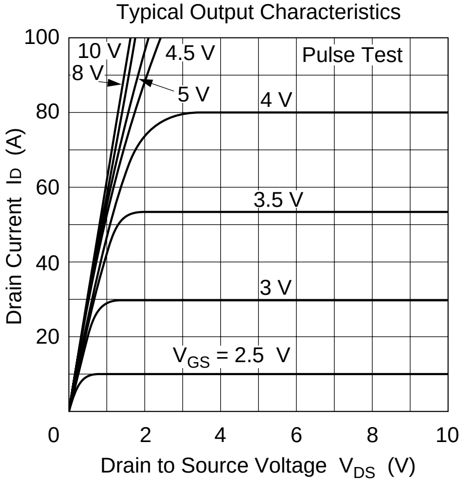
Power vs. Temperature Derating



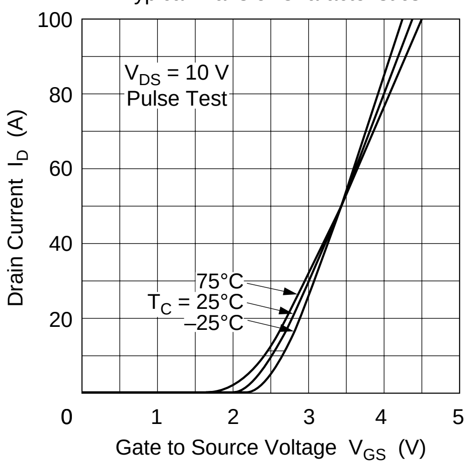
Maximum Safe Operation Area

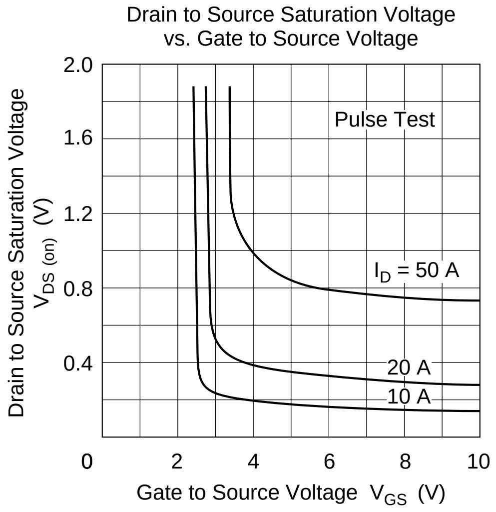


Typical Output Characteristics

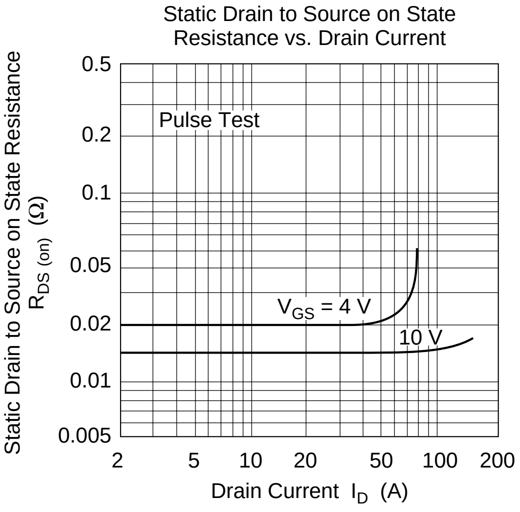


Typical Transfer Characteristics

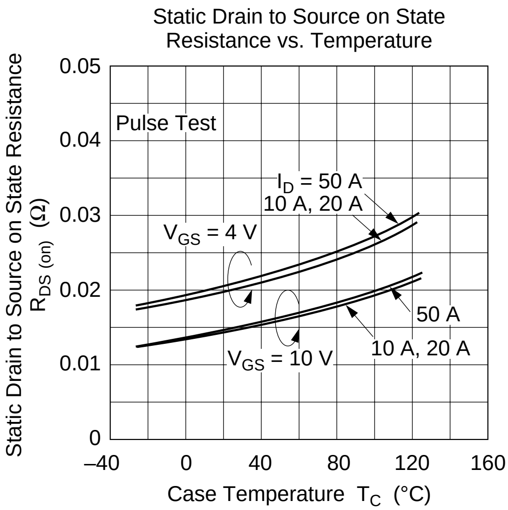




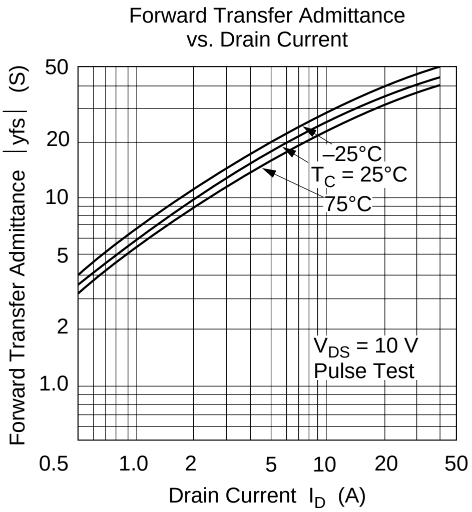
Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 50 A
20 A
10 A
Drain to Source Saturation Voltage
$V_{DS (on)}$ (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)



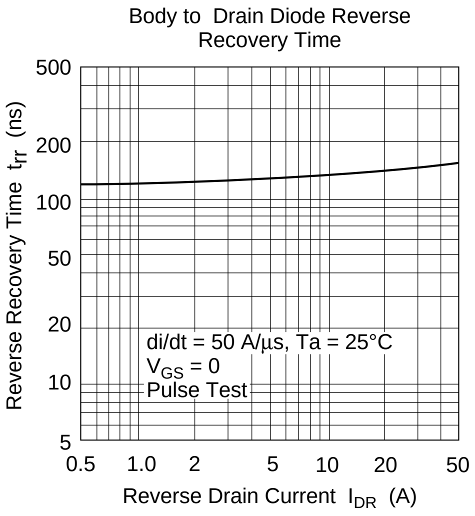
Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 4 V
10 V
Static Drain to Source on State Resistance
$R_{DS (on)}$ (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I_D (A)

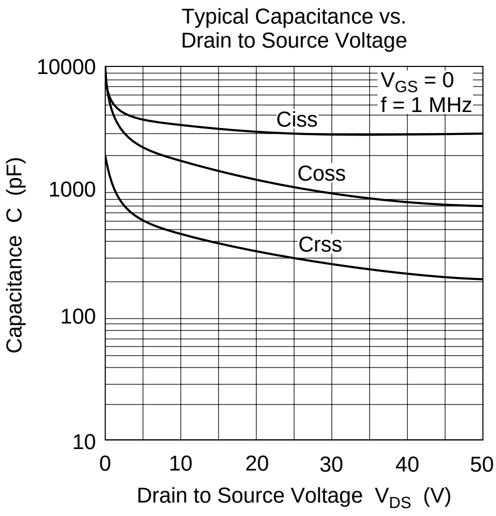


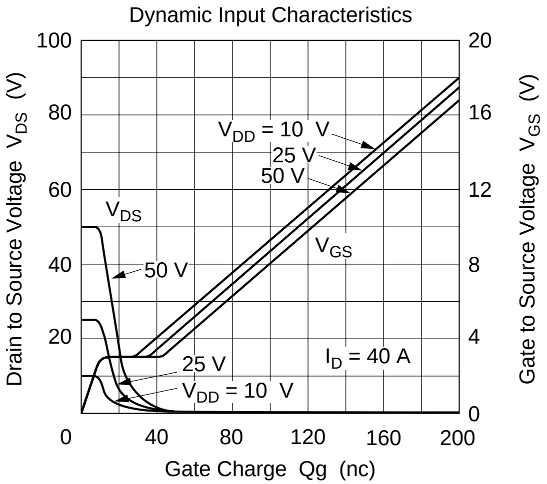
Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 50 A
10 A, 20 A
V_{GS} = 4 V
50 A
10 A, 20 A
V_{GS} = 10 V
Static Drain to Source on State Resistance
$R_{DS (on)}$ (Ω)
0.05
0.04
0.03
0.02
0.01
0
–40
0
40
80
120
160
Case Temperature T_C (°C)

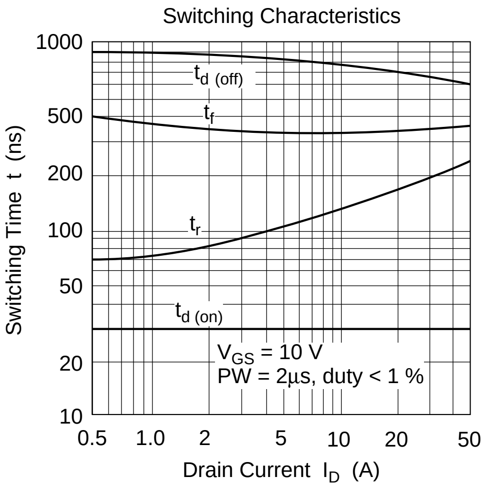


Forward Transfer Admittance
vs. Drain Current
–25°C
T_C = 25°C
75°C
V_{DS} = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1.0
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)

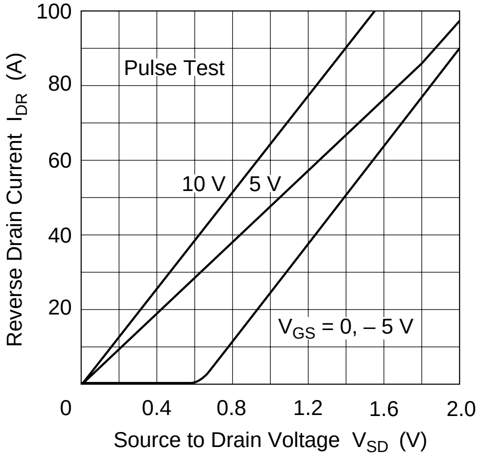

Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
500
200
100
50
20
10
5
0.5
1.0
2
5
10
20
50
Reverse Drain Current I_{DR} (A)
di/dt = 50 A/μs, Ta = 25°C
V_{GS} = 0
Pulse Test


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)
V_{GS} = 0
f = 1 MHz
Ciss
Coss
Crss

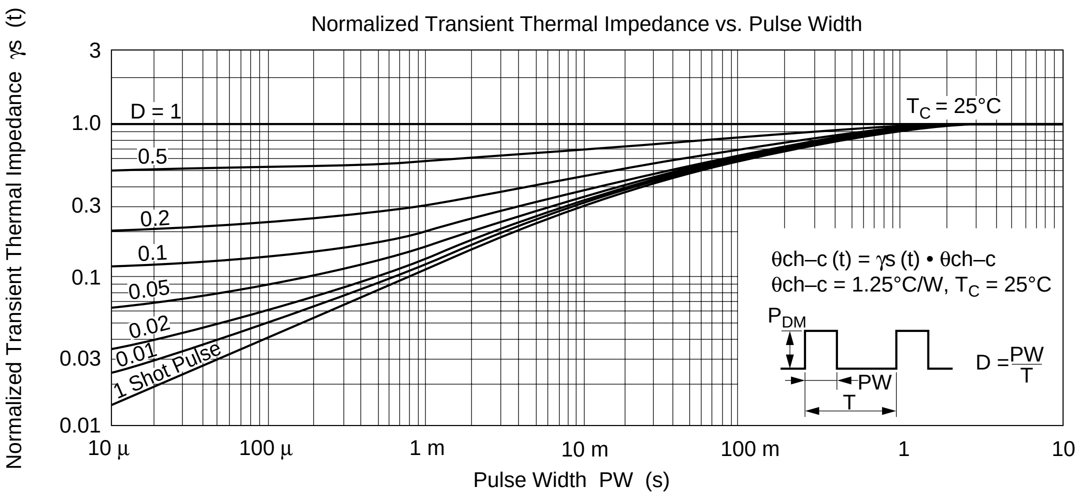

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
100
80
60
40
20
0
40
80
120
160
200
Gate Charge Qg (nc)
Gate to Source Voltage V_{GS} (V)
20
16
12
8
4
0
V_{DD} = 10 V
25 V
50 V
V_{DS}
V_{GS}
50 V
25 V
V_{DD} = 10 V
I_D = 40 A


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)
$t_{d\ (off)}$
t_f
t_r
$t_{d\ (on)}$
V_{GS} = 10 V
PW = 2μs, duty < 1 %

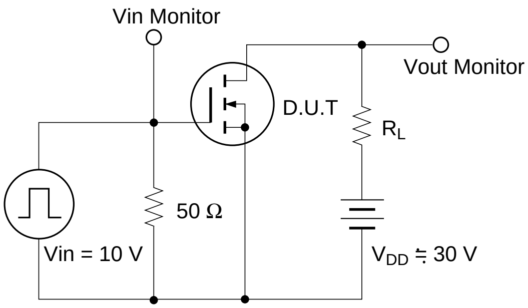
Reverse Drain Current vs.
Source to Drain Voltage



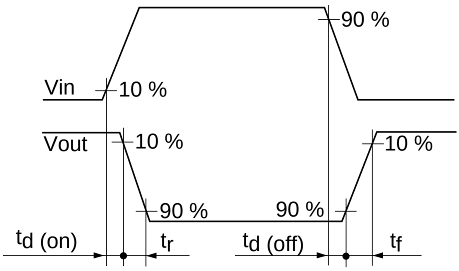
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Wavewforms



2SK1298

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

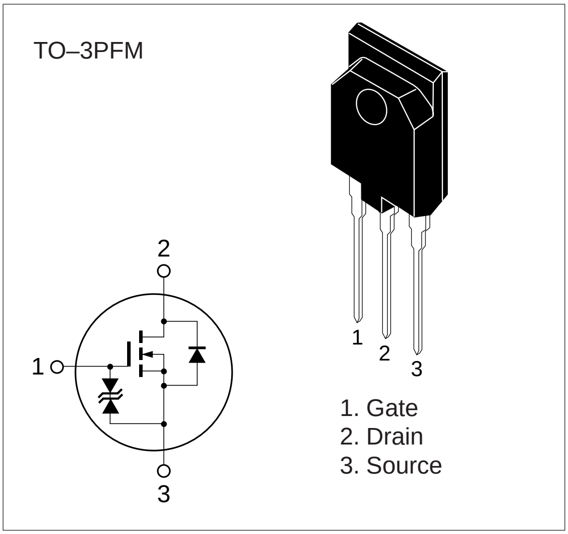


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*	160	A
Body to drain diode reverse drain current	I_{DR}	40	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %

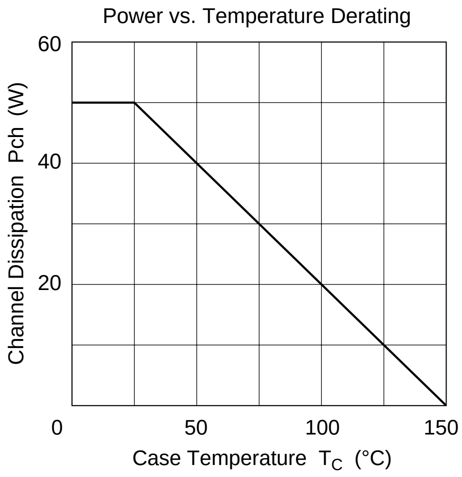
** Value at T_C = 25 °C

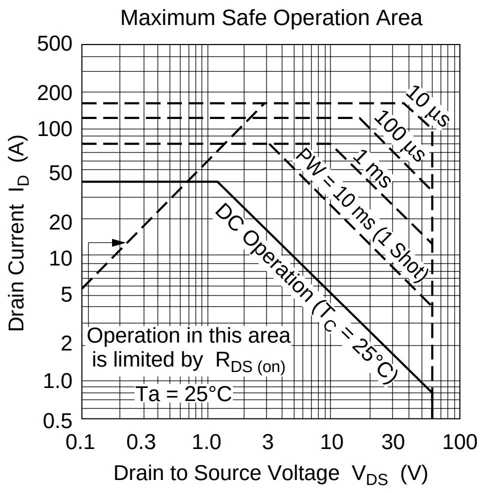
Table 2 Electrical Characteristics (Ta = 25°C)

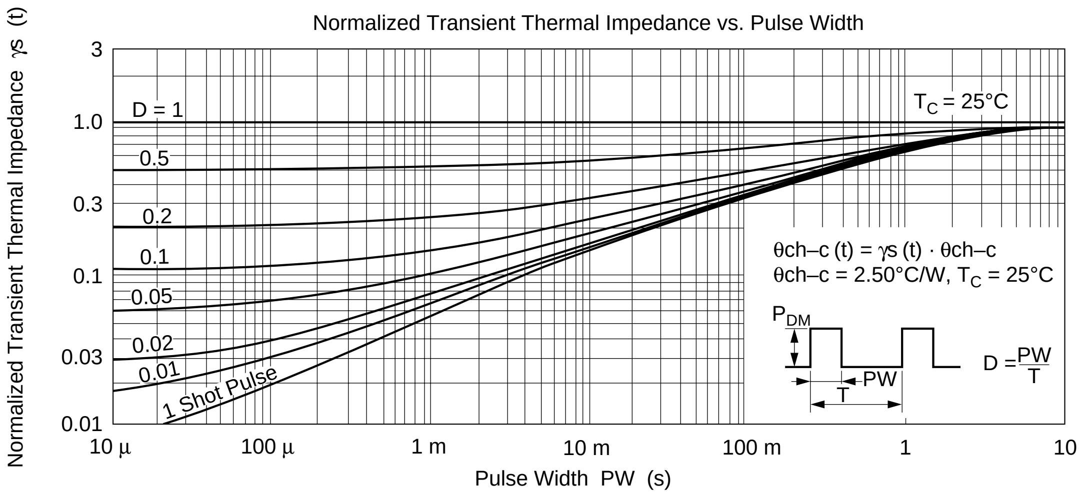
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.015	0.018	Ω	I_D = 20 A, V_{GS} = 10 V *
		—	0.02	0.025		I_D = 20 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	22	35	—	S	I_D = 20 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	3600	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	1850	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	450	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 20 A, V_{GS} = 10 V,
Rise time	t_r	—	170	—	ns	R_L = 1.5 Ω
Turn-off delay time	$t_{d(off)}$	—	700	—	ns	
Fall time	t_f	—	350	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	155	—	ns	I_F = 40 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK1297.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
500
200
100
50
20
10
5
2
1.0
0.5
0.1
0.3
1.0
3
10
30
100
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this area is limited by $R_{DS\ (on)}$
Ta = 25°C


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1.0
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
θch–c (t) = γs (t) · θch–c
θch–c = 2.50°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$

2SK1299 (L), 2SK1299 (S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

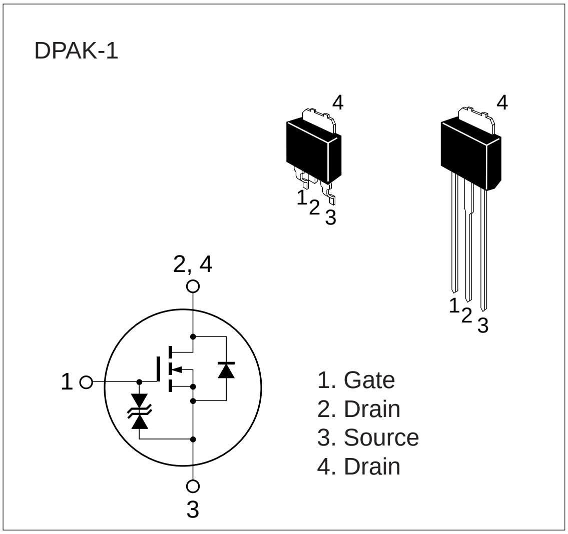


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$*	12	A
Body to drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

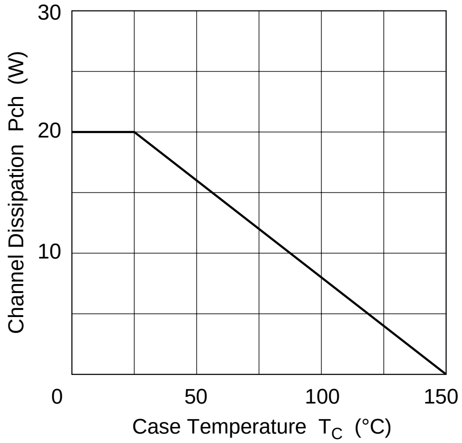
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

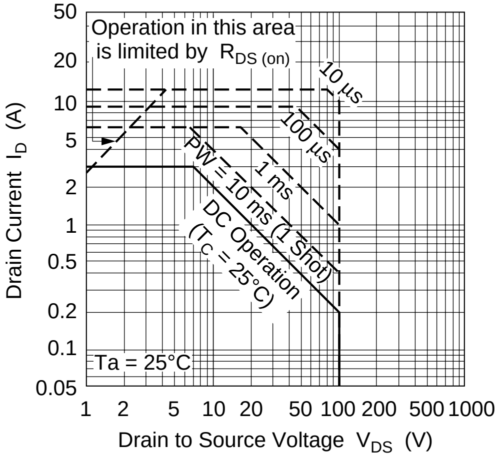
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.35	Ω	I_D = 2 A, V_{GS} = 10 V *
		—	0.30	0.45		I_D = 2 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	2.4	4.0	—	S	I_D = 2 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	165	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	45	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 2 A, V_{GS} = 10 V,
Rise time	t_r	—	35	—	ns	R_L = 15 Ω
Turn-off delay time	$t_{d(off)}$	—	160	—	ns	
Fall time	t_f	—	60	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 3 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 3 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

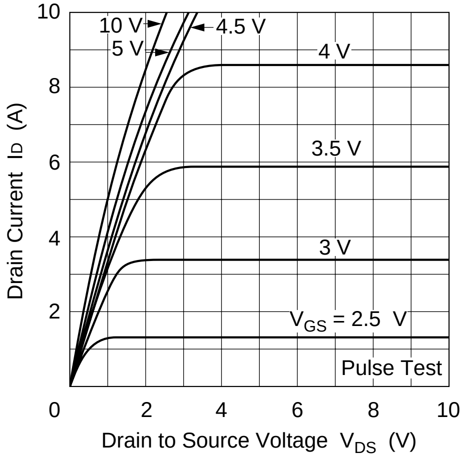
Power vs. Temperature Derating



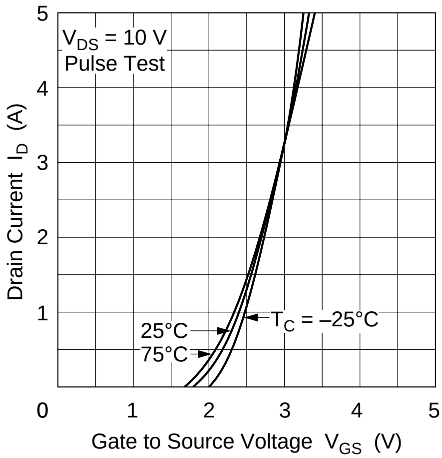
Maximum Safe Operation Area



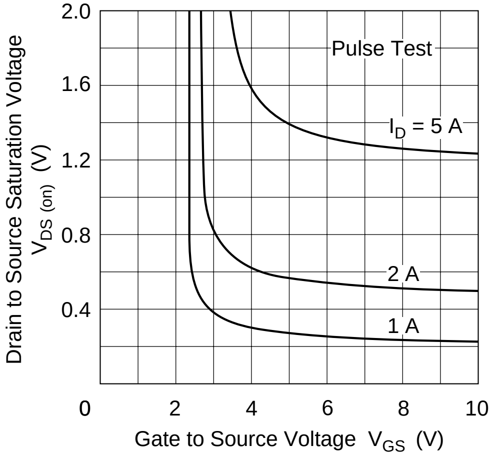
Typical Output Characteristics



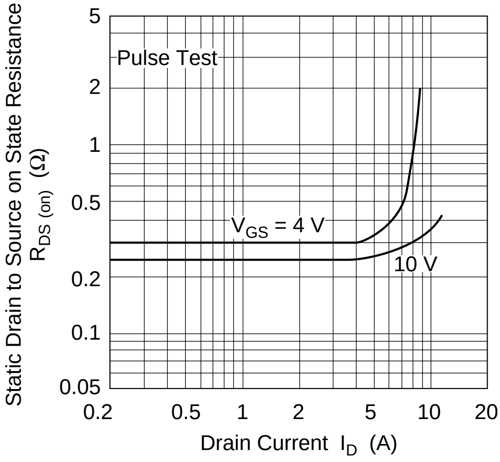
Typical Transfer Characteristics



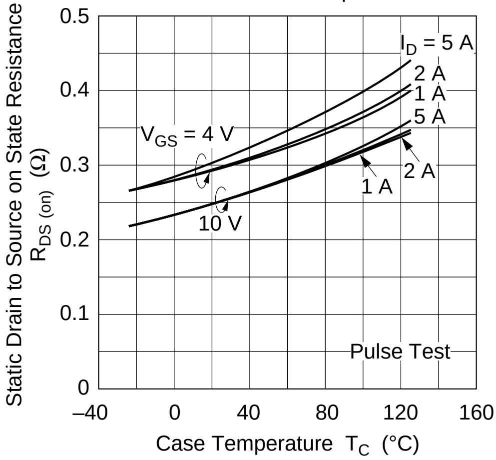
Drain to Source Saturation Voltage vs. Gate to Source Voltage



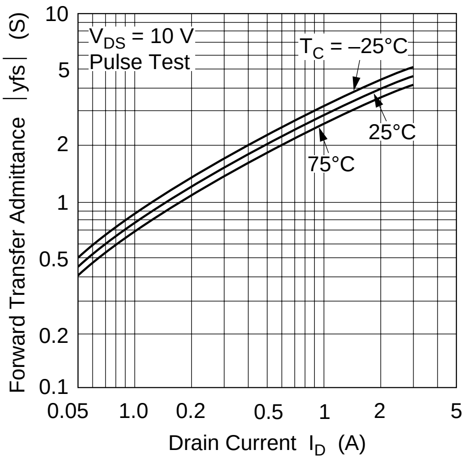
Static Drain to Source on State Resistance vs. Drain Current

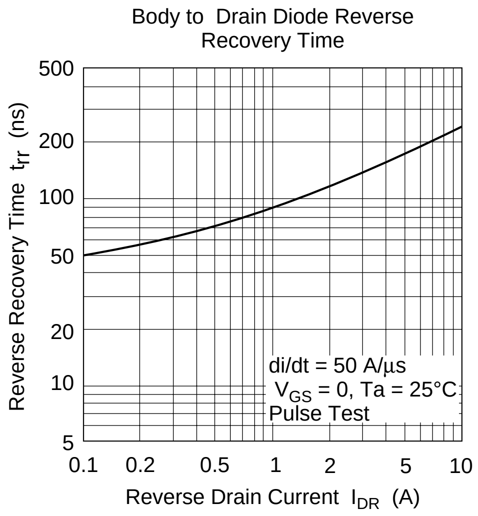


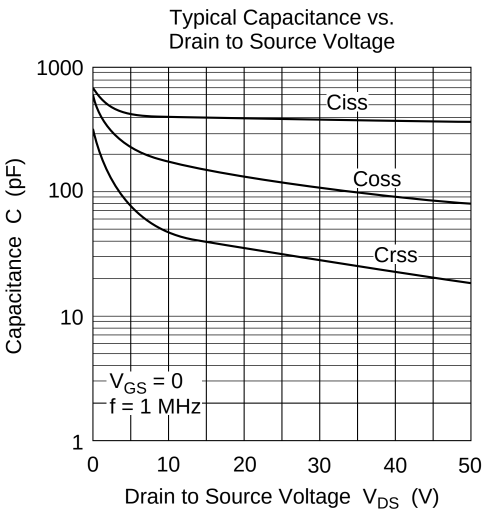
Static Drain to Source on State Resistance vs. Temperature

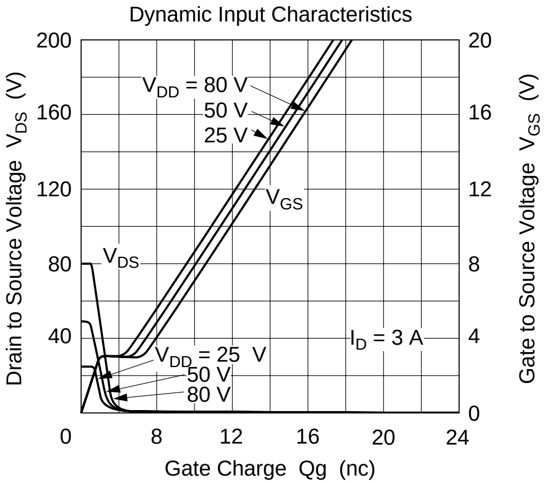


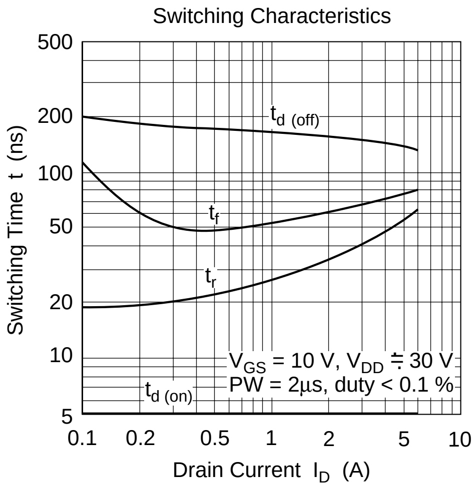
Forward Transfer Admittance vs. Drain Current

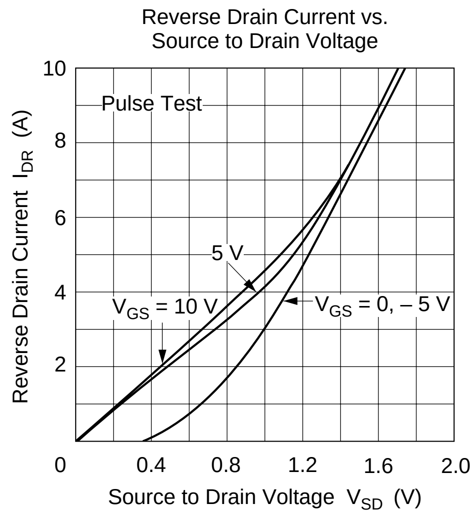



Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1
2
5
10
di/dt = 50 A/µs
V_{GS} = 0, Ta = 25°C
Pulse Test
Reverse Drain Current I_{DR} (A)

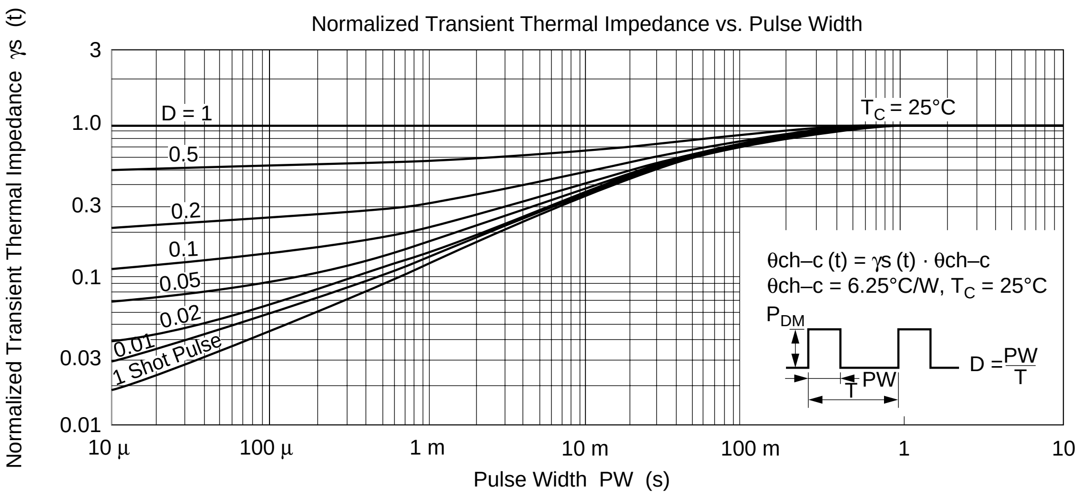

Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
1000
100
10
1
Ciss
Coss
Crss
V_{GS} = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)


Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
200
160
120
80
40
0
Gate to Source Voltage V_{GS} (V)
20
16
12
8
4
0
V_{DD} = 80 V
50 V
25 V
V_{GS}
V_{DS}
V_{DD} = 25 V
50 V
80 V
I_D = 3 A
8
12
16
20
24
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
$t_{d\ (off)}$
t_f
t_r
$t_{d\ (on)}$
V_{GS} = 10 V, V_{DD} ≒ 30 V
PW = 2µs, duty < 0.1 %
0.1
0.2
0.5
1
2
5
10
Drain Current I_D (A)

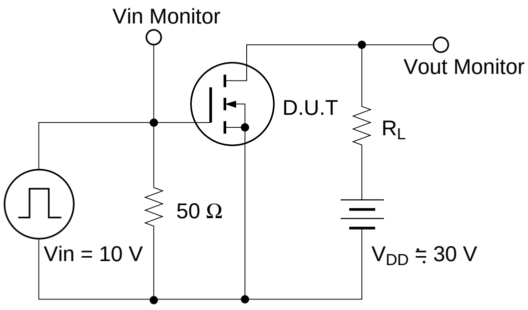


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5 V
V_{GS} = 10 V
V_{GS} = 0, – 5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
2
4
6
8
10
0.4
0.8
1.2
1.6
2.0

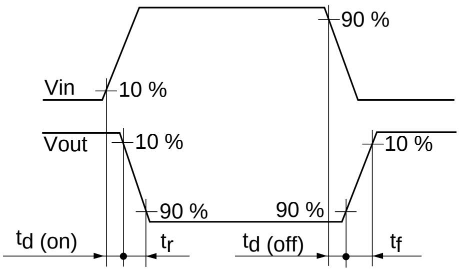


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (s)
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γs (t) · θch–c
θch–c = 6.25°C/W, T_C = 25°C
P_{DM}
PW
T
D = PW/T
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1300

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

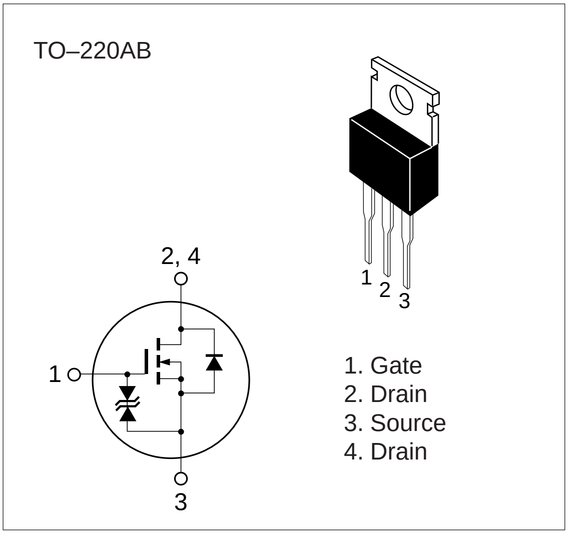


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	40	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

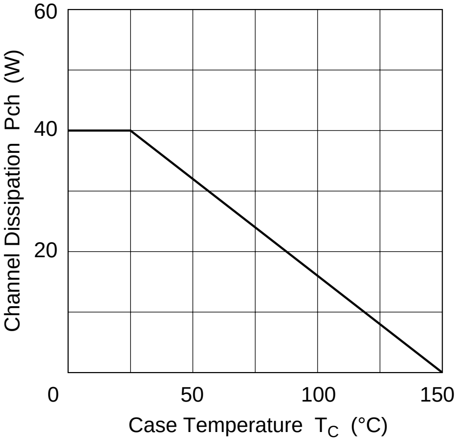
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

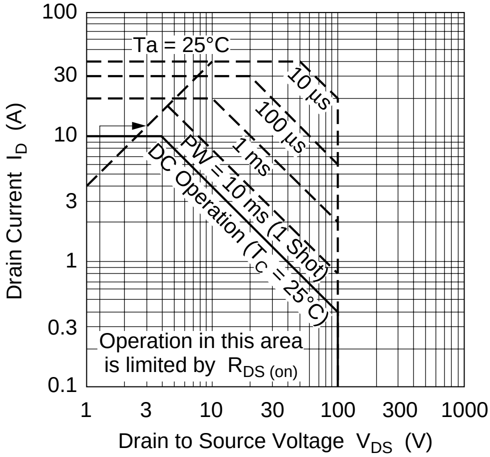
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.20	0.25	Ω	I_D = 5 A, V_{GS} = 10 V *
		—	0.25	0.35		I_D = 5 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	4.5	7.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	525	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	205	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	60	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time	t_r	—	50	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	170	—	ns	
Fall time	t_f	—	75	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

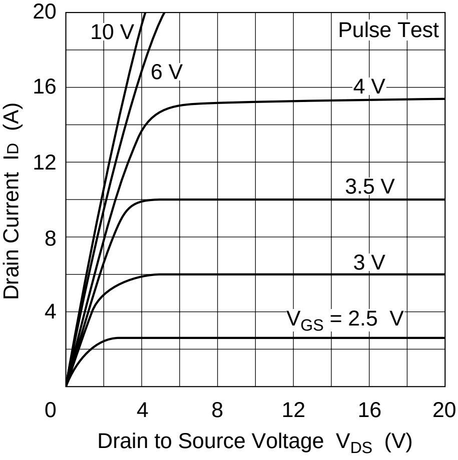
Power vs. Temperature Derating



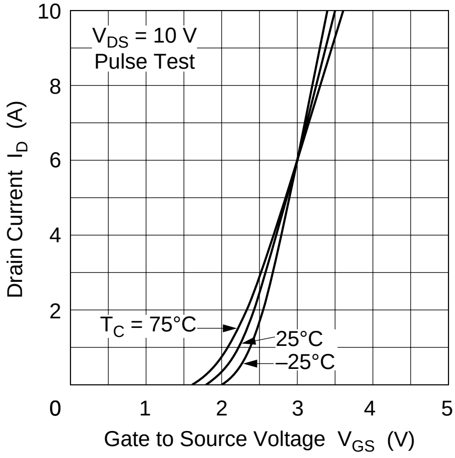
Maximum Safe Operation Area

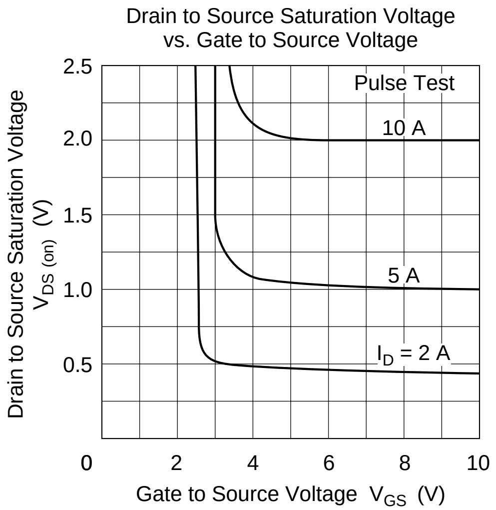


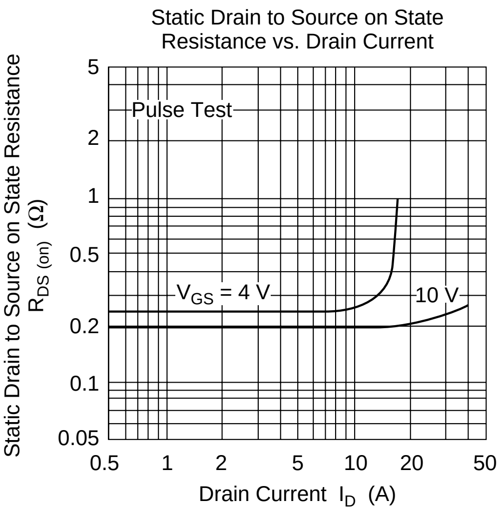
Typical Output Characteristics

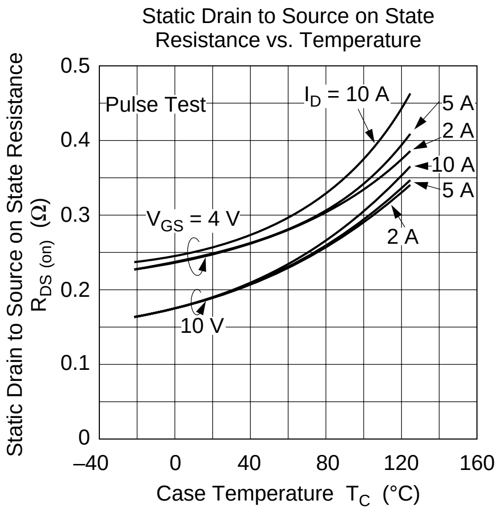


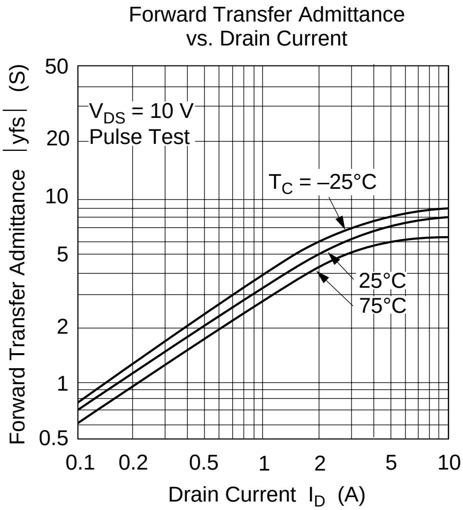
Typical Transfer Characteristics

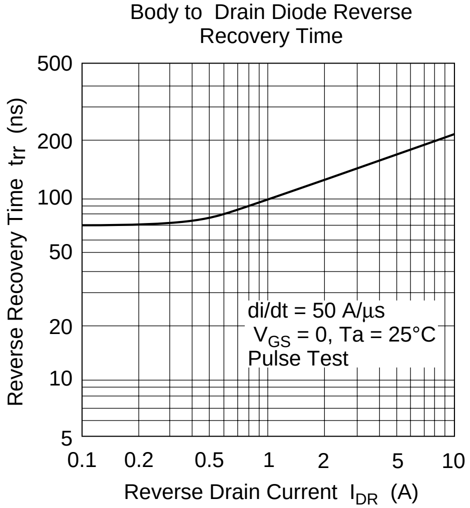


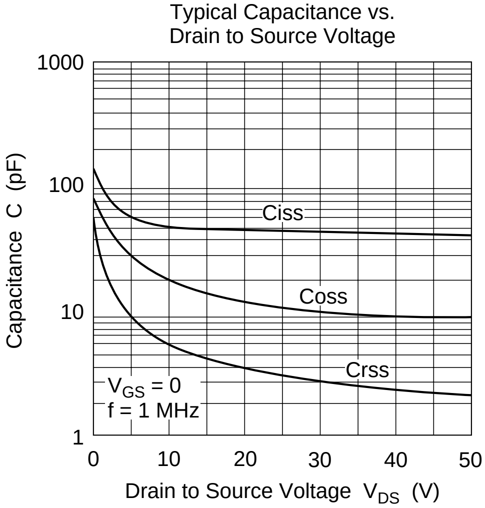

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
10 A
5 A
I_D = 2 A
Drain to Source Saturation Voltage
V_DS (on) (V)
2.5
2.0
1.5
1.0
0.5
0
2
4
6
8
10
Gate to Source Voltage V_GS (V)

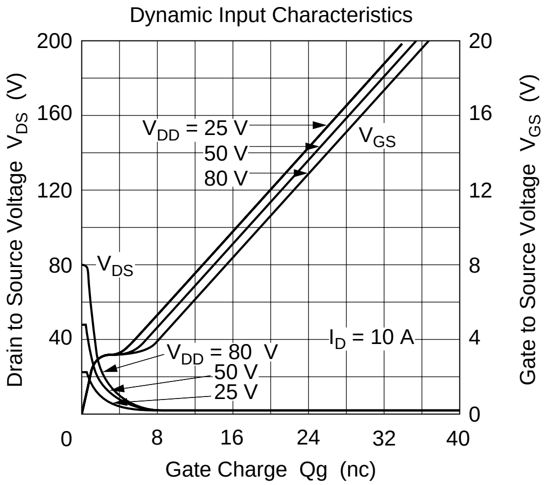

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_GS = 4 V
10 V
Static Drain to Source on State Resistance
R_DS (on) (Ω)
5
2
1
0.5
0.2
0.1
0.05
0.5
1
2
5
10
20
50
Drain Current I_D (A)

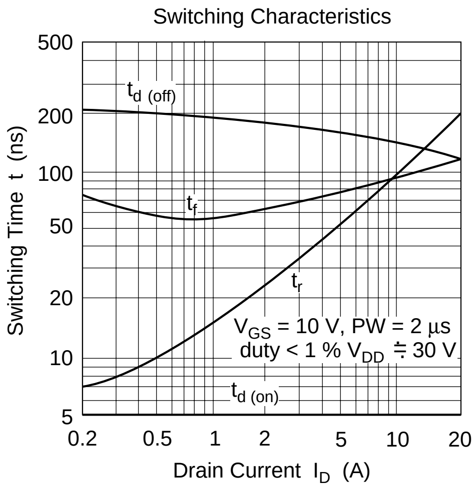

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 10 A
5 A
2 A
10 A
5 A
2 A
V_GS = 4 V
10 V
Static Drain to Source on State Resistance
R_DS (on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature T_C (°C)

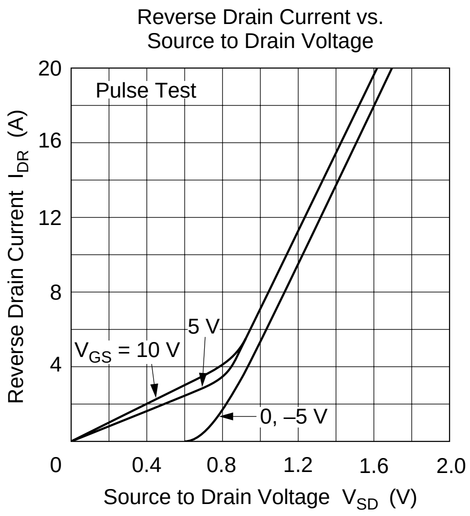

Forward Transfer Admittance
vs. Drain Current
V_DS = 10 V
Pulse Test
T_C = –25°C
25°C
75°C
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Drain Current I_D (A)

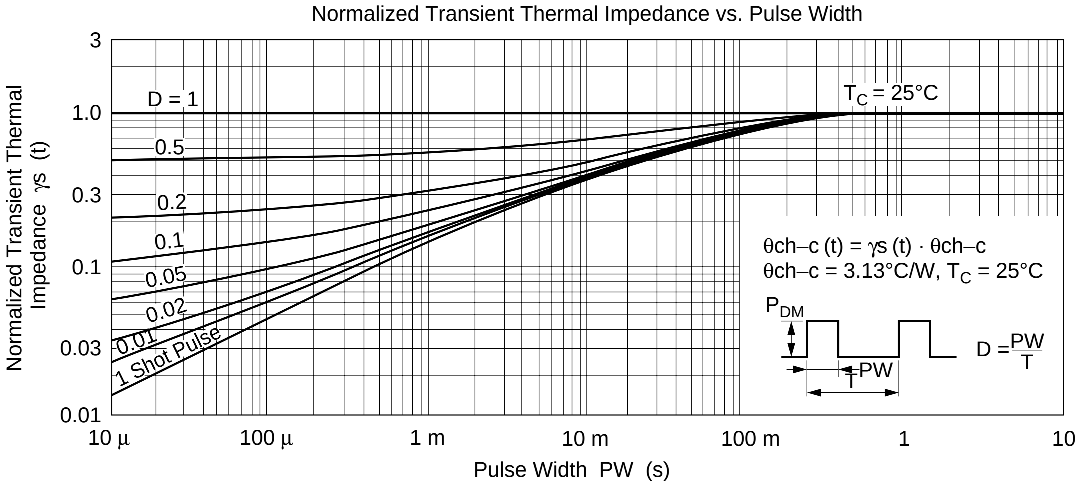

Body to Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current IDR (A)
di/dt = 50 A/μs
VGS = 0, Ta = 25°C
Pulse Test

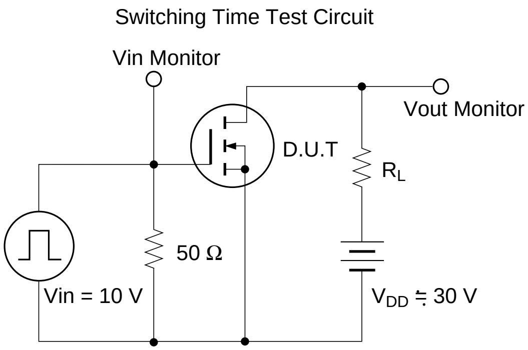

Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
1000
100
10
1
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

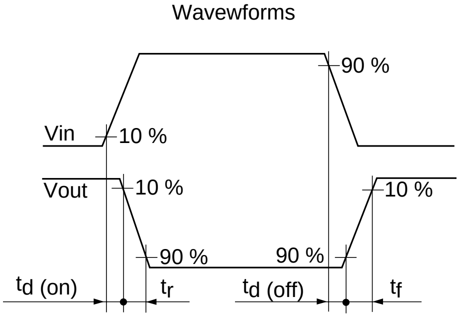

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
200
160
120
80
40
0
8
16
24
32
40
20
16
12
8
4
0
Gate Charge Qg (nc)
VDD = 25 V
50 V
80 V
VGS
VDS
VDD = 80 V
50 V
25 V
ID = 10 A


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20
Drain Current ID (A)
td (off)
tf
tr
td (on)
VGS = 10 V, PW = 2 μs
duty < 1 % VDD ≒ 30 V


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
5 V
0, –5 V
20
16
12
8
4
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)
Reverse Drain Current I_{DR} (A)


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
θch–c (t) = γs (t) · θch–c
θch–c = 3.13°C/W, T_C = 25°C
P_{DM}
PW
T
D = PW/T
3
1.0
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)
Normalized Transient Thermal Impedance γs (t)


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T
RL
50 Ω
Vin = 10 V
VDD ≒ 30 V


Wavewforms
90 %
Vin
10 %
Vout
10 %
10 %
90 %
90 %
td (on)
tr
td (off)
tf

2SK1301

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

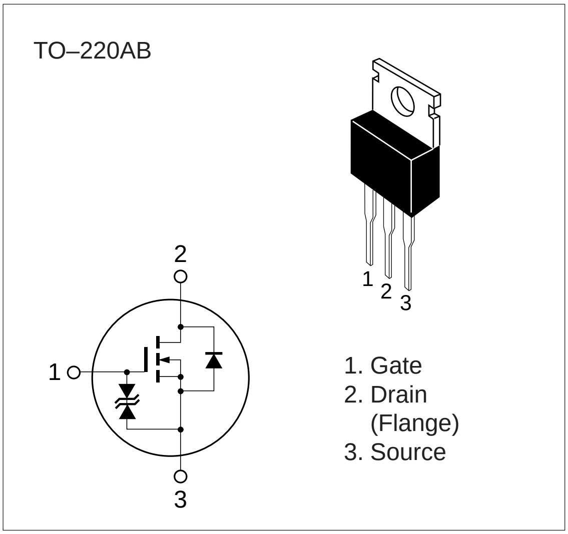


Table 1 Absolute Maximum Ratings (Ta = 25°C)

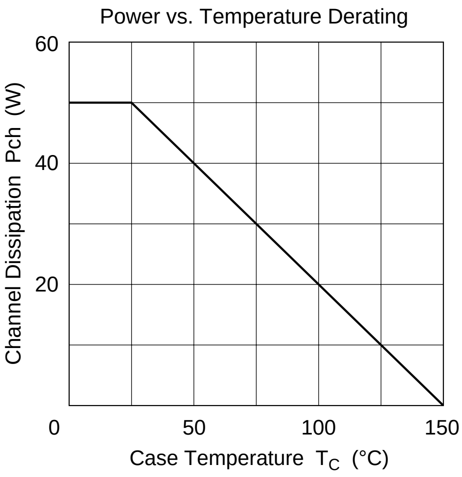
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body to drain diode reverse drain current	I_{DR}	15	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

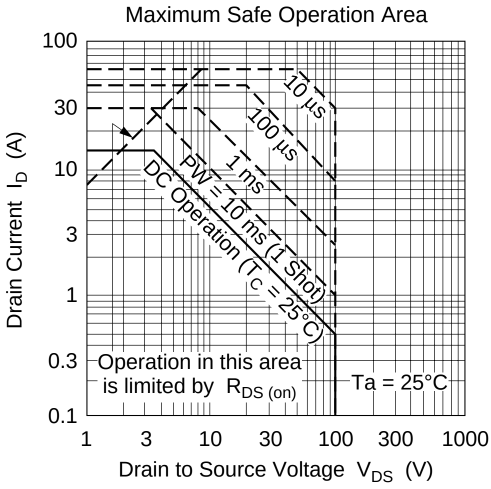
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

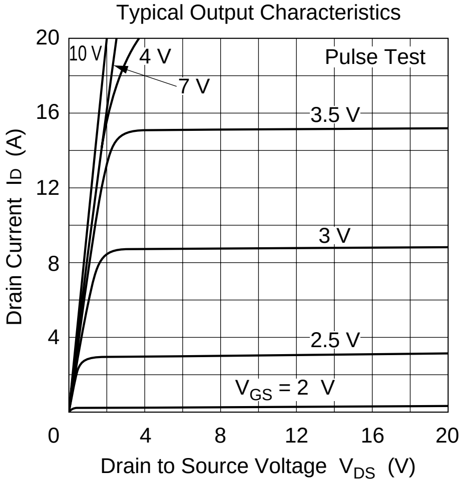
Table 2 Electrical Characteristics (Ta = 25°C)

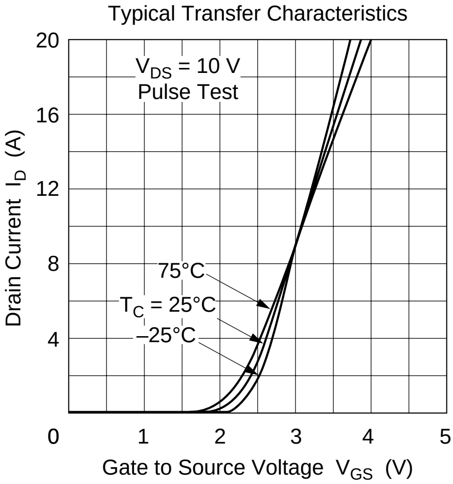
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.10	0.13	Ω	I_D = 8 A, V_{GS} = 10 V *
		—	0.13	0.18		I_D = 8 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	7	11	—	S	I_D = 8 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	340	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	100	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 8 A, V_{GS} = 10 V,
Rise time	t_r	—	70	—	ns	R_L = 3.75 Ω
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	
Fall time	t_f	—	100	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 15 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	250	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 50 A/µs

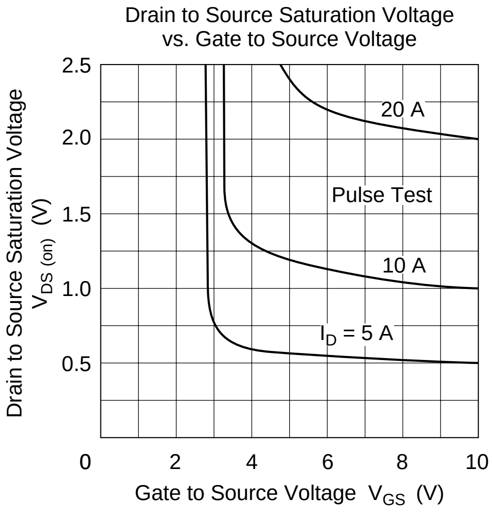
* Pulse Test

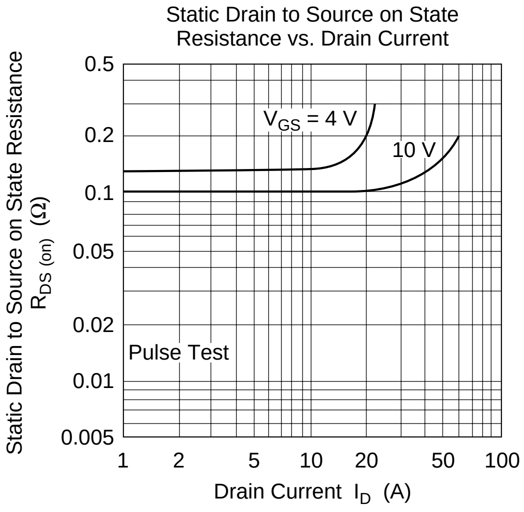

Power vs. Temperature Derating
Channel Dissipation Pch (W)
Case Temperature T_C (°C)
0
20
40
60
50
100
150

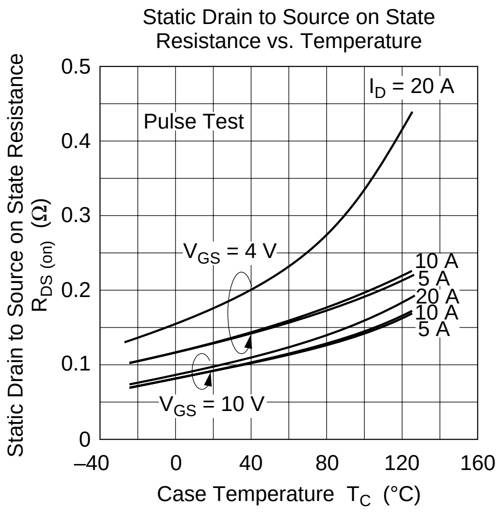

Maximum Safe Operation Area
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this area is limited by $R_{DS (on)}$
Ta = 25°C
100
30
10
3
1
0.3
0.1
1
3
10
30
100
300
1000

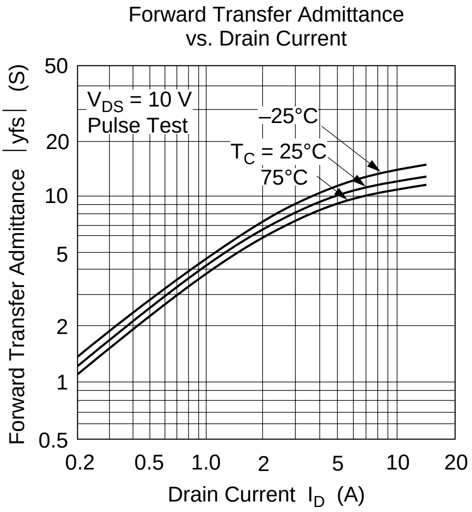

Typical Output Characteristics
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10 V
4 V
7 V
Pulse Test
3.5 V
3 V
2.5 V
V_{GS} = 2 V
0
4
8
12
16
20

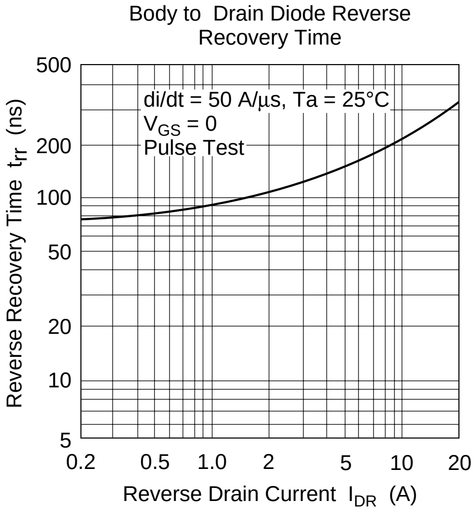

Typical Transfer Characteristics
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
75°C
T_C = 25°C
–25°C
0
4
8
12
16
20
1
2
3
4
5

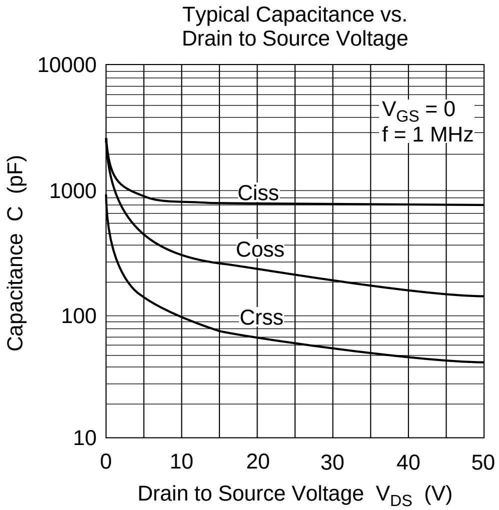

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
V DS (on) (V)
2.5
2.0
1.5
1.0
0.5
0
2
4
6
8
10
Gate to Source Voltage V GS (V)
20 A
Pulse Test
10 A
I D = 5 A

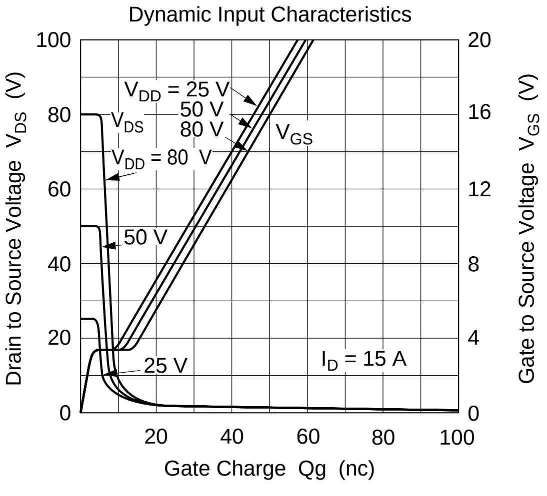

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
R DS (on) (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
1
2
5
10
20
50
100
Drain Current I D (A)
V GS = 4 V
10 V
Pulse Test

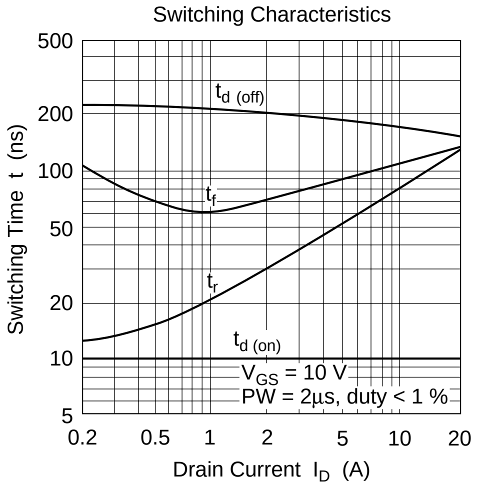

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
R DS (on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature T C (°C)
I D = 20 A
Pulse Test
V GS = 4 V
10 A
5 A
20 A
10 A
5 A
V GS = 10 V

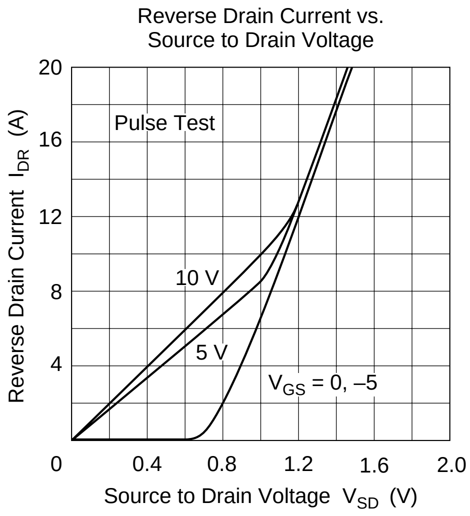

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
0.2
0.5
1.0
2
5
10
20
Drain Current I D (A)
V DS = 10 V
Pulse Test
–25°C
T C = 25°C
75°C


Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
Reverse Drain Current IDR (A)
500
200
100
50
20
10
5
0.2
0.5
1.0
2
5
10
20

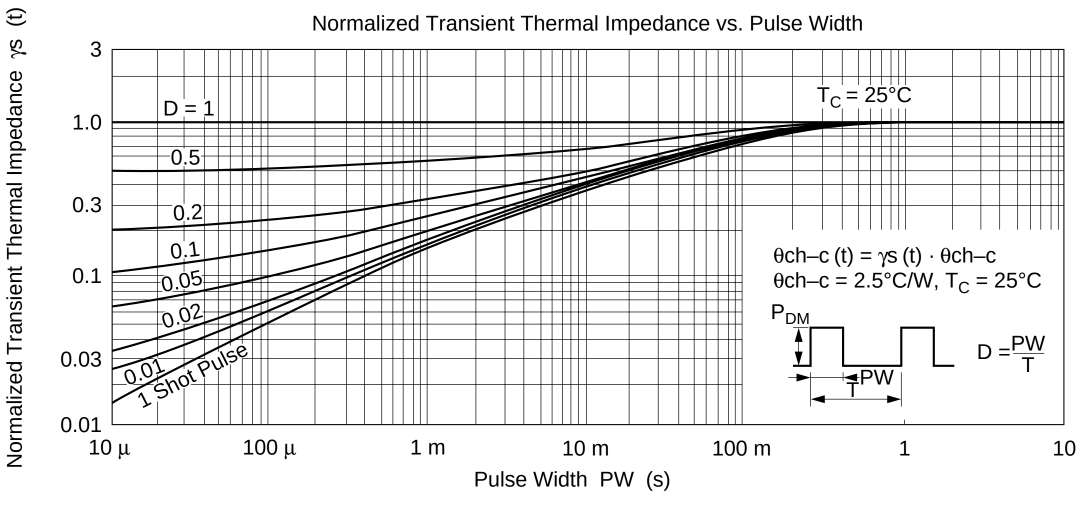

Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
Drain to Source Voltage VDS (V)
10000
1000
100
10
0
10
20
30
40
50


Dynamic Input Characteristics
VDD = 25 V
50 V
80 V
VDS
VDD = 80 V
VGS
50 V
25 V
ID = 15 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
100
80
60
40
20
0
20
16
12
8
4
0
20
40
60
80
100


Switching Characteristics
td (off)
tf
tr
td (on)
VGS = 10 V
PW = 2µs, duty < 1 %
Switching Time t (ns)
Drain Current ID (A)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20

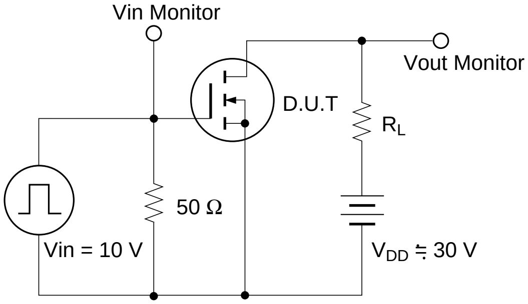


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
V_GS = 0, –5
Reverse Drain Current I_DR (A)
Source to Drain Voltage V_SD (V)
0
4
8
12
16
20
0.4
0.8
1.2
1.6
2.0

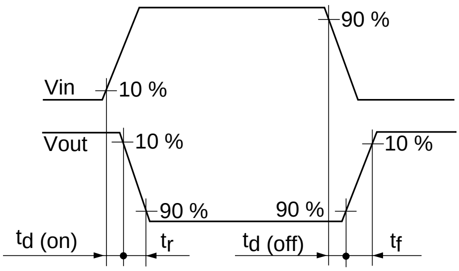


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γs (t) · θch–c
θch–c = 2.5°C/W, T_C = 25°C
P_DM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1302

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

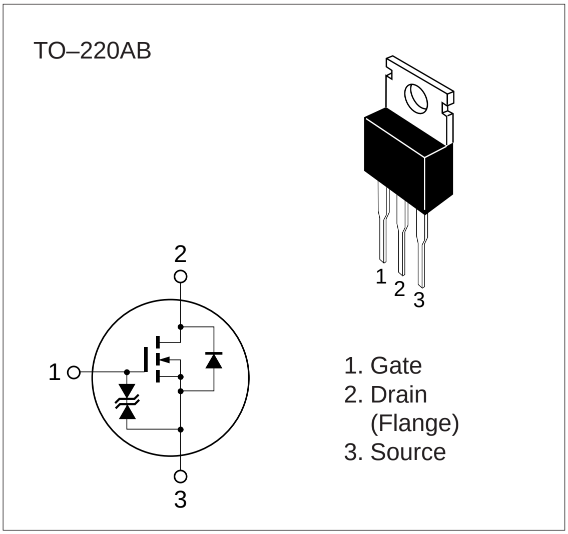


Table 1 Absolute Maximum Ratings (Ta = 25°C)

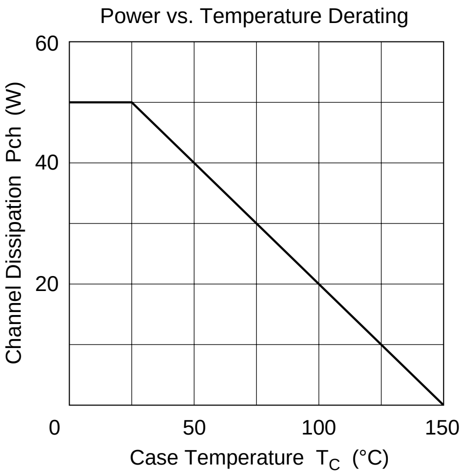
Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{(BR)DSS}$	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body to drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

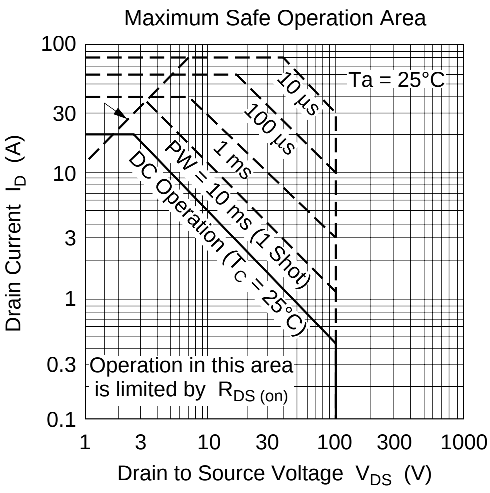
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

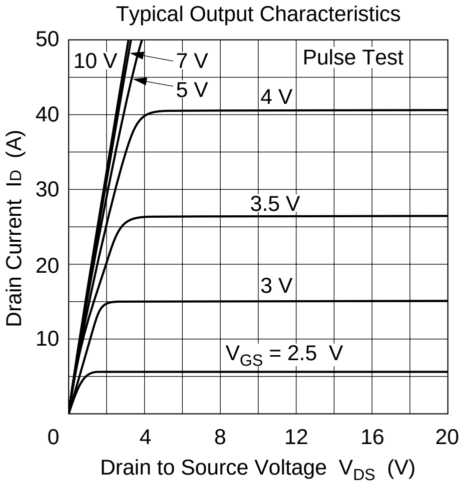
Table 2 Electrical Characteristics (Ta = 25°C)

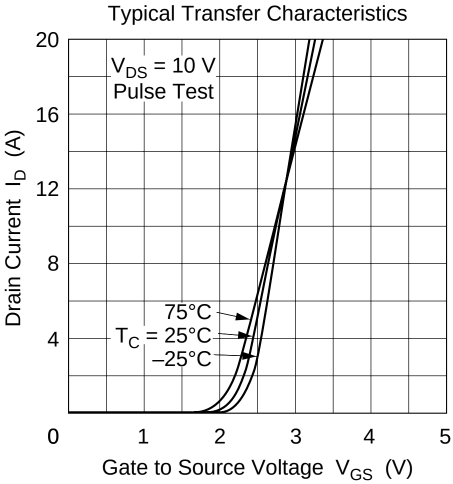
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.065	0.085	Ω	I_D = 10 A, V_{GS} = 10 V *
		—	0.085	0.12		I_D = 10 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	16	—	S	I_D = 10 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1300	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	540	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	160	—	pF	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	I_D = 10 A, V_{GS} = 10 V,
Rise time	t_r	—	100	—	ns	R_L = 3 Ω
Turn-off delay time	$t_{d(off)}$	—	300	—	ns	
Fall time	t_f	—	150	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 20 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	300	—	ns	I_F = 20 A, V_{GS} = 0, di_F/dt = 50 A/µs

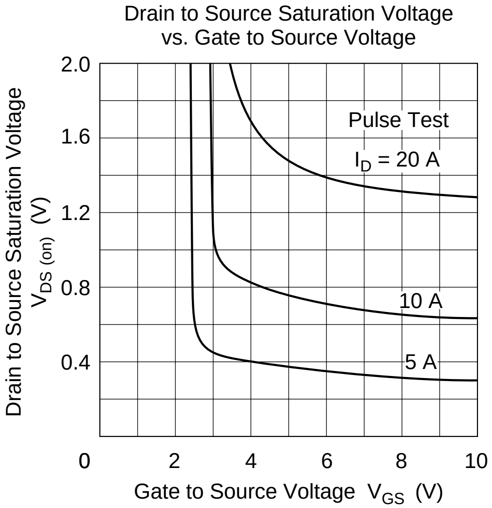
* Pulse Test

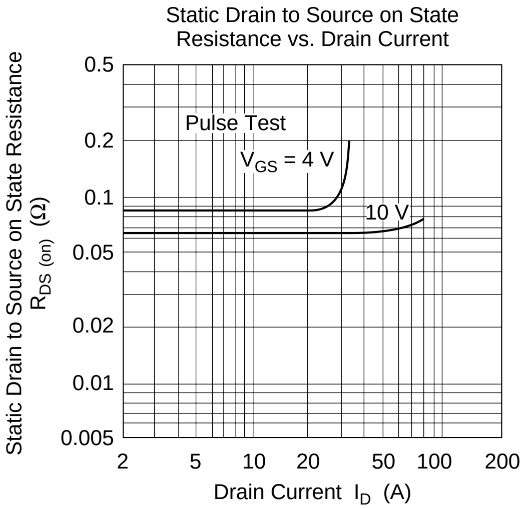

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

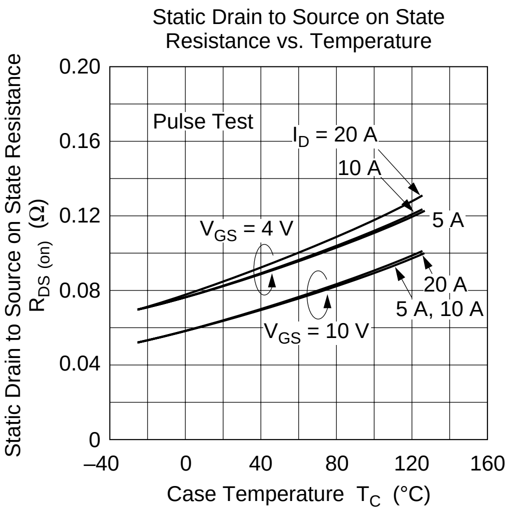

Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1
0.3
0.1
1
3
10
30
100
300
1000
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C
Operation in this area
is limited by $R_{DS (on)}$

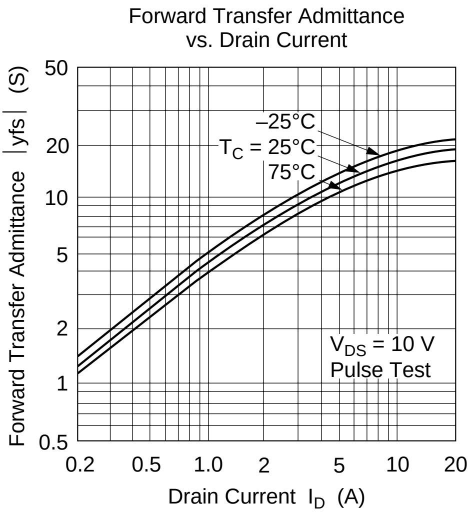

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)
10 V
7 V
5 V
Pulse Test
4 V
3.5 V
3 V
V_{GS} = 2.5 V

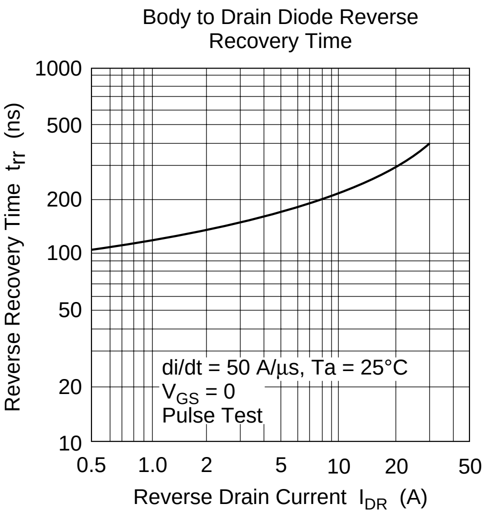

Typical Transfer Characteristics
Drain Current I_D (A)
20
16
12
8
4
0
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
75°C
T_C = 25°C
–25°C

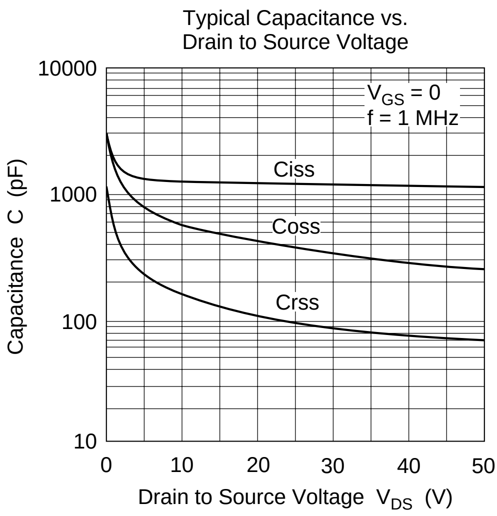

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 20 A
10 A
5 A
Drain to Source Saturation Voltage
$V_{DS\ (on)}$ (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

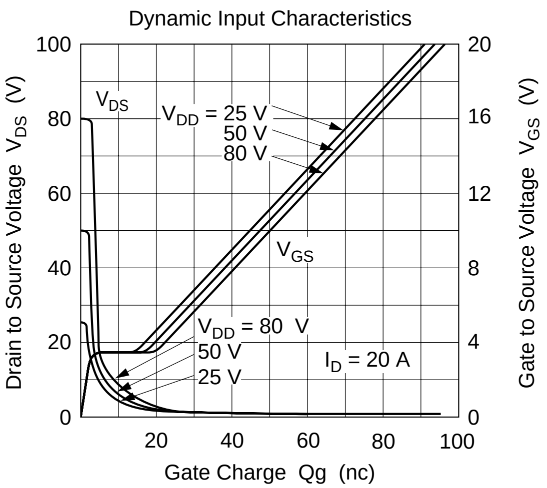

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 4 V
10 V
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I_D (A)

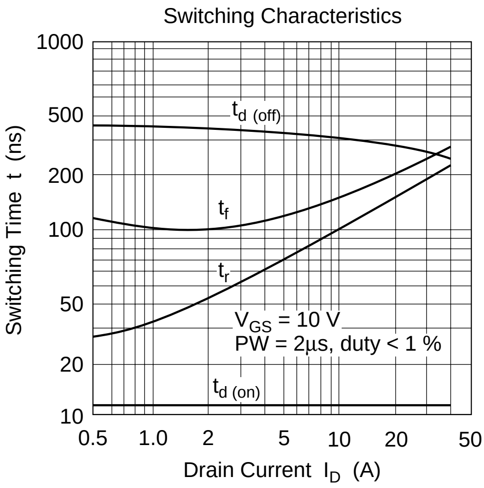

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 20 A
10 A
5 A
V_{GS} = 4 V
20 A
5 A, 10 A
V_{GS} = 10 V
Static Drain to Source on State Resistance
$R_{DS\ (on)}$ (Ω)
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature T_C (°C)

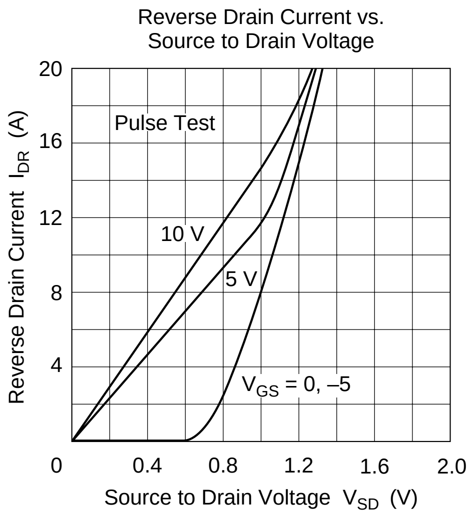

Forward Transfer Admittance
vs. Drain Current
–25°C
T_C = 25°C
75°C
V_{DS} = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
0.2
0.5
1.0
2
5
10
20
Drain Current I_D (A)


Body to Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
di/dt = 50 A/µs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Drain Current IDR (A)

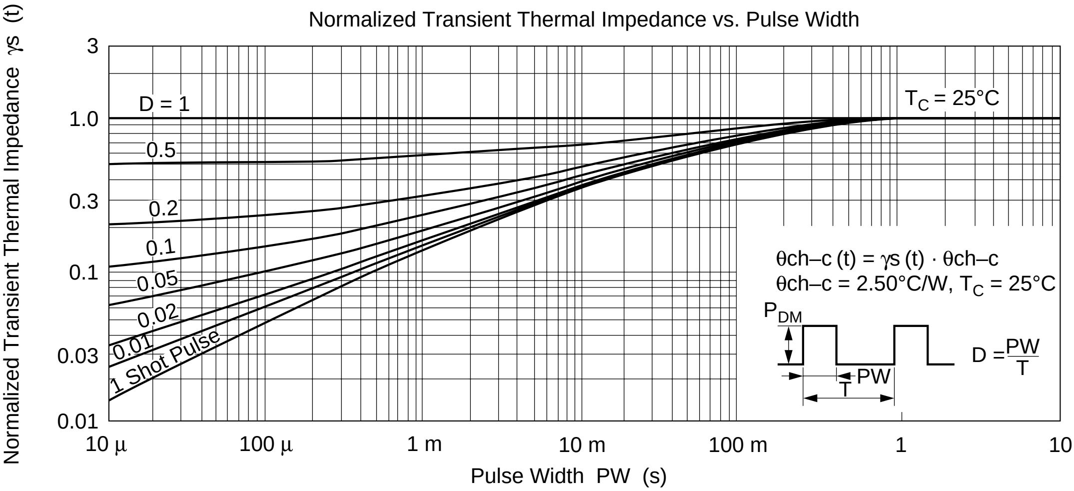

Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
20
40
60
80
100
VDS
VDD = 25 V
50 V
80 V
VGS
VDD = 80 V
50 V
25 V
ID = 20 A
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
td (off)
tf
tr
VGS = 10 V
PW = 2µs, duty < 1 %
td (on)
Drain Current ID (A)

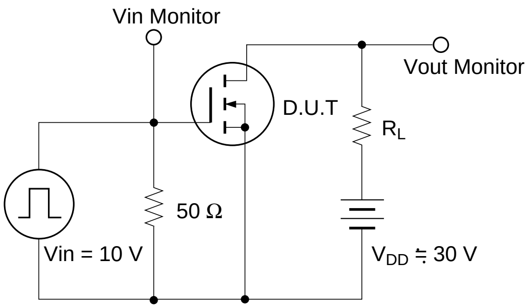


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5
Reverse Drain Current IDR (A)
Source to Drain Voltage VSD (V)
0
4
8
12
16
20
0.4
0.8
1.2
1.6
2.0

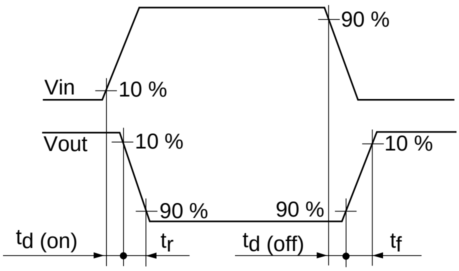


Normalized Transient Thermal Impedance vs. Pulse Width
TC = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γs (t) · θch–c
θch–c = 2.50°C/W, TC = 25°C
PDM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1303

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

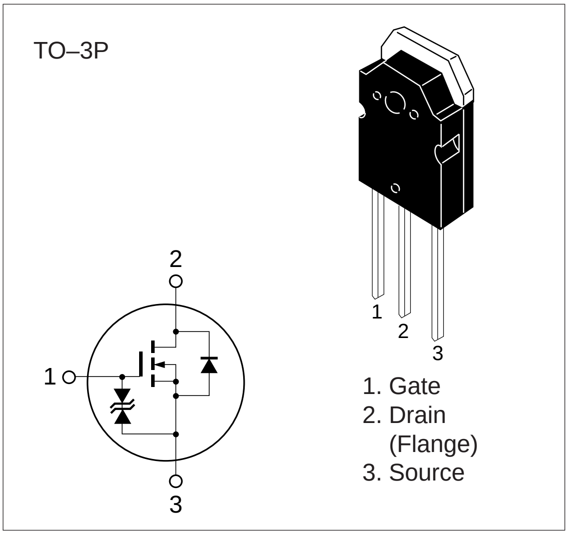


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$*	120	A
Body to drain diode reverse drain current	I_{DR}	30	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

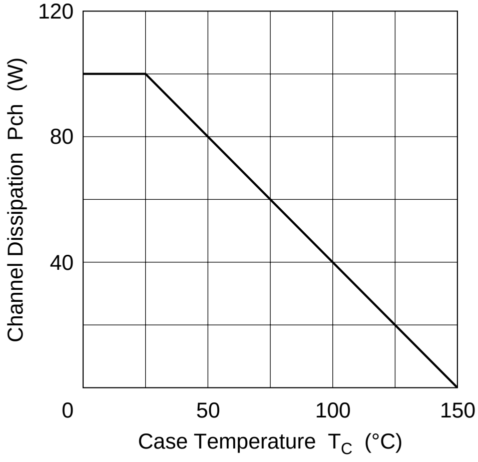
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

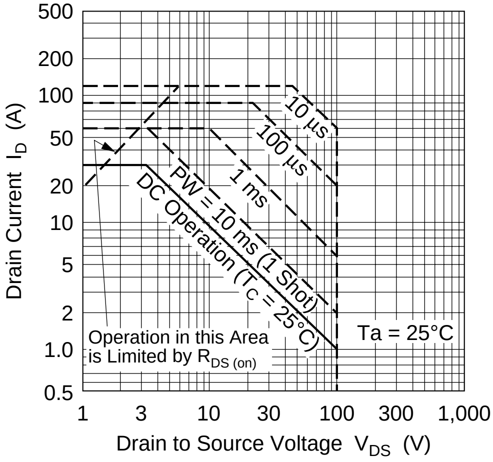
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.06	Ω	I_D = 15 A, V_{GS} = 10 V *
		—	0.06	0.09		I_D = 15 A, V_{GS} = 4 V *
Forward transfer admittance	$\lvert y_{fs} \rvert$	13	22	—	S	I_D = 15 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1750	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	710	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	180	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 15 A, V_{GS} = 10 V,
Rise time	t_r	—	120	—	ns	R_L = 2 Ω
Turn-off delay time	$t_{d(off)}$	—	390	—	ns	
Fall time	t_f	—	195	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 30 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	360	—	ns	I_F = 30 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

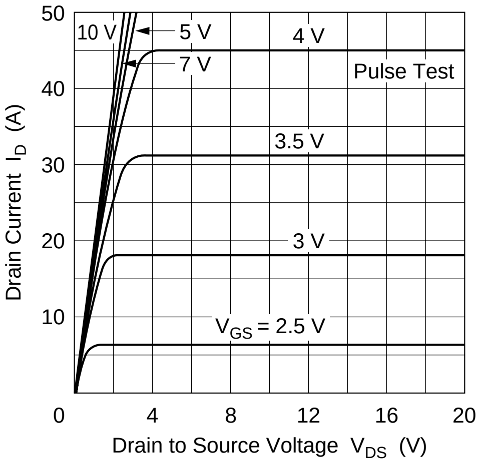
Power vs. Temperature Derating



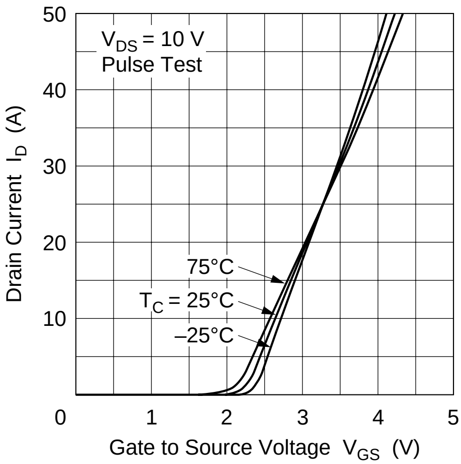
Maximum Safe Operation Area

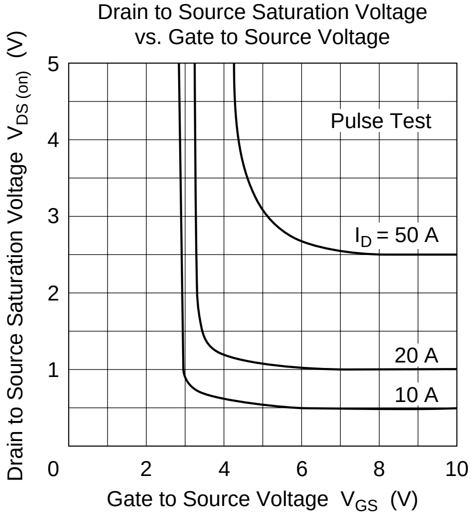


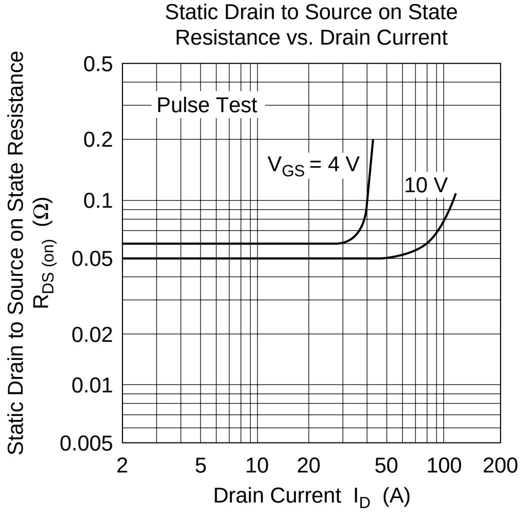
Typical Output Characteristics

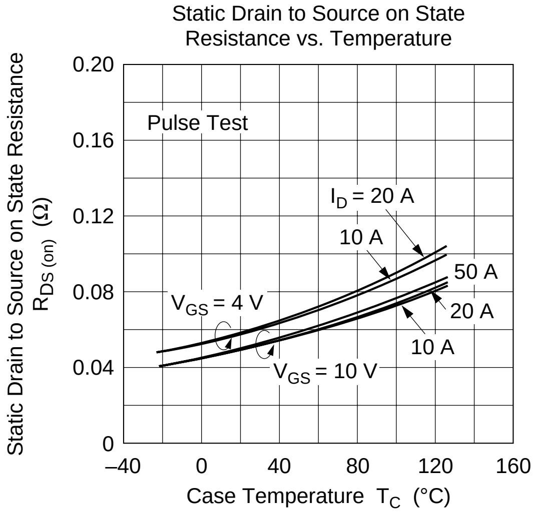


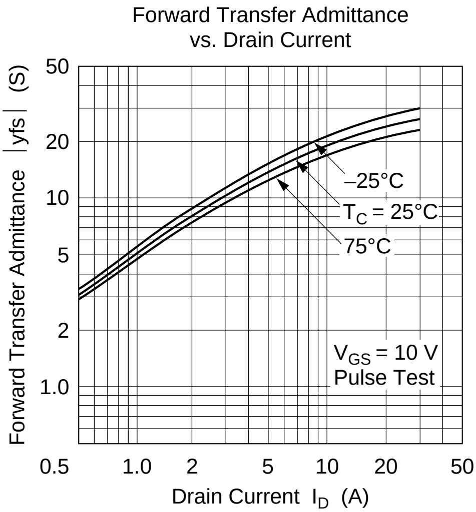
Typical Transfer Characteristics

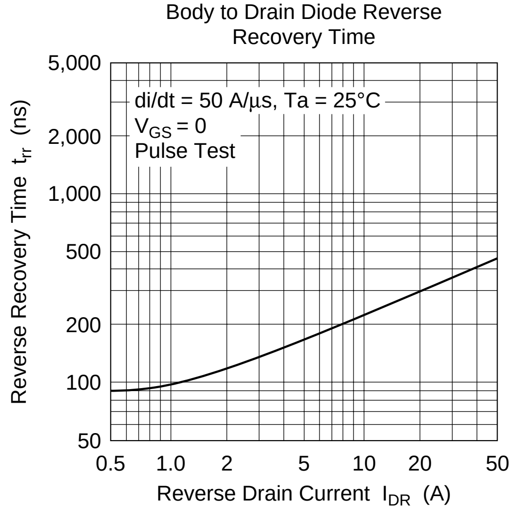


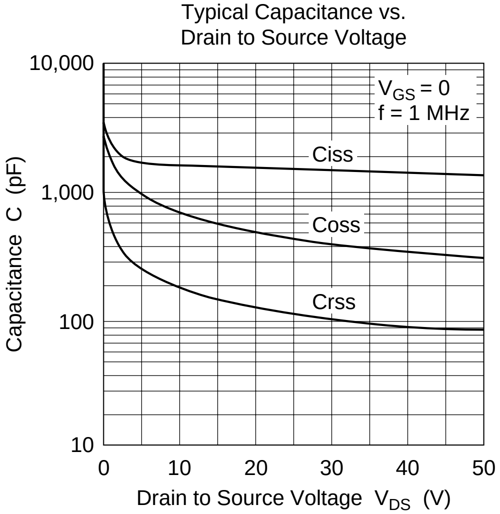

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS\,(on)}$ (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
I_D = 50 A
20 A
10 A
0
1
2
3
4
5
2
4
6
8
10

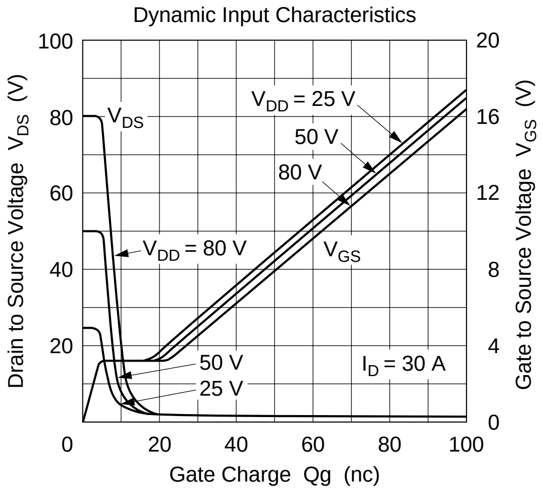

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State Resistance
$R_{DS\,(on)}$ (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 4 V
10 V
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200

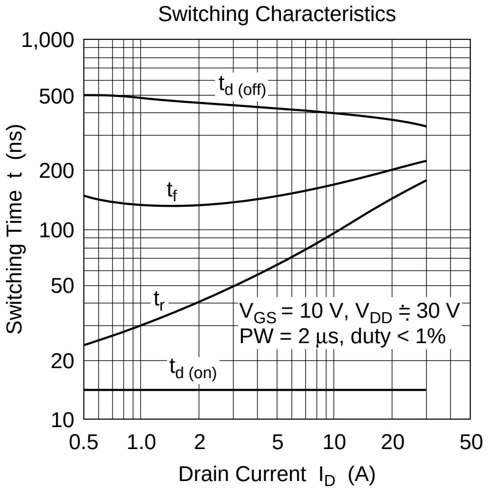

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance
$R_{DS\,(on)}$ (Ω)
Case Temperature T_C (°C)
Pulse Test
I_D = 20 A
10 A
50 A
20 A
10 A
V_{GS} = 4 V
V_{GS} = 10 V
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160


Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
–25°C
T_C = 25°C
75°C
V_{GS} = 10 V
Pulse Test
50
20
10
5
2
1.0
0.5
1.0
2
5
10
20
50

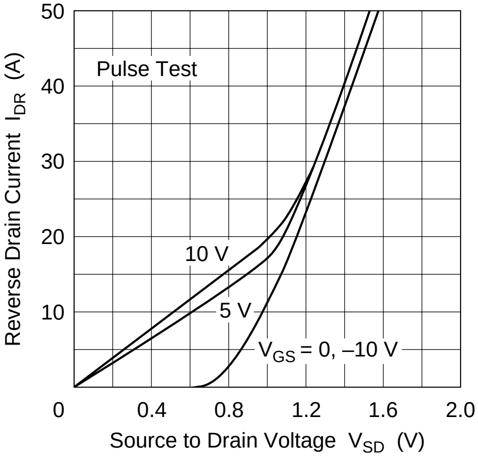

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/μs, Ta = 25°C
V_GS = 0
Pulse Test
Reverse Recovery Time t_rr (ns)
5,000
2,000
1,000
500
200
100
50
0.5
1.0
2
5
10
20
50
Reverse Drain Current I_DR (A)


Typical Capacitance vs. Drain to Source Voltage
V_GS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10,000
1,000
100
10
0
10
20
30
40
50
Drain to Source Voltage V_DS (V)

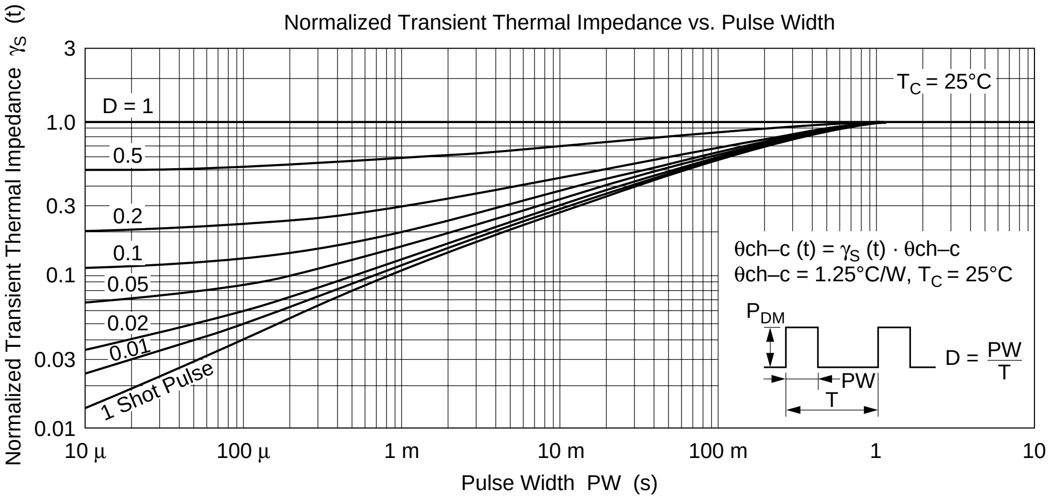

Dynamic Input Characteristics
V_DD = 25 V
50 V
80 V
V_DS
V_DD = 80 V
V_GS
50 V
25 V
I_D = 30 A
Drain to Source Voltage V_DS (V)
Gate to Source Voltage V_GS (V)
100
80
60
40
20
0
20
16
12
8
4
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
t_d (off)
t_f
t_r
t_d (on)
V_GS = 10 V, V_DD ≒ 30 V
PW = 2 μs, duty < 1%
Switching Time t (ns)
1,000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)

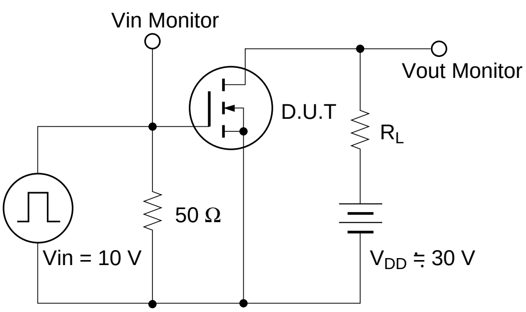
Reverse Drain Current vs.
Source to Drain Voltage



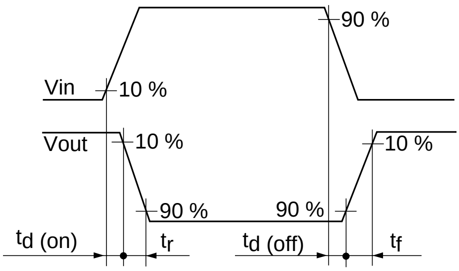
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Wavewforms



2SK1304

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

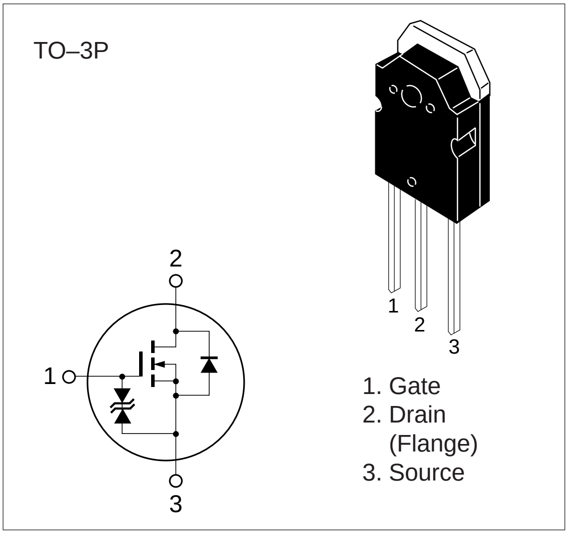


Table 1 Absolute Maximum Ratings (Ta = 25°C)

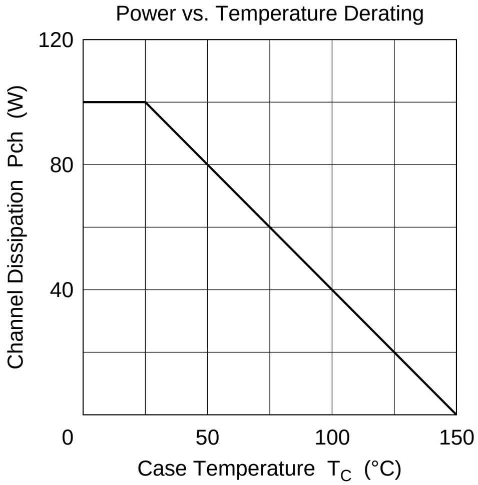
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*	160	A
Body to drain diode reverse drain current	I_{DR}	40	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

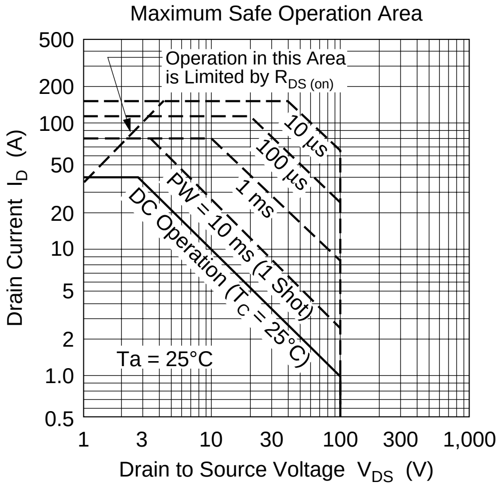
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

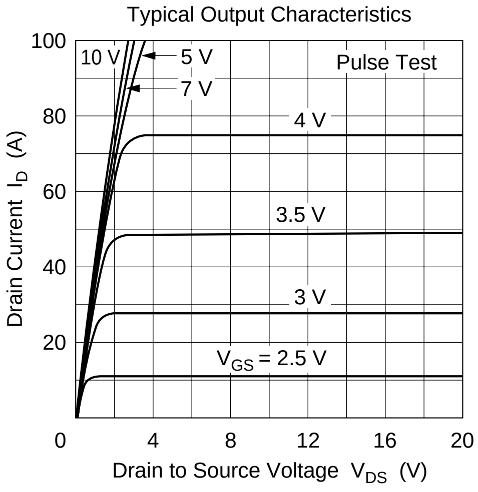
Table 2 Electrical Characteristics (Ta = 25°C)

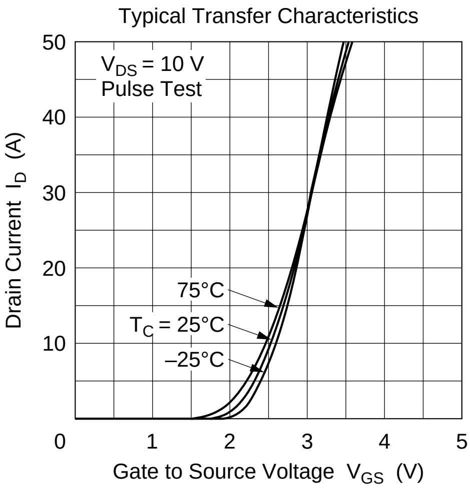
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.025	0.03	Ω	I_D = 20 A, V_{GS} = 10 V *
		—	0.03	0.04		I_D = 20 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	22	35	—	S	I_D = 20 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	3500	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	1400	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	340	—	pF	
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	I_D = 20 A, V_{GS} = 10 V,
Rise time	t_r	—	170	—	ns	R_L = 1.5 Ω
Turn-off delay time	$t_{d(off)}$	—	730	—	ns	
Fall time	t_f	—	300	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	300	—	ns	I_F = 40 A, V_{GS} = 0, di_F/dt = 50 A/µs

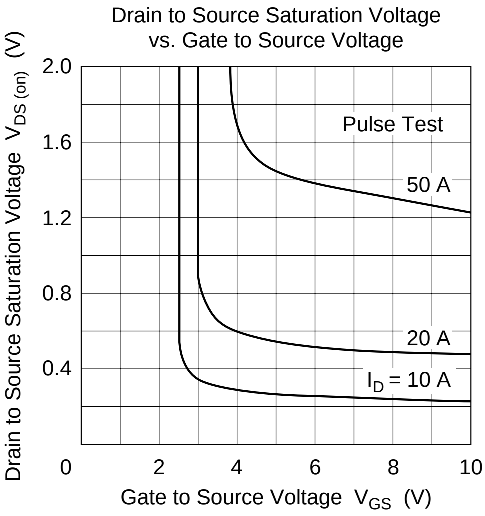
* Pulse Test

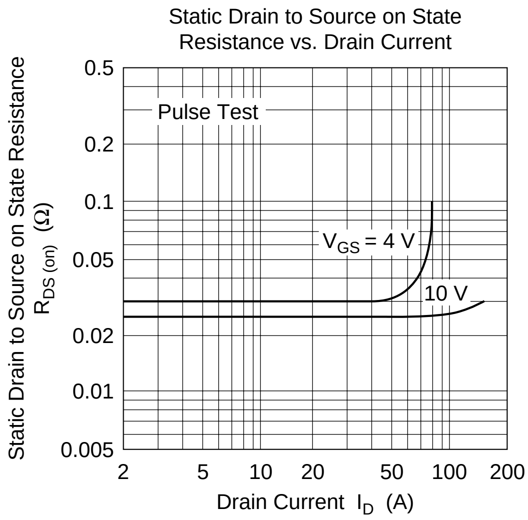

Power vs. Temperature Derating
120
80
40
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

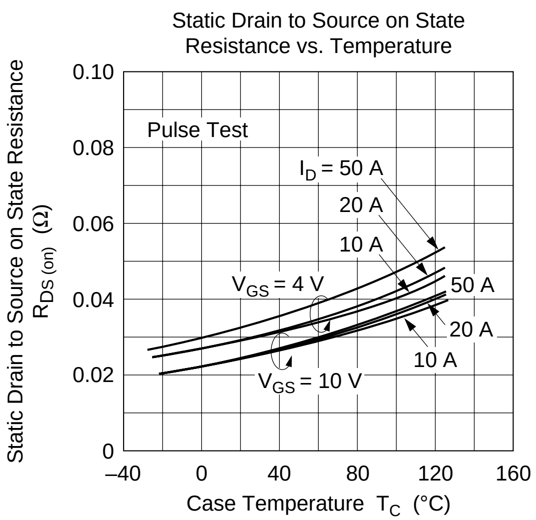

Maximum Safe Operation Area
Operation in this Area
is Limited by $R_{DS (on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Ta = 25°C
500
200
100
50
20
10
5
2
1.0
0.5
1
3
10
30
100
300
1,000
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

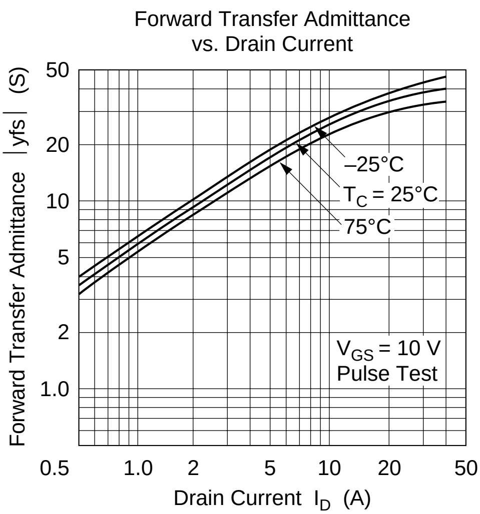

Typical Output Characteristics
10 V
5 V
7 V
Pulse Test
4 V
3.5 V
3 V
V_{GS} = 2.5 V
100
80
60
40
20
0
4
8
12
16
20
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

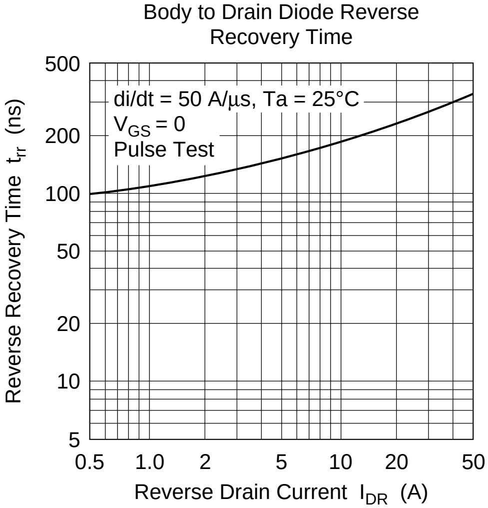

Typical Transfer Characteristics
V_{DS} = 10 V
Pulse Test
75°C
T_C = 25°C
–25°C
50
40
30
20
10
0
1
2
3
4
5
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

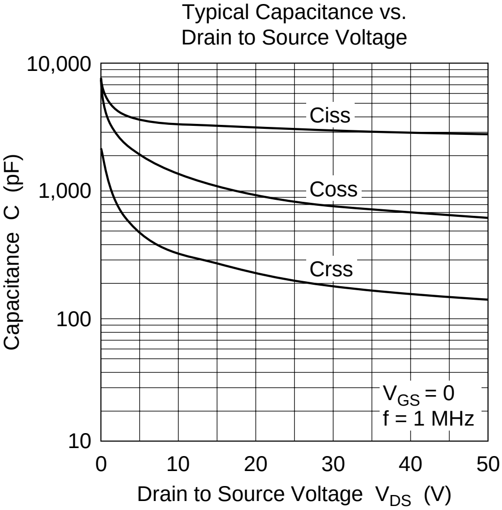

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
50 A
20 A
I_D = 10 A
Drain to Source Saturation Voltage V_DS (on) (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_GS (V)

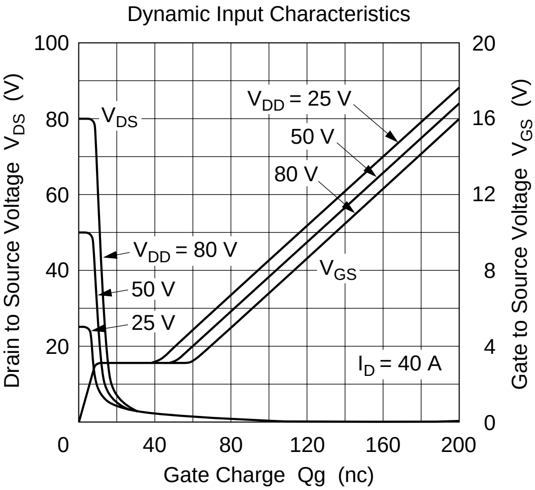

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_GS = 4 V
10 V
Static Drain to Source on State Resistance R_DS (on) (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I_D (A)

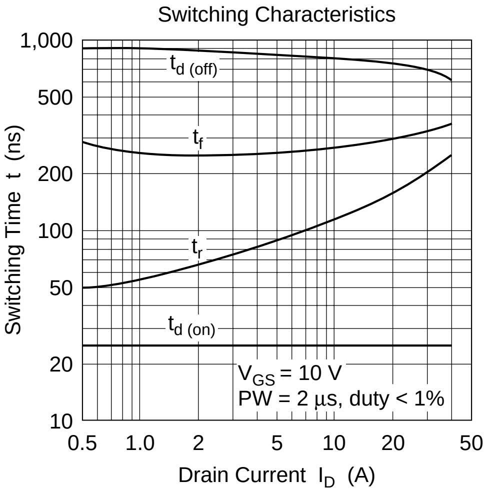

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
I_D = 50 A
20 A
10 A
V_GS = 4 V
50 A
20 A
10 A
V_GS = 10 V
Static Drain to Source on State Resistance R_DS (on) (Ω)
0.10
0.08
0.06
0.04
0.02
0
–40
0
40
80
120
160
Case Temperature T_C (°C)

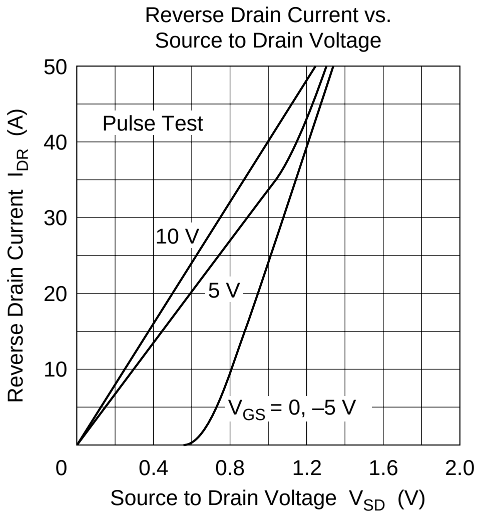

Forward Transfer Admittance
vs. Drain Current
–25°C
T_C = 25°C
75°C
V_GS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1.0
0.5
1.0
2
5
10
20
50
Drain Current I_D (A)

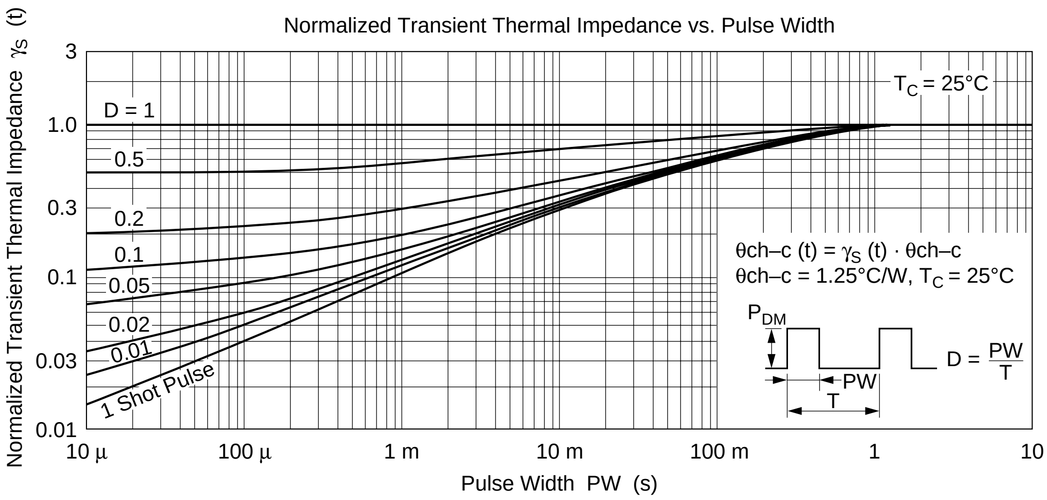

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/μs, Ta = 25°C
VGS = 0
Pulse Test
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.5
1.0
2
5
10
20
50
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
10,000
1,000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

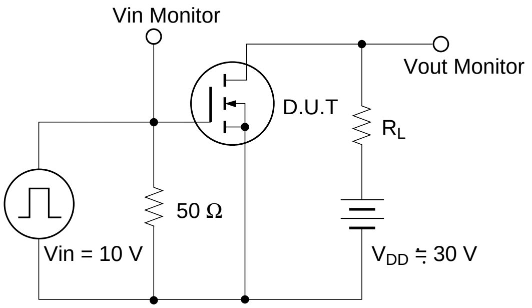

Dynamic Input Characteristics
VDS
VDD = 25 V
50 V
80 V
VDD = 80 V
50 V
25 V
VGS
ID = 40 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
td (off)
tf
tr
td (on)
VGS = 10 V
PW = 2 μs, duty < 1%
Switching Time t (ns)
1,000
500
200
100
50
20
10
0.5
1.0
2
5
10
20
50
Drain Current ID (A)

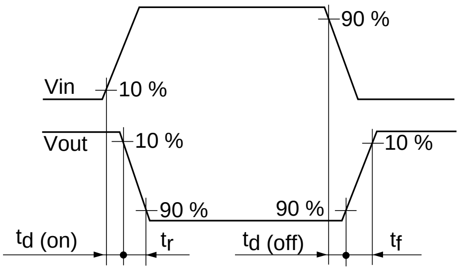

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
Reverse Drain Current IDR (A)
Source to Drain Voltage VSD (V)
0
0.4
0.8
1.2
1.6
2.0
10
20
30
40
50


Normalized Transient Thermal Impedance vs. Pulse Width
TC = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γS (t) · θch–c
θch–c = 1.25°C/W, TC = 25°C
PDM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γS (t)
Pulse Width PW (s)
3
1.0
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Wavewforms



2SK1305

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

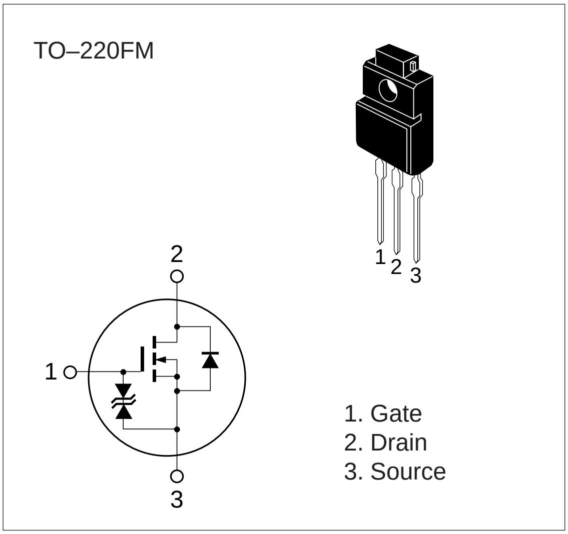


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

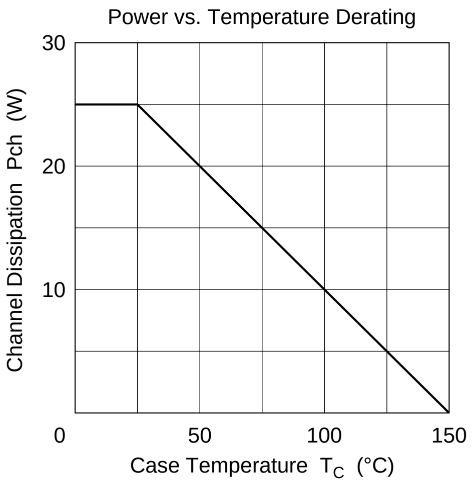
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

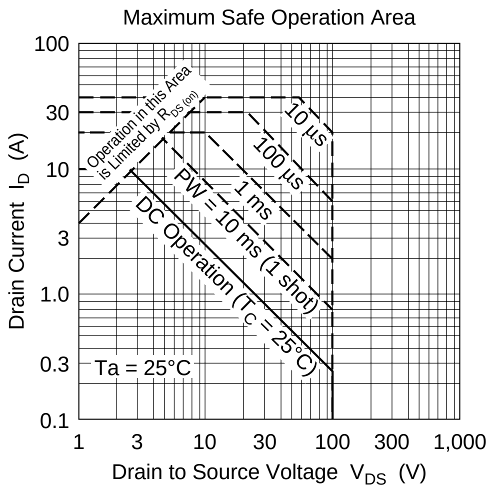
Table 2 Electrical Characteristics (Ta = 25°C)

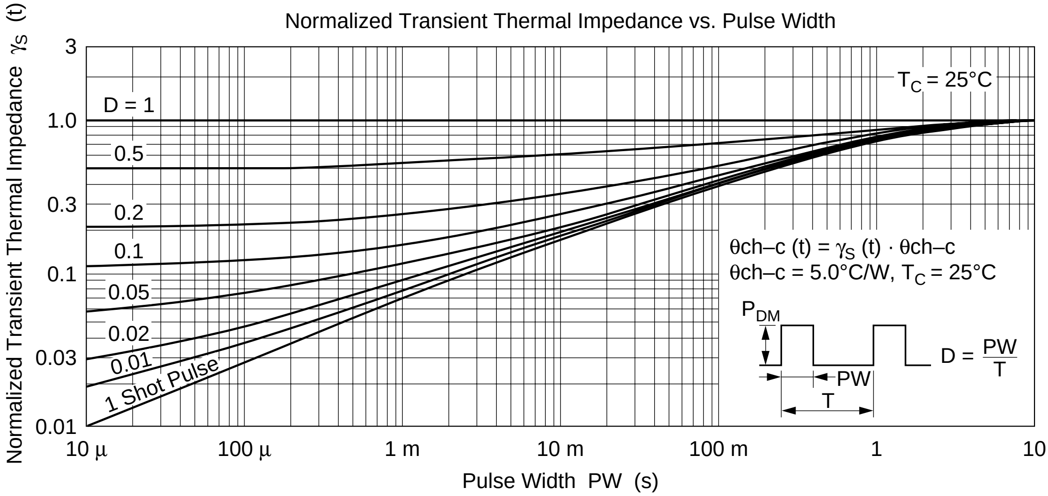
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.20	0.25	Ω	I_D = 5 A, V_{GS} = 10 V *
		—	0.25	0.35		I_D = 5 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	4.5	7.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	525	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	205	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	60	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time	t_r	—	50	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	170	—	ns	
Fall time	t_f	—	75	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK1300.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
Operation in this Area is Limited by $R_{DS(on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_C = 25°C)
Ta = 25°C
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 5.0°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1306

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

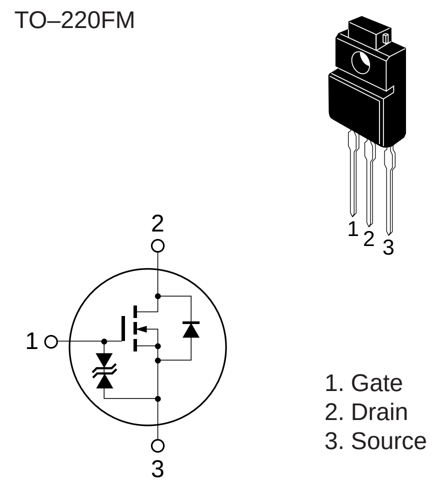


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body to drain diode reverse drain current	I_{DR}	15	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

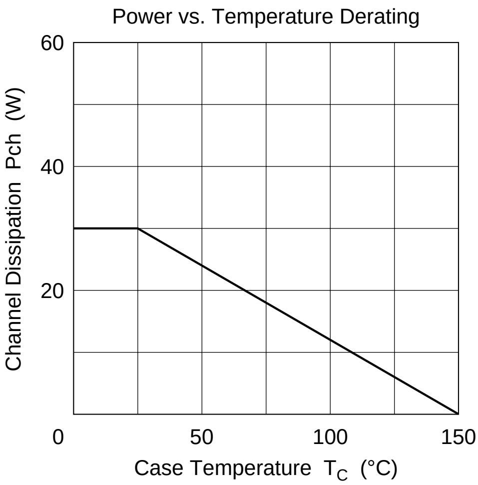
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

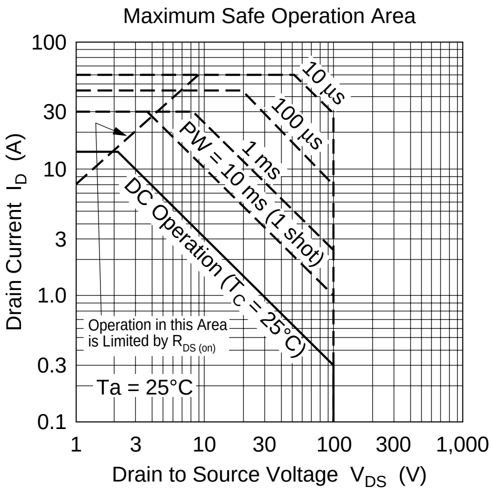
Table 2 Electrical Characteristics (Ta = 25°C)

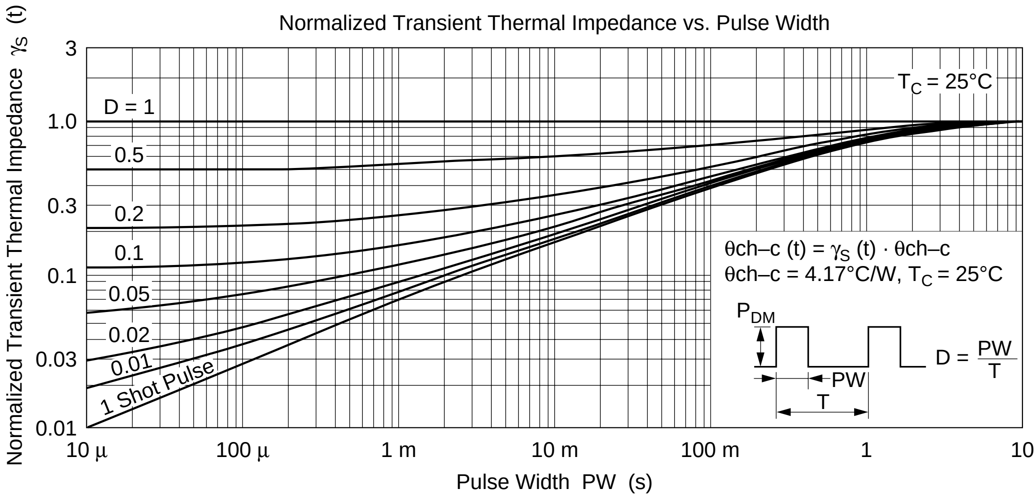
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.10	0.13	Ω	I_D = 8 A, V_{GS} = 10 V *
		—	0.13	0.18		I_D = 8 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	7	11	—	S	I_D = 8 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	340	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	100	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 8 A, V_{GS} = 10 V,
Rise time	t_r	—	70	—	ns	R_L = 3.75 Ω
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	
Fall time	t_f	—	100	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 15 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	250	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK1301.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS\ (on)}$
Ta = 25°C
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 4.17°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1307

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

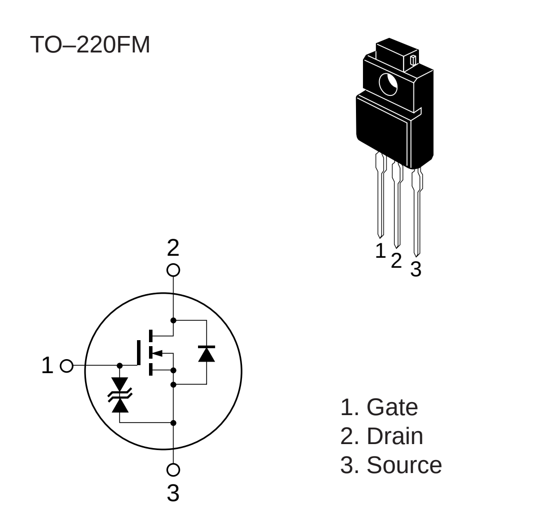


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body to drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

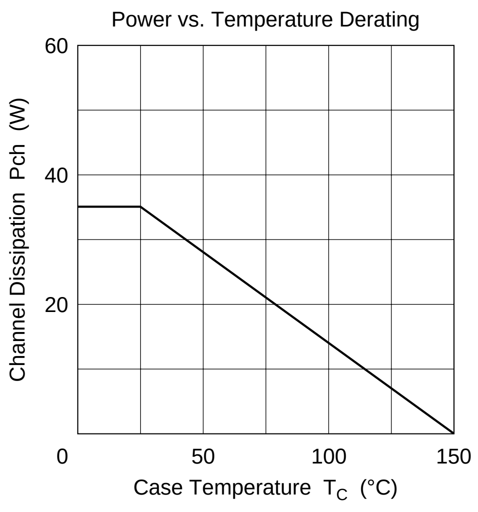
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

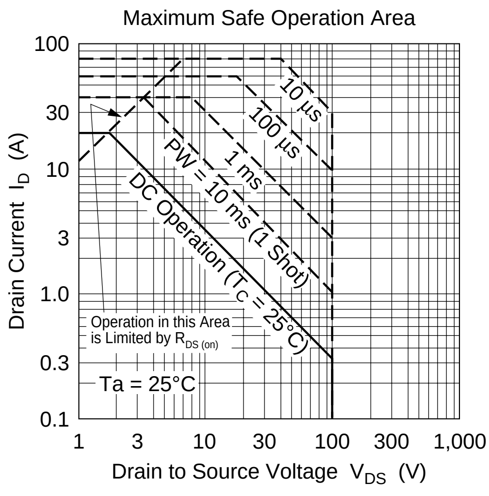
Table 2 Electrical Characteristics (Ta = 25°C)

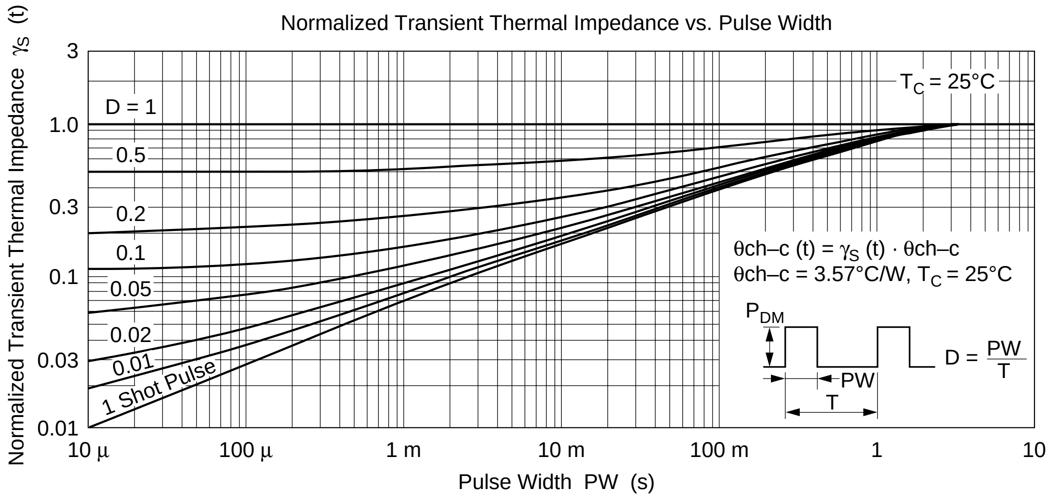
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.065	0.085	Ω	I_D = 10 A, V_{GS} = 10 V *
		—	0.085	0.12		I_D = 10 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	16	—	S	I_D = 10 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1300	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	540	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	160	—	pF	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	I_D = 10 A, V_{GS} = 10 V,
Rise time	t_r	—	100	—	ns	R_L = 3 Ω
Turn-off delay time	$t_{d(off)}$	—	300	—	ns	
Fall time	t_f	—	150	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 20 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	300	—	ns	I_F = 20 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK1302.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS (on)}$
Ta = 25°C
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
T_C = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch–c (t) = γ_S (t) · θch–c
θch–c = 3.57°C/W, T_C = 25°C
P_{DM}
PW
T
$D = \frac{PW}{T}$
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1313(L), 2SK1314(L), 2SK1313(S), 2SK1314(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

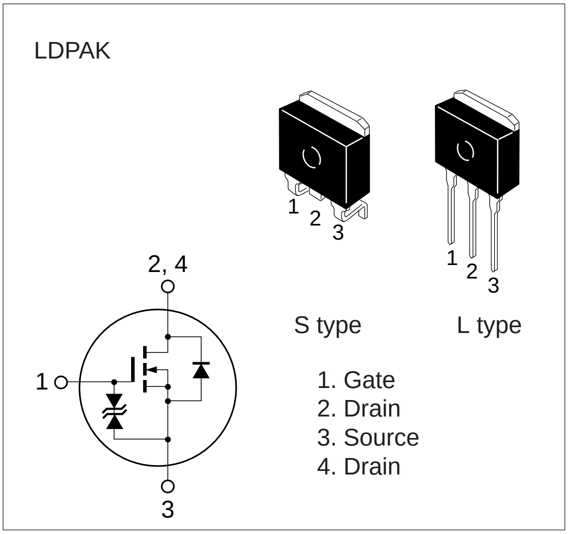


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1313	V_{DSS}	450	V
	2SK1314		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	5	A
Drain peak current		$I_{D(pulse)}$*	20	A
Body to drain diode reverse drain current		I_{DR}	5	A
Channel dissipation		Pch**	50	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

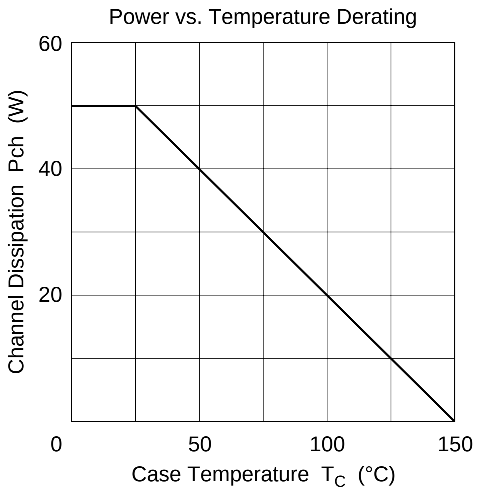
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	2SK1313	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1314		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1313	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1314						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1313	$R_{DS(on)}$	—	1.0	1.4	Ω	I_D = 2.5 A, V_{GS} = 10 V *
	2SK1314		—	1.2	1.5		
Forward transfer admittance		$\|y_{fs}\|$	2.5	4.0	—	S	I_D = 2.5 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	640	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	160	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	20	—	pF	
Turn-on delay time		$t_{d(on)}$	—	10	—	ns	I_D = 2.5 A, V_{GS} = 10 V,
Rise time		t_r	—	25	—	ns	R_L = 12 Ω
Turn-off delay time		$t_{d(off)}$	—	50	—	ns	
Fall time		t_f	—	30	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 5 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	300	—	ns	I_F = 5 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

See characteristic curves of 2SK1155, 2SK1156.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

2SK1315 (L), 2SK1316 (L), 2SK1315 (S), 2SK1316 (S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

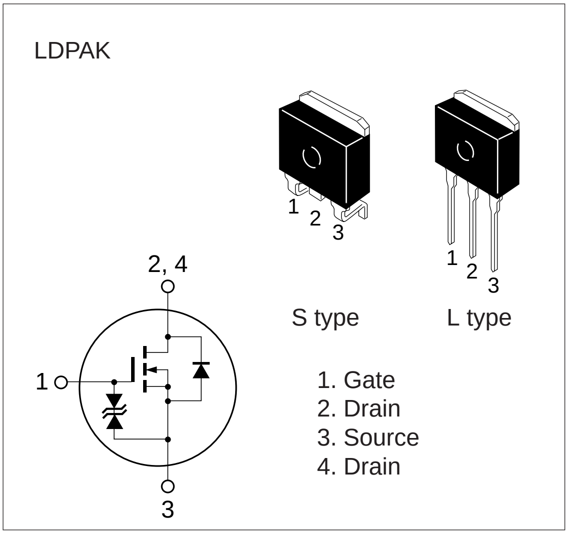


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1315	V_{DSS}	450	V
	2SK1316		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	8	A
Drain peak current		$I_{D(pulse)}^*$	32	A
Body to drain diode reverse drain current		I_{DR}	8	A
Channel dissipation		Pch**	60	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

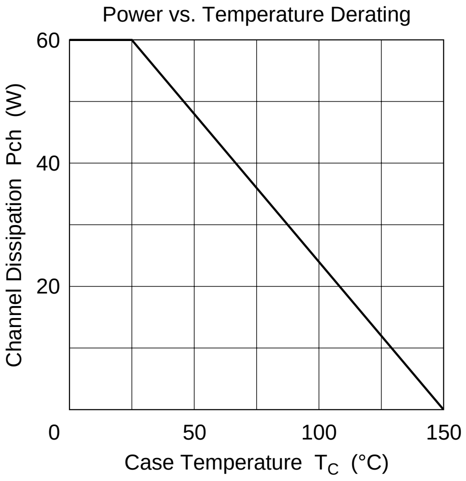
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	2SK1315	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1316		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1315	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1316						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1315	$R_{DS(on)}$	—	0.55	0.7	Ω	I_D = 4 A, V_{GS} = 10 V *
	2SK1316		—	0.60	0.8		
Forward transfer admittance		$\|y_{fs}\|$	4.5	7.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1150	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	340	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	55	—	pF	
Turn-on delay time		$t_{d(on)}$	—	17	—	ns	I_D = 4 A, V_{GS} = 10 V,
Rise time		t_r	—	55	—	ns	R_L = 7.5 Ω
Turn-off delay time		$t_{d(off)}$	—	100	—	ns	
Fall time		t_f	—	45	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	350	—	ns	I_F = 8 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

See characteristic curves of 2SK1159, 2SK1160.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

2SK1328, 2SK1329

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

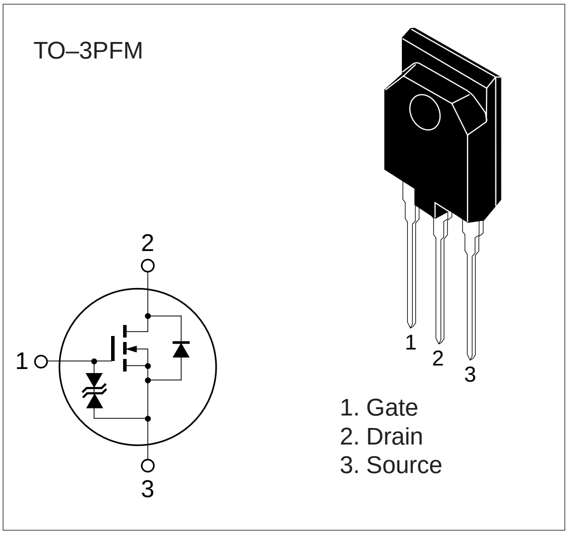


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1328	V_{DSS}	450	V
	2SK1329		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	12	A
Drain peak current		$I_{D(pulse)}$*	48	A
Body to drain diode reverse drain current		I_{DR}	12	A
Channel dissipation		Pch**	60	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

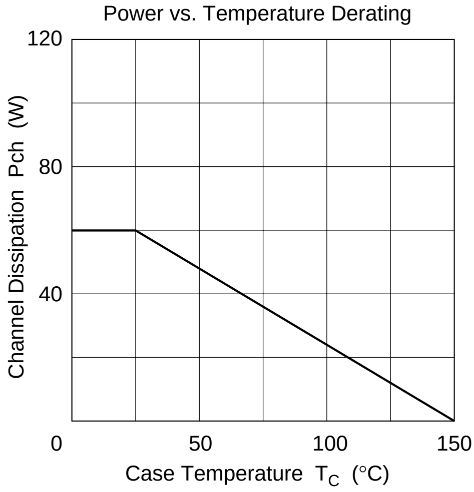
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

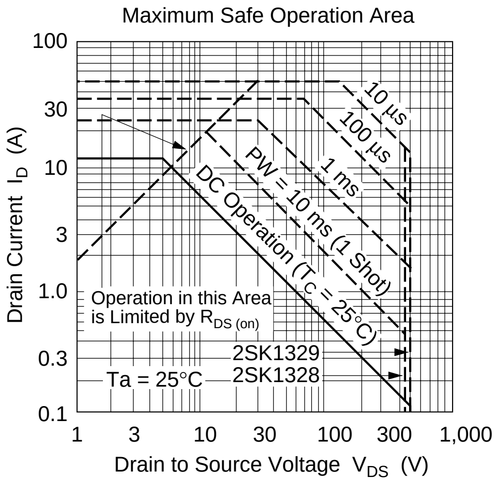
Table 2 Electrical Characteristics (Ta = 25°C)

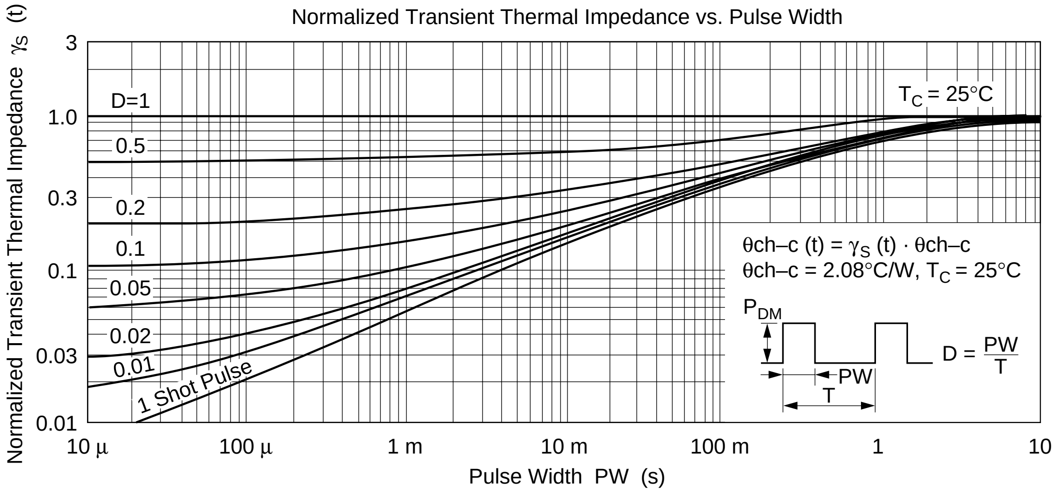
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1328	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1329		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	μA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1328	I_{DSS}	—	—	250	μA	V_{DS} = 360 V, V_{GS} = 0
	2SK1329						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1328	$R_{DS(on)}$	—	0.40	0.55	Ω	I_D = 6 A, V_{GS} = 10 V *
	2SK1329		—	0.45	0.60		
Forward transfer admittance		$\|y_{fs}\|$	6.0	10	—	S	I_D = 6 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1450	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	410	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	55	—	pF	
Turn-on delay time		$t_{d(on)}$	—	20	—	ns	I_D = 6 A, V_{GS} = 10 V,
Rise time		t_r	—	70	—	ns	R_L = 5 Ω
Turn-off delay time		$t_{d(off)}$	—	120	—	ns	
Fall time		t_f	—	60	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 12 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	450	—	ns	I_F = 12 A, V_{GS} = 0, di_F/dt = 100 A/μs

* Pulse Test

See characteristic curves of 2SK1165, 2SK1166.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
120
80
40
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1.0
0.3
0.1
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS (on)}$
2SK1329
2SK1328
Ta = 25°C
1
3
10
30
100
300
1,000
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ_S (t)
3
1.0
0.3
0.1
0.03
0.01
D=1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
θch–c (t) = γ_S (t) · θch–c
θch–c = 2.08°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1540(L), 2SK1541(L), 2SK1540(S), 2SK1541(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

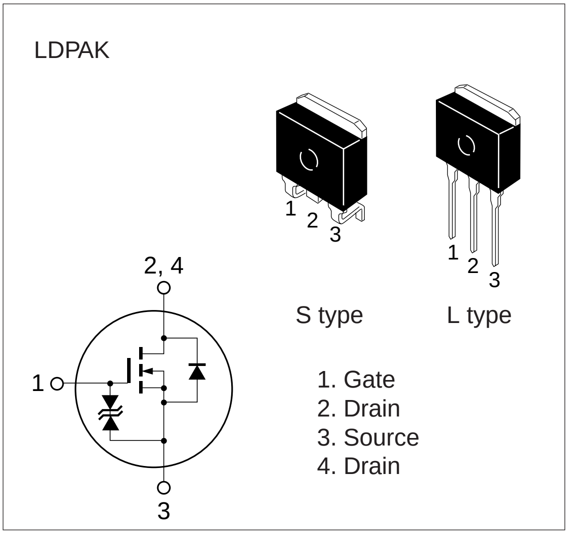


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1540	V_{DSS}	450	V
	2SK1541		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	7	A
Drain peak current		$I_{D(pulse)}$*	28	A
Body to drain diode reverse drain current		I_{DR}	7	A
Channel dissipation		Pch**	60	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

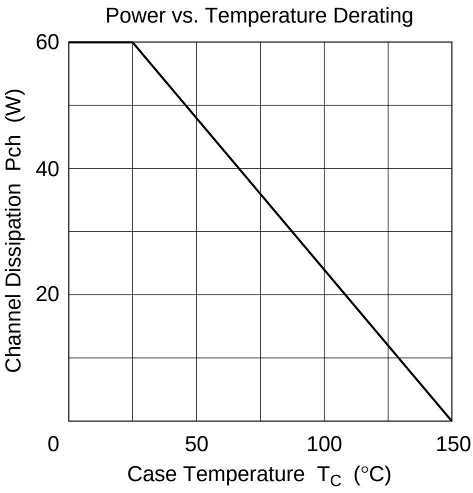
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	2SK1540	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1541		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1540	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1541						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1540	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 4 A, V_{GS} = 10 V *
	2SK1541		—	0.7	0.9		
Forward transfer admittance		$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1050	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	280	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	40	—	pF	
Turn-on delay time		$t_{d(on)}$	—	15	—	ns	I_D = 4 A, V_{GS} = 10 V,
Rise time		t_r	—	55	—	ns	R_L = 7.5 Ω
Turn-off delay time		$t_{d(off)}$	—	95	—	ns	
Fall time		t_f	—	40	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 7 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	320	—	ns	I_F = 7 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

See characteristic curves of 2SK1157, 2SK1158.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

2SK1566, 2SK1567

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

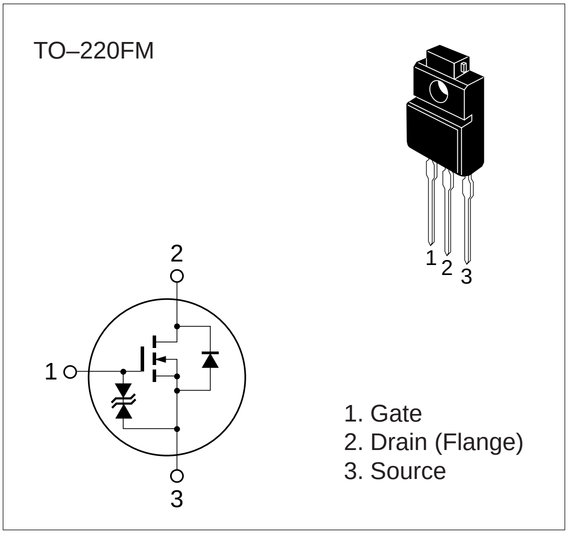


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1566	V_{DSS}	450	V
	2SK1567		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	7	A
Drain peak current		$I_{D(pulse)}$*	28	A
Body to drain diode reverse drain current		I_{DR}	7	A
Channel dissipation		Pch**	35	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

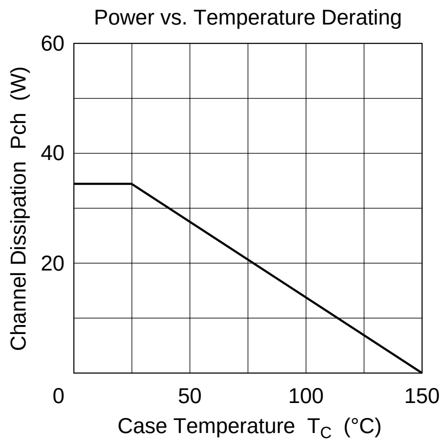
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

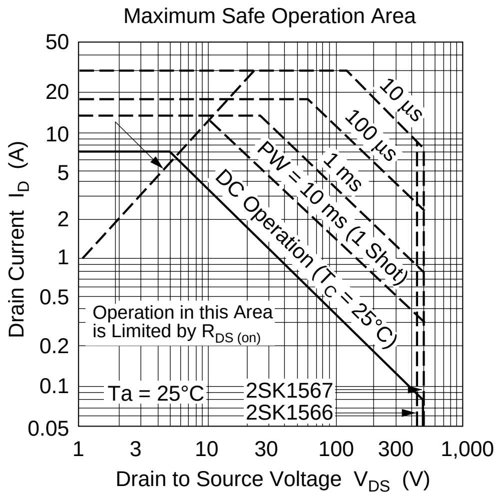
Table 2 Electrical Characteristics (Ta = 25°C)

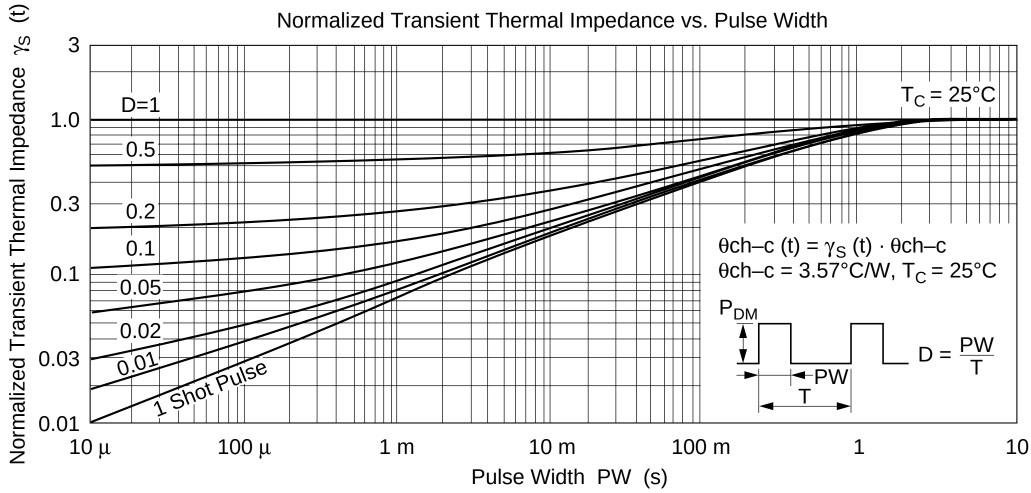
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1566	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1567		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1566	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1567						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1566	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 4 A, V_{GS} = 10 V *
	2SK1567		—	0.7	0.9		
Forward transfer admittance		$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	1050	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	280	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	40	—	pF	
Turn-on delay time		$t_{d(on)}$	—	15	—	ns	I_D = 4 A, V_{GS} = 10 V,
Rise time		t_r	—	55	—	ns	R_L = 7.5 Ω
Turn-off delay time		$t_{d(off)}$	—	95	—	ns	
Fall time		t_f	—	40	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 7 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	320	—	ns	I_F = 7 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

See characteristic curves of 2SK1157, 2SK1158.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
Case Temperature T_C (°C)


Maximum Safe Operation Area
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this Area is Limited by $R_{DS (on)}$
Ta = 25°C
2SK1567
2SK1566
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
T_C = 25°C
D=1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
$\theta ch\text{–}c (t) = \gamma_S (t) \cdot \theta ch\text{–}c$
$\theta ch\text{–}c = 3.57°C/W$, $T_C = 25°C$
P_{DM}
PW
T
$D = \frac{PW}{T}$
Normalized Transient Thermal Impedance γ_S (t)
Pulse Width PW (s)

2SK1620(L), 2SK1620(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

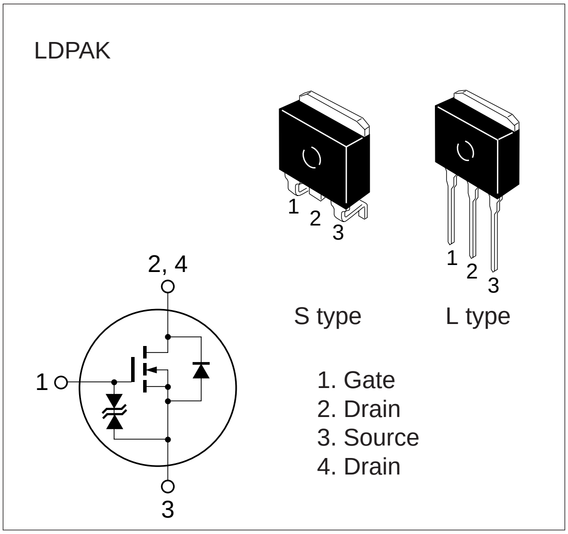


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	150	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

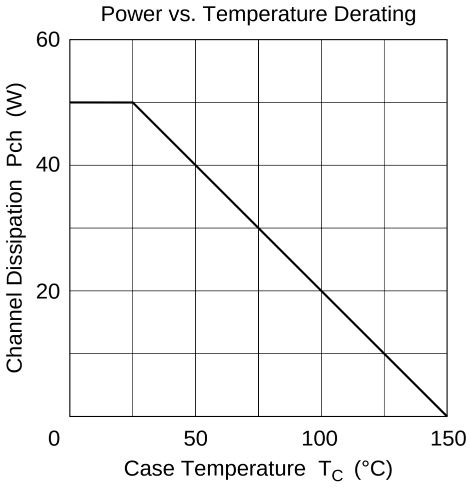
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	150	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 120 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 5 A, V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	7.0	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1200	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	550	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	85	—	pF	
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 5 A, V_{GS} = 10 V,
Rise time	t_r	—	50	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	t_f	—	40	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK740.


Power vs. Temperature Derating
60
40
20
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

2SK1621(L), 2SK1621(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and motor driver

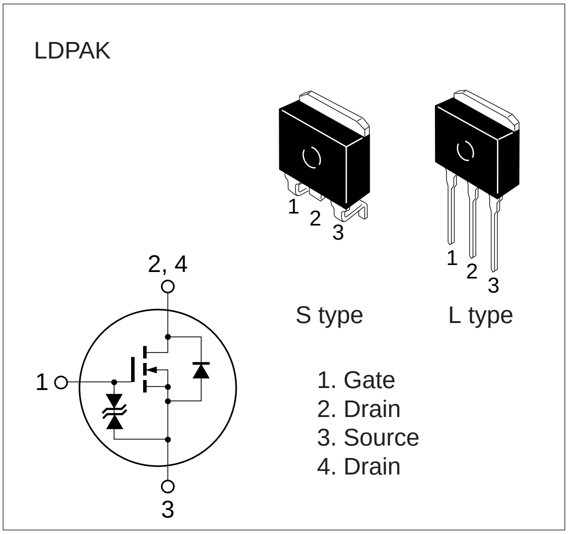


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body to drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

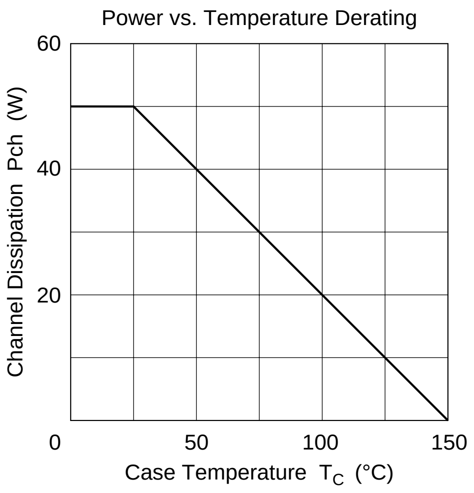
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.40	0.55	Ω	I_D = 4 A, V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	2.7	4.5	—	S	I_D = 4 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	820	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	370	—	pF	
Reverse transfer capacitance	Crss	—	115	—	pF	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	I_D = 4 A, V_{GS} = 10 V, R_L = 7.5 Ω
Rise time	t_r	—	48	—	ns	
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	t_f	—	50	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 7 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	400	—	ns	I_F = 7 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK741.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

2SK1622(L), 2SK1622(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

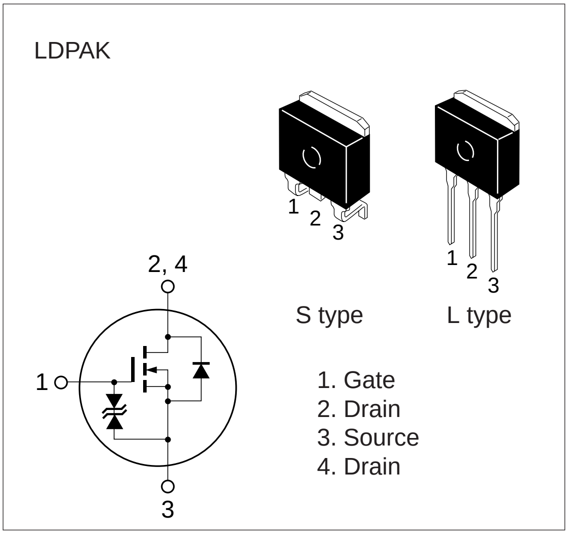


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$*	100	A
Body to drain diode reverse drain current	I_{DR}	25	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

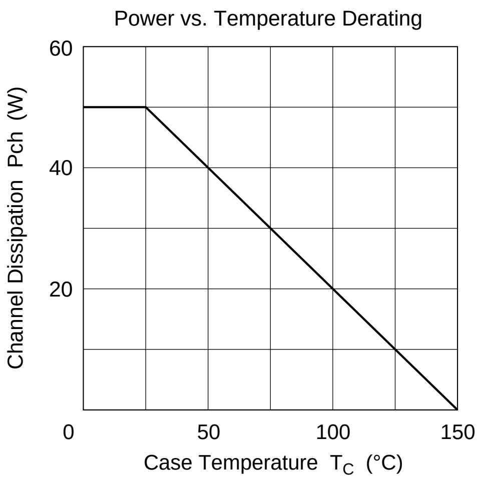
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.04	Ω	I_D = 15 A, V_{GS} = 10 V *
		—	0.05	0.06		I_D = 15 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	20	—	S	I_D = 15 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	720	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	220	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 15 A, V_{GS} = 10 V,
Rise time	t_r	—	130	—	ns	R_L = 2 Ω
Turn-off delay time	$t_{d(off)}$	—	270	—	ns	
Fall time	t_f	—	180	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 25 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 25 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK972.


Power vs. Temperature Derating
60
40
20
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

2SK1626, 2SK1627

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

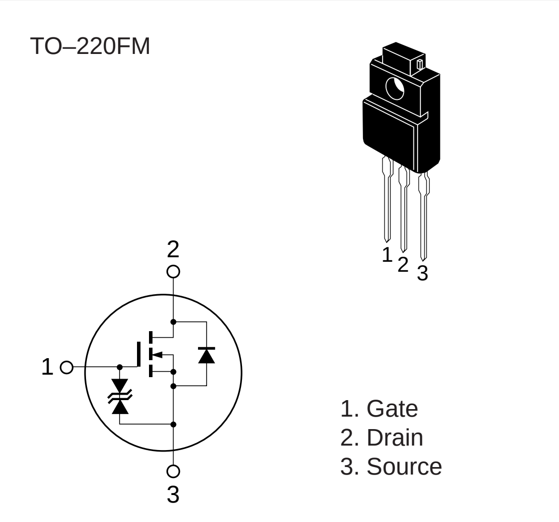


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1626	V_{DSS}	450	V
	2SK1627		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	5	A
Drain peak current		$I_{D(pulse)}$*	20	A
Body to drain diode reverse drain current		I_{DR}	5	A
Channel dissipation		Pch**	35	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +125	°C

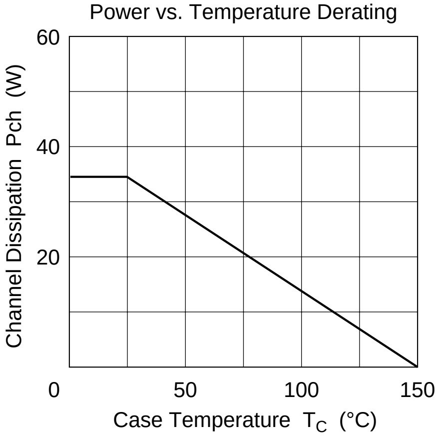
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

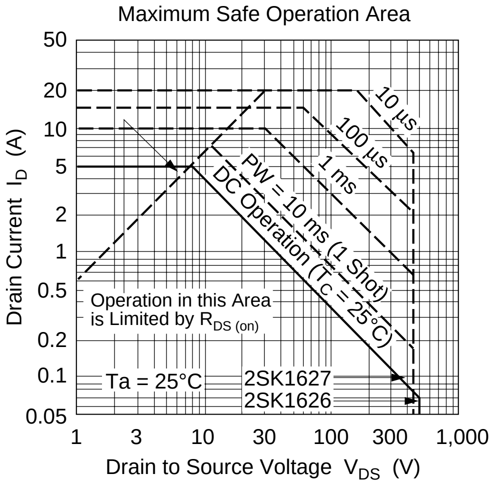
Table 2 Electrical Characteristics (Ta = 25°C)

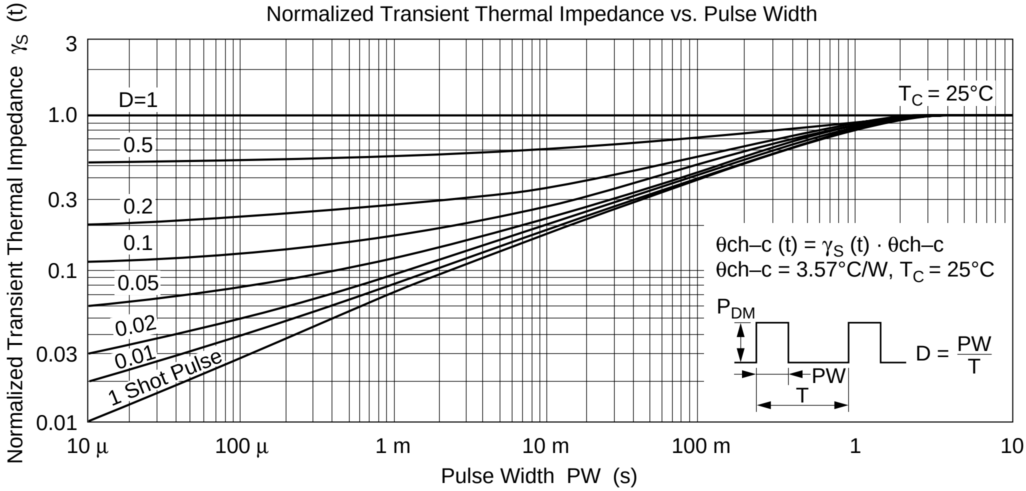
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1626	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1627		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1626	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1627						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	2SK1626	$R_{DS(on)}$	—	1.0	1.4	Ω	I_D = 2.5 A, V_{GS} = 10 V *
	2SK1627		—	1.2	1.5		
Forward transfer admittance		$\|y_{fs}\|$	2.5	4.0	—	S	I_D = 2.5 A, V_{DS} = 10 V *
Input capacitance		Ciss	—	640	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance		Coss	—	160	—	pF	f = 1 MHz
Reverse transfer capacitance		Crss	—	20	—	pF	
Turn-on delay time		$t_{d(on)}$	—	10	—	ns	I_D = 2.5 A, V_{GS} = 10 V,
Rise time		t_r	—	25	—	ns	R_L = 12 Ω
Turn-off delay time		$t_{d(off)}$	—	50	—	ns	
Fall time		t_f	—	30	—	ns	
Body to drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 5 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	300	—	ns	I_F = 5 A, V_{GS} = 0, di_F/dt = 100 A/µs

* Pulse Test

See characteristic curves of 2SK1155, 2SK1156.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature TC (°C)


Maximum Safe Operation Area
Drain Current ID (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (TC = 25°C)
Operation in this Area is Limited by RDS (on)
Ta = 25°C
2SK1627
2SK1626
1
3
10
30
100
300
1,000
Drain to Source Voltage VDS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γS (t)
3
1.0
0.3
0.1
0.03
0.01
D=1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
TC = 25°C
θch–c (t) = γS (t) · θch–c
θch–c = 3.57°C/W, TC = 25°C
PDM
PW
T
D = PW/T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK1648(L), 2SK1648(S)

Silicon N-Channel MOS FET

Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- 4 V gate drive device
  – Can be driven from 5 V source
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

LDPAK

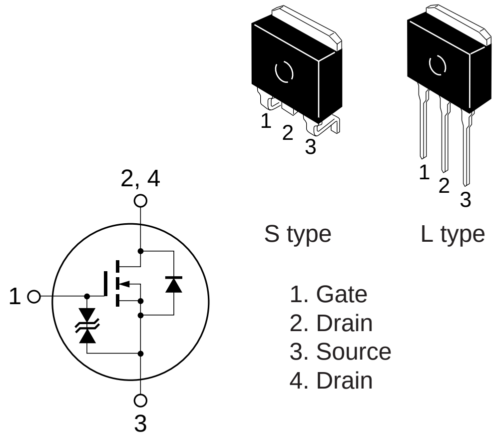


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body to drain diode reverse drain current	I_{DR}	15	A
Channel dissipation	Pch**	40	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

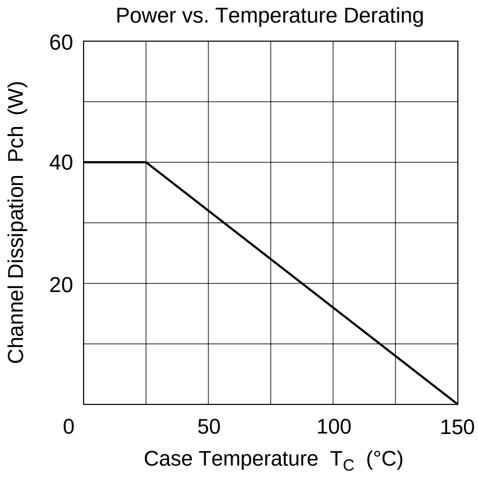
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at T_C = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.055	0.065	Ω	I_D = 8 A, V_{GS} = 10 V *
		—	0.075	0.095		I_D = 8 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = 8 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V, V_{GS} = 0,
Output capacitance	Coss	—	450	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	140	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 8 A, V_{GS} = 10 V,
Rise time	t_r	—	70	—	ns	R_L = 3.75 Ω
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	
Fall time	t_f	—	120	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 15 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 15 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK971.



Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature T_C (°C)

2SK1667

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC convertor

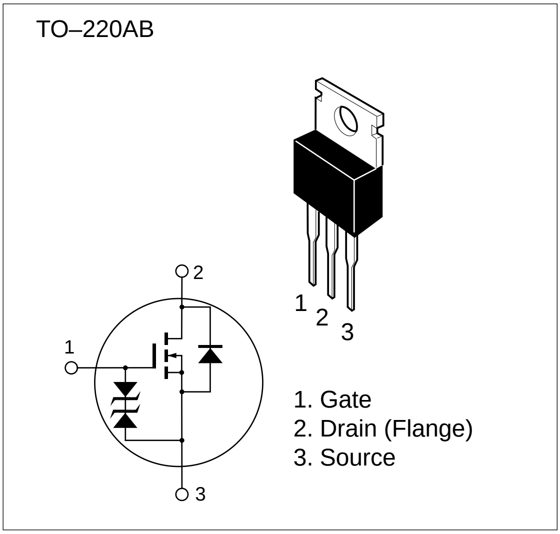


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

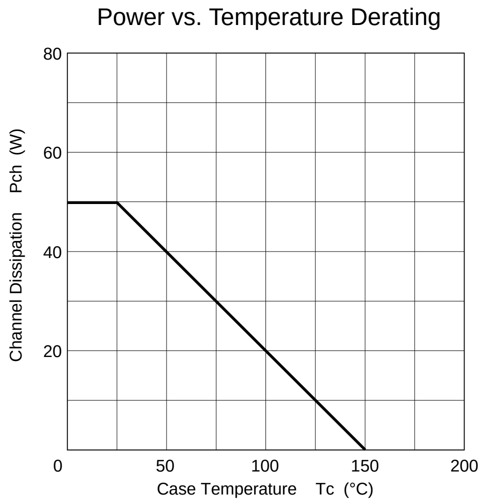
* PW ≤ 10 µs, duty cycle ≤ 1 %

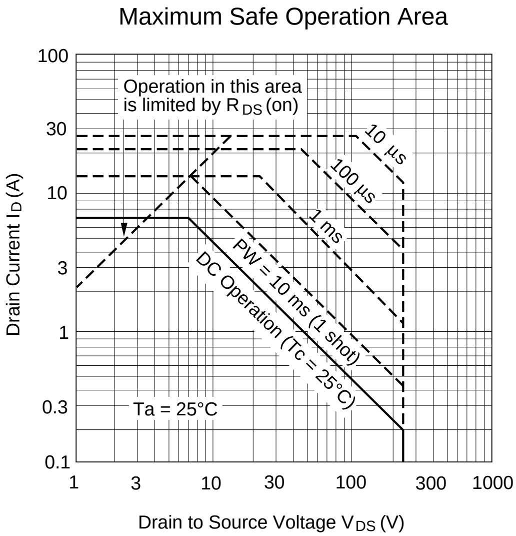
** Value at Tc = 25 °C

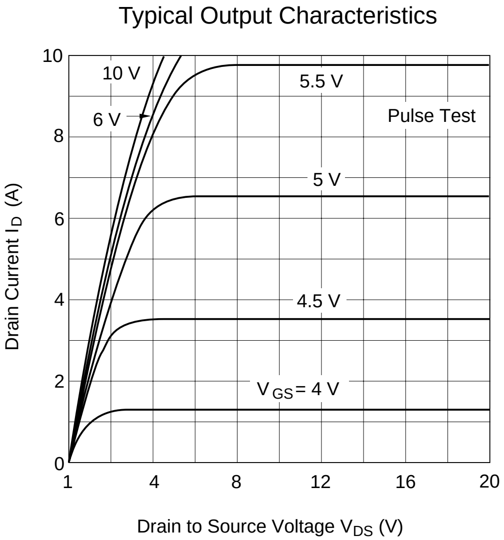
Table 2 Electrical Characteristics (Ta = 25°C)

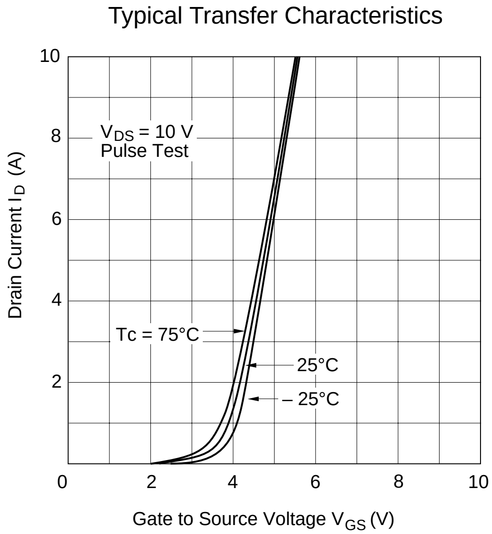
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.4	0.55	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	690	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	265	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	13	—	ns	I_D =4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	37	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	180	—	ns	I_F = 7 A, V_{GS} = 0, di_F / dt = 100 A / µs

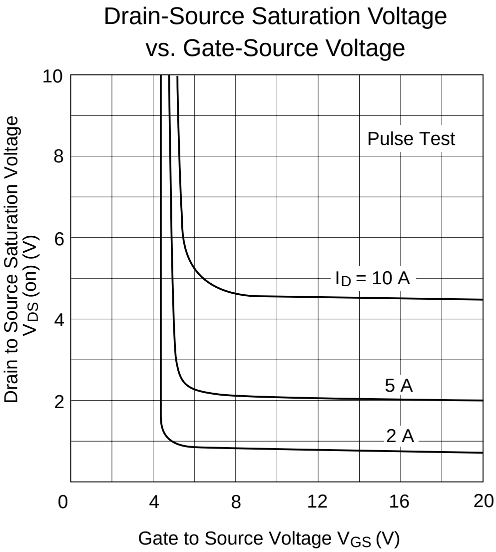
* Pulse Test

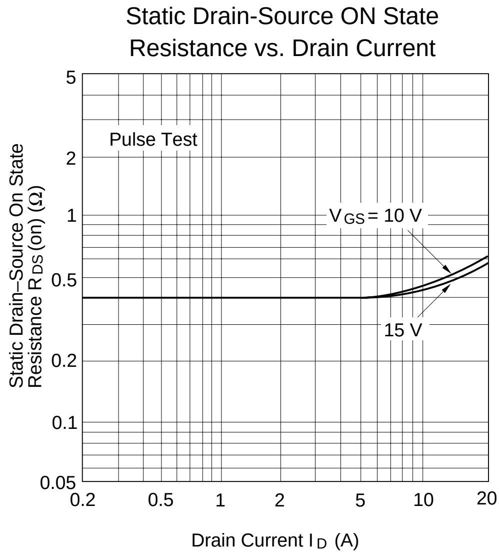

Power vs. Temperature Derating
80
60
40
20
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

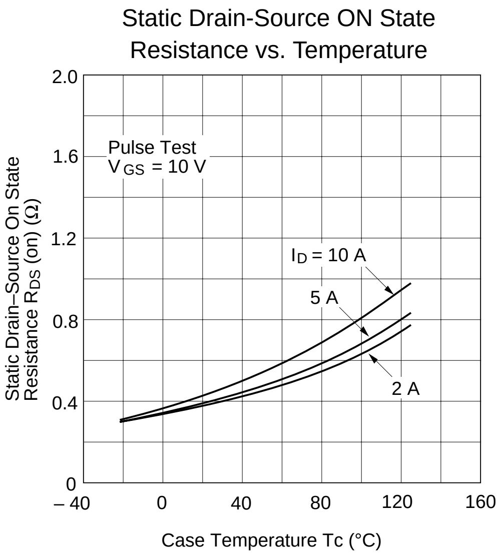

Maximum Safe Operation Area
Operation in this area
is limited by R DS (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25°C
100
30
10
3
1
0.3
0.1
1
3
10
30
100
300
1000
Drain Current I D (A)
Drain to Source Voltage V DS (V)

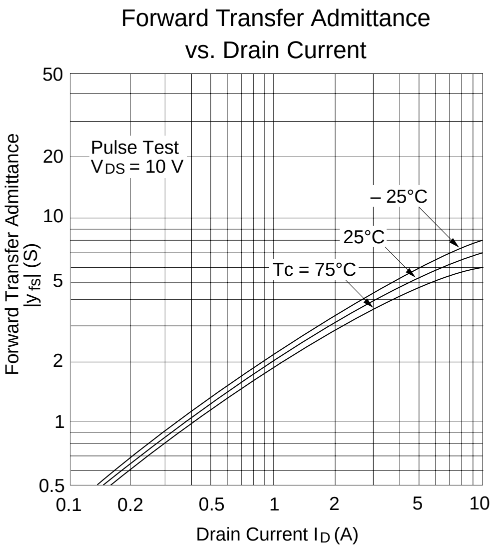

Typical Output Characteristics
10 V
6 V
5.5 V
Pulse Test
5 V
4.5 V
V GS = 4 V
10
8
6
4
2
0
1
4
8
12
16
20
Drain Current I D (A)
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
V DS = 10 V
Pulse Test
Tc = 75°C
25°C
– 25°C
10
8
6
4
2
0
2
4
6
8
10
Drain Current I D (A)
Gate to Source Voltage V GS (V)

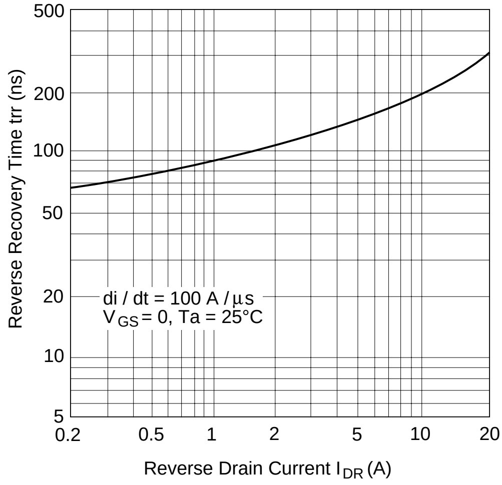

Drain-Source Saturation Voltage
vs. Gate-Source Voltage
Pulse Test
I D = 10 A
5 A
2 A
Drain to Source Saturation Voltage
V DS (on) (V)
Gate to Source Voltage V GS (V)
0
4
8
12
16
20
2
4
6
8
10


Static Drain-Source ON State
Resistance vs. Drain Current
Pulse Test
V GS = 10 V
15 V
Static Drain–Source On State
Resistance R DS (on) (Ω)
Drain Current I D (A)
0.2
0.5
1
2
5
10
20
0.05
0.1
0.2
0.5
1
2
5

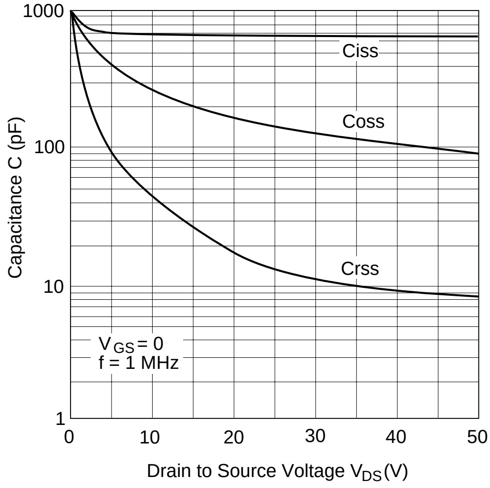

Static Drain-Source ON State
Resistance vs. Temperature
Pulse Test
V GS = 10 V
I D = 10 A
5 A
2 A
Static Drain–Source On State
Resistance R DS (on) (Ω)
Case Temperature Tc (°C)
– 40
0
40
80
120
160
0
0.4
0.8
1.2
1.6
2.0


Forward Transfer Admittance
vs. Drain Current
Pulse Test
V DS = 10 V
– 25°C
25°C
Tc = 75°C
Forward Transfer Admittance
|y fs| (S)
Drain Current I D (A)
0.1
0.2
0.5
1
2
5
10
0.5
1
2
5
10
20
50

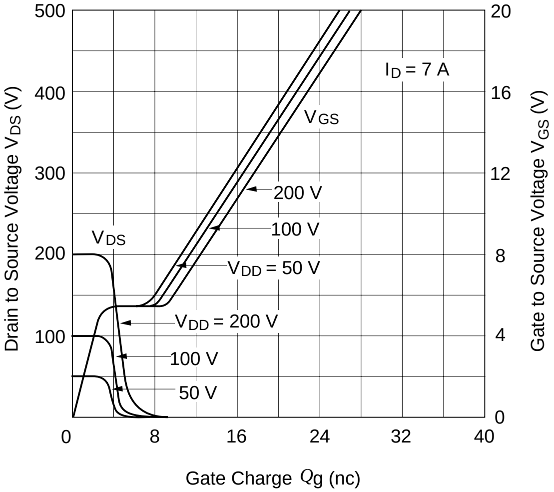
Body-Drain Diode Reverse Recovery Time



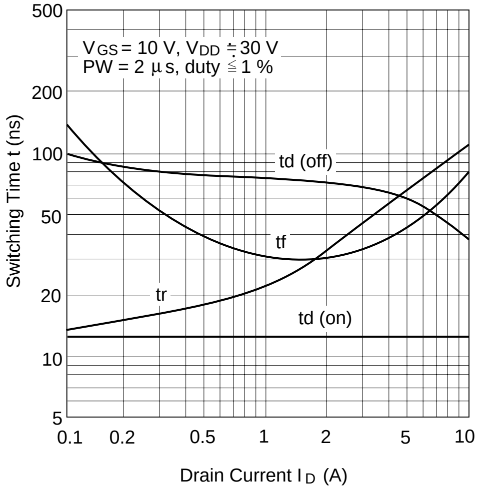
Typical Capacitance vs. Drain-Source Voltage

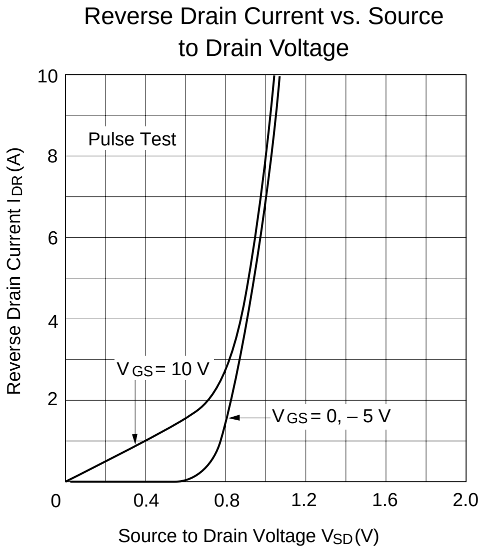


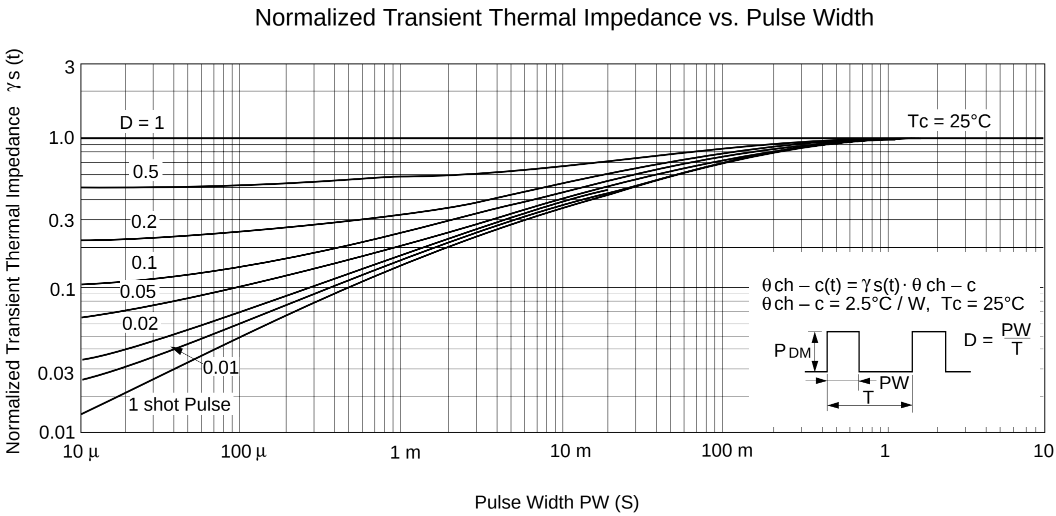
Dynamic Input Characteristics



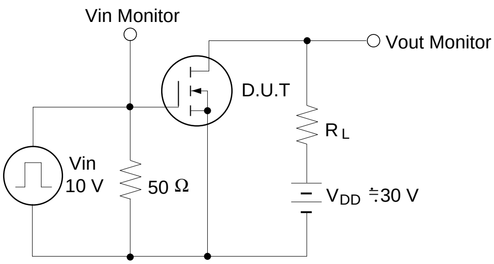
Switching Characteristics



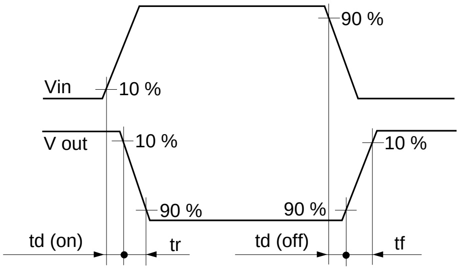

Reverse Drain Current vs. Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
10
8
6
4
2
0
Pulse Test
V_{GS} = 10 V
V_{GS} = 0, – 5 V
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
Tc = 25°C
$\theta ch-c(t) = \gamma s(t) \cdot \theta ch-c$
$\theta ch-c$ = 2.5°C / W, Tc = 25°C
P_{DM}
D = $\frac{PW}{T}$
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Switching Time Test Circuit



Waveforms



2SK1668

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC convertor

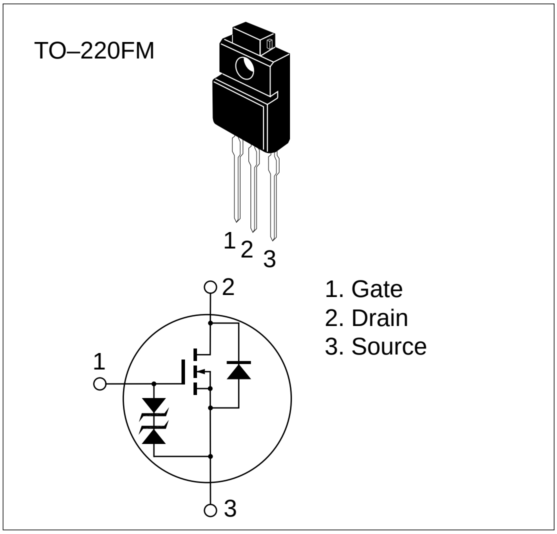


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}{}^*$	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

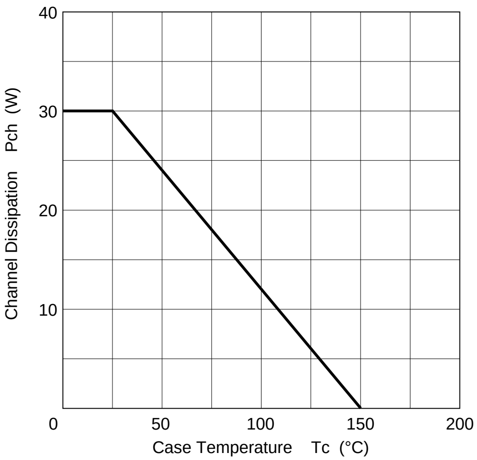
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.4	0.55	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	690	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	265	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	13	—	ns	I_D = 4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	37	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	180	—	ns	I_F = 7 A, V_{GS} = 0, di_F / dt = 100 A / µs

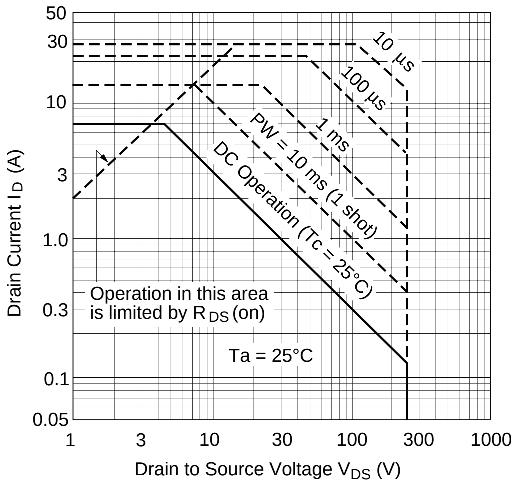
* Pulse Test

See characteristic curves of 2SK1667.

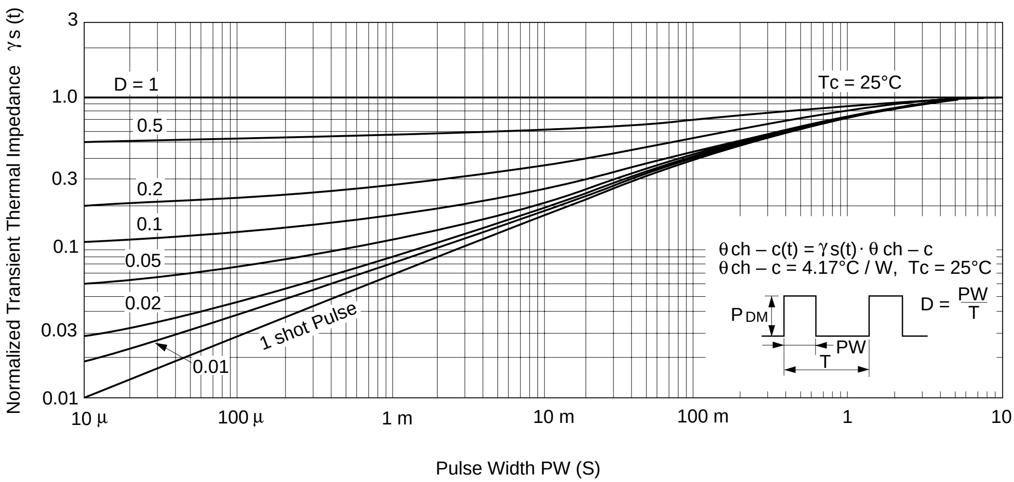
Power vs. Temperature Derating



Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width



2SK1697

Silicon N Channel MOS FET

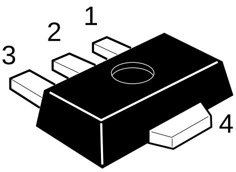
Application

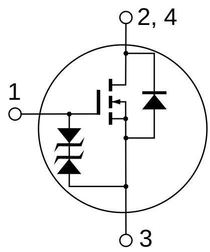
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source.
- Suitable for DC – DC converter, motor drive, power switch, solenoid drive

UPAK





1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.5	A
Drain peak current	$I_{D(pulse)}$*	1.5	A
Body–drain diode reverse drain current	I_{DR}	0.5	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

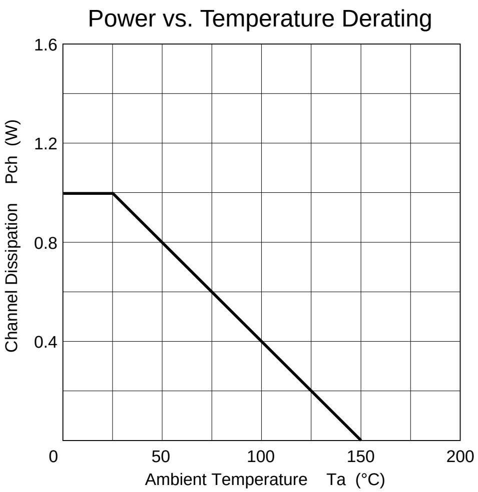
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the alumina ceramic board (12.5 × 20 × 0.7mm)
*** Marking is "EY".

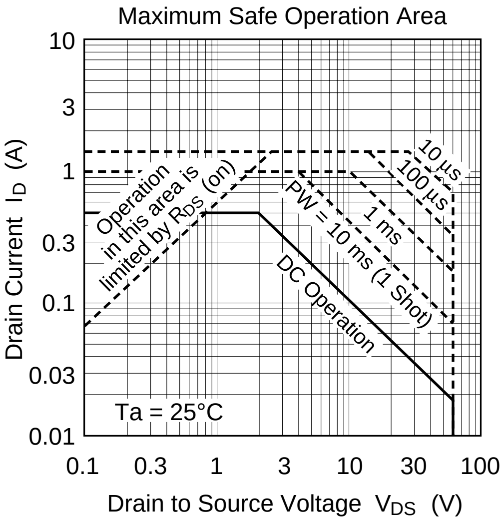
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	50	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.3	1.7	Ω	I_D = 0.3 A V_{GS} = 10 V *
		—	1.8	2.5	Ω	I_D = 0.3 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.25	0.38	—	S	I_D = 0.3 A V_{DS} = 10 V *
Input capacitance	Ciss	—	30	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	13	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	4	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	3	—	ns	I_D = 0.3 A
Rise time	t_r	—	8	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	18	—	ns	R_L = 100 Ω
Fall time	t_f	—	14	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1	—	V	I_F = 0.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F =0.5 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK1336.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
1.6
1.2
0.8
0.4
0
50
100
150
200
Ambient Temperature Ta (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
10
3
1
0.3
0.1
0.03
0.01
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V_{DS} (V)
Operation in this area is limited by R_{DS} (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation
Ta = 25°C

2SK1698

Silicon N Channel MOS FET

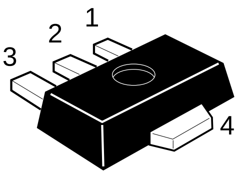
Application

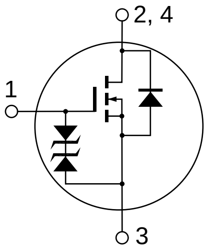
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source.
- Suitable for DC – DC converter, motor drive, power switch, solenoid drive

UPAK





1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.3	A
Drain peak current	$I_{D(pulse)}$*	1.2	A
Body–drain diode reverse drain current	I_{DR}	0.3	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

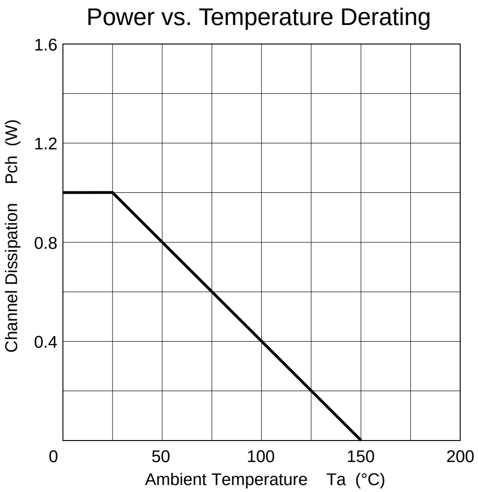
* PW ≤ 10 μs, duty cycle ≤ 1 %
** When using the alumina ceramic board (12.5 × 20 × 0.7mm)
*** Marking is "FY".

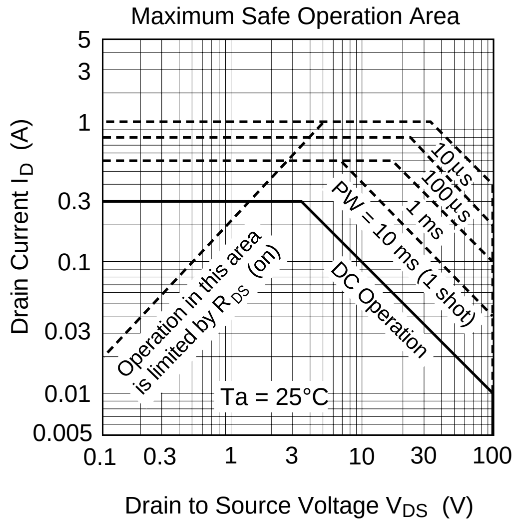
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	50	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	3.5	4.5	Ω	I_D = 0.2 A, V_{GS} = 10 V *
		—	4.5	6.5	Ω	I_D = 0.2 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.22	0.35	—	S	I_D = 0.2 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	35	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	14	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3.5	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	2	—	ns	I_D = 0.2 A
Rise time	t_r	—	4	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	17	—	ns	R_L = 150 Ω
Fall time	t_f	—	15	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 0.3 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	80	—	ns	I_F =0.5 A, V_{GS} = 0, di_F/dt = 50 A/µs

* Pulse Test

See characteristic curves of 2SK1337.


Power vs. Temperature Derating
1.6
1.2
0.8
0.4
0
50
100
150
200
Channel Dissipation Pch (W)
Ambient Temperature Ta (°C)


Maximum Safe Operation Area
5
3
1
0.3
0.1
0.03
0.01
0.005
0.1
0.3
1
3
10
30
100
Drain Current I_D (A)
Drain to Source Voltage V_DS (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation
Operation in this area
is limited by R_DS (on)
Ta = 25°C

2SK1761

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

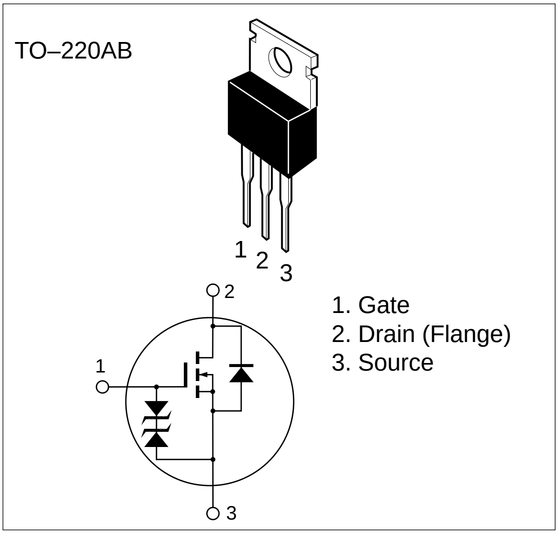


Table 1 Absolute Maximum Ratings (Ta = 25°C)

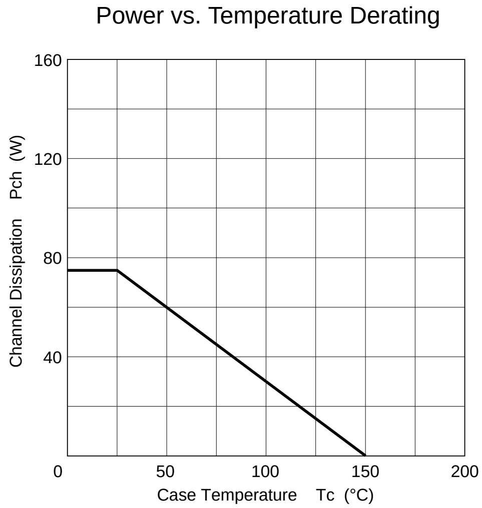
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	12	A
Drain peak current	$I_{D(pulse)}$*	48	A
Body–drain diode reverse drain current	I_{DR}	12	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

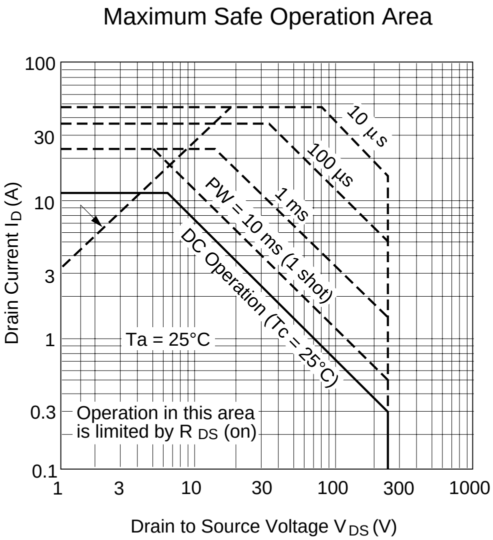
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

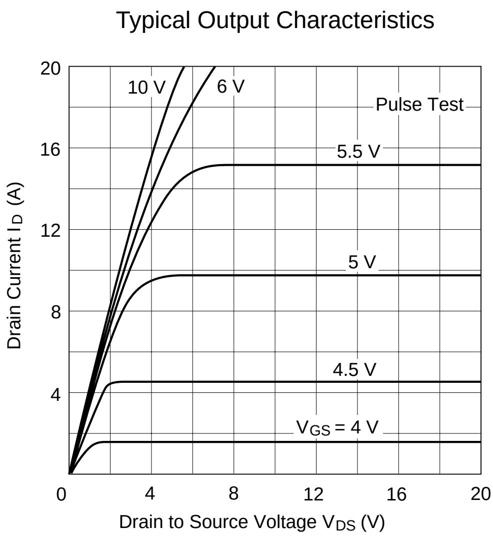
Table 2 Electrical Characteristics (Ta = 25°C)

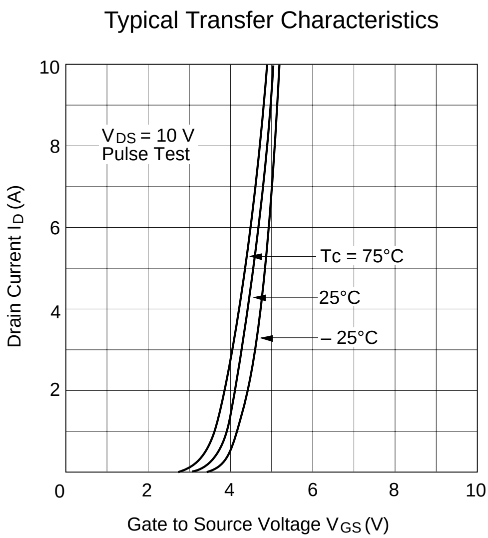
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.23	0.35	Ω	I_D = 6 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	8.0	—	S	I_D = 6 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1100	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	68	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 6 A
Rise time	t_r	—	65	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 5 Ω
Fall time	t_f	—	44	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 12 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = 12 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

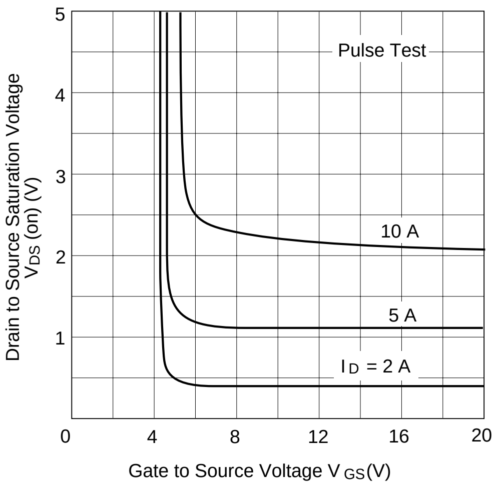

Power vs. Temperature Derating
160
120
80
40
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
100
30
10
3
1
0.3
0.1
1
3
10
30
100
300
1000
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25°C
Operation in this area
is limited by R DS (on)
Drain Current I D (A)
Drain to Source Voltage V DS (V)

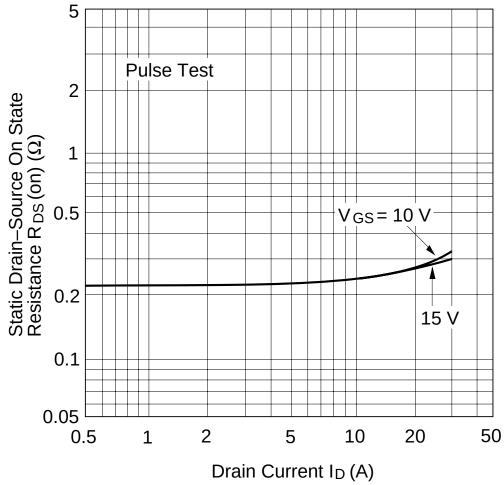

Typical Output Characteristics
20
16
12
8
4
0
4
8
12
16
20
10 V
6 V
Pulse Test
5.5 V
5 V
4.5 V
VGS = 4 V
Drain Current I D (A)
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
10
8
6
4
2
0
2
4
6
8
10
VDS = 10 V
Pulse Test
Tc = 75°C
25°C
– 25°C
Drain Current I D (A)
Gate to Source Voltage VGS (V)

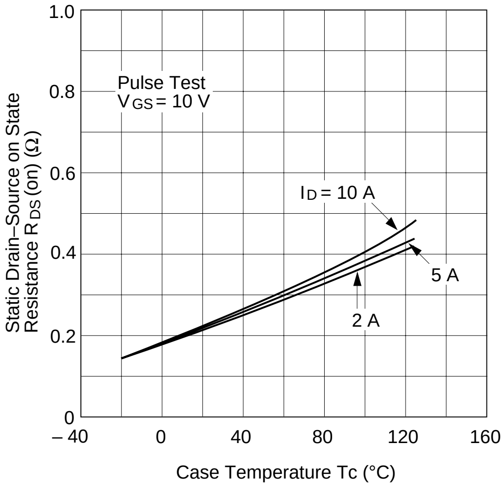
Drain-Source Saturation Voltage vs. Gate-Source Voltage



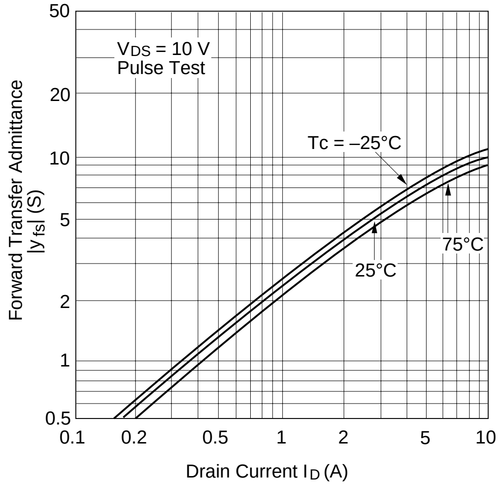
Static Drain-Source on State Resistance vs. Drain Current



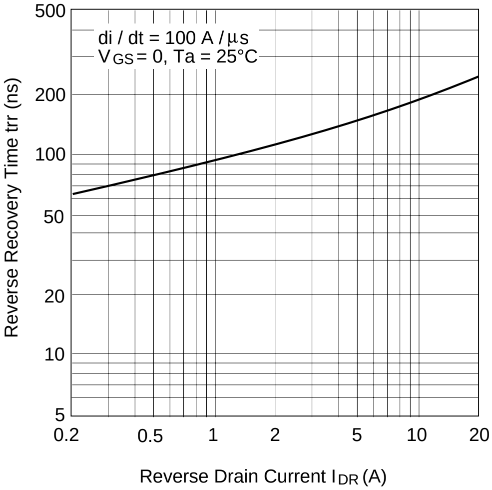
Static Drain-Sourve on State Resistance vs. Temperature



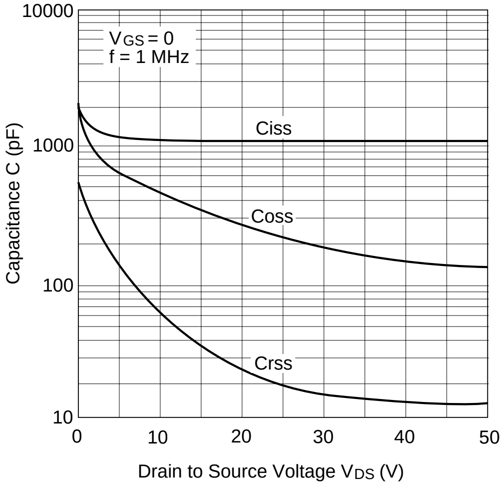
Forward Transfer Admittance vs. Drain Current



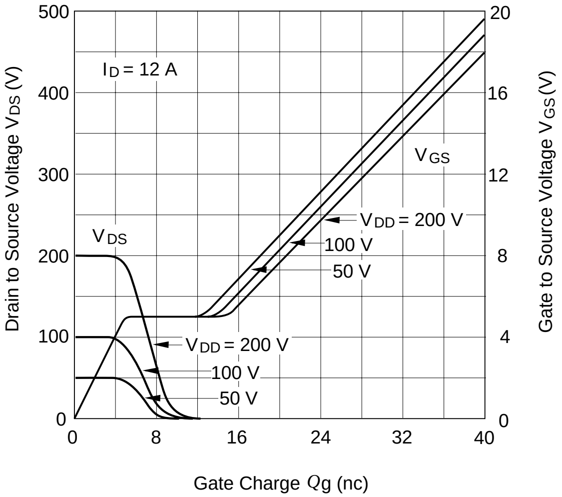
Body-Drain Diode Reverse Recovery Time



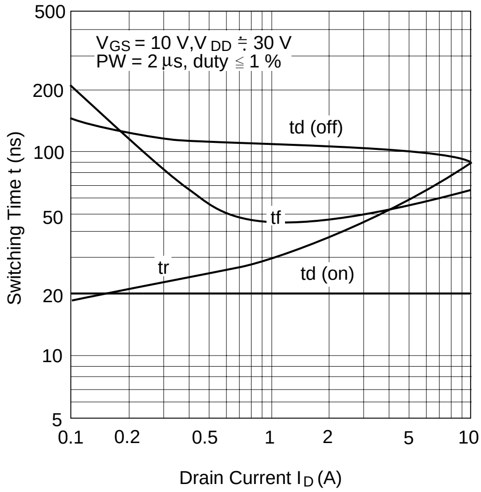
Typical Capacitance vs. Drain-Source Voltage



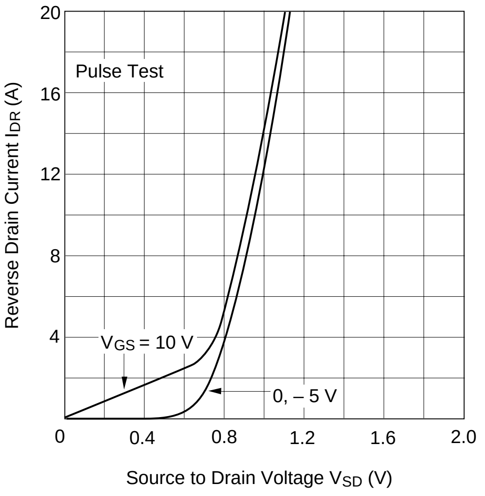
Dynamic Input Characteristics



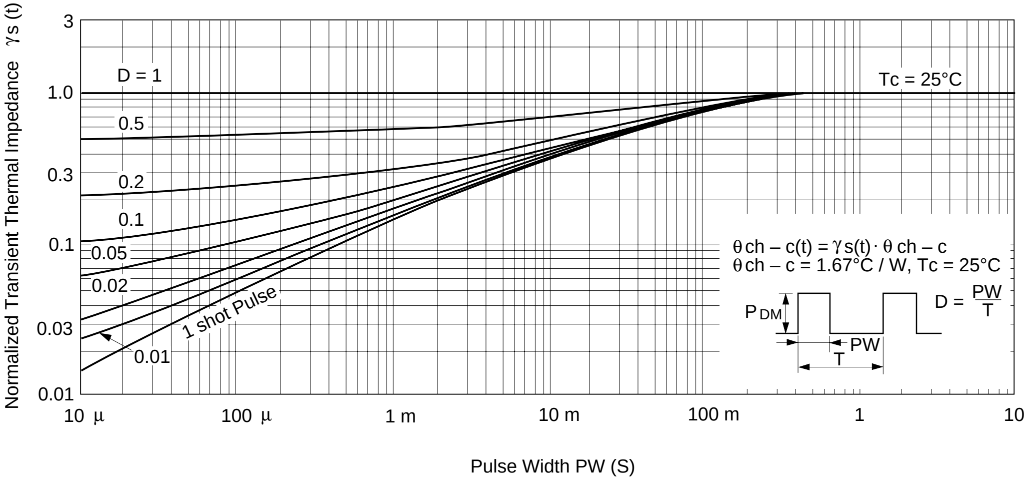
Switching Characteristics



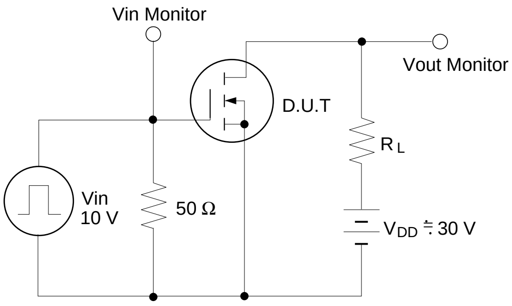
Reverse Drain Current vs. Source to Drain Voltage



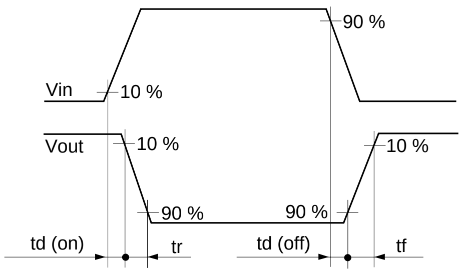
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveforms



2SK1762

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

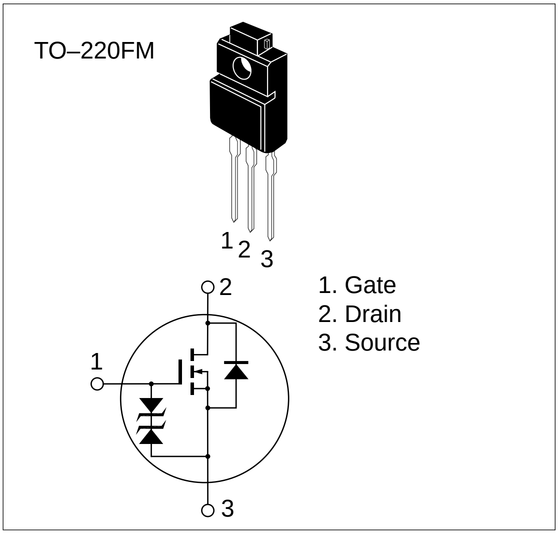


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	12	A
Drain peak current	$I_{D(pulse)}$*	48	A
Body–drain diode reverse drain current	I_{DR}	12	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

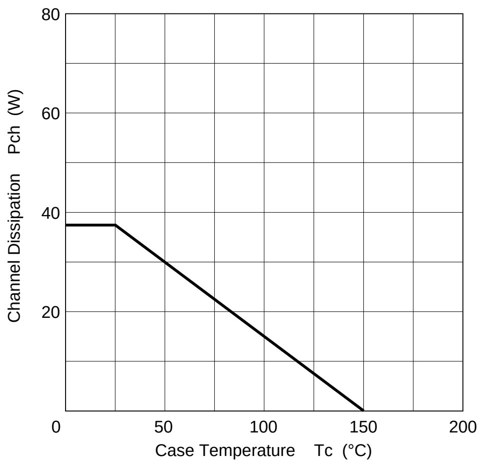
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.23	0.35	Ω	I_D = 6 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	8.0	—	S	I_D = 6 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1100	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	68	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 6 A
Rise time	t_r	—	65	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 5 Ω
Fall time	t_f	—	44	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 12 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = 12 A, V_{GS} = 0, di_F / dt = 100 A / µs

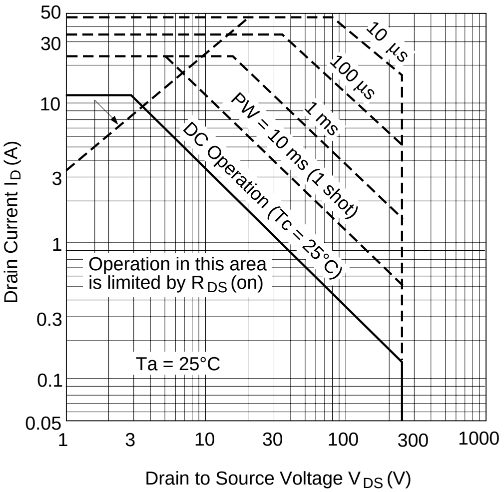
* Pulse Test

See characteristic curves of 2SK1761.

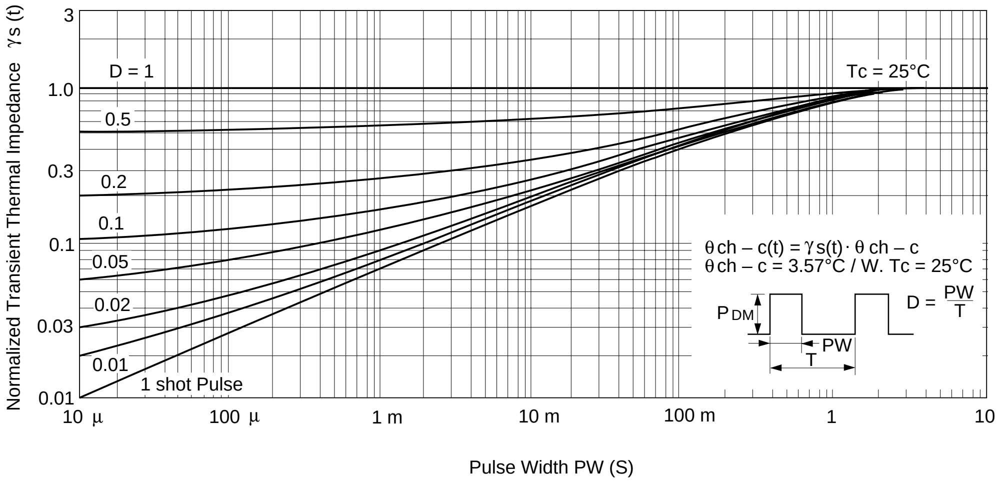
Power vs. Temperature Derating



Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width



2SK1764

Silicon N Channel MOS FET

Application

Low frequency amplifier
High speed switching

Features

- Low on–resistance
- High speed switching
- 4 V Gate drive device can be driven from 5 V source
- Suitable for switchingregulator, DC–DC converter

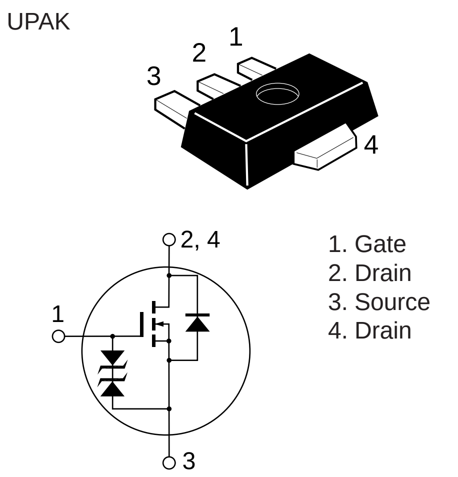


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	±2	A
Drain peak current	$I_{D(pulse)}$*	±4	A
Channel power dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

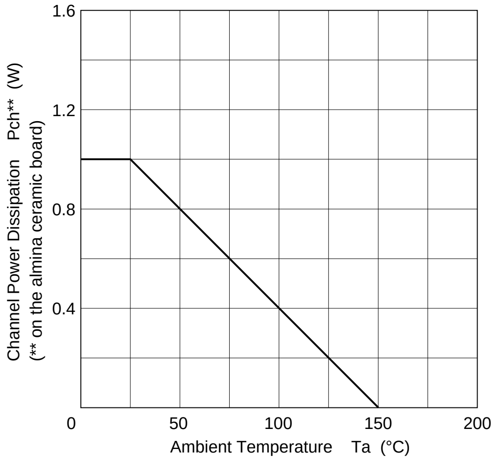
* PW ≤ 100 µs, duty cycle ≤ 10 %
** Value on the alumina ceramic board (12.5 x 20 x 0.7 mm)
*** Marking is "KY".

Table 2 Electrical Characteristics (Ta = 25°C)

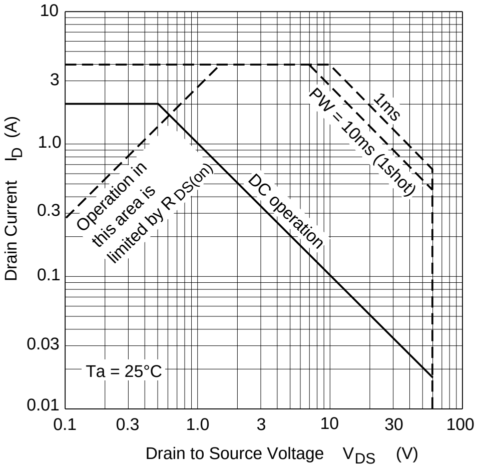
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1	—	2	V	V_{DS} = 10 V, I_D = 1 mA
Drain to source cutoff current	I_{DSS}	—	—	10	μA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff current	I_{GSS}	—	—	±5	μA	V_{GS} = ±15 V, V_{DS} = 0
Static drain to source on state resistance	$R_{DS(on)1}$	—	0.3	0.45	Ω	V_{GS} = 10 V I_D = 1 A*
Static drain to source on state resistance	$R_{DS(on)2}$	—	0.4	0.60	Ω	V_{GS} = 4 V I_D = 1 A*
Forward transfer admittance	$\|y_{fs}\|$	0.9	1.7	—	S	V_{DS} = 10 V I_D = 1 A*
Input capacitance	Ciss	—	140	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	75	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	20	—	pF	f = 1 MHz
Turn on time	ton	—	18	—	ns	V_{DS} = 10 V, I_D = 1 A*
Turn off time	toff	—	80	—	ns	R_L = 30 Ω

* Pulse Test

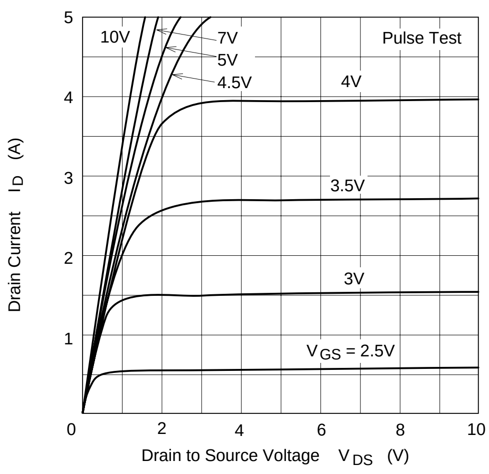
Maximum Channel Power Dissipation Curve



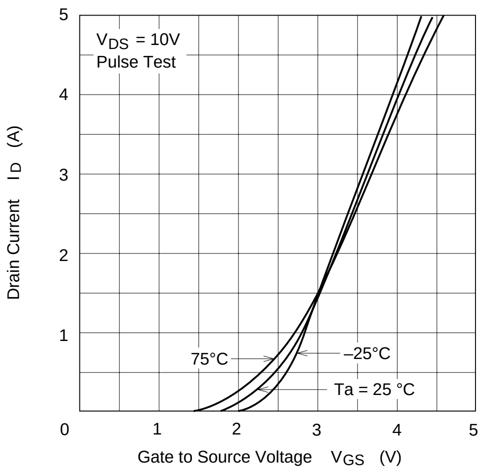
Safe Operation Area



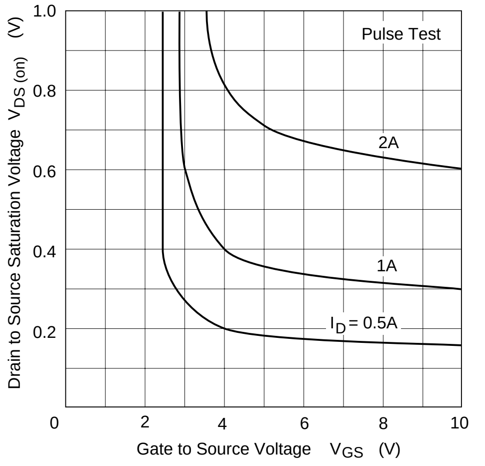
Typical Output Characteristics



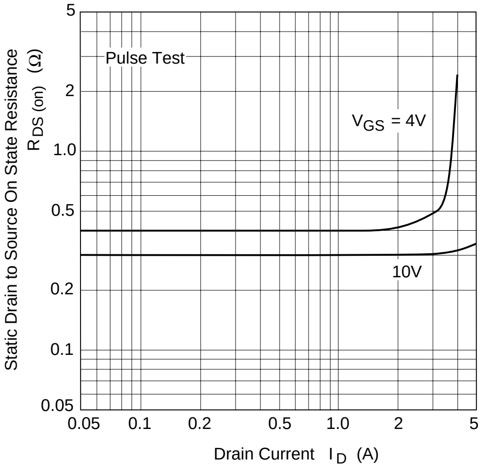
Typical Transfer Characteristics



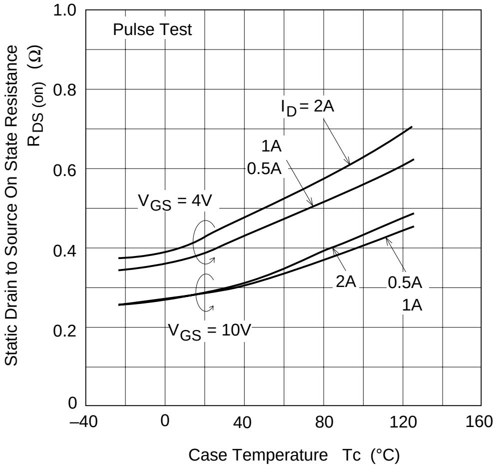
Drain to Source Saturation Voltage vs. Gate to Source Voltage



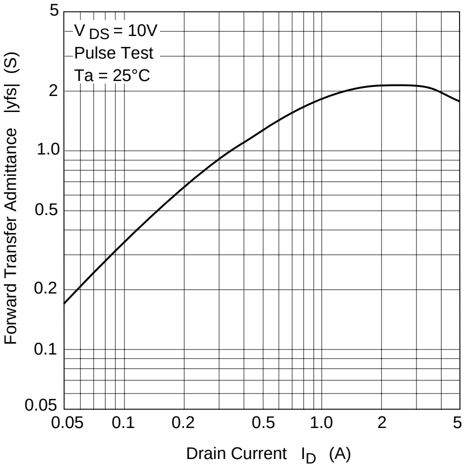
Static Drain to Source On State Resistance vs. Drain Current



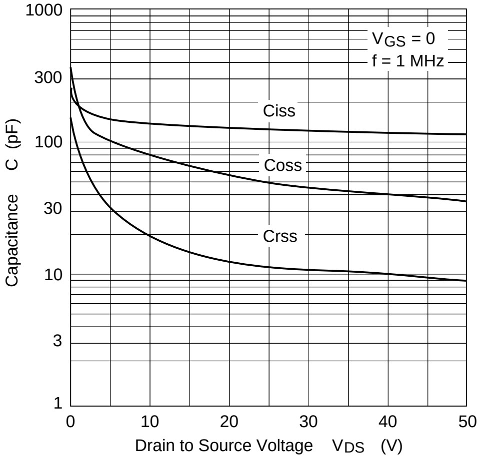
Static Drain to Source On State Resistance vs. Case Temperature



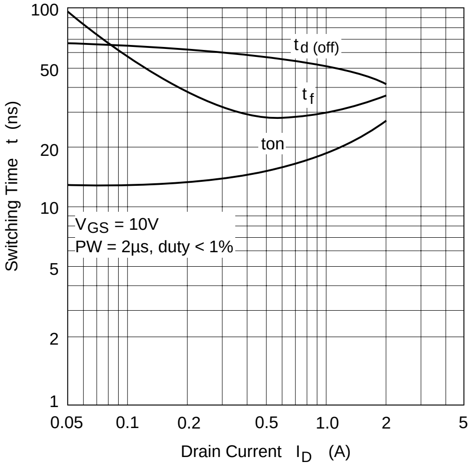
Forward Transfer Admittance vs. Drain Current



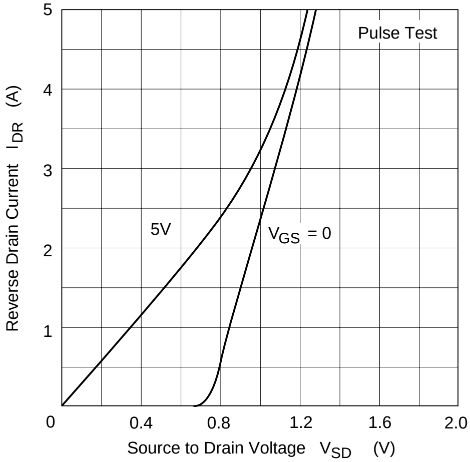
Typical Capacitance vs. Drain to Source Voltage



Switching Time vs. Drain Current



Reverse Drain Current vs. Source to Drain Voltage



2SK1772

Silicon N Channel MOS FET

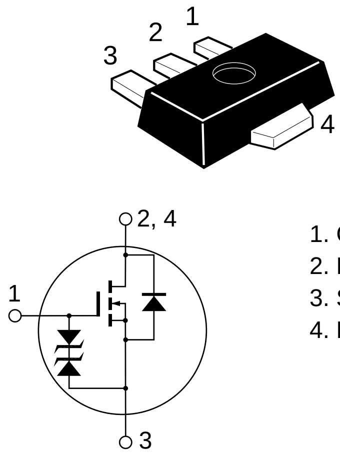
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source.
- Suitable for DC – DC converter, motor drive, power switch, solenoid drive

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

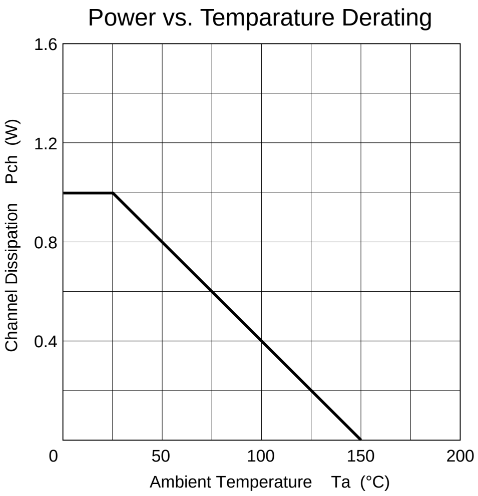
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	1	A
Drain peak current	$I_{D(pulse)}$*	2	A
Body–drain diode reverse drain current	I_{DR}	1	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

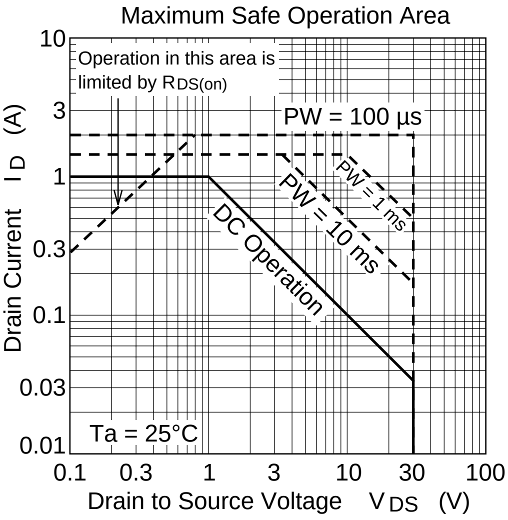
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the alumina ceramic board (12.5 × 20 × 0.7mm)
*** Marking is "HY".

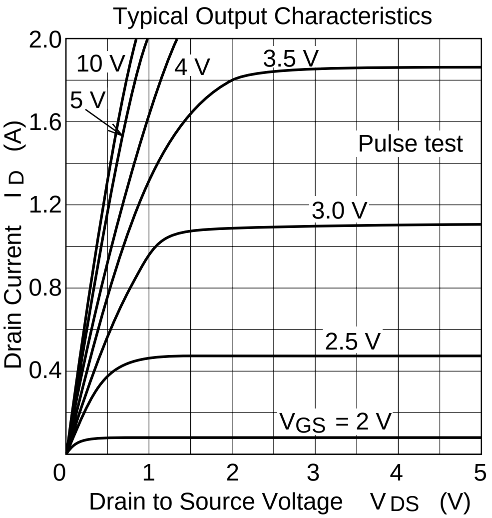
Table 2 Electrical Characteristics (Ta = 25°C)

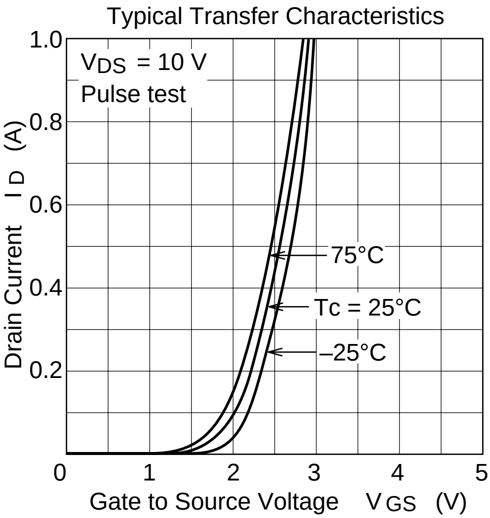
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	50	µA	V_{DS} = 25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.4	0.6	Ω	I_D = 0.5 A V_{GS} = 10 V *
		—	0.6	0.85	Ω	I_D = 0.5 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.6	1.0	—	S	I_D = 0.5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	85	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	65	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	20	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 0.5 A
Rise time	t_r	—	15	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	40	—	ns	R_L = 60 Ω
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 1 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	30	—	ns	I_F = 1 A, V_{GS} = 0, di_F/dt = 50 A/µs

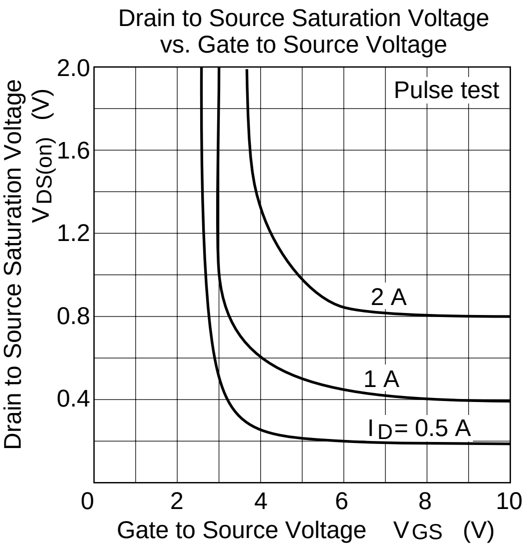
* Pulse Test

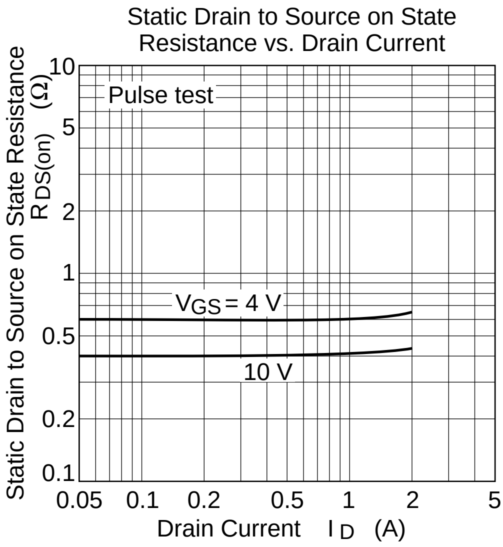

Power vs. Temparature Derating
Channel Dissipation Pch (W)
1.6
1.2
0.8
0.4
0
50
100
150
200
Ambient Temperature Ta (°C)

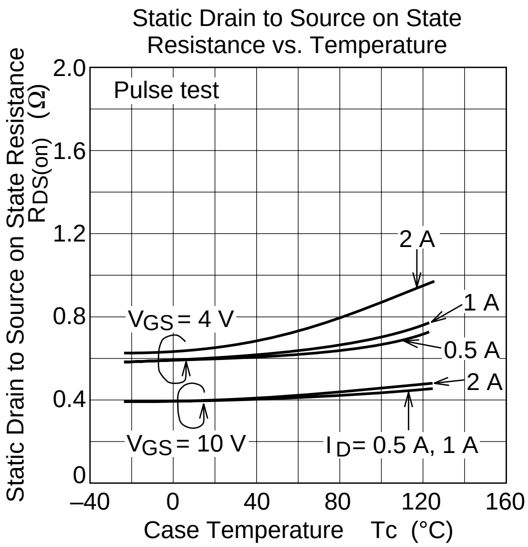

Maximum Safe Operation Area
Operation in this area is limited by RDS(on)
PW = 100 µs
PW = 1 ms
PW = 10 ms
DC Operation
Ta = 25°C
Drain Current I D (A)
10
3
1
0.3
0.1
0.03
0.01
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

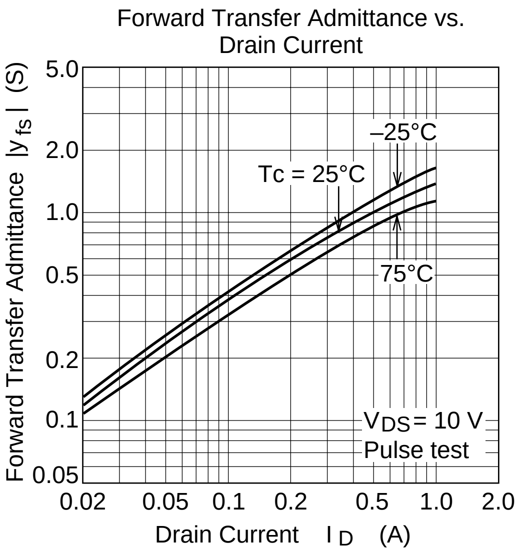

Typical Output Characteristics
10 V
4 V
3.5 V
5 V
Pulse test
3.0 V
2.5 V
VGS = 2 V
Drain Current I D (A)
2.0
1.6
1.2
0.8
0.4
0
1
2
3
4
5
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
VDS = 10 V
Pulse test
75°C
Tc = 25°C
–25°C
Drain Current I D (A)
1.0
0.8
0.6
0.4
0.2
0
1
2
3
4
5
Gate to Source Voltage V GS (V)

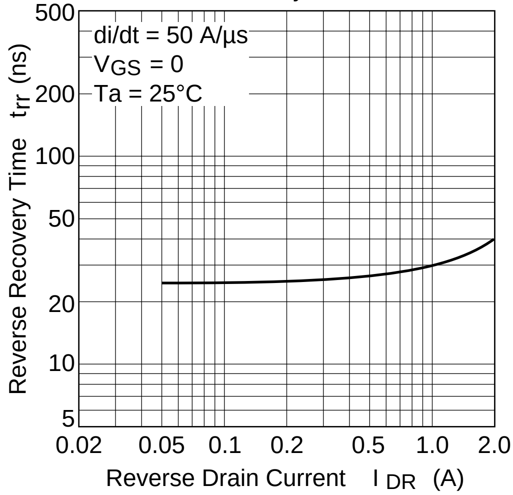

Drain to Source Saturation Voltage vs. Gate to Source Voltage
Drain to Source Saturation Voltage VDS(on) (V)
2.0
1.6
1.2
0.8
0.4
Pulse test
2 A
1 A
ID = 0.5 A
0
2
4
6
8
10
Gate to Source Voltage VGS (V)


Static Drain to Source on State Resistance vs. Drain Current
Static Drain to Source on State Resistance RDS(on) (Ω)
10
5
2
1
0.5
0.2
0.1
Pulse test
VGS = 4 V
10 V
0.05
0.1
0.2
0.5
1
2
5
Drain Current ID (A)

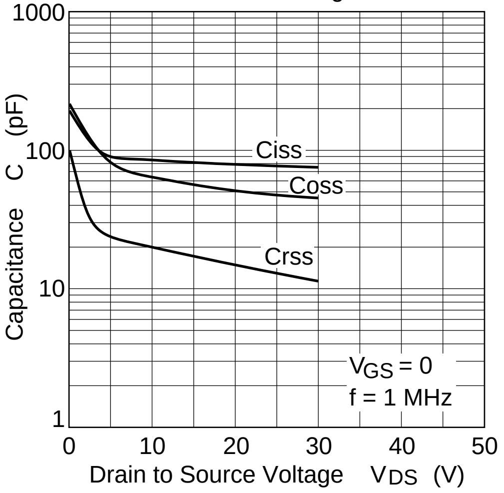

Static Drain to Source on State Resistance vs. Temperature
Static Drain to Source on State Resistance RDS(on) (Ω)
2.0
1.6
1.2
0.8
0.4
0
Pulse test
2 A
1 A
0.5 A
2 A
VGS = 4 V
VGS = 10 V
ID = 0.5 A, 1 A
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs. Drain Current
Forward Transfer Admittance |yfs| (S)
5.0
2.0
1.0
0.5
0.2
0.1
0.05
–25°C
Tc = 25°C
75°C
VDS = 10 V
Pulse test
0.02
0.05
0.1
0.2
0.5
1.0
2.0
Drain Current ID (A)

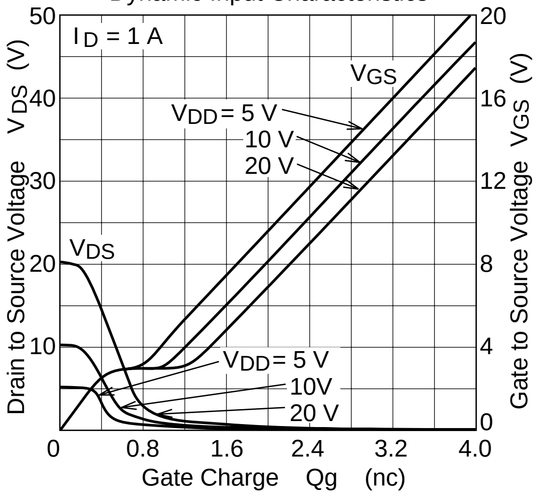
Body-Drain Diode Reverse Recovery Time



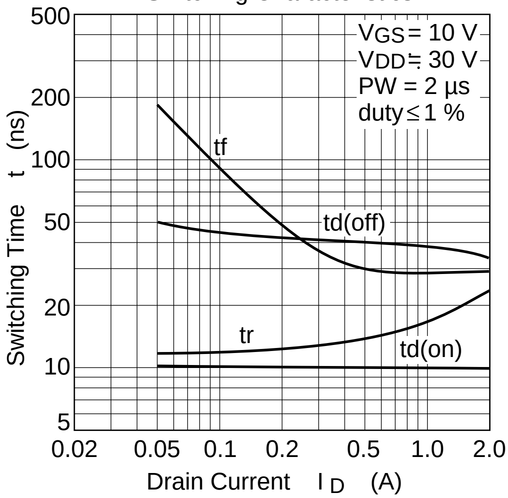
Typical Capacitance vs. Drain to Source Voltage

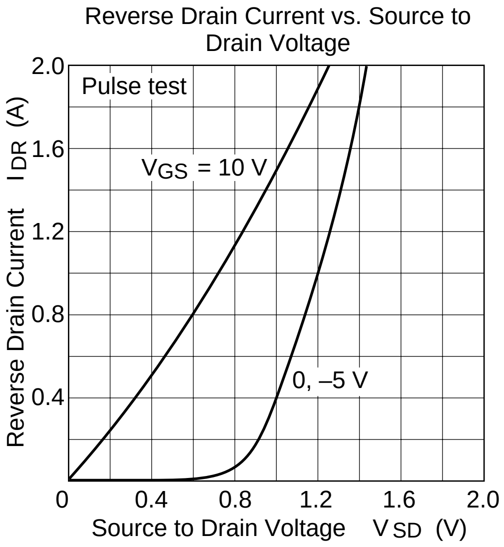


Dynamic Input Characteristics



Switching Characteristics




Reverse Drain Current vs. Source to Drain Voltage
Pulse test
VGS = 10 V
0, –5 V
Reverse Drain Current I DR (A)
2.0
1.6
1.2
0.8
0.4
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V SD (V)

2SK1773

Silicon N Channel MOS FET

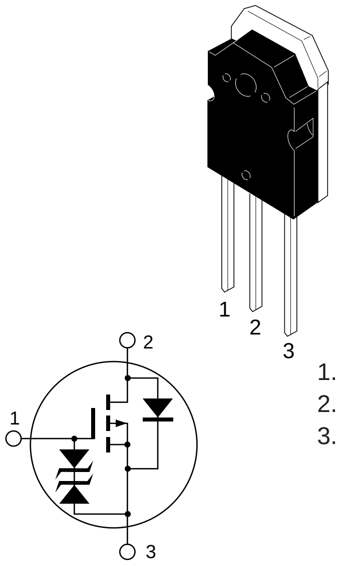
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

TO–3P



1. Gate
2. Drain (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

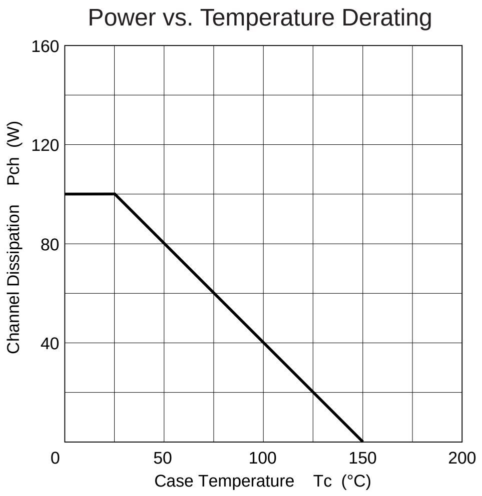
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1000	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	15	A
Body–drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

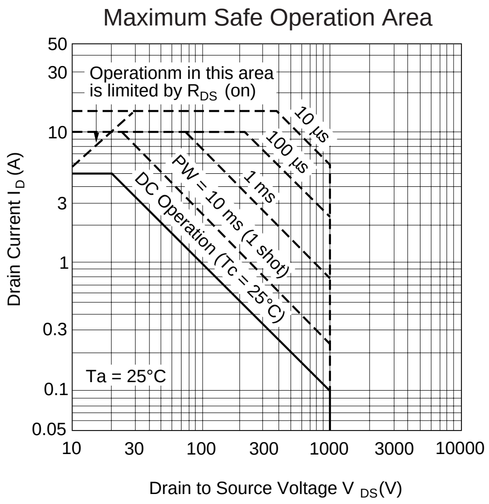
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

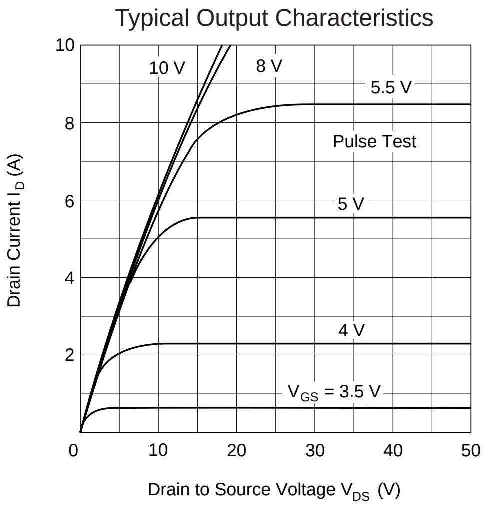
Table 2 Electrical Characteristics (Ta = 25°C)

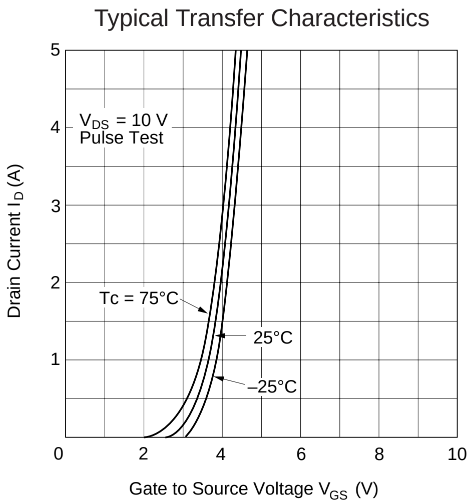
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1000	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 800 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.5	2.0	Ω	I_D = 3 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.2	5.0	—	S	I_D = 3 A V_{DS} = 20 V *
Input capacitance	Ciss	—	1700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	700	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	315	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	I_D = 3 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	210	—	ns	R_L = 10 Ω
Fall time	t_f	—	135	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.85	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	1050	—	ns	I_F = 5 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

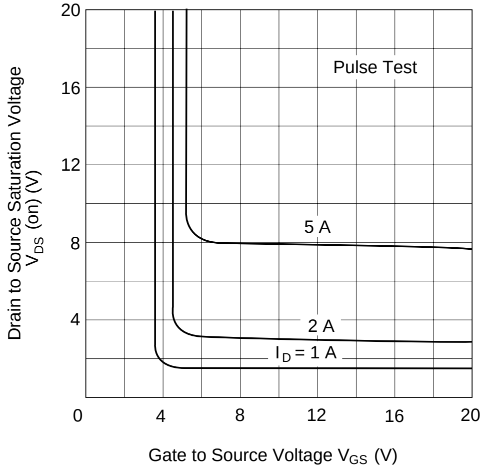

Power vs. Temperature Derating
160
120
80
40
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
Operationm in this area
is limited by R_{DS} (on)
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25°C
50
30
10
3
1
0.3
0.1
0.05
10
30
100
300
1000
3000
10000
Drain Current I_D (A)
Drain to Source Voltage V_{DS}(V)

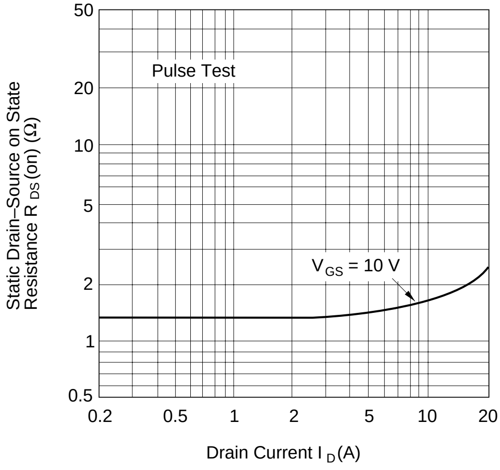

Typical Output Characteristics
10 V
8 V
5.5 V
Pulse Test
5 V
4 V
V_{GS} = 3.5 V
10
8
6
4
2
0
10
20
30
40
50
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
V_{DS} = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
5
4
3
2
1
0
2
4
6
8
10
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

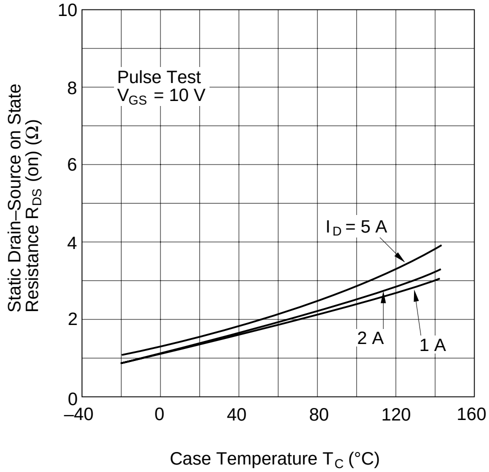
Drain-Source Saturation Voltage vs. Gate-Source Voltage



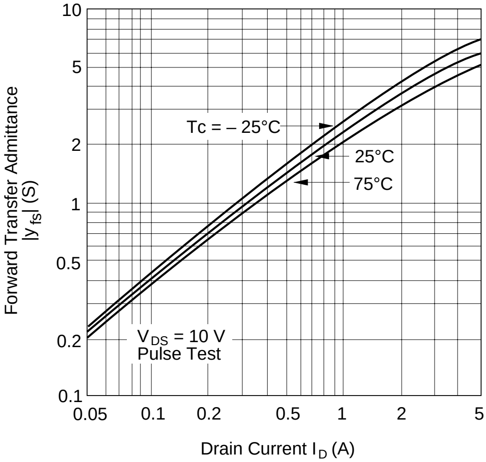
Static Drain-Source on State Resistance vs. Current



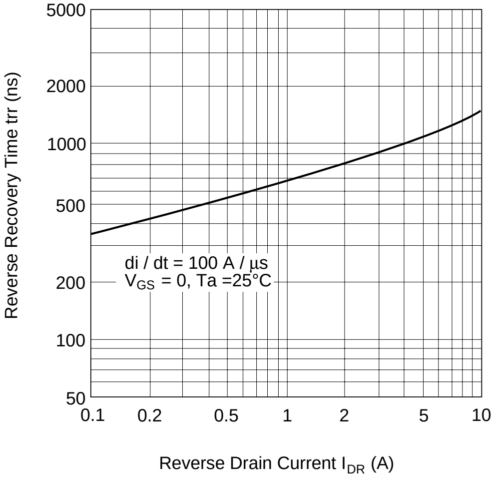
Static Drain-Source on State Resistance vs. Temperature



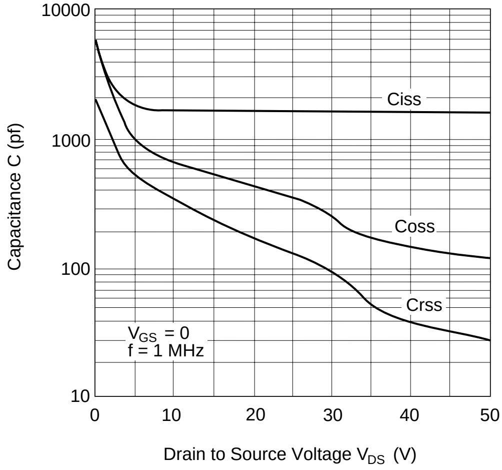
Forward Transfer Admittance vs. Drain Current



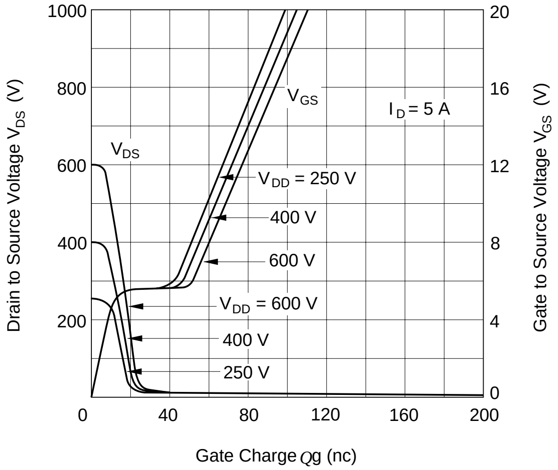
Body-Drain Diode Reverse Recovery Time



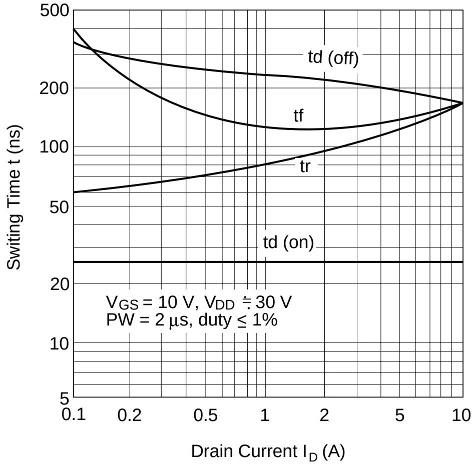
Typical Capacitance vs. Drain-Source Voltage

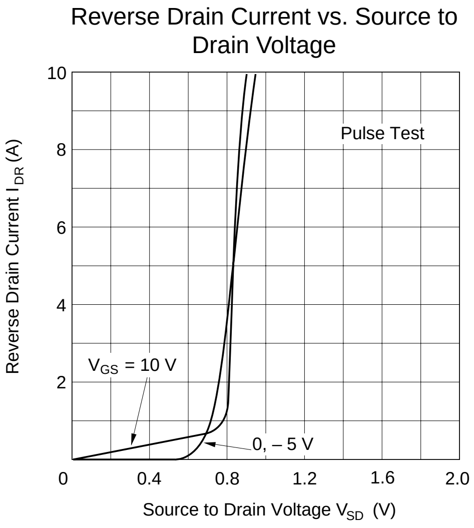


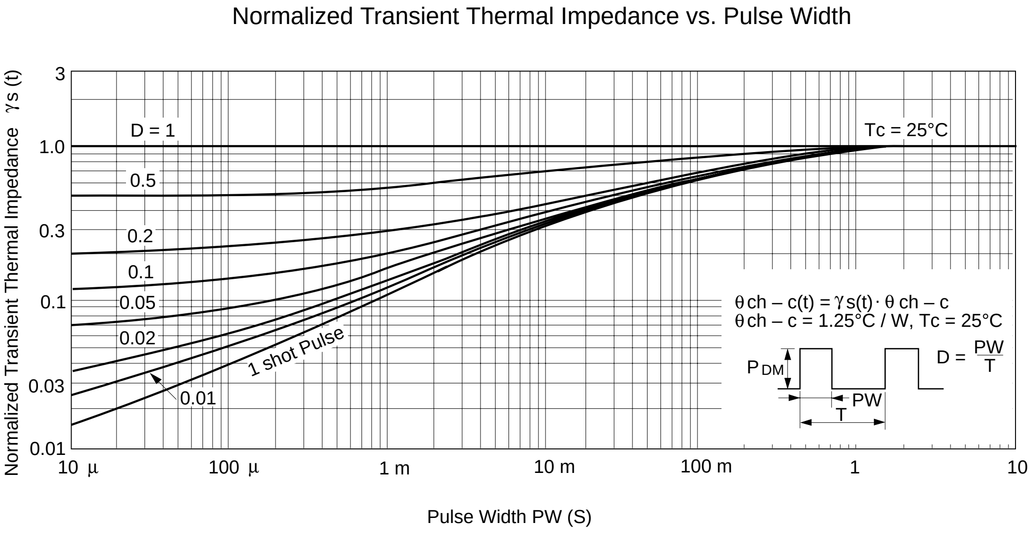
Dynamic Input Characteristics



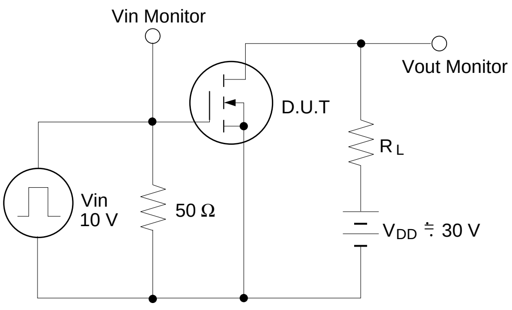
Switching Characteristics



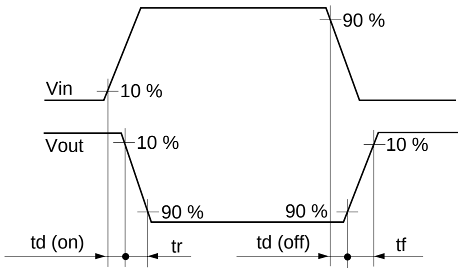

Reverse Drain Current vs. Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
0, – 5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
2
4
6
8
10


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
Tc = 25°C
θ ch – c(t) = γ s(t) · θ ch – c
θ ch – c = 1.25°C / W, Tc = 25°C
P DM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
10 μ
100 μ
1 m
10 m
100 m
1
10
0.01
0.03
0.1
0.3
1.0
3

Switching Time Test Circuit



Waveforms



2SK1775

Silicon N Channel MOS FET

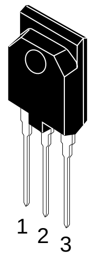
Application

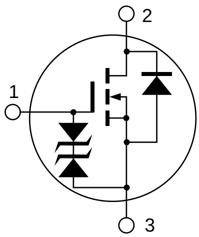
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

TO–3PFM





1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	900	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}^{*}$	20	A
Body–drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

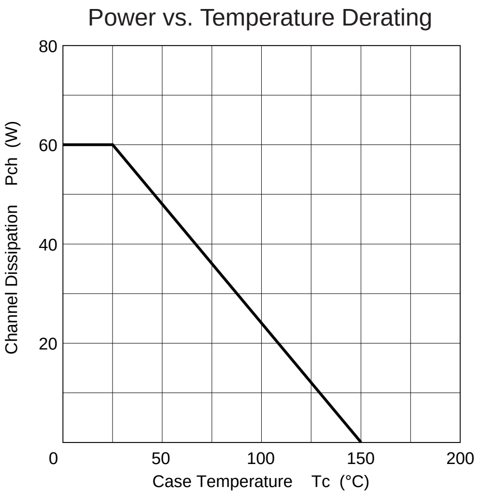
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

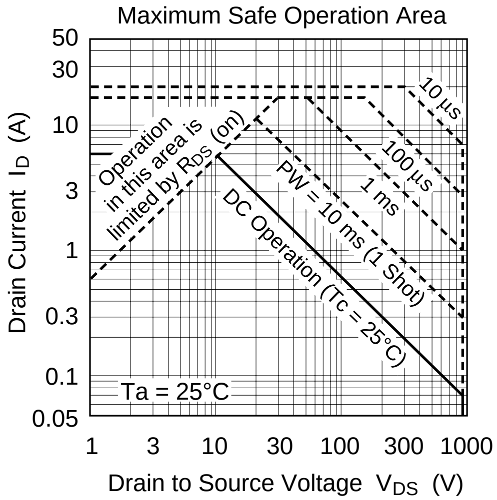
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	900	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 720 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.2	1.6	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	5.5	—	S	I_D = 4 A V_{DS} = 20 V *
Input capacitance	Ciss	—	1730	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	700	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	310	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	I_D = 4 A
Rise time	t_r	—	135	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	185	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	130	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	900	—	ns	I_F = 8 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1342





Normalized Transient Thermal Impedance vs. Pulse Width

2SK1807

Silicon N Channel MOS FET

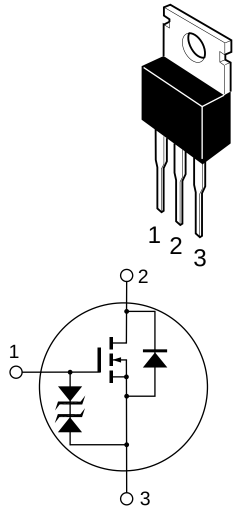
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

TO-220AB



1. Gate
2. Drain (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	900	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$*	10	A
Body–drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

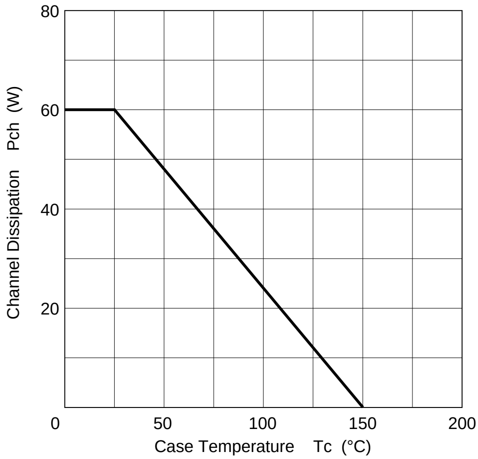
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	900	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	V_{DS} = 720 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	3.0	4.0	Ω	I_D = 2 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.7	2.7	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	740	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	305	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	150	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 2 A
Rise time	t_r	—	60	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 15 Ω
Fall time	t_f	—	80	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	800	—	ns	I_F = 4 A, V_{GS} = 0, di_F / dt = 100 A / μs

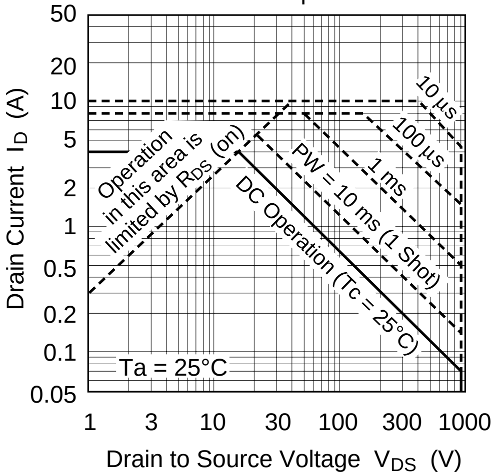
* Pulse Test

See characteristic curves of 2SK1340

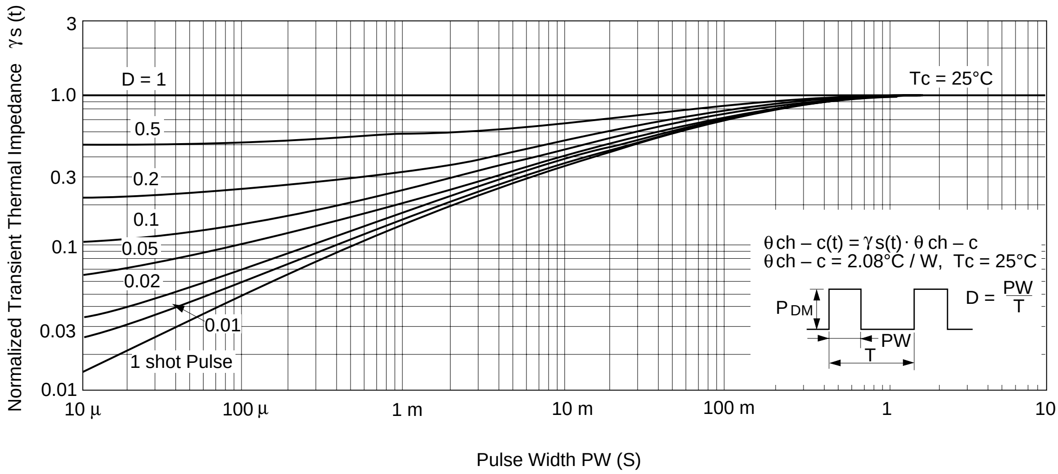
Power vs. Temperature Derating



Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width



2SK1808

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

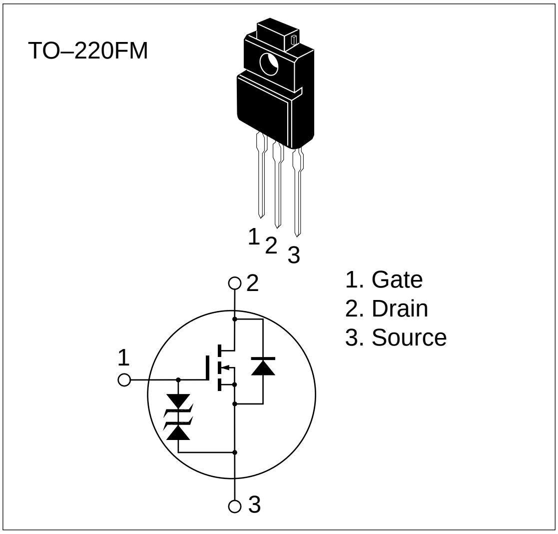


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	900	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$*	10	A
Body–drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

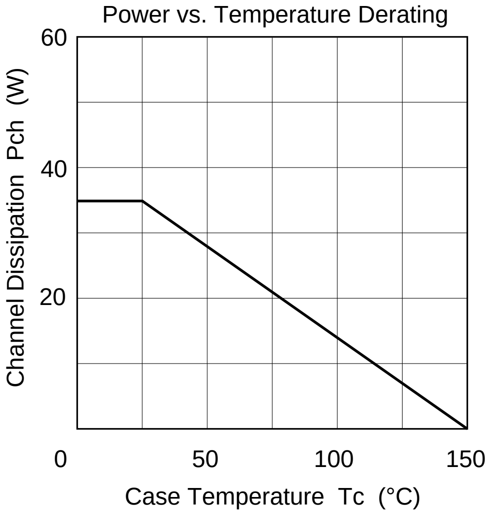
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

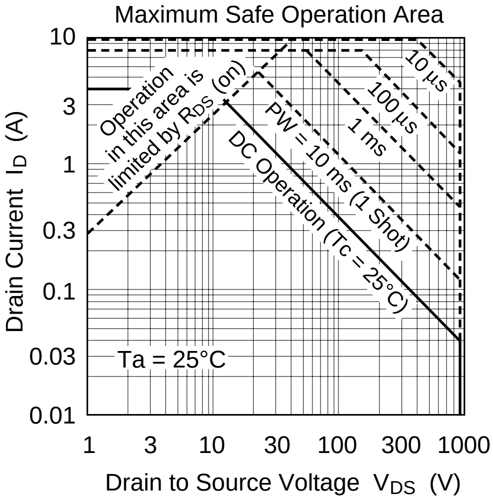
Table 2 Electrical Characteristics (Ta = 25°C)

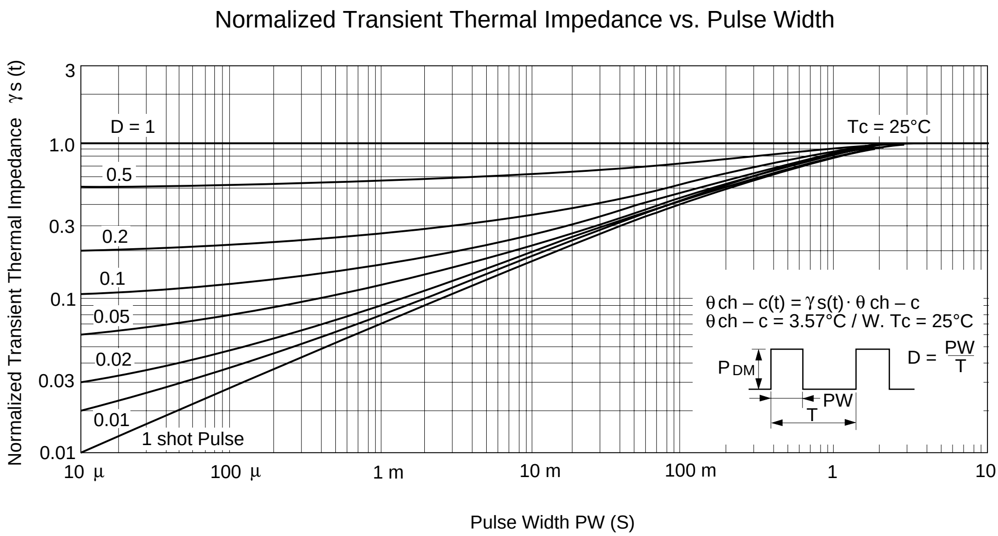
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	900	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 720 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	3.0	4.0	Ω	I_D = 2 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.7	2.7	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	740	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	305	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	150	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 2 A
Rise time	t_r	—	60	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 15 Ω
Fall time	t_f	—	80	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	800	—	ns	I_F = 4 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1340


Power vs. Temperature Derating
Channel Dissipation Pch (W)
Case Temperature Tc (°C)
0
20
40
60
50
100
150


Maximum Safe Operation Area
Operation in this area is limited by RDS (on)
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C
Drain Current ID (A)
Drain to Source Voltage VDS (V)
10
3
1
0.3
0.1
0.03
0.01
1
3
10
30
100
300
1000


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
Tc = 25°C
θch – c(t) = γs(t) · θch – c
θch – c = 3.57°C / W. Tc = 25°C
PDM
D = PW/T
PW
T
3
1.0
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

2SK1809

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

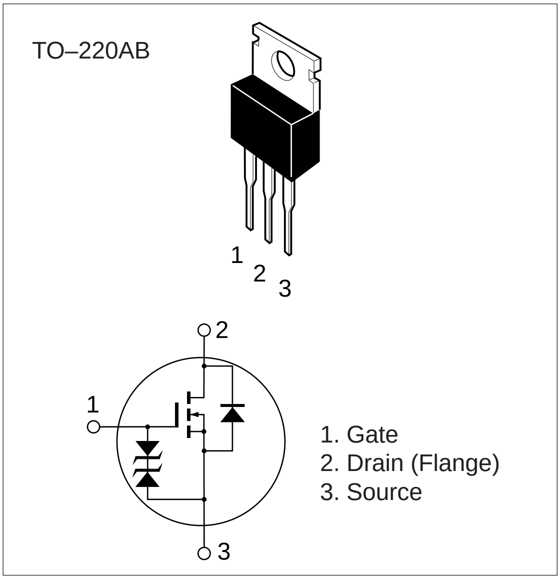


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	20	A
Body–drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

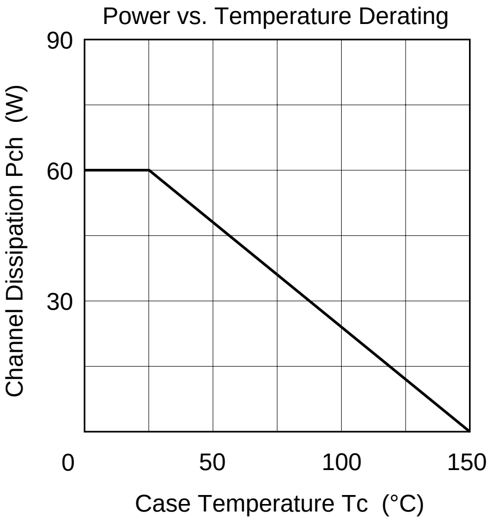
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

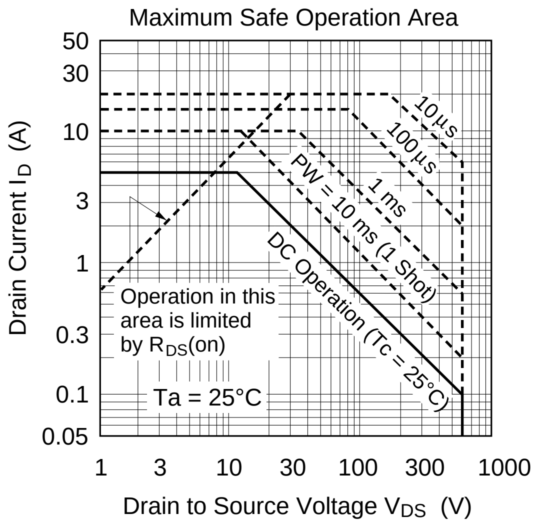
Table 2 Electrical Characteristics (Ta = 25°C)

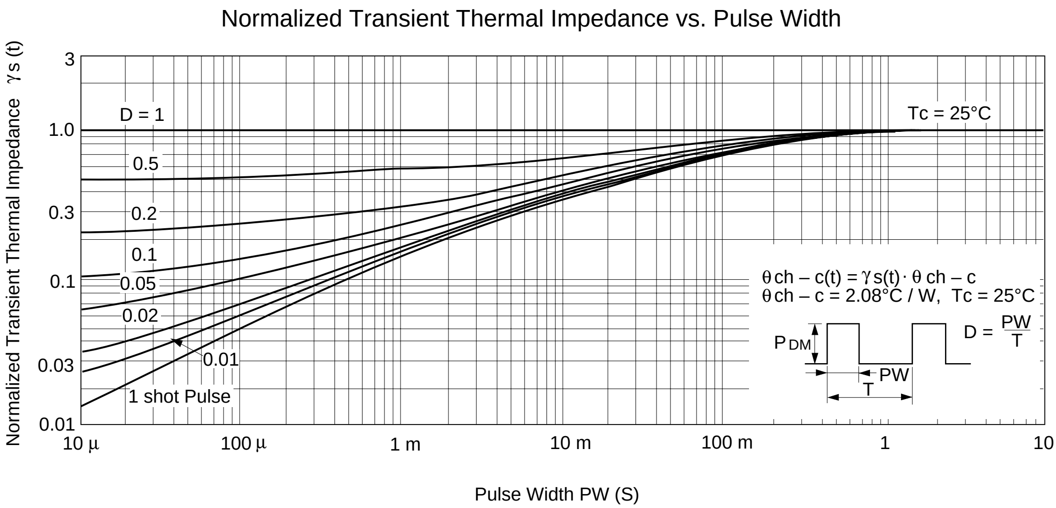
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	V_{DS} = 500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.5	Ω	I_D = 2.5A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 2.5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1000	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	250	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	12	—	ns	I_D = 2.5 A
Rise time	t_r	—	45	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	105	—	ns	R_L = 12 Ω
Fall time	t_f	—	55	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	500	—	ns	I_F = 5 A, V_{GS} = 0, di_F / dt = 100 A / μs

* Pulse Test

See characteristic curves of 2SK1404


Power vs. Temperature Derating
90
60
30
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
50
30
10
3
1
0.3
0.1
0.05
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Operation in this
area is limited
by R_{DS}(on)
Ta = 25°C
1
3
10
30
100
300
1000
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
Tc = 25°C
θ ch – c(t) = γ s(t) · θ ch – c
θ ch – c = 2.08°C / W, Tc = 25°C
P DM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
Normalized Transient Thermal Impedance γ s (t)
Pulse Width PW (S)

2SK1831, 2SK1832

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

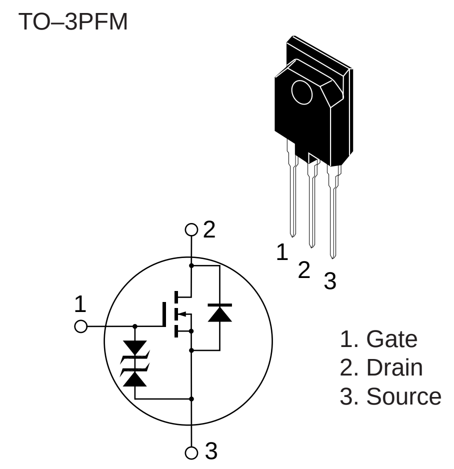


Table 1 Ordering Information

Type No	V_{DSS}
2SK1831	450V
2SK1832	500V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	K1831	V_{DSS}	450	V
	K1832		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	10	A
Drain peak current		$I_{D(pulse)}$*	30	A
Body–drain diode reverse drain current		I_{DR}	10	A
Channel dissipation		Pch**	50	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

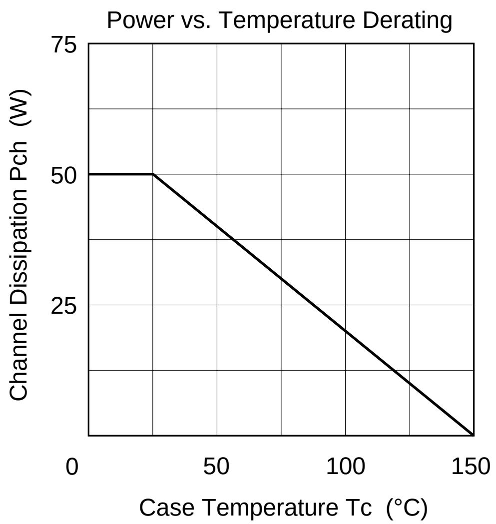
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

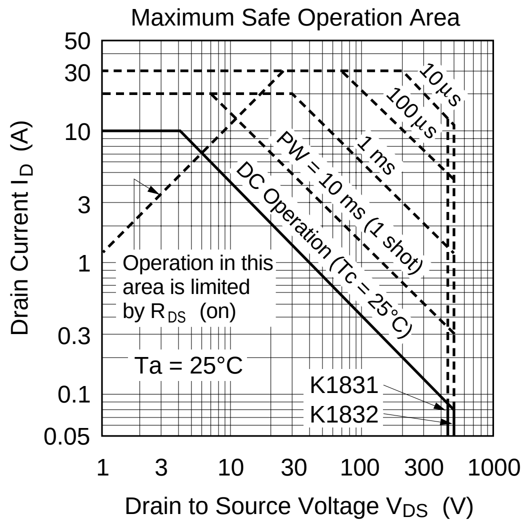
Table 3 Electrical Characteristics (Ta = 25°C)

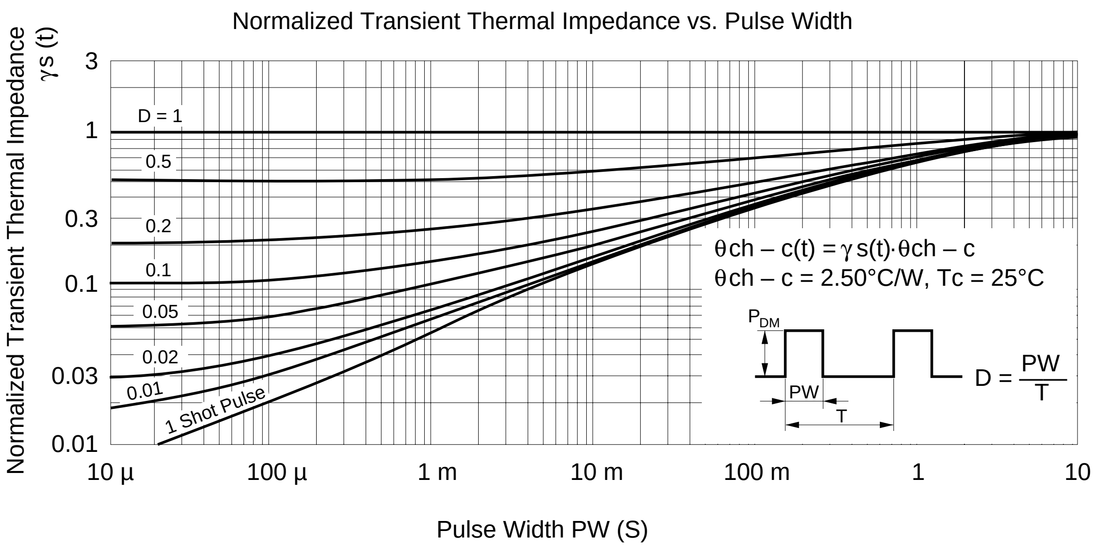
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	K1831	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	K1832		500	—	—		
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	K1831	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	K1832						V_{DS} = 400 V, VGS= 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	K1831	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 5 A V_{GS} = 10 V *
	K1832		—	0.7	0.9		
Forward transfer admittance		$\|y_{fs}\|$	4.0	7.0	—	S	I_D = 5 A V_{DS} = 10 V *
Input capacitance		Ciss	—	1050	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	280	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	40	—	pF	f = 1 MHz
Turn–on delay time		$t_{d(on)}$	—	15	—	ns	I_D = 5 A
Rise time		t_r	—	60	—	ns	V_{GS} = 10 V
Turn–off delay time		$t_{d(off)}$	—	90	—	ns	R_L = 6 Ω
Fall time		t_f	—	45	—	ns	
Body–drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time		t_{rr}	—	350	—	ns	I_F = 10 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1157, 2SK1158


Power vs. Temperature Derating
Channel Dissipation Pch (W)
75
50
25
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
50
30
10
3
1
0.3
0.1
0.05
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this
area is limited
by R_DS (on)
Ta = 25°C
K1831
K1832
1
3
10
30
100
300
1000
Drain to Source Voltage V_DS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch – c(t) = γ s(t)·θch – c
θch – c = 2.50°C/W, Tc = 25°C
P_DM
PW
T
D = PW/T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

2SK1835

Silicon N Channel MOS FET

Application

High speed power switching

Features

- High breakdown voltage (V_{DSS} = 1500V)
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator

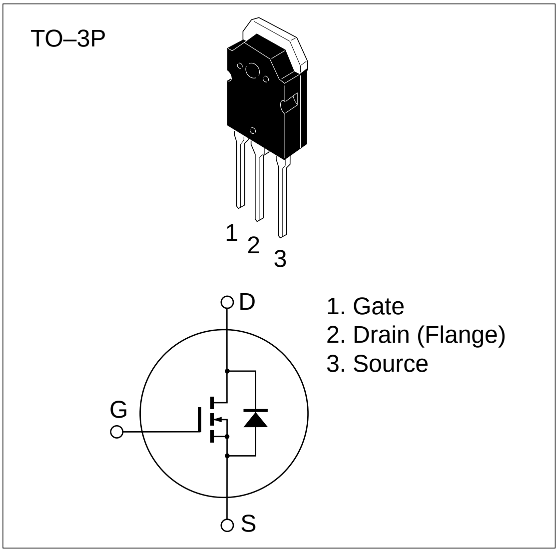


Table 1 Absolute Maximum Ratings (Ta = 25°C)

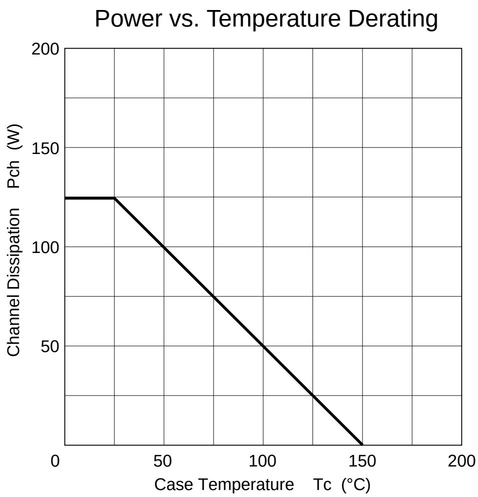
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1500	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$*	10	A
Body–drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch**	125	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

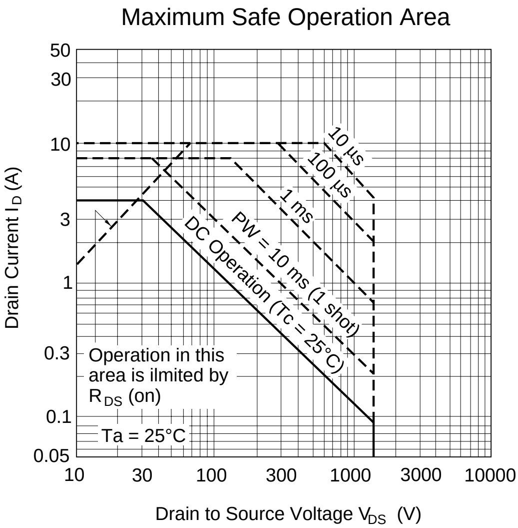
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

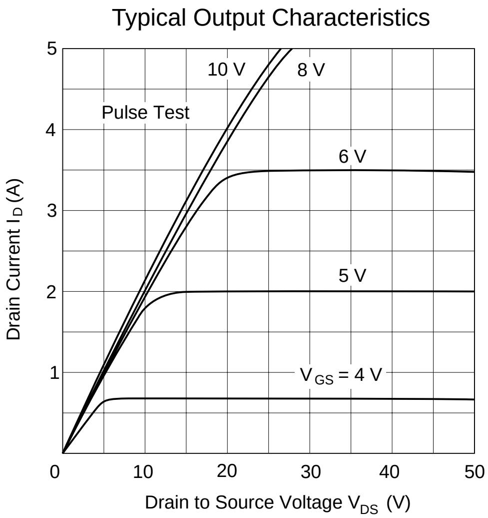
Table 2 Electrical Characteristics (Ta = 25°C)

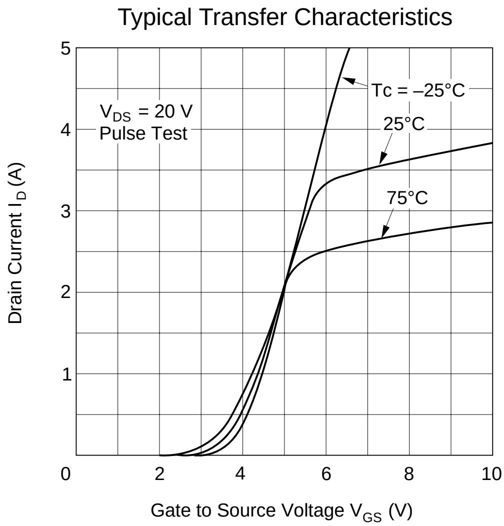
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	500	µA	V_{DS} = 1200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	4.6	7.0	Ω	I_D = 2 A V_{GS} = 15 V *
Forward transfer admittance	$\|y_{fs}\|$	0.9	1.4	—	S	I_D = 2 A V_{DS} = 20V *
Input capacitance	Ciss	—	1700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	230	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	100	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	I_D = 2A
Rise time	t_r	—	80	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	230	—	ns	R_L = 15 Ω
Fall time	t_f	—	80	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.85	—	V	I_F = 4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	2500	—	ns	I_F = 4 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

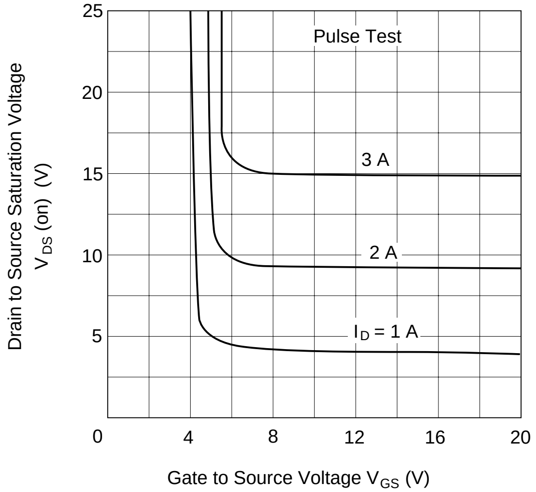

Power vs. Temperature Derating
Channel Dissipation Pch (W)
200
150
100
50
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
30
10
3
1
0.3
0.1
0.05
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this
area is ilmited by
R DS (on)
Ta = 25°C
10
30
100
300
1000
3000
10000
Drain to Source Voltage VDS (V)

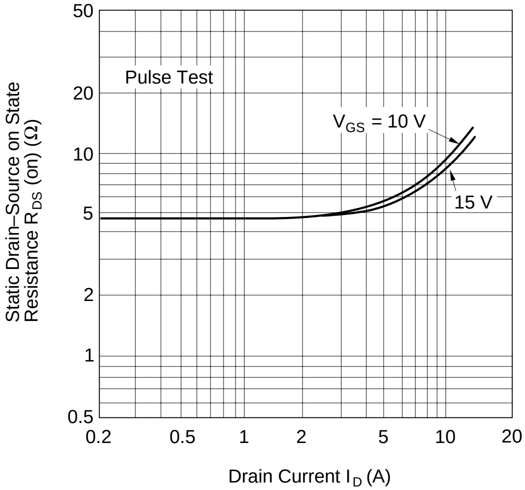

Typical Output Characteristics
Drain Current I D (A)
5
4
3
2
1
0
10 V
8 V
Pulse Test
6 V
5 V
VGS = 4 V
10
20
30
40
50
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
Drain Current I D (A)
5
4
3
2
1
0
VDS = 20 V
Pulse Test
Tc = –25°C
25°C
75°C
2
4
6
8
10
Gate to Source Voltage VGS (V)

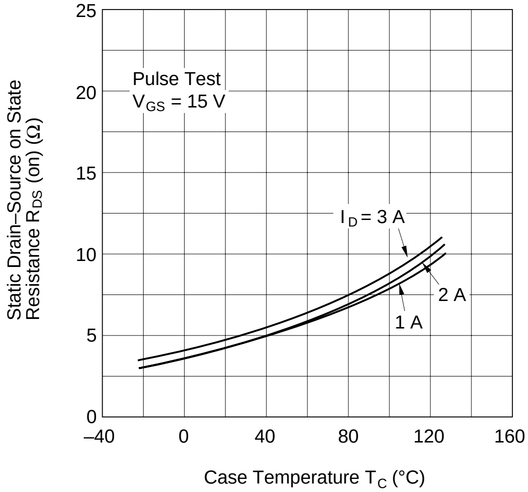
Drain-Source Saturation Voltage vs. Gate-Source Voltage



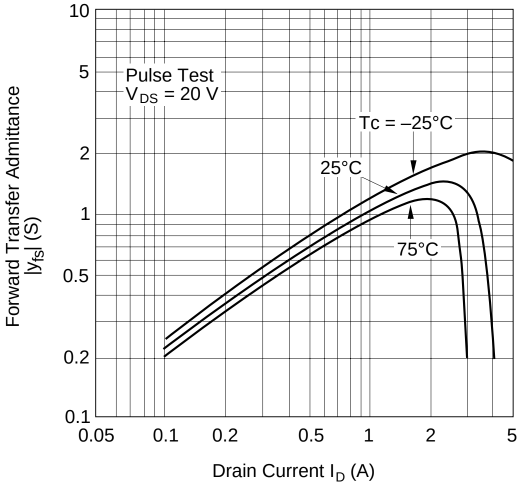
Static Drain-Source on State Resistance vs. Drain Current

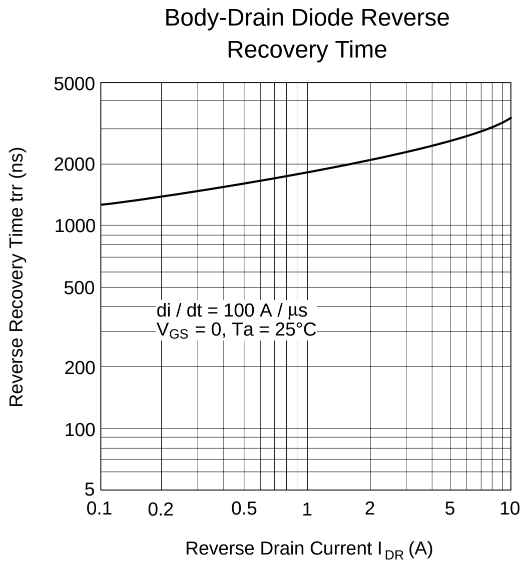


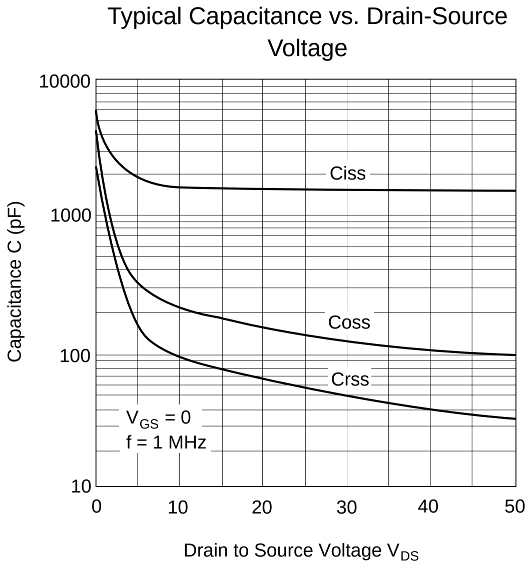
Static Drain-Source on State Resistance vs. Temperature

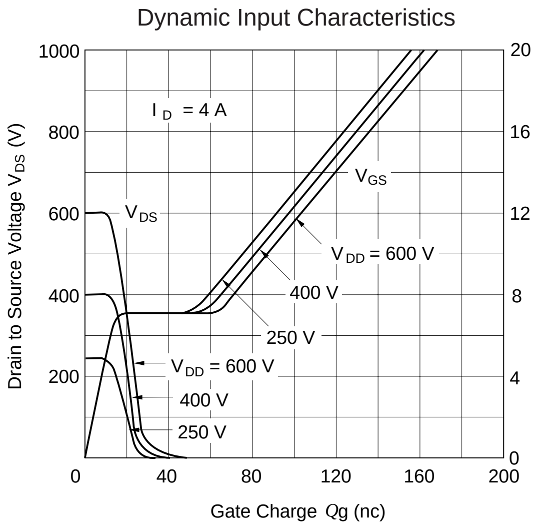


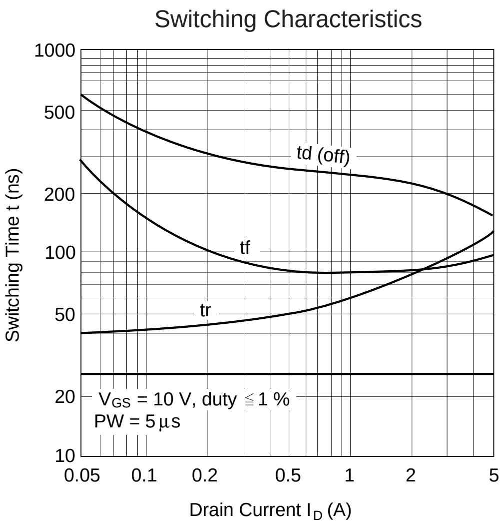
Forward Transfer Admittance vs. Drain Current



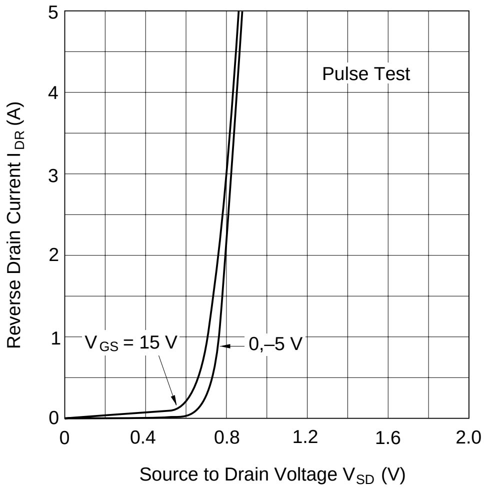

Body-Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
5000
2000
1000
500
200
100
5
di / dt = 100 A / µs
VGS = 0, Ta = 25°C
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain-Source Voltage
Capacitance C (pF)
10000
1000
100
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS

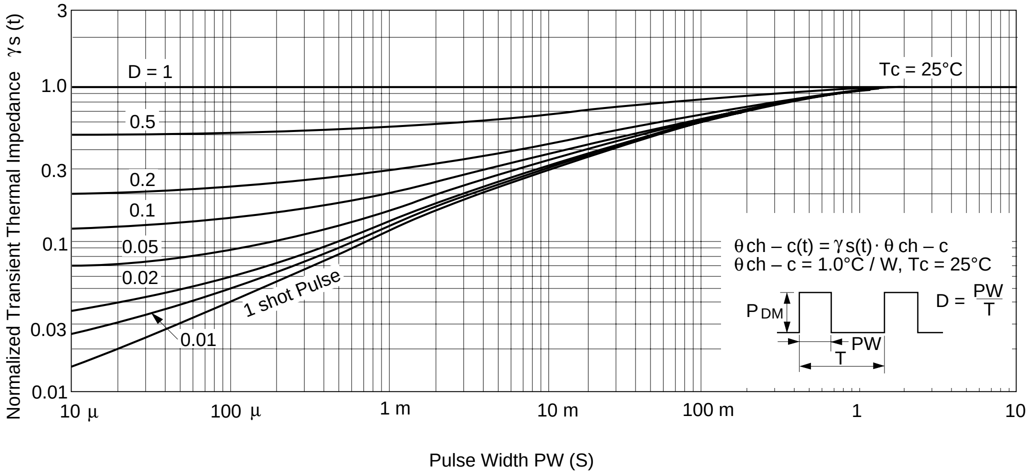

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
1000
800
600
400
200
20
16
12
8
4
0
I D = 4 A
VGS
VDS
VDD = 600 V
400 V
250 V
VDD = 600 V
400 V
250 V
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
td (off)
tf
tr
VGS = 10 V, duty ≦ 1 %
PW = 5 µs
0.05
0.1
0.2
0.5
1
2
5
Drain Current ID (A)

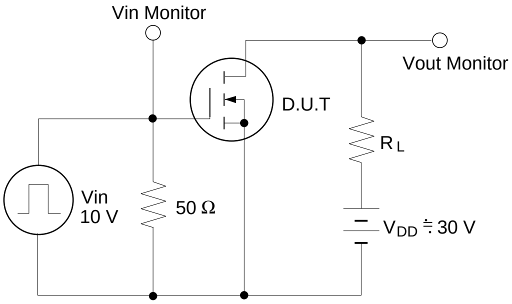
Reverse Drain Current vs. Source to Drain Voltage



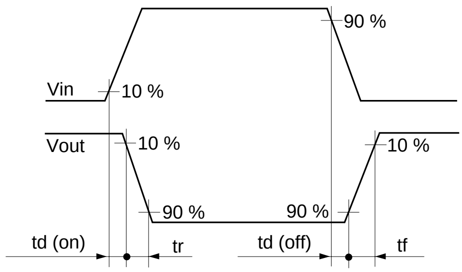
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveforms



2SK1836, 2SK1837

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

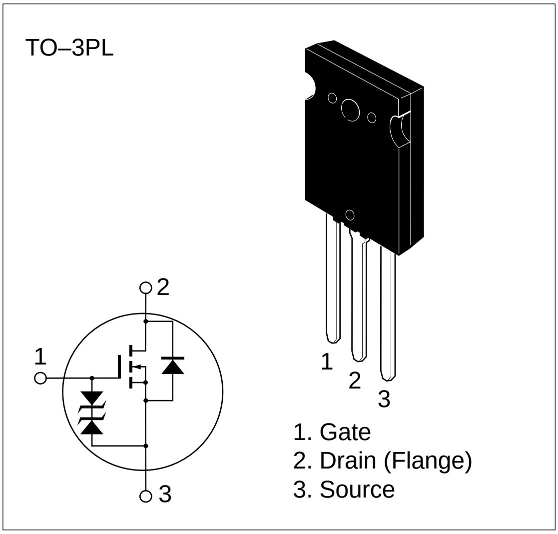


Table 1 Ordering Information

Type No	V_{DSS}
2SK1836	450V
2SK1837	500V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

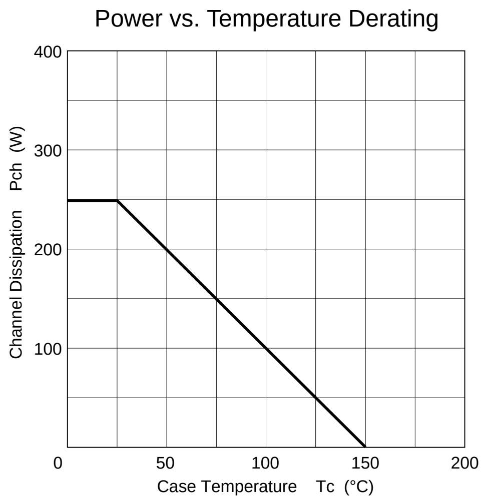
Item		Symbol	Ratings	Unit
Drain to source voltage	K1836	V_{DSS}	450	V
	K1837		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	50	A
Drain peak current		$I_{D(pulse)}^*$	200	A
Body–drain diode reverse drain current		I_{DR}	50	A
Channel dissipation		Pch**	250	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

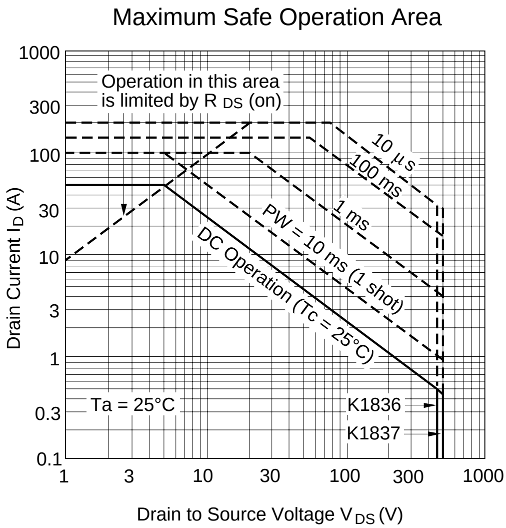
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

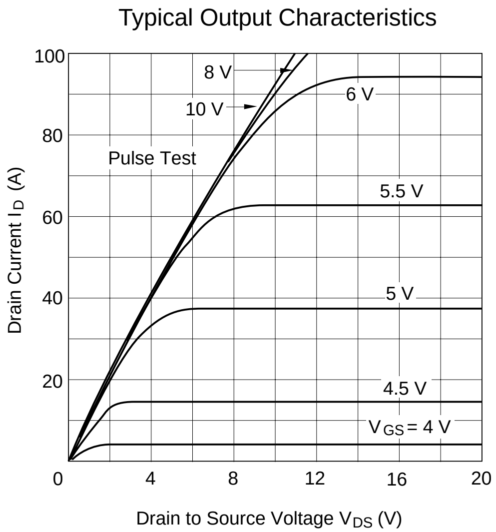
Table 3 Electrical Characteristics (Ta = 25°C)

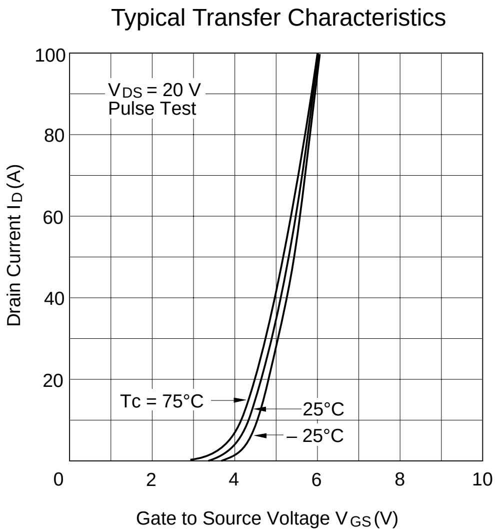
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	K1836	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	K1837		500	—	—		
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	μA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	K1836	I_{DSS}	—	—	250	μA	V_{DS} = 360 V, V_{GS} = 0
	K1837						V_{DS} = 400 V, V_{GS}= 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	K1836	$R_{DS(on)}$	—	0.08	0.10	Ω	I_D = 25 A V_{GS}= 10 V *
	K1837		—	0.085	0.11		
Forward transfer admittance		$\|y_{fs}\|$	22	35	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance		Ciss	—	8150	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	2100	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	180	—	pF	f = 1 MHz
Turn–on delay time		$t_{d(on)}$	—	80	—	ns	I_D = 25 A
Rise time		t_r	—	250	—	ns	V_{GS} = 10 V
Turn–off delay time		$t_{d(off)}$	—	550	—	ns	R_L = 1.2 Ω
Fall time		t_f	—	220	—	ns	
Body–drain diode forward voltage		V_{DF}	—	1.1	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time		t_{rr}	—	620	—	ns	I_F = 50 A, V_{GS} = 0, di_F / dt = 100 A / μs

* Pulse Test

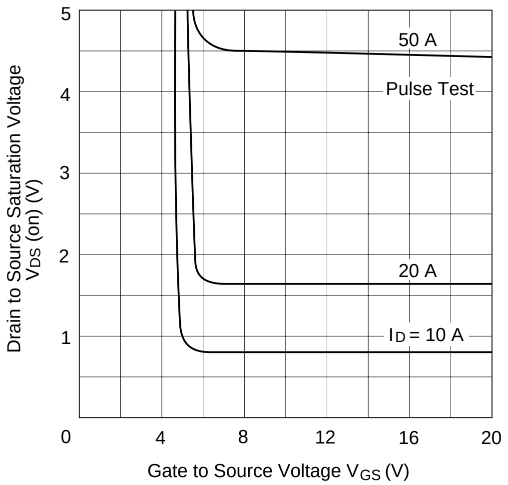

Power vs. Temperature Derating
400
300
200
100
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
1000
300
100
30
10
3
1
0.3
0.1
Operation in this area
is limited by R DS (on)
10 μs
100 ms
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25°C
K1836
K1837
1
3
10
30
100
300
1000
Drain Current ID (A)
Drain to Source Voltage VDS (V)

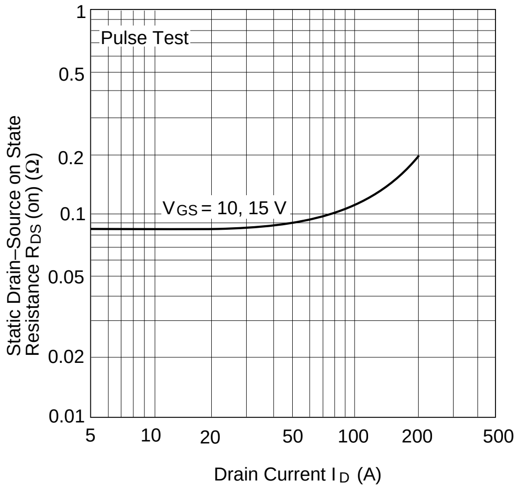

Typical Output Characteristics
100
80
60
40
20
8 V
10 V
6 V
Pulse Test
5.5 V
5 V
4.5 V
VGS = 4 V
0
4
8
12
16
20
Drain Current ID (A)
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
100
80
60
40
20
VDS = 20 V
Pulse Test
Tc = 75°C
25°C
– 25°C
0
2
4
6
8
10
Drain Current ID (A)
Gate to Source Voltage VGS (V)

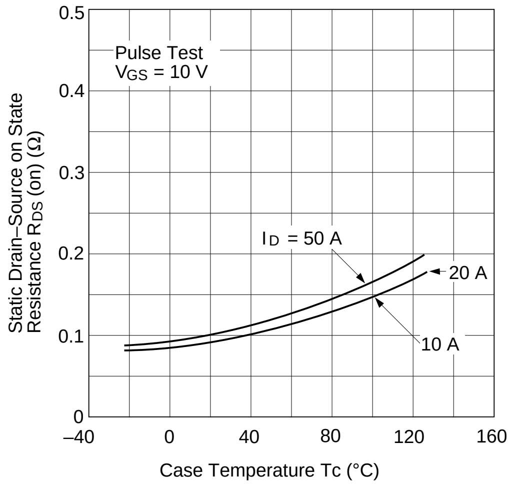
Drain-Source Saturation Voltage vs. Gate-Source Voltage



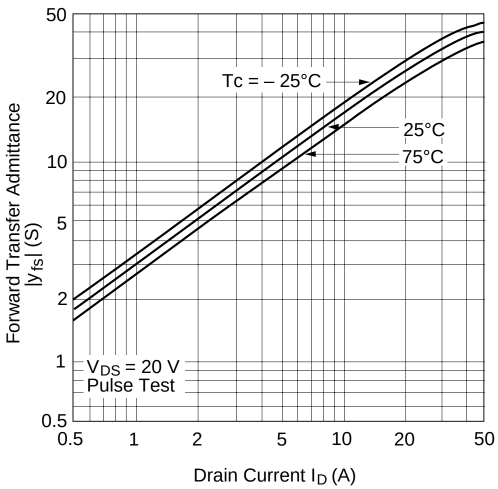
Static Drain-Source on State Resistance vs. Drain Current



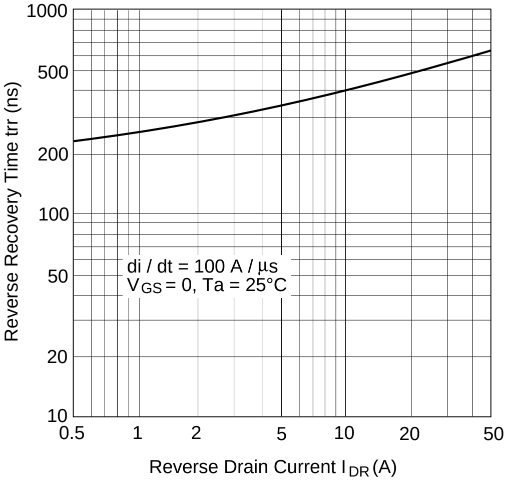
Static Drain-Source on State Resistance vs. Temperature



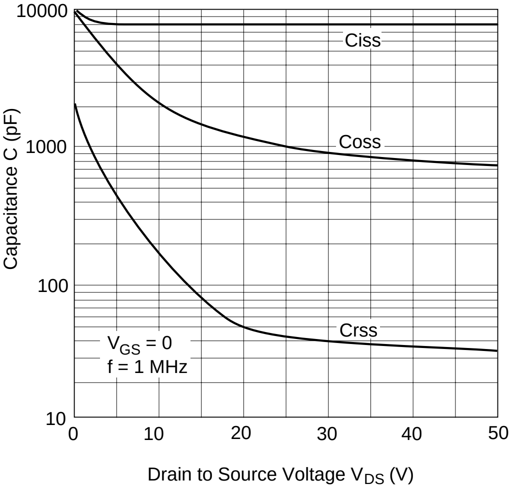
Forward Transfer Admittance vs. Drain Current



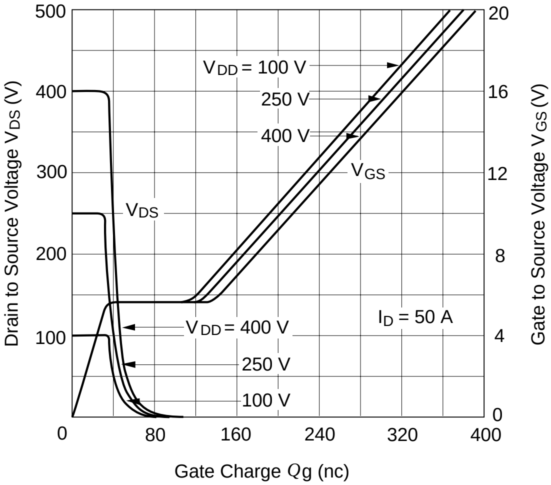
Body-Drain Diode Reverse Recovery Time



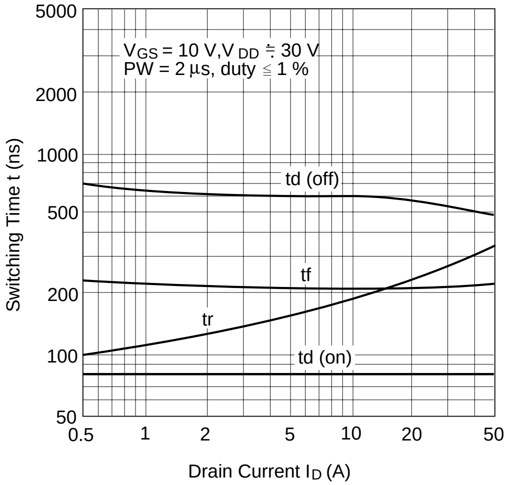
Typical Capacitance vs. Drain-Source Voltage

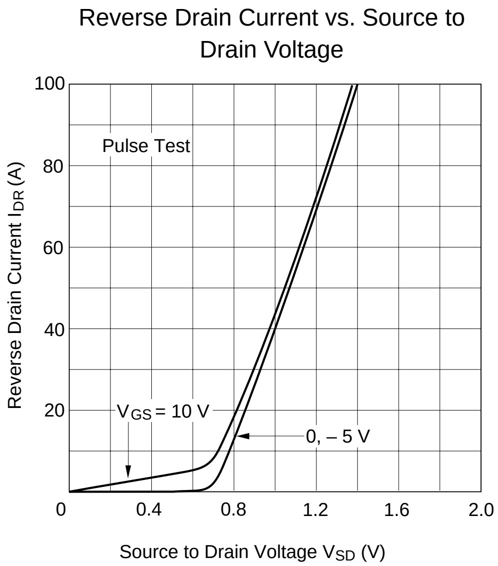


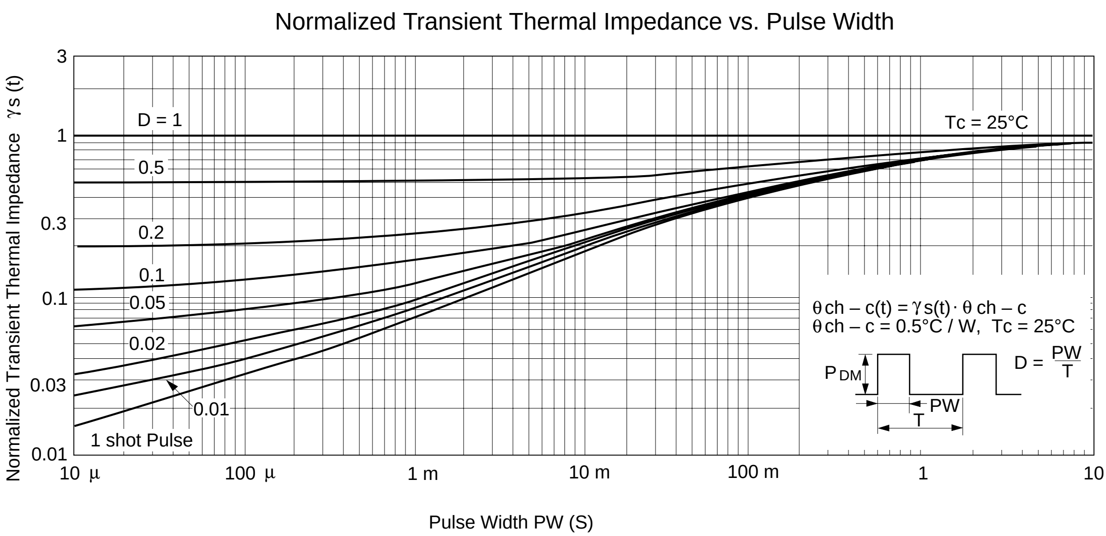
Dynamic Input Characteristics



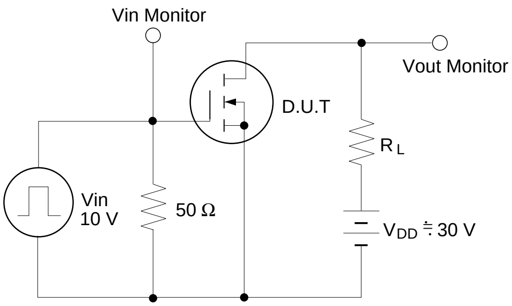
Switching Characteristics



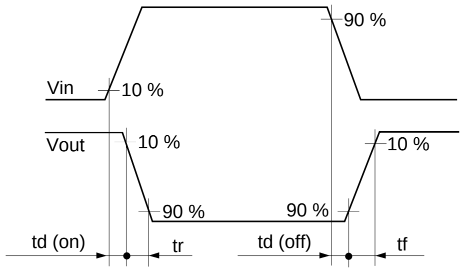

Reverse Drain Current vs. Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
100
80
60
40
20
0
Pulse Test
V_{GS} = 10 V
0, – 5 V
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
Tc = 25°C
θ ch – c(t) = γ s(t) · θ ch – c
θ ch – c = 0.5°C / W, Tc = 25°C
P_{DM}
D = PW / T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Switching Time Test Circuit



Waveforms



2SK1838(L), 2SK1838(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

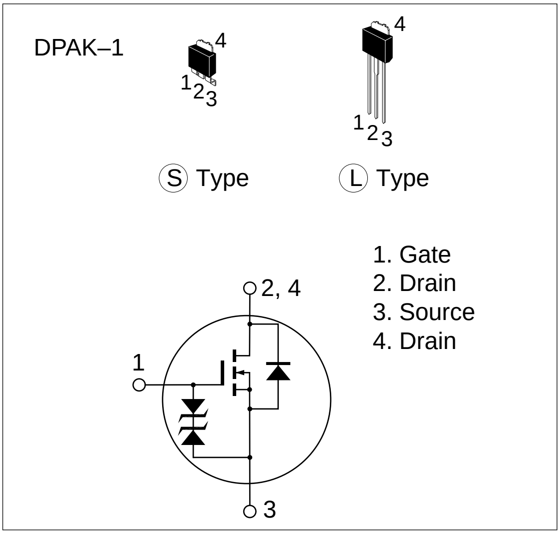


Table 1 Absolute Maximum Ratings (Ta = 25°C)

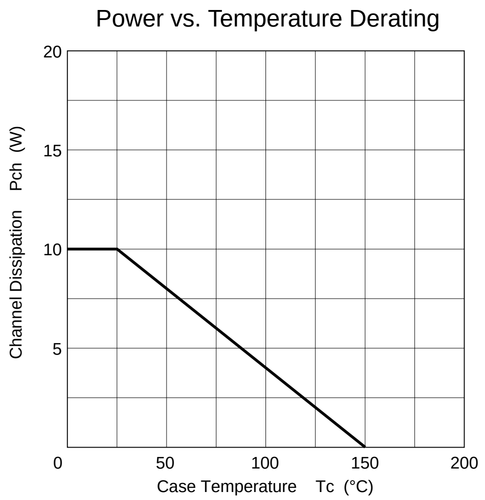
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	1	A
Drain peak current	$I_{D(pulse)}$*	2	A
Body–drain diode reverse drain current	I_{DR}	1	A
Channel dissipation	Pch**	10	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

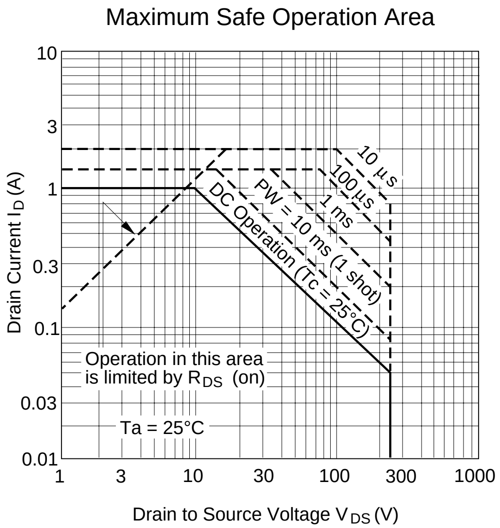
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	50	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	5.5	8.0	Ω	I_D = 0.5 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	0.3	0.5	—	S	I_D = 0.5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	60	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	30	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	5	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 0.5 A
Rise time	t_r	—	6	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	10	—	ns	R_L = 60 Ω
Fall time	t_f	—	4.5	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.96	—	V	I_F = 1 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	160	—	ns	I_F = 1 A, V_{GS} = 0, di_F / dt = 100 A / µs

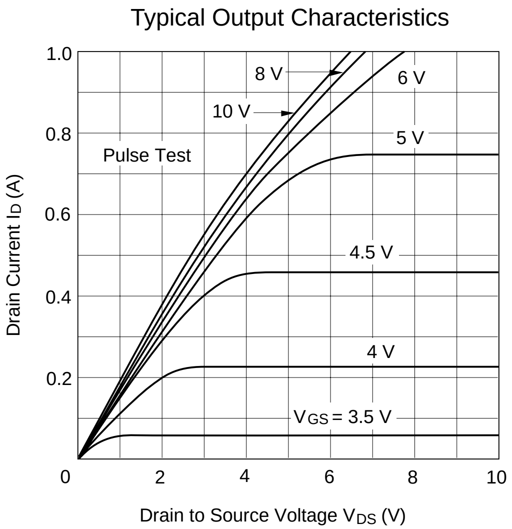
* Pulse Test



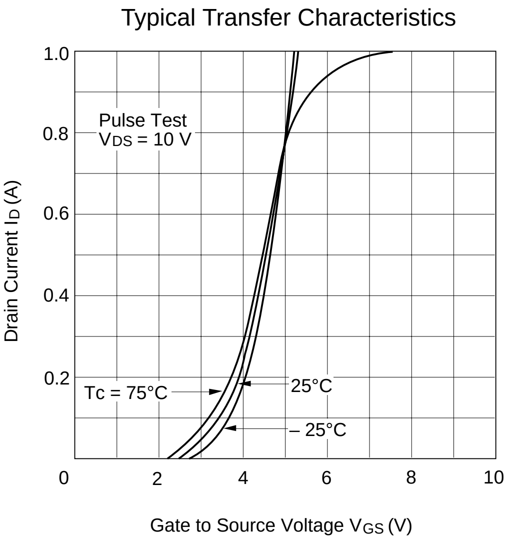
Power vs. Temperature Derating
Channel Dissipation Pch (W)
20
15
10
5
0
50
100
150
200
Case Temperature Tc (°C)



Maximum Safe Operation Area
Drain Current I D (A)
10
3
1
0.3
0.1
0.03
0.01
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R DS (on)
Ta = 25°C
1
3
10
30
100
300
1000
Drain to Source Voltage V DS (V)

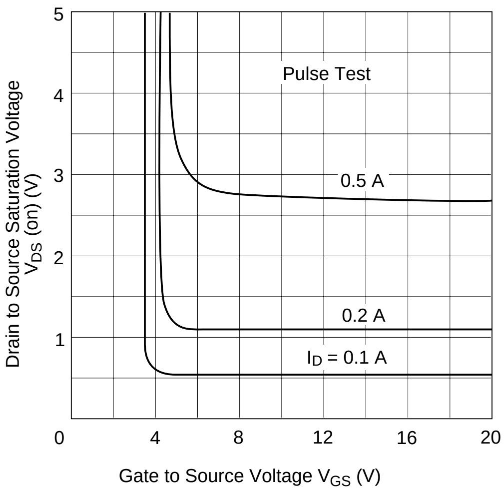


Typical Output Characteristics
Drain Current I D (A)
1.0
0.8
0.6
0.4
0.2
0
8 V
10 V
6 V
5 V
Pulse Test
4.5 V
4 V
V GS = 3.5 V
2
4
6
8
10
Drain to Source Voltage V DS (V)

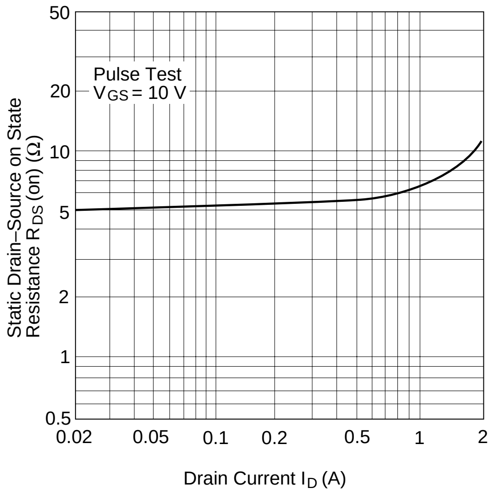


Typical Transfer Characteristics
Drain Current I D (A)
1.0
0.8
0.6
0.4
0.2
0
Pulse Test
V DS = 10 V
Tc = 75°C
25°C
– 25°C
2
4
6
8
10
Gate to Source Voltage V GS (V)

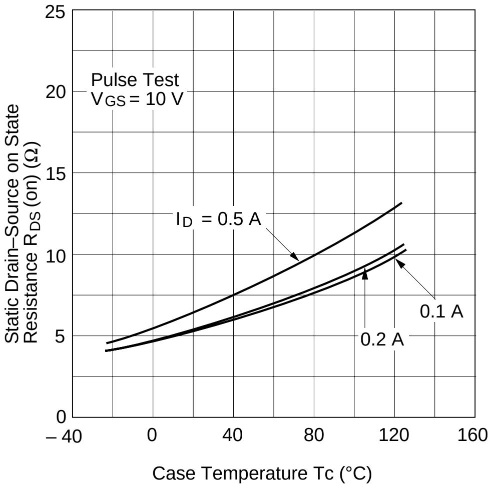
Drain-Source Saturation Voltage vs. Gate-Source Voltage



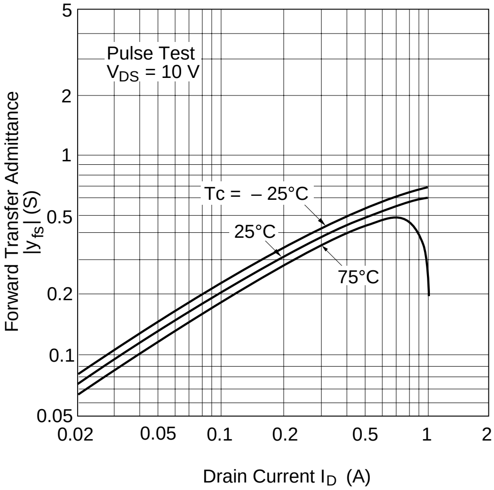
Static Drain-Source on State Resistance vs. Drain Current

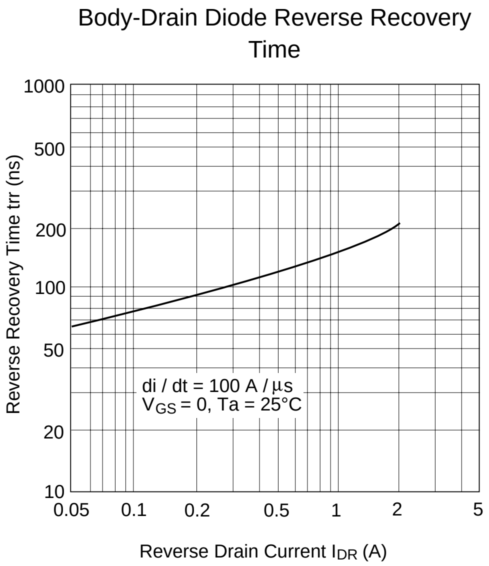


Static Drain-Source on State Resistance vs. Temperature

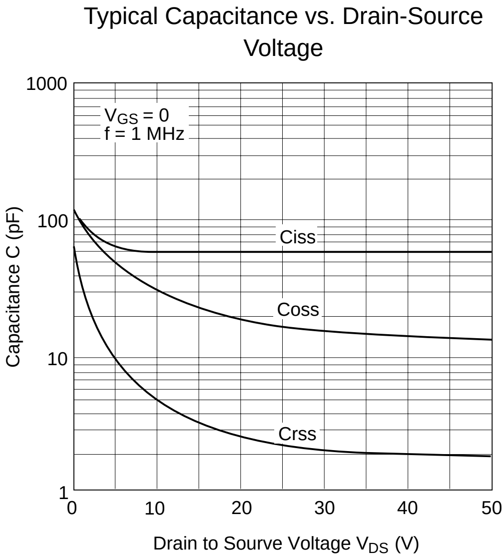


Forward Transfer Admittance vs. Drain Current

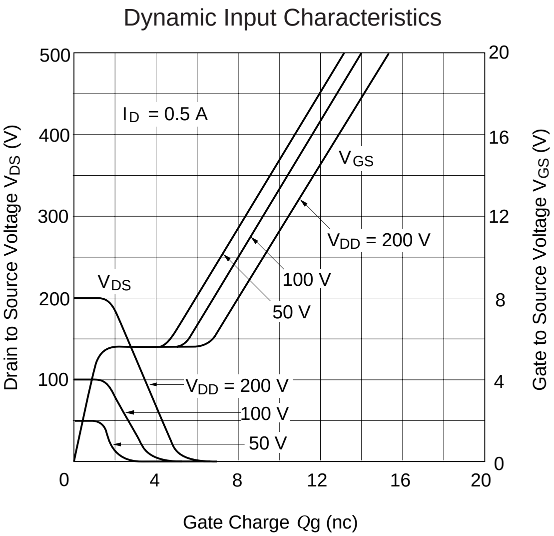




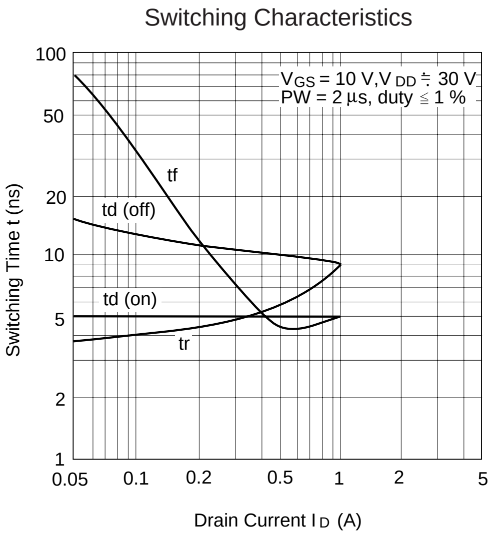
Body-Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.05
0.1
0.2
0.5
1
2
5
di / dt = 100 A / µs
V_GS = 0, Ta = 25°C
Reverse Drain Current I_DR (A)



Typical Capacitance vs. Drain-Source Voltage
Capacitance C (pF)
1000
100
10
1
0
10
20
30
40
50
V_GS = 0
f = 1 MHz
Ciss
Coss
Crss
Drain to Sourve Voltage V_DS (V)

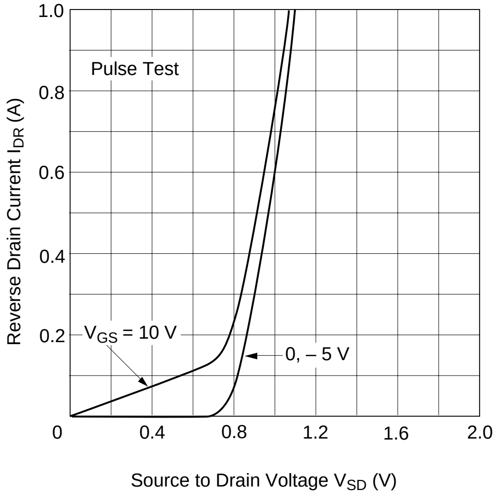


Dynamic Input Characteristics
Drain to Source Voltage V_DS (V)
500
400
300
200
100
0
4
8
12
16
20
Gate to Source Voltage V_GS (V)
20
16
12
8
4
0
I_D = 0.5 A
V_GS
V_DD = 200 V
100 V
50 V
V_DS
V_DD = 200 V
100 V
50 V
Gate Charge Qg (nc)

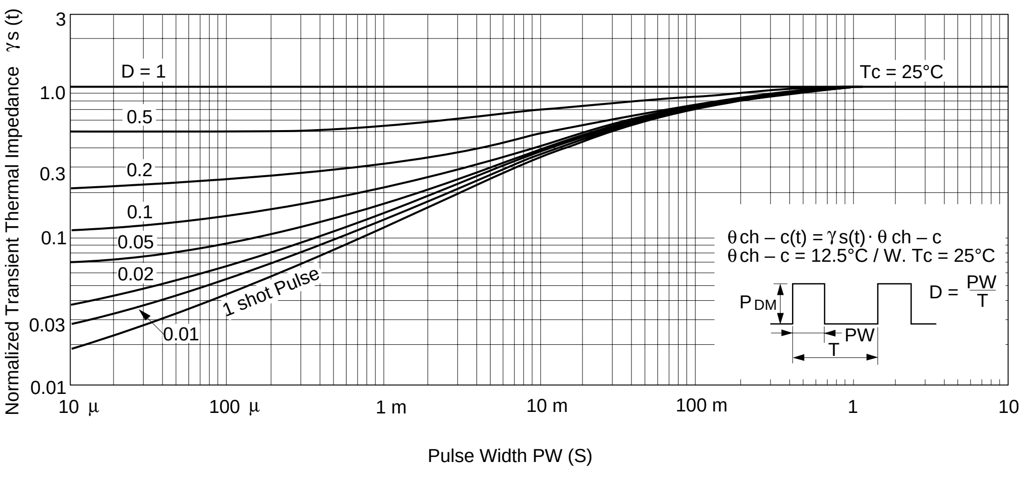


Switching Characteristics
Switching Time t (ns)
100
50
20
10
5
2
1
0.05
0.1
0.2
0.5
1
2
5
V_GS = 10 V,V_DD ≒ 30 V
PW = 2 µs, duty ≦ 1 %
tf
td (off)
td (on)
tr
Drain Current I_D (A)

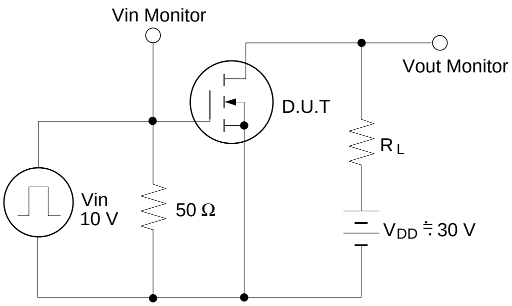
Reverse Drain Current vs. Source to Drain Voltage



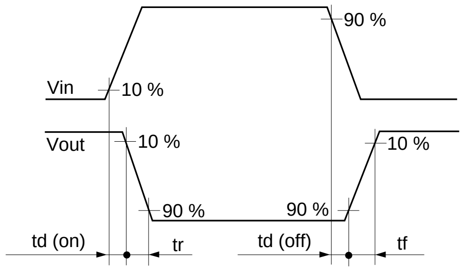
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveforms



2SK1859

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low Drive Current
- No secondary breakdown
- Suitable for Switching regulator

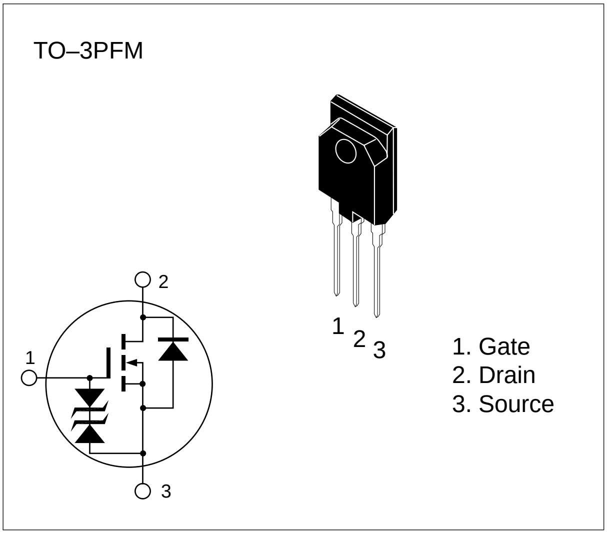


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	900	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	6	A
Drain peak current	$I_{D(pulse)}$*	15	A
Body–drain diode reverse drain current	I_{DR}	6	A
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

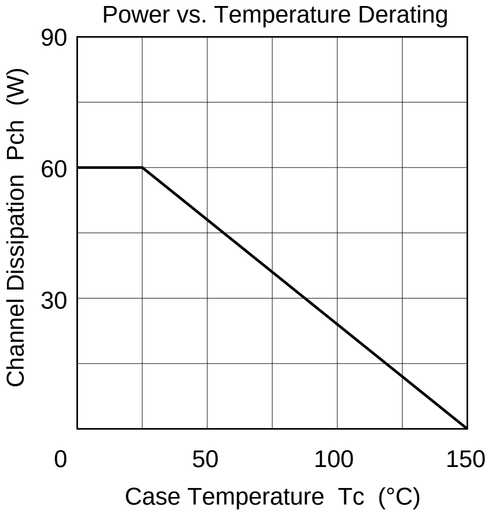
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

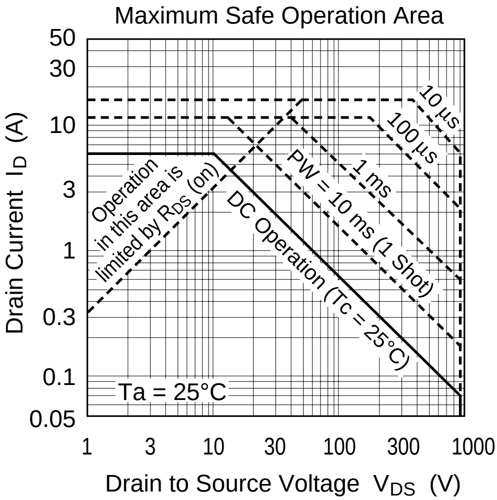
Table 2 Electrical Characteristics (Ta = 25°C)

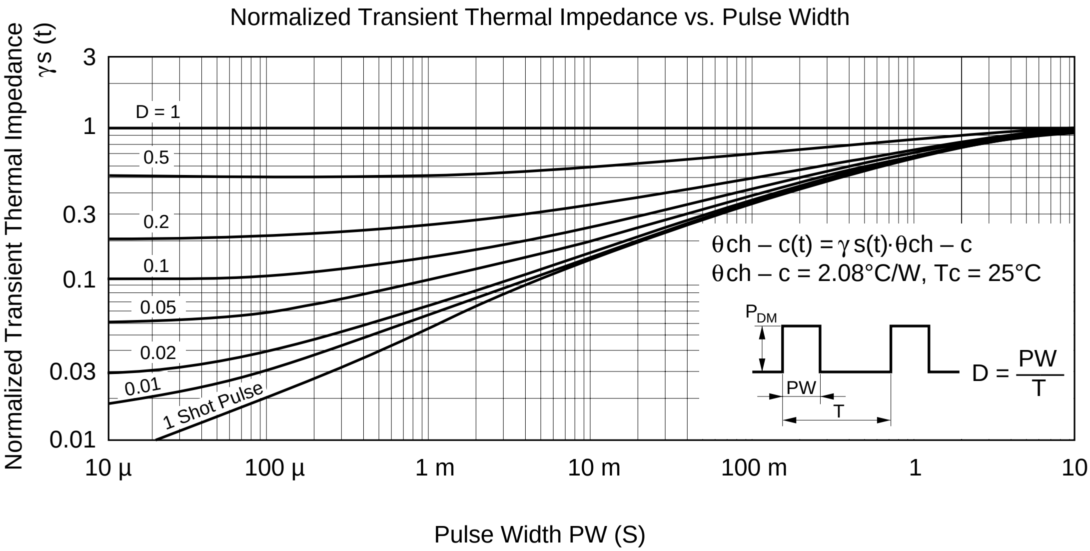
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	900	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 720 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	2.0	3.0	Ω	I_D = 3 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	2.3	3.7	—	S	I_D = 3 A V_{DS} = 20 V *
Input capacitance	Ciss	—	980	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	400	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	195	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 3 A
Rise time	t_r	—	80	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	125	—	ns	R_L = 10 Ω
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 6 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	1000	—	ns	I_F = 6 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1341


Power vs. Temperature Derating
90
60
30
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
50
30
10
3
1
0.3
0.1
0.05
1
3
10
30
100
300
1000
Drain Current I_D (A)
Drain to Source Voltage V_DS (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_DS (on)
Ta = 25°C


Normalized Transient Thermal Impedance vs. Pulse Width
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
θch – c(t) = γ s(t)·θch – c
θch – c = 2.08°C/W, Tc = 25°C
P_DM
PW
T
D = PW / T

2SK1862, 2SK1863

Silicon N Channel MOS FET

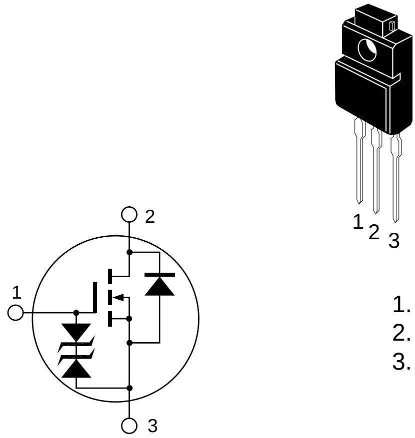
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for Switching regulator

TO–220FM



1. Gate
2. Drain
3. Source

Table 1 Ordering Information

Type No.	V_{DSS}
2SK1862	450 V
2SK1863	500 V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1862	V_{DSS}	450	V
	2SK1863	V_{DSS}	500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	3	A
Drain peak current		$I_{D(pulse)}$*	12	A
Body–drain diode reverse drain current		I_{DR}	3	A
Channel dissipation		Pch**	25	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

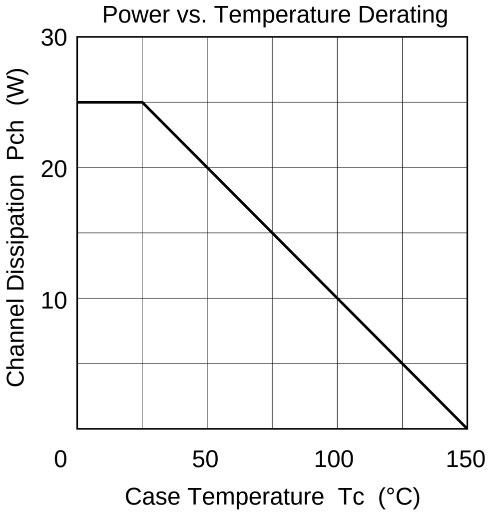
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

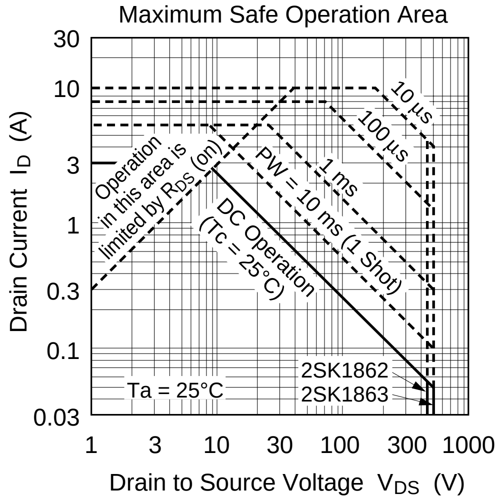
Table 3 Electrical Characteristics (Ta = 25°C)

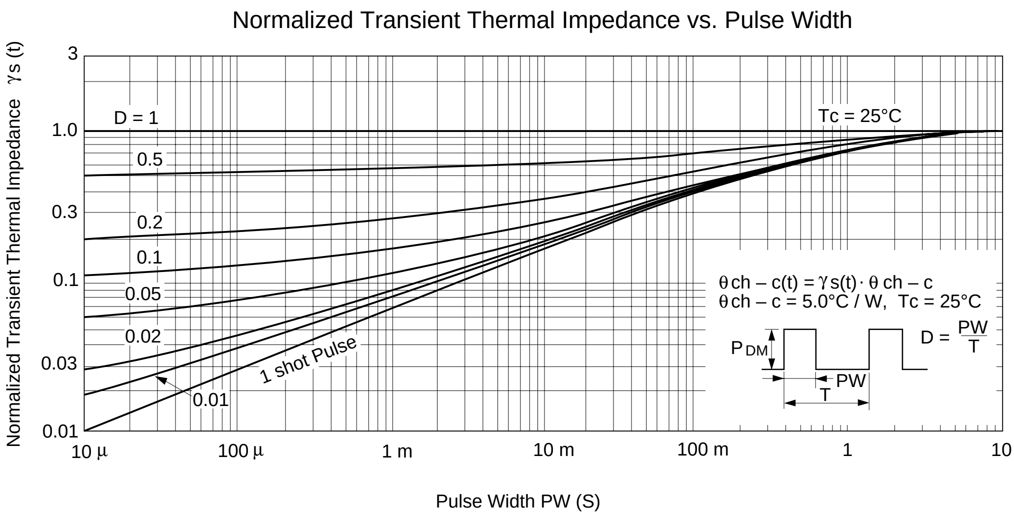
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1862	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1863		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1862	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1863						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	2SK1862	$R_{DS(on)}$	—	2.0	2.8	Ω	I_D = 2 A, V_{GS} = 10 V *
	2SK1863		—	2.2	3.0		
Forward transfer admittance		$\|y_{fs}\|$	1.5	2.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance		Ciss	—	330	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	90	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	15	—	pF	f = 1 MHz
Turn–on delay time		$t_{d(on)}$	—	7	—	ns	I_D = 2 A
Rise time		t_r	—	20	—	ns	V_{GS} = 10 V
Turn–off delay time		$t_{d(off)}$	—	30	—	ns	R_L = 15 Ω
Fall time		t_f	—	20	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.9	—	V	I_F = 3 A, V_{GS} = 0
Body–drain diode reverse recovery time		t_{rr}	—	300	—	ns	I_F = 3 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1153, 2SK1154


Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current ID (A)
30
10
3
1
0.3
0.1
0.03
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
Operation in this area is limited by RDS (on)
DC Operation (Tc = 25°C)
Ta = 25°C
2SK1862
2SK1863
1
3
10
30
100
300
1000
Drain to Source Voltage VDS (V)

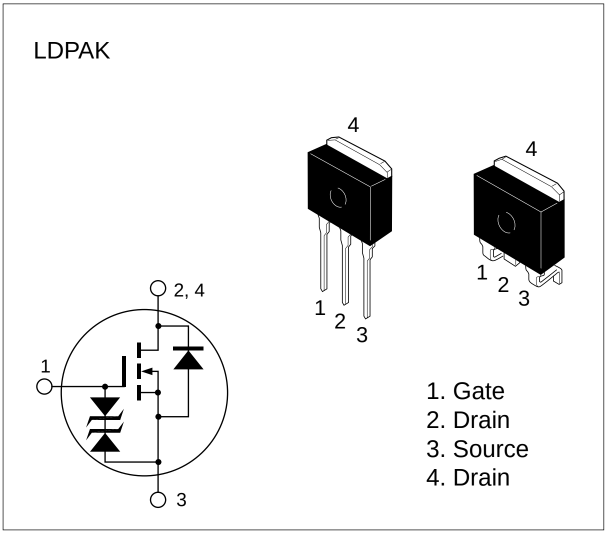

Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
Tc = 25°C
θ ch – c(t) = γ s(t) · θ ch – c
θ ch – c = 5.0°C / W, Tc = 25°C
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

2SK1869(L), 2SK1869(S)

Silicon N Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	350	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

*   PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	350	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =280 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	635	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	230	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	40	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 4 A
Rise time	t_r	—	50	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	60	—	ns	R_L = 7.5Ω
Fall time	t_f	—	40	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	240	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristic cures of 2SK1400A

2SK1880 (L), 2SK1880 (S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- No secondary breakdown
- Suitable for Switching regulator

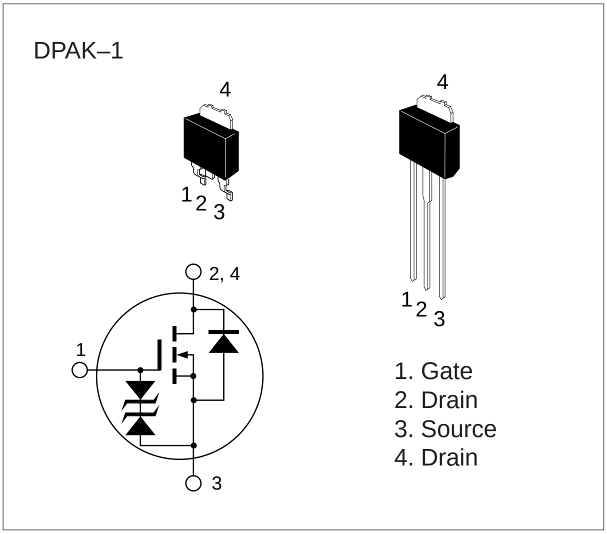


Table 1 Absolute Maximum Ratings (Ta = 25°C)

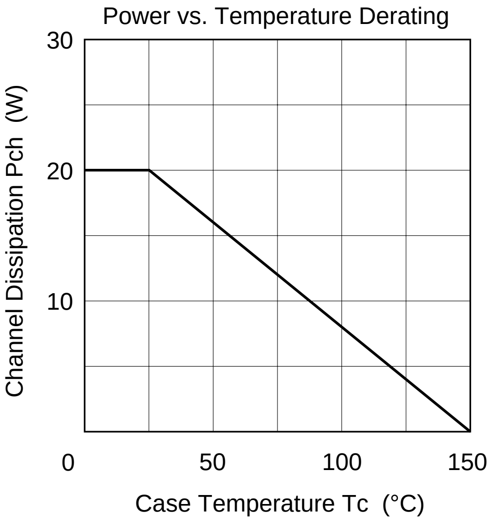
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	1.5	A
Drain peak current	$I_{D(pulse)}$*	3.0	A
Body–drain diode reverse drain current	I_{DR}	1.5	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

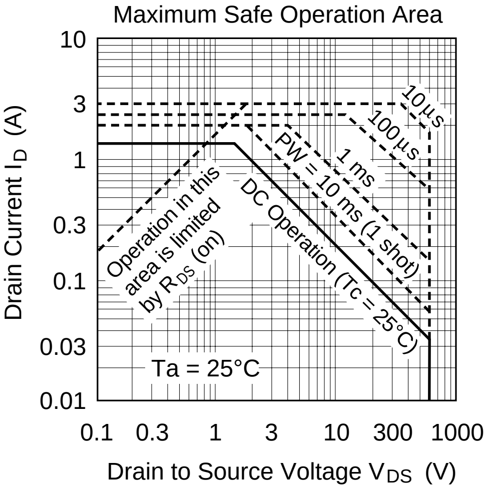
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

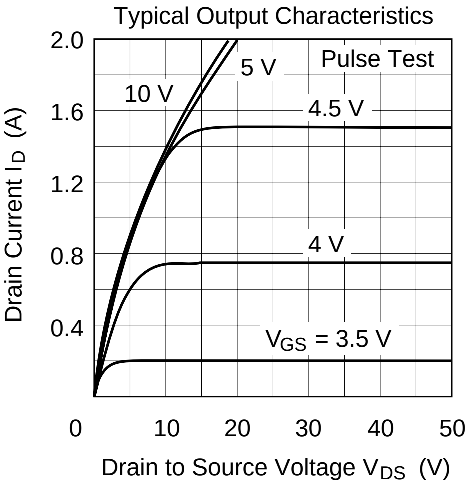
Table 2 Electrical Characteristics (Ta = 25°C)

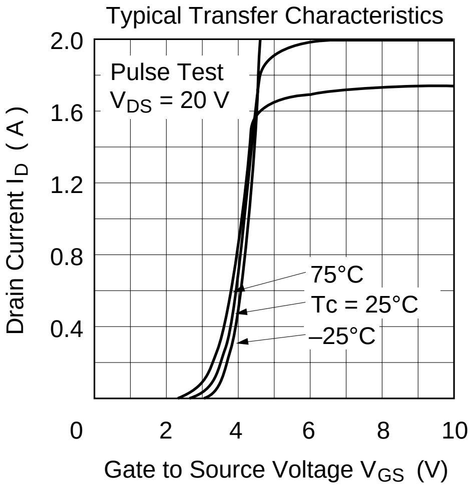
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	6.5	8.0	Ω	I_D = 1 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	0.85	1.4	—	S	I_D = 1 A V_{DS} = 20 V *
Input capacitance	Ciss	—	250	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	55	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	8	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 1 A
Rise time	t_r	—	25	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	35	—	ns	R_L = 30 Ω
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 1.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	350	—	µs	I_F = 1.5 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

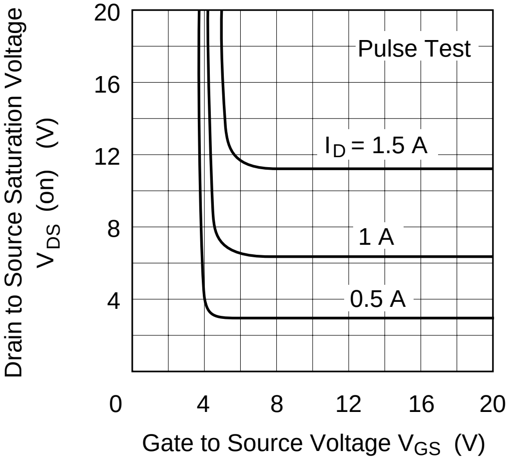

Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
10
3
1
0.3
0.1
0.03
0.01
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_{DS} (on)
Ta = 25°C
0.1
0.3
1
3
10
300
1000
Drain to Source Voltage V_{DS} (V)

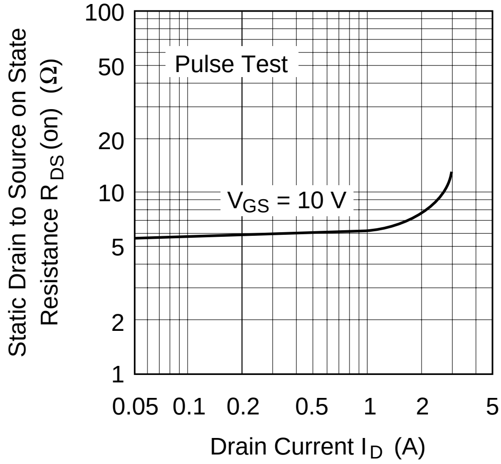

Typical Output Characteristics
Drain Current I_D (A)
2.0
1.6
1.2
0.8
0.4
10 V
5 V
Pulse Test
4.5 V
4 V
V_{GS} = 3.5 V
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
Drain Current I_D (A)
2.0
1.6
1.2
0.8
0.4
Pulse Test
V_{DS} = 20 V
75°C
Tc = 25°C
–25°C
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

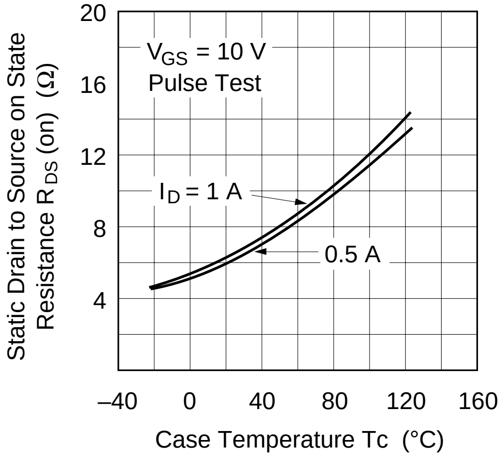
Drain to Source Saturation Voltage vs. Gate to Source Voltage



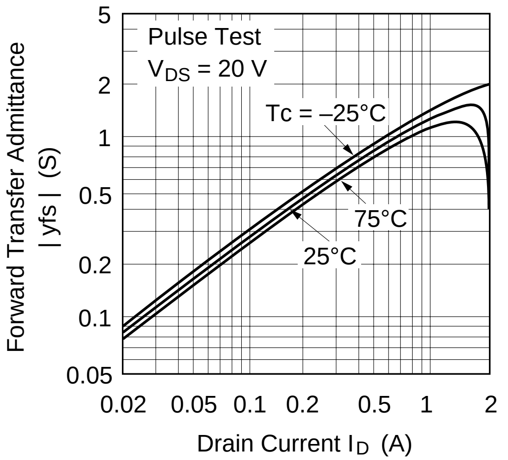
Static Drain to Source on State Resistance vs. Drain Current

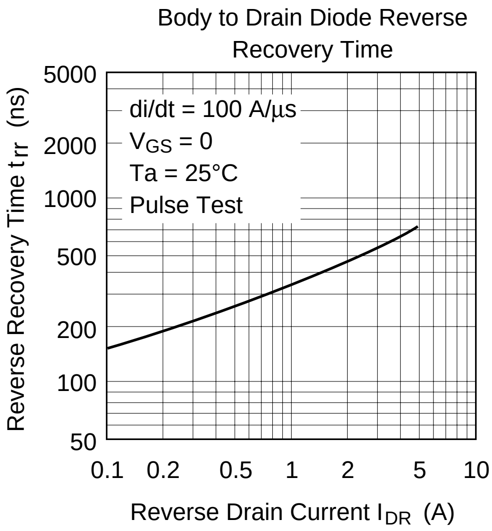


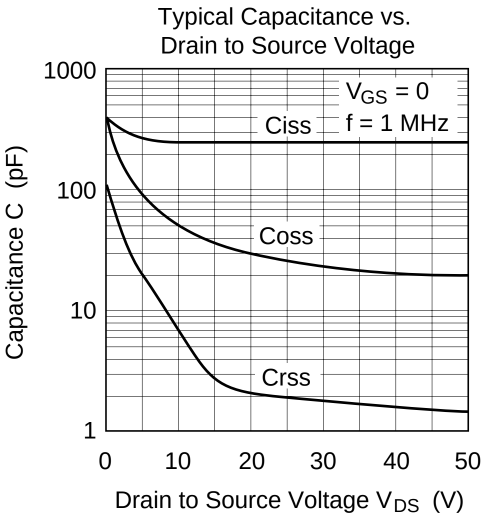
Static Drain to Source on State Resistance vs. Temperature

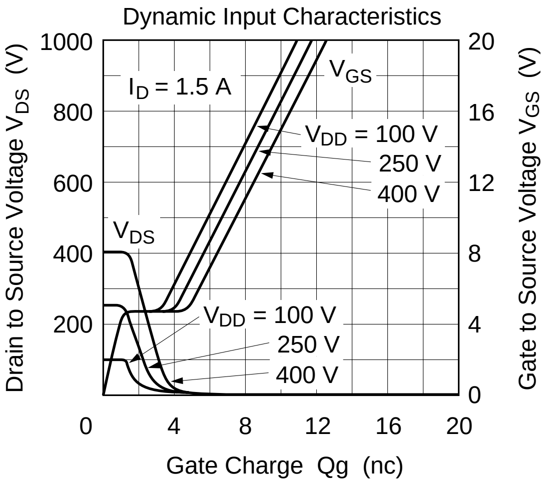


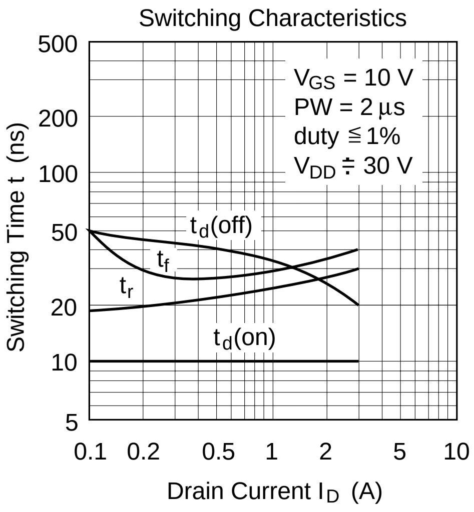
Forward Transfer Admittance vs. Drain Current



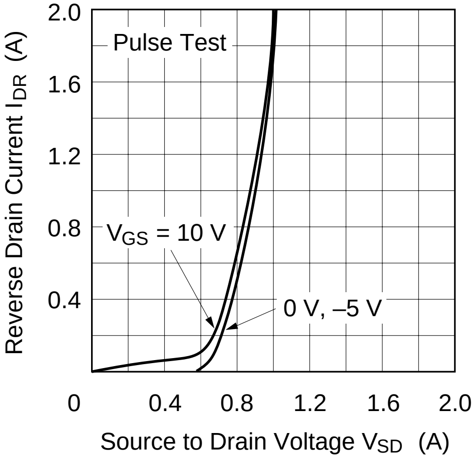

Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/μs
VGS = 0
Ta = 25°C
Pulse Test
Reverse Recovery Time trr (ns)
5000
2000
1000
500
200
100
50
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
1000
100
10
1
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
ID = 1.5 A
VGS
VDD = 100 V
250 V
400 V
VDS
VDD = 100 V
250 V
400 V
Drain to Source Voltage VDS (V)
1000
800
600
400
200
Gate to Source Voltage VGS (V)
20
16
12
8
4
0
0
4
8
12
16
20
Gate Charge Qg (nc)


Switching Characteristics
VGS = 10 V
PW = 2 μs
duty ≦ 1%
VDD ≒ 30 V
td(off)
tf
tr
td(on)
Switching Time t (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1
2
5
10
Drain Current ID (A)

Reverse Drain Current vs.
Source to Drain Voltage



2SK1910

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

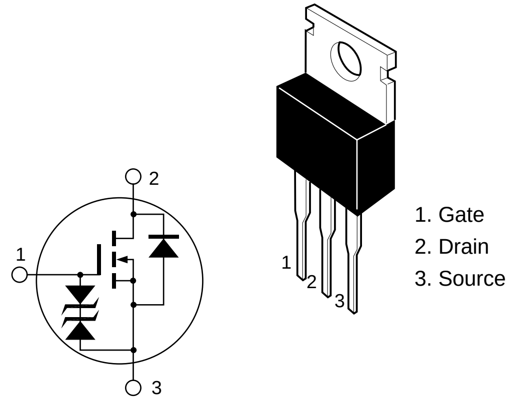


Table 1 Absolute Maximum Ratings (Ta = 25°C)

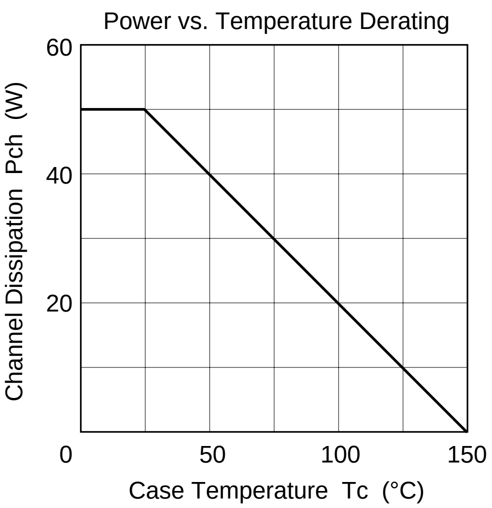
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$*	100	A
Body–drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP}***	25	A
Avalanche energy	E_{AR}***	53	mJ
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

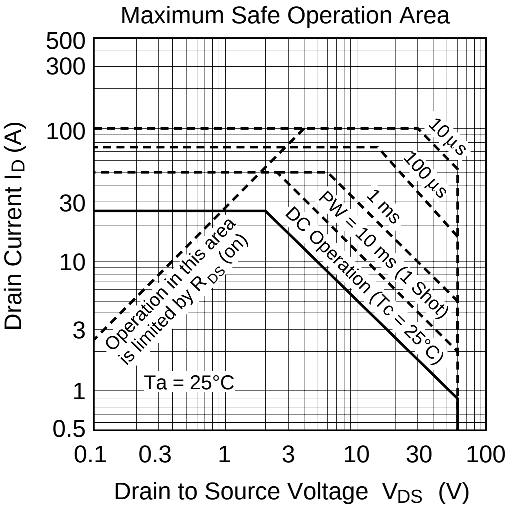
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

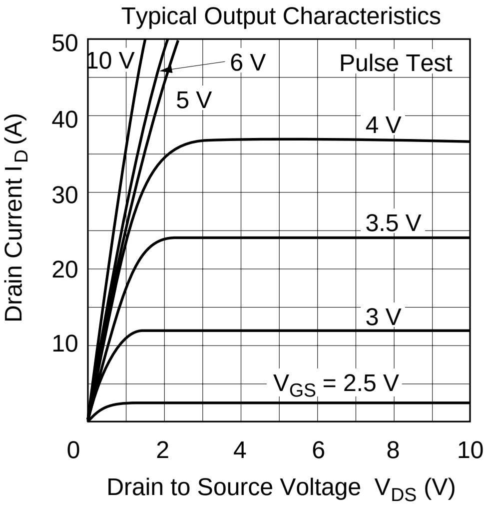
Table 2 Electrical Characteristics (Ta = 25°C)

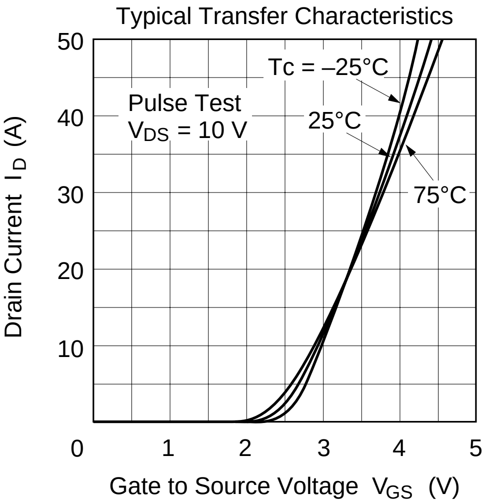
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.04	Ω	I_D = 15 A V_{GS} = 10 V *
		—	0.043	0.06	Ω	I_D = 15 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	21	—	S	I_D = 15 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	655	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	195	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 15 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	225	—	ns	R_L = 2 Ω
Fall time	t_f	—	145	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 25 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 25 A, V_{GS} = 0, diF / dt = 50 A / µs

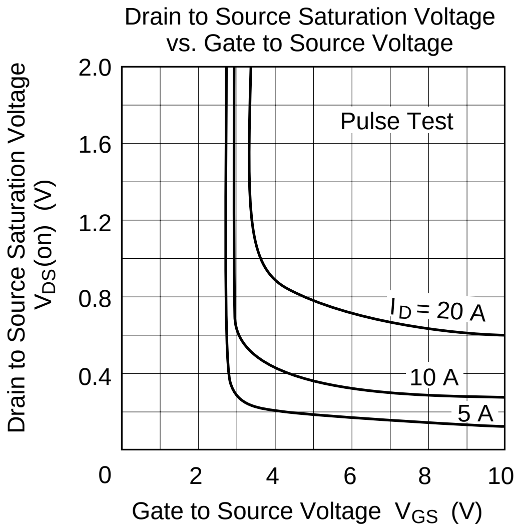
* Pulse Test

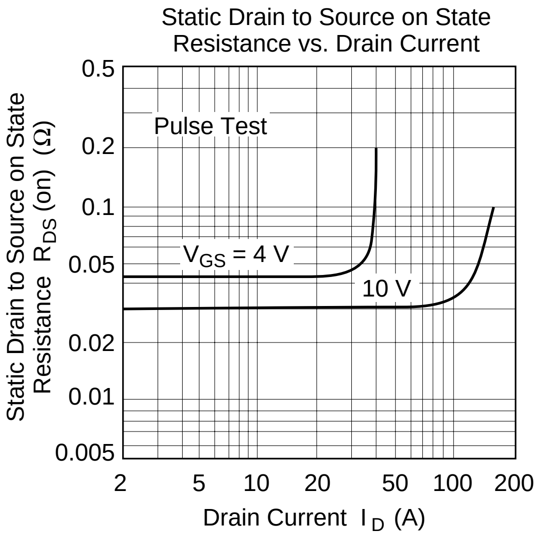

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)

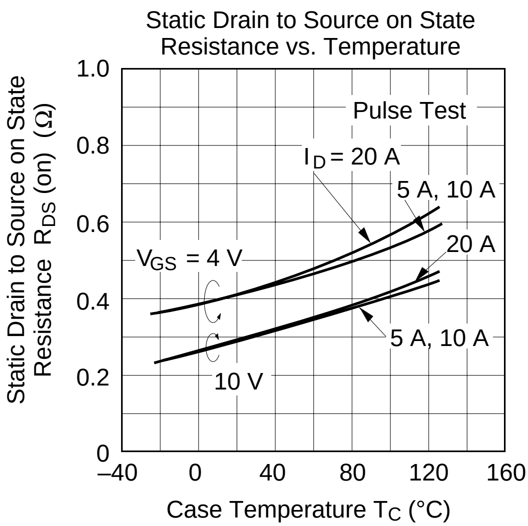

Maximum Safe Operation Area
Drain Current I_D (A)
500
300
100
30
10
3
1
0.5
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_{DS} (on)
Ta = 25°C

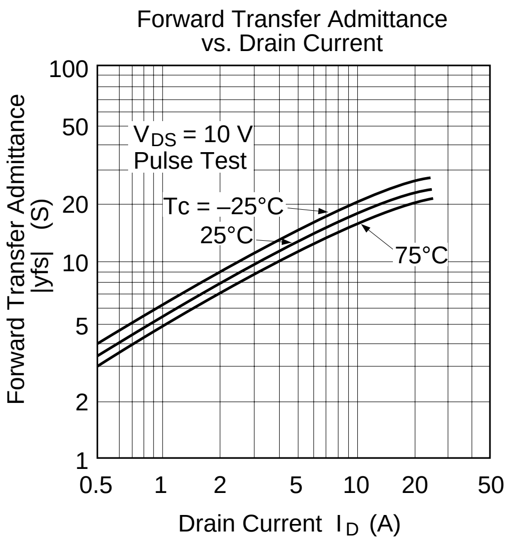

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
2
4
6
8
10
Drain to Source Voltage V_{DS} (V)
10 V
6 V
5 V
Pulse Test
4 V
3.5 V
3 V
V_{GS} = 2.5 V

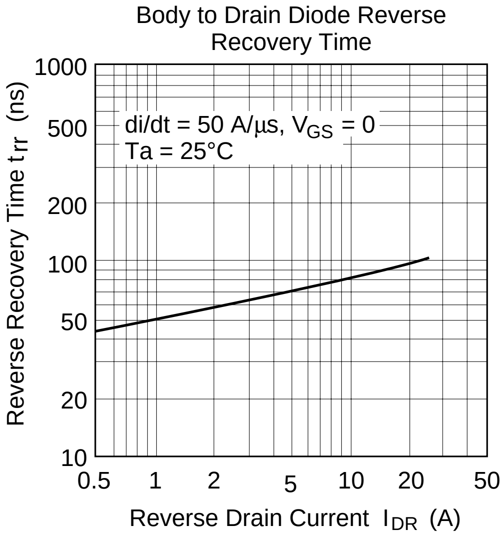

Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
1
2
3
4
5
Gate to Source Voltage V_{GS} (V)
Tc = –25°C
Pulse Test
V_{DS} = 10 V
25°C
75°C

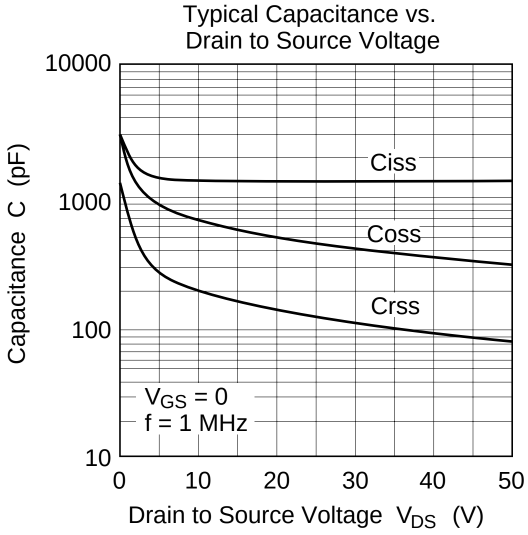

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
V_DS(on) (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V_GS (V)
Pulse Test
I_D = 20 A
10 A
5 A

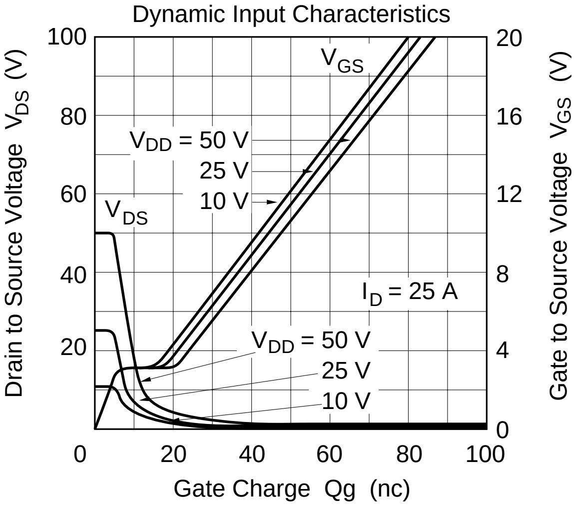

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State
Resistance R_DS (on) (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I_D (A)
Pulse Test
V_GS = 4 V
10 V

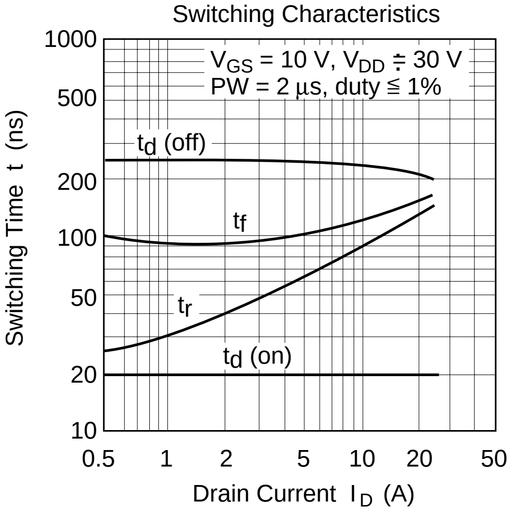

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State
Resistance R_DS (on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160
Case Temperature T_C (°C)
Pulse Test
I_D = 20 A
5 A, 10 A
20 A
V_GS = 4 V
5 A, 10 A
10 V

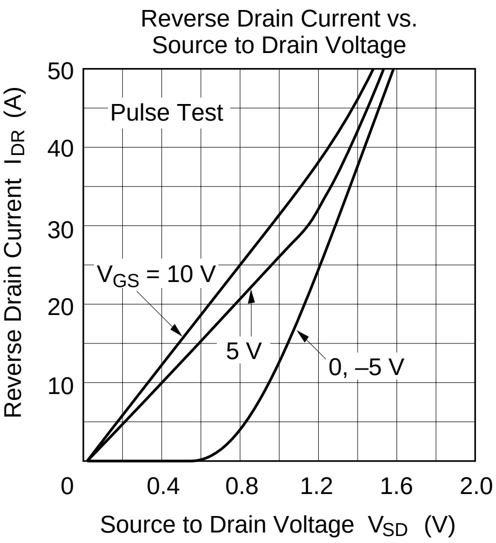

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance
|yfs| (S)
100
50
20
10
5
2
1
0.5
1
2
5
10
20
50
Drain Current I_D (A)
V_DS = 10 V
Pulse Test
Tc = –25°C
25°C
75°C

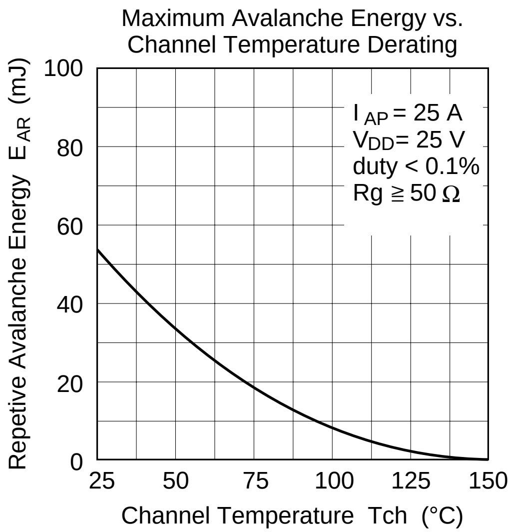

Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs, VGS = 0
Ta = 25°C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
VGS
VDD = 50 V
25 V
10 V
VDS
ID = 25 A
VDD = 50 V
25 V
10 V
Drain to Source Voltage VDS (V)
100
80
60
40
20
0
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
0
20
40
60
80
100
Gate Charge Qg (nc)

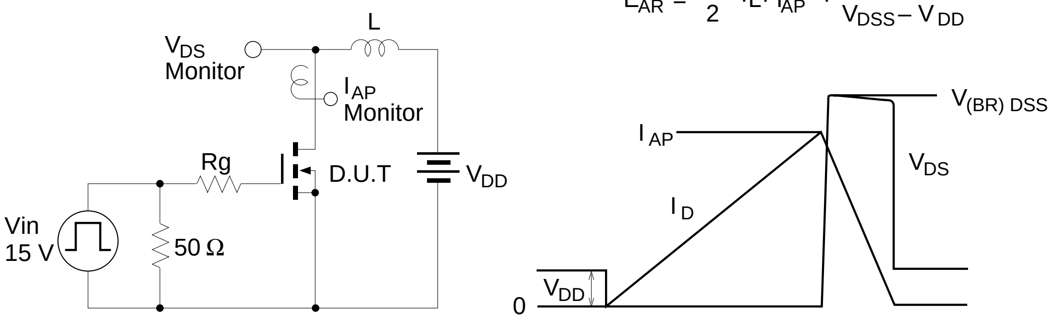

Switching Characteristics
VGS = 10 V, VDD ≒ 30 V
PW = 2 µs, duty ≦ 1%
td (off)
tf
tr
td (on)
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50
Drain Current ID (A)





Avalanche Test Circuit and Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



2SK1918(L), 2SK1918(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

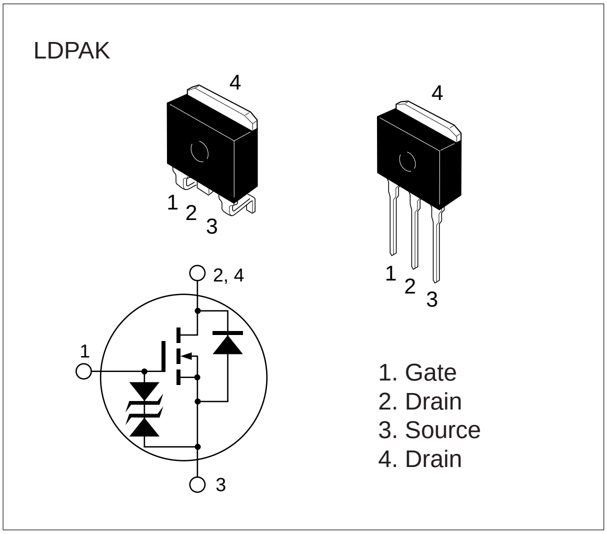


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$*	100	A
Body–drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP}***	25	A
Avalanche energy	E_{AR}***	53	mJ
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

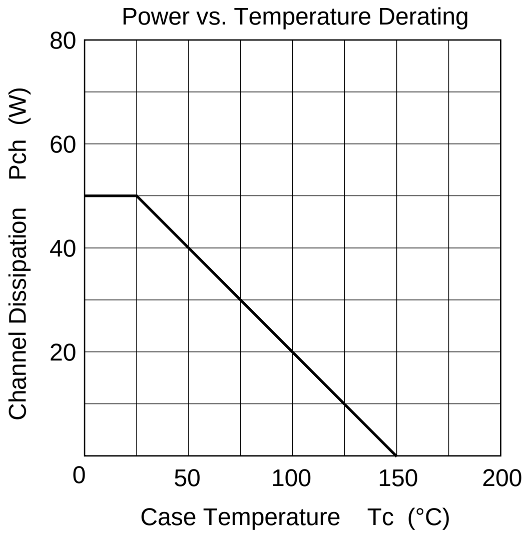
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.04	Ω	I_D = 15 A V_{GS} = 10 V *
		—	0.043	0.06	Ω	I_D = 15 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	21	—	S	I_D = 15 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	655	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	195	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 15 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	225	—	ns	R_L = 2 Ω
Fall time	t_f	—	145	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 25 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 25 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristics curves of 2SK1910


Power vs. Temperature Derating
80
60
40
20
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

2SK1919(L), 2SK1919(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

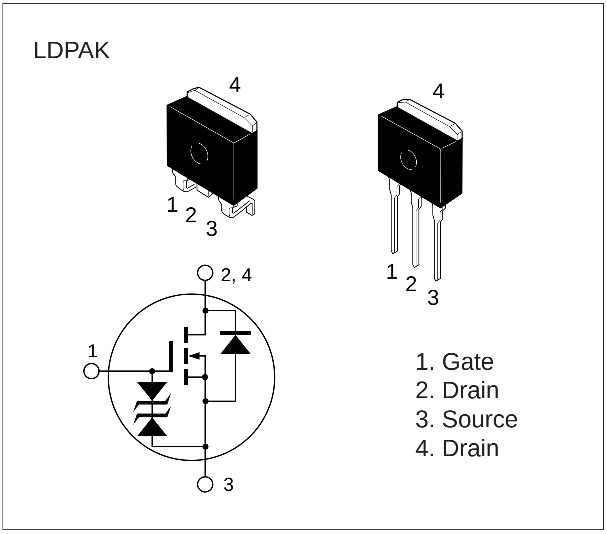


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*	160	A
Body–drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP}***	40	A
Avalanche energy	E_{AR}***	137	mJ
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.018	0.022	Ω	I_D = 20 A V_{GS} = 10 V *
		—	0.023	0.028	Ω	I_D = 20 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	22	35	—	S	I_D = 20 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3530	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1480	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	33	—	ns	I_D = 20 A
Rise time	t_r	—	155	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	450	—	ns	R_L = 1.5 Ω
Fall time	t_f	—	220	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 40 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curves of 2SK1911

2SK1933

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- No secondary breakdown
- Suitable for Switching regulator

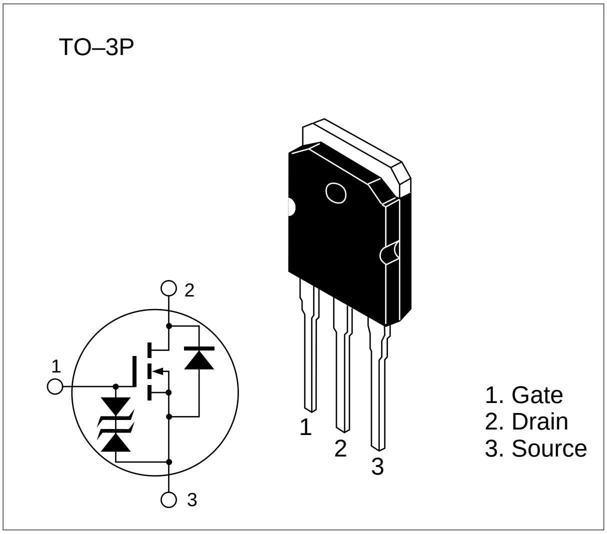


Table 1 Absolute Maximum Ratings (Ta = 25°C)

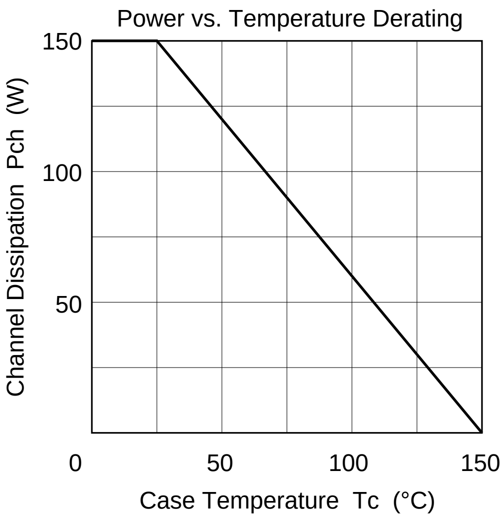
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	900	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	30	A
Body–drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	150	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

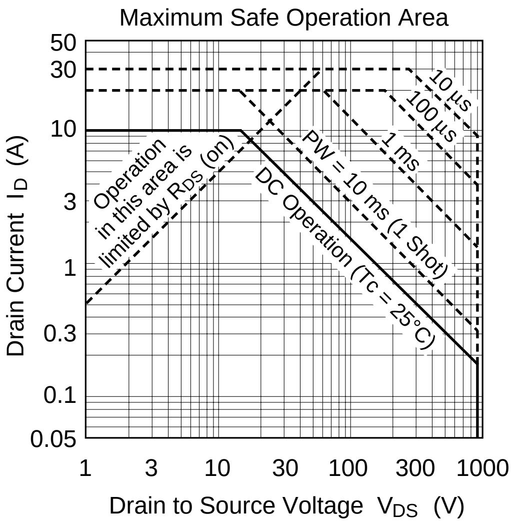
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

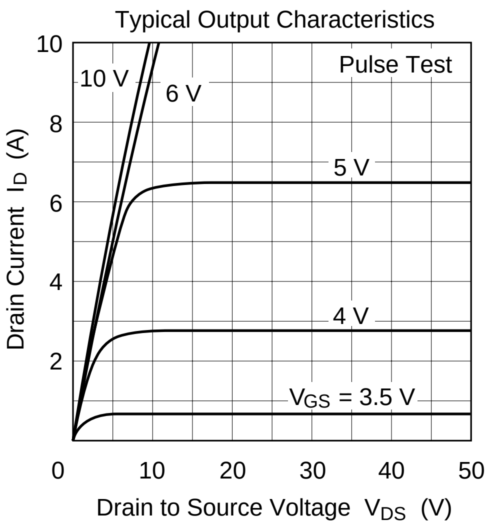
Table 2 Electrical Characteristics (Ta = 25°C)

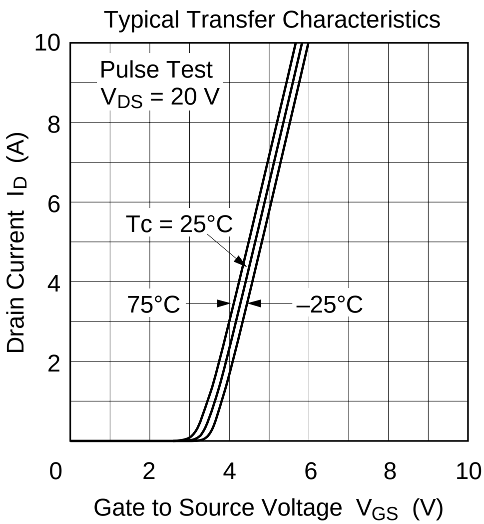
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	900	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 720 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.9	1.2	Ω	I_D = 5 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	4.5	7	—	S	I_D = 5 A V_{DS} = 20 V *
Input capacitance	Ciss	—	2620	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	830	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	320	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 5 A
Rise time	t_r	—	140	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	285	—	ns	R_L = 6 Ω
Fall time	t_f	—	170	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	1600	—	ns	I_F = 10 A, V_{GS} = 0, diF / dt = 100 A / µs

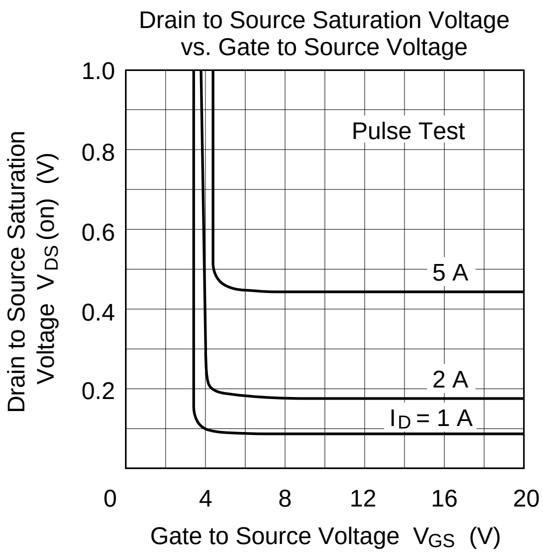
* Pulse Test

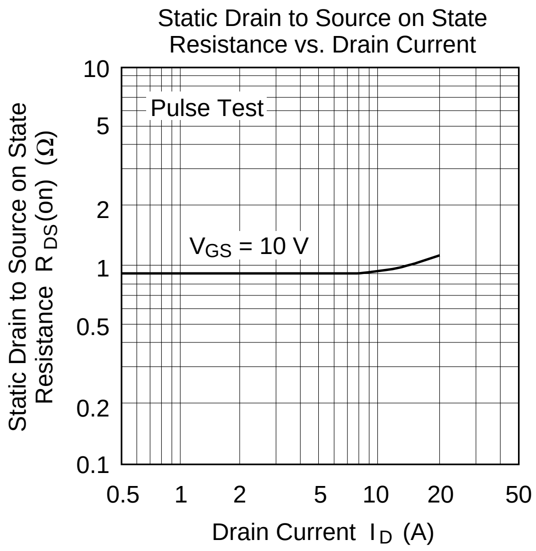

Power vs. Temperature Derating
150
100
50
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

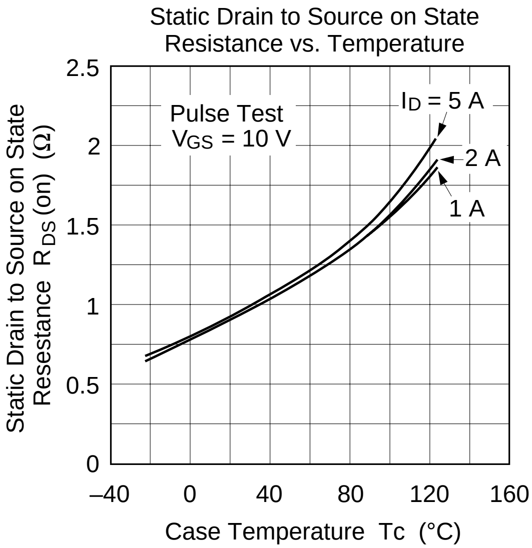

Maximum Safe Operation Area
50
30
10
3
1
0.3
0.1
0.05
1
3
10
30
100
300
1000
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_{DS} (on)

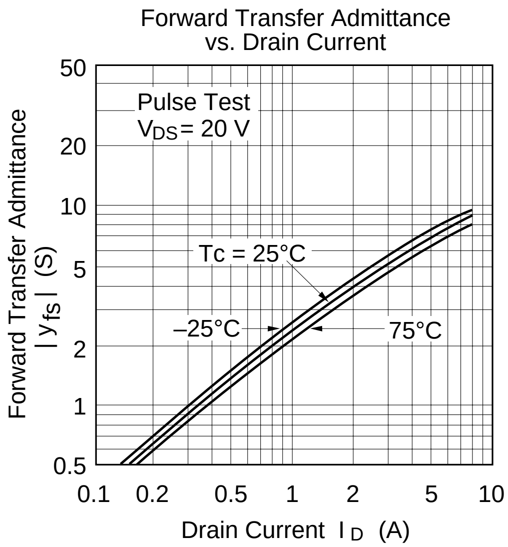

Typical Output Characteristics
10
8
6
4
2
0
10
20
30
40
50
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
Pulse Test
10 V
6 V
5 V
4 V
V_{GS} = 3.5 V

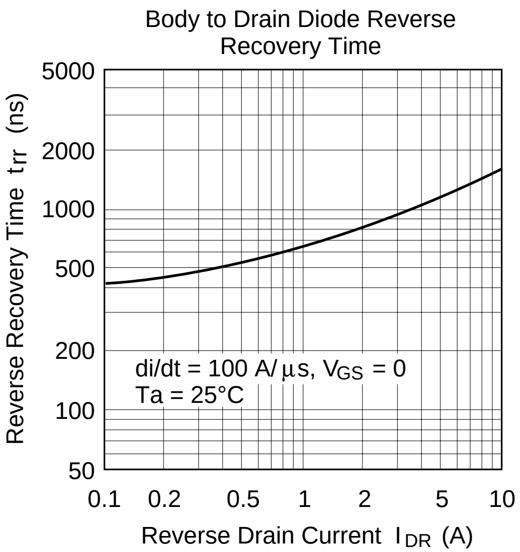

Typical Transfer Characteristics
10
8
6
4
2
0
2
4
6
8
10
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)
Pulse Test
V_{DS} = 20 V
Tc = 25°C
75°C
–25°C

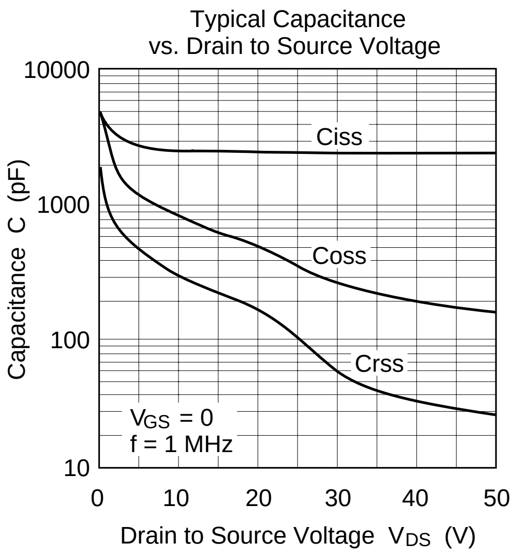

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
5 A
2 A
I_D = 1 A
Drain to Source Saturation Voltage $V_{DS(on)}$ (V)
1.0
0.8
0.6
0.4
0.2
0
4
8
12
16
20
Gate to Source Voltage V_{GS} (V)

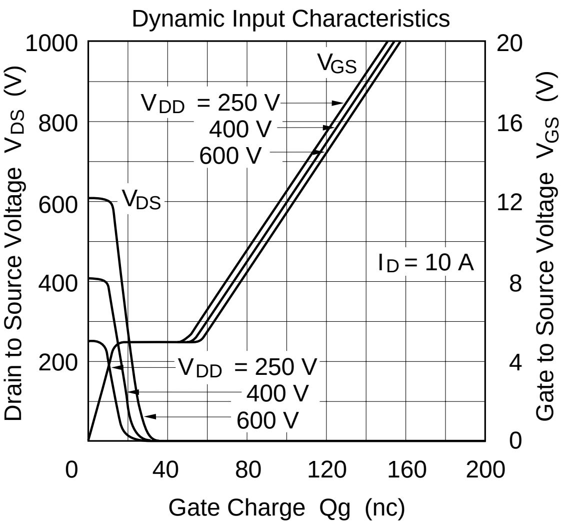

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 10 V
Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)
10
5
2
1
0.5
0.2
0.1
0.5
1
2
5
10
20
50
Drain Current I_D (A)

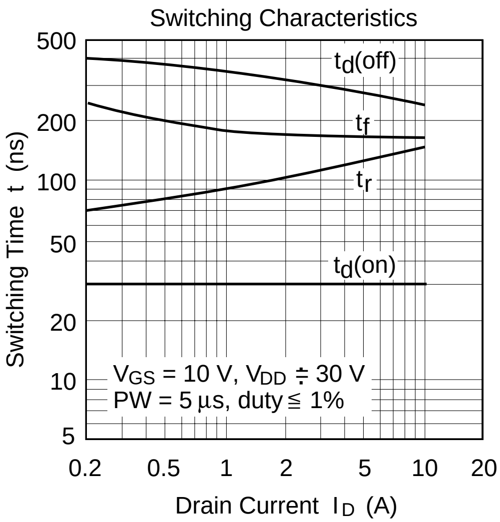

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
V_{GS} = 10 V
I_D = 5 A
2 A
1 A
Static Drain to Source on State Resestance $R_{DS(on)}$ (Ω)
2.5
2
1.5
1
0.5
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

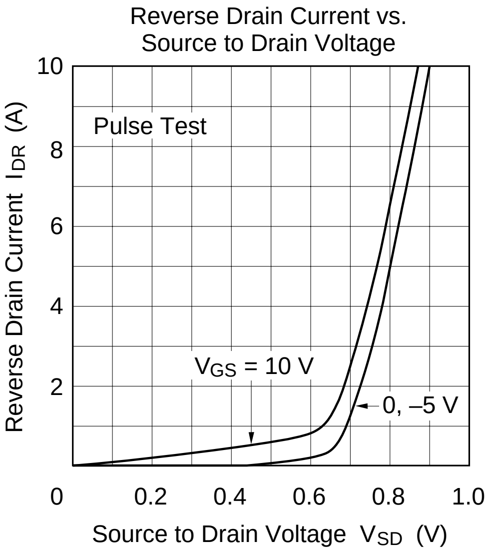

Forward Transfer Admittance
vs. Drain Current
Pulse Test
V_{DS} = 20 V
Tc = 25°C
–25°C
75°C
Forward Transfer Admittance $|y_{fs}|$ (S)
50
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Drain Current I_D (A)


Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
5000
2000
1000
500
200
100
50
di/dt = 100 A/µs, VGS = 0
Ta = 25°C
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
1000
800
600
400
200
VGS
VDD = 250 V
400 V
600 V
VDS
ID = 10 A
VDD = 250 V
400 V
600 V
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
td(off)
tf
tr
td(on)
VGS = 10 V, VDD ≑ 30 V
PW = 5 µs, duty ≦ 1%
0.2
0.5
1
2
5
10
20
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
2
4
6
8
10
0.2
0.4
0.6
0.8
1.0

2SK1934

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- No secondary breakdown
- Suitable for Switching regulator

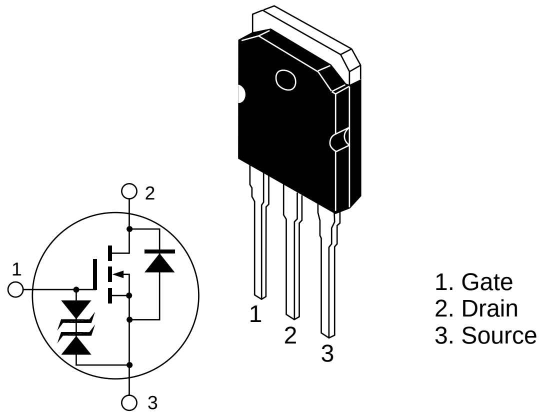


Table 1 Absolute Maximum Ratings (Ta = 25°C)

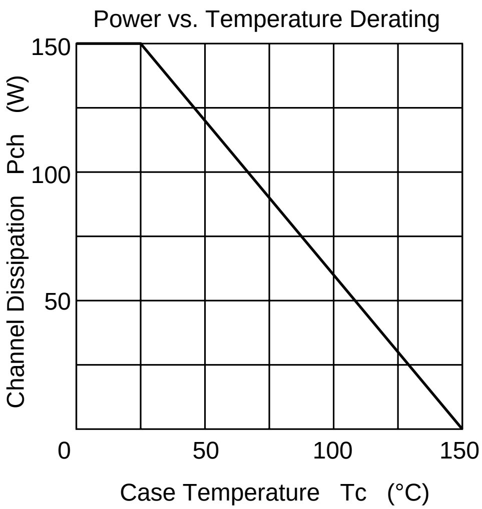
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1000	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}$*	24	A
Body–drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	Pch**	150	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

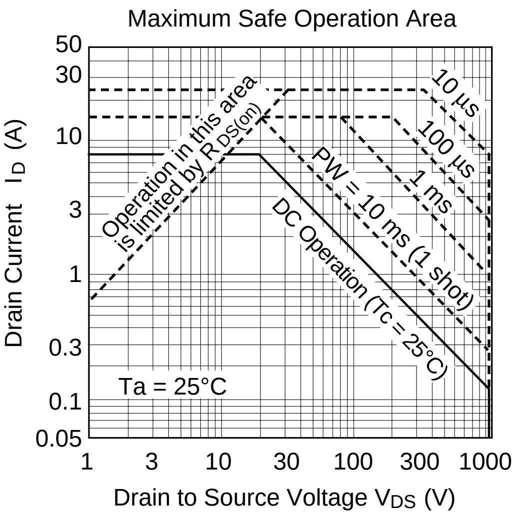
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

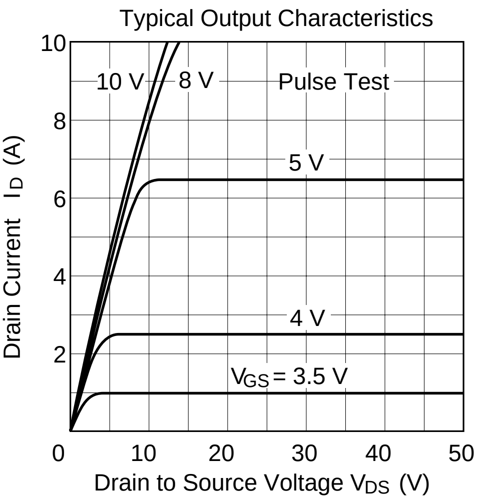
Table 2 Electrical Characteristics (Ta = 25°C)

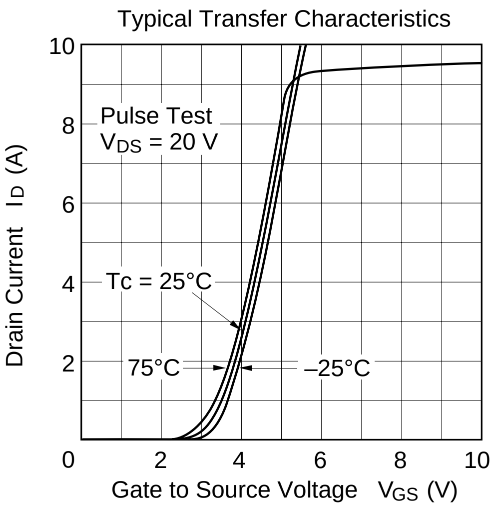
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1000	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 800 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.2	1.6	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	4	6	—	S	I_D = 4 A V_{DS} = 20 V *
Input capacitance	Ciss	—	2690	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	920	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	375	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	35	—	ns	I_D = 4 A
Rise time	t_r	—	135	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	300	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	205	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	1600	—	µs	I_F = 8 A, V_{GS} = 0, diF / dt = 100 A / µs

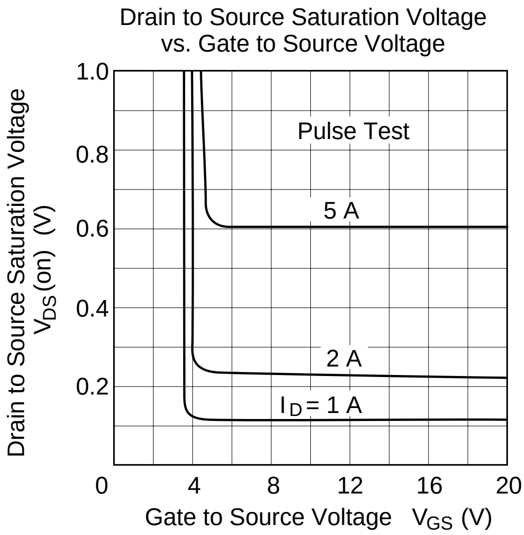
* Pulse Test

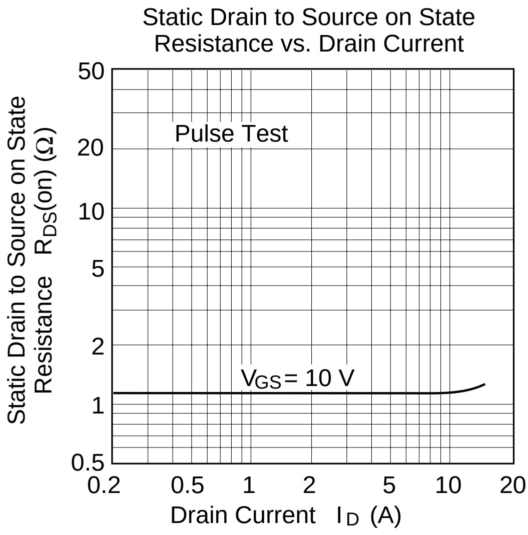

Power vs. Temperature Derating
Channel Dissipation Pch (W)
150
100
50
0
50
100
150
Case Temperature Tc (°C)

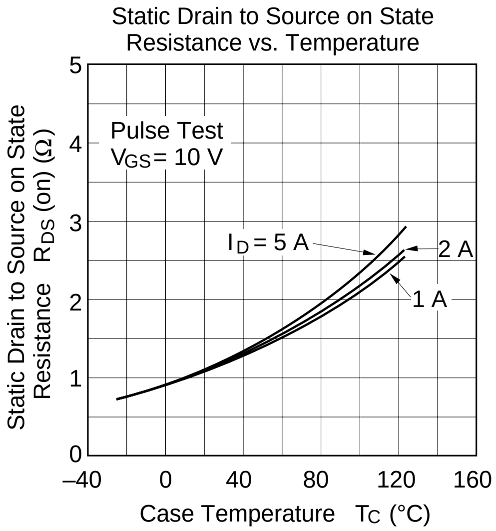

Maximum Safe Operation Area
Drain Current ID (A)
50
30
10
3
1
0.3
0.1
0.05
Operation in this area is limited by RDS(on)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Ta = 25°C
1
3
10
30
100
300
1000
Drain to Source Voltage VDS (V)

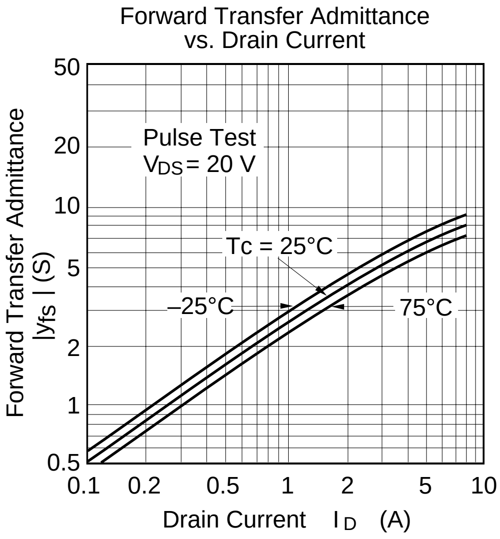

Typical Output Characteristics
Drain Current ID (A)
10
8
6
4
2
10 V
8 V
Pulse Test
5 V
4 V
VGS = 3.5 V
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

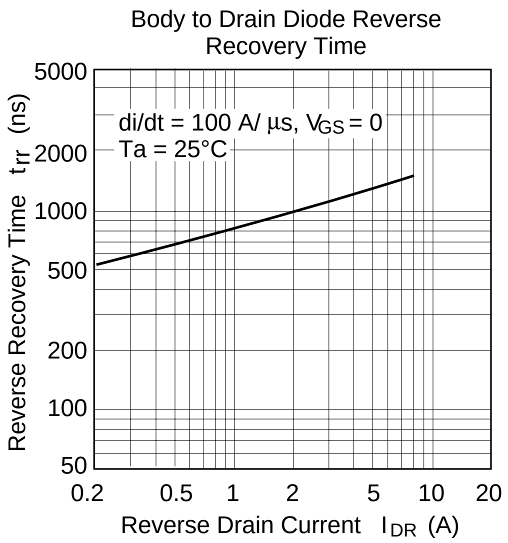

Typical Transfer Characteristics
Drain Current ID (A)
10
8
6
4
2
Pulse Test
VDS = 20 V
Tc = 25°C
75°C
–25°C
0
2
4
6
8
10
Gate to Source Voltage VGS (V)

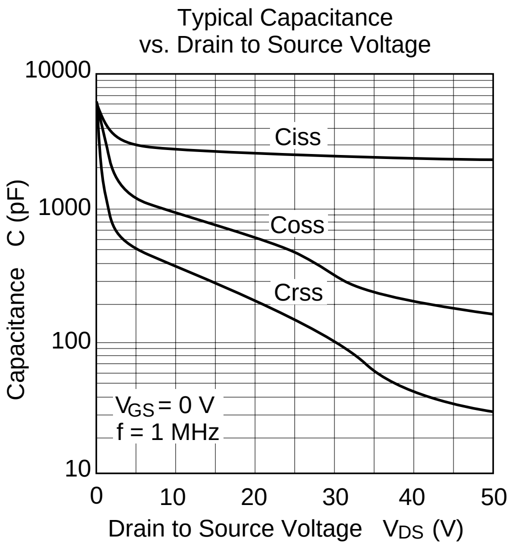

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
5 A
2 A
I D = 1 A
1.0
0.8
0.6
0.4
0.2
0
4
8
12
16
20
Drain to Source Saturation Voltage
VDS(on) (V)
Gate to Source Voltage VGS (V)

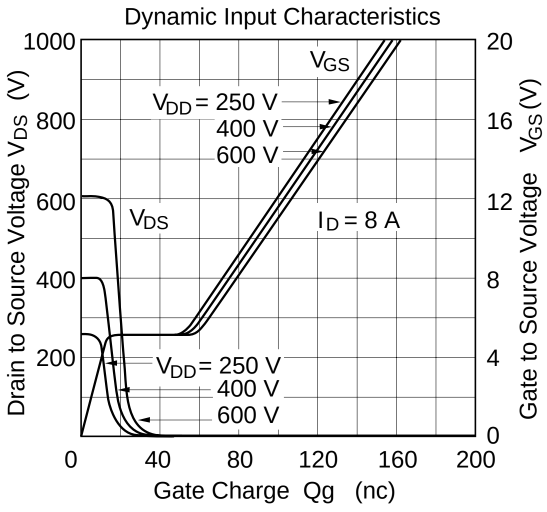

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
VGS = 10 V
50
20
10
5
2
1
0.5
0.2
0.5
1
2
5
10
20
Static Drain to Source on State
Resistance RDS(on) (Ω)
Drain Current I D (A)

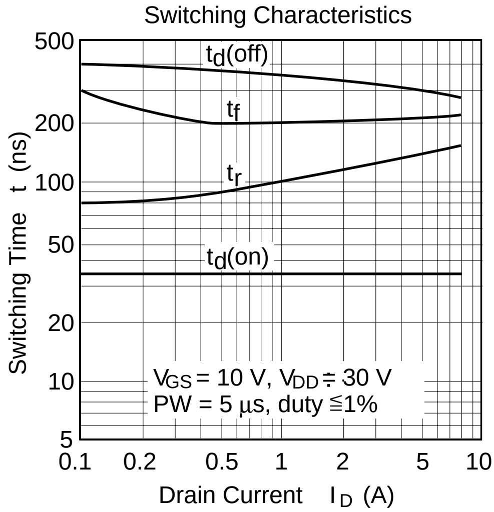

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
VGS = 10 V
I D = 5 A
2 A
1 A
5
4
3
2
1
0
–40
0
40
80
120
160
Static Drain to Source on State
Resistance RDS (on) (Ω)
Case Temperature TC (°C)

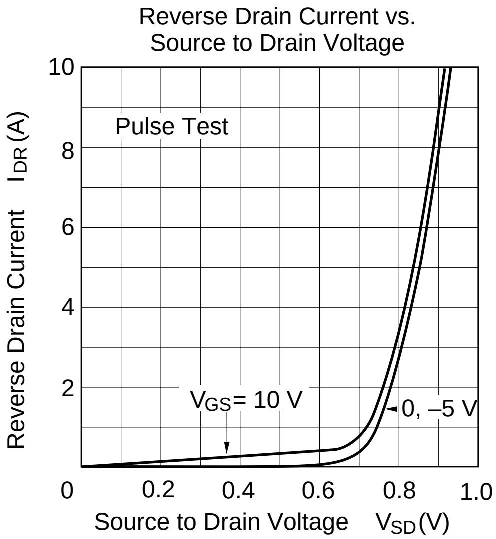

Forward Transfer Admittance
vs. Drain Current
Pulse Test
VDS = 20 V
Tc = 25°C
–25°C
75°C
50
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Forward Transfer Admittance
|yfs | (S)
Drain Current I D (A)


Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/ µs, VGS = 0
Ta = 25°C
Reverse Recovery Time trr (ns)
5000
2000
1000
500
200
100
50
0.2
0.5
1
2
5
10
20
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0 V
f = 1 MHz
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
VGS
VDD = 250 V
400 V
600 V
VDS
ID = 8 A
VDD = 250 V
400 V
600 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
1000
800
600
400
200
20
16
12
8
4
0
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
td(off)
tf
tr
td(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦1%
Switching Time t (ns)
500
200
100
50
20
10
5
0.1
0.2
0.5
1
2
5
10
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
10
8
6
4
2
0
0.2
0.4
0.6
0.8
1.0

2SK1947

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low Drive Current
- Built–In Fast Recovery Diode (t_{rr} = 140 ns)
- Suitable for Switching regulator,
  Motor Control

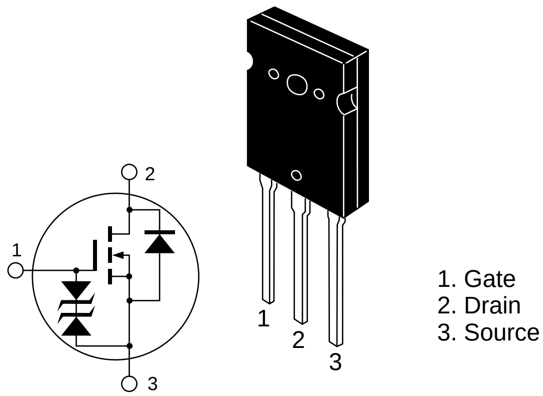


Table 1 Absolute Maximum Ratings (Ta = 25°C)

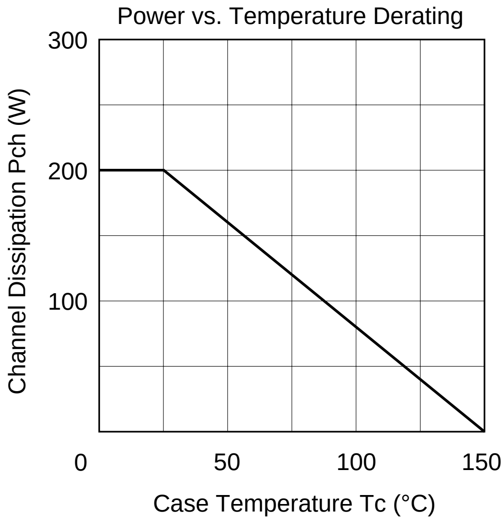
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$*	200	A
Body–drain diode reverse drain current	I_{DR}	50	A
Channel dissipation	Pch**	200	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

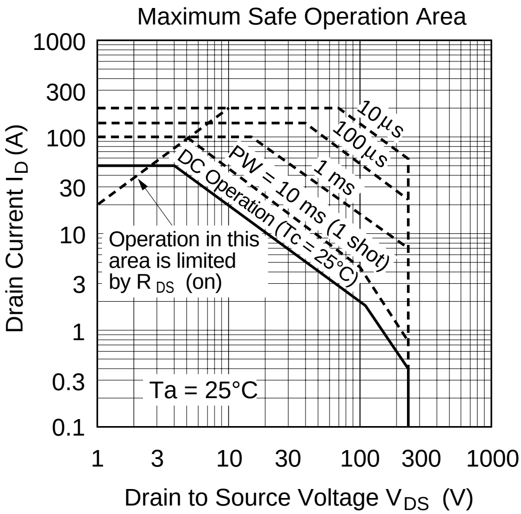
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

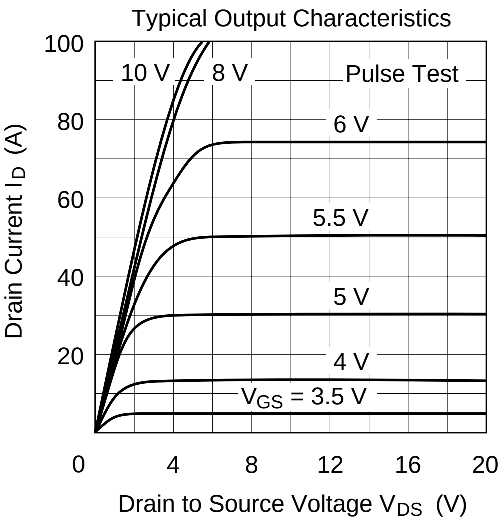
Table 2 Electrical Characteristics (Ta = 25°C)

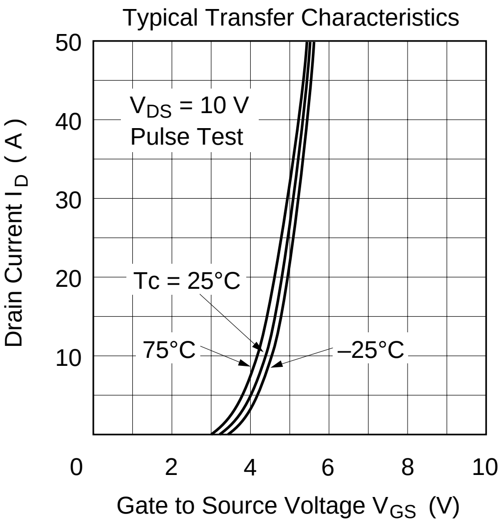
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.047	0.06	Ω	I_D = 25 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	20	30	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	5810	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	2360	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	270	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	75	—	ns	I_D = 25 A
Rise time	t_r	—	270	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	420	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	200	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 50 A, V_{GS} = 0, diF / dt = 100 A / µs

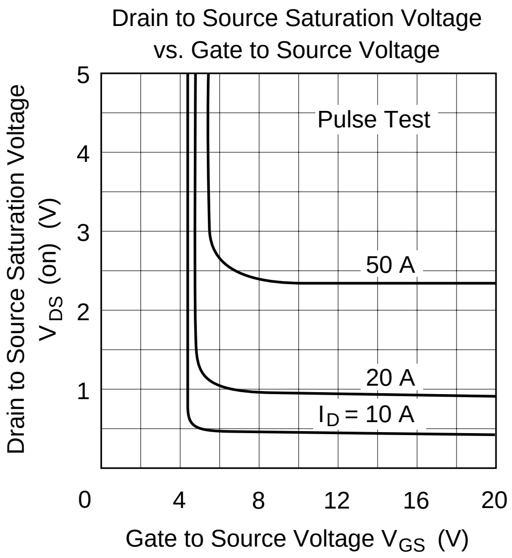
* Pulse Test

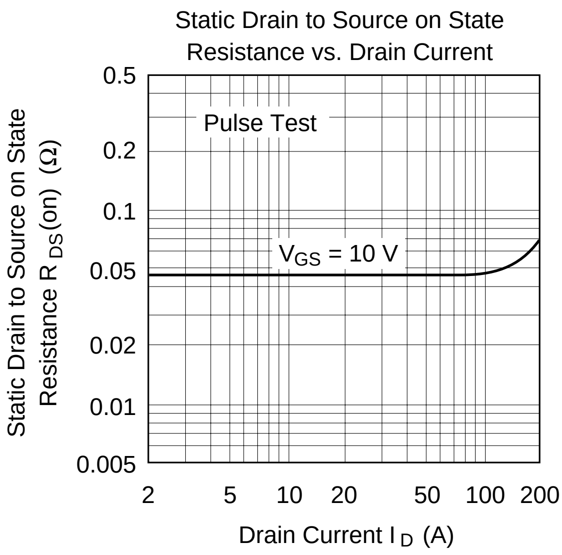

Power vs. Temperature Derating
Channel Dissipation Pch (W)
300
200
100
0
50
100
150
Case Temperature Tc (°C)

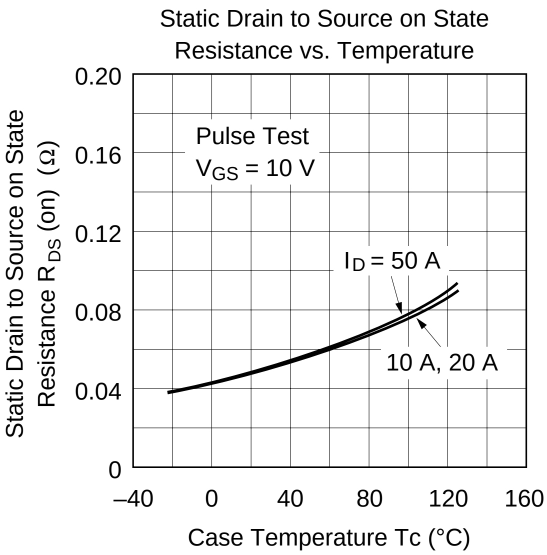

Maximum Safe Operation Area
Drain Current I_D (A)
1000
300
100
30
10
3
1
0.3
0.1
10 μs
100 μs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_{DS} (on)
Ta = 25°C
1
3
10
30
100
300
1000
Drain to Source Voltage V_{DS} (V)

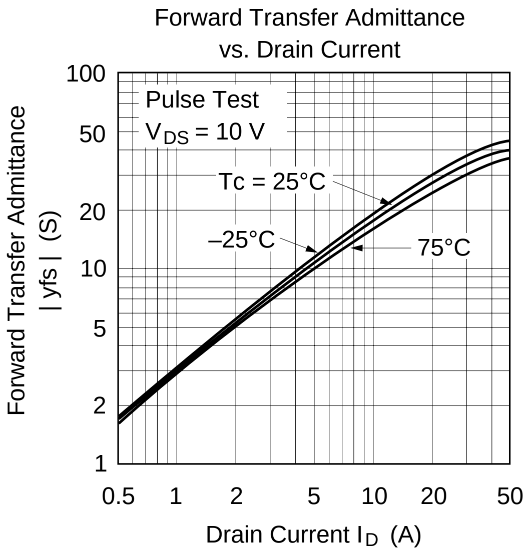

Typical Output Characteristics
Drain Current I_D (A)
100
80
60
40
20
10 V
8 V
Pulse Test
6 V
5.5 V
5 V
4 V
V_{GS} = 3.5 V
0
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)

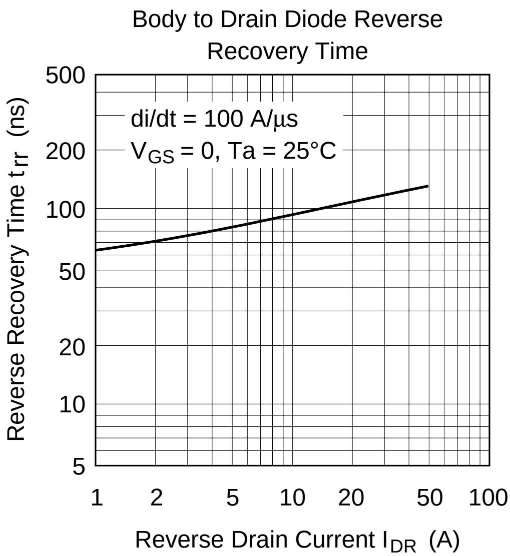

Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
V_{DS} = 10 V
Pulse Test
Tc = 25°C
75°C
–25°C
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)


Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
V DS (on) (V)
Pulse Test
50 A
20 A
I D = 10 A
0
4
8
12
16
20
1
2
3
4
5
Gate to Source Voltage V GS (V)

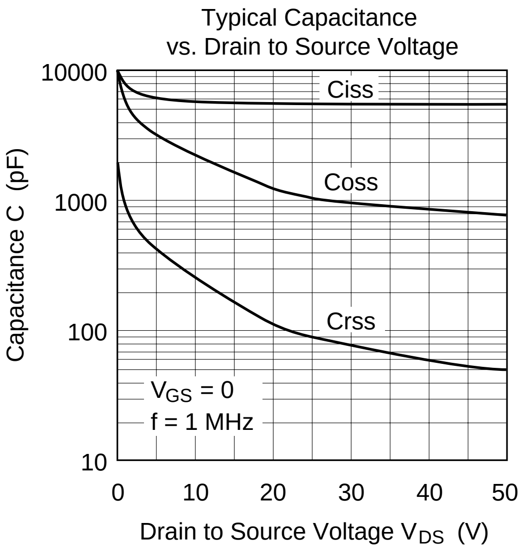

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State
Resistance R DS(on) (Ω)
Pulse Test
V GS = 10 V
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200
Drain Current I D (A)


Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State
Resistance R DS (on) (Ω)
Pulse Test
V GS = 10 V
I D = 50 A
10 A, 20 A
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

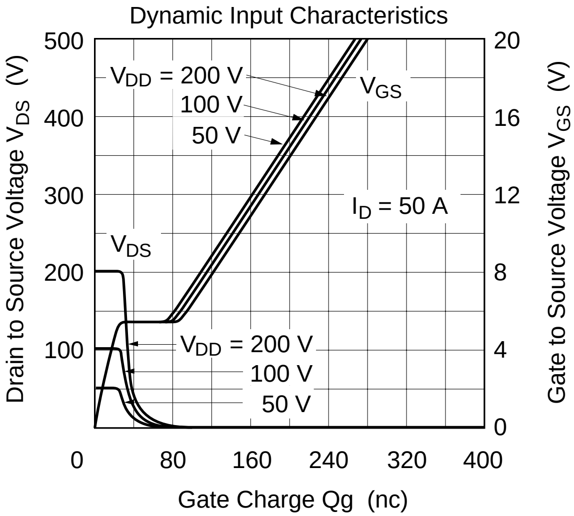

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance
| yfs | (S)
Pulse Test
V DS = 10 V
Tc = 25°C
–25°C
75°C
100
50
20
10
5
2
1
0.5
1
2
5
10
20
50
Drain Current I D (A)



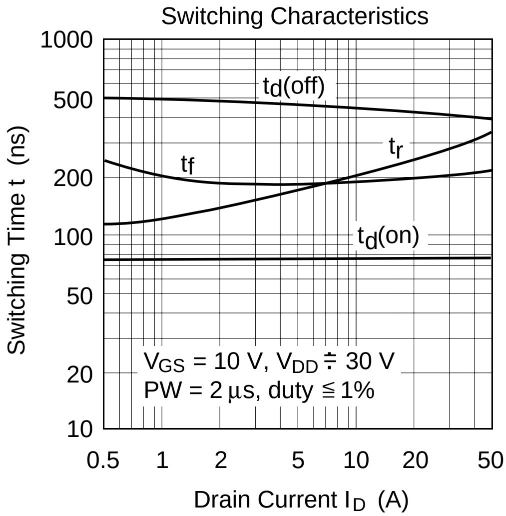
Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/µs
VGS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
1
2
5
10
20
50
100
Reverse Drain Current IDR (A)



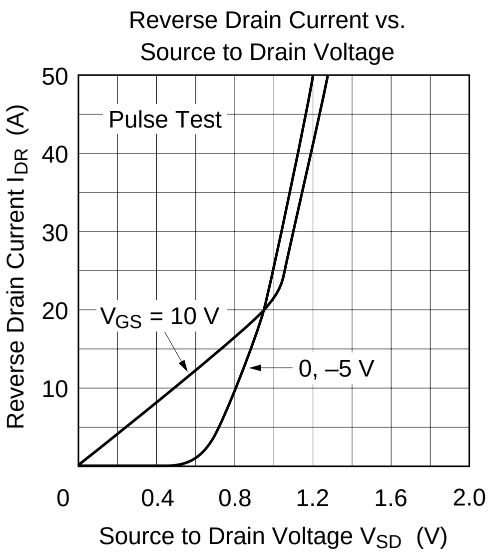
Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)



Dynamic Input Characteristics
VDD = 200 V
100 V
50 V
VGS
ID = 50 A
VDS
VDD = 200 V
100 V
50 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
500
400
300
200
100
0
20
16
12
8
4
0
80
160
240
320
400
Gate Charge Qg (nc)



Switching Characteristics
td(off)
tf
tr
td(on)
VGS = 10 V, VDD ≒ 30 V
PW = 2 µs, duty ≦ 1%
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
0, –5 V
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)

2SK1948

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low Drive Current
- No Secondary Breakdown
- Suitable for Switching regulator, Motor Control

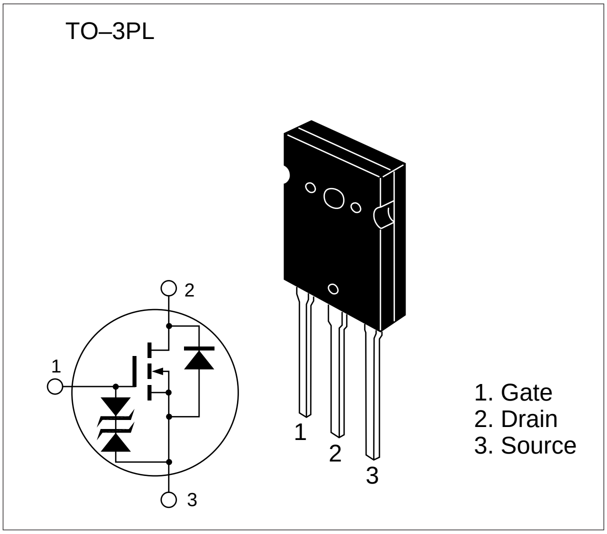


Table 1 Absolute Maximum Ratings (Ta = 25°C)

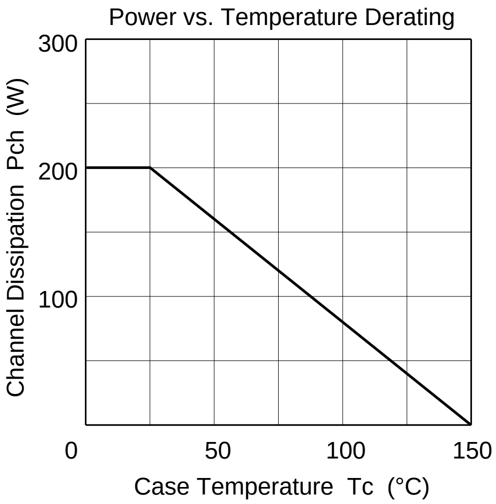
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$*	200	A
Body–drain diode reverse drain current	I_{DR}	50	A
Channel dissipation	Pch**	200	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

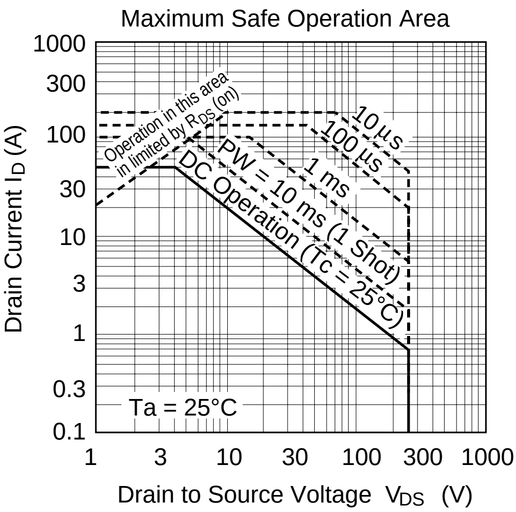
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

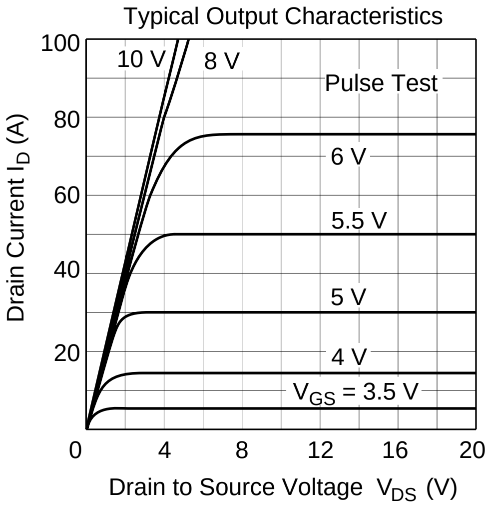
Table 2 Electrical Characteristics (Ta = 25°C)

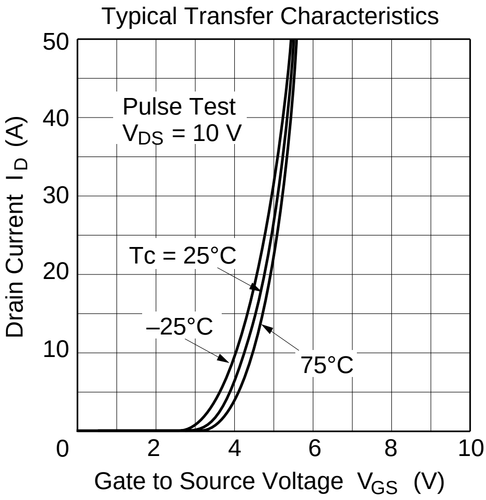
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.047	0.06	Ω	I_D = 25 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	20	30	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	5830	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	2310	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	265	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	70	—	ns	I_D = 25 A
Rise time	t_r	—	260	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	430	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	190	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	450	—	ns	I_F = 50 A, V_{GS} = 0, diF / dt = 100 A / µs

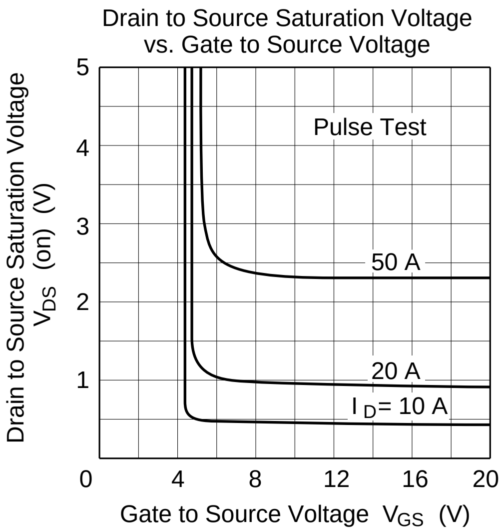
* Pulse Test

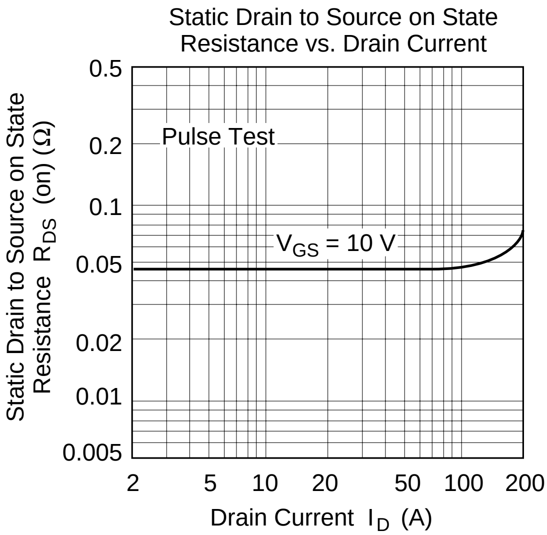

Power vs. Temperature Derating
300
200
100
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

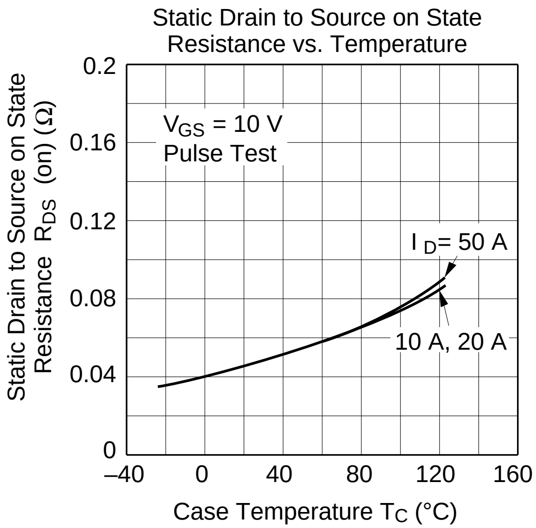

Maximum Safe Operation Area
1000
300
100
30
10
3
1
0.3
0.1
1
3
10
30
100
300
1000
Operation in this area
is limited by $R_{DS (on)}$
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

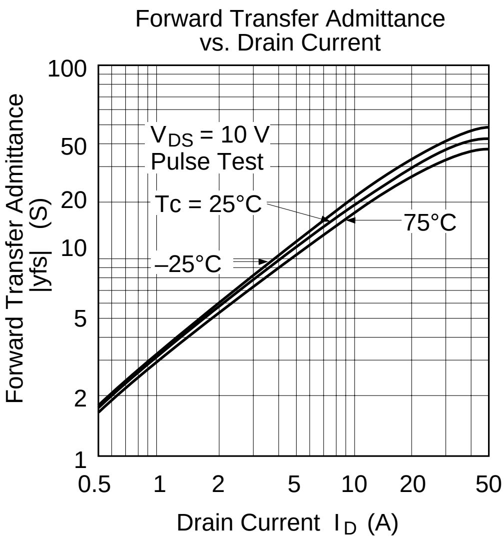

Typical Output Characteristics
100
80
60
40
20
0
4
8
12
16
20
10 V
8 V
Pulse Test
6 V
5.5 V
5 V
4 V
V_{GS} = 3.5 V
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

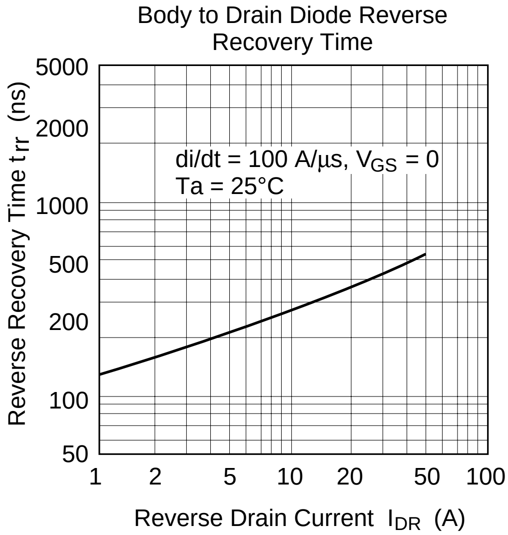

Typical Transfer Characteristics
50
40
30
20
10
0
2
4
6
8
10
Pulse Test
V_{DS} = 10 V
Tc = 25°C
–25°C
75°C
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

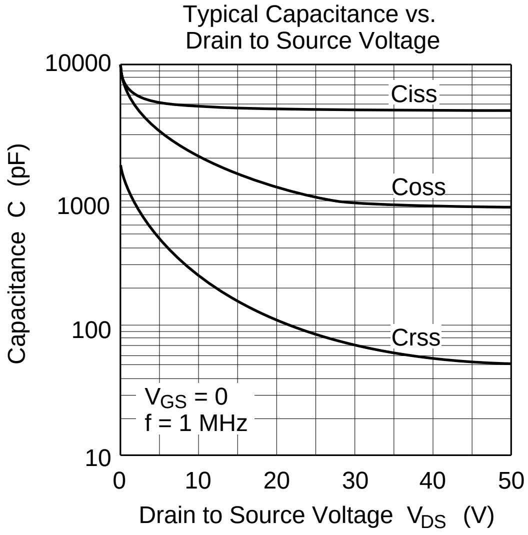

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
V_{DS} (on) (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
50 A
20 A
I_D = 10 A
0
4
8
12
16
20
1
2
3
4
5

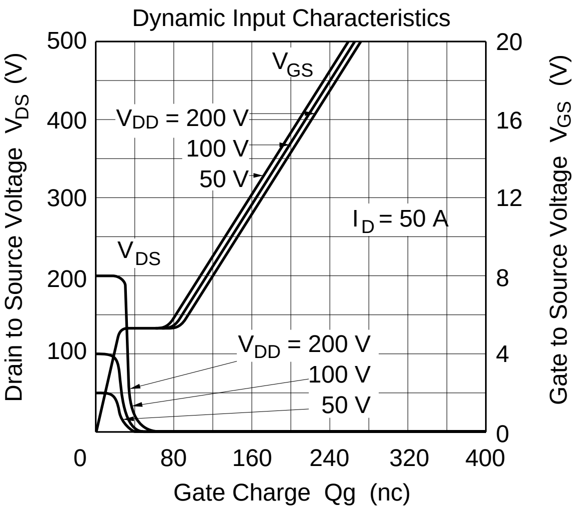

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State
Resistance R_{DS} (on) (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 10 V
0.5
0.2
0.1
0.05
0.02
0.01
0.005
2
5
10
20
50
100
200

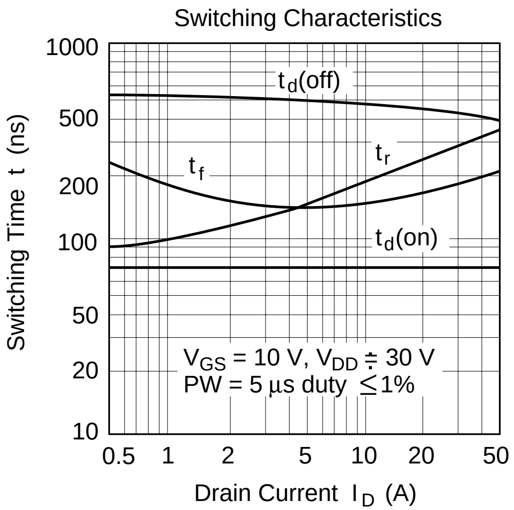

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State
Resistance R_{DS} (on) (Ω)
Case Temperature T_C (°C)
V_{GS} = 10 V
Pulse Test
I_D = 50 A
10 A, 20 A
0.2
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160

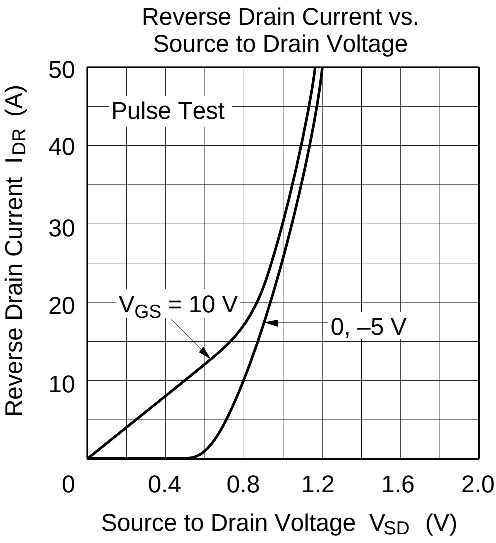

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance
|yfs| (S)
Drain Current I_D (A)
V_{DS} = 10 V
Pulse Test
Tc = 25°C
75°C
–25°C
100
50
20
10
5
2
1
0.5
1
2
5
10
20
50


Body to Drain Diode Reverse
Recovery Time
di/dt = 100 A/µs, VGS = 0
Ta = 25°C
Reverse Recovery Time trr (ns)
5000
2000
1000
500
200
100
50
1
2
5
10
20
50
100
Reverse Drain Current IDR (A)


Typical Capacitance vs.
Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
VGS
VDD = 200 V
100 V
50 V
ID = 50 A
VDS
VDD = 200 V
100 V
50 V
Drain to Source Voltage VDS (V)
500
400
300
200
100
0
80
160
240
320
400
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)


Switching Characteristics
td(off)
tf
tr
td(on)
VGS = 10 V, VDD ≑ 30 V
PW = 5 µs duty ≦1%
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50
Drain Current ID (A)

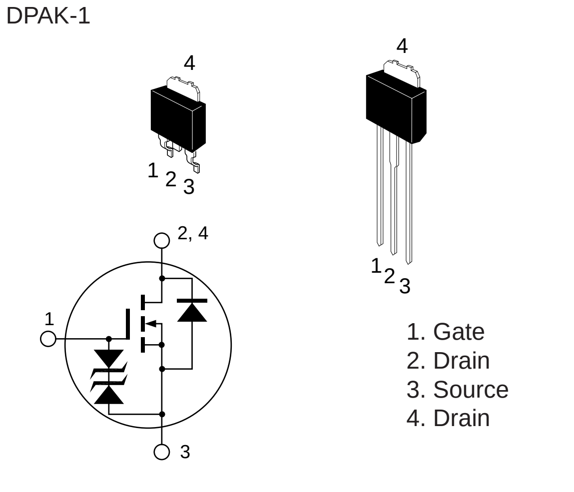

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
0, –5 V
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)

2SK1949(L), 2SK1949(S)

Silicon N Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	20	A
Body–drain diode reverse drain current	I_{DR}	5	A
Avalanche current	I_{AP}***	5	A
Avalanche energy	E_{AR}***	2.1	mJ
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

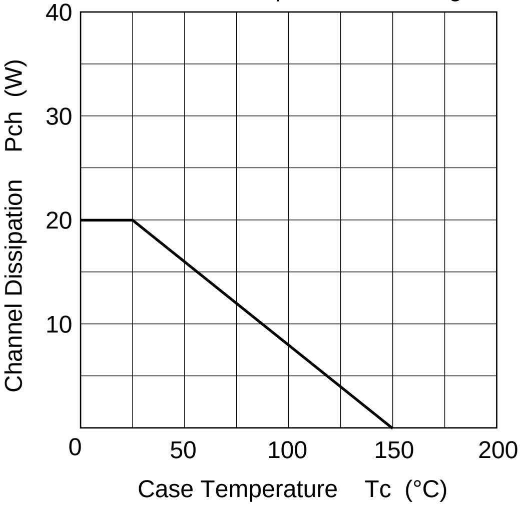
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

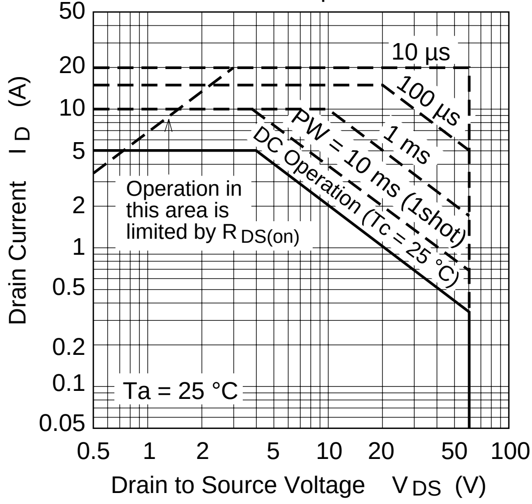
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 3 A V_{GS} = 10 V *
		—	0.15	0.2	Ω	I_D = 3 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	3	5.5	—	S	I_D = 3 A V_{DS} = 10 V *
Input capacitance	Ciss	—	390	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	190	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 3 A
Rise time	t_r	—	42	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	90	—	ns	R_L = 10 Ω
Fall time	t_f	—	55	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = 5 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

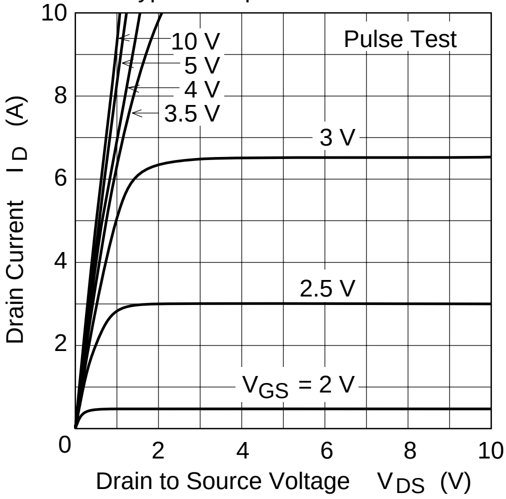
Power vs. Temperature Derating



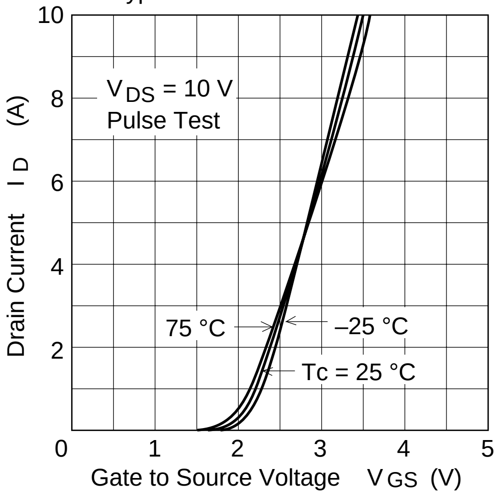
Maximum Safe Operation Area

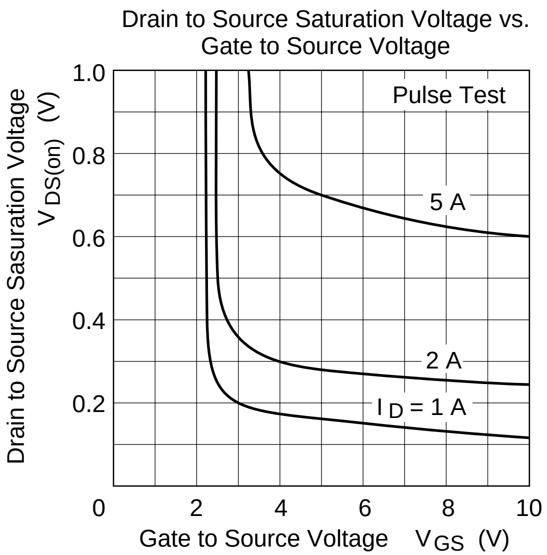


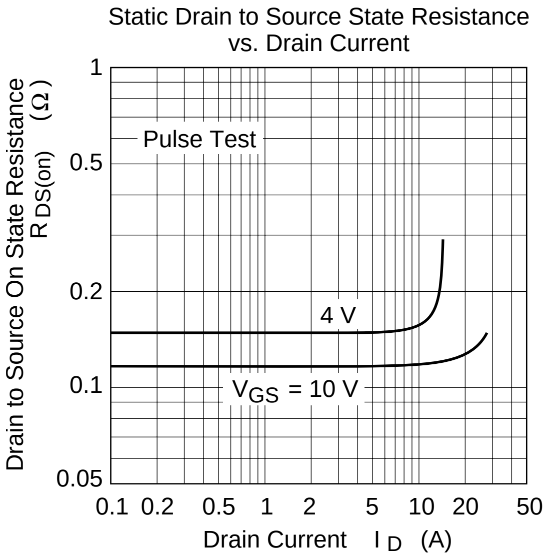
Typical Output Characteristics

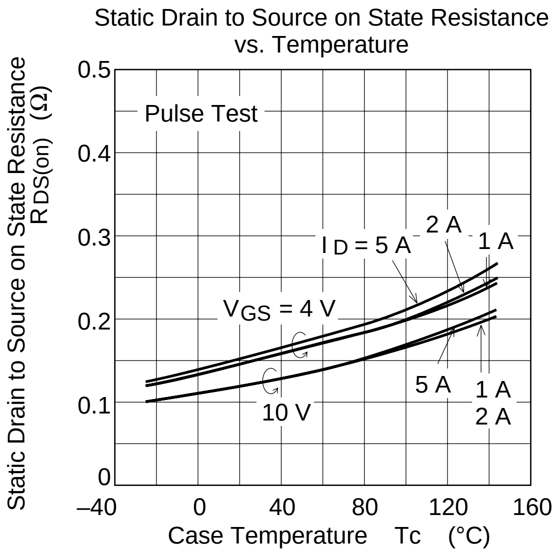


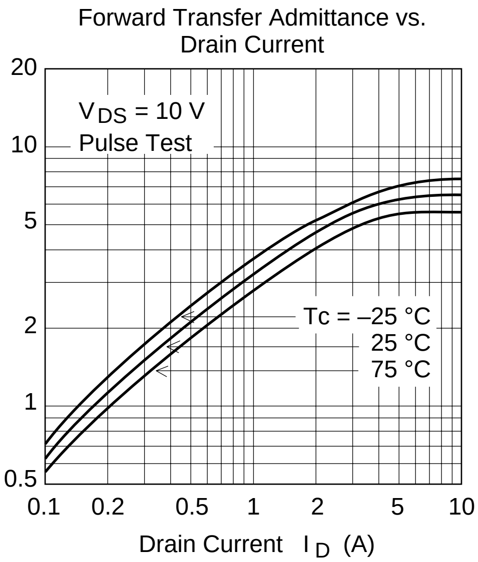
Typical Transfer Characteristics



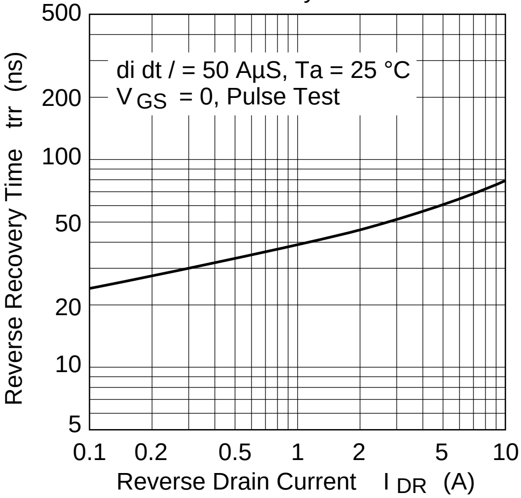

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
5 A
2 A
I D = 1 A
Drain to Source Sasuration Voltage
V DS(on) (V)
1.0
0.8
0.6
0.4
0.2
0
2
4
6
8
10
Gate to Source Voltage V GS (V)


Static Drain to Source State Resistance
vs. Drain Current
Pulse Test
4 V
VGS = 10 V
Drain to Source On State Resistance
R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.1
0.2
0.5
1
2
5
10
20
50
Drain Current I D (A)

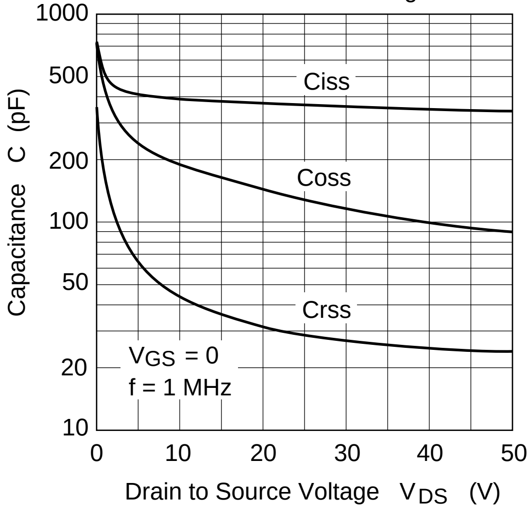

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 5 A
2 A
1 A
VGS = 4 V
10 V
5 A
1 A
2 A
Static Drain to Source on State Resistance
RDS(on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
VDS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

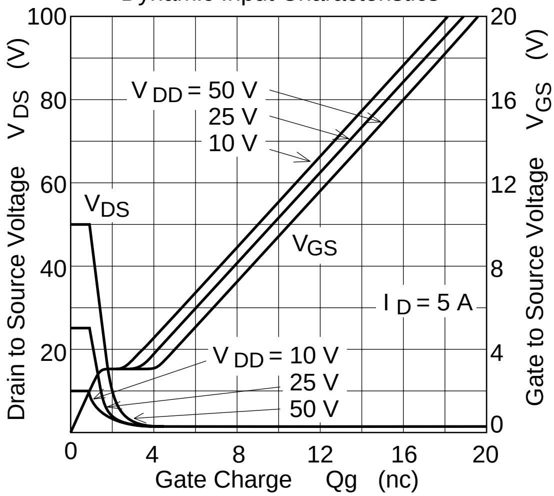
Body–Drain Diode Reverse Recovery Time



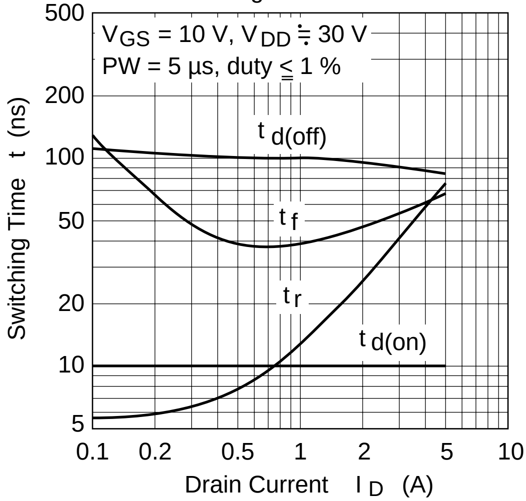
Typical Capacitance vs. Drain to Source Voltage



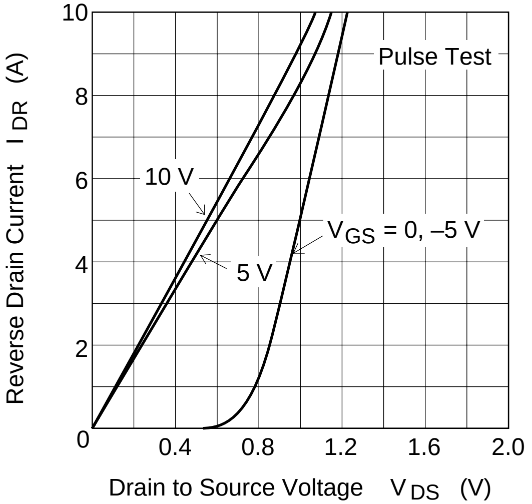
Dynamic Input Characteristics



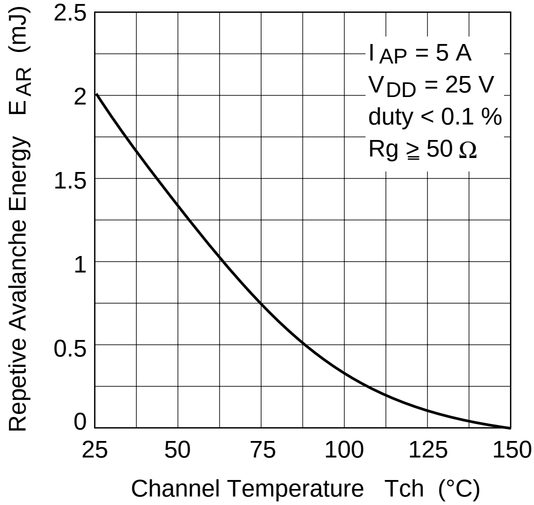
Switching Characteristics



Reverse Drain Current vs.
Souece to Drain Voltage

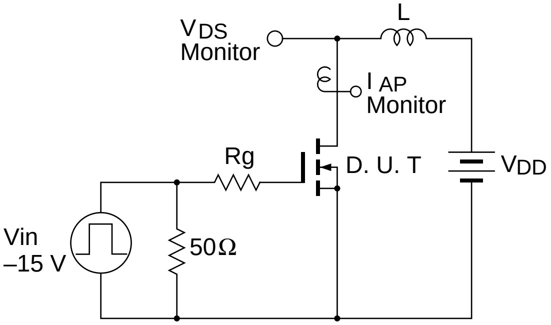


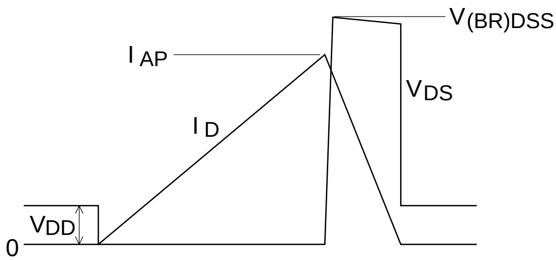
Maximun Avalanche Energy vs.
Channel Temperature Derating



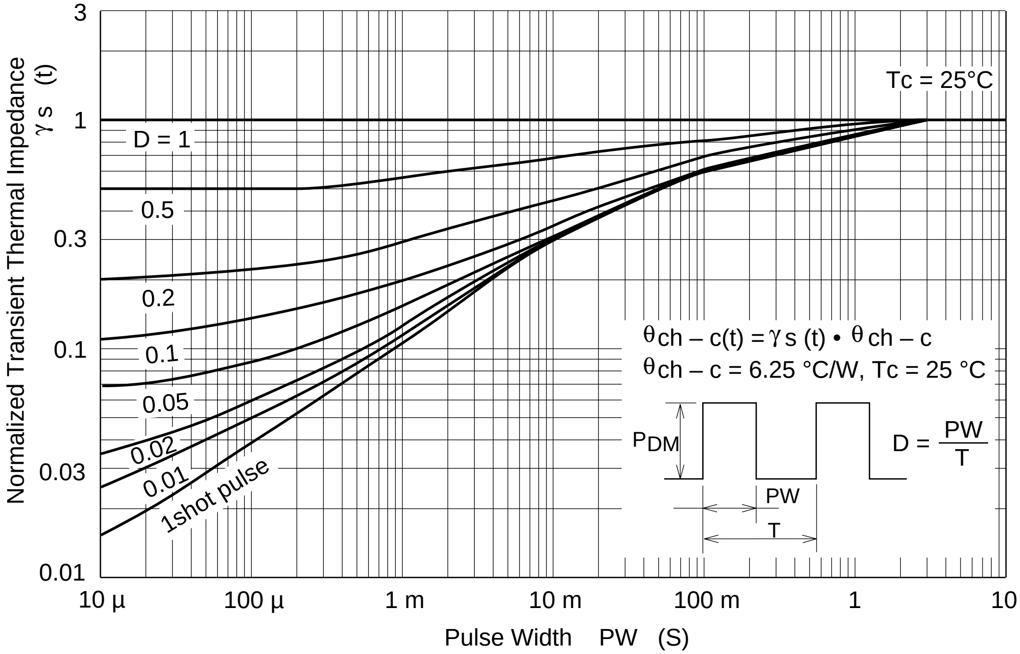
Avalanche Test Circuit and Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

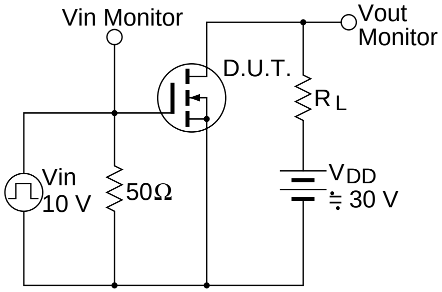




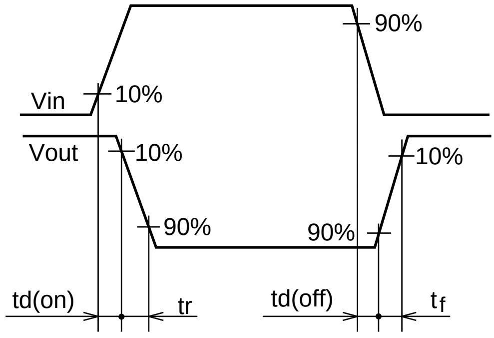
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveform



2SK1950

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device can be driven from 3 V source
- Suitable for Switching regulator, DC – DC converter

DPAK–1

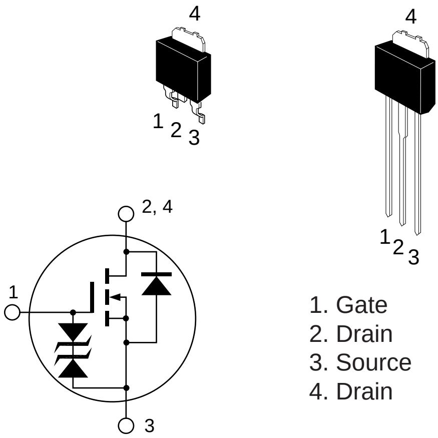


Table 1 Absolute Maximum Ratings (Ta = 25°C)

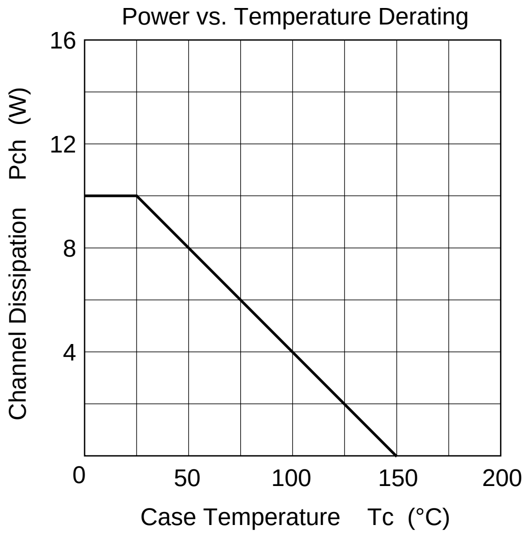
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$*	12	A
Body–drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	10	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.25	Ω	I_D = 2 A V_{GS} = 10 V *
		—	0.3	0.45	Ω	I_D = 0.6 A V_{GS} = 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	(6)	(10)	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(350)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(200)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(80)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(10)	—	ns	I_D = 2 A
Rise time	t_r	—	(50)	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(100)	—	ns	R_L = 15 Ω
Fall time	t_f	—	(60)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(1.2)	—	V	I_F = 3 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(100)	—	ns	I_F = 3 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
16
12
8
4
0
50
100
150
200
Case Temperature Tc (°C)

2SK1951

Silicon N Channel MOS FET

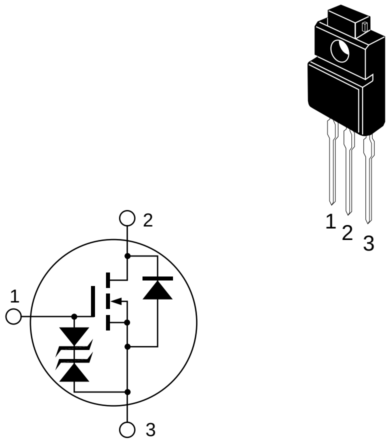
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

TO–220FM



1. Gate
2. Drain
3. Source

Table 1   Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}{}^{*}$	100	A
Body–drain diode reverse drain current	I_{DR}	25	A
Avalanche current	$I_{AP}{}^{***}$	25	A
Avalanche energy	$E_{AR}{}^{***}$	53	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

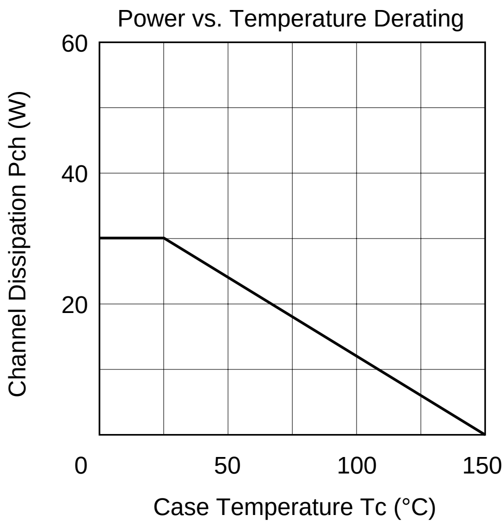
*   PW ≤ 10 μs, duty cycle ≤ 1 %
**   Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

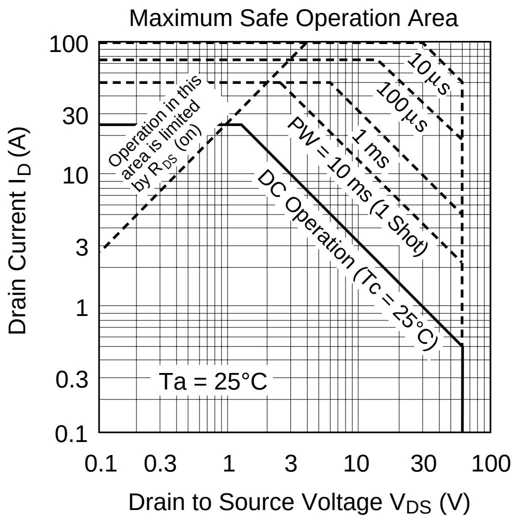
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.04	Ω	I_D = 15 A V_{GS} = 10 V *
		—	0.043	0.06	Ω	I_D = 15 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	21	—	S	I_D = 15 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	655	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	195	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 15 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	225	—	ns	R_L = 2 Ω
Fall time	t_f	—	145	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 25 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 25 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristics curves of 2SK1910


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1
0.3
0.1
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V_{DS} (V)
Operation in this area is limited by R_{DS} (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C

2SK1952

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

TO–220FM

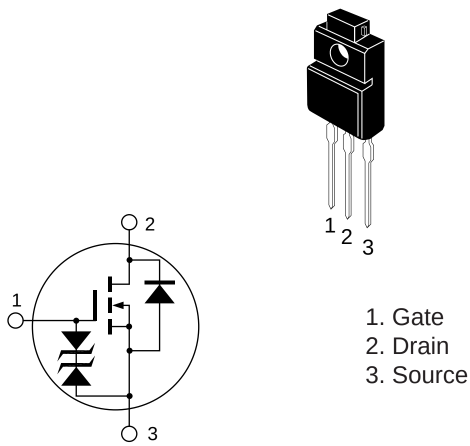


Table 1   Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*	160	A
Body–drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP}***	40	A
Avalanche energy	E_{AR}***	137	mJ
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

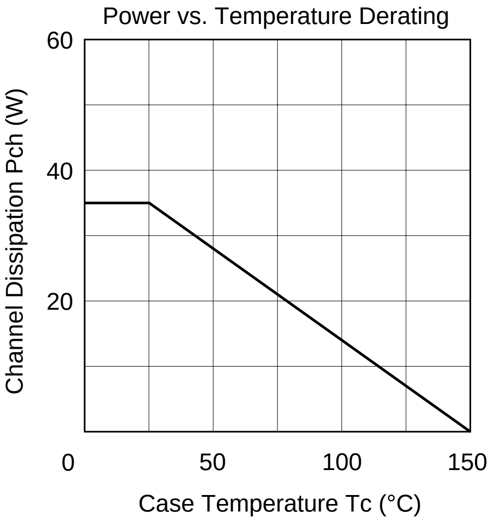
*   PW ≤ 10 µs, duty cycle ≤ 1 %
**   Value at Tc = 25 °C
***   Value at Tch = 25 °C, Rg ≥ 50 Ω

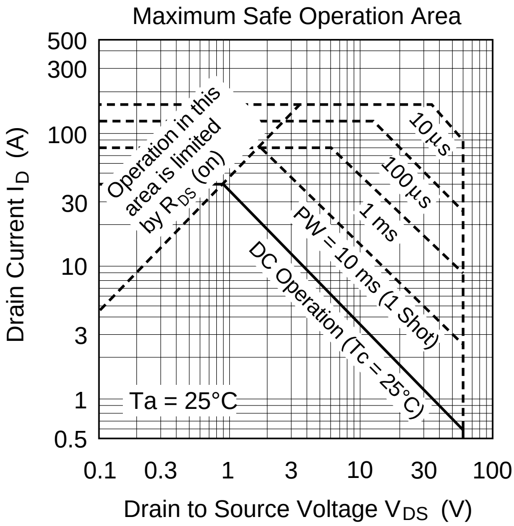
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.018	0.022	Ω	I_D = 20 A V_{GS} = 10 V *
		—	0.023	0.028	Ω	I_D = 20 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	22	35	—	S	I_D = 20 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3530	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1480	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	33	—	ns	I_D = 20 A
Rise time	t_r	—	155	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	450	—	ns	R_L = 1.5 Ω
Fall time	t_f	—	220	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 40 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

See characteristic curves of 2SK1911


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
500
300
100
30
10
3
1
0.5
Operation in this area is limited by R DS (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

2SK1957

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter,Motor Control

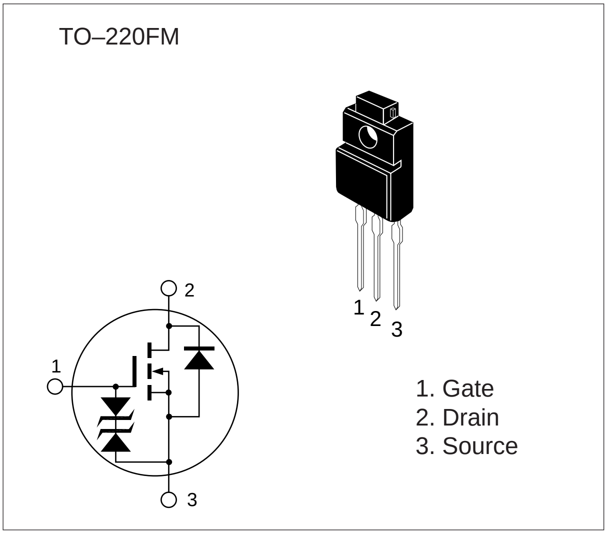


Table 1 Absolute Maximum Ratings (Ta = 25°C)

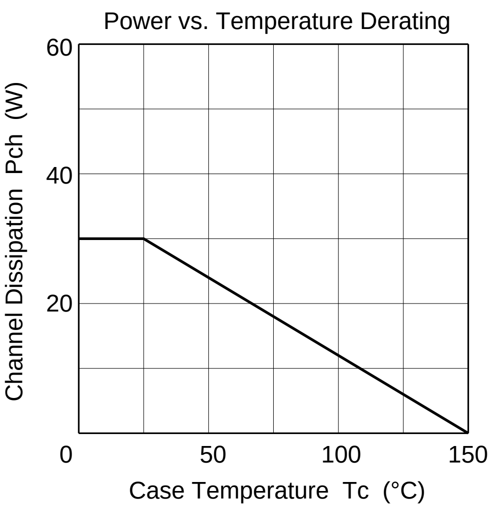
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

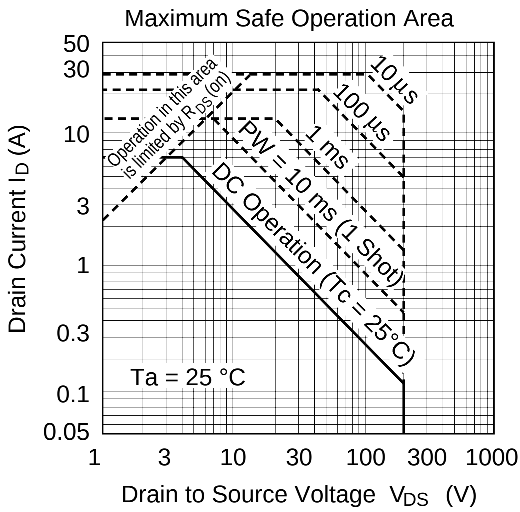
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

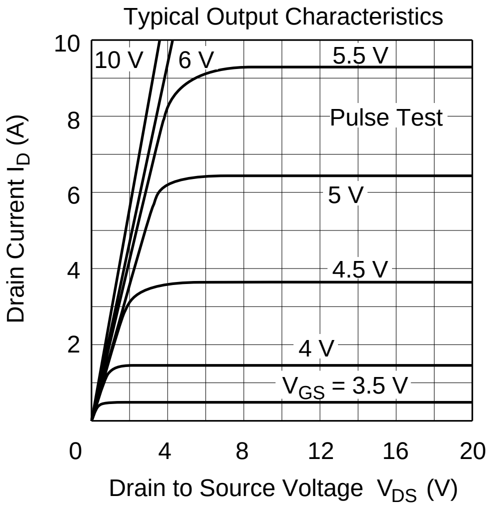
Table 2 Electrical Characteristics (Ta = 25°C)

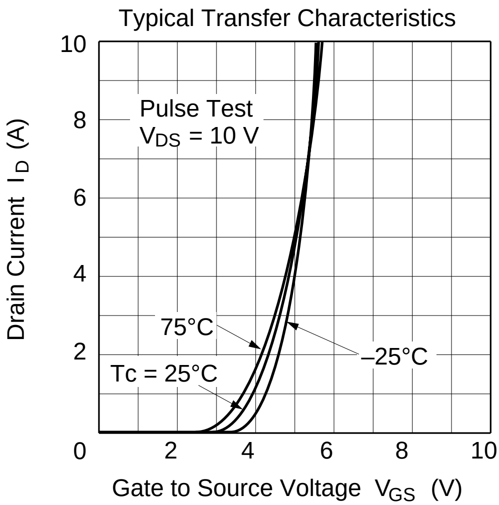
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.33	0.45	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	4.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	260	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 4 A
Rise time	t_r	—	45	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	50	—	ns	R_L = 7.5Ω
Fall time	t_f	—	35	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	150	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 100 A / µs

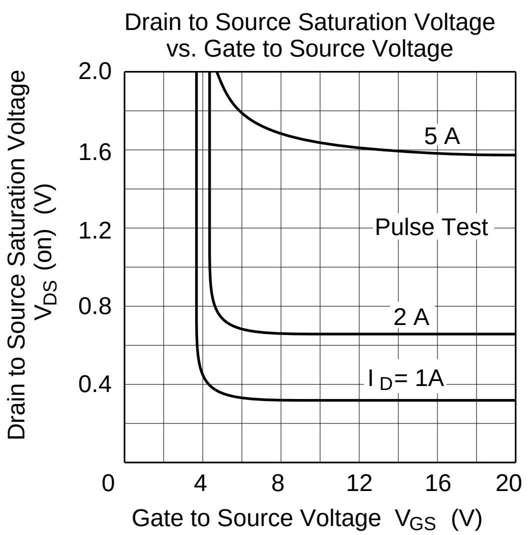
* Pulse Test

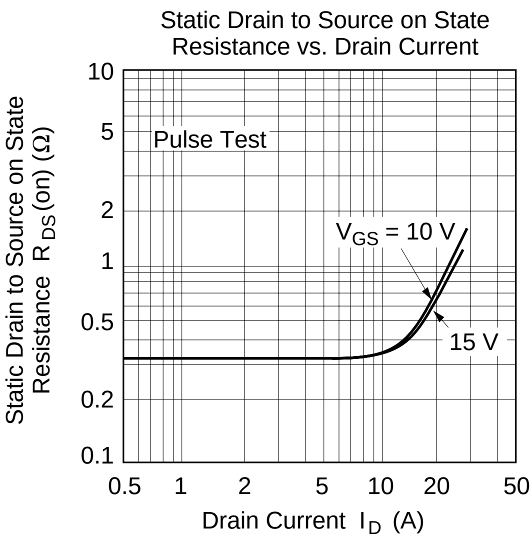

Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)

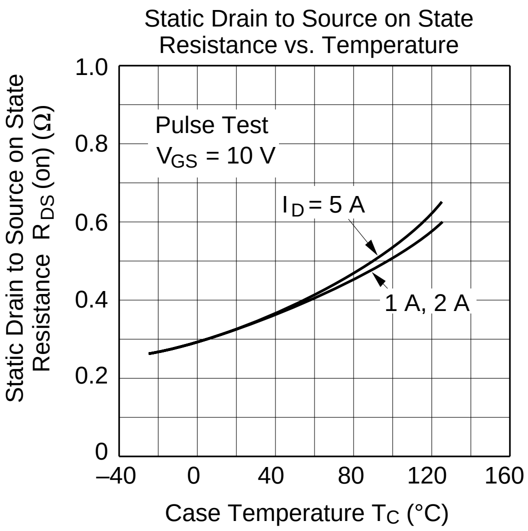

Maximum Safe Operation Area
Drain Current ID (A)
50
30
10
3
1
0.3
0.1
0.05
Operation in this area is limited by RDS (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25 °C
1
3
10
30
100
300
1000
Drain to Source Voltage VDS (V)

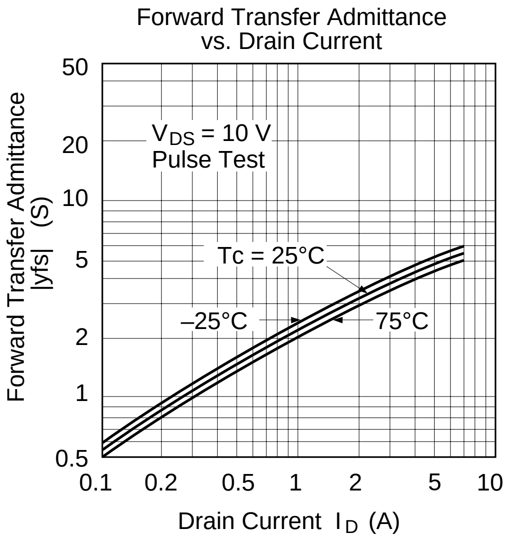

Typical Output Characteristics
Drain Current ID (A)
10
8
6
4
2
0
10 V
6 V
5.5 V
Pulse Test
5 V
4.5 V
4 V
VGS = 3.5 V
4
8
12
16
20
Drain to Source Voltage VDS (V)

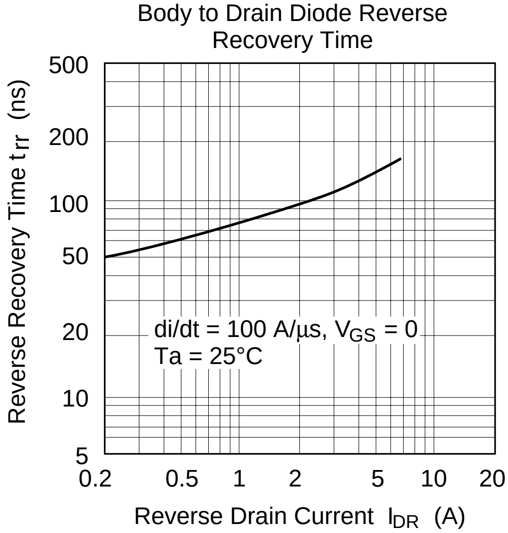

Typical Transfer Characteristics
Drain Current ID (A)
10
8
6
4
2
0
Pulse Test
VDS = 10 V
75°C
–25°C
Tc = 25°C
2
4
6
8
10
Gate to Source Voltage VGS (V)

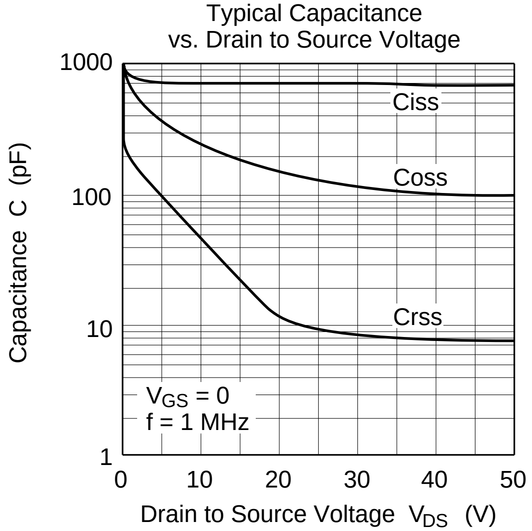

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
V_DS (on) (V)
2.0
1.6
1.2
0.8
0.4
0
4
8
12
16
20
5 A
Pulse Test
2 A
I_D = 1A
Gate to Source Voltage V_GS (V)

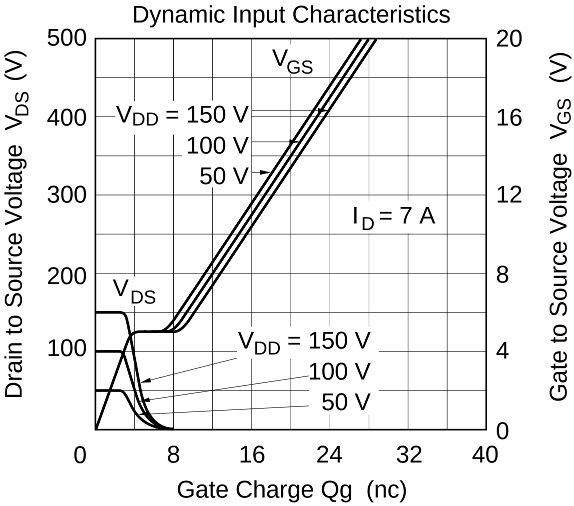

Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source on State
Resistance R_DS(on) (Ω)
10
5
2
1
0.5
0.2
0.1
Pulse Test
V_GS = 10 V
15 V
0.5
1
2
5
10
20
50
Drain Current I_D (A)

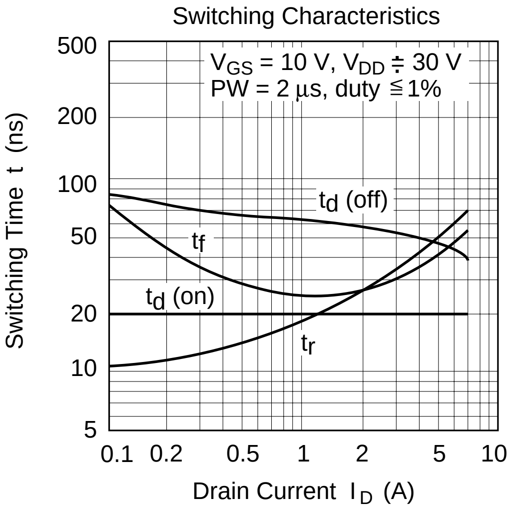

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State
Resistance R_DS(on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
Pulse Test
V_GS = 10 V
I_D = 5 A
1 A, 2 A
–40
0
40
80
120
160
Case Temperature T_C (°C)

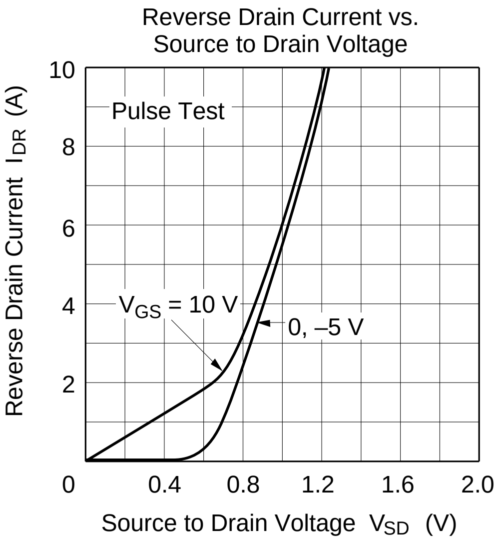

Forward Transfer Admittance
vs. Drain Current
Forward Transfer Admittance
|yfs| (S)
50
20
10
5
2
1
0.5
V_DS = 10 V
Pulse Test
Tc = 25°C
–25°C
75°C
0.1
0.2
0.5
1
2
5
10
Drain Current I_D (A)


Body to Drain Diode Reverse Recovery Time
di/dt = 100 A/μs, VGS = 0
Ta = 25°C
Reverse Recovery Time trr (ns)
Reverse Drain Current IDR (A)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20


Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
Drain to Source Voltage VDS (V)
1000
100
10
1
0
10
20
30
40
50


Dynamic Input Characteristics
VGS
VDD = 150 V
100 V
50 V
ID = 7 A
VDS
VDD = 150 V
100 V
50 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
500
400
300
200
100
20
16
12
8
4
0
0
8
16
24
32
40


Switching Characteristics
VGS = 10 V, VDD ≑ 30 V
PW = 2 μs, duty ≦ 1%
td (off)
tf
td (on)
tr
Switching Time t (ns)
Drain Current ID (A)
500
200
100
50
20
10
5
0.1
0.2
0.5
1
2
5
10


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 10 V
0, –5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
2
4
6
8
10

2SK1971

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter,Motor Control

TO–3PL

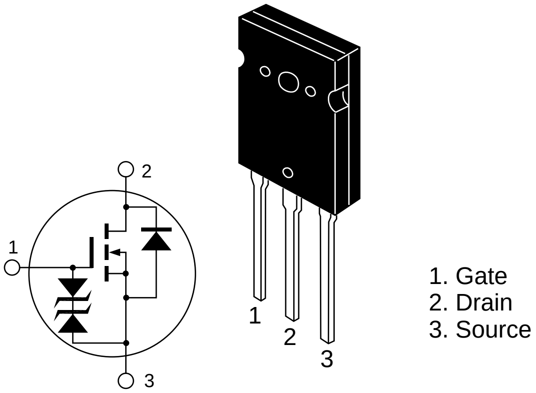


Table 1 Absolute Maximum Ratings (Ta = 25°C)

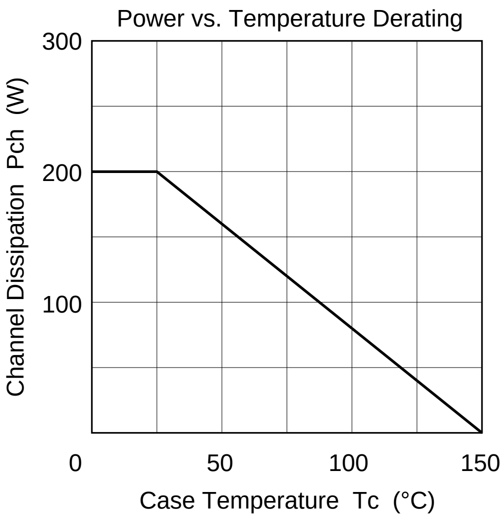
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	35	A
Drain peak current	$I_{D(pulse)}$*	140	A
Body–drain diode reverse drain current	I_{DR}	35	A
Channel dissipation	Pch**	200	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

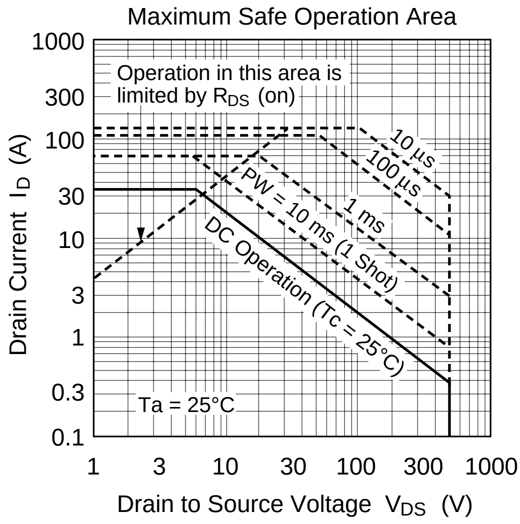
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

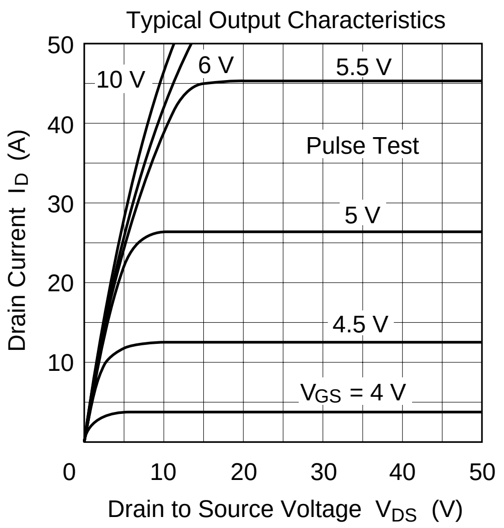
Table 2 Electrical Characteristics (Ta = 25°C)

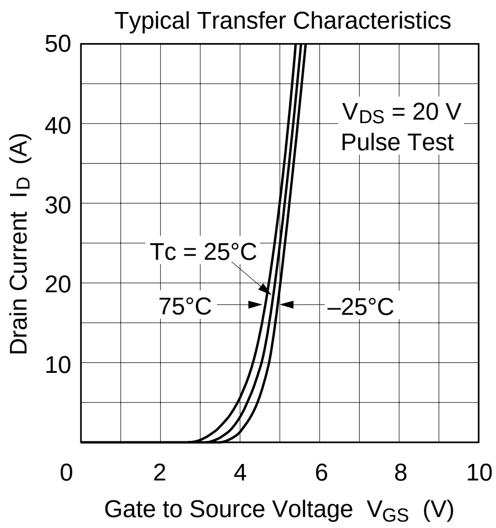
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =400 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.19	0.23	Ω	I_D = 18A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	16	24	—	S	I_D = 18A V_{DS} = 10 V *
Input capacitance	Ciss	—	4320	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1120	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	130	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	50	—	ns	I_D = 18A
Rise time	t_r	—	170	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	320	—	ns	R_L = 1.67Ω
Fall time	t_f	—	130	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F =35 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	530	—	ns	I_F = 35 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

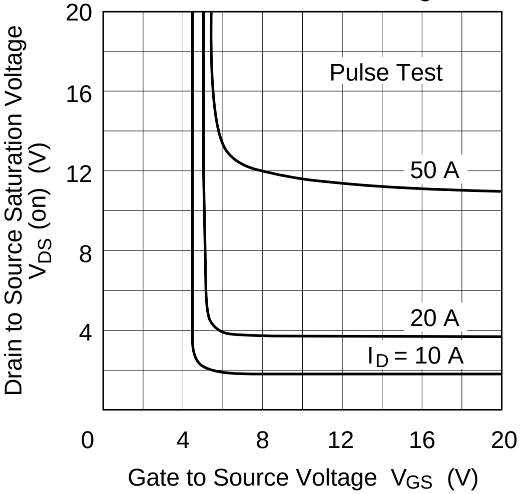

Power vs. Temperature Derating
300
200
100
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
Operation in this area is limited by R_{DS} (on)
10 µs
100 µs
PW = 10 ms (1 Shot)
1 ms
DC Operation (Tc = 25°C)
Ta = 25°C
1000
300
100
30
10
3
1
0.3
0.1
1
3
10
30
100
300
1000
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

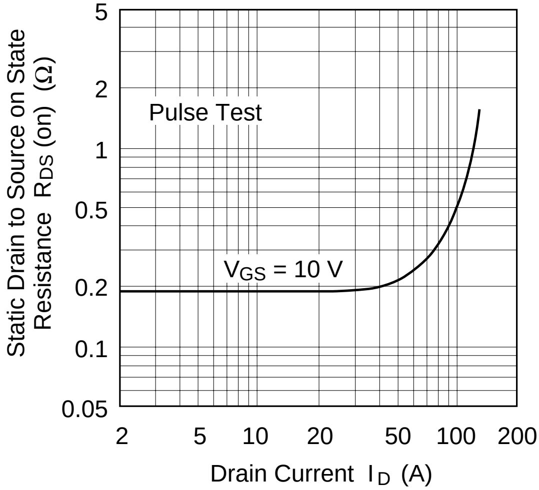

Typical Output Characteristics
10 V
6 V
5.5 V
Pulse Test
5 V
4.5 V
V_{GS} = 4 V
50
40
30
20
10
0
10
20
30
40
50
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
V_{DS} = 20 V
Pulse Test
Tc = 25°C
75°C
–25°C
50
40
30
20
10
0
2
4
6
8
10
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

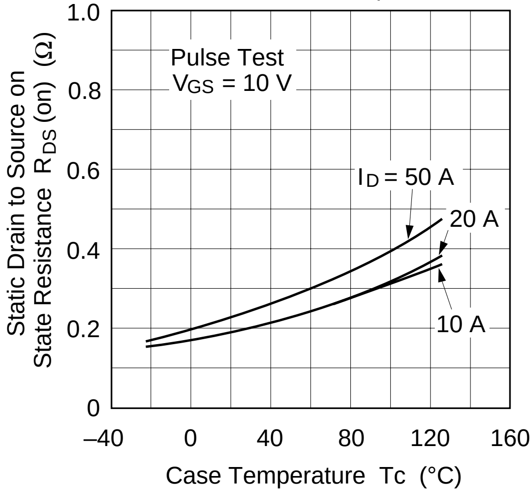
Drain to Source Saturation Voltage vs. Gate to Source Voltage



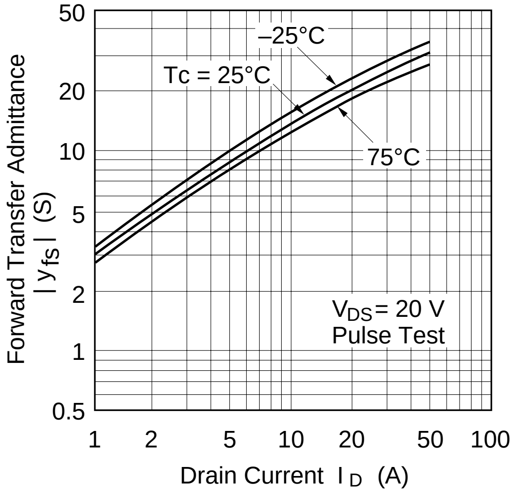
Static Drain to Source on State Resistance vs. Drain Current

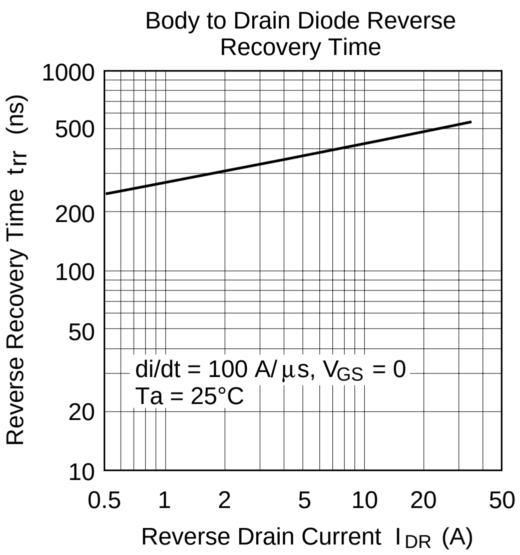


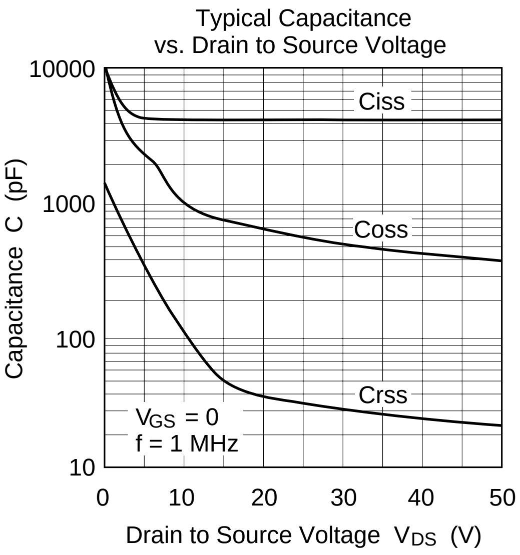
Static Drain to Source on State Resistance vs. Temperature

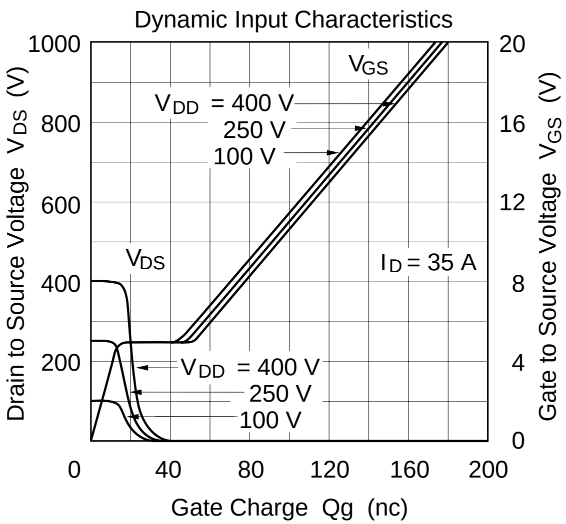


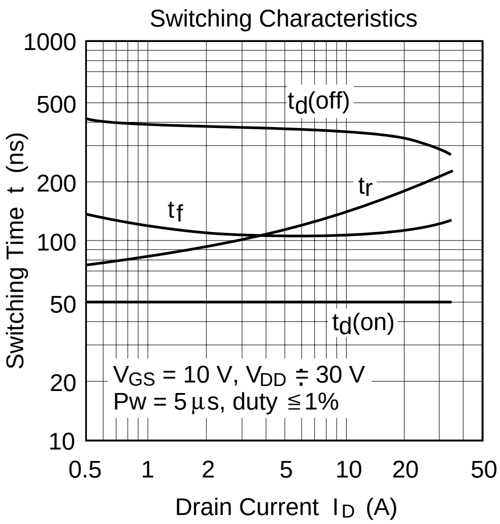
Forward Transfer Admittance vs. Drain Current

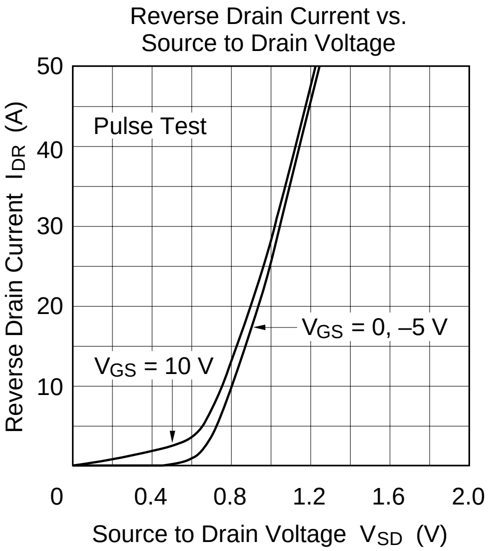



Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50
di/dt = 100 A/μs, VGS = 0
Ta = 25°C
Reverse Drain Current IDR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
10
0
10
20
30
40
50
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
1000
800
600
400
200
0
40
80
120
160
200
Gate to Source Voltage VGS (V)
20
16
12
8
4
0
VGS
VDD = 400 V
250 V
100 V
VDS
ID = 35 A
VDD = 400 V
250 V
100 V
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50
td(off)
tr
tf
td(on)
VGS = 10 V, VDD ≑ 30 V
Pw = 5 μs, duty ≦ 1%
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
0.4
0.8
1.2
1.6
2.0
10
20
30
40
50

2SK2008

Silicon N Channel MOS FET

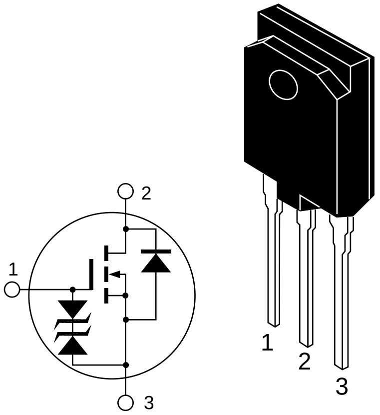
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter,Motor Control

TO–3PFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body–drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

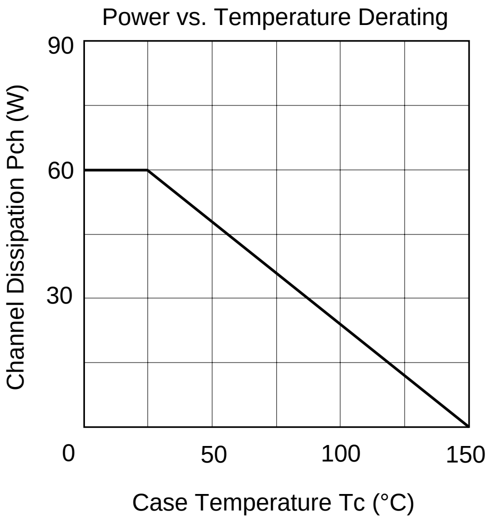
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

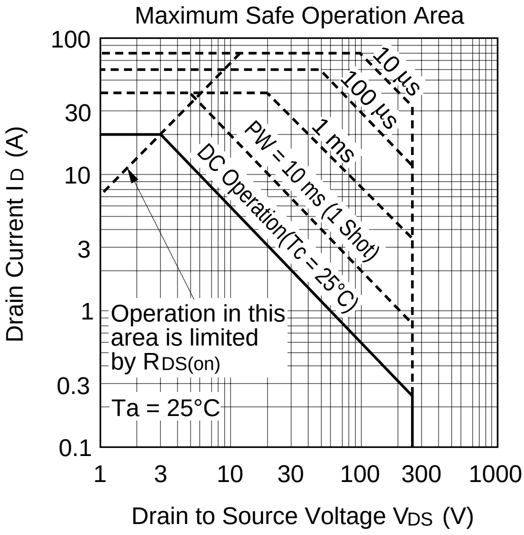
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 10 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	9.0	14	—	S	I_D = 10 A V_{DS} = 10 V *
Input capacitance	Ciss	—	2340	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	160	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 10 A
Rise time	t_r	—	125	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	190	—	ns	R_L = 3 Ω
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 20 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See chracteristic curves of 2SK2007


Power vs. Temperature Derating
Channel Dissipation Pch (W)
90
60
30
0
50
100
150
Case Temperature Tc (°C)

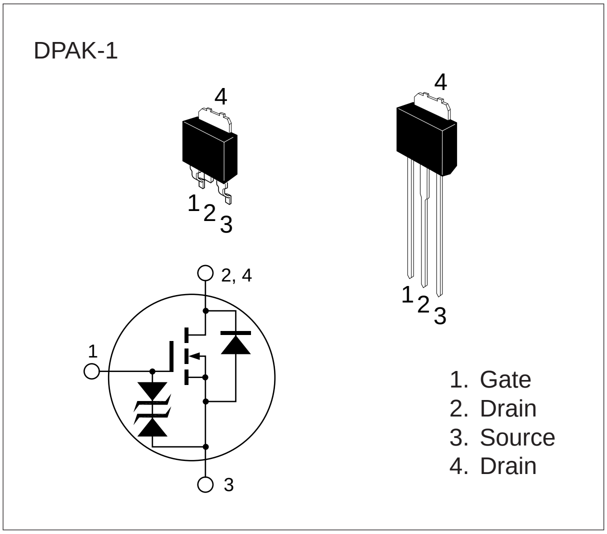

Maximum Safe Operation Area
Drain Current ID (A)
100
30
10
3
1
0.3
0.1
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation(Tc = 25°C)
Operation in this
area is limited
by RDS(on)
Ta = 25°C
1
3
10
30
100
300
1000
Drain to Source Voltage VDS (V)

2SK2059L, 2SK2059S

Silicon N Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- High speed switching
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}^*$	6	A
Body–drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} =500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	3.8	5.0	Ω	I_D = 2A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = 2A V_{DS} = 10 V *
Input capacitance	Ciss	—	295	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	70	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	12	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = 1A
Rise time	t_r	—	25	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 30Ω
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F =3 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 3A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

2SK2075

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low Drive Current
- No secondary breakdown
- Suitable for Switching regulator

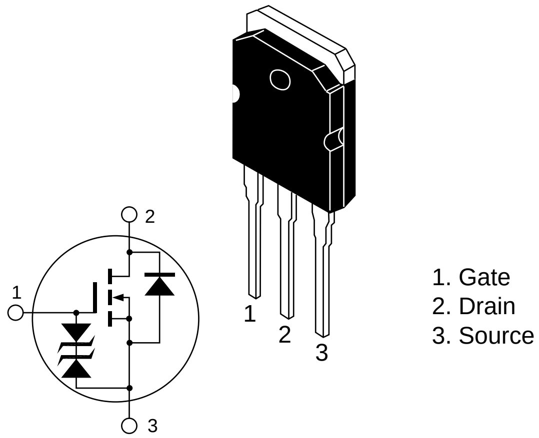


Table 1 Absolute Maximum Ratings (Ta = 25°C)

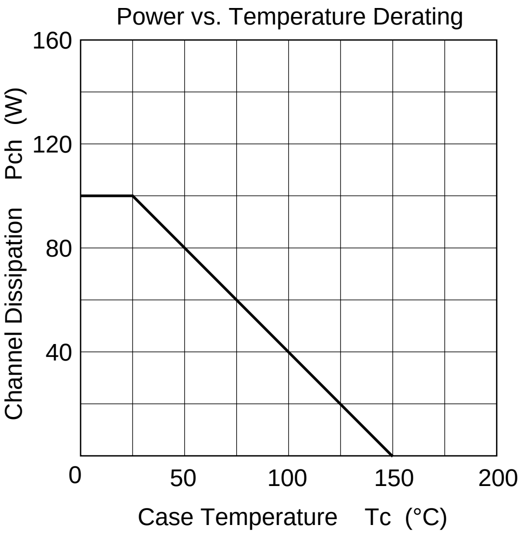
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body–drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

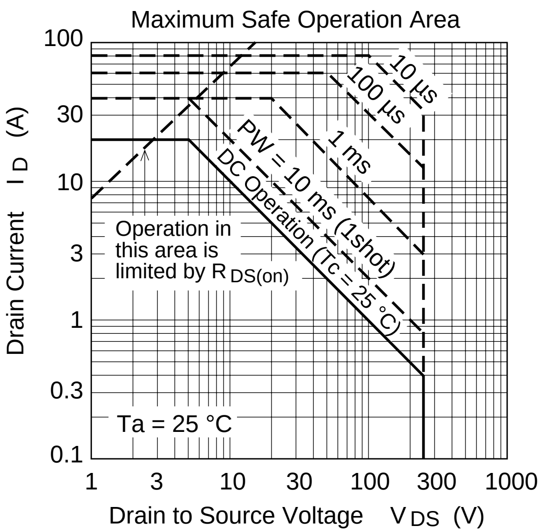
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

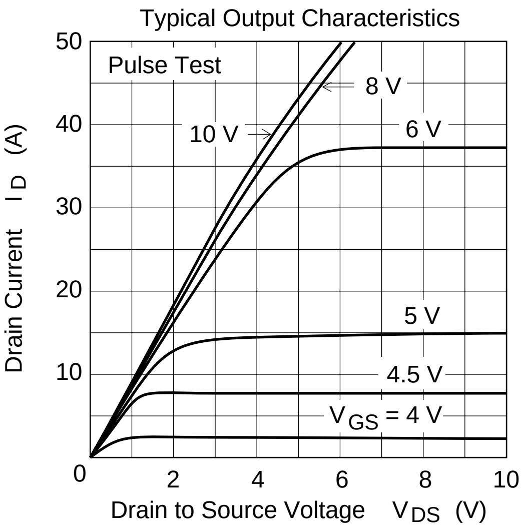
Table 2 Electrical Characteristics (Ta = 25°C)

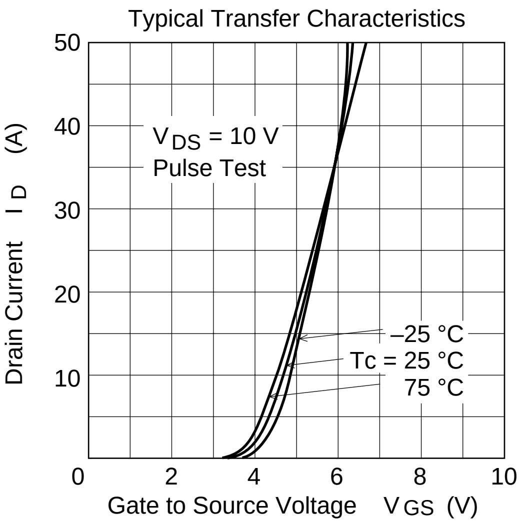
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.105	0.13	Ω	I_D = 10 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	9	14	—	S	I_D = 10 A V_{DS} = 10 V *
Input capacitance	Ciss	—	2400	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	970	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	145	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 10 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	220	—	ns	R_L = 3 Ω
Fall time	t_f	—	95	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	330	—	ns	I_F = 20 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

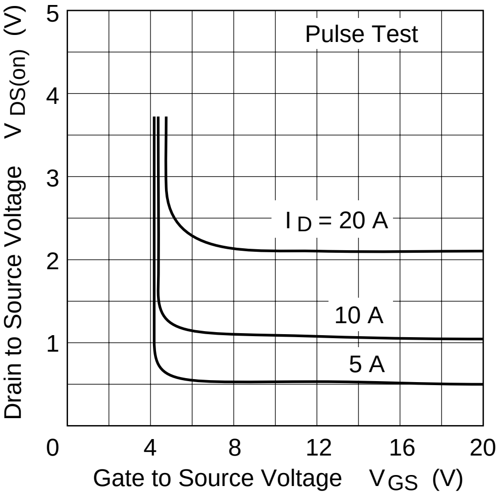

Power vs. Temperature Derating
Channel Dissipation Pch (W)
160
120
80
40
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
100
30
10
3
1
0.3
0.1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
1
3
10
30
100
300
1000
Drain to Source Voltage V DS (V)

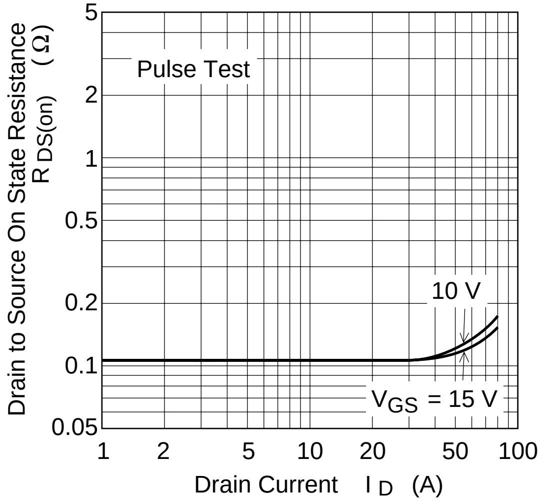

Typical Output Characteristics
Drain Current I D (A)
50
40
30
20
10
0
Pulse Test
8 V
10 V
6 V
5 V
4.5 V
V GS = 4 V
2
4
6
8
10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
50
40
30
20
10
V DS = 10 V
Pulse Test
–25 °C
Tc = 25 °C
75 °C
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

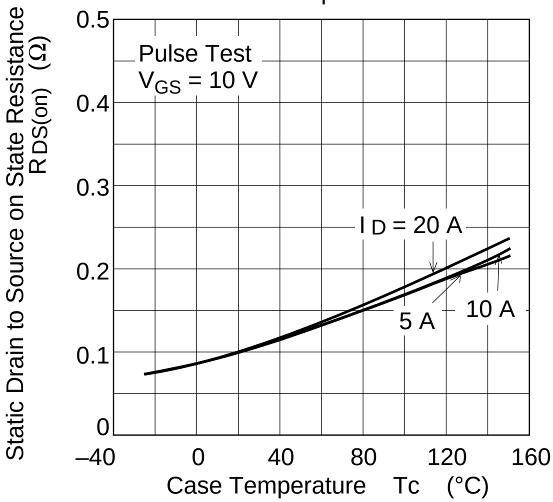
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



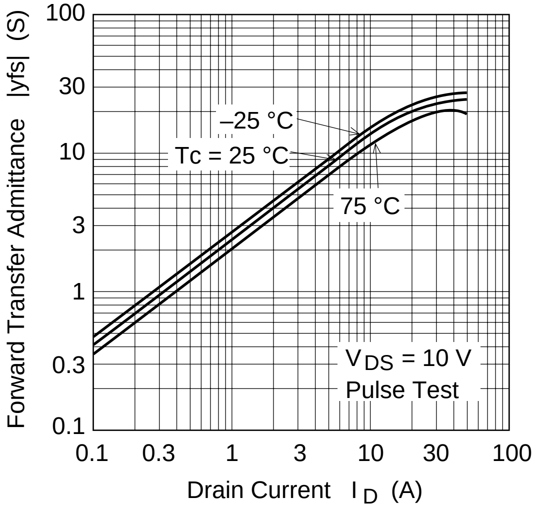
Static Drain to Source on State Resistance
vs. Drain Current

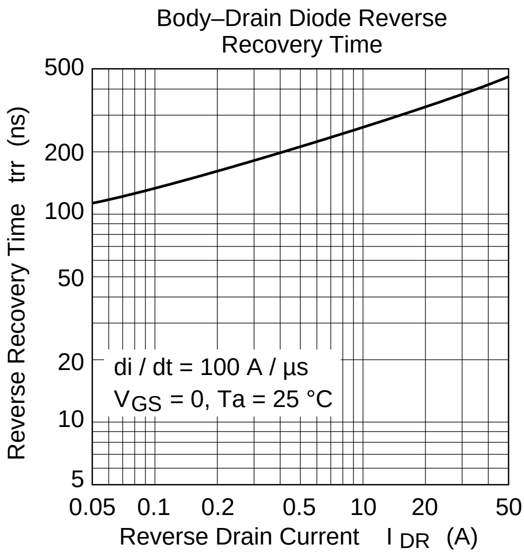


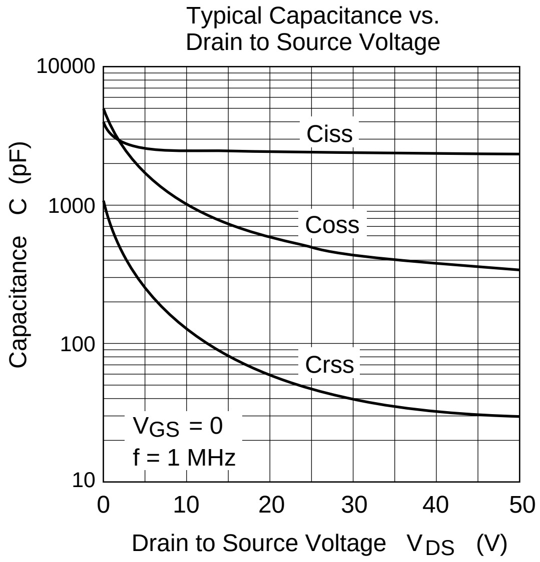
Static Drain to Source on State Resistance
vs. Temperature

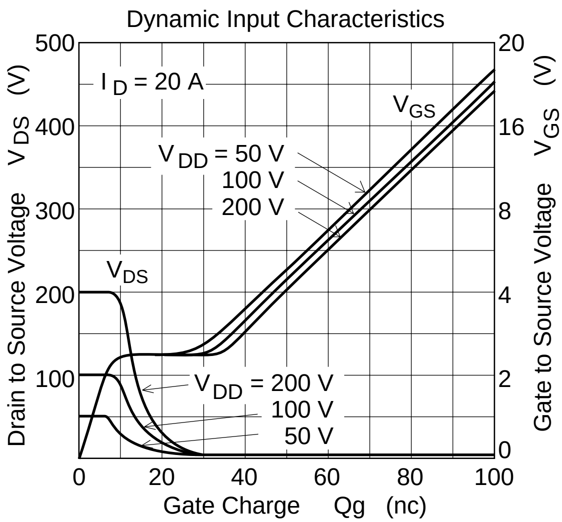


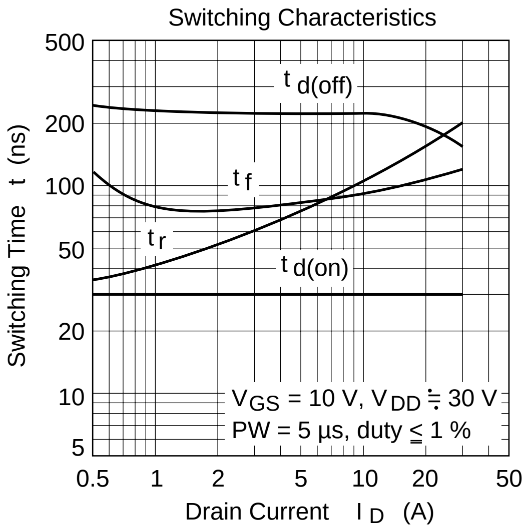
Forward Transfer Admittance vs.
Drain Current

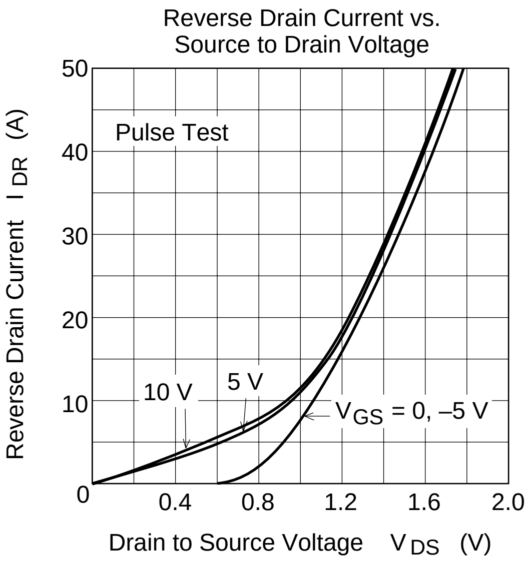


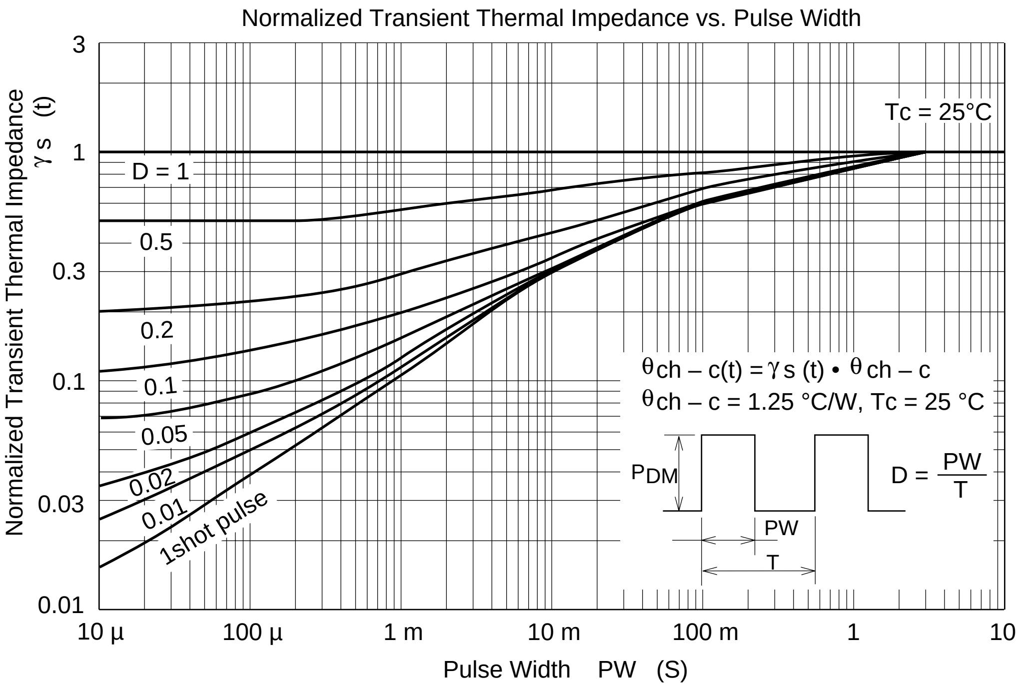

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
di / dt = 100 A / µs
VGS = 0, Ta = 25 °C
500
200
100
50
20
10
5
0.05
0.1
0.2
0.5
10
20
50


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
10000
1000
100
10
0
10
20
30
40
50

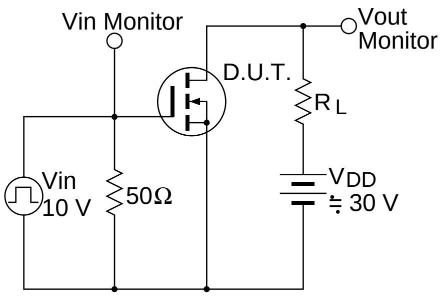

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
I D = 20 A
VGS
VDD = 50 V
100 V
200 V
VDS
VDD = 200 V
100 V
50 V
500
400
300
200
100
0
20
40
60
80
100
20
16
8
4
2
0


Switching Characteristics
Switching Time t (ns)
Drain Current I D (A)
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
500
200
100
50
20
10
5
0.5
1
2
5
10
20
50

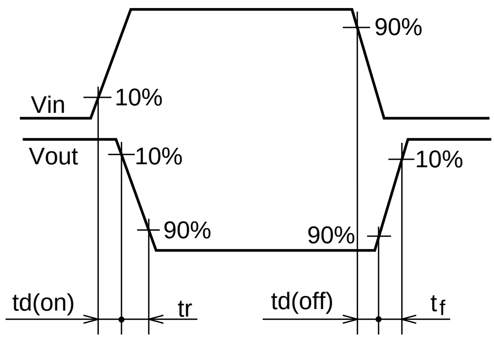

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
Reverse Drain Current I DR (A)
Drain to Source Voltage V DS (V)
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 1.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Waveform



2SK2084(L), 2SK2084(S)

Silicon N Channel MOS FET

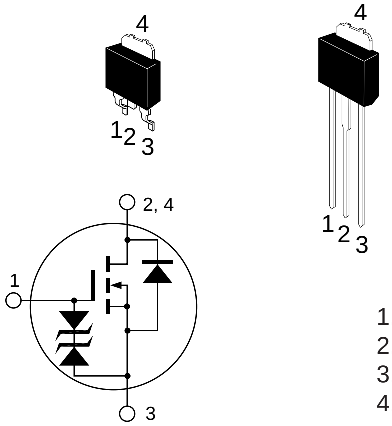
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

DPAK-2



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

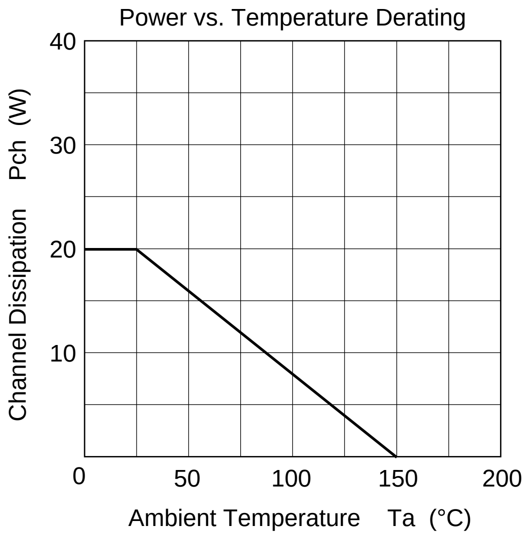
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

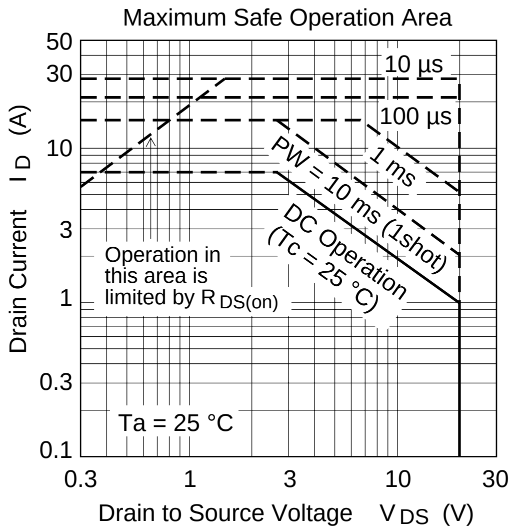
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

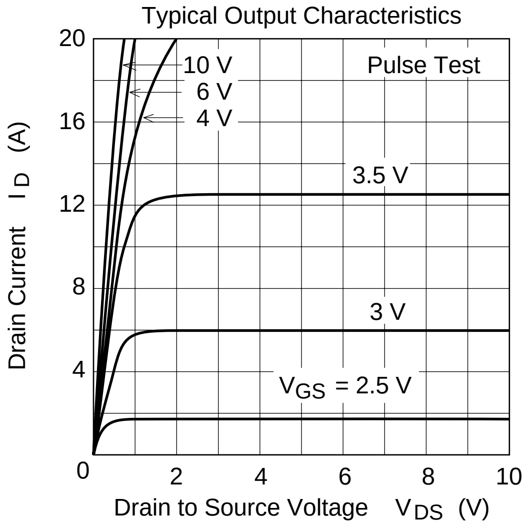
Table 2 Electrical Characteristics (Ta = 25°C)

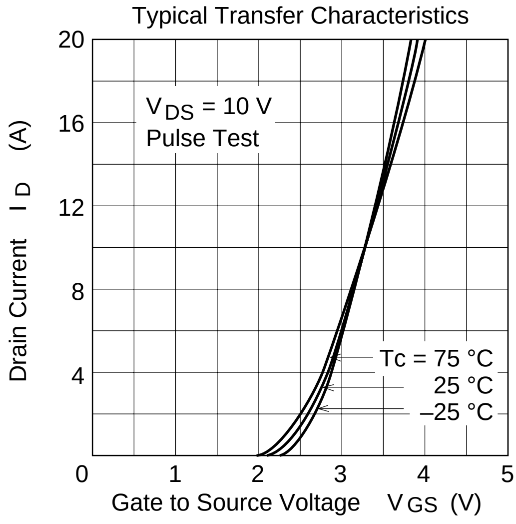
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 16 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.04	0.053	Ω	I_D = 4 A V_{GS} = 10 V *
		—	0.058	0.075	Ω	I_D = 4 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	5	9	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	800	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	680	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	165	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 4 A
Rise time	t_r	—	60	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 5 Ω
Fall time	t_f	—	80	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	80	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 20 A / µs

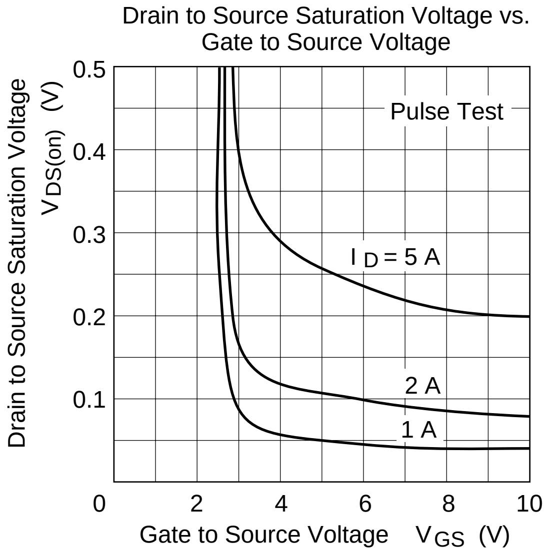
* Pulse Test

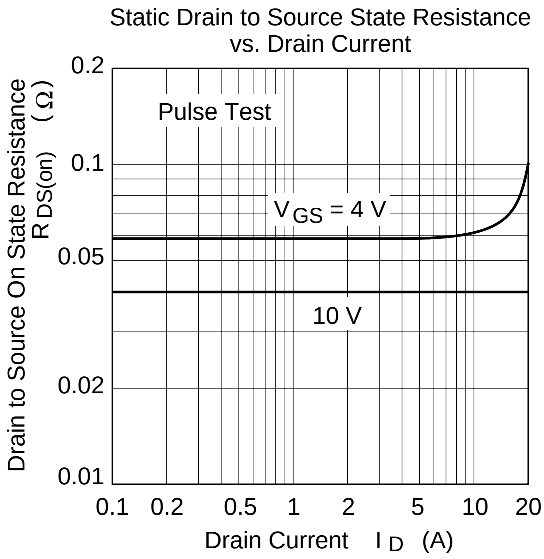

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Ambient Temperature Ta (°C)

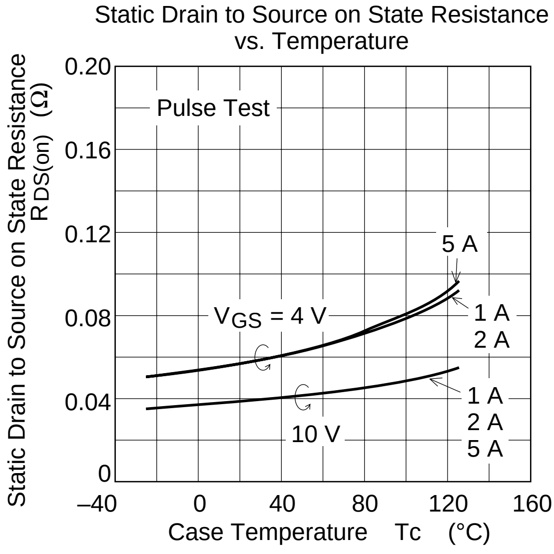

Maximum Safe Operation Area
Drain Current I D (A)
50
30
10
3
1
0.3
0.1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation
(Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.3
1
3
10
30
Drain to Source Voltage V DS (V)

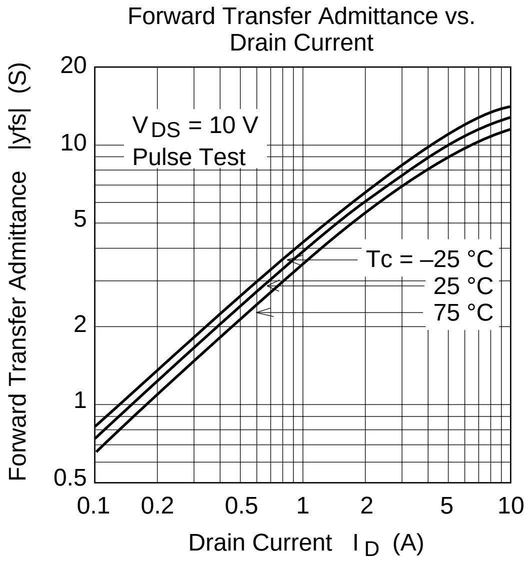

Typical Output Characteristics
Drain Current I D (A)
20
16
12
8
4
0
10 V
6 V
4 V
Pulse Test
3.5 V
3 V
VGS = 2.5 V
2
4
6
8
10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
20
16
12
8
4
0
VDS = 10 V
Pulse Test
Tc = 75 °C
25 °C
–25 °C
1
2
3
4
5
Gate to Source Voltage V GS (V)

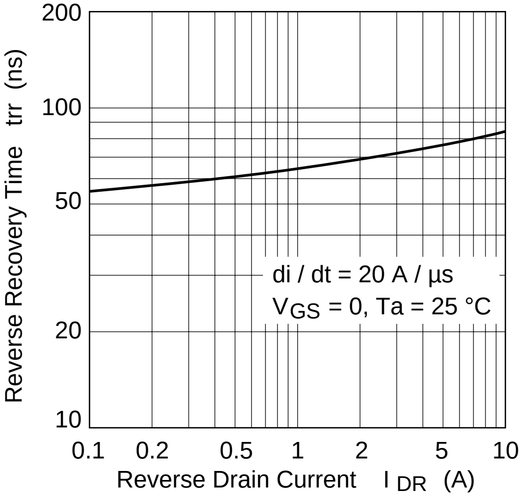

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage
VDS(on) (V)
0.5
0.4
0.3
0.2
0.1
0
2
4
6
8
10
Pulse Test
I D = 5 A
2 A
1 A
Gate to Source Voltage VGS (V)


Static Drain to Source State Resistance
vs. Drain Current
Drain to Source On State Resistance
R DS(on) (Ω)
0.2
0.1
0.05
0.02
0.01
Pulse Test
VGS = 4 V
10 V
0.1
0.2
0.5
1
2
5
10
20
Drain Current I D (A)

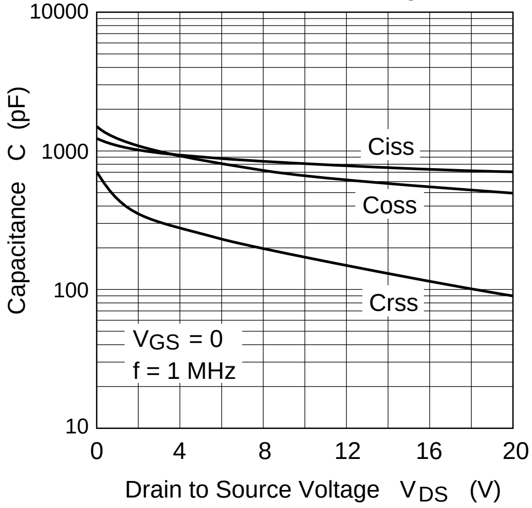

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance
R DS(on) (Ω)
0.20
0.16
0.12
0.08
0.04
0
Pulse Test
5 A
VGS = 4 V
1 A
2 A
1 A
2 A
5 A
10 V
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
20
10
5
2
1
0.5
VDS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

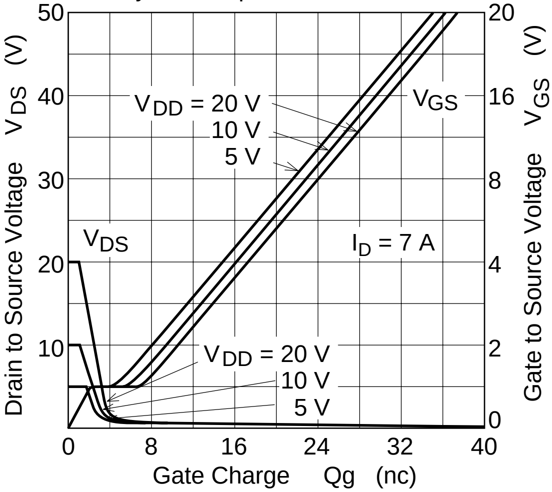
Body–Drain Diode Reverse Recovery Time



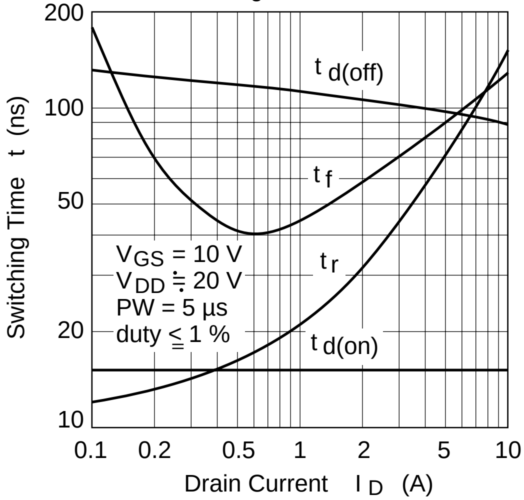
Typical Capacitance vs. Drain to Source Voltage

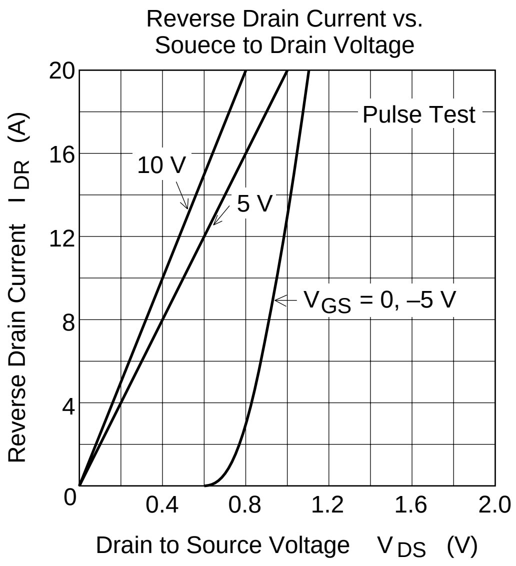


Dynamic Input Characteristics

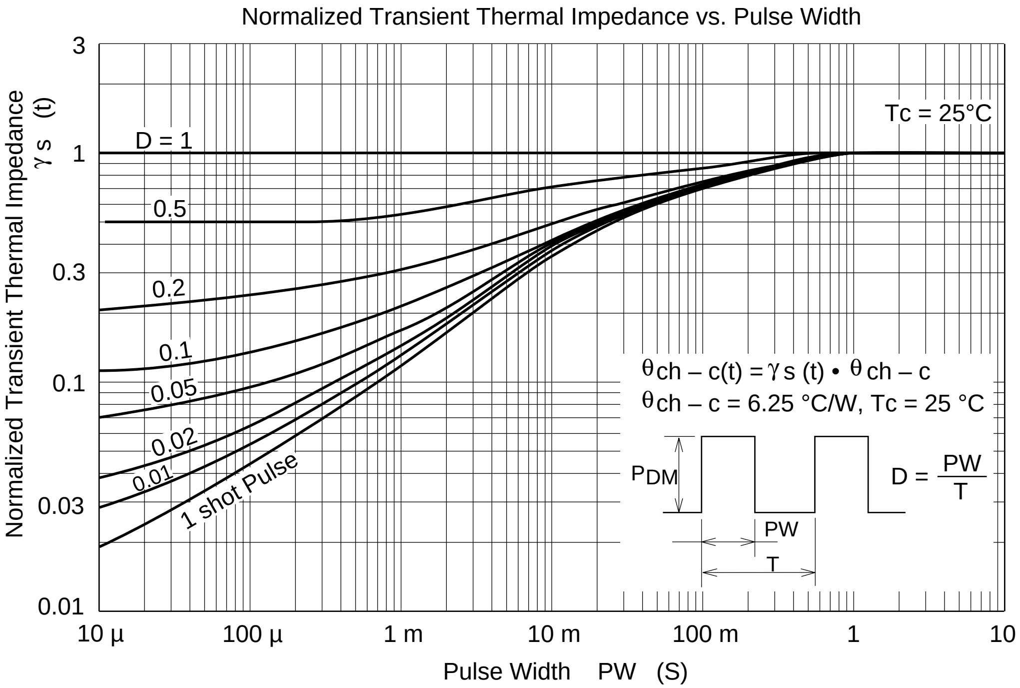


Switching Characteristics



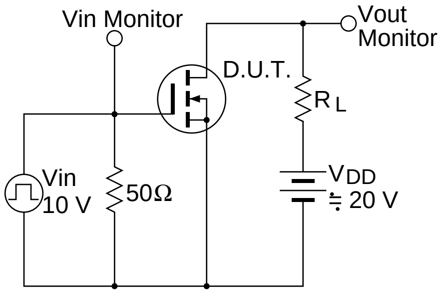


Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
10 V
5 V
V_{GS} = 0, –5 V
20
16
12
8
4
0
0.4
0.8
1.2
1.6
2.0
Reverse Drain Current I_{DR} (A)
Drain to Source Voltage V_{DS} (V)

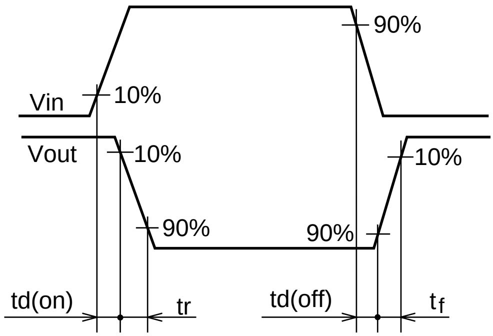


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
$\theta ch – c(t) = \gamma s (t) \bullet \theta ch – c$
$\theta ch – c$ = 6.25 °C/W, Tc = 25 °C
P_{DM}
PW
T
D = $\frac{PW}{T}$
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)

Switching Time Test Circuit



Waveform



2SK2085

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

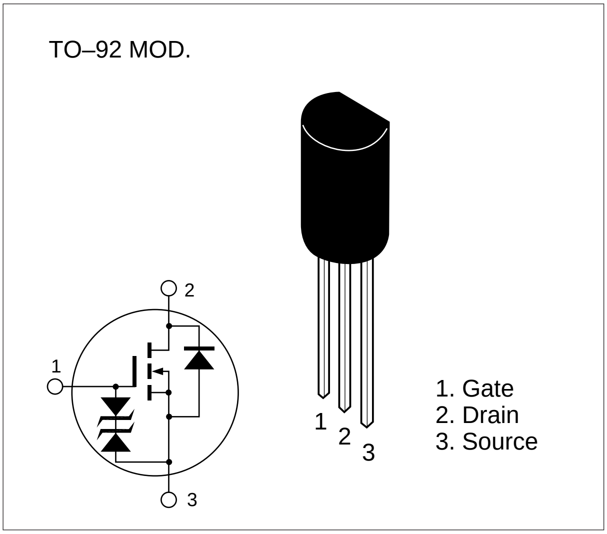


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$*	4.0	A
Body–drain diode reverse drain current	I_{DR}	1.0	A
Channel dissipation	Pch**	0.9	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

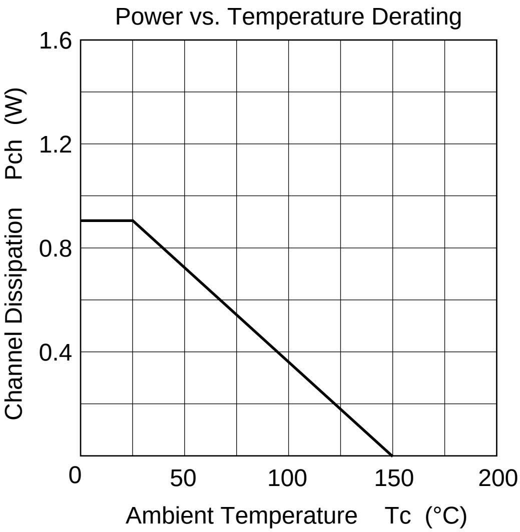
* PW ≤ 10 µs, duty cycle ≤ 1 %

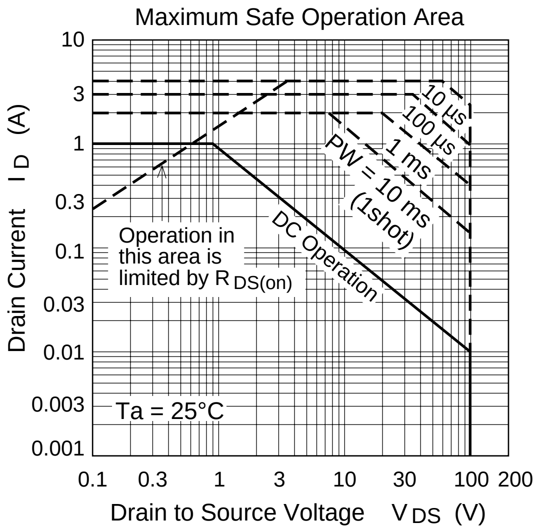
** Value at Tc = 25 °C

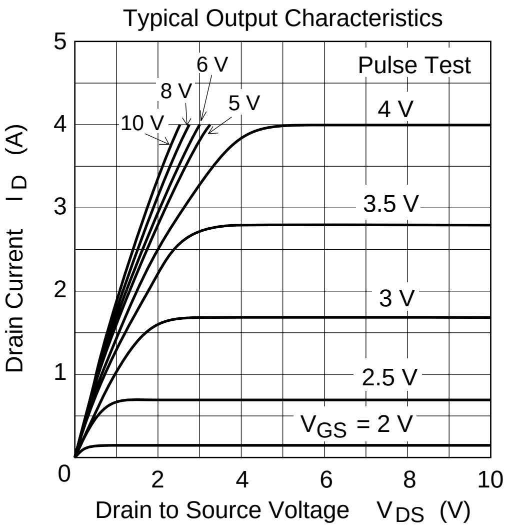
Table 2 Electrical Characteristics (Ta = 25°C)

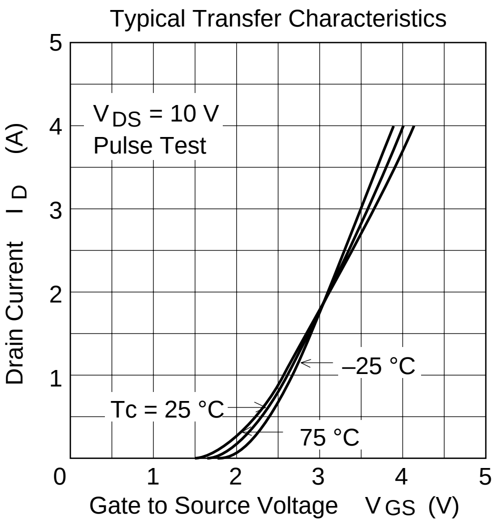
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.6	0.9	Ω	I_D = 0.5 A V_{GS} = 10 V *
		—	0.75	1.35	Ω	I_D = 0.5 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.7	1.2	—	S	I_D = 0.5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	130	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	50	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	12	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	7	—	ns	I_D = 0.5 A
Rise time	t_r	—	6.5	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	55	—	ns	R_L = 60 Ω
Fall time	t_f	—	20	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.85	—	V	I_F = 1.0 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	80	—	ns	I_F = 1.0 A, V_{GS} = 0, diF / dt = 50 A / µs

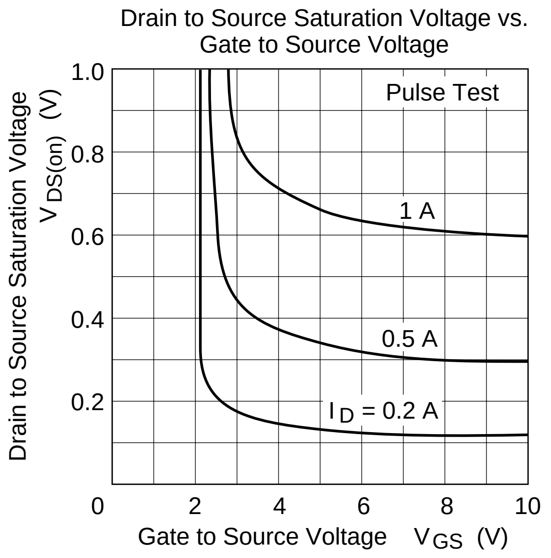
* Pulse Test

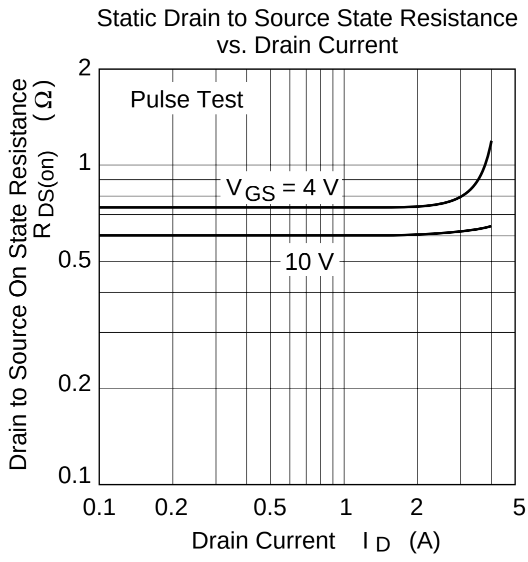

Power vs. Temperature Derating
Channel Dissipation Pch (W)
1.6
1.2
0.8
0.4
0
50
100
150
200
Ambient Temperature Tc (°C)

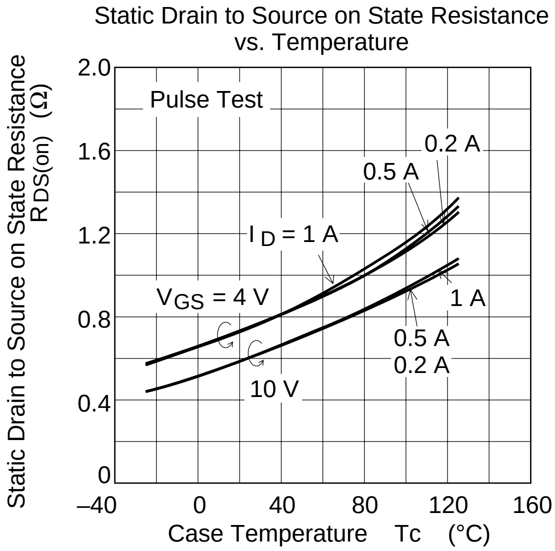

Maximum Safe Operation Area
Drain Current I D (A)
10
3
1
0.3
0.1
0.03
0.01
0.003
0.001
10 µs
100 µs
1 ms
PW = 10 ms
(1shot)
DC Operation
Operation in
this area is
limited by R DS(on)
Ta = 25°C
0.1
0.3
1
3
10
30
100
200
Drain to Source Voltage V DS (V)

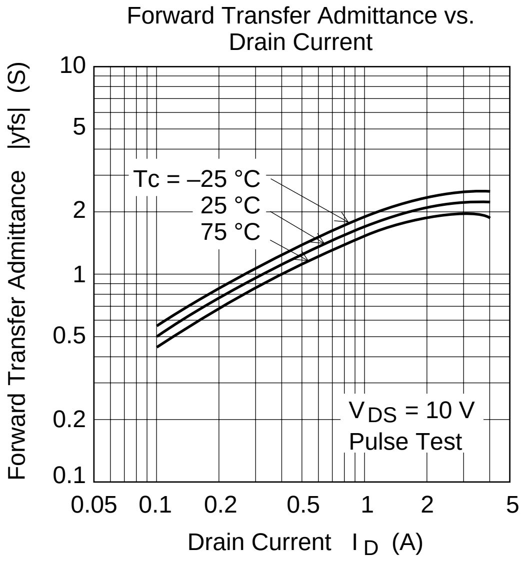

Typical Output Characteristics
Drain Current I D (A)
5
4
3
2
1
0
6 V
8 V
5 V
10 V
Pulse Test
4 V
3.5 V
3 V
2.5 V
VGS = 2 V
2
4
6
8
10
Drain to Source Voltage V DS (V)

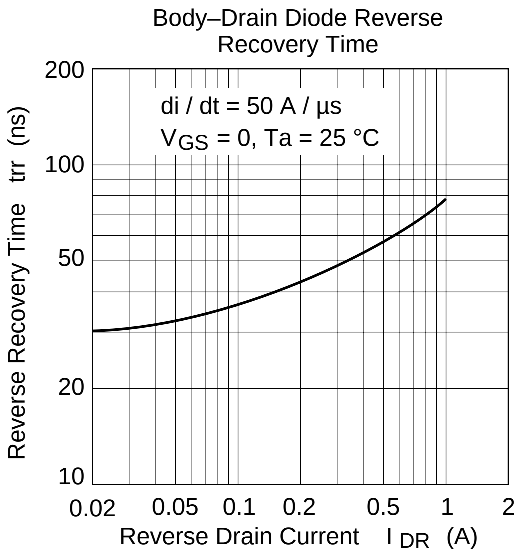

Typical Transfer Characteristics
Drain Current I D (A)
5
4
3
2
1
0
V DS = 10 V
Pulse Test
–25 °C
Tc = 25 °C
75 °C
1
2
3
4
5
Gate to Source Voltage V GS (V)

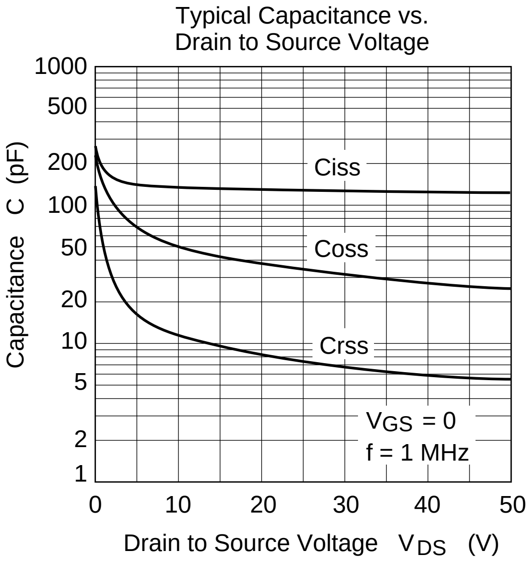

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
1 A
0.5 A
I D = 0.2 A
Drain to Source Saturation Voltage
V DS(on) (V)
1.0
0.8
0.6
0.4
0.2
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

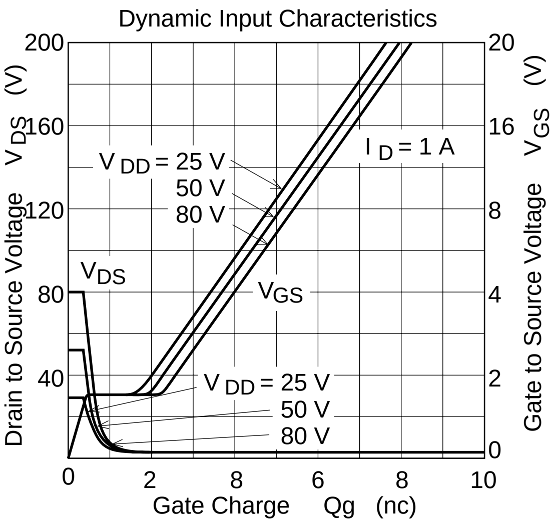

Static Drain to Source State Resistance
vs. Drain Current
Pulse Test
V GS = 4 V
10 V
Drain to Source On State Resistance
R DS(on) (Ω)
2
1
0.5
0.2
0.1
0.1
0.2
0.5
1
2
5
Drain Current I D (A)

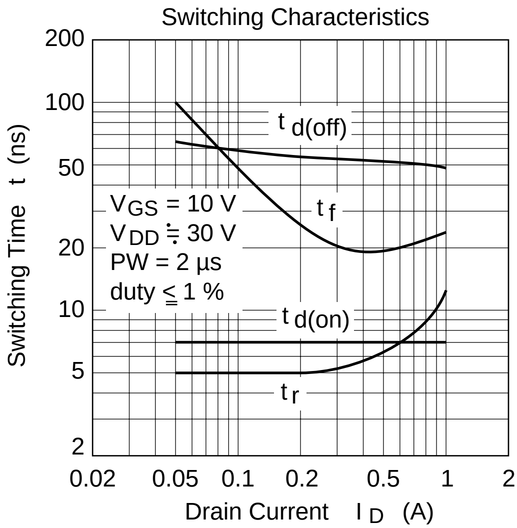

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
0.2 A
0.5 A
I D = 1 A
V GS = 4 V
1 A
0.5 A
0.2 A
10 V
Static Drain to Source on State Resistance
R DS(on) (Ω)
2.0
1.6
1.2
0.8
0.4
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

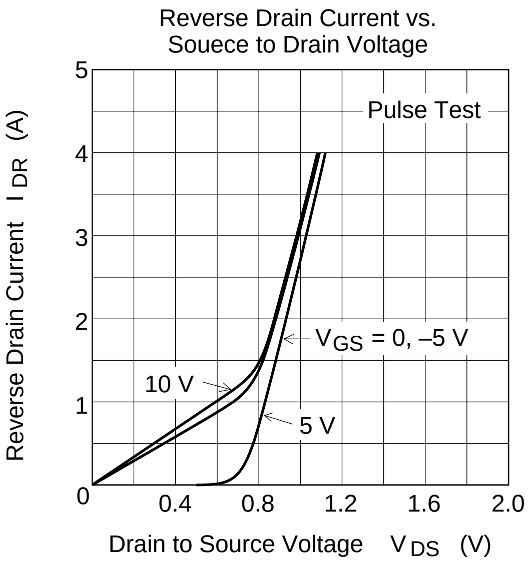

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
10
5
2
1
0.5
0.2
0.1
0.05
0.1
0.2
0.5
1
2
5
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
di / dt = 50 A / μs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
200
100
50
20
10
0.02
0.05
0.1
0.2
0.5
1
2
Reverse Drain Current I DR (A)

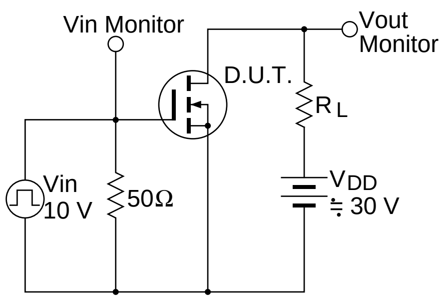

Typical Capacitance vs. Drain to Source Voltage
1000
500
200
100
50
20
10
5
2
1
Capacitance C (pF)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
200
160
120
80
40
20
16
8
4
2
0
Gate to Source Voltage VGS (V)
ID = 1 A
VDD = 25 V
50 V
80 V
VDS
VGS
VDD = 25 V
50 V
80 V
0
2
8
6
8
10
Gate Charge Qg (nc)

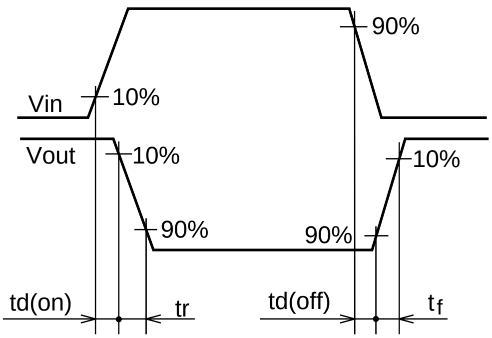

Switching Characteristics
Switching Time t (ns)
200
100
50
20
10
5
2
t d(off)
t f
t d(on)
t r
VGS = 10 V
VDD ≒ 30 V
PW = 2 μs
duty ≦ 1 %
0.02
0.05
0.1
0.2
0.5
1
2
Drain Current I D (A)



Switching Time Test Circuit



Waveform



2SK2096

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for switching regulator, DC-DC converter
- Avalanche ratings

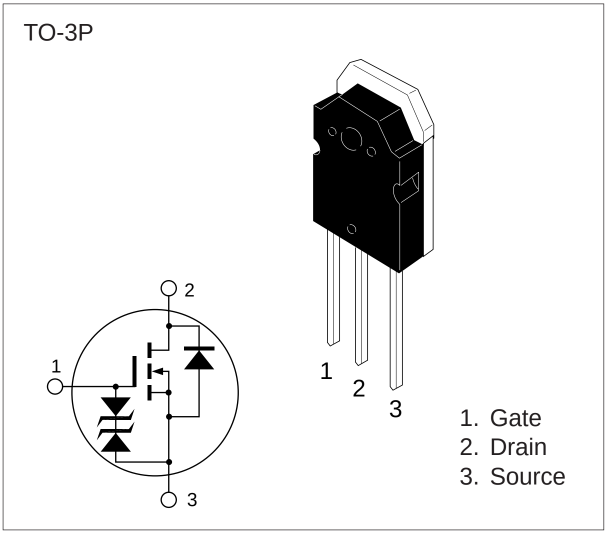


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	45	A
Drain peak current	$I_{D(pulse)}$*	180	A
Body–drain diode reverse drain current	I_{DR}	45	A
Avalanche current	I_{AP}***	45	A
Avalanche energy	E_{AR}***	173	mJ
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

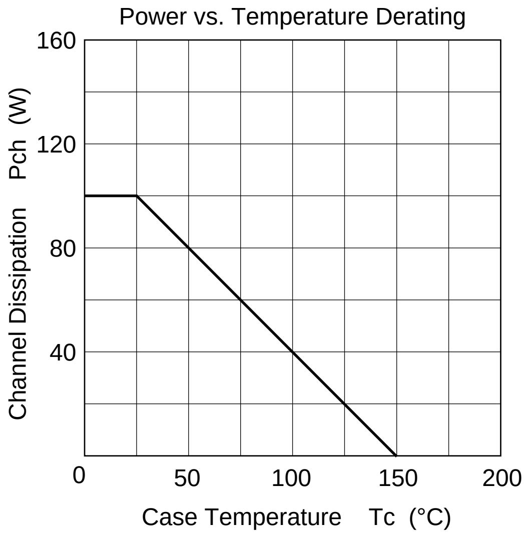
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

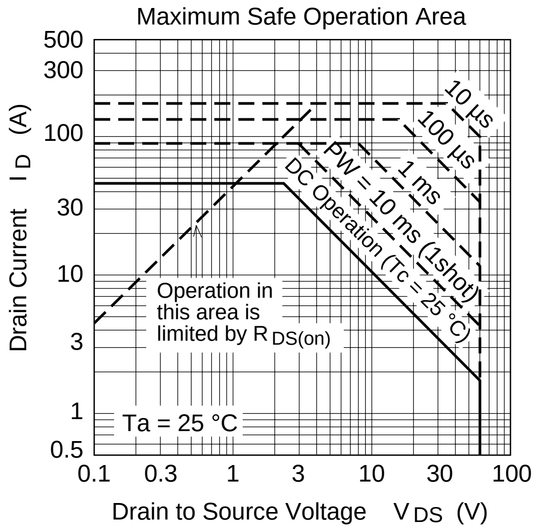
Table 2 Electrical Characteristics (Ta = 25°C)

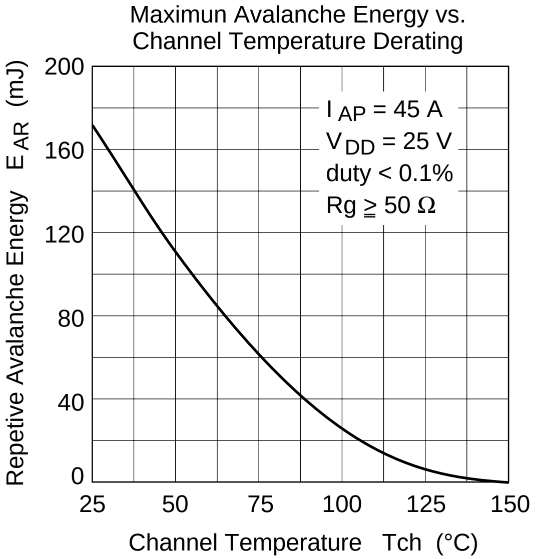
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.018	0.022	Ω	I_D = 25 A V_{GS} = 10 V *
		—	0.023	0.028	Ω	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	25	37	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3530	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1480	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	33	—	ns	I_D = 25 A
Rise time	t_r	—	160	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	450	—	ns	R_L = 1.5 Ω
Fall time	t_f	—	230	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 45 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 45 A, V_{GS} = 0, diF / dt = 50 A / µs

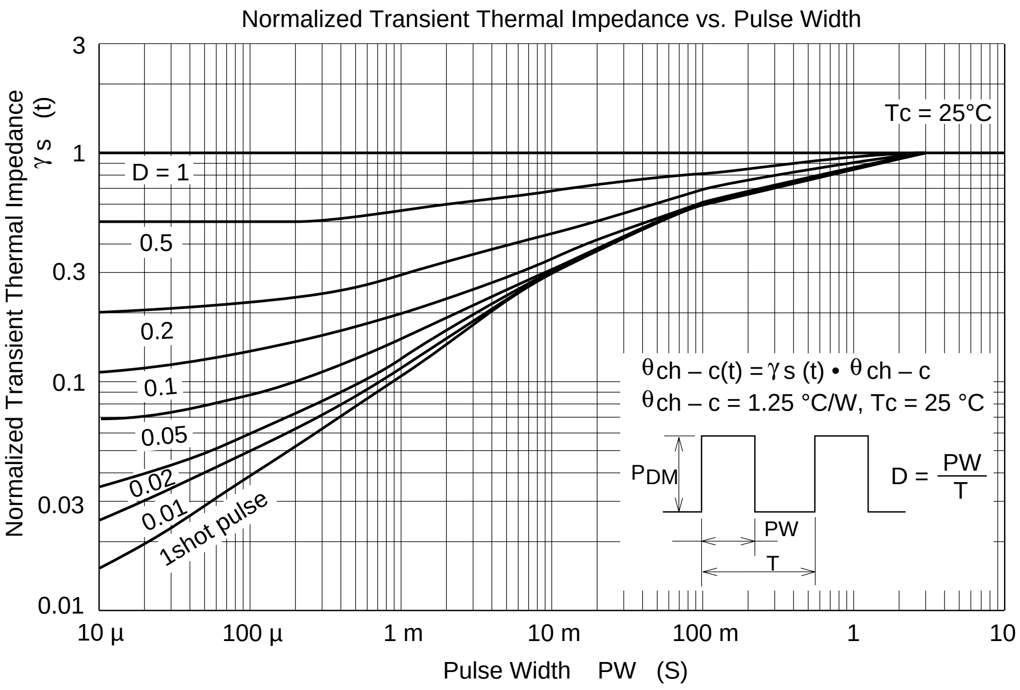
* Pulse Test

■ See characteristic curve of 2SK1911.

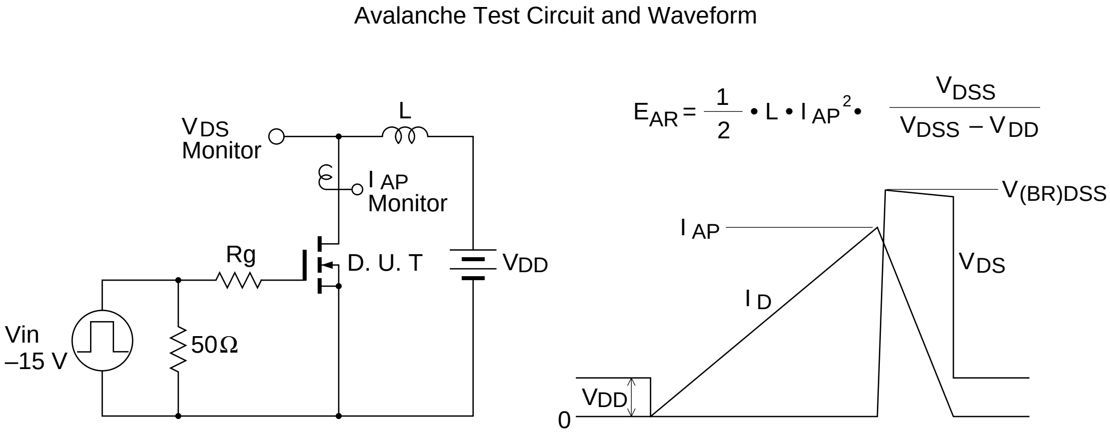

Power vs. Temperature Derating
160
120
80
40
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
500
300
100
30
10
3
1
0.5
0.1
0.3
1
3
10
30
100
Drain Current I D (A)
Drain to Source Voltage V DS (V)
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C


Maximun Avalanche Energy vs.
Channel Temperature Derating
200
160
120
80
40
0
25
50
75
100
125
150
Repetive Avalanche Energy E AR (mJ)
Channel Temperature Tch (°C)
I AP = 45 A
V DD = 25 V
duty < 0.1%
Rg ≧ 50 Ω



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance
γs (t)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 1.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)



Avalanche Test Circuit and Waveform
VDS Monitor
L
I AP Monitor
Rg
D. U. T
VDD
Vin
–15 V
50Ω
EAR = 1/2 • L • I AP^2 • VDSS / (VDSS – VDD)
V(BR)DSS
I AP
VDS
I D
VDD
0

2SK2097

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter.

TO–220CFM

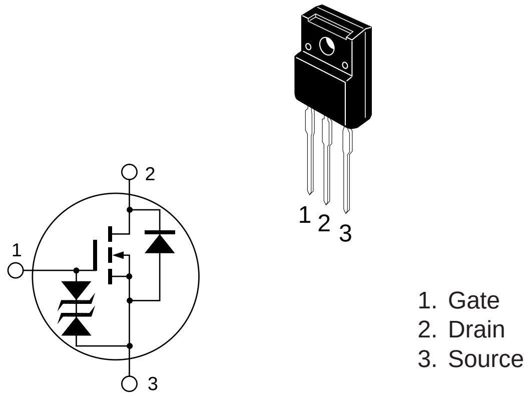


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$*	16	A
Body–drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

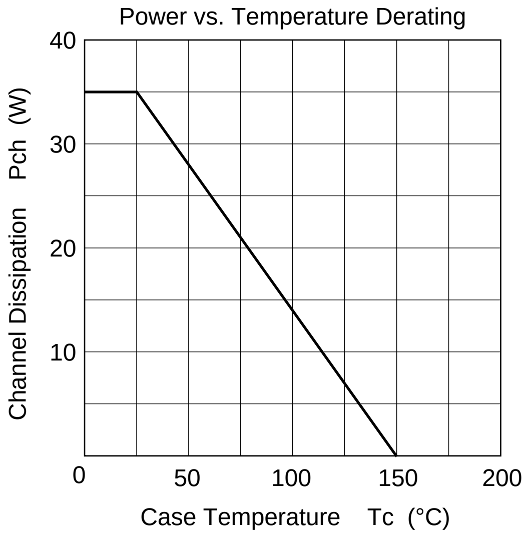
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.8	2.4	Ω	I_D = 2 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	2.2	3.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	600	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	140	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	25	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = 2 A
Rise time	t_r	—	30	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	60	—	ns	R_L = 15Ω
Fall time	t_f	—	35	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	300	—	ns	I_F = 4 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

■ See characteristic curve of 2SK1402.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

2SK2114, 2SK2115

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for Switching regulator

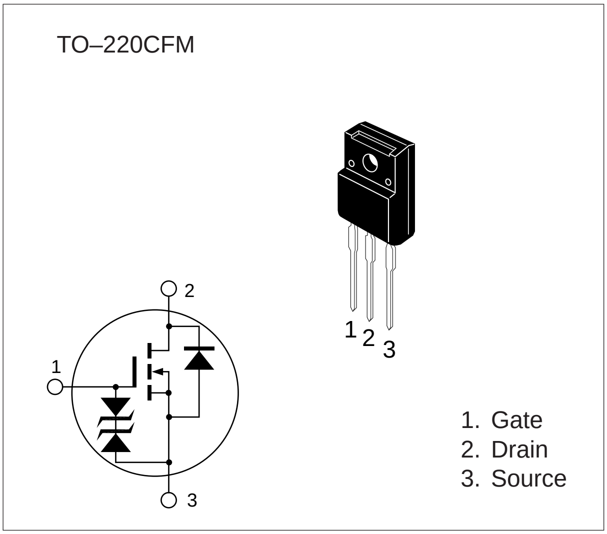


Table 1 Ordering Information

Type No.	V_{DSS}
2SK2114	450 V
2SK2115	500 V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK2114	V_{DSS}	450	V
	2SK2115	V_{DSS}	500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	5	A
Drain peak current		$I_{D(pulse)}$*	20	A
Body–drain diode reverse drain current		I_{DR}	5	A
Channel dissipation		Pch**	35	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

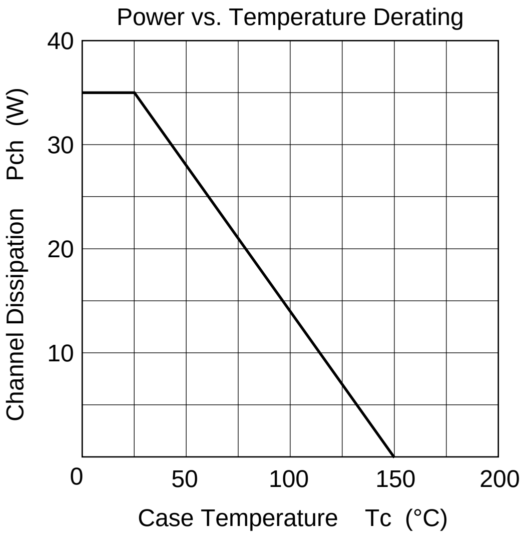
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

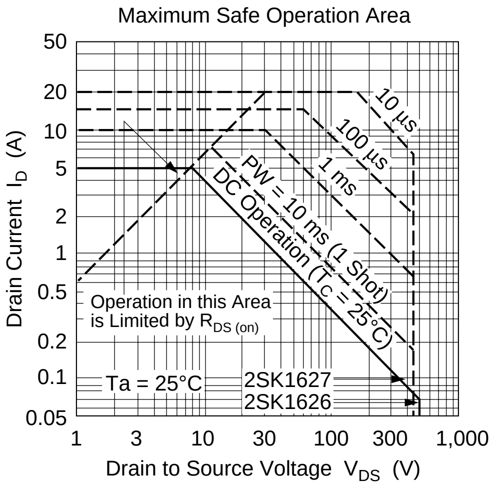
Table 3 Electrical Characteristics (Ta = 25°C)

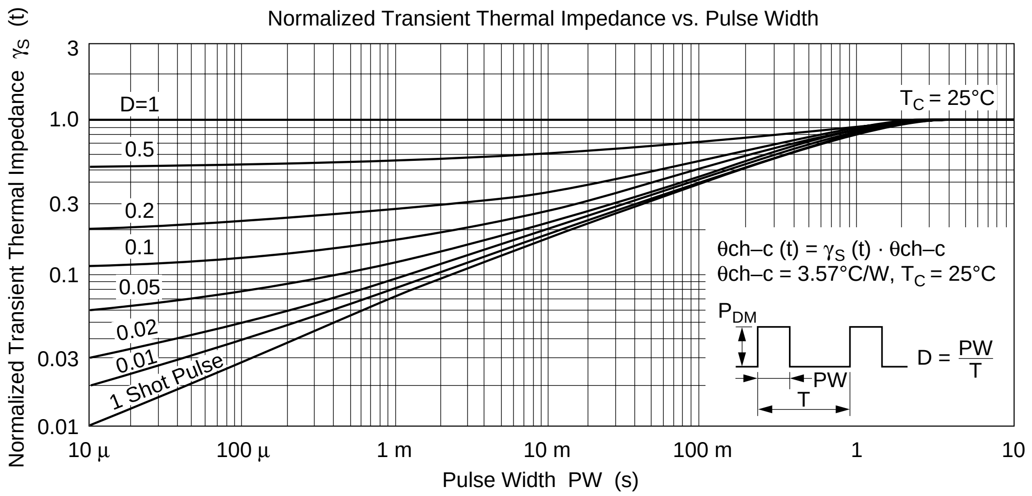
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK2114	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK2115		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK2114	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK2115						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	2SK2114	$R_{DS(on)}$	—	1.0	1.4	Ω	I_D = 2.5 A, V_{GS} = 10 V *
	2SK2115		—	1.2	1.5		
Forward transfer admittance		$\|y_{fs}\|$	2.5	4.0	—	S	I_D = 2.5 A V_{DS} = 10 V *
Input capacitance		Ciss	—	640	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	160	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	20	—	pF	f = 1 MHz
Turn–on delay time		$t_{d(on)}$	—	10	—	ns	I_D = 2.5 A
Rise time		t_r	—	25	—	ns	V_{GS} = 10 V
Turn–off delay time		$t_{d(off)}$	—	50	—	ns	R_L = 12 Ω
Fall time		t_f	—	30	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time		t_{rr}	—	300	—	ns	I_F = 5 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

■ See characteristics curve of 2SK1155, 2SK1156.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (TC = 25°C)
Operation in this Area
is Limited by RDS (on)
Ta = 25°C
2SK1627
2SK1626
1
3
10
30
100
300
1,000
Drain to Source Voltage VDS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γS (t)
3
1.0
0.3
0.1
0.03
0.01
D=1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
TC = 25°C
θch–c (t) = γS (t) · θch–c
θch–c = 3.57°C/W, TC = 25°C
PDM
PW
T
D = PW / T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK2116, 2SK2117

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for Switching regulator

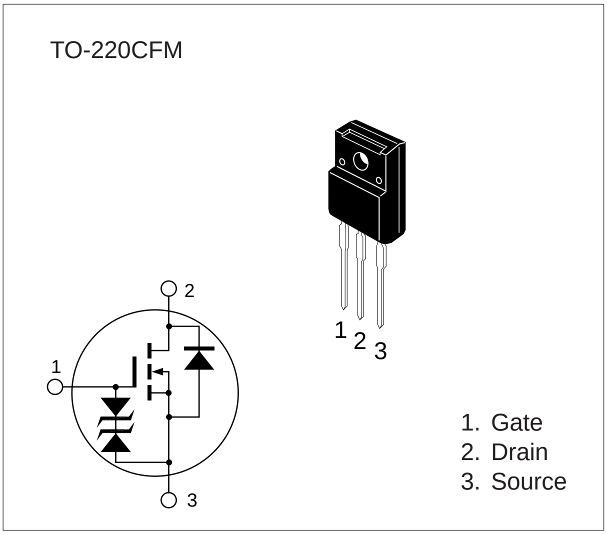


Table 1 Ordering Information

Type No.	V_{DSS}
2SK2116	450 V
2SK2117	500 V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK2116	V_{DSS}	450	V
	2SK2117	V_{DSS}	500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	7	A
Drain peak current		$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current		I_{DR}	7	A
Channel dissipation		Pch**	35	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

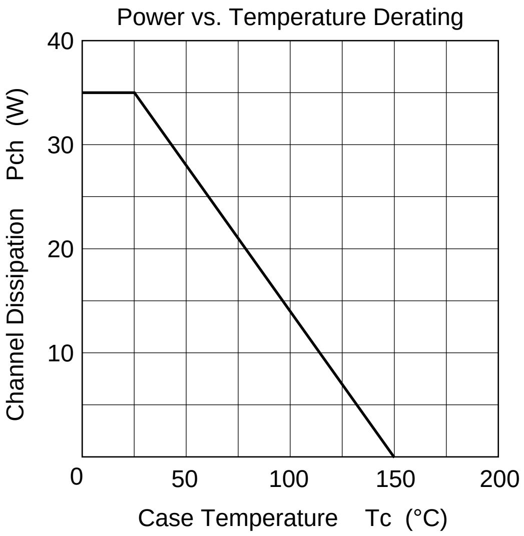
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

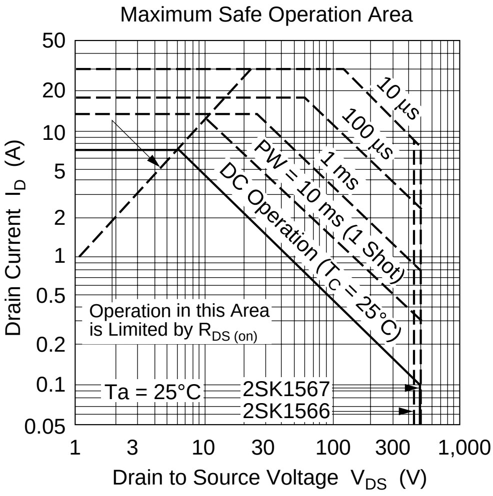
Table 3 Electrical Characteristics (Ta = 25°C)

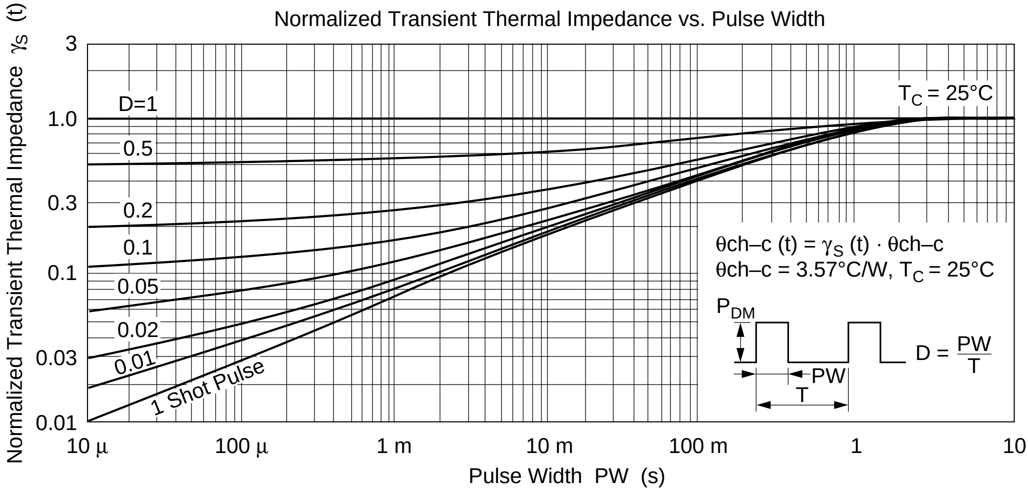
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK2116	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK2117		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK2116	I_{DSS}	—	—	250	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK2117						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	2SK2116	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 4 A, V_{GS} = 10 V *
	2SK2117		—	0.7	0.9		
Forward transfer admittance		$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance		Ciss	—	1050	—	pF	V_{DS} = 10 V
Output capacitance		Coss	—	280	—	pF	V_{GS} = 0
Reverse transfer capacitance		Crss	—	40	—	pF	f = 1 MHz
Turn–on delay time		$t_{d(on)}$	—	15	—	ns	I_D = 4 A
Rise time		t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time		$t_{d(off)}$	—	95	—	ns	R_L = 7.5 Ω
Fall time		t_f	—	40	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.95	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time		t_{rr}	—	320	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

■ See characteristic curve of 2SK1157, 2SK1158.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (T_C = 25°C)
Operation in this Area
is Limited by R_DS (on)
Ta = 25°C
2SK1567
2SK1566
1
3
10
30
100
300
1,000
Drain to Source Voltage V_DS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γS (t)
3
1.0
0.3
0.1
0.03
0.01
D=1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
T_C = 25°C
θch–c (t) = γS (t) · θch–c
θch–c = 3.57°C/W, T_C = 25°C
P_DM
PW
T
D = PW/T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

2SK2118

Silicon N Channel MOS FET

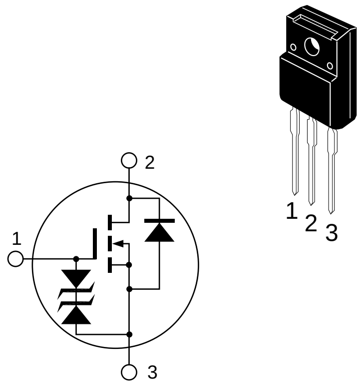
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter,Motor Control

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}{}^{*}$	20	A
Body–drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

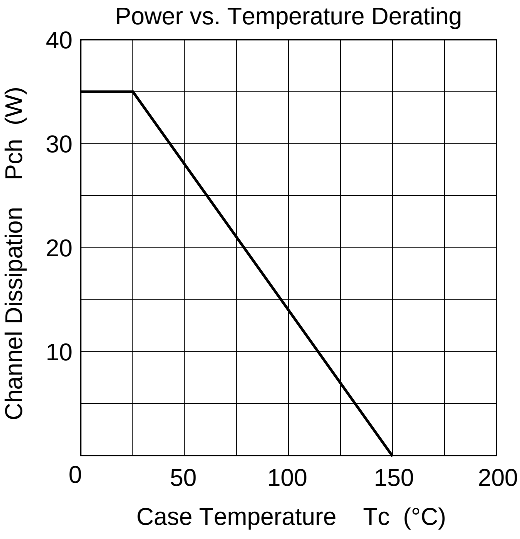
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.5	Ω	I_D = 2.5 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 2.5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1000	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	250	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	12	—	ns	I_D = 2.5 A
Rise time	t_r	—	45	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	105	—	ns	R_L = 12Ω
Fall time	t_f	—	55	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	500	—	ns	I_F = 5 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

■ See characteristic curve of 2SK1404.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

2SK2119

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

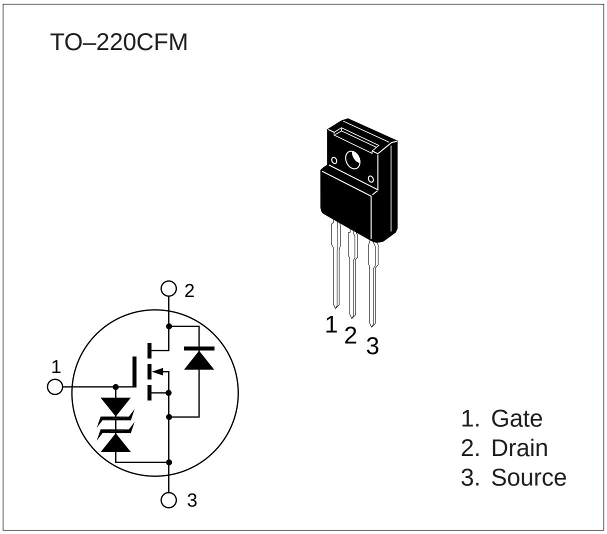


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$*	100	A
Body–drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP}***	25	A
Avalanche energy	E_{AR}***	53	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

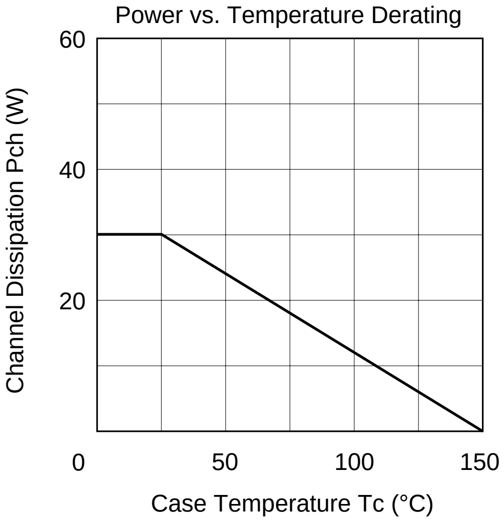
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

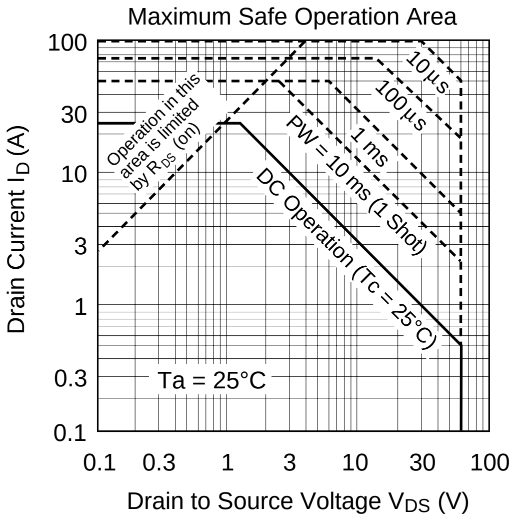
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.04	Ω	I_D = 15 A V_{GS} = 10 V *
		—	0.043	0.06	Ω	I_D = 15 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	12	21	—	S	I_D = 15 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	655	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	195	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 15 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	225	—	ns	R_L = 2 Ω
Fall time	t_f	—	145	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 25 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 25 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

■ See characteristic curve of 2SK1910.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
100
30
10
3
1
0.3
0.1
Operation in this area is limited by R_{DS} (on)
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V_{DS} (V)

2SK2120

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

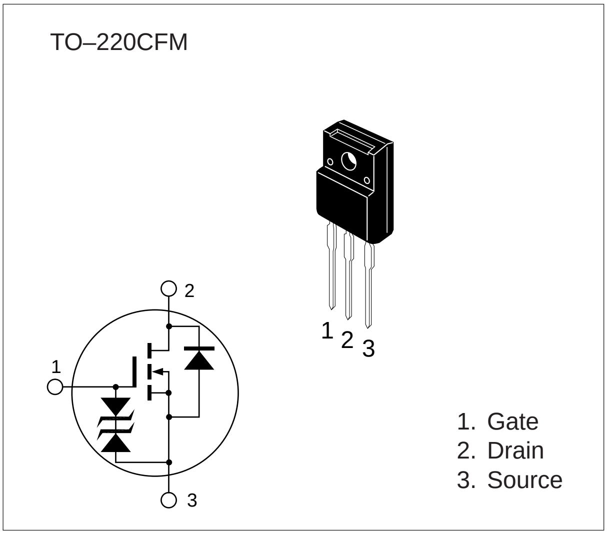


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$*	160	A
Body–drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP}***	40	A
Avalanche energy	E_{AR}***	137	mJ
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

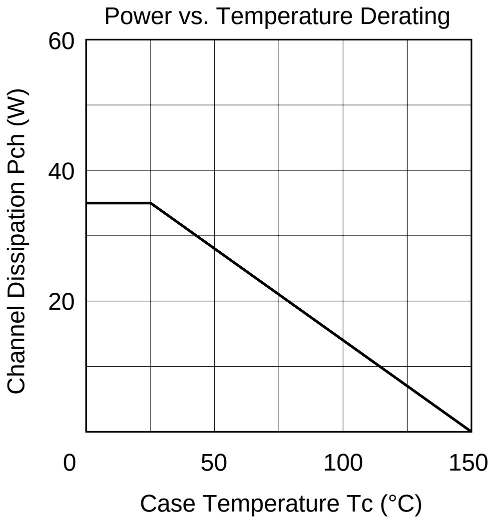
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

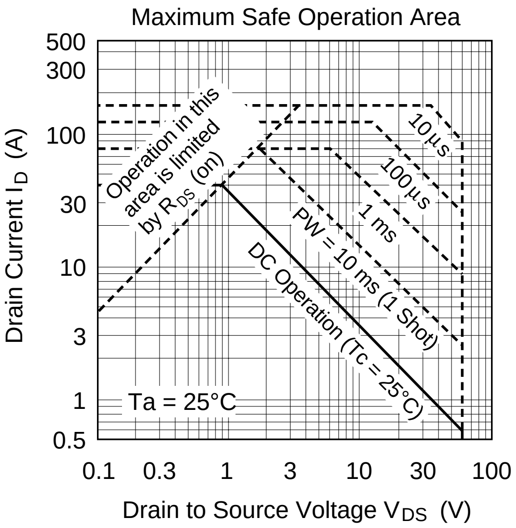
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.018	0.022	Ω	I_D = 20 A V_{GS} = 10 V *
		—	0.023	0.028	Ω	I_D = 20 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	22	35	—	S	I_D = 20 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3530	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1480	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	33	—	ns	I_D = 20 A
Rise time	t_r	—	155	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	450	—	ns	R_L = 1.5 Ω
Fall time	t_f	—	220	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 40 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

■ See characteristic curve of 2SK1911.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
60
40
20
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
500
300
100
30
10
3
1
0.5
Operation in this area is limited by R_{DS} (on)
10 μs
100 μs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Ta = 25°C
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V_{DS} (V)

2SK2121

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

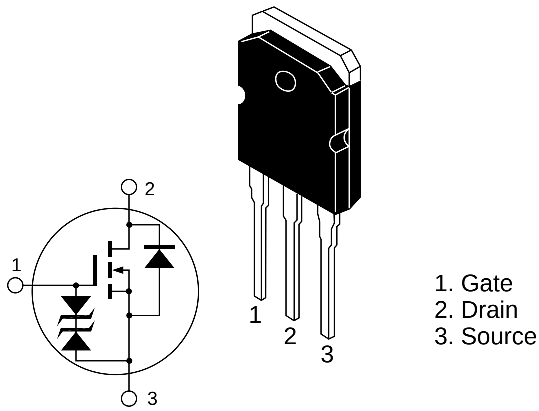


Table 1 Absolute Maximum Ratings (Ta = 25°C)

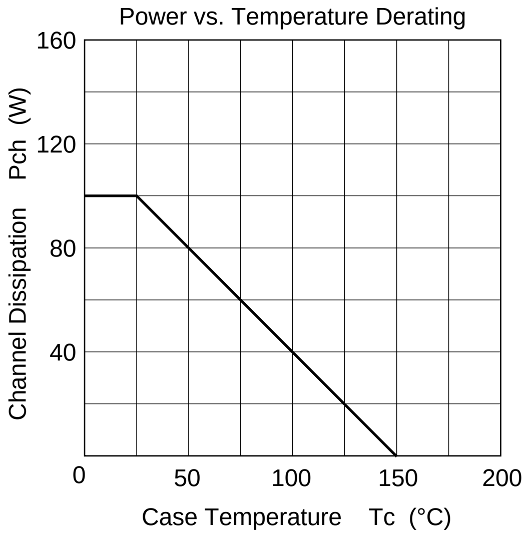
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$*	200	A
Body–drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP}***	50	A
Avalanche energy	E_{AR}***	214	mJ
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

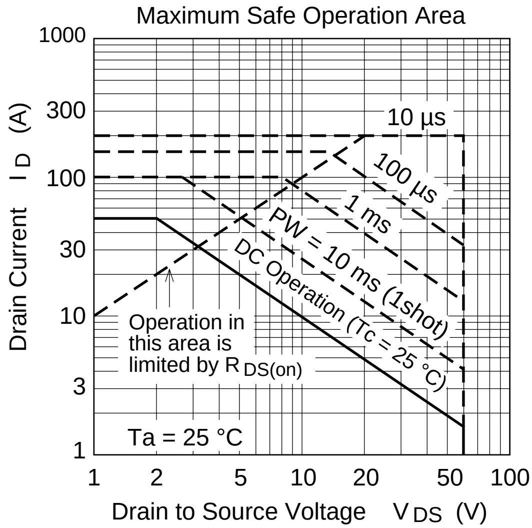
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

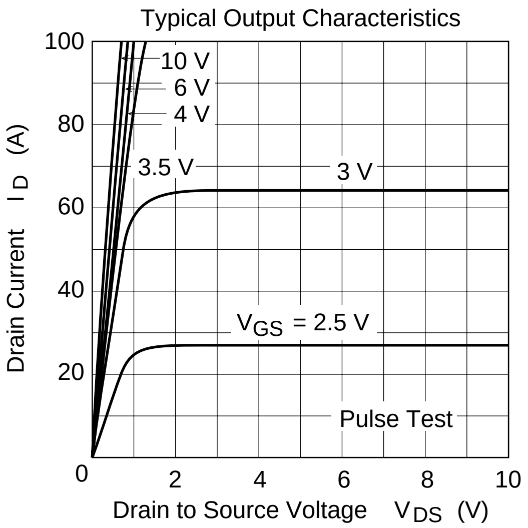
Table 2 Electrical Characteristics (Ta = 25°C)

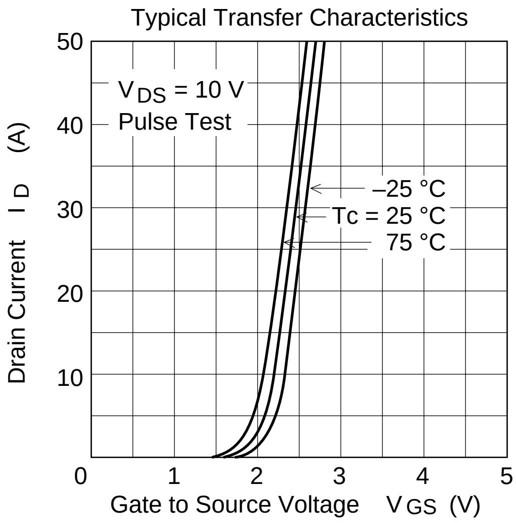
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.007	0.01	Ω	I_D = 25 A V_{GS} = 10 V *
		—	0.009	0.016	Ω	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	40	65	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	8330	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	3500	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	550	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	50	—	ns	I_D = 25 A
Rise time	t_r	—	270	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	1400	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	560	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	150	—	ns	I_F = 50 A, V_{GS} = 0, diF / dt = 50 A / µs

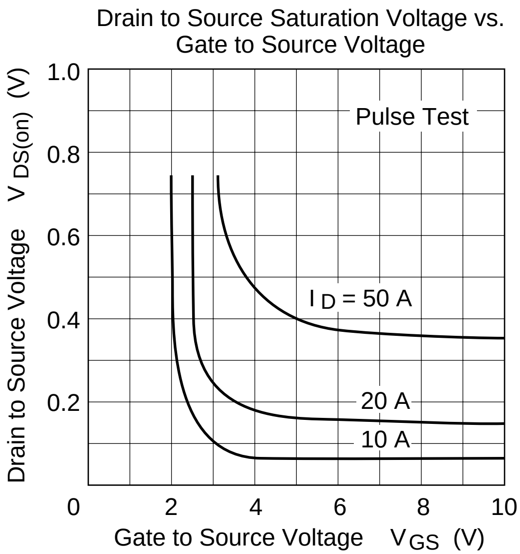
* Pulse Test

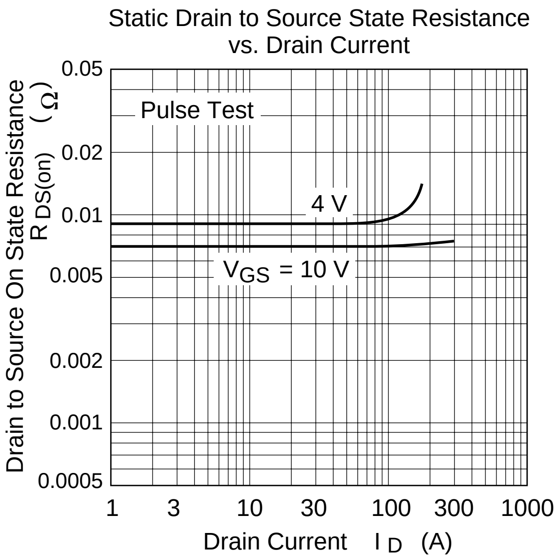

Power vs. Temperature Derating
Channel Dissipation Pch (W)
160
120
80
40
0
50
100
150
200
Case Temperature Tc (°C)

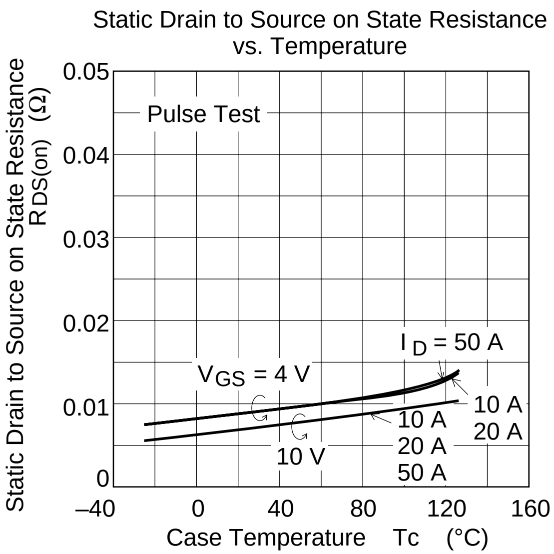

Maximum Safe Operation Area
Drain Current I D (A)
1000
300
100
30
10
3
1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1
2
5
10
20
50
100
Drain to Source Voltage V DS (V)

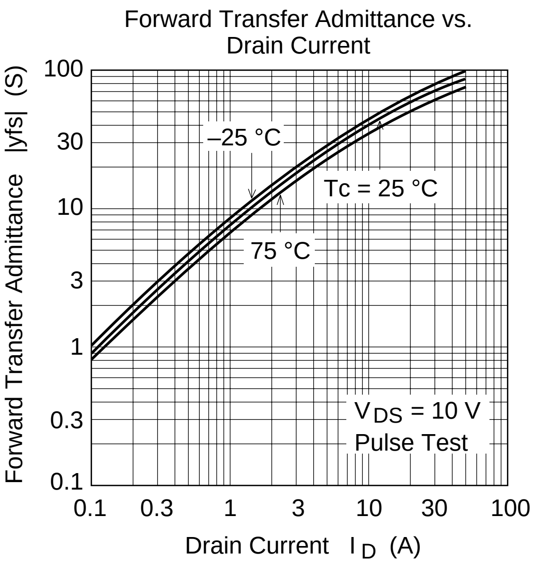

Typical Output Characteristics
Drain Current I D (A)
100
80
60
40
20
0
10 V
6 V
4 V
3.5 V
3 V
VGS = 2.5 V
Pulse Test
2
4
6
8
10
Drain to Source Voltage VDS (V)

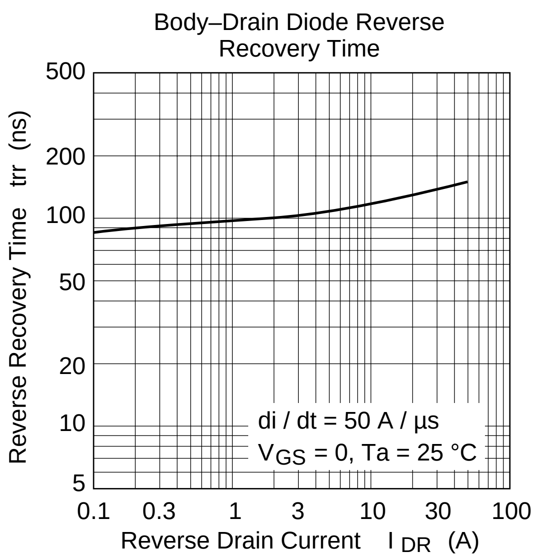

Typical Transfer Characteristics
Drain Current I D (A)
50
40
30
20
10
0
VDS = 10 V
Pulse Test
–25 °C
Tc = 25 °C
75 °C
1
2
3
4
5
Gate to Source Voltage V GS (V)

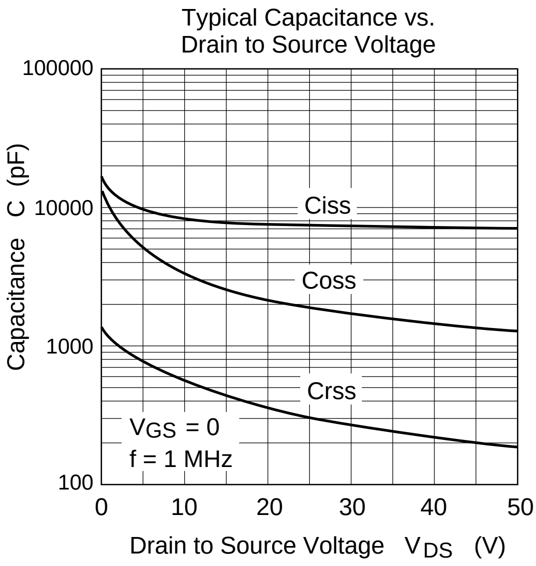

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 50 A
20 A
10 A
Drain to Source Voltage V DS(on) (V)
Gate to Source Voltage V GS (V)

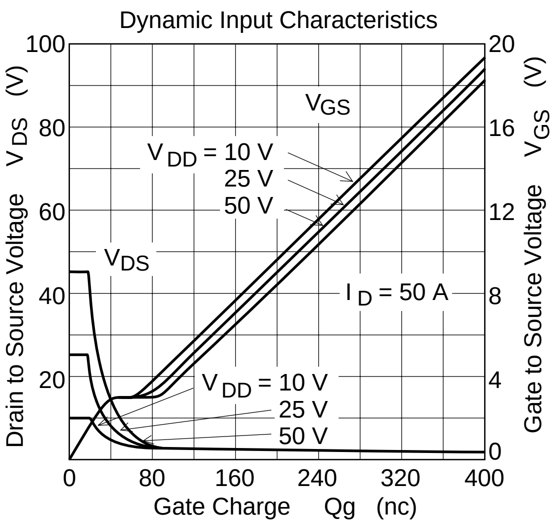

Static Drain to Source State Resistance
vs. Drain Current
Pulse Test
4 V
VGS = 10 V
Drain to Source On State Resistance R DS(on) (Ω)
Drain Current I D (A)

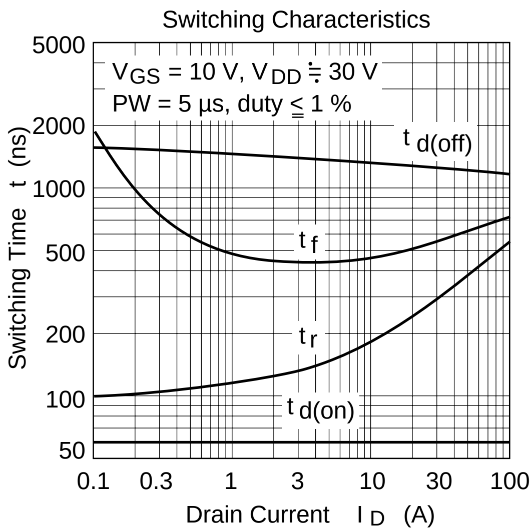

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 50 A
VGS = 4 V
10 A
20 A
10 V
10 A
20 A
50 A
Static Drain to Source on State Resistance RDS(on) (Ω)
Case Temperature Tc (°C)

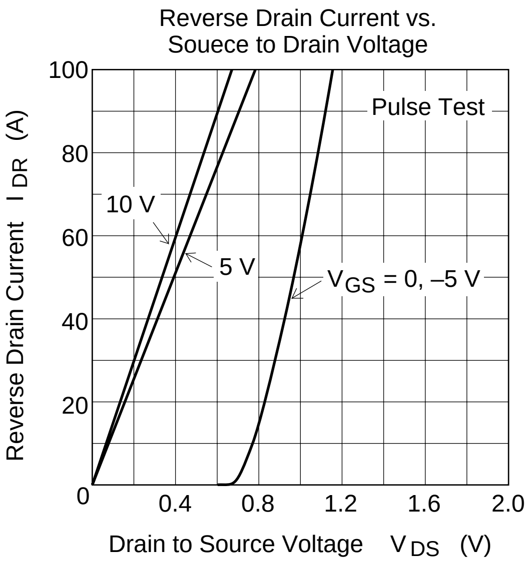

Forward Transfer Admittance vs.
Drain Current
–25 °C
Tc = 25 °C
75 °C
VDS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)

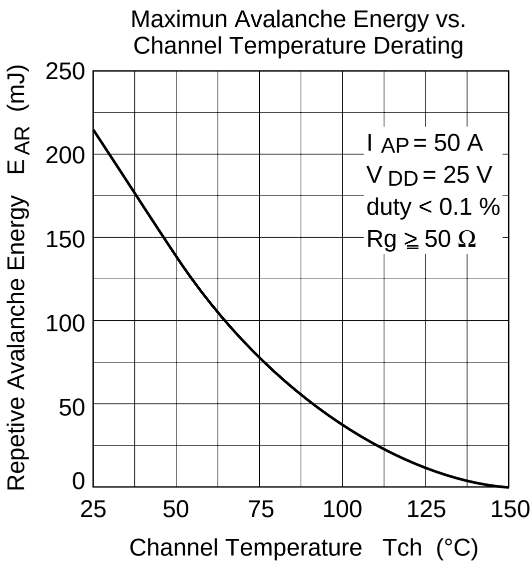

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
100000
10000
1000
100
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

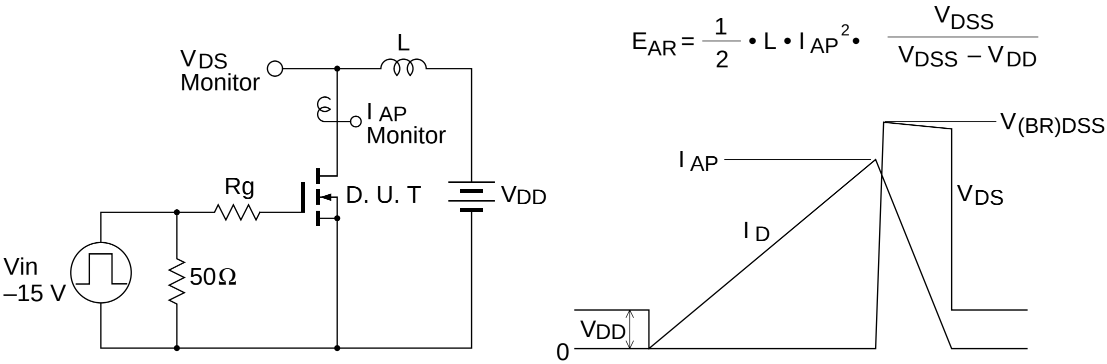

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
80
160
240
320
400
Gate Charge Qg (nc)
VGS
VDD = 10 V
25 V
50 V
VDS
ID = 50 A
VDD = 10 V
25 V
50 V


Switching Characteristics
Switching Time t (ns)
5000
2000
1000
500
200
100
50
0.1
0.3
1
3
10
30
100
Drain Current ID (A)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)

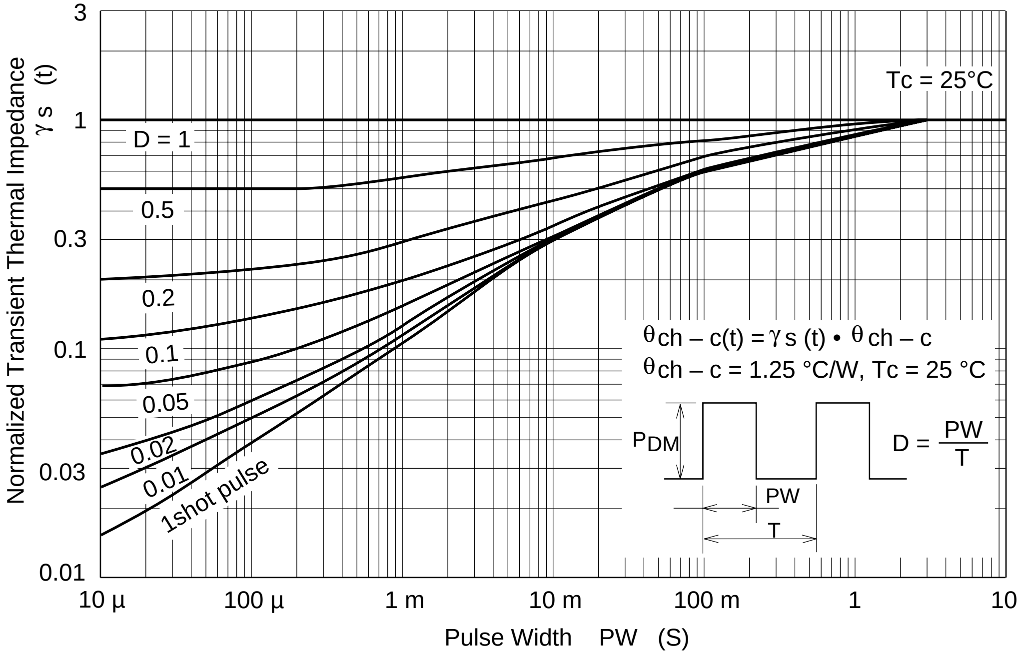




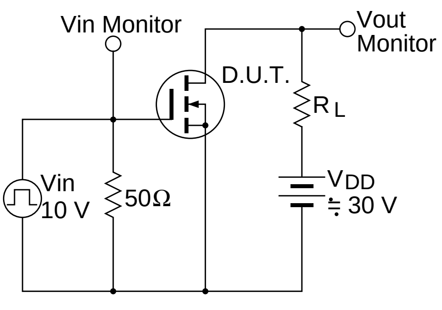
Avalanche Test Circuit and Waveform



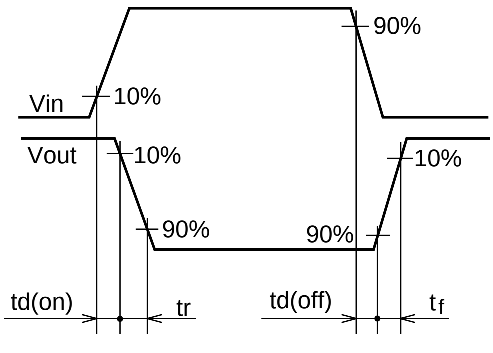
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveform



2SK2144

Silicon N Channel MOS FET

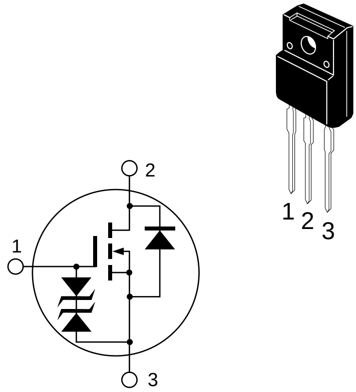
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	600	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$*	6	A
Body–drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

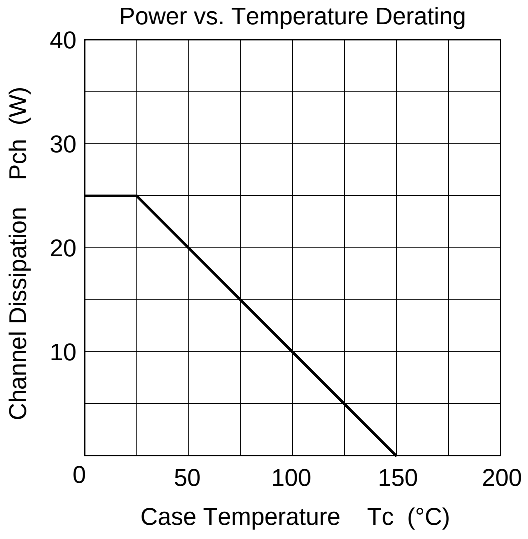
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	3.8	5.0	Ω	I_D = 1 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.2	2.0	—	S	I_D = 1 A V_{DS} = 10 V *
Input capacitance	Ciss	—	295	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	70	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	12	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = 1 A
Rise time	t_r	—	25	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 30Ω
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 2 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	220	—	ns	I_F = 2 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

■ See characteristic curve of 2SK1572.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

2SK2174(L), 2SK2174(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- No secondary breakdown
- Suitable for Switching regulator, DC – DC converter

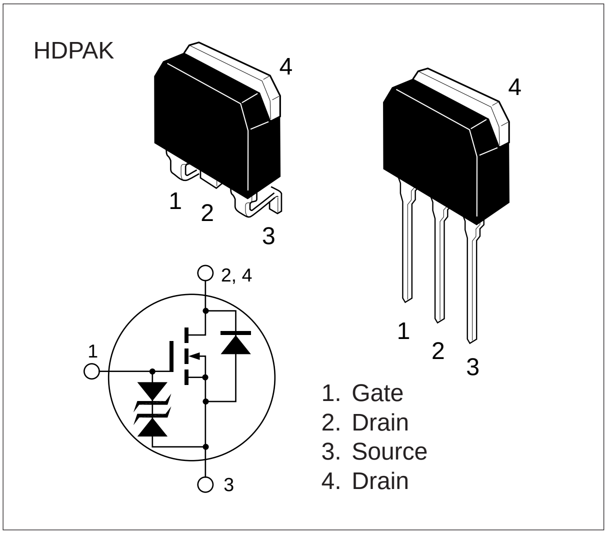


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body–drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	120	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

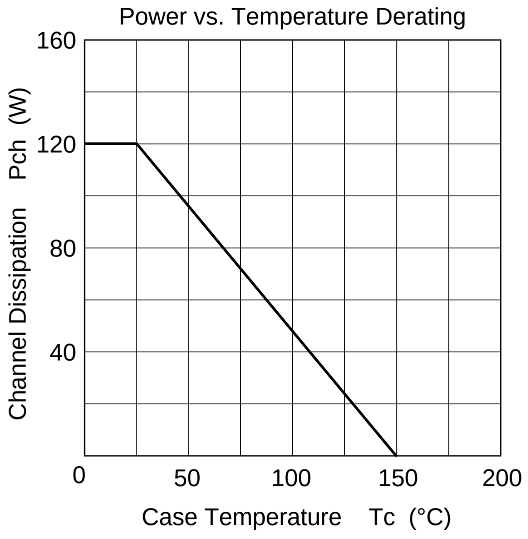
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.22	0.27	Ω	I_D = 10 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	10	16	—	S	I_D = 10 A V_{DS} = 10 V *
Input capacitance	Ciss	—	2800	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	780	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	90	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	32	—	ns	I_D = 10 A
Rise time	t_r	—	115	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	200	—	ns	R_L = 3 Ω
Fall time	t_f	—	90	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	500	—	µs	I_F = 20 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

■ See characteristic curves of 2SK1170.



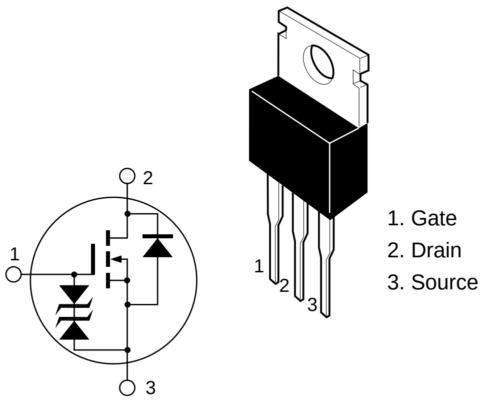
Power vs. Temperature Derating
160
120
80
40
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

2SK2175

Silicon N Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body–drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP}***	10	A
Avalanche energy	E_{AR}***	8.5	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

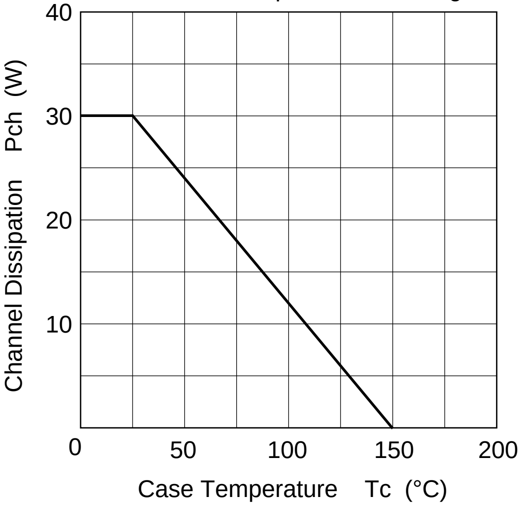
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

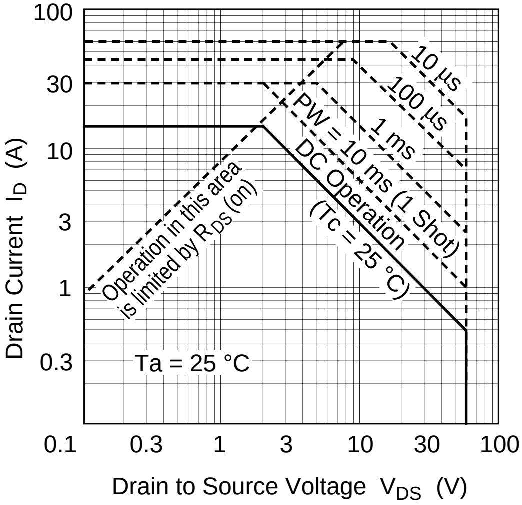
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.10	0.13	Ω	I_D = 8 A V_{GS} = 10 V *
		—	0.13	0.18	Ω	I_D = 8 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	4.5	8	—	S	I_D = 8 A V_{DS} = 10 V *
Input capacitance	Ciss	—	390	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	190	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 8 A
Rise time	t_r	—	65	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	90	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	90	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.3	—	V	I_F = 15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	ns	I_F = 15 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

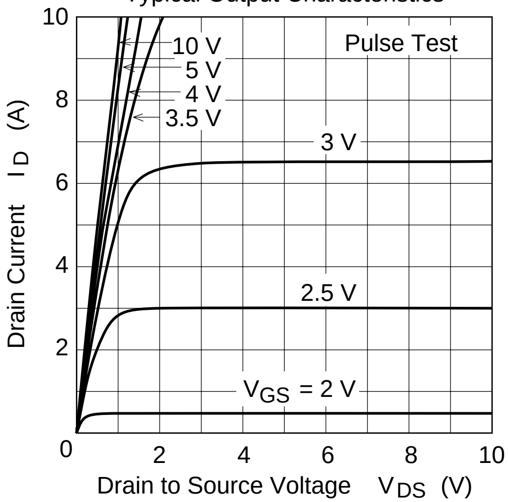
Power vs. Temperature Derating



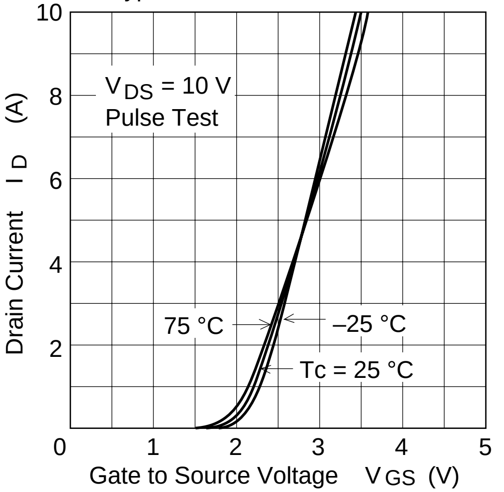
Maximum Safe Operation Area

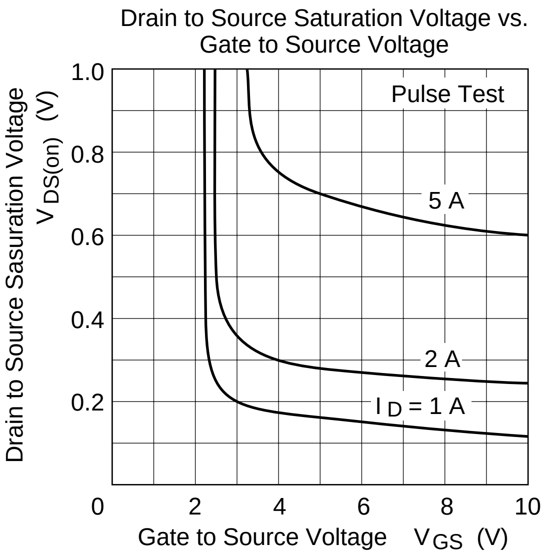


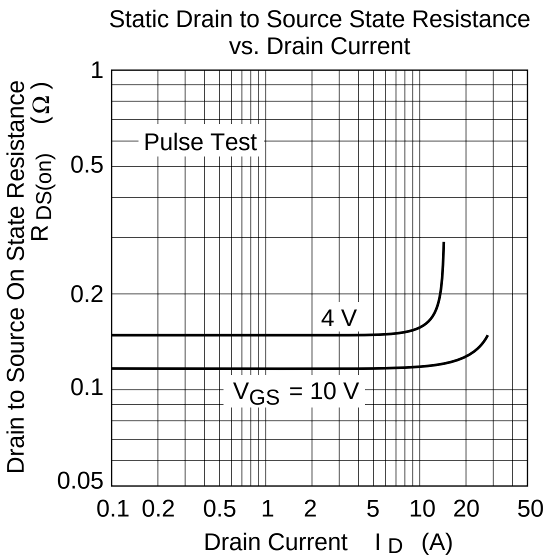
Typical Output Characteristics

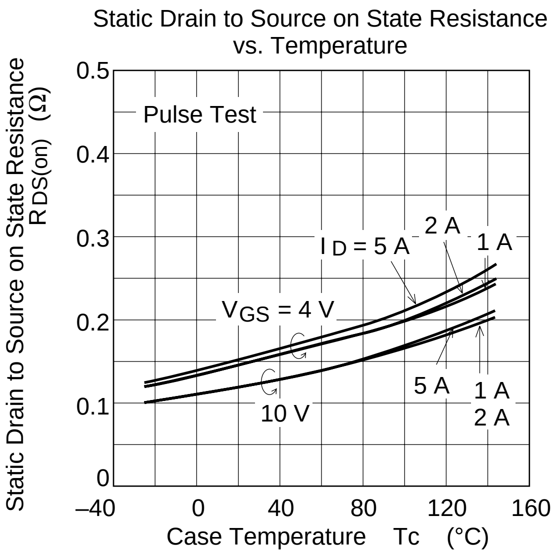


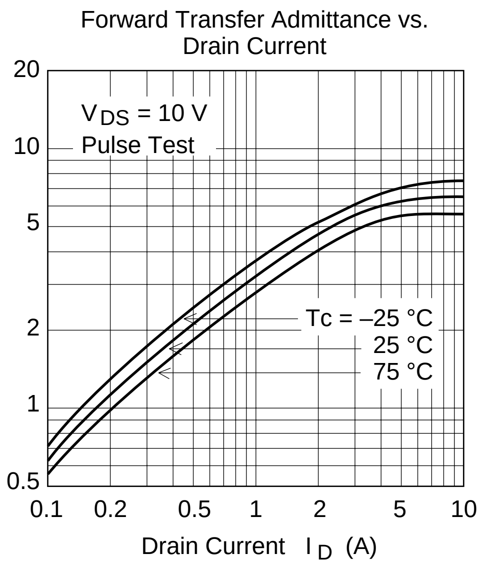
Typical Transfer Characteristics



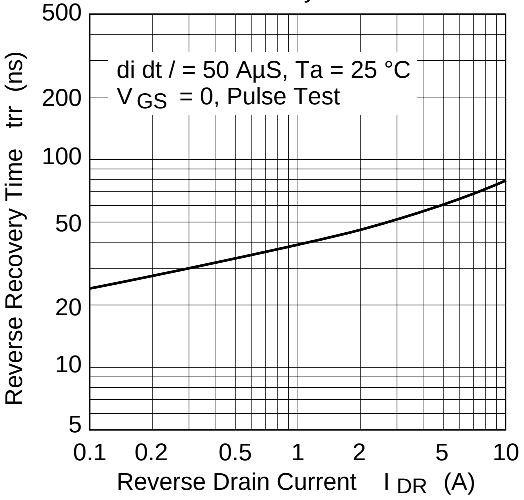

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
5 A
2 A
I D = 1 A
Drain to Source Sasuration Voltage
V DS(on) (V)
1.0
0.8
0.6
0.4
0.2
0
2
4
6
8
10
Gate to Source Voltage V GS (V)


Static Drain to Source State Resistance
vs. Drain Current
Pulse Test
4 V
V GS = 10 V
Drain to Source On State Resistance
R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.1
0.2
0.5
1
2
5
10
20
50
Drain Current I D (A)

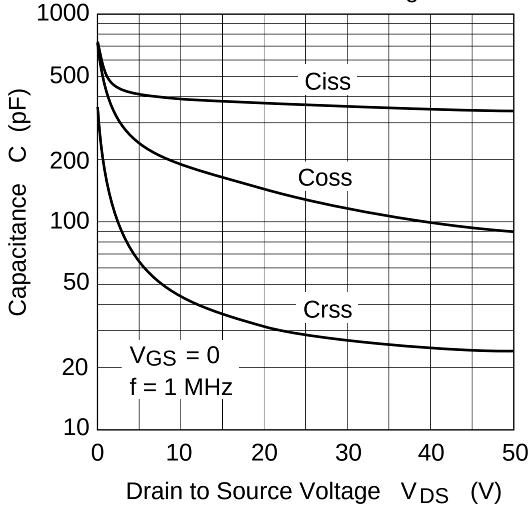

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 5 A
2 A
1 A
V GS = 4 V
10 V
5 A
1 A
2 A
Static Drain to Source on State Resistance
R DS(on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
V DS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

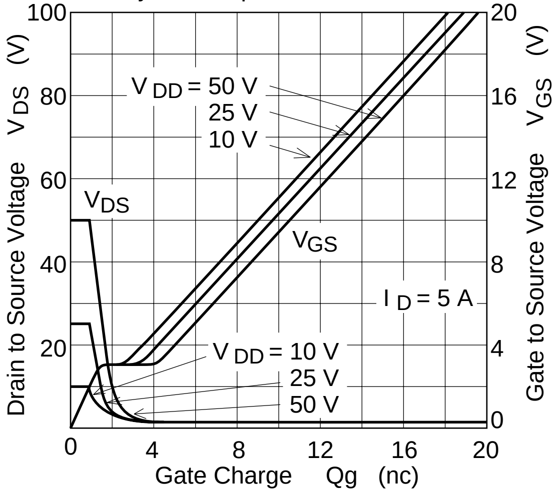
Body–Drain Diode Reverse Recovery Time



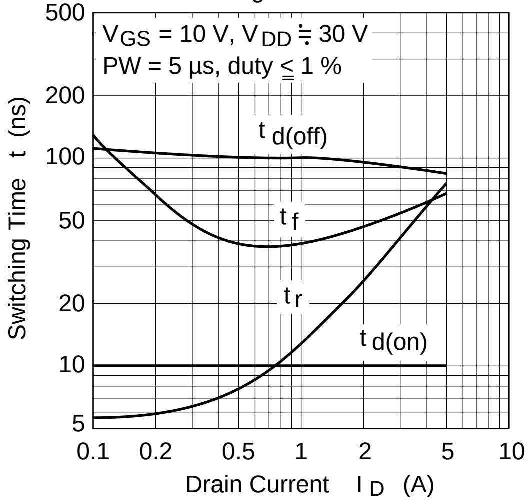
Typical Capacitance vs. Drain to Source Voltage

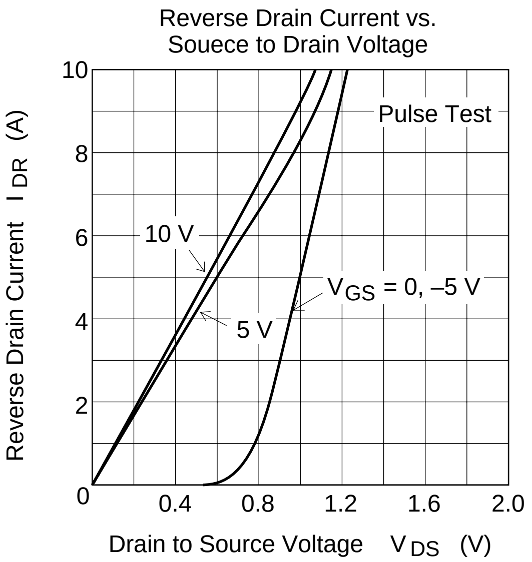


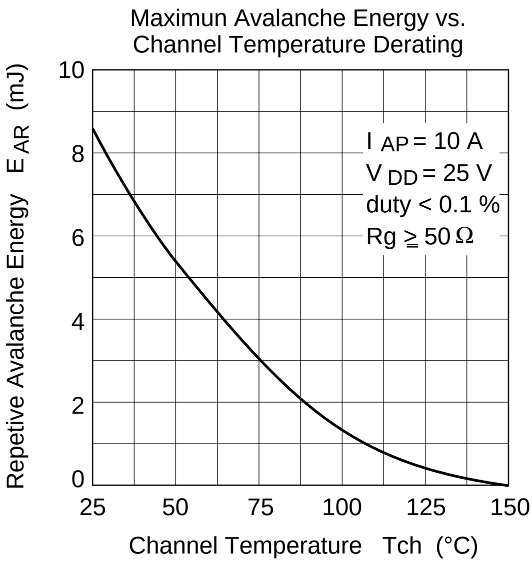
Dynamic Input Characteristics



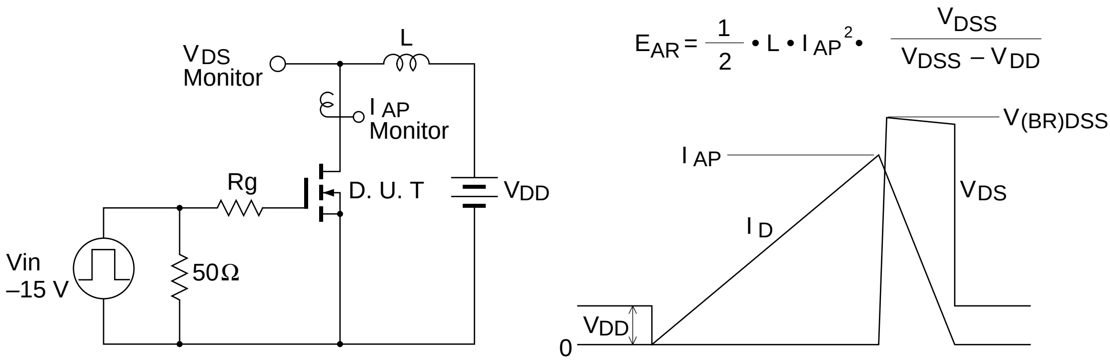
Switching Characteristics



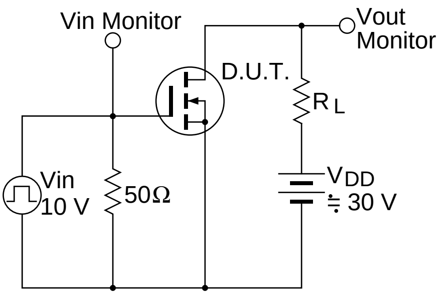




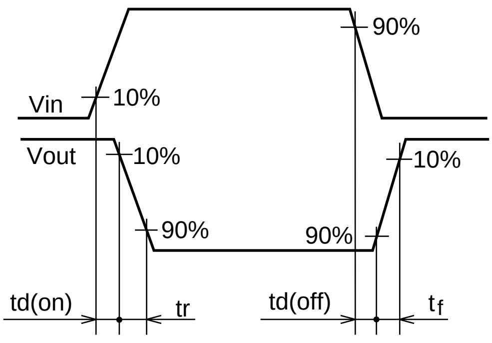
Avalanche Test Circuit and Waveform



Switching Time Test Circuit



Waveform



2SK2202

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter

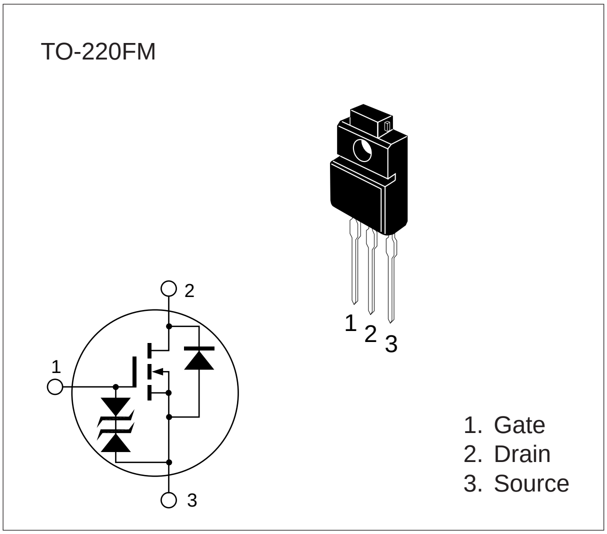


Table 1 Absolute Maximum Ratings (Ta = 25°C)

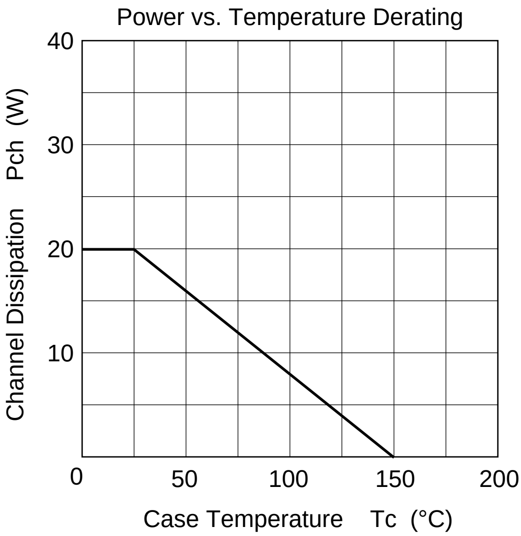
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	120	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	14	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

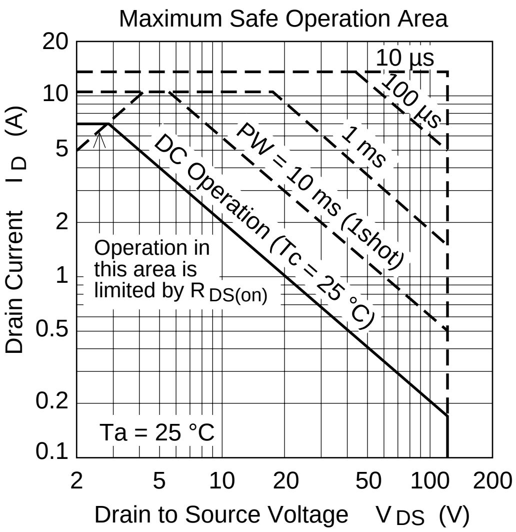
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

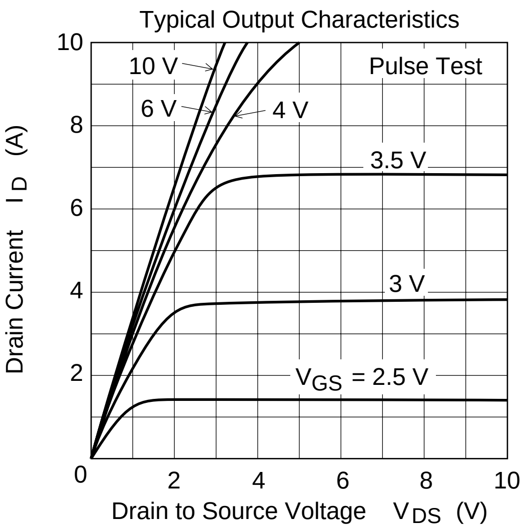
Table 2 Electrical Characteristics (Ta = 25°C)

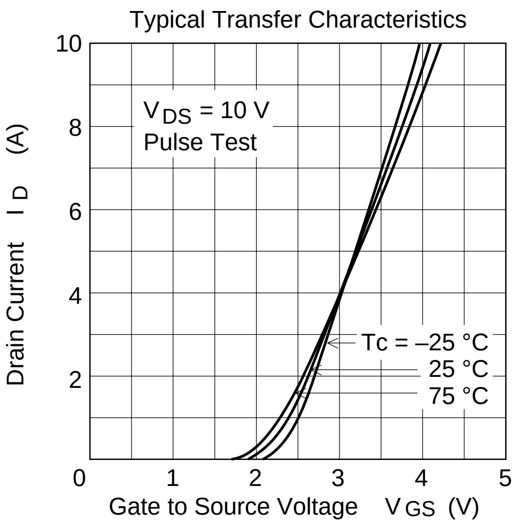
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	120	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.4	Ω	I_D = 4 A V_{GS} = 10 V *
		—	0.35	0.55	Ω	I_D = 4 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	420	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	140	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	35	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	9	—	ns	I_D = 4 A
Rise time	t_r	—	50	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	140	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	65	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.35	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	320	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 50 A / µs

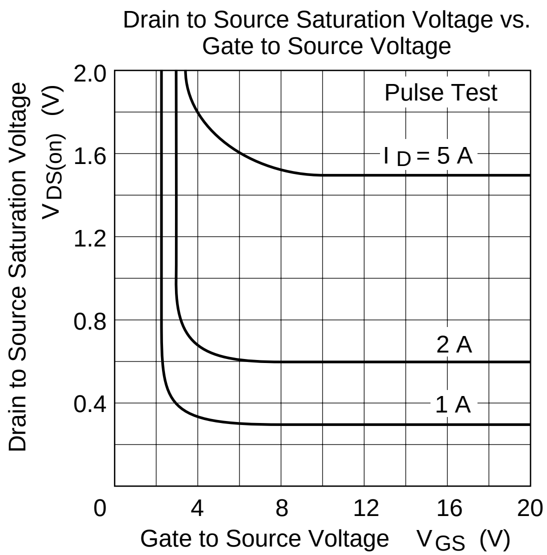
* Pulse Test

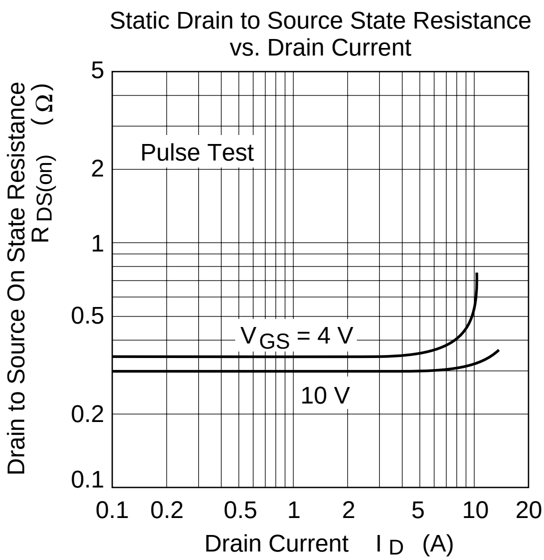

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

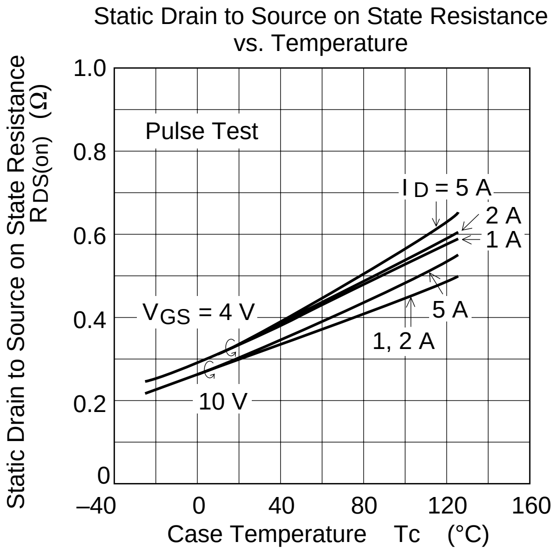

Maximum Safe Operation Area
Drain Current I D (A)
Drain to Source Voltage V DS (V)
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
20
10
5
2
1
0.5
0.2
0.1
2
5
10
20
50
100
200

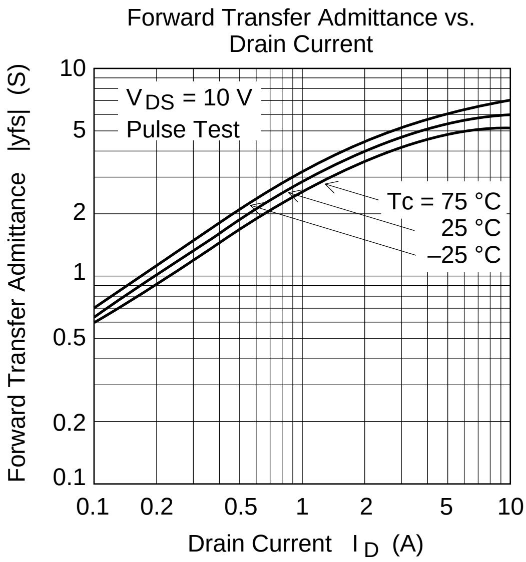

Typical Output Characteristics
Drain Current I D (A)
Drain to Source Voltage V DS (V)
10 V
6 V
4 V
Pulse Test
3.5 V
3 V
VGS = 2.5 V
10
8
6
4
2
0
2
4
6
8
10

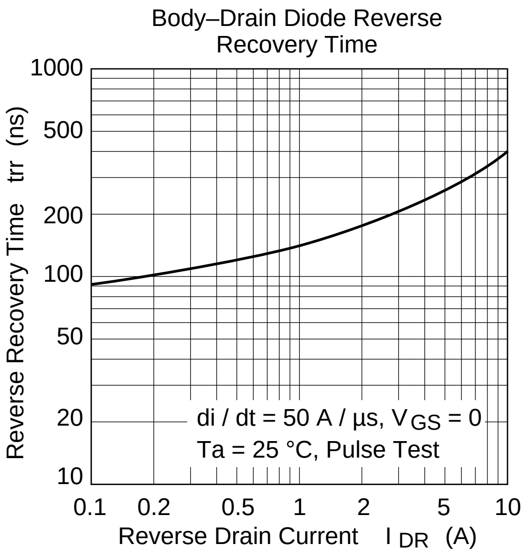

Typical Transfer Characteristics
Drain Current I D (A)
Gate to Source Voltage V GS (V)
VDS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
10
8
6
4
2
0
1
2
3
4
5

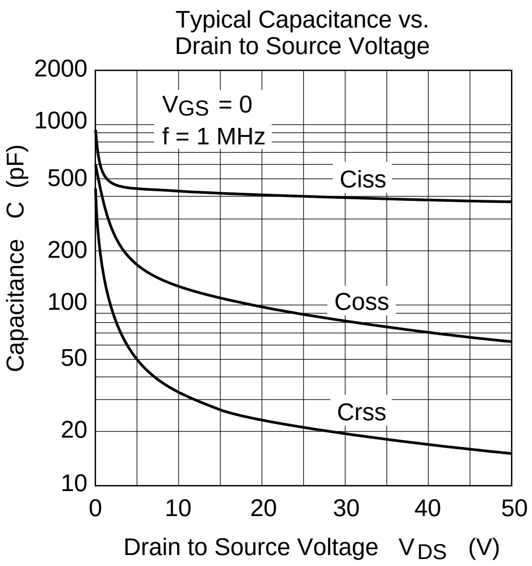

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage
VDS(on) (V)
2.0
1.6
1.2
0.8
0.4
0
4
8
12
16
20
Gate to Source Voltage VGS (V)
Pulse Test
I D = 5 A
2 A
1 A

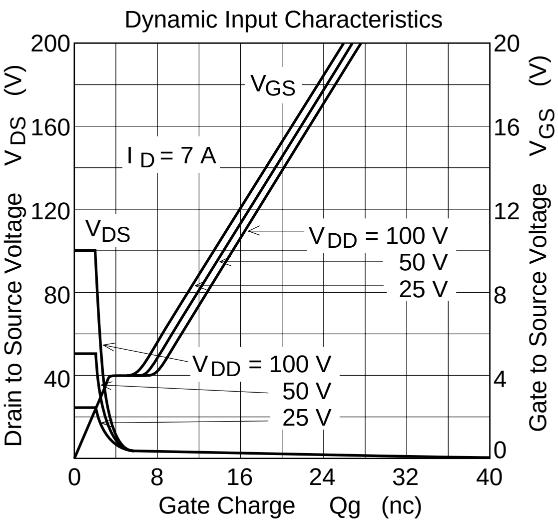

Static Drain to Source State Resistance
vs. Drain Current
Drain to Source On State Resistance
RDS(on) (Ω)
5
2
1
0.5
0.2
0.1
0.1
0.2
0.5
1
2
5
10
20
Drain Current I D (A)
Pulse Test
VGS = 4 V
10 V

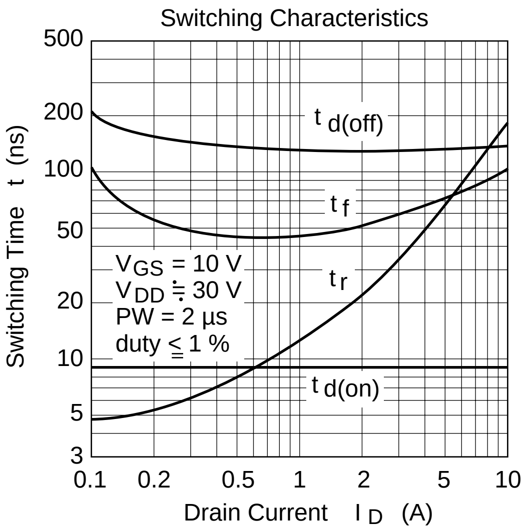

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance
RDS(on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160
Case Temperature Tc (°C)
Pulse Test
I D = 5 A
2 A
1 A
VGS = 4 V
5 A
1, 2 A
10 V

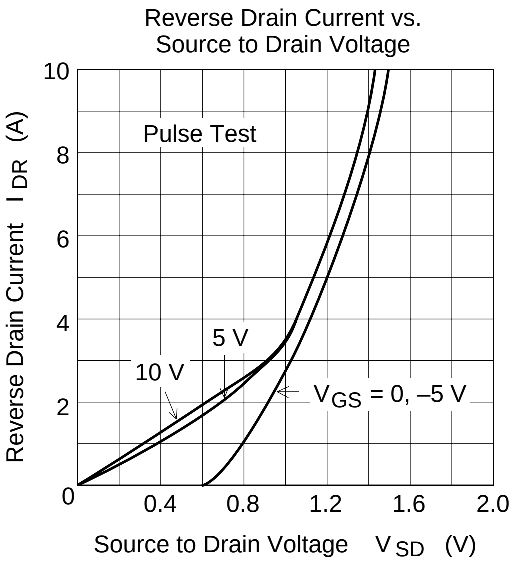

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
10
5
2
1
0.5
0.2
0.1
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)
VDS = 10 V
Pulse Test
Tc = 75 °C
25 °C
–25 °C

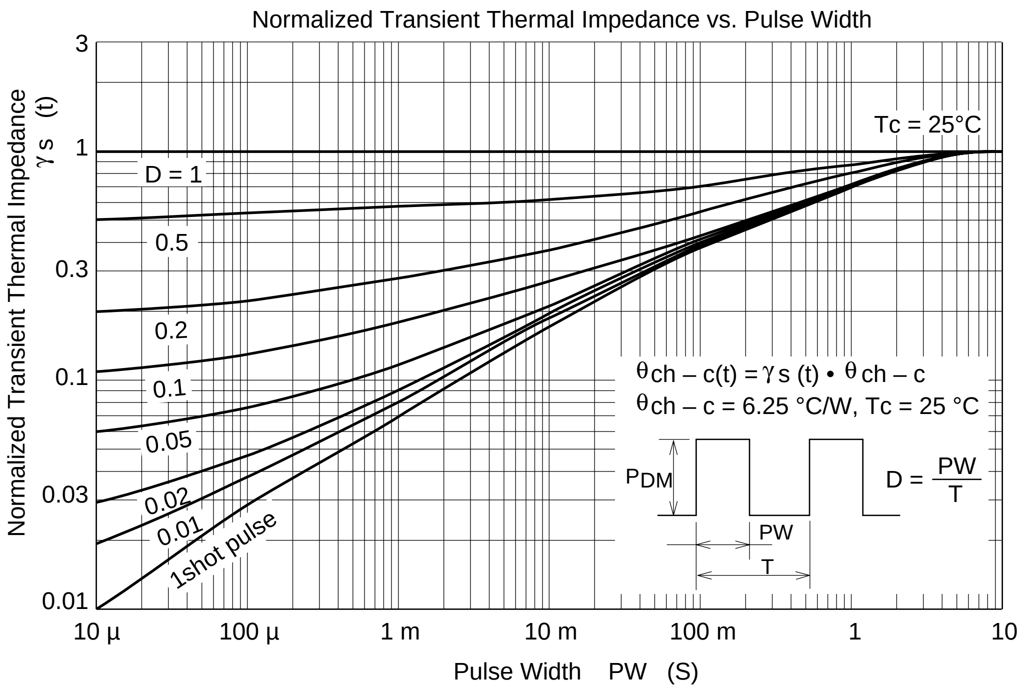

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 50 A / µs, VGS = 0
Ta = 25 °C, Pulse Test
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
2000
1000
500
200
100
50
20
10
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

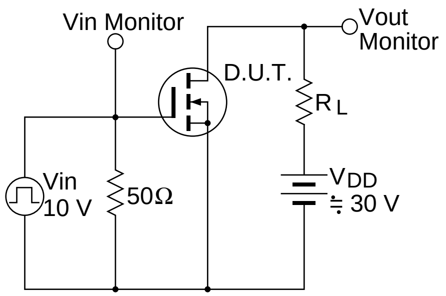

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
200
160
120
80
40
VGS
I D = 7 A
VDS
VDD = 100 V
50 V
25 V
VDD = 100 V
50 V
25 V
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
3
t d(off)
t f
t r
t d(on)
VGS = 10 V
VDD ≒ 30 V
PW = 2 µs
duty ≦ 1 %
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

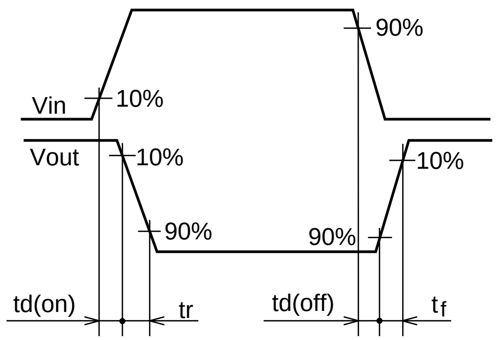

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
Reverse Drain Current I DR (A)
10
8
6
4
2
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V SD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Switching Time Test Circuit



Waveform



2SK2203

Silicon N Channel MOS FET

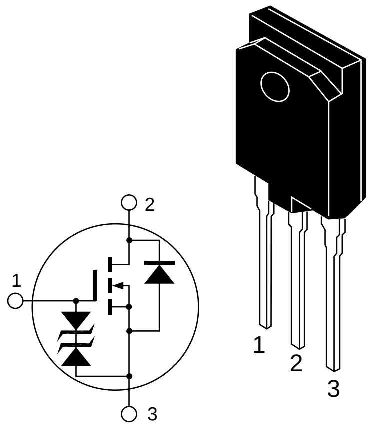
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V cource
- Suitable for Switching regulator, DC – DC converter

TO–3PFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$*	200	A
Body–drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP}***	50	A
Avalanche energy	E_{AR}***	214	mJ
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

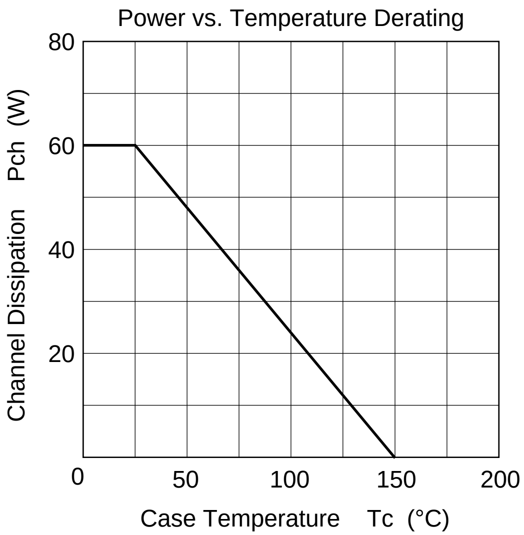
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

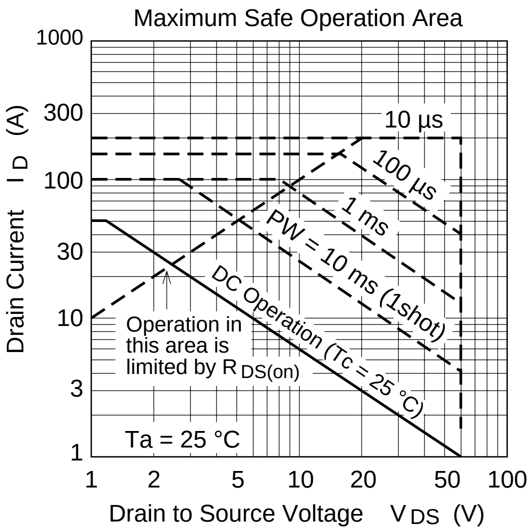
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	V_{DS} = 25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.007	0.01	Ω	I_D = 25 A V_{GS} = 10 V *
		—	0.009	0.013	Ω	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	40	65	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	8330	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	3500	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	550	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	50	—	ns	I_D = 25 A
Rise time	t_r	—	270	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	1400	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	560	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	150	—	ns	I_F = 50 A, V_{GS} = 0, diF / dt = 50 A / μs

* Pulse Test

See characteristic curves of 2SK2121.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
1000
300
100
30
10
3
1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1
2
5
10
20
50
100
Drain to Source Voltage V DS (V)

2SK2204(L), 2SK2204(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V cource
- Suitable for Switching regulator, DC – DC converter

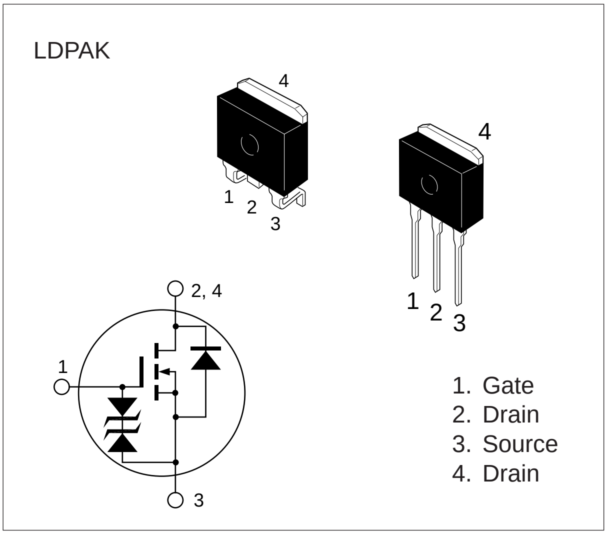


Table 1 Absolute Maximum Ratings (Ta = 25°C)

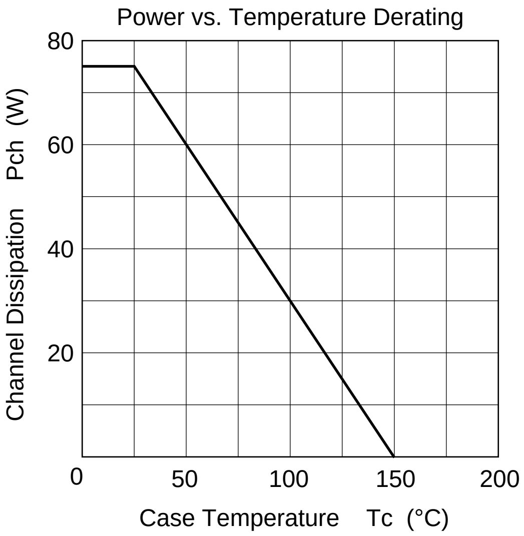
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	45	A
Drain peak current	I_D*	180	A
Body–drain diode reverse drain current	I_{DR}	45	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

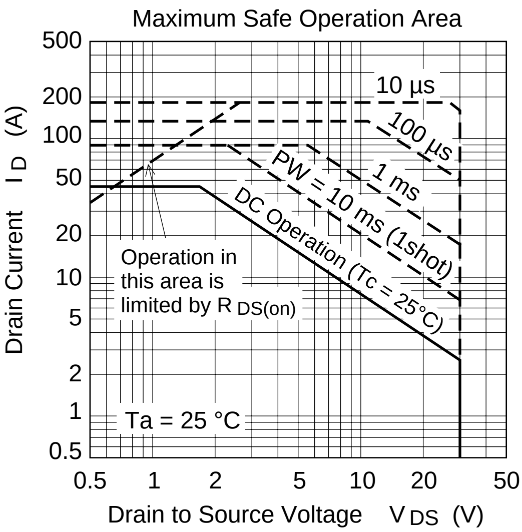
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

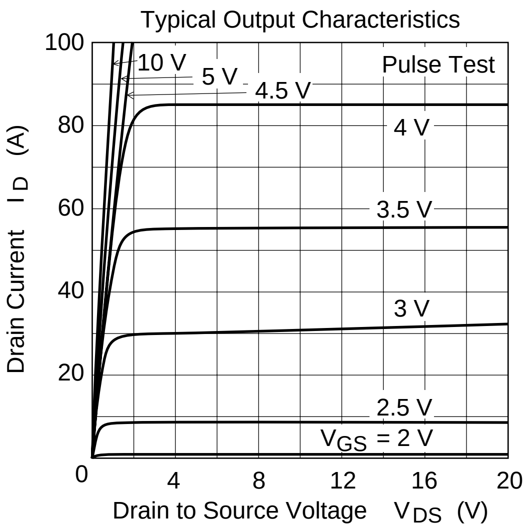
Table 2 Electrical Characteristics (Ta = 25°C)

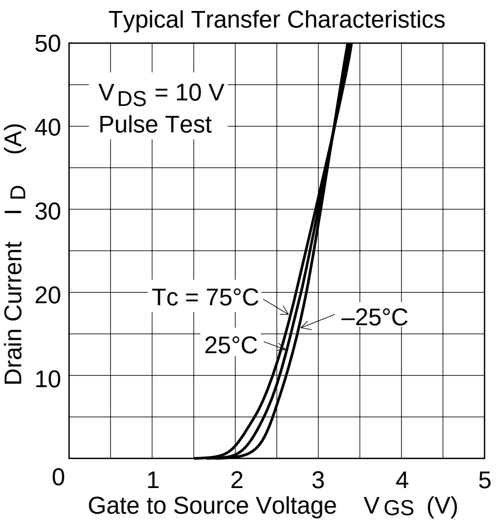
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.011	0.015	Ω	I_D = 25 A V_{GS} = 10 V *
		—	0.016	0.022	Ω	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	23	38	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3600	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	2000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	400	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 25 A
Rise time	t_r	—	230	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	435	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	360	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 45 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	75	—	ns	I_F = 45 A, V_{GS} = 0, diF / dt = 50 A / µs

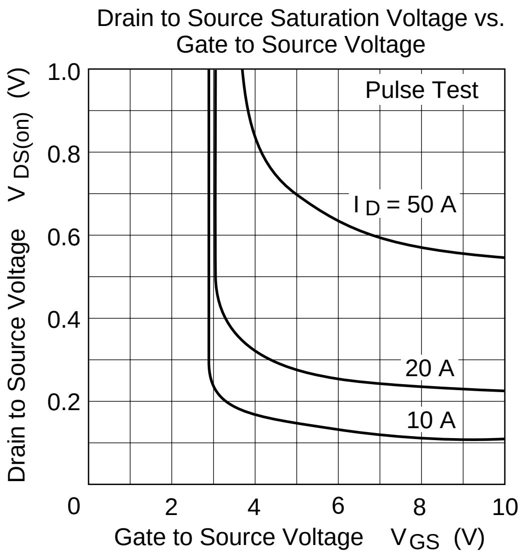
* Pulse Test

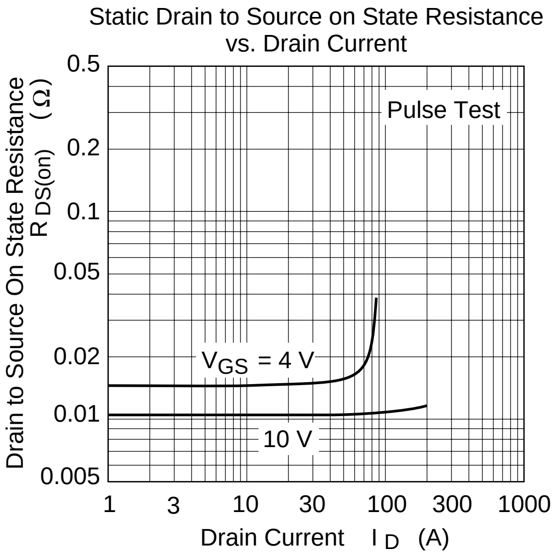

Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)

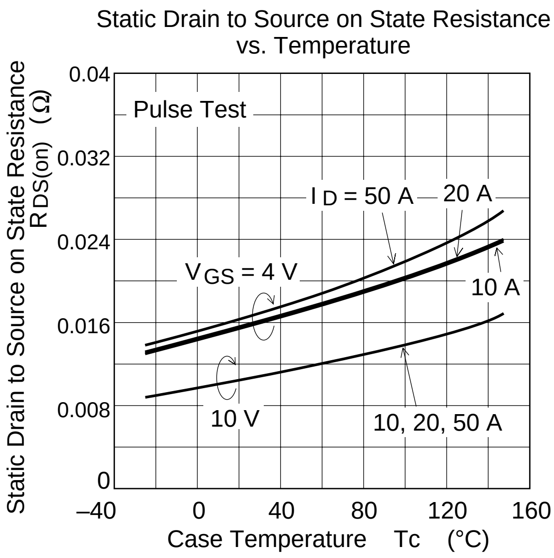

Maximum Safe Operation Area
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.5
1
2
5
10
20
50
Drain to Source Voltage V DS (V)

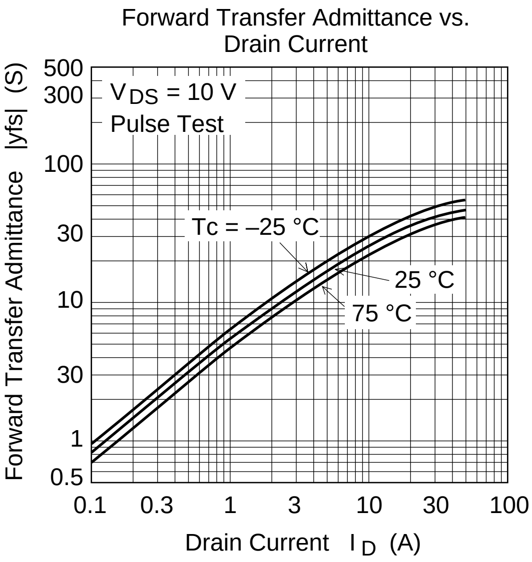

Typical Output Characteristics
Drain Current I D (A)
100
80
60
40
20
0
10 V
5 V
4.5 V
Pulse Test
4 V
3.5 V
3 V
2.5 V
VGS = 2 V
4
8
12
16
20
Drain to Source Voltage V DS (V)

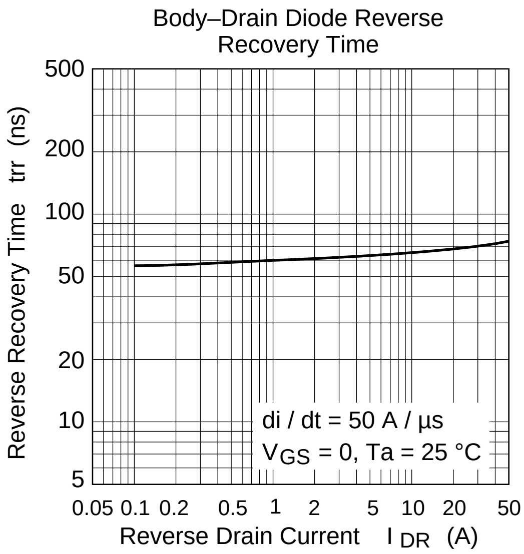

Typical Transfer Characteristics
Drain Current I D (A)
50
40
30
20
10
0
V DS = 10 V
Pulse Test
Tc = 75°C
–25°C
25°C
1
2
3
4
5
Gate to Source Voltage V GS (V)

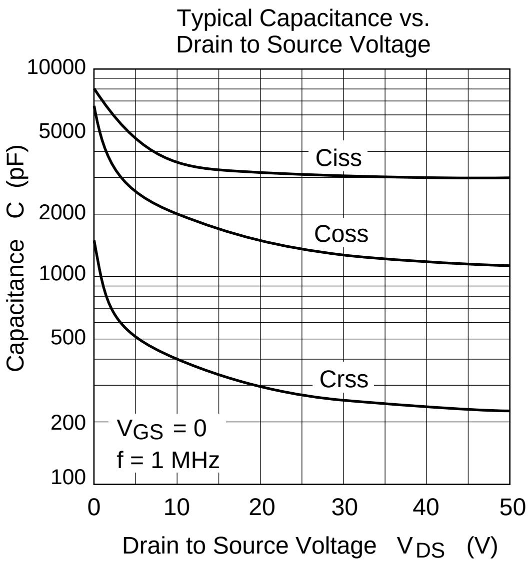

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Voltage V DS(on) (V)
1.0
0.8
0.6
0.4
0.2
0
2
4
6
8
10
Pulse Test
I D = 50 A
20 A
10 A
Gate to Source Voltage V GS (V)

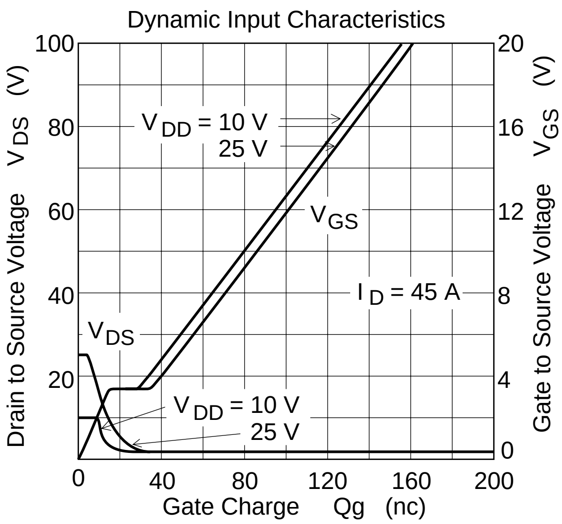

Static Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
0.5
0.2
0.1
0.05
0.02
0.01
0.005
Pulse Test
VGS = 4 V
10 V
1
3
10
30
100
300
1000
Drain Current I D (A)

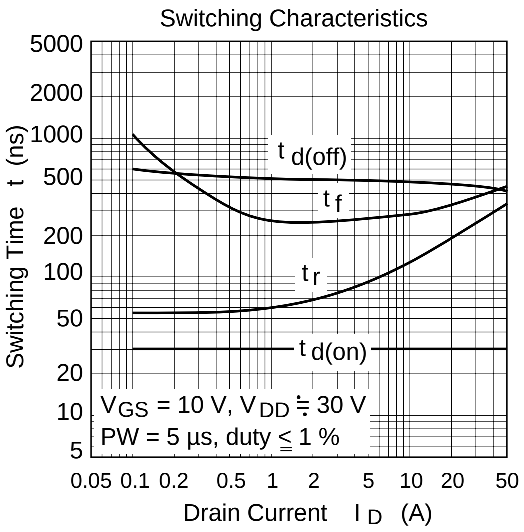

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance RDS(on) (Ω)
0.04
0.032
0.024
0.016
0.008
0
Pulse Test
I D = 50 A
20 A
10 A
VGS = 4 V
10 V
10, 20, 50 A
–40
0
40
80
120
160
Case Temperature Tc (°C)

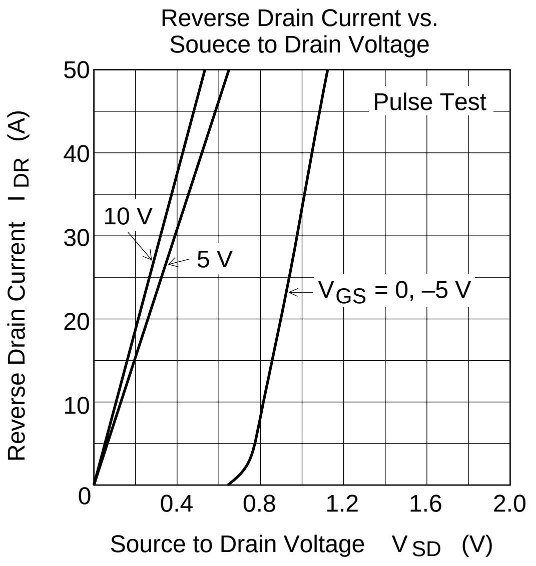

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
500
300
100
30
10
30
1
0.5
VDS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
0.1
0.3
1
3
10
30
100
Drain Current I D (A)

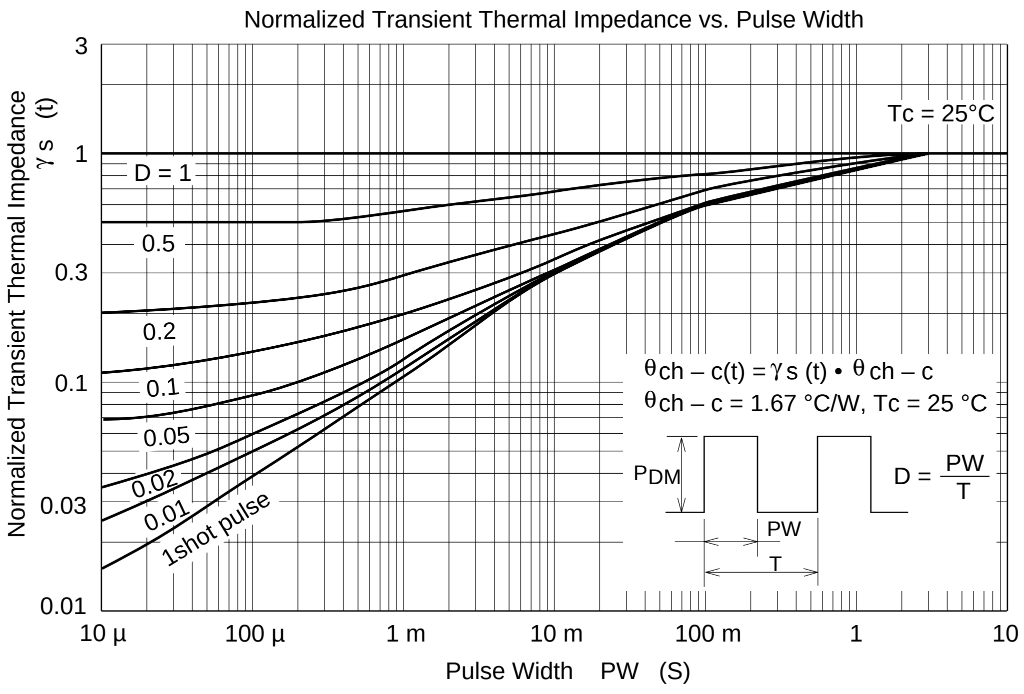

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.05 0.1 0.2 0.5 1 2 5 10 20 50
Reverse Drain Current I DR (A)
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
5000
2000
1000
500
200
100
0 10 20 30 40 50
Drain to Source Voltage V DS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

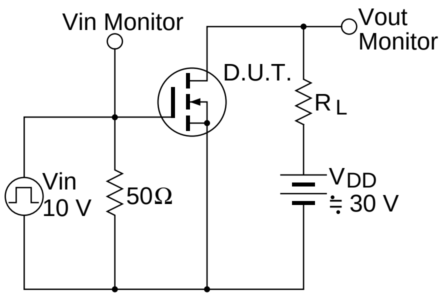

Dynamic Input Characteristics
Drain to Source Voltage V DS (V)
Gate to Source Voltage V GS (V)
100
80
60
40
20
20
16
12
8
4
0
0 40 80 120 160 200
Gate Charge Qg (nc)
V DD = 10 V
25 V
VGS
I D = 45 A
VDS
V DD = 10 V
25 V


Switching Characteristics
Switching Time t (ns)
5000
2000
1000
500
200
100
50
20
10
5
0.05 0.1 0.2 0.5 1 2 5 10 20 50
Drain Current I D (A)
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≤ 1 %

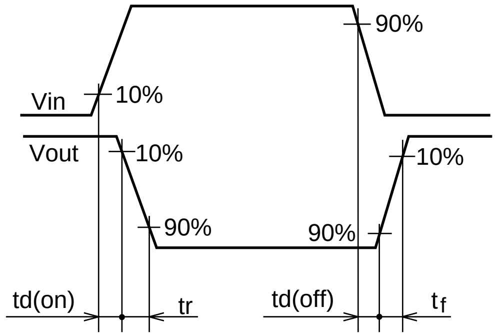

Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
Reverse Drain Current I DR (A)
Source to Drain Voltage V SD (V)
0
10
20
30
40
50
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 1.67 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
3
1
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Waveform

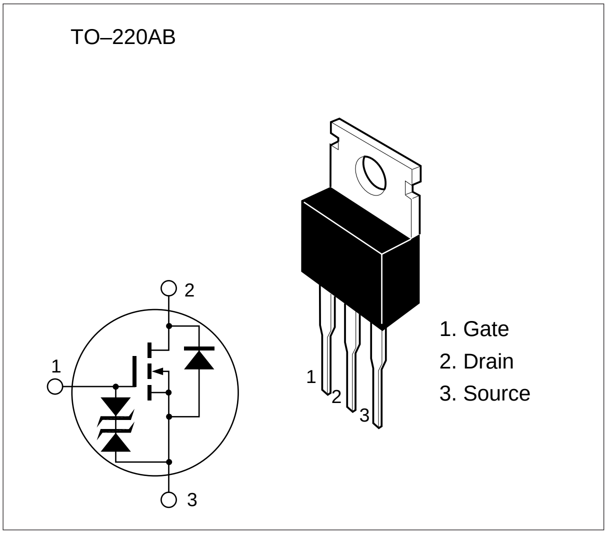


2SK2205

Silicon N Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- Low drive current
- High speed switching
- 4 V gate drive device can be driven from 5 V source
- Suitable for DC – DC converter, Motor control

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	45	A
Drain peak current	I_D*	180	A
Body–drain diode reverse drain current	I_{DR}	45	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

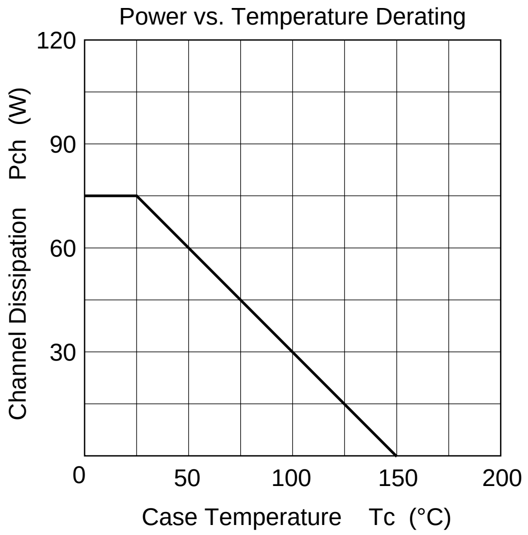
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.011	0.015	Ω	I_D = 25 A V_{GS} = 10 V *
		—	0.016	0.022	Ω	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	23	38	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3600	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	2000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	400	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 25 A
Rise time	t_r	—	230	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	435	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	360	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 45 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	75	—	ns	I_F = 45 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

■ See characteristic curve of 2SK2204.


Power vs. Temperature Derating
120
90
60
30
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

2SK2206

Silicon N Channel MOS FET

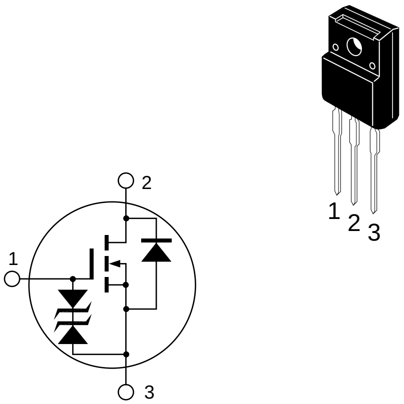
Application

High speed power switching

Features

- Low on–resistance
- Low drive current
- High speed switching
- 4 V gate drive device can be driven from 5 V source
- Suitable for DC – DC converter, Motor control

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	45	A
Drain peak current	I_D*	180	A
Body–drain diode reverse drain current	I_{DR}	45	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

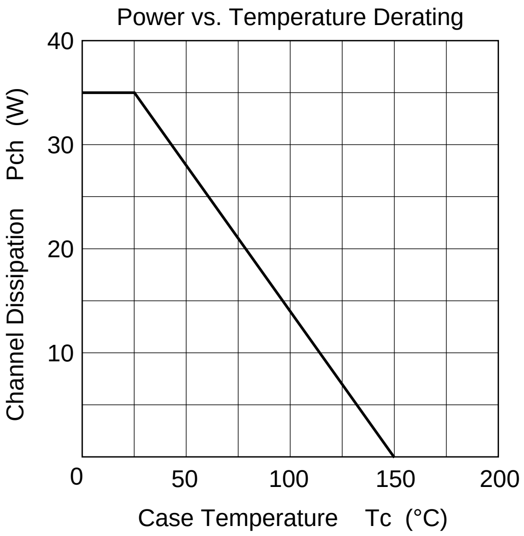
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

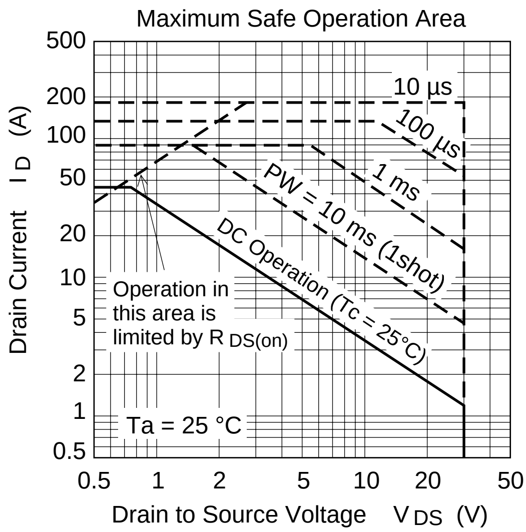
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.011	0.015	Ω	I_D = 25 A, V_{GS} = 10 V *
		—	0.016	0.022	Ω	I_D = 25 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	23	38	—	S	I_D = 25 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	3600	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	2000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	400	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 25 A
Rise time	t_r	—	230	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	435	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	360	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 45 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	75	—	ns	I_F = 45 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

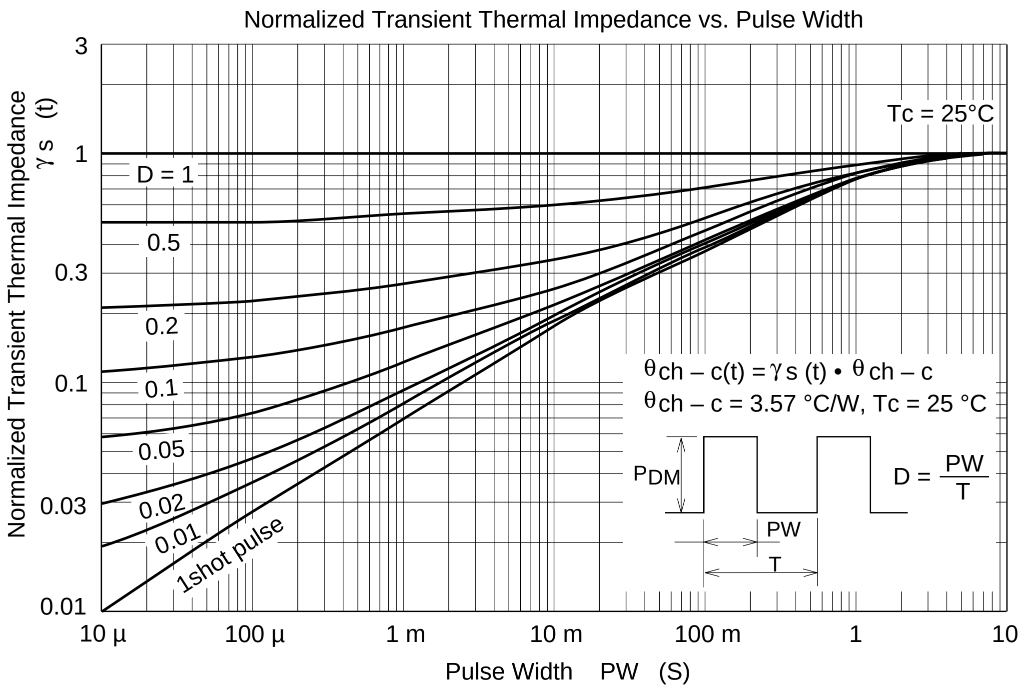
■ See characteristic curve of 2SK2204.



Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)



Maximum Safe Operation Area
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.5
1
2
5
10
20
50
Drain to Source Voltage V DS (V)



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ s (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γ s (t) • θ ch – c
θch – c = 3.57 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

2SK2212

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter,Motor Control

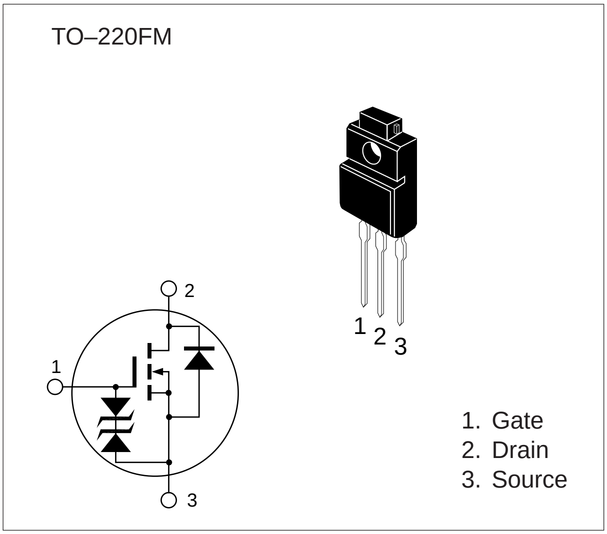


Table 1 Absolute Maximum Ratings (Ta = 25°C)

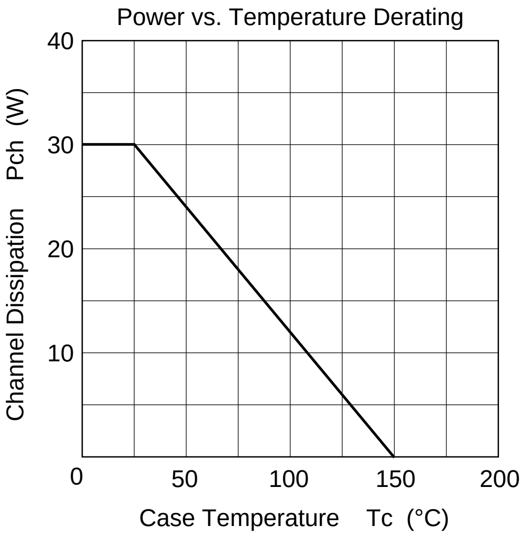
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}^*$	40	A
Body–drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

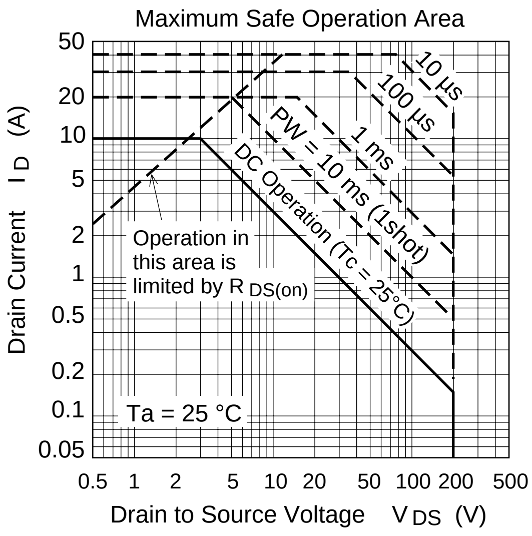
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

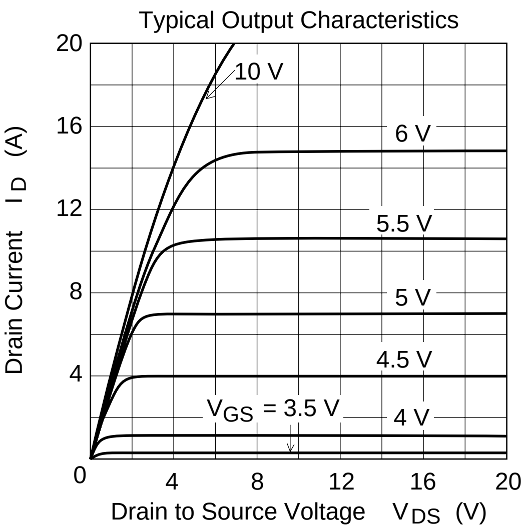
Table 2 Electrical Characteristics (Ta = 25°C)

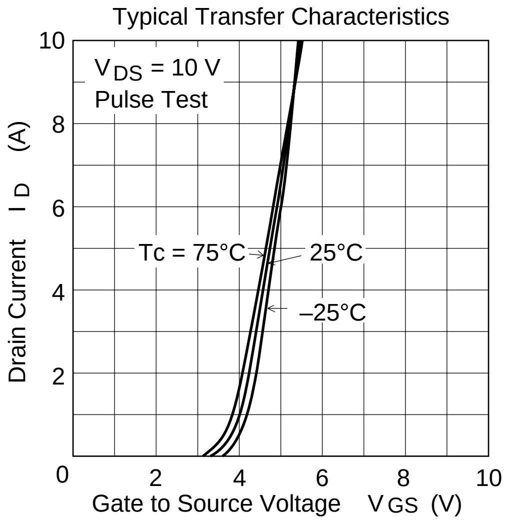
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.24	0.3	Ω	I_D = 5 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	6	—	S	I_D = 5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1000	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	360	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	65	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	18	—	ns	I_D = 5 A
Rise time	t_r	—	80	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 6Ω
Fall time	t_f	—	50	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	190	—	ns	I_F = 10 A, V_{GS} = 0, diF / dt = 100 A / µs

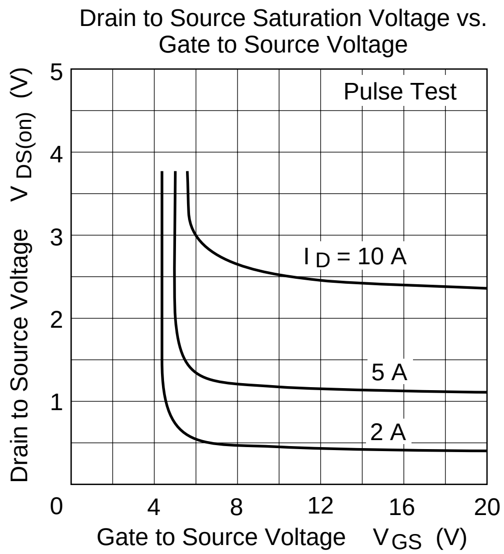
* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

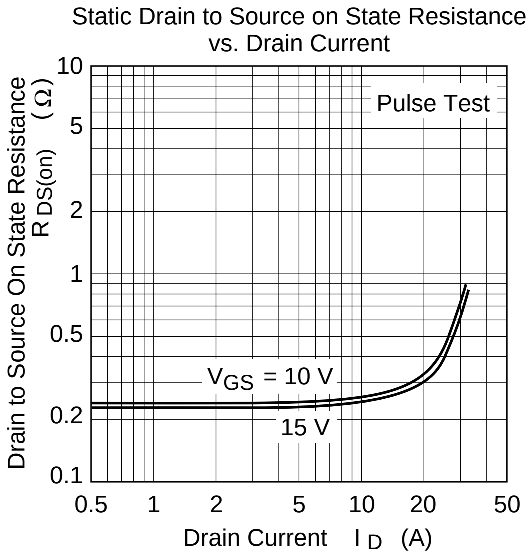

Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.5
1
2
5
10
20
50
100
200
500
Drain to Source Voltage V DS (V)


Typical Output Characteristics
Drain Current I D (A)
20
16
12
8
4
0
10 V
6 V
5.5 V
5 V
4.5 V
4 V
V GS = 3.5 V
4
8
12
16
20
Drain to Source Voltage V DS (V)

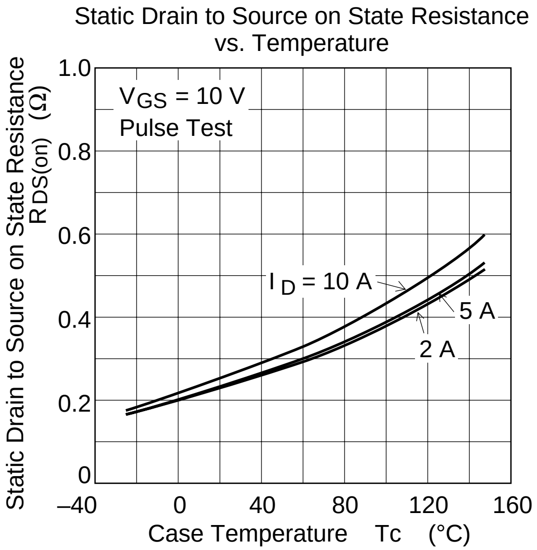

Typical Transfer Characteristics
Drain Current I D (A)
10
8
6
4
2
0
V DS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
2
4
6
8
10
Gate to Source Voltage V GS (V)



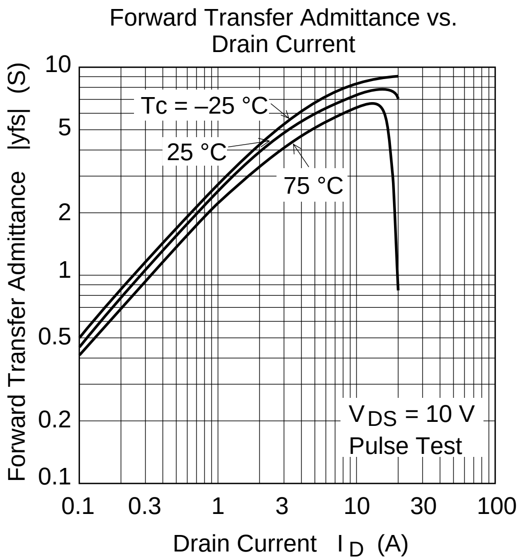
Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 10 A
5 A
2 A
Drain to Source Voltage V DS(on) (V)
0
1
2
3
4
5
4
8
12
16
20
Gate to Source Voltage V GS (V)



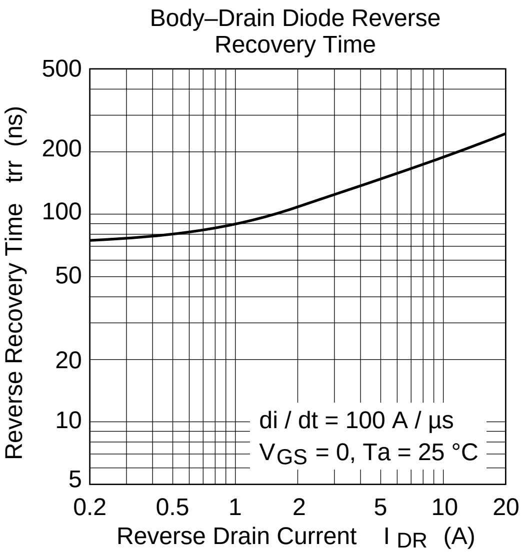
Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
VGS = 10 V
15 V
Drain to Source On State Resistance R DS(on) (Ω)
10
5
2
1
0.5
0.2
0.1
0.5
1
2
5
10
20
50
Drain Current I D (A)



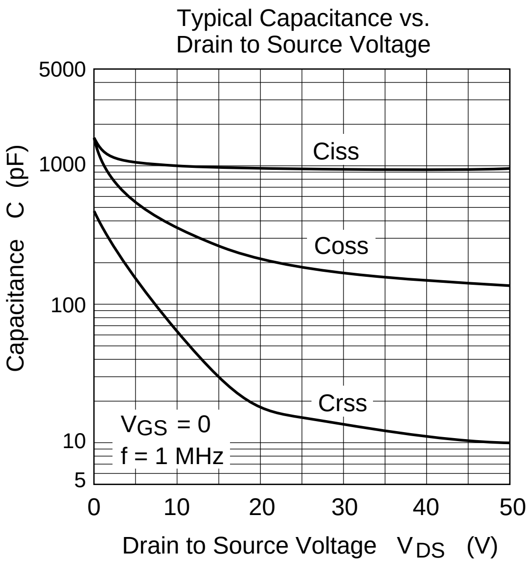
Static Drain to Source on State Resistance
vs. Temperature
VGS = 10 V
Pulse Test
I D = 10 A
5 A
2 A
Static Drain to Source on State Resistance RDS(on) (Ω)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160
Case Temperature Tc (°C)



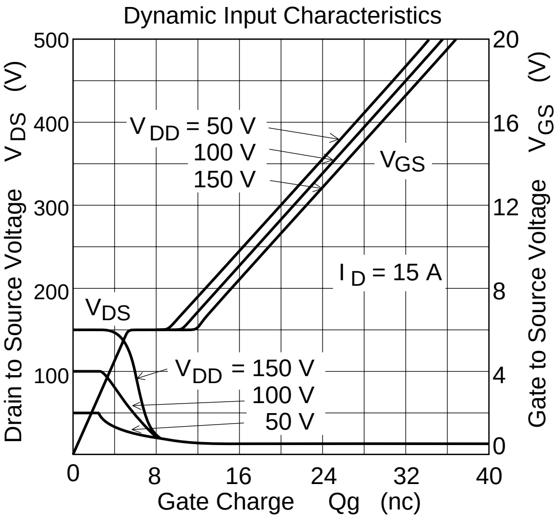
Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
VDS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
10
5
2
1
0.5
0.2
0.1
0.1
0.3
1
3
10
30
100
Drain Current I D (A)



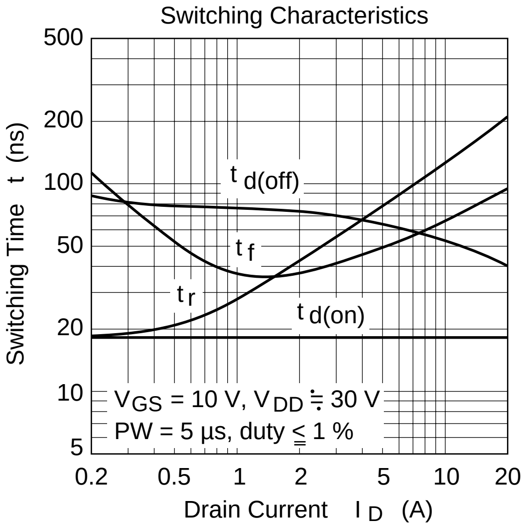
Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)
di / dt = 100 A / µs
VGS = 0, Ta = 25 °C



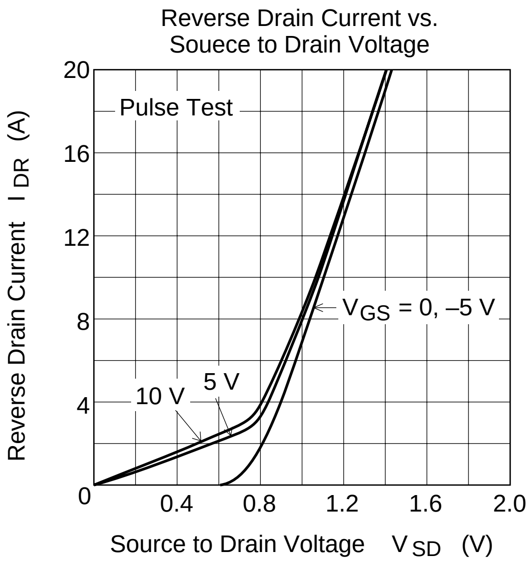
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
1000
100
10
5
0
10
20
30
40
50
Drain to Source Voltage V DS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

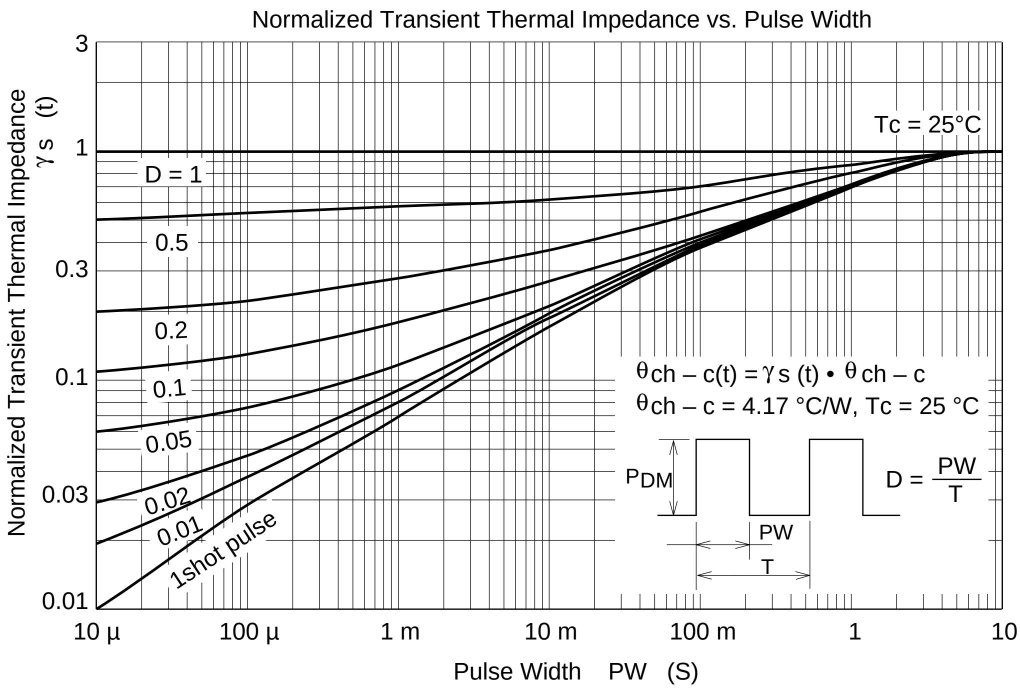


Dynamic Input Characteristics
Drain to Source Voltage V DS (V)
500
400
300
200
100
0
8
16
24
32
40
Gate Charge Qg (nc)
20
16
12
8
4
0
Gate to Source Voltage V GS (V)
V DD = 50 V
100 V
150 V
VGS
I D = 15 A
VDS
V DD = 150 V
100 V
50 V

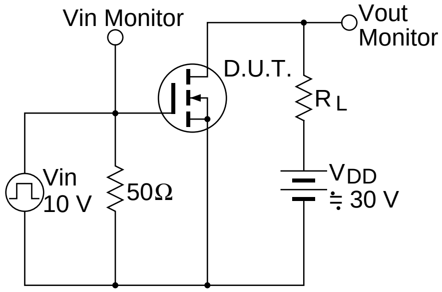


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20
Drain Current I D (A)
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %

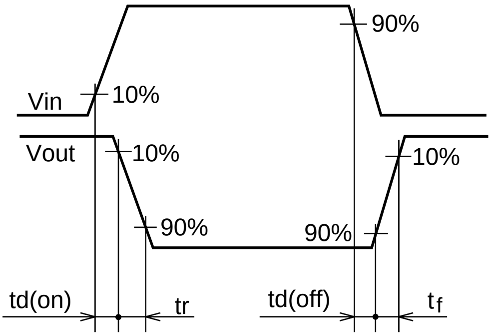

Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
Reverse Drain Current I DR (A)
Source to Drain Voltage V SD (V)
VGS = 0, –5 V
10 V
5 V
0
4
8
12
16
20
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 4.17 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Waveform



2SK2220, 2SK2221

Silicon N Channel MOS FET

Application

Low frequency power amplifier
Complementary pair with 2SJ351, 2SJ352

Features

- High power gain
- Excellent frequency response
- High speed switching
- Wide area of safe operation
- Enhancement–mode
- Good complementary characteristics
- Equipped with gate protection diodes

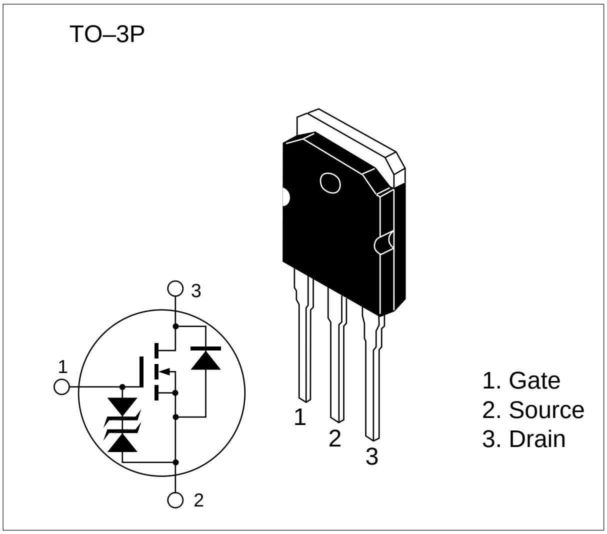


Table 1 Ordering Information

Type No.	V_{DSS}
2SK2220	180 V
2SK2221	200 V

Table 2 Absolute Maximum Ratings (Ta = 25°C)

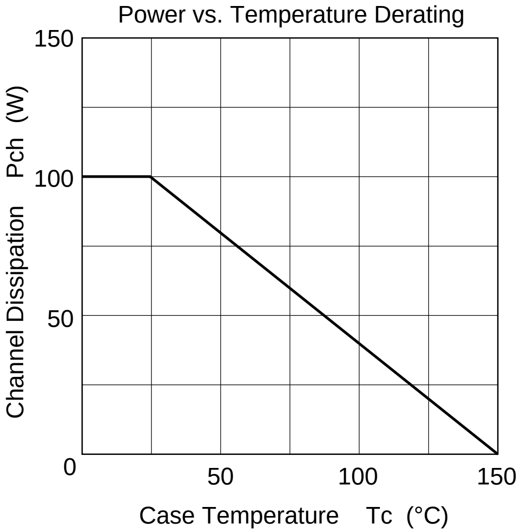
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK2220	V_{DSX}	180	V
	2SK2221		200	
Gate to source voltage		V_{GSS}	±20	V
Drain current		I_D	8	A
Body–drain diode reverse drain current		I_{DR}	8	A
Channel dissipation		Pch*	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

* Value at Tc = 25 °C

Table 3 Electrical Characteristics (Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK2220	$V_{(BR)DSX}$	180	—	—	V	I_D = 10 mA, V_{GS} = –10 V
	2SK2221		200	—	—		
Gate to source breakdown voltage		$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	0.15	—	1.45	V	I_D = 100 mA V_{DS} = 10 V
Drain to source saturation voltage		$V_{DS(sat)}$	—	—	12	V	I_D = 8 A, V_{GD} = 0 V*
Forward transfer admittance		$\|y_{fs}\|$	0.7	1.0	1.4	S	I_D = 3 A V_{DS} = 10 V *
Input capacitance		Ciss	—	600	—	pF	V_{GS} = –5 V
Output capacitance		Coss	—	800	—	pF	V_{DS} = 10 V
Reverse transfer capacitance		Crss	—	8	—	pF	f = 1 MHz
Turn–on time		t_{on}	—	250	—	ns	V_{DD} = 30 V
Turn–off time		t_{off}	—	90	—	ns	I_D = 4 A

* Pulse Test



Power vs. Temperature Derating
Channel Dissipation Pch (W)
150
100
50
0
50
100
150
Case Temperature Tc (°C)

2SK2225

Silicon N Channel MOS FET

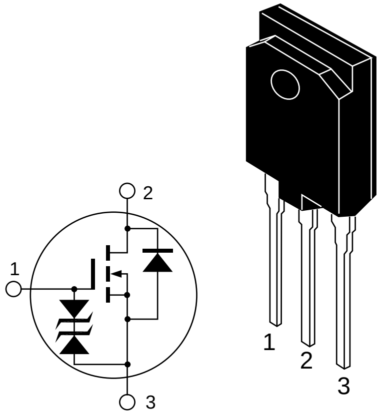
Application

High speed power switching

Features

- High breakdown voltage (V_{DSS} = 1500 V)
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–3PFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

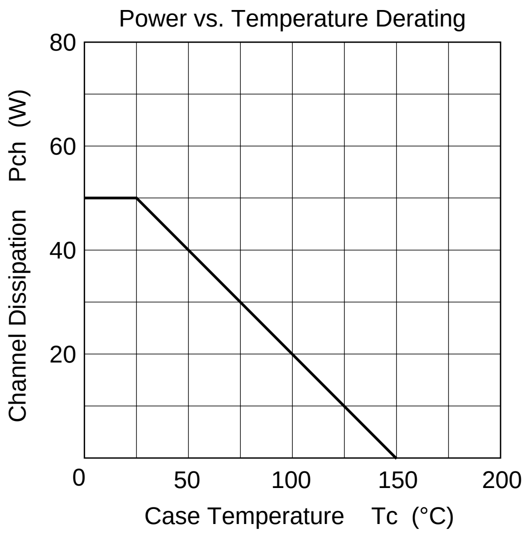
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1500	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}$*	7	A
Body–drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

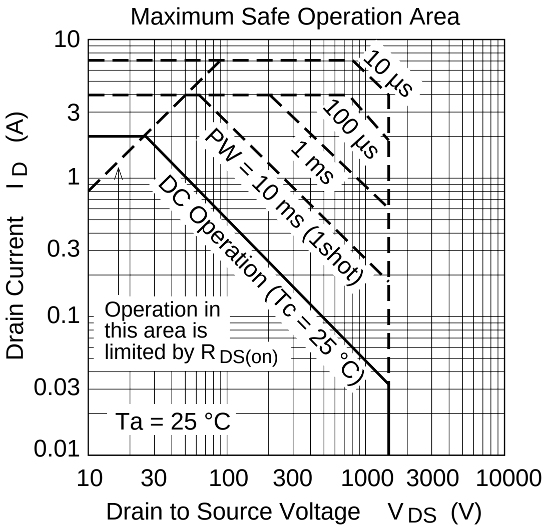
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

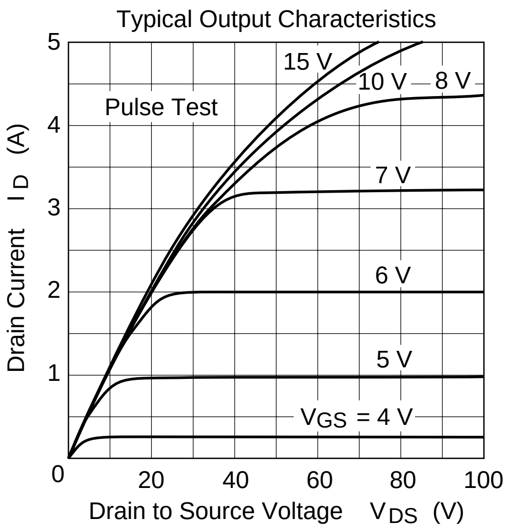
Table 2 Electrical Characteristics (Ta = 25°C)

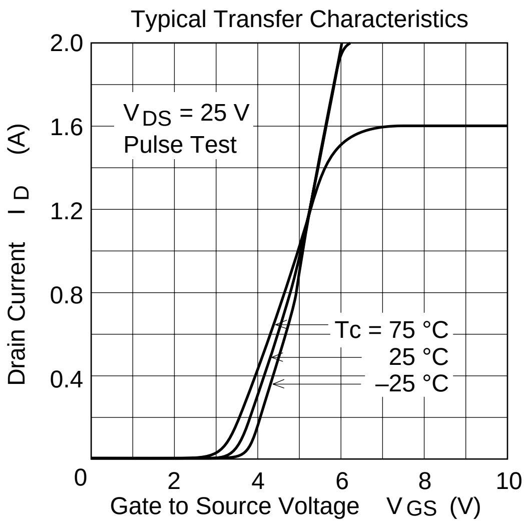
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	500	µA	V_{DS} =1200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	9	12	Ω	I_D = 1 A V_{GS} = 15 V *
Forward transfer admittance	$\|y_{fs}\|$	0.45	0.75	—	S	I_D = 1 A V_{DS} = 20 V *
Input capacitance	Ciss	—	990	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	125	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	60	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	17	—	ns	I_D = 1 A
Rise time	t_r	—	50	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	150	—	ns	R_L = 30 Ω
Fall time	t_f	—	50	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 2 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	1750	—	ns	I_F = 20 A, V_{GS} = 0, diF / dt = 100 A / µs

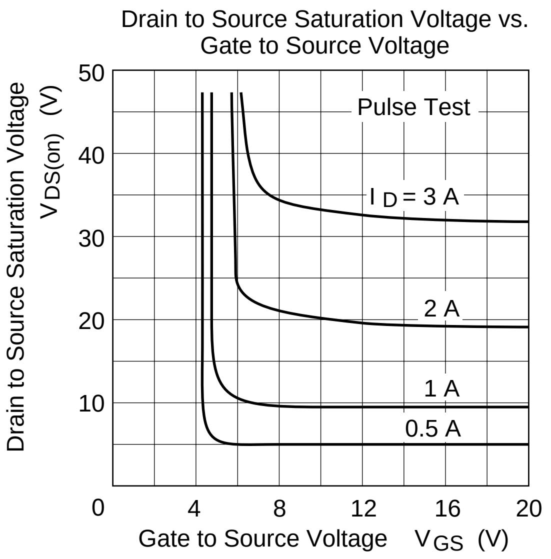
* Pulse Test

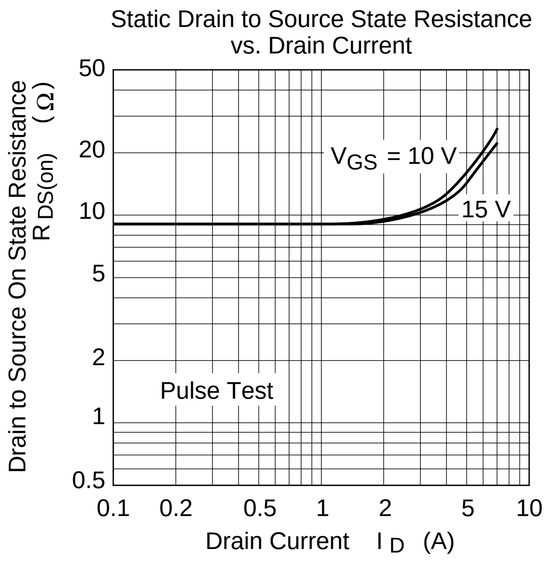

Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)

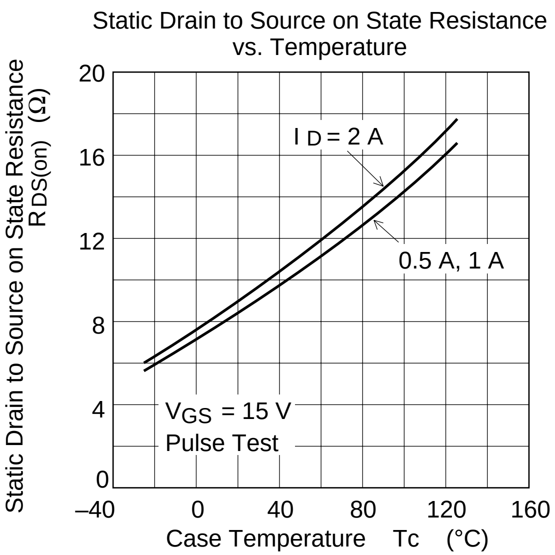

Maximum Safe Operation Area
Drain Current I D (A)
10
3
1
0.3
0.1
0.03
0.01
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
10
30
100
300
1000
3000
10000
Drain to Source Voltage V DS (V)

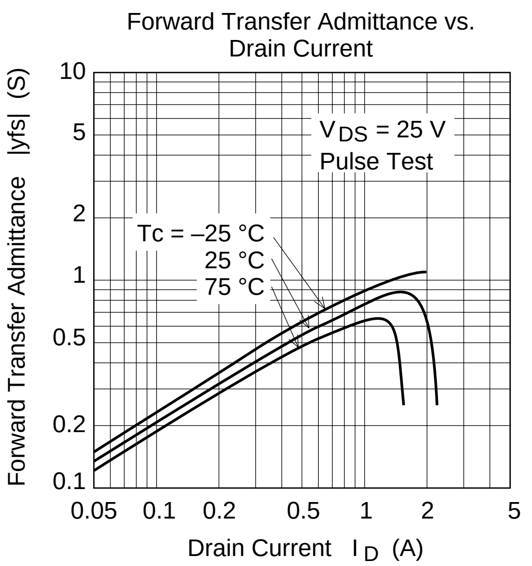

Typical Output Characteristics
Drain Current I D (A)
5
4
3
2
1
0
15 V
10 V
8 V
Pulse Test
7 V
6 V
5 V
VGS = 4 V
20
40
60
80
100
Drain to Source Voltage V DS (V)

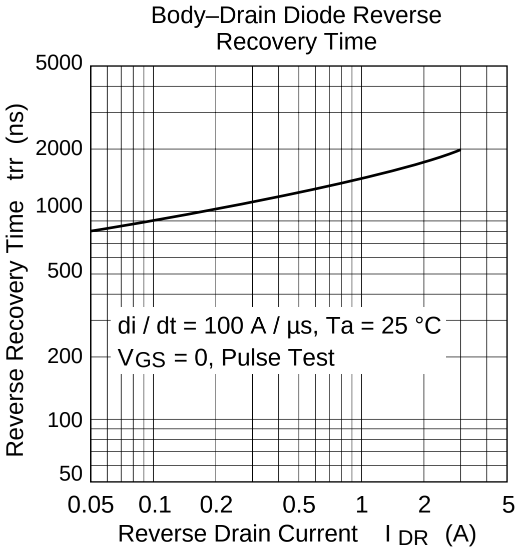

Typical Transfer Characteristics
Drain Current I D (A)
2.0
1.6
1.2
0.8
0.4
0
V DS = 25 V
Pulse Test
Tc = 75 °C
25 °C
–25 °C
2
4
6
8
10
Gate to Source Voltage V GS (V)

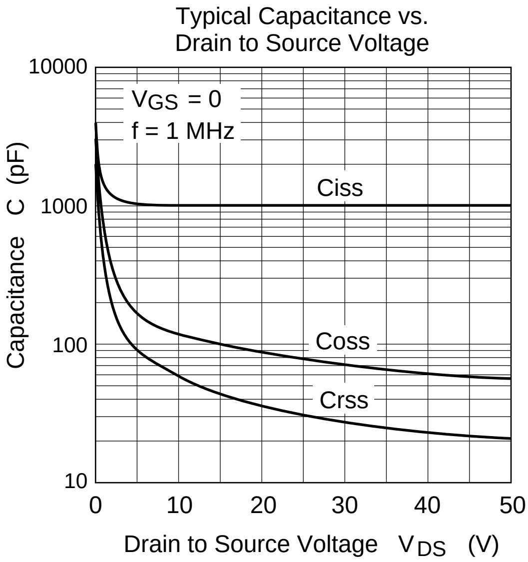

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 3 A
2 A
1 A
0.5 A
Drain to Source Saturation Voltage
VDS(on) (V)
50
40
30
20
10
0
4
8
12
16
20
Gate to Source Voltage VGS (V)

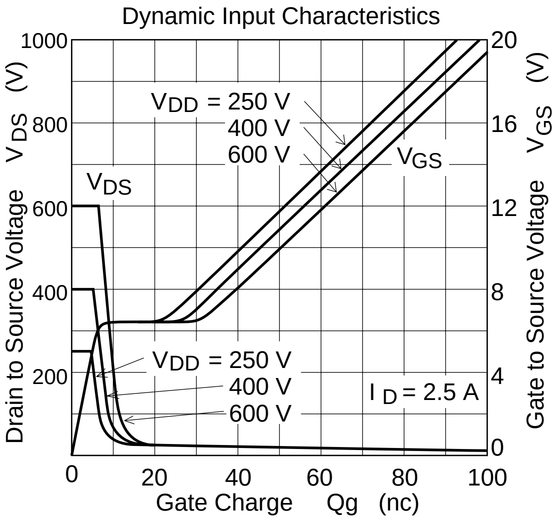

Static Drain to Source State Resistance
vs. Drain Current
VGS = 10 V
15 V
Pulse Test
Drain to Source On State Resistance
R DS(on) (Ω)
50
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

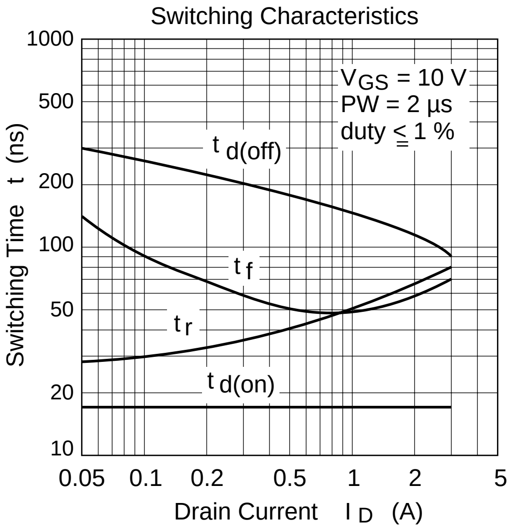

Static Drain to Source on State Resistance
vs. Temperature
I D = 2 A
0.5 A, 1 A
VGS = 15 V
Pulse Test
Static Drain to Source on State Resistance
R DS(on) (Ω)
20
16
12
8
4
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

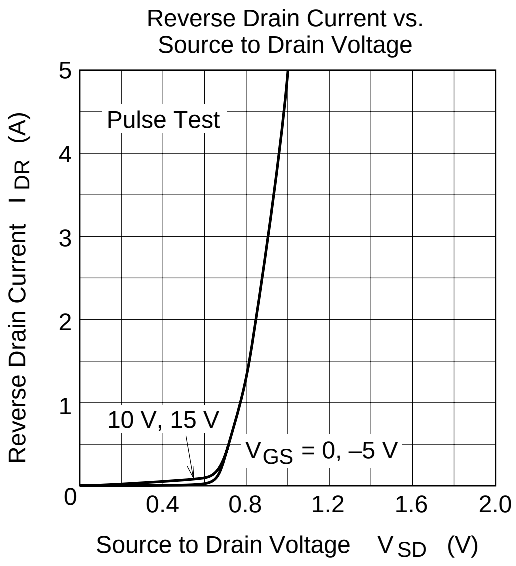

Forward Transfer Admittance vs.
Drain Current
VDS = 25 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
Forward Transfer Admittance |yfs| (S)
10
5
2
1
0.5
0.2
0.1
0.05
0.1
0.2
0.5
1
2
5
Drain Current I D (A)

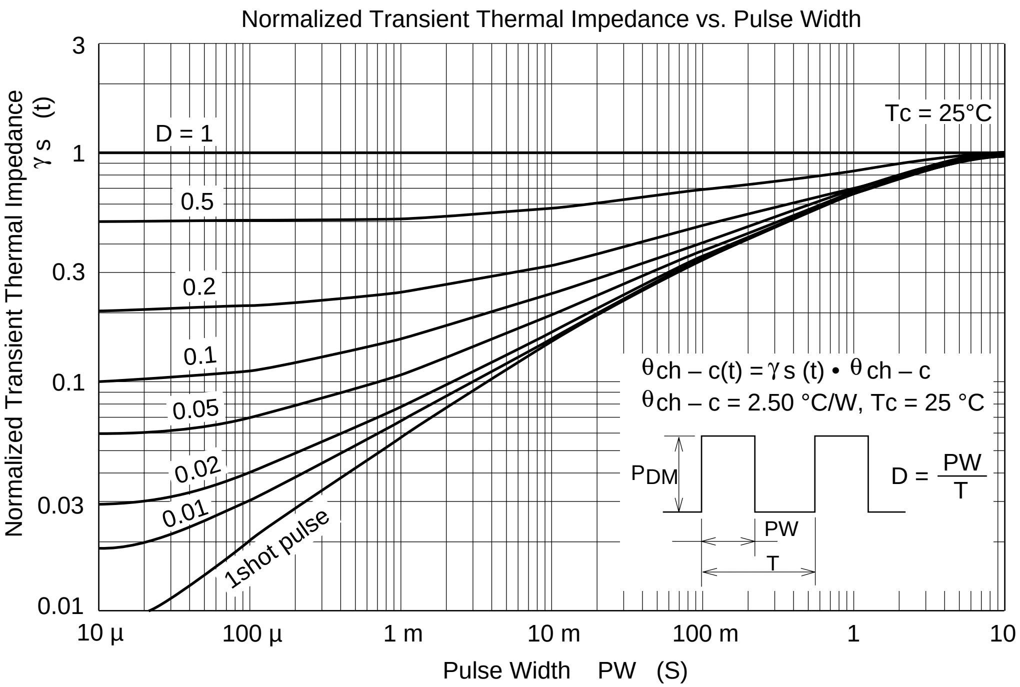

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
5000
2000
1000
500
200
100
50
di / dt = 100 A / µs, Ta = 25 °C
VGS = 0, Pulse Test
0.05
0.1
0.2
0.5
1
2
5
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
10
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

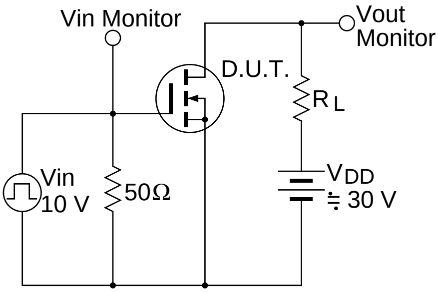

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
1000
800
600
400
200
VDD = 250 V
400 V
600 V
VGS
VDS
VDD = 250 V
400 V
600 V
I D = 2.5 A
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
VGS = 10 V
PW = 2 µs
duty ≦ 1 %
t d(off)
t f
t r
t d(on)
0.05
0.1
0.2
0.5
1
2
5
Drain Current I D (A)

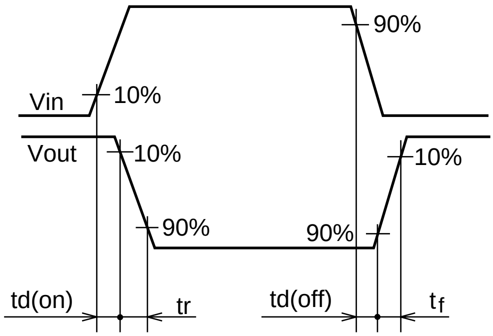

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V, 15 V
VGS = 0, –5 V
0
0.4
0.8
1.2
1.6
2.0
1
2
3
4
5
Source to Drain Voltage VSD (V)
Reverse Drain Current IDR (A)


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 2.50 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)
Normalized Transient Thermal Impedance γs (t)

Switching Time Test Circuit



Waveform



2SK2247

Silicon N Channel MOS FET

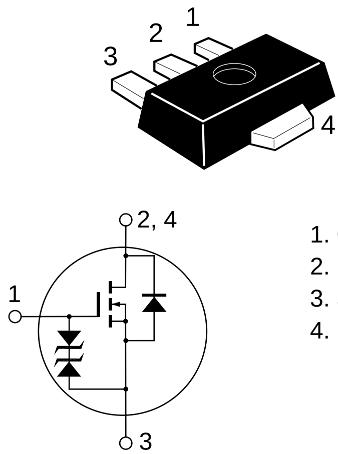
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source.
- Suitable for DC – DC converter, motor drive, power switch, solenoid drive

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

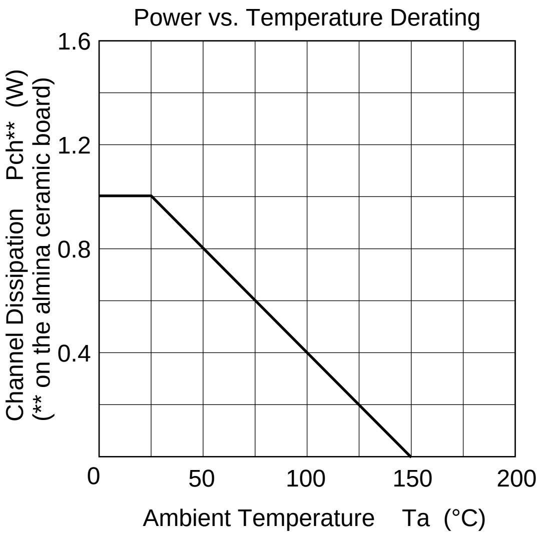
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}{}^*$	4	A
Body–drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

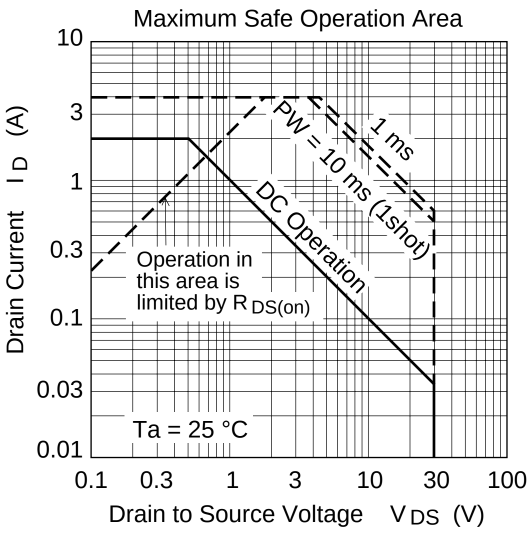
* PW ≤ 100 µs, duty cycle ≤ 10 %
** When using the alumina ceramic board (12.5 × 20 × 0.7mm)
*** Marking is “QY”

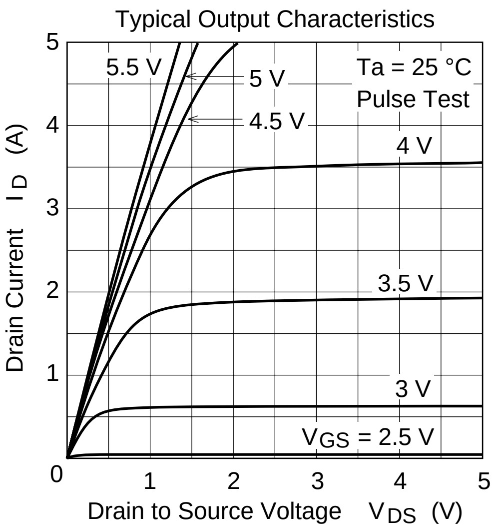
Table 2 Electrical Characteristics (Ta = 25°C)

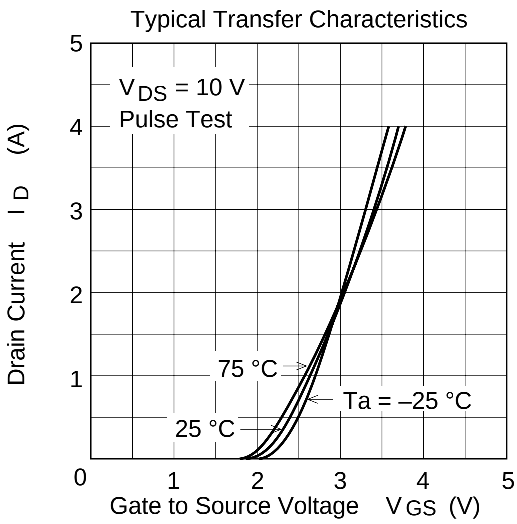
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 1 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±10 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 24 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	1.5	2.0	V	I_D = 100 µA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.45	Ω	I_D = 1 A, V_{GS} = 4 V *
		—	0.22	0.35	Ω	I_D = 1 A, V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.5	1.9	—	S	I_D = 1 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	177	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	116	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	43	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = 1 A
Rise time	t_r	—	14	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	37	—	ns	R_L = 30 Ω
Fall time	t_f	—	33	—	ns	PW = 2 µs

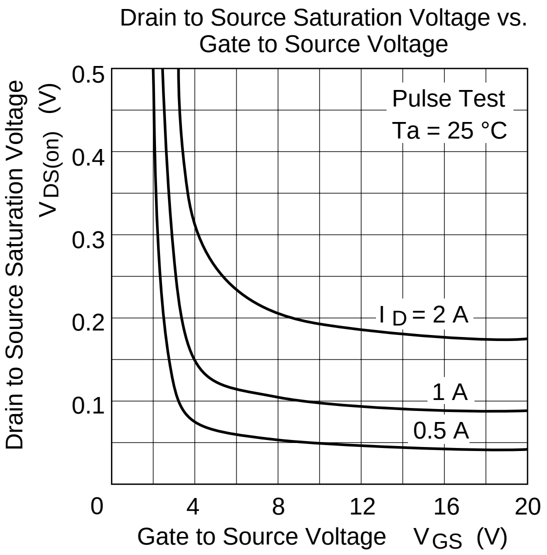
* Pulse Test

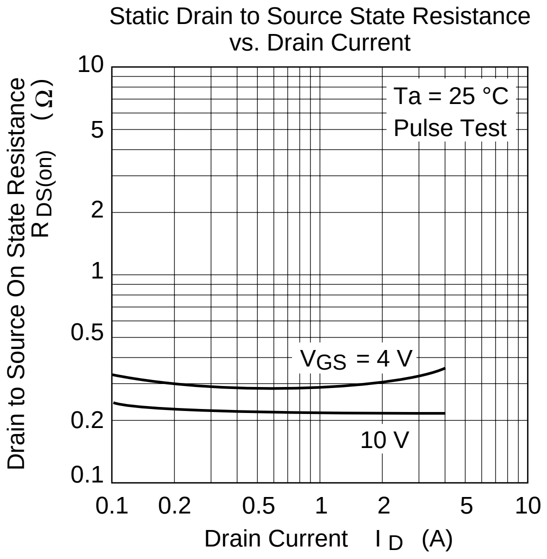

Power vs. Temperature Derating
Channel Dissipation Pch** (W)
(** on the alumina ceramic board)
1.6
1.2
0.8
0.4
0
50
100
150
200
Ambient Temperature Ta (°C)

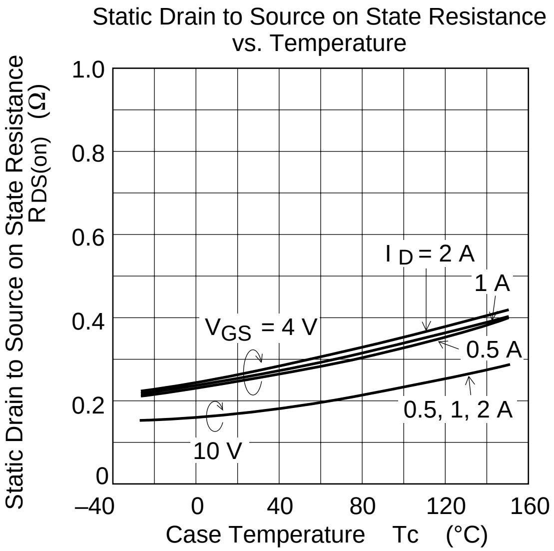

Maximum Safe Operation Area
Drain Current I D (A)
10
3
1
0.3
0.1
0.03
0.01
PW = 10 ms (1shot)
1 ms
DC Operation
Operation in this area is limited by R DS(on)
Ta = 25 °C
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

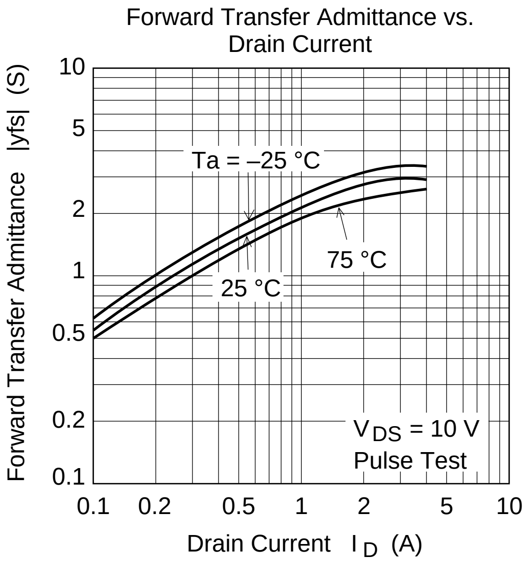

Typical Output Characteristics
Drain Current I D (A)
5
4
3
2
1
0
5.5 V
5 V
4.5 V
Ta = 25 °C
Pulse Test
4 V
3.5 V
3 V
VGS = 2.5 V
1
2
3
4
5
Drain to Source Voltage V DS (V)

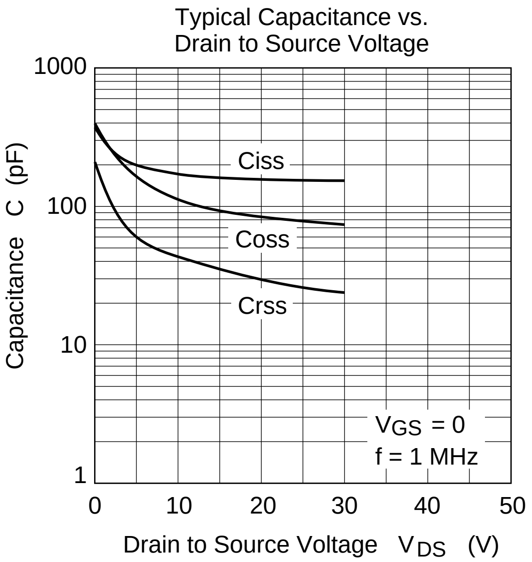

Typical Transfer Characteristics
Drain Current I D (A)
5
4
3
2
1
0
V DS = 10 V
Pulse Test
75 °C
Ta = –25 °C
25 °C
1
2
3
4
5
Gate to Source Voltage V GS (V)

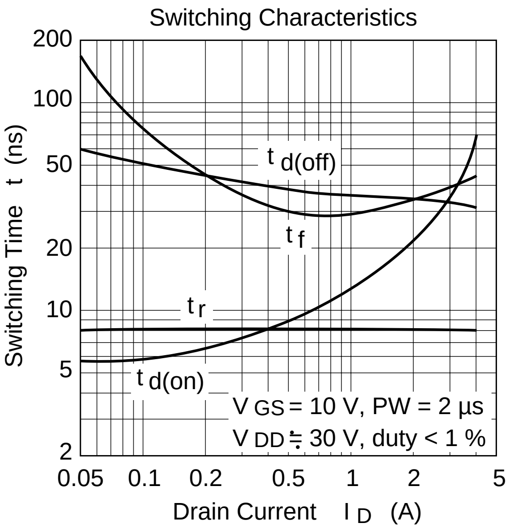

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
Ta = 25 °C
I D = 2 A
1 A
0.5 A
Drain to Source Saturation Voltage
VDS(on) (V)
Gate to Source Voltage VGS (V)
0.5
0.4
0.3
0.2
0.1
0
4
8
12
16
20

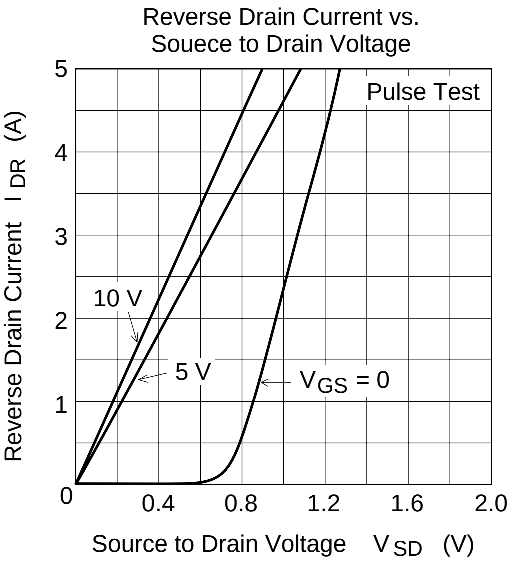

Static Drain to Source State Resistance
vs. Drain Current
Ta = 25 °C
Pulse Test
VGS = 4 V
10 V
Drain to Source On State Resistance
RDS(on) (Ω)
Drain Current I D (A)
10
5
2
1
0.5
0.2
0.1
0.1
0.2
0.5
1
2
5
10


Static Drain to Source on State Resistance
vs. Temperature
I D = 2 A
1 A
0.5 A
VGS = 4 V
10 V
0.5, 1, 2 A
Static Drain to Source on State Resistance
RDS(on) (Ω)
Case Temperature Tc (°C)
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160


Forward Transfer Admittance vs.
Drain Current
Ta = –25 °C
25 °C
75 °C
VDS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
10
5
2
1
0.5
0.2
0.1
0.1
0.2
0.5
1
2
5
10


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
1000
100
10
1
Ciss
Coss
Crss
V_{GS} = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)


Switching Characteristics
Switching Time t (ns)
200
100
50
20
10
5
2
$t_{d(off)}$
t_f
t_r
$t_{d(on)}$
V_{GS} = 10 V, PW = 2 µs
V_{DD} ≒ 30 V, duty < 1 %
0.05
0.1
0.2
0.5
1
2
5
Drain Current I_D (A)


Reverse Drain Current vs.
Souece to Drain Voltage
Reverse Drain Current I_{DR} (A)
5
4
3
2
1
0
Pulse Test
10 V
5 V
V_{GS} = 0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)

2SK2278(L), 2SK2278(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- High breakdown voltage (V_{DSS} = 1500 V)
- High speed switching
- No secondary breakdown
- Suitable for Switching regulator, DC – DC converter

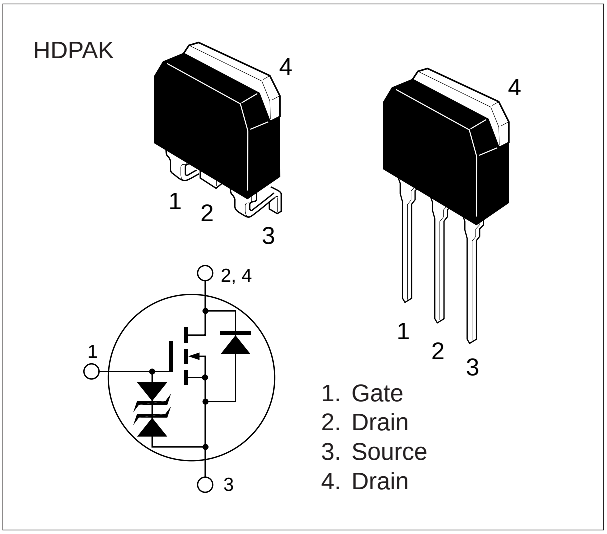


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1500	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	2.5	A
Drain peak current	$I_{D(pulse)}$*	7	A
Body–drain diode reverse drain current	I_{DR}	2.5	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

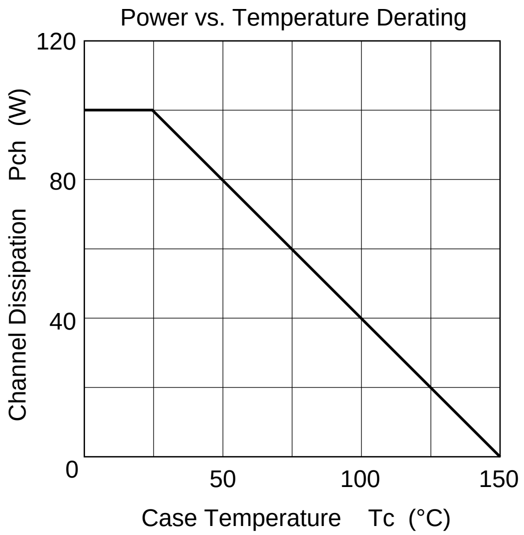
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±1	μA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	500	μA	V_{DS} = 1200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	9	12	Ω	I_D = 2 A V_{GS} = 15 V *
Forward transfer admittance	$\|y_{fs}\|$	0.45	0.75	—	S	I_D = 1 A V_{DS} = 20 V *
Input capacitance	Ciss	—	990	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	125	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	60	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	17	—	ns	I_D = 2 A
Rise time	t_r	—	70	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	110	—	ns	R_L = 15 Ω
Fall time	t_f	—	60	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 2 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	1750	—	μs	I_F = 2 A, V_{GS} = 0, diF / dt = 100 A / μs

* Pulse Test

See characteristic curves of 2SK1317.


Power vs. Temperature Derating
120
80
40
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature Tc (°C)

2SK2315

Silicon N Channel MOS FET

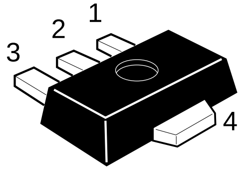
Application

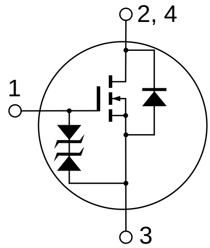
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device - - - can be driven from 3 V source.
- Suitable for DC – DC converter, motor drive, power switch, solenoid drive

UPAK





1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

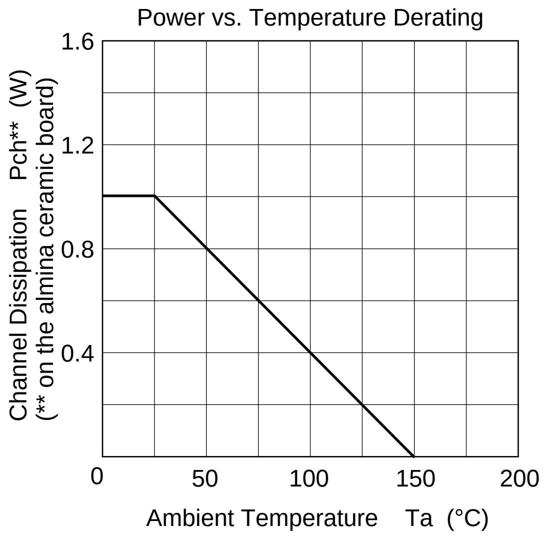
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}^*$	±4	A
Body–drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

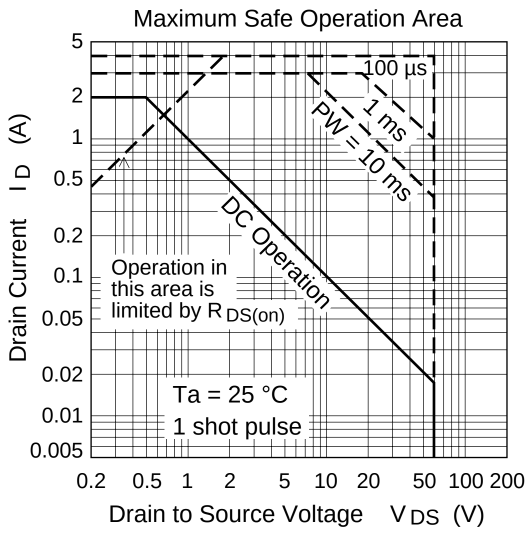
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the alumina ceramic board (12.5 × 20 × 0.7mm)
*** Marking is “TY”

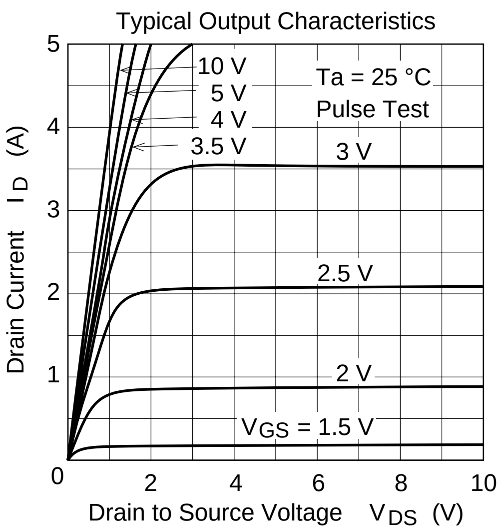
Table 2 Electrical Characteristics (Ta = 25°C)

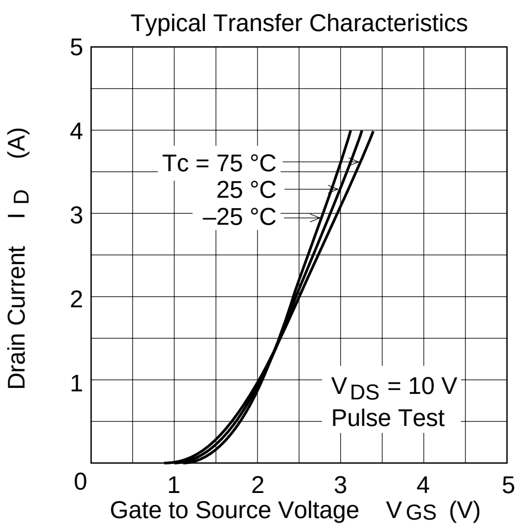
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	5	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.4	0.6	Ω	I_D = 0.3 A V_{GS} = 3 V *
		—	0.35	0.45	Ω	I_D = 1 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	1.5	1.8	—	S	I_D = 1 A V_{DS} = 10 V *
Input capacitance	Ciss	—	173	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	85	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	23	—	pF	f = 1 MHz
Turn–on time	t_{on}	—	21	—	ns	I_D = 1 A, R_L = 30 Ω
Turn–off time	t_{off}	—	85	—	ns	V_{GS} = 10 V

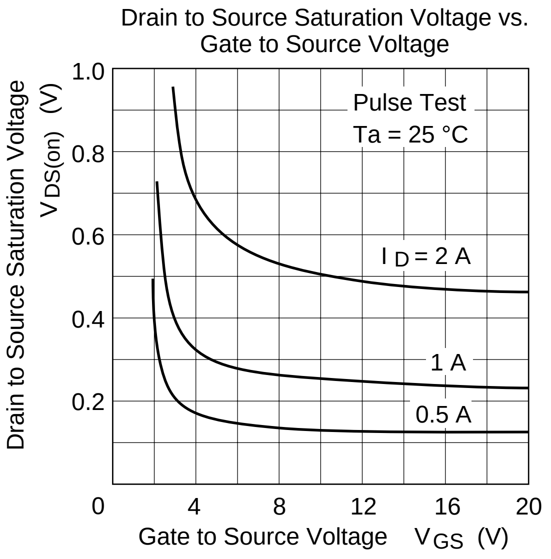
* Pulse Test

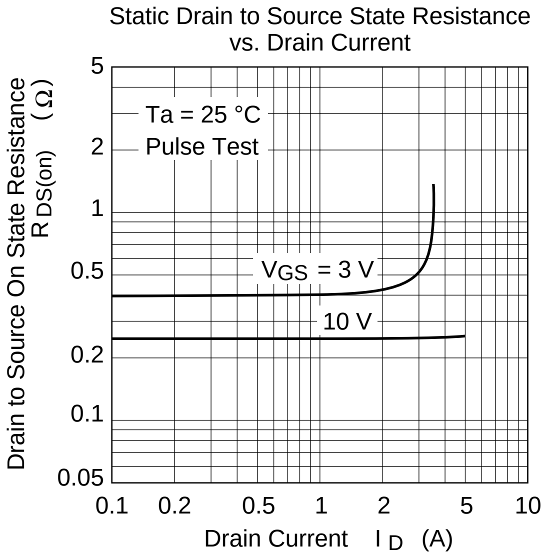

Power vs. Temperature Derating
1.6
1.2
0.8
0.4
0
50
100
150
200
Channel Dissipation Pch** (W)
(** on the alumina ceramic board)
Ambient Temperature Ta (°C)

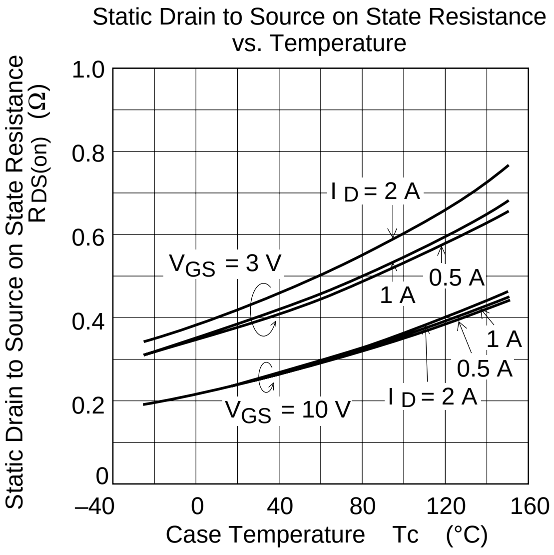

Maximum Safe Operation Area
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.005
100 μs
1 ms
PW = 10 ms
DC Operation
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1 shot pulse
0.2
0.5
1
2
5
10
20
50
100
200
Drain Current I D (A)
Drain to Source Voltage V DS (V)

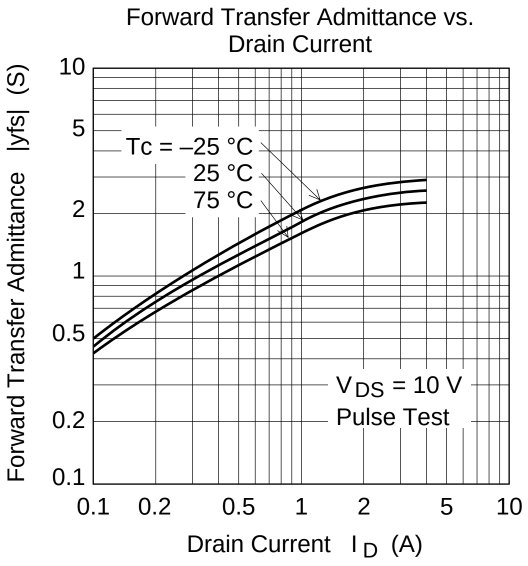

Typical Output Characteristics
5
4
3
2
1
0
10 V
5 V
4 V
3.5 V
Ta = 25 °C
Pulse Test
3 V
2.5 V
2 V
VGS = 1.5 V
2
4
6
8
10
Drain Current I D (A)
Drain to Source Voltage V DS (V)

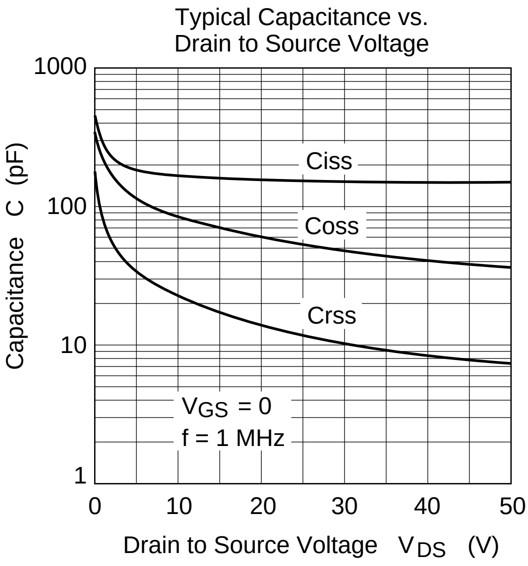

Typical Transfer Characteristics
5
4
3
2
1
0
Tc = 75 °C
25 °C
–25 °C
V DS = 10 V
Pulse Test
1
2
3
4
5
Drain Current I D (A)
Gate to Source Voltage V GS (V)

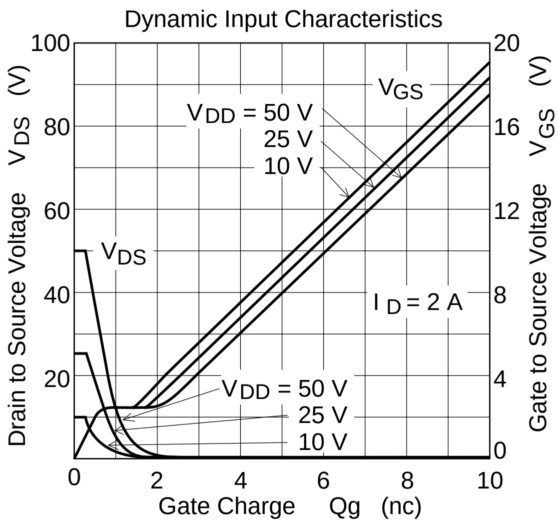

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage
V DS(on) (V)
Pulse Test
Ta = 25 °C
I D = 2 A
1 A
0.5 A
1.0
0.8
0.6
0.4
0.2
0
4
8
12
16
20
Gate to Source Voltage V GS (V)

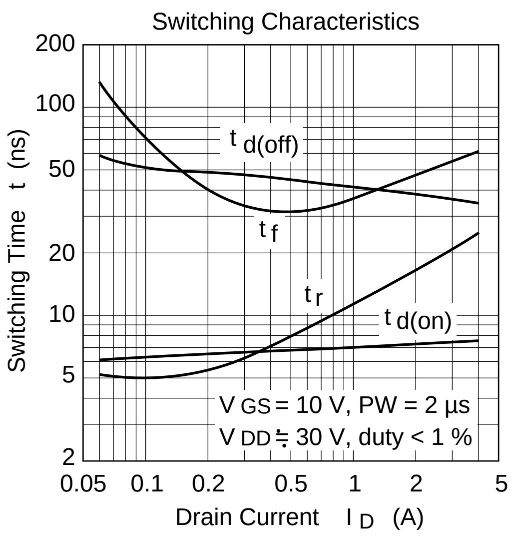

Static Drain to Source State Resistance
vs. Drain Current
Drain to Source On State Resistance
R DS(on) (Ω)
Ta = 25 °C
Pulse Test
V GS = 3 V
10 V
5
2
1
0.5
0.2
0.1
0.05
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)

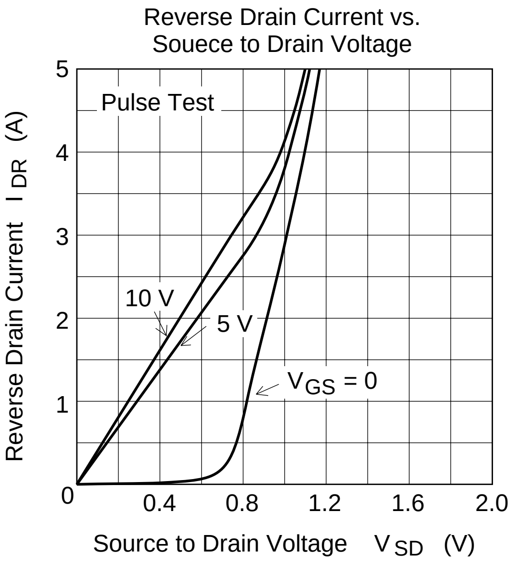

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance
R DS(on) (Ω)
I D = 2 A
V GS = 3 V
0.5 A
1 A
1 A
0.5 A
I D = 2 A
V GS = 10 V
1.0
0.8
0.6
0.4
0.2
0
–40
0
40
80
120
160
Case Temperature Tc (°C)


Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
Tc = –25 °C
25 °C
75 °C
V DS = 10 V
Pulse Test
10
5
2
1
0.5
0.2
0.1
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage V DS (V)
1000
100
10
1
0
10
20
30
40
50
Ciss
Coss
Crss
VGS = 0
f = 1 MHz


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
100
80
60
40
20
0
2
4
6
8
10
16
12
8
4
VGS
VDD = 50 V
25 V
10 V
VDS
I D = 2 A
VDD = 50 V
25 V
10 V


Switching Characteristics
Switching Time t (ns)
Drain Current I D (A)
200
100
50
20
10
5
2
0.05
0.1
0.2
0.5
1
2
5
t d(off)
t f
t r
t d(on)
V GS = 10 V, PW = 2 µs
V DD ≒ 30 V, duty < 1 %


Reverse Drain Current vs.
Souece to Drain Voltage
Reverse Drain Current I DR (A)
Source to Drain Voltage V SD (V)
5
4
3
2
1
0
0.4
0.8
1.2
1.6
2.0
Pulse Test
10 V
5 V
VGS = 0

2SK2322(L), 2SK2322(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device can be driven from 3 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

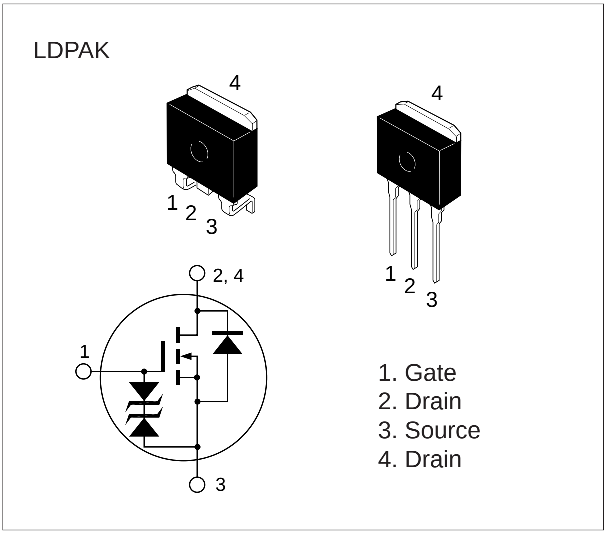


Table 1 Absolute Maximum Ratings (Ta = 25°C)

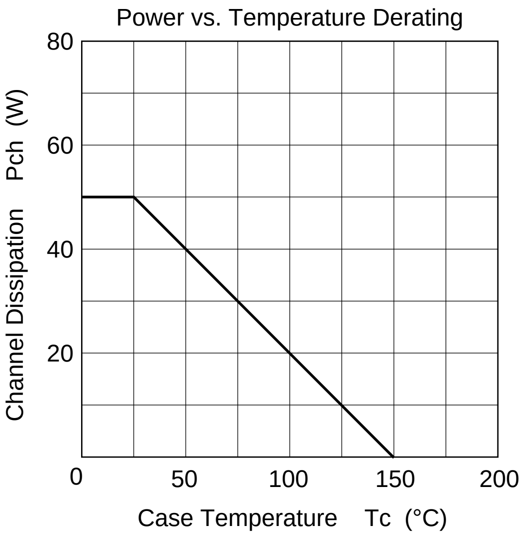
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body–drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP}***	15	A
Avalanche energy	E_{AR}***	19	mJ
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

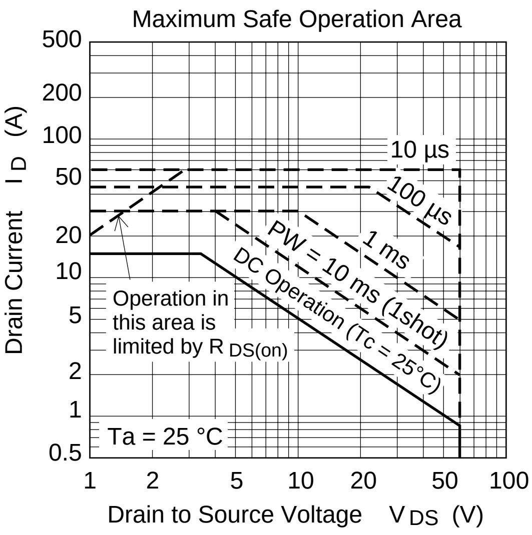
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.04	0.05	Ω	I_D = 8 A V_{GS} = 10 V *
		—	0.08	0.15	Ω	I_D = 3 A V_{GS} = 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	8	14	—	S	I_D = 8 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1600	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	680	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	120	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 8 A
Rise time	t_r	—	190	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	130	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	120	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	85	—	ns	I_F = 15 A, V_{GS} = 0, diF / dt = 50 A / µs

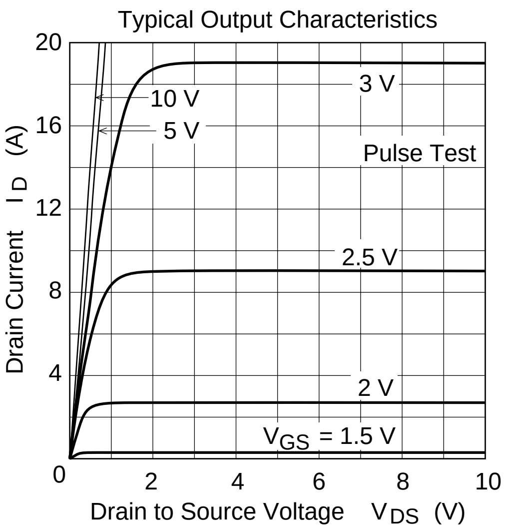
* Pulse Test



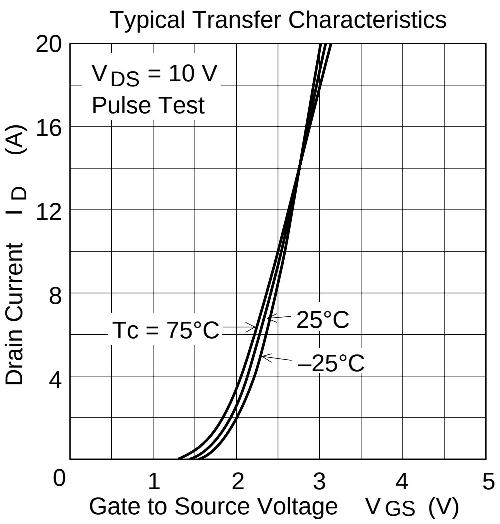
Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)



Maximum Safe Operation Area
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1
2
5
10
20
50
100
Drain to Source Voltage V DS (V)

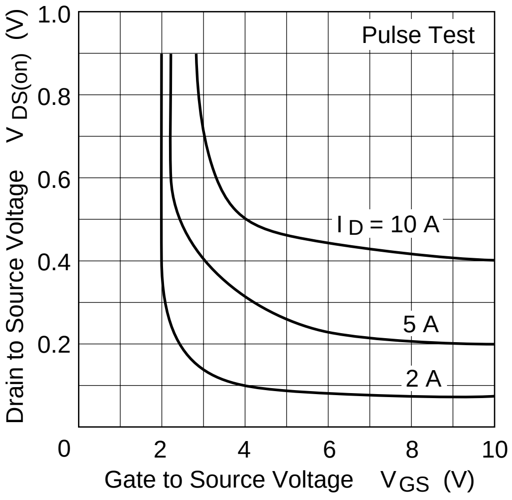


Typical Output Characteristics
Drain Current I D (A)
20
16
12
8
4
0
10 V
5 V
3 V
Pulse Test
2.5 V
2 V
VGS = 1.5 V
2
4
6
8
10
Drain to Source Voltage VDS (V)

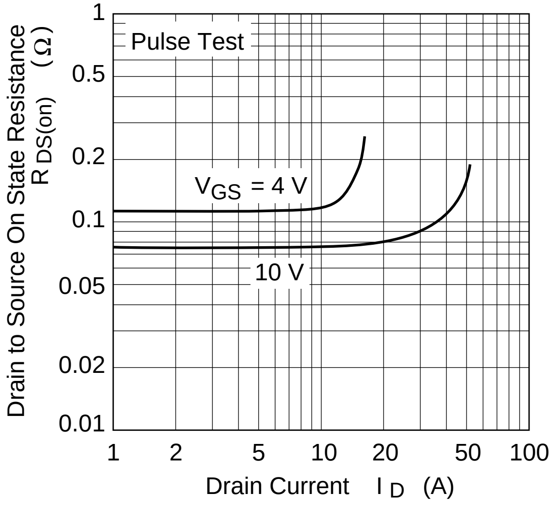


Typical Transfer Characteristics
Drain Current I D (A)
20
16
12
8
4
0
VDS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
1
2
3
4
5
Gate to Source Voltage V GS (V)

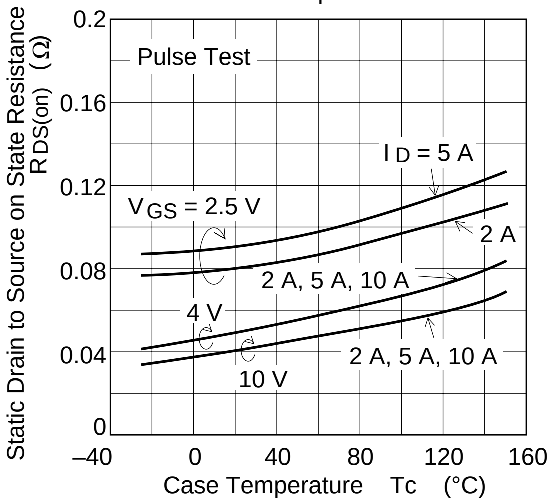
Drain to Source Saturation Voltage vs. Gate to Source Voltage



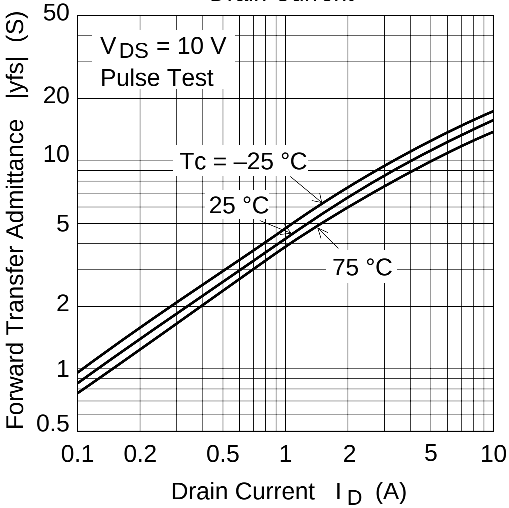
Static Drain to Source on State Resistance vs. Drain Current

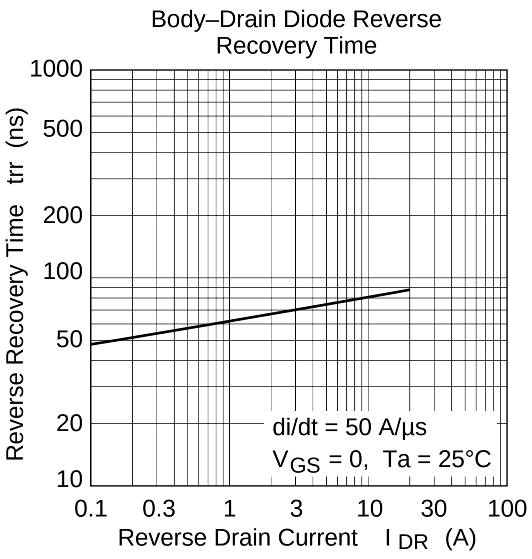


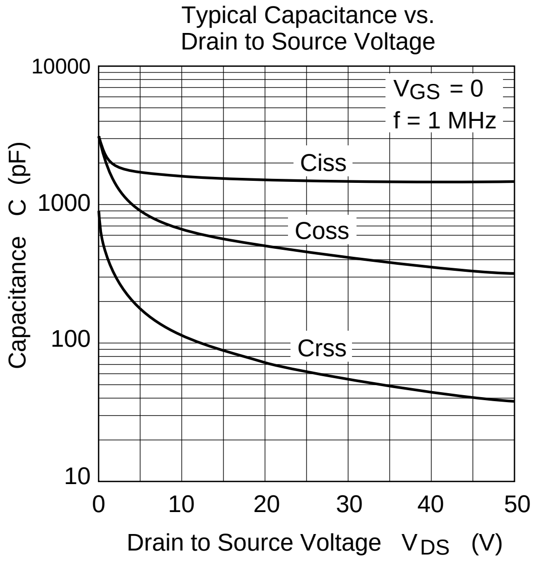
Static Drain to Source on State Resistance vs. Temperature

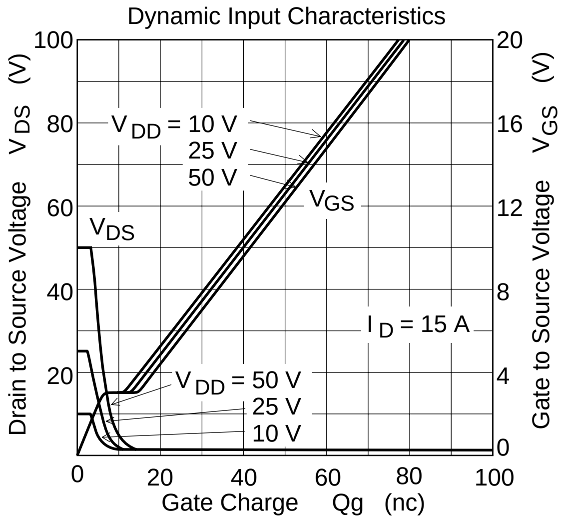


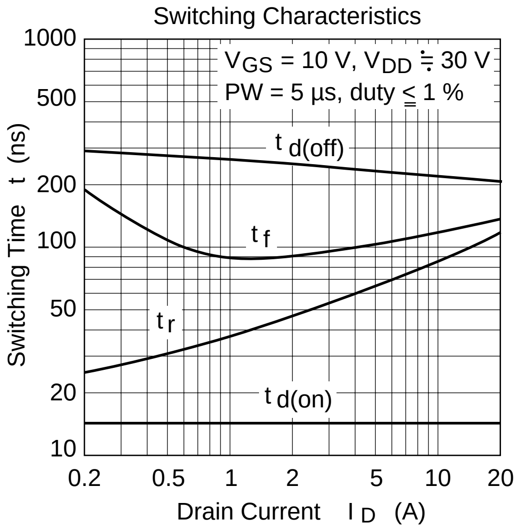
Forward Transfer Admittance vs. Drain Current

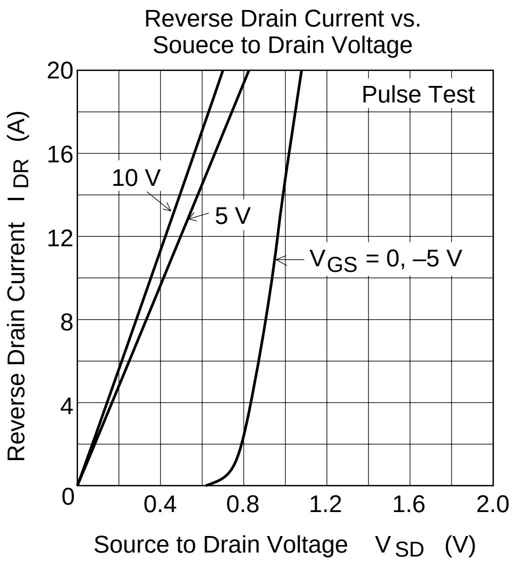


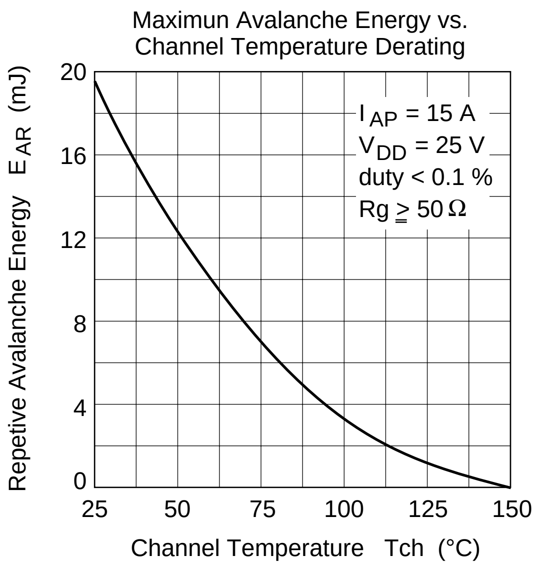

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di/dt = 50 A/μs
VGS = 0, Ta = 25°C
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
1000
100
10
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

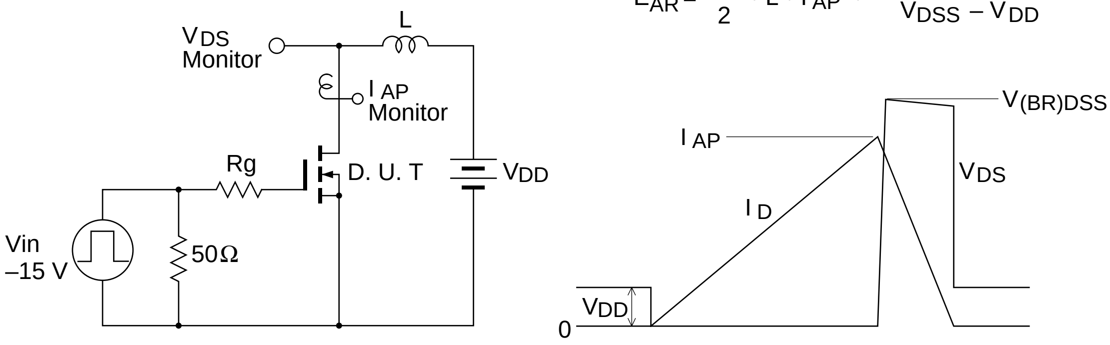

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
100
80
60
40
20
0
VDD = 10 V
25 V
50 V
VGS
VDS
ID = 15 A
VDD = 50 V
25 V
10 V
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
VGS = 10 V, VDD ≒ 30 V
PW = 5 μs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
0.2
0.5
1
2
5
10
20
Drain Current I D (A)

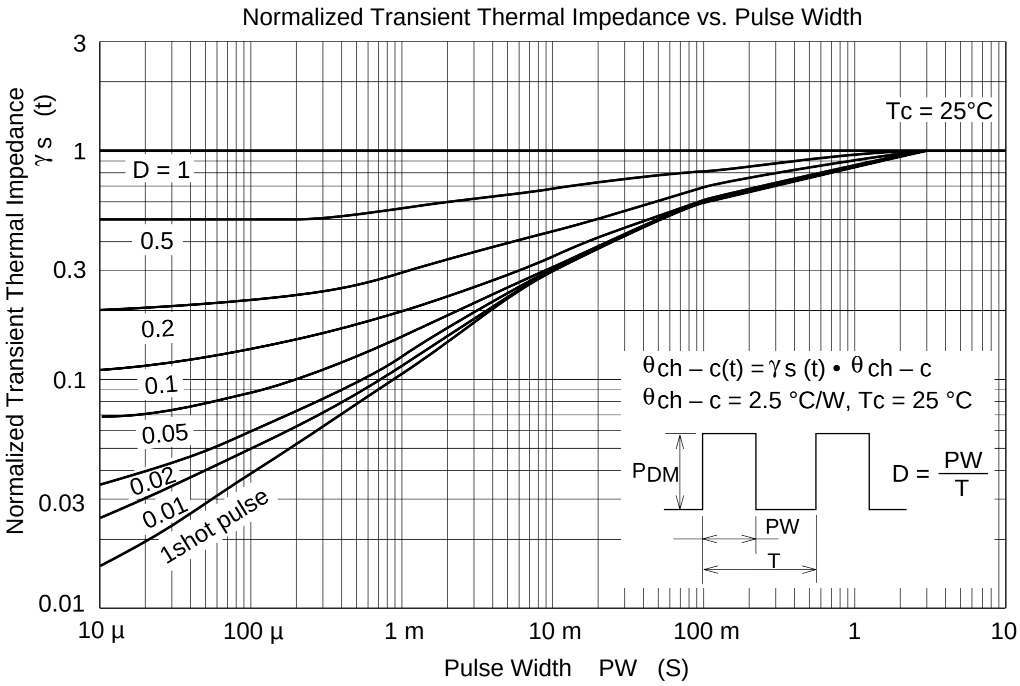


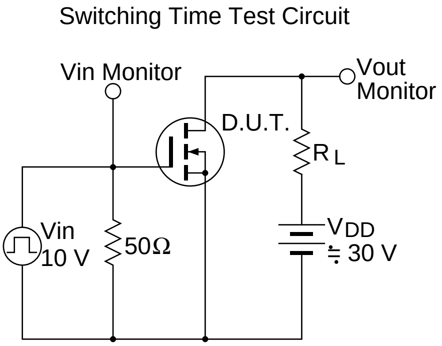


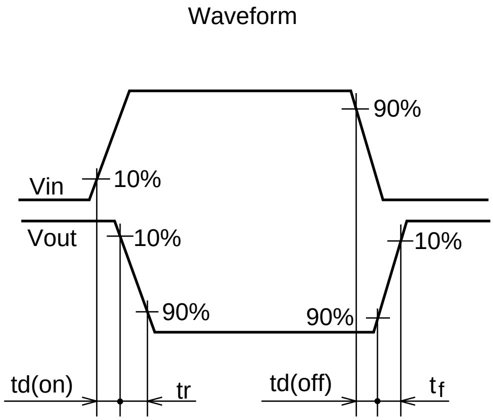
Avalanche Test Circuit and Waveform



$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 2.5 °C/W, Tc = 25 °C
PDM
D = PW/T
PW
T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T.
RL
Vin 10 V
50Ω
VDD ≒ 30 V


Waveform
Vin
Vout
10%
90%
10%
90%
90%
10%
td(on)
tr
td(off)
tf

2SK2328

Silicon N Channel MOS FET

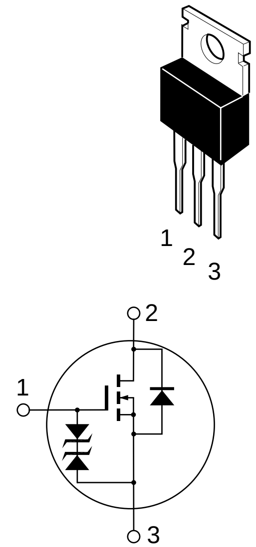
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

TO-220AB



1. Gate
2. Drain (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	650	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

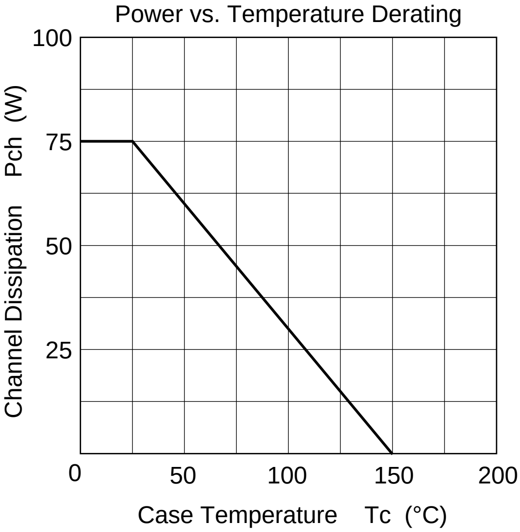
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

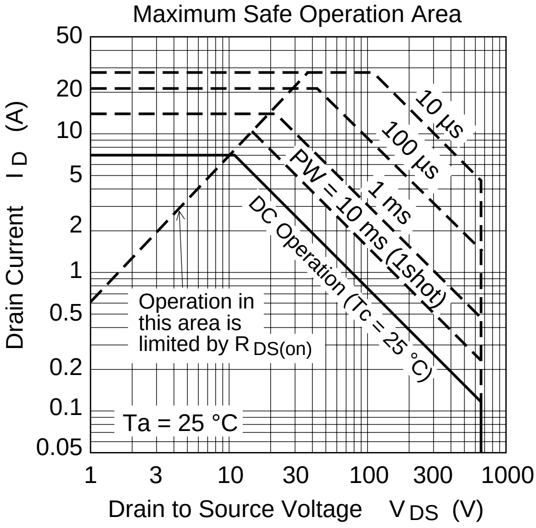
Table 2 Electrical Characteristics (Ta = 25°C)

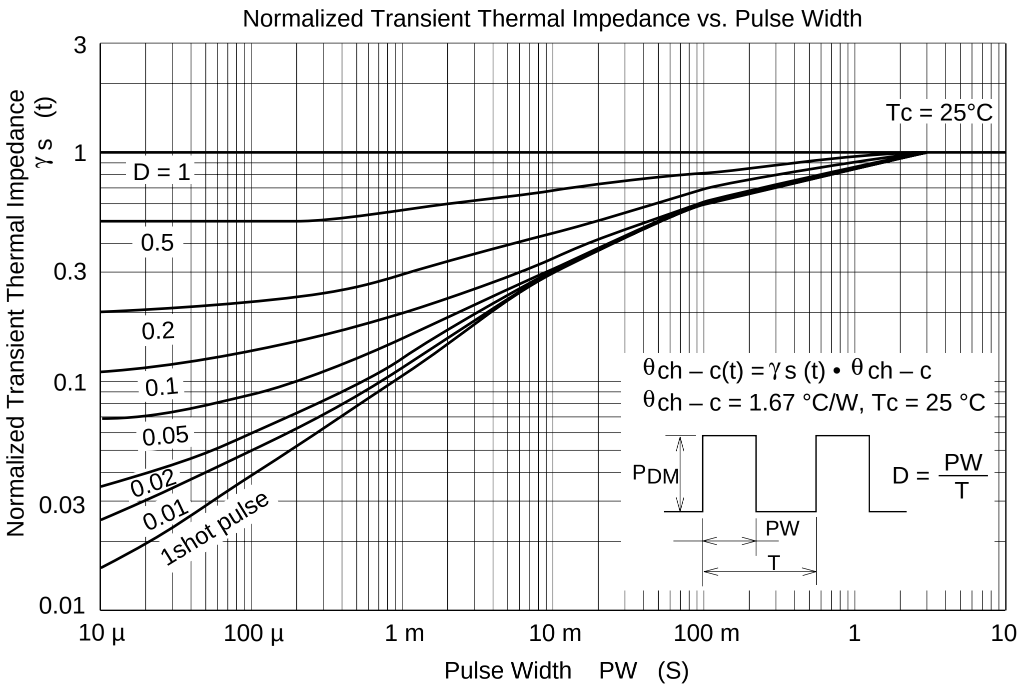
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	650	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 550 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.0	1.4	Ω	I_D = 4A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1180	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	265	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	50	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 4 A
Rise time	t_r	—	50	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	105	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	45	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	420	—	ns	I_F = 7 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1403A


Power vs. Temperature Derating
Channel Dissipation Pch (W)
100
75
50
25
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1
3
10
30
100
300
1000
Drain to Source Voltage V DS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ s (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θ ch – c(t) = γ s (t) • θ ch – c
θ ch – c = 1.67 °C/W, Tc = 25 °C
P DM
PW
T
D = PW / T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

2SK2329(L), 2SK2329(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device can be driven from 3 V source
- Suitable for Switching regulator, DC – DC converter

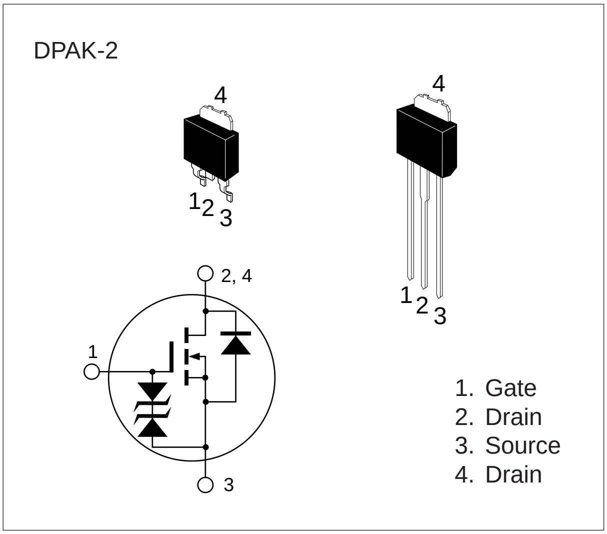


Table 1 Absolute Maximum Ratings (Ta = 25°C)

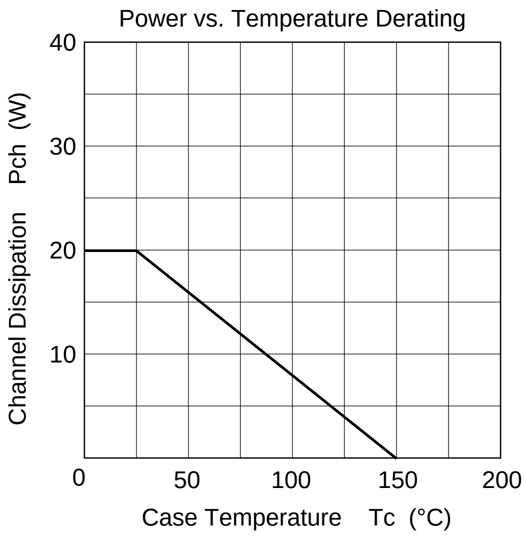
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body–drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

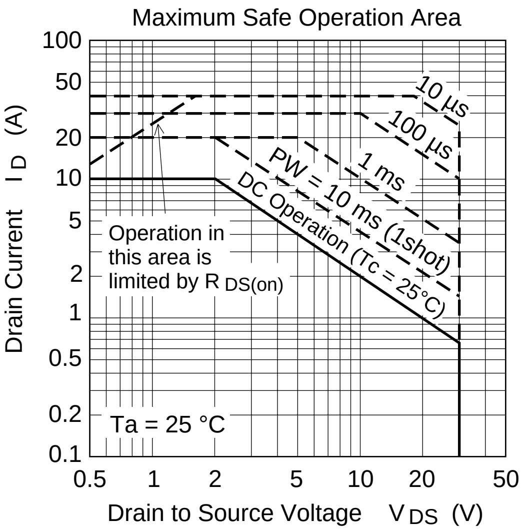
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

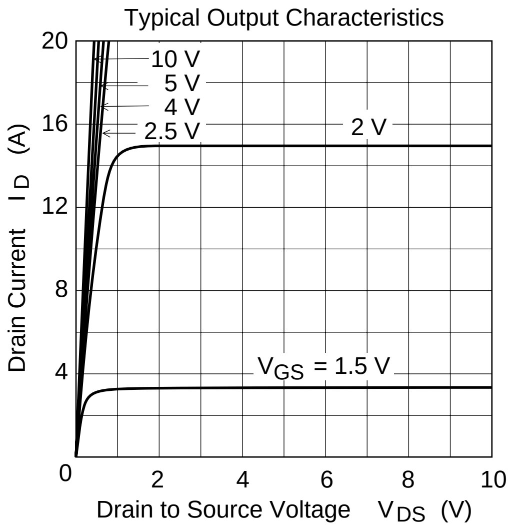
Table 2 Electrical Characteristics (Ta = 25°C)

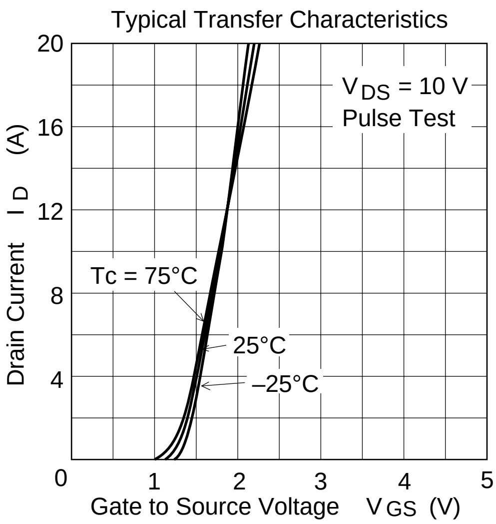
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 25 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.04	Ω	I_D = 5 A V_{GS} = 4 V *
		—	0.04	0.06	Ω	I_D = 5 A V_{GS} = 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	10	18	—	S	I_D = 5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1250	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	540	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	120	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 5 A
Rise time	t_r	—	145	—	ns	V_{GS} = 4 V
Turn–off delay time	$t_{d(off)}$	—	225	—	ns	R_L = 2 Ω
Fall time	t_f	—	125	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 10 A, V_{GS} = 0, diF / dt = 20 A / µs

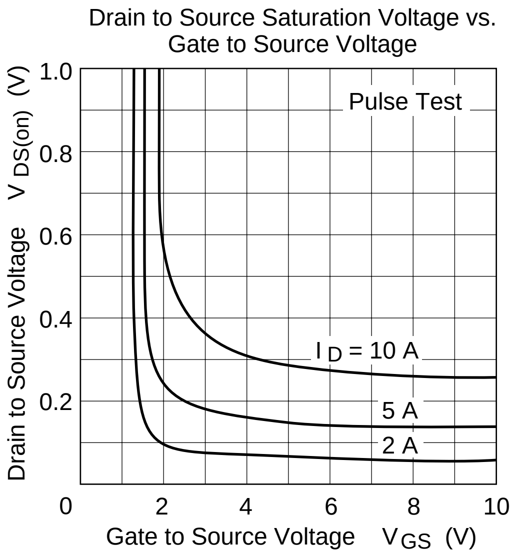
* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

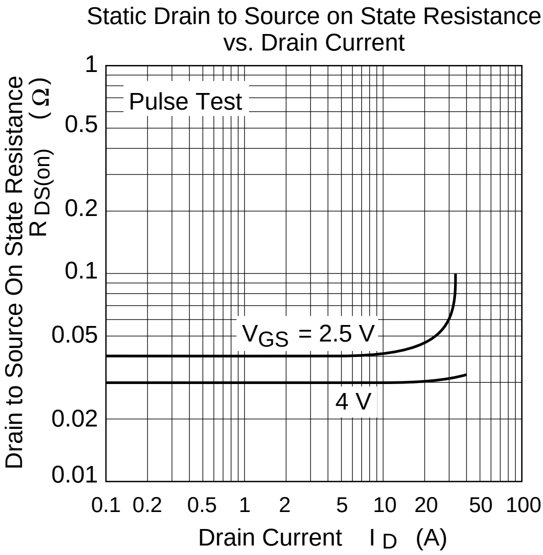

Maximum Safe Operation Area
Drain Current I D (A)
100
50
20
10
5
2
1
0.5
0.2
0.1
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.5
1
2
5
10
20
50
Drain to Source Voltage V DS (V)


Typical Output Characteristics
Drain Current I D (A)
20
16
12
8
4
0
10 V
5 V
4 V
2.5 V
2 V
V GS = 1.5 V
2
4
6
8
10
Drain to Source Voltage V DS (V)

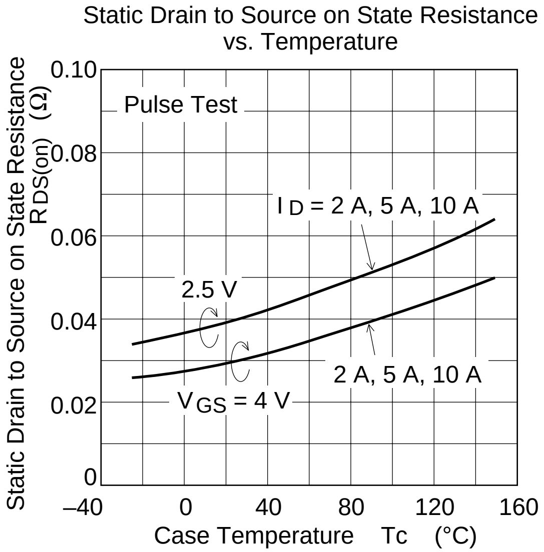

Typical Transfer Characteristics
Drain Current I D (A)
20
16
12
8
4
0
V DS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
1
2
3
4
5
Gate to Source Voltage V GS (V)



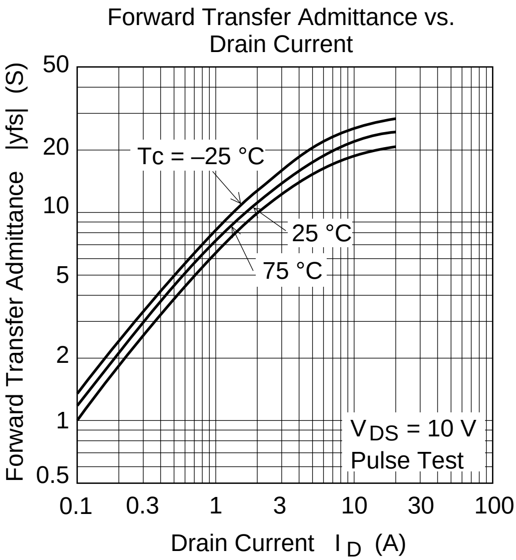
Drain to Source Saturation Voltage vs. Gate to Source Voltage
Pulse Test
I D = 10 A
5 A
2 A
Drain to Source Voltage V DS(on) (V)
Gate to Source Voltage V GS (V)



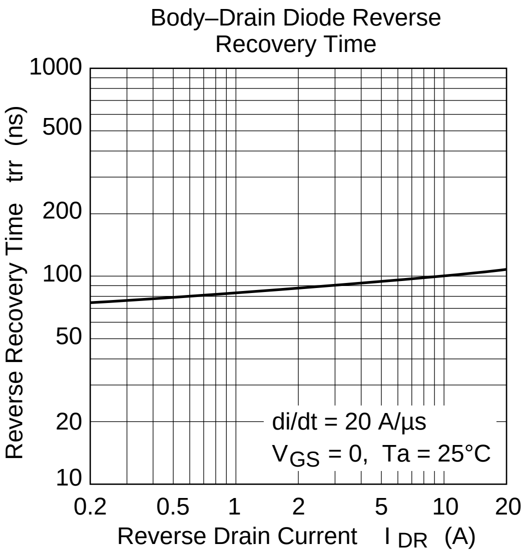
Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
V GS = 2.5 V
4 V
Drain to Source On State Resistance R DS(on) (Ω)
Drain Current I D (A)

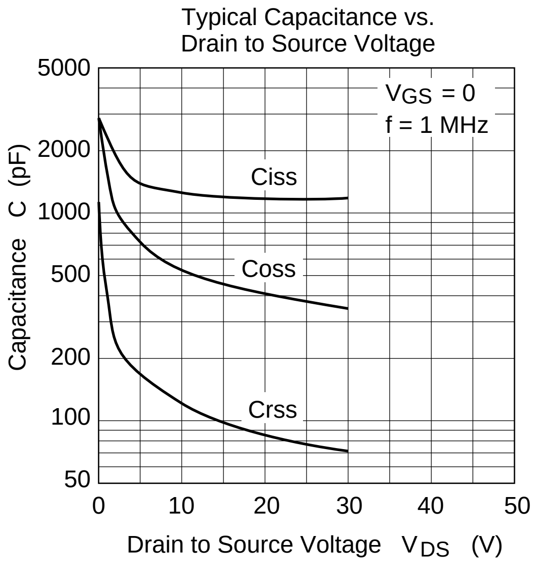


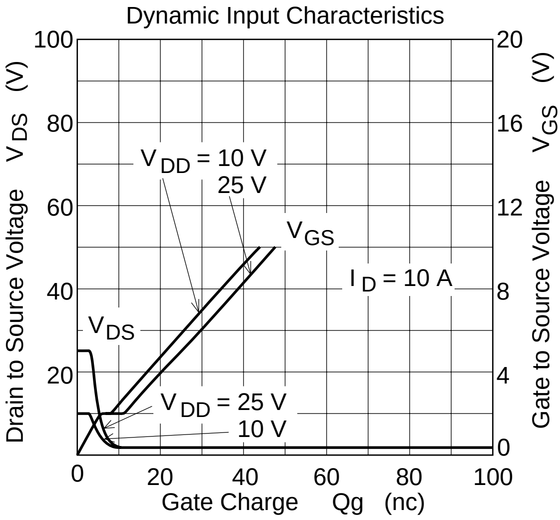
Static Drain to Source on State Resistance vs. Temperature
Pulse Test
I D = 2 A, 5 A, 10 A
2.5 V
2 A, 5 A, 10 A
V GS = 4 V
Static Drain to Source on State Resistance R DS(on) (Ω)
Case Temperature Tc (°C)

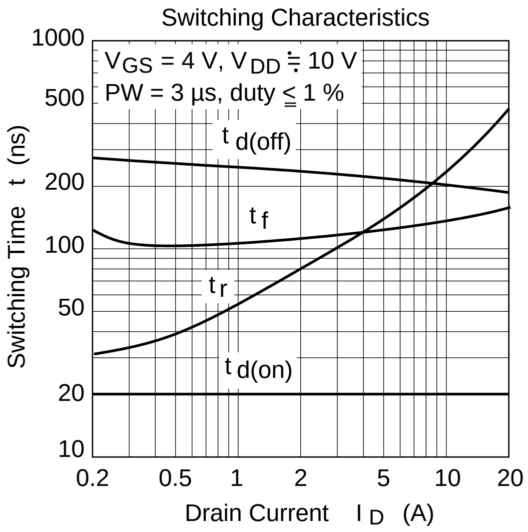


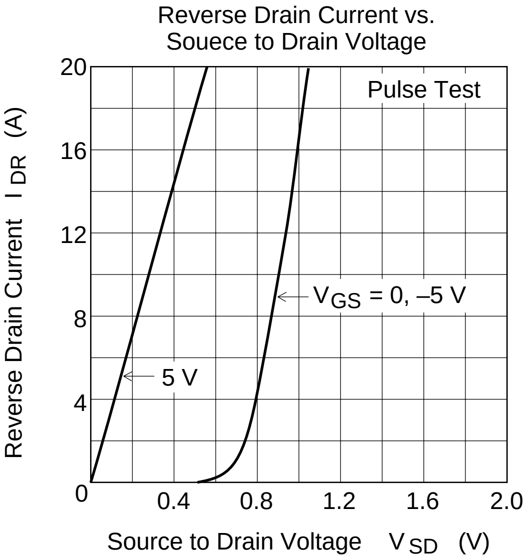
Forward Transfer Admittance vs. Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)

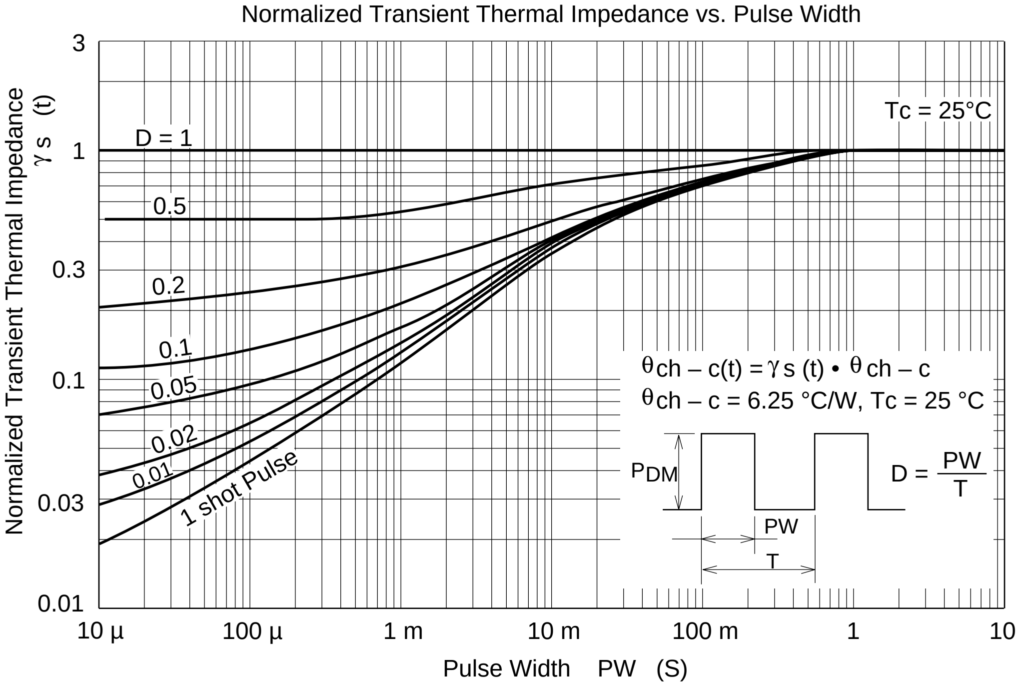

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di/dt = 20 A/μs
V GS = 0, Ta = 25°C
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
V GS = 0
f = 1 MHz
Ciss
Coss
Crss
0
10
20
30
40
50
Drain to Source Voltage V DS (V)

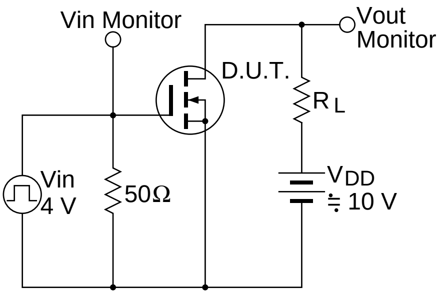

Dynamic Input Characteristics
Drain to Source Voltage V DS (V)
100
80
60
40
20
V DD = 10 V
25 V
V GS
I D = 10 A
V DS
V DD = 25 V
10 V
20
16
12
8
4
0
Gate to Source Voltage V GS (V)
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
V GS = 4 V, V DD ≒ 10 V
PW = 3 μs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
0.2
0.5
1
2
5
10
20
Drain Current I D (A)

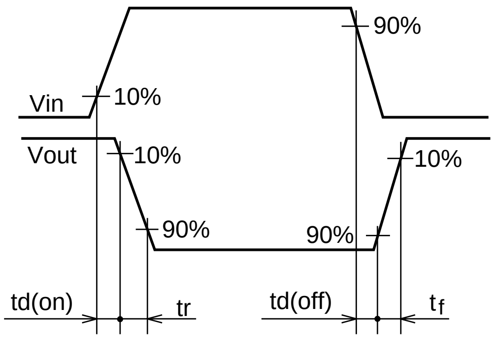

Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
5 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
4
8
12
16
20
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
P_{DM}
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10

Switching Time Test Circuit



Waveform



2SK2330L, 2SK2330S

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- No secondary breakdown
- Suitable for Switching regulator, DC – DC converter

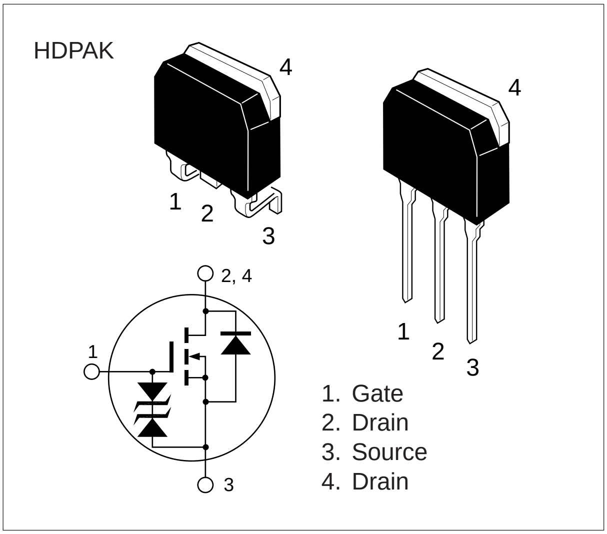


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$*	60	A
Body–drain diode reverse drain current	I_{DR}	15	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.4	Ω	I_D = 8 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	8	13	—	S	I_D = 8 A V_{DS} = 10 V *
Input capacitance	Ciss	—	2050	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	600	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	75	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	I_D = 8 A
Rise time	t_r	—	110	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	150	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 15 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	500	—	µs	I_F = 15 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1168.

2SK2334(L), 2SK2334(S)

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche Ratings

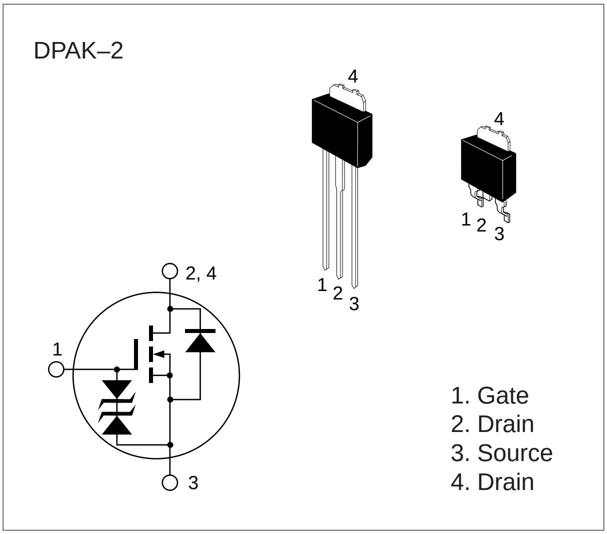


Table 1 Absolute Maximum Ratings (Ta = 25°C)

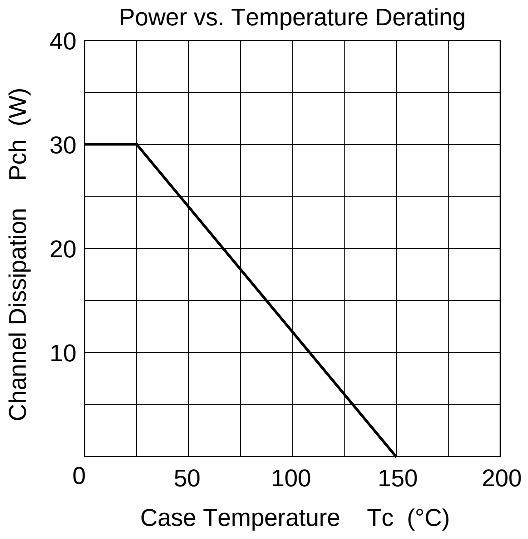
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body–drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP}***	20	A
Avalanche energy	E_{AR}***	34	mJ
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

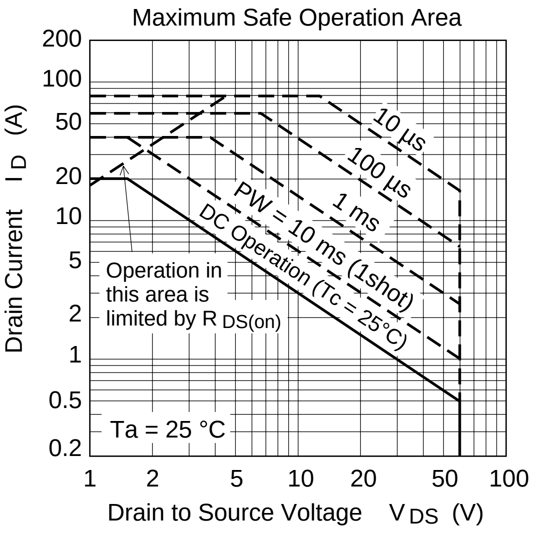
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

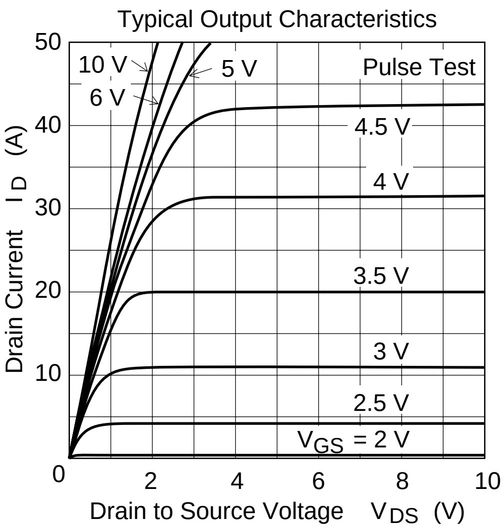
Table 2 Electrical Characteristics (Ta = 25°C)

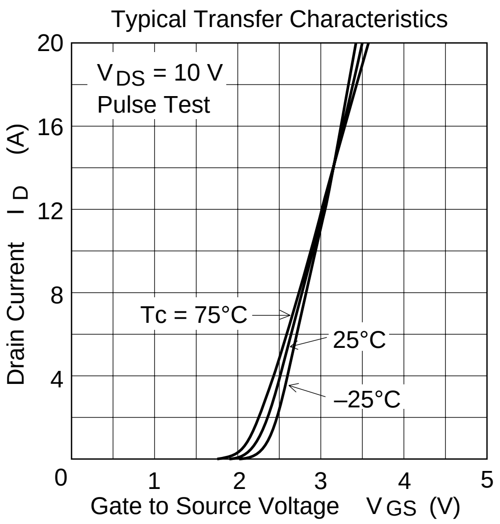
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.04	0.055	Ω	I_D = 10 A V_{GS} = 10 V *
		—	0.055	0.07	Ω	I_D = 10 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	9	15	—	S	I_D = 10 A V_{DS} = 10 V *
Input capacitance	Ciss	—	980	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	135	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	14	—	ns	I_D = 10 A
Rise time	t_r	—	90	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	180	—	ns	R_L = 3 Ω
Fall time	t_f	—	125	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	µs	I_F = 20 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

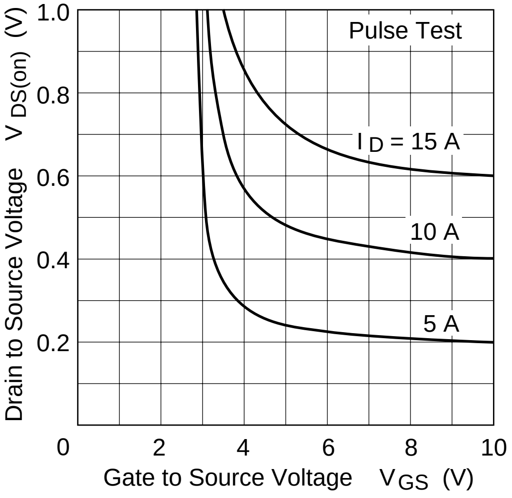

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
200
100
50
20
10
5
2
1
0.5
0.2
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1
2
5
10
20
50
100
Drain to Source Voltage V DS (V)

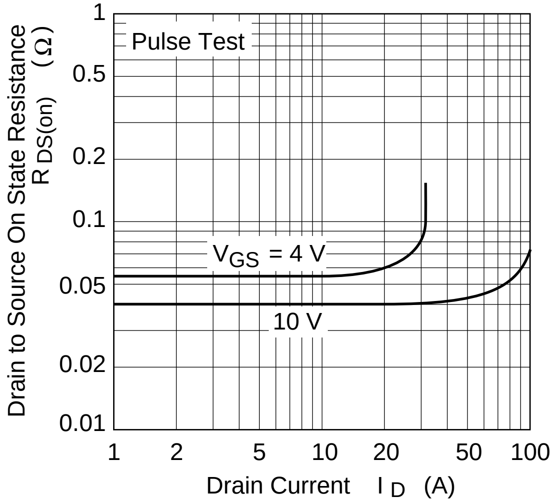

Typical Output Characteristics
Drain Current I D (A)
50
40
30
20
10
0
10 V
6 V
5 V
Pulse Test
4.5 V
4 V
3.5 V
3 V
2.5 V
VGS = 2 V
2
4
6
8
10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
20
16
12
8
4
0
VDS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
1
2
3
4
5
Gate to Source Voltage V GS (V)

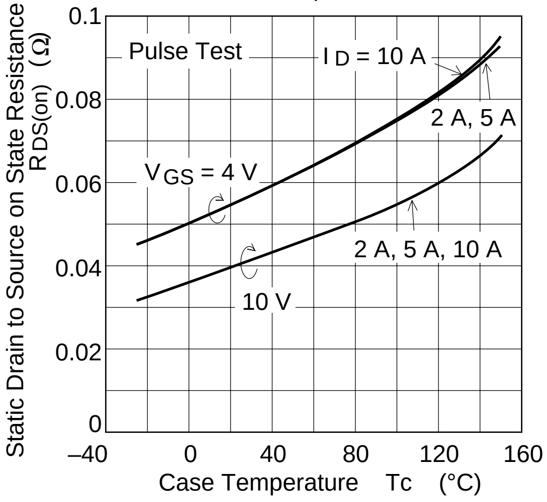
Drain to Source Saturation Voltage vs. Gate to Source Voltage



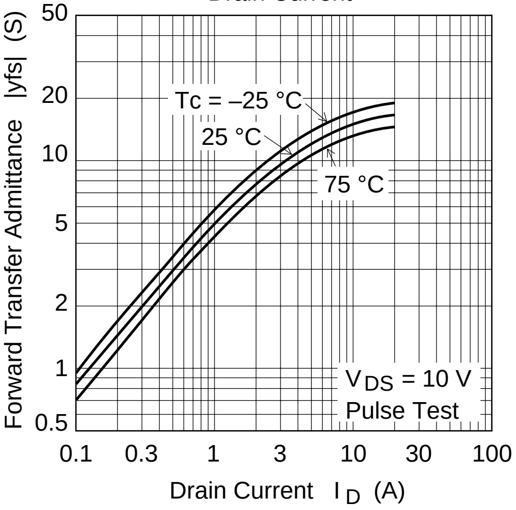
Static Drain to Source on State Resistance vs. Drain Current

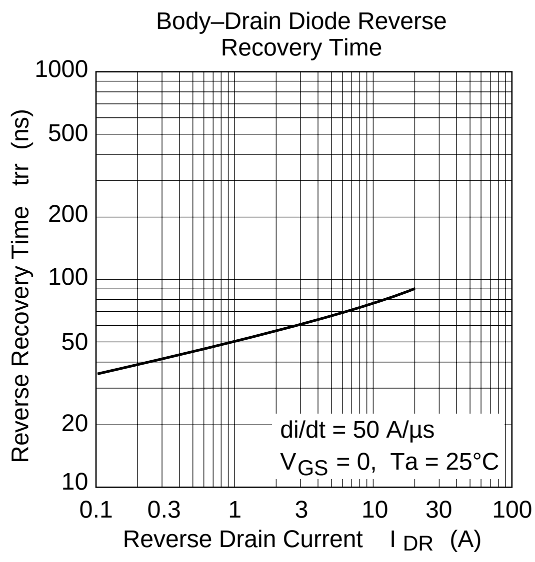


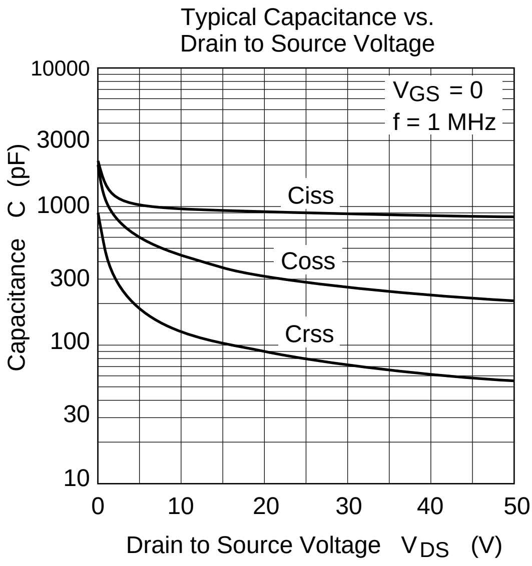
Static Drain to Source on State Resistance vs. Temperature

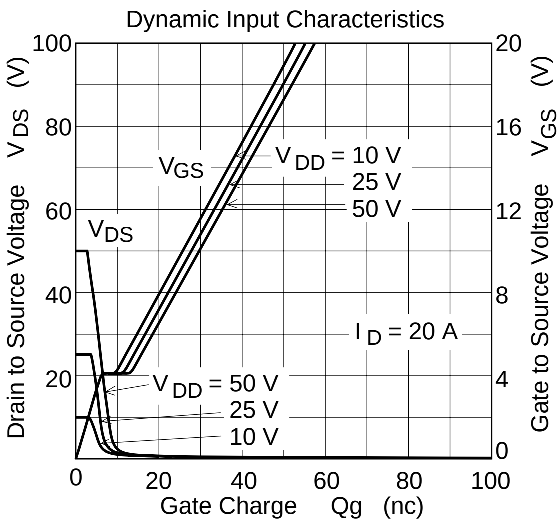


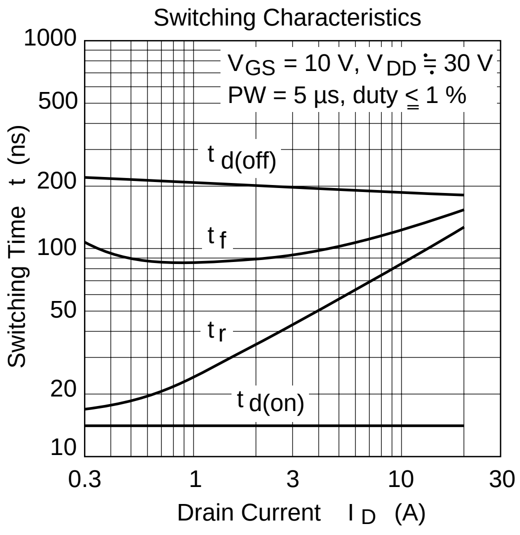
Forward Transfer Admittance vs. Drain Current



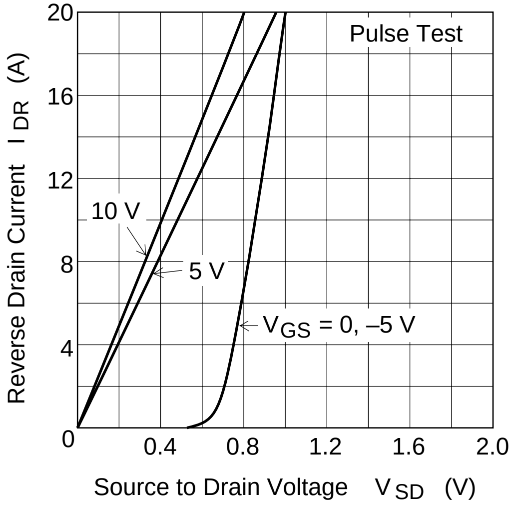

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)
di/dt = 50 A/µs
VGS = 0, Ta = 25°C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
VGS = 0
f = 1 MHz
Ciss
Coss
Crss

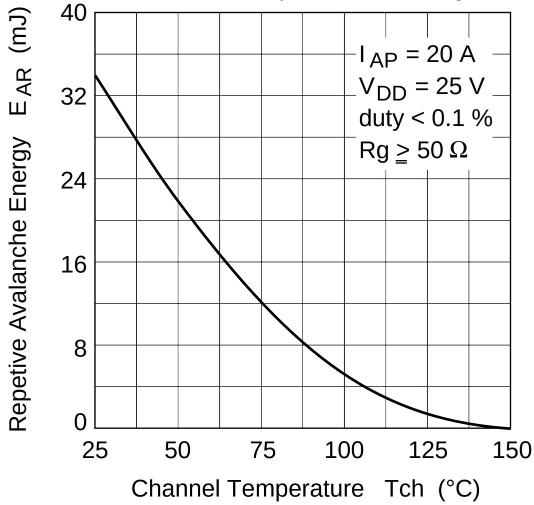

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
16
12
8
4
0
20
40
60
80
100
Gate Charge Qg (nc)
VGS
VDD = 10 V
25 V
50 V
VDS
ID = 20 A
VDD = 50 V
25 V
10 V


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.3
1
3
10
30
Drain Current ID (A)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)

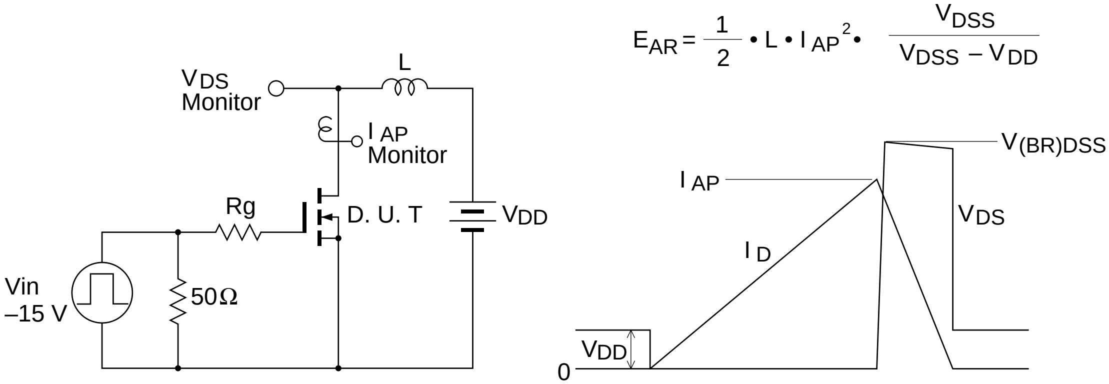
Reverse Drain Current vs. Souece to Drain Voltage



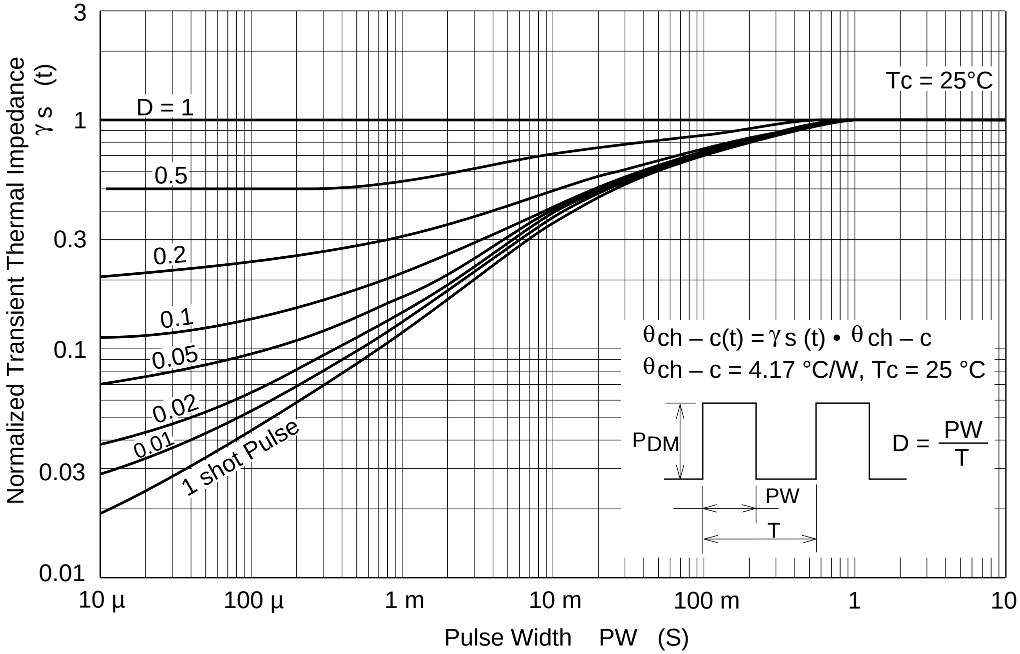
Maximun Avalanche Energy vs. Channel Temperature Derating



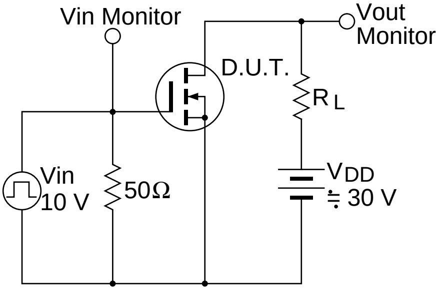
Avalanche Test Circuit and Waveform



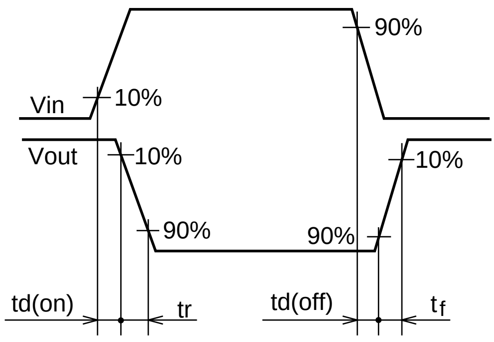
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveform



2SK2345

Silicon N Channel MOS FET

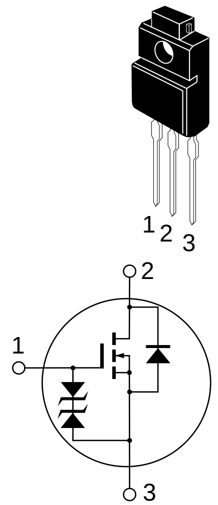
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switchingregulator, DC–DC converter

TO-220FM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	350	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	6	A
Drain peak current	$I_{D(pulse)}$*	24	A
Body–drain diode reverse drain current	I_{DR}	6	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

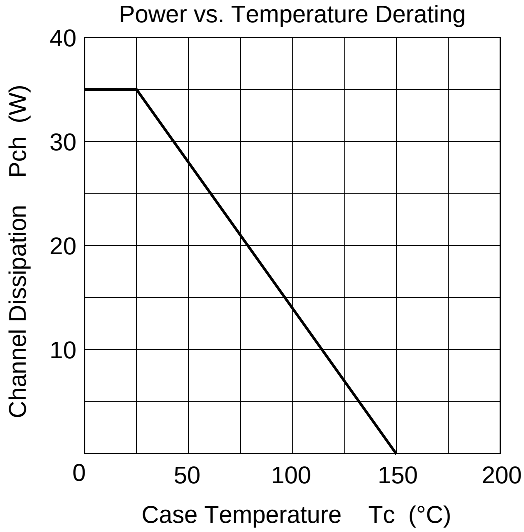
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

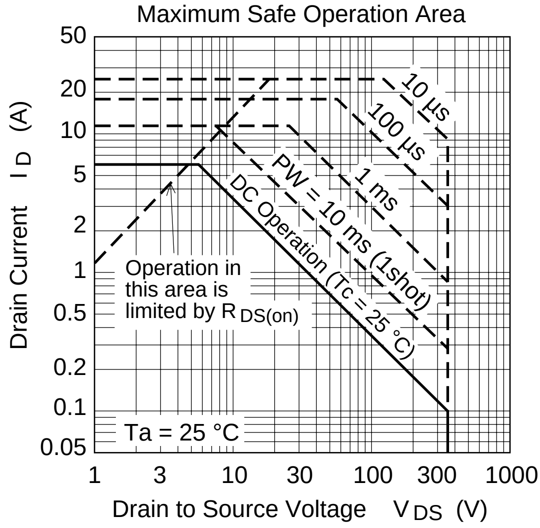
Table 2 Electrical Characteristics (Ta = 25°C)

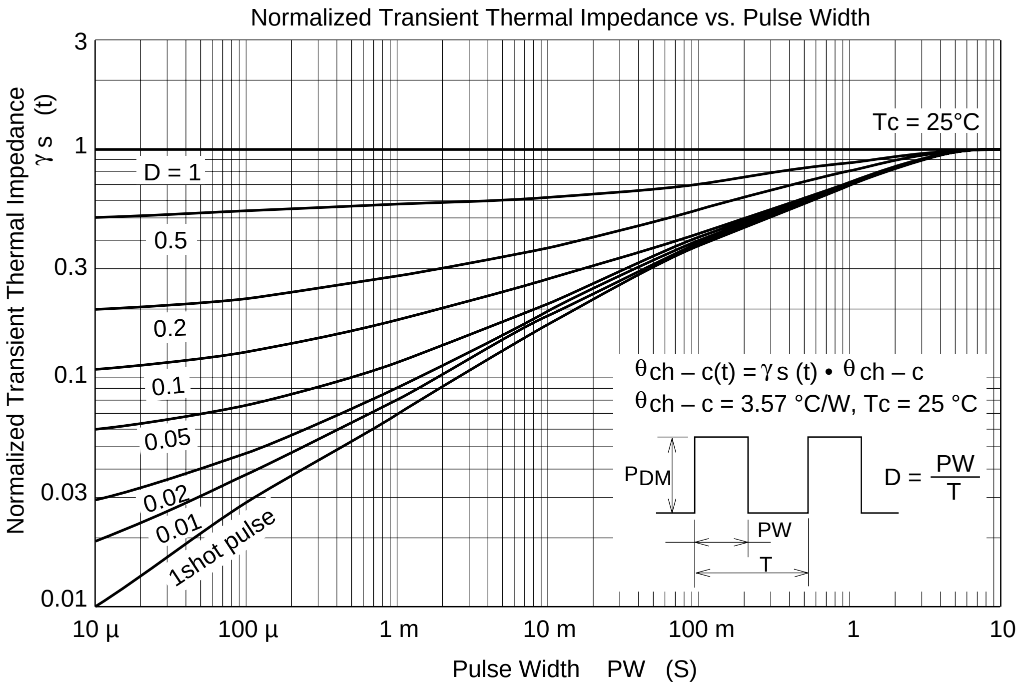
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	350	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 350 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.6	0.8	Ω	I_D = 3 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	2.5	4.5	—	S	I_D = 3 A V_{DS} = 10 V *
Input capacitance	Ciss	—	635	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	230	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	40	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 3 A
Rise time	t_r	—	40	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	60	—	ns	R_L = 10 Ω
Fall time	t_f	—	35	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 6 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	230	—	ns	I_F = 6 A, V_{GS} = 0, di_F / dt = 100 A / µs

* Pulse Test

See characteristic curves of 2SK1400A.


Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
1
3
10
30
100
300
1000
Drain to Source Voltage V DS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ s (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θ ch – c(t) = γ s (t) • θ ch – c
θ ch – c = 3.57 °C/W, Tc = 25 °C
P DM
PW
T
D = PW / T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

2SK2346

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

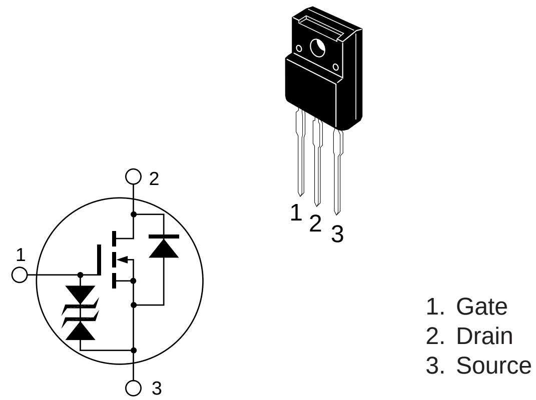


Table 1 Absolute Maximum Ratings (Ta = 25°C)

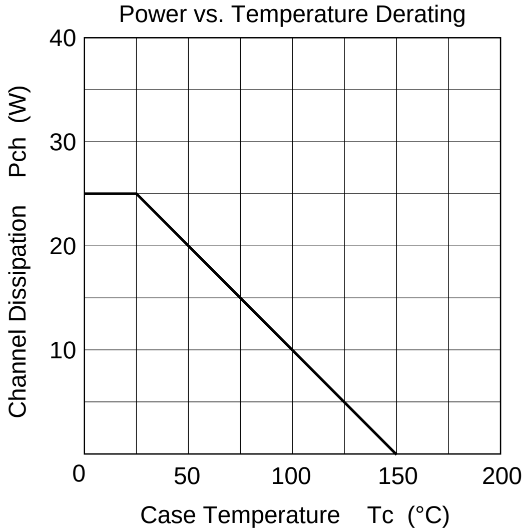
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	80	A
Body–drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP}***	20	A
Avalanche energy	E_{AR}***	34	mJ
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

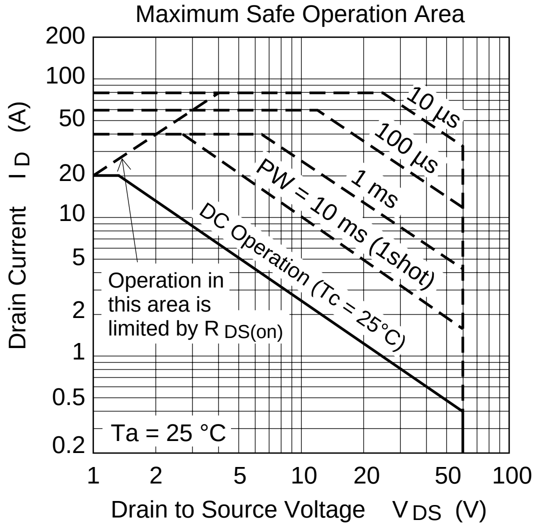
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

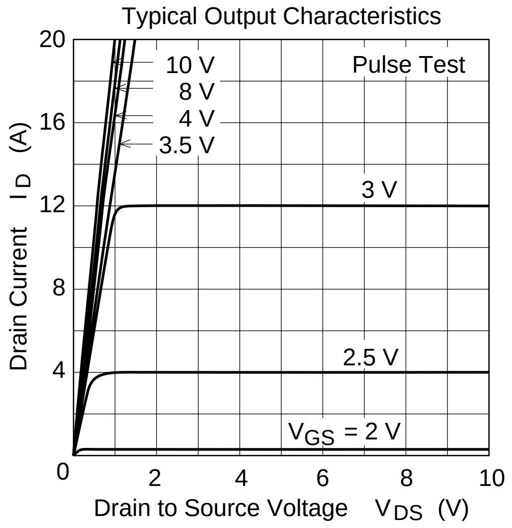
Table 2 Electrical Characteristics (Ta = 25°C)

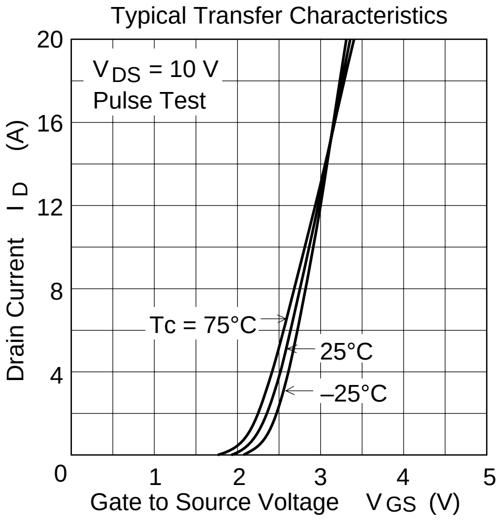
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.036	0.05	Ω	I_D = 10 A V_{GS} = 10 V *
		—	0.05	0.07	Ω	I_D = 10 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	17	—	S	I_D = 10 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1130	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	520	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	155	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 10 A
Rise time	t_r	—	90	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	185	—	ns	R_L = 3 Ω
Fall time	t_f	—	125	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	125	—	ns	I_F = 20 A, V_{GS} = 0, diF / dt = 50 A / µs

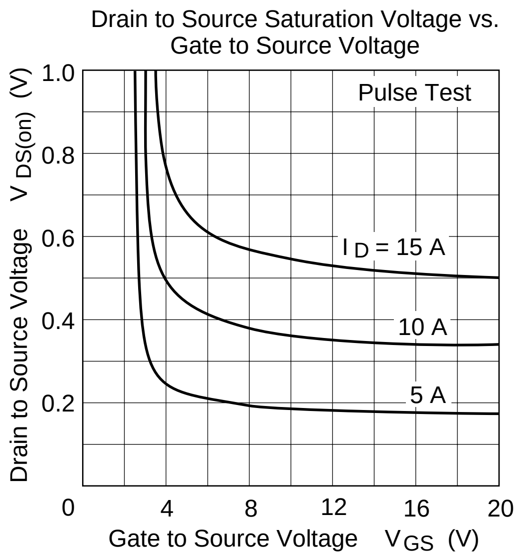
* Pulse Test

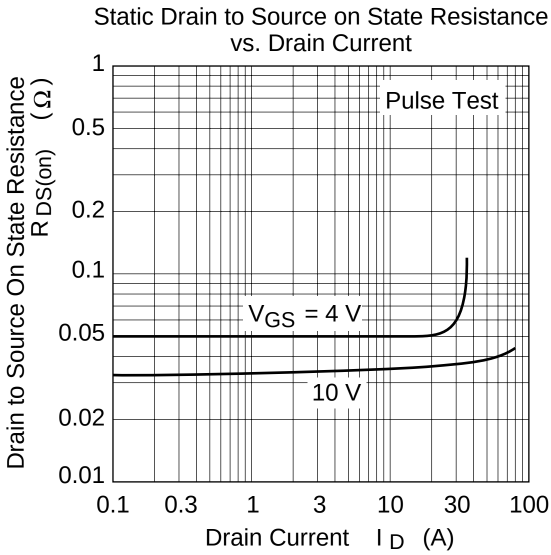

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

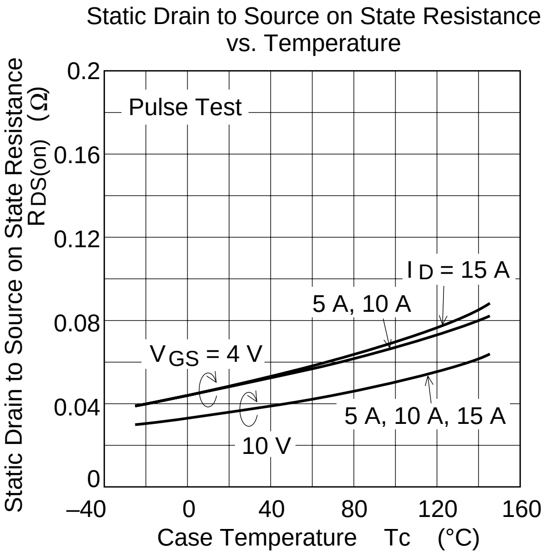

Maximum Safe Operation Area
Drain Current I D (A)
200
100
50
20
10
5
2
1
0.5
0.2
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1
2
5
10
20
50
100
Drain to Source Voltage V DS (V)

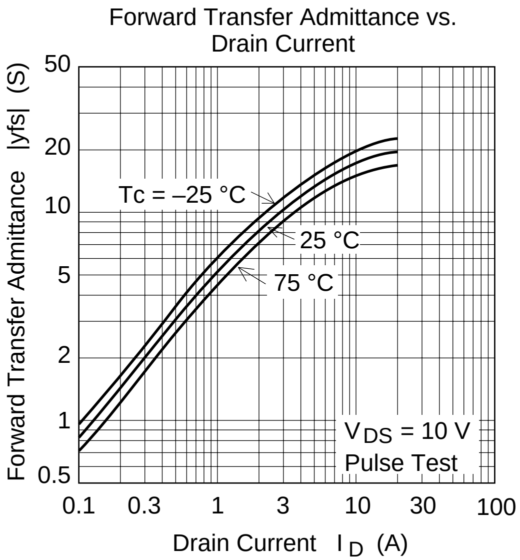

Typical Output Characteristics
Drain Current I D (A)
20
16
12
8
4
0
10 V
8 V
4 V
3.5 V
Pulse Test
3 V
2.5 V
VGS = 2 V
2
4
6
8
10
Drain to Source Voltage VDS (V)

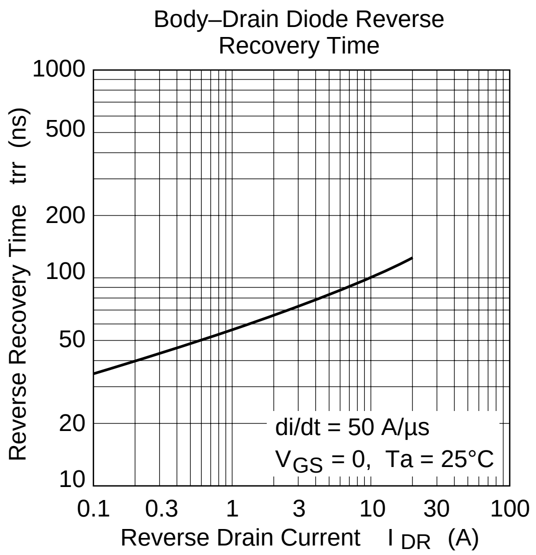

Typical Transfer Characteristics
Drain Current I D (A)
20
16
12
8
4
0
VDS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
1
2
3
4
5
Gate to Source Voltage VGS (V)


Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 15 A
10 A
5 A
Drain to Source Voltage V DS(on) (V)
1.0
0.8
0.6
0.4
0.2
0
4
8
12
16
20
Gate to Source Voltage V GS (V)

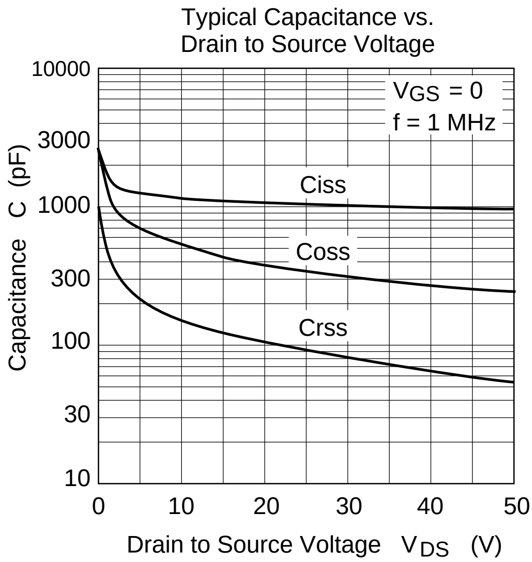

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = 4 V
10 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1
0.3
1
3
10
30
100
Drain Current I D (A)


Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 15 A
5 A, 10 A
V GS = 4 V
10 V
5 A, 10 A, 15 A
Static Drain to Source on State Resistance R DS(on) (Ω)
0.2
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

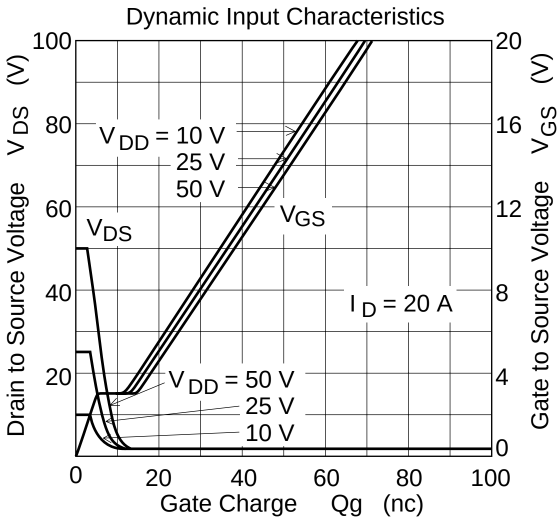

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
0.1
0.3
1
3
10
30
100
Drain Current I D (A)



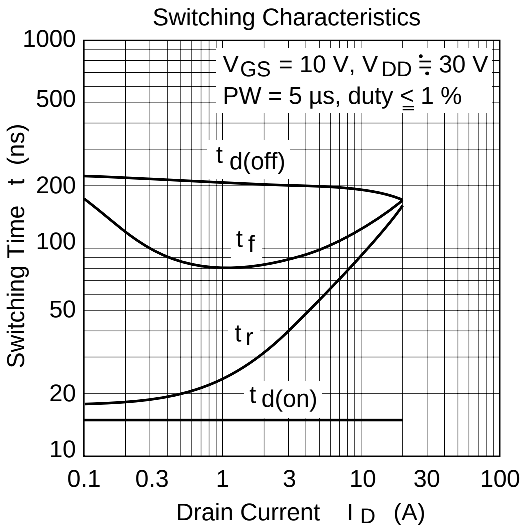
Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)
di/dt = 50 A/µs
VGS = 0, Ta = 25°C



Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
VGS = 0
f = 1 MHz
Ciss
Coss
Crss

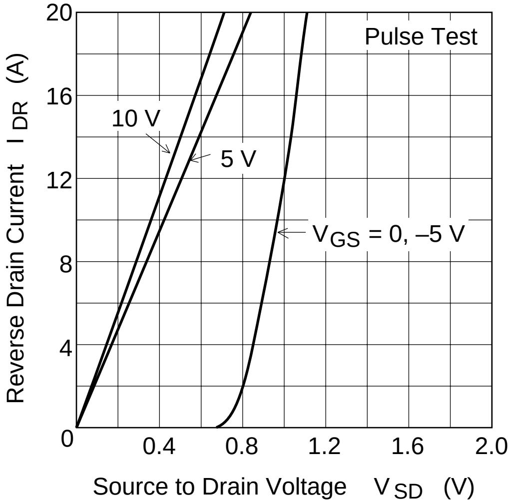


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
20
40
60
80
100
20
16
12
8
4
0
Gate Charge Qg (nc)
VDD = 10 V
25 V
50 V
VGS
VDS
I D = 20 A
VDD = 50 V
25 V
10 V

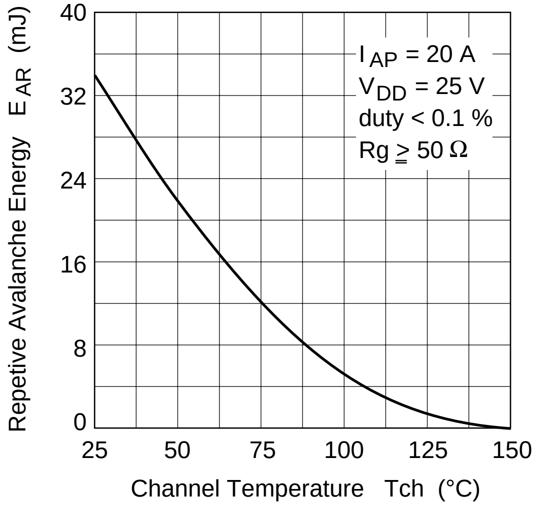


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.1
0.3
1
3
10
30
100
Drain Current I D (A)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)

Reverse Drain Current vs.
Souece to Drain Voltage

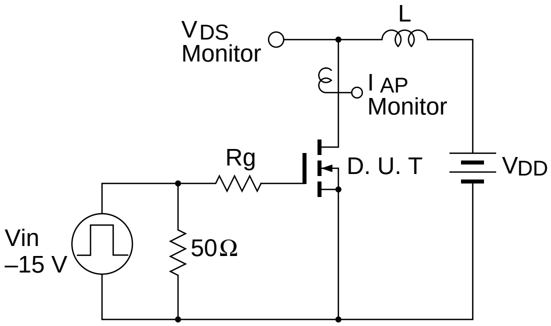


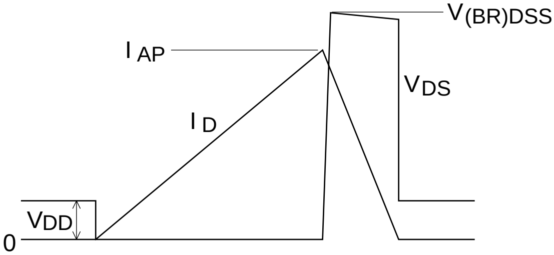
Maximun Avalanche Energy vs.
Channel Temperature Derating



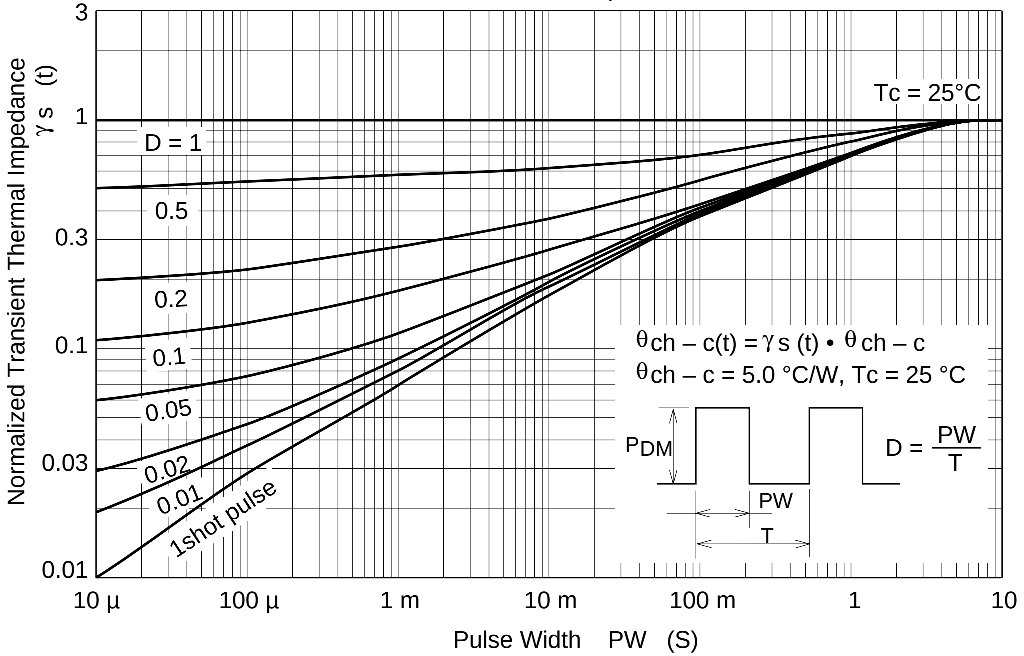
Avalanche Test Circuit and Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

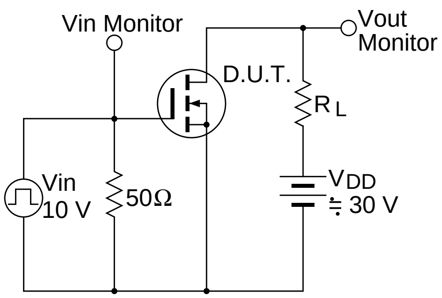




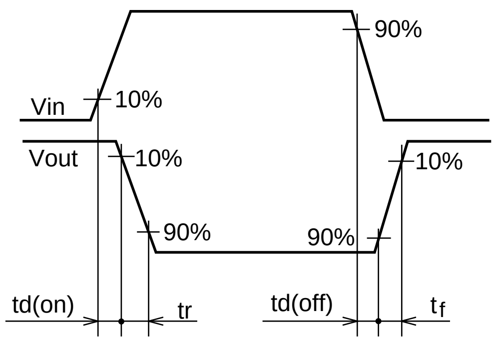
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



Waveform



2SK2373

Silicon N Channel MOS FET

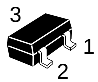
Application

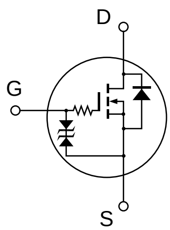
Low frequency power switching

Features

- Low on–resistance
- Small package
- Low drive current
- 4 V gate drive device - - - can be driven from 5 V source.
- Suitable for low signal load switch

MPAK





1. Source
2. Gate
3. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

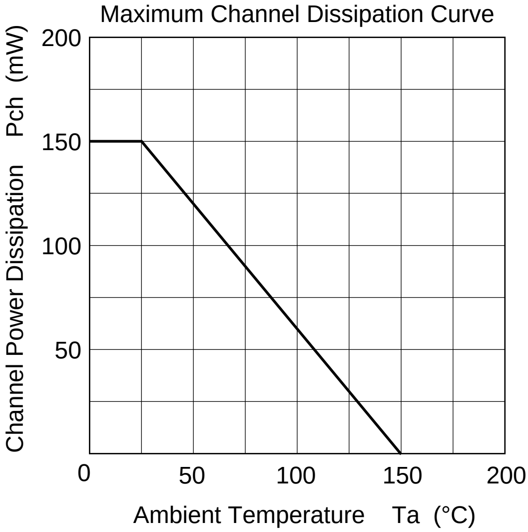
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}$*	0.4	A
Body–drain diode reverse drain current	I_{DR}	0.2	A
Channel dissipation	Pch**	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

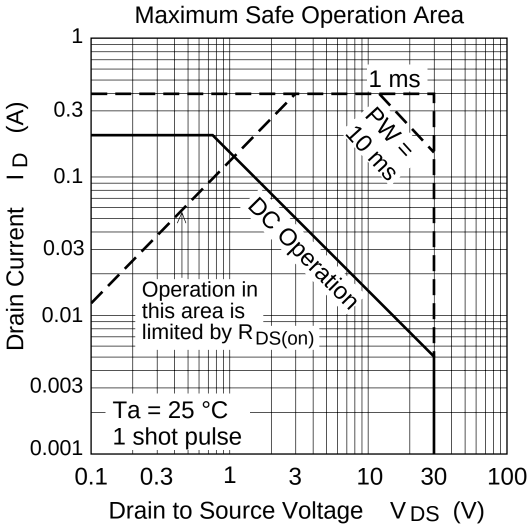
* PW ≤ 100 µs, duty cycle ≤ 10 %
** Marking is “ZE–”.

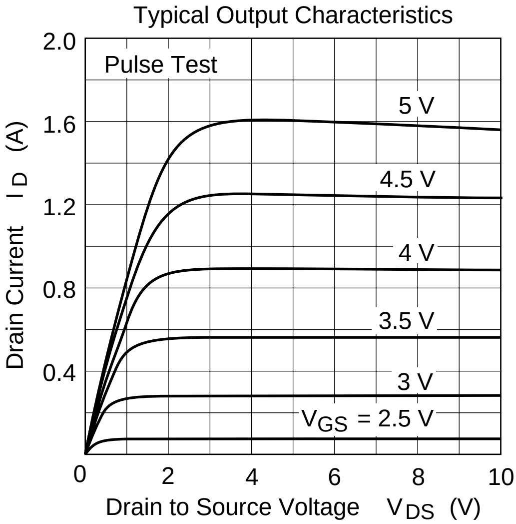
Table 2 Electrical Characteristics (Ta = 25°C)

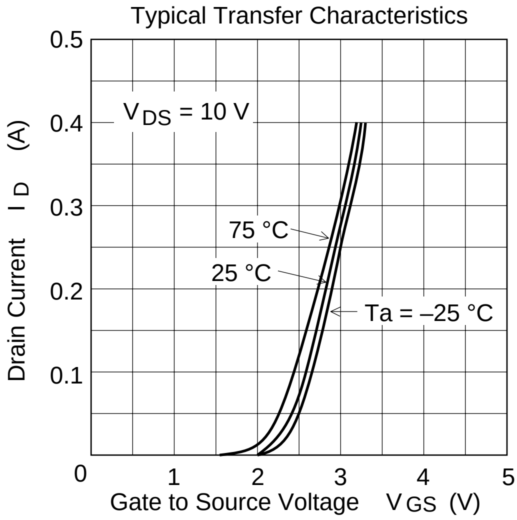
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±2	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 10 µA, V_{DS} = 5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.4	2.5	Ω	I_D = 20 mA V_{GS} = 4 V *
		—	1.0	1.4	Ω	I_D = 10 mA V_{GS} = 10 V *
Input capacitance	Ciss	—	17.8	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	25.4	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3.7	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	50	—	ns	I_D = 0.1 A
Rise time	t_r	—	125	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	660	—	ns	R_L = 100 Ω
Fall time	t_f	—	400	—	ns	PW = 2 µs

* Pulse Test

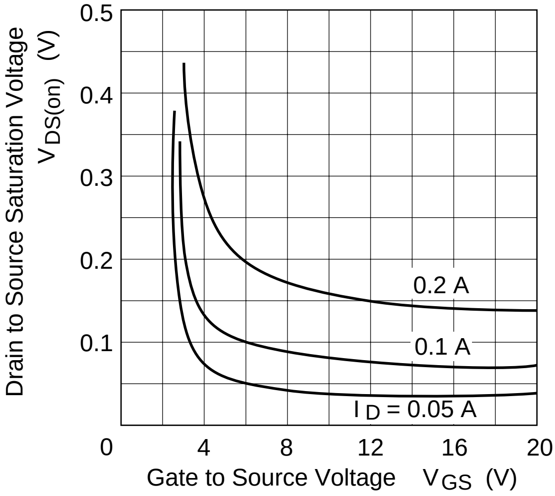

Maximum Channel Dissipation Curve
Channel Power Dissipation Pch (mW)
200
150
100
50
0
50
100
150
200
Ambient Temperature Ta (°C)


Maximum Safe Operation Area
Drain Current I D (A)
1
0.3
0.1
0.03
0.01
0.003
0.001
1 ms
PW = 10 ms
DC Operation
Operation in this area is limited by R DS(on)
Ta = 25 °C
1 shot pulse
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

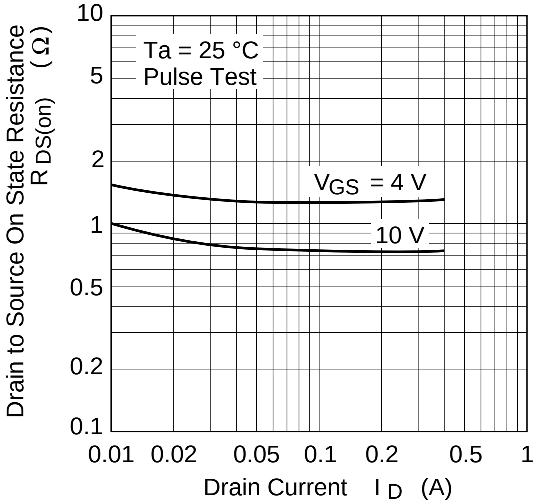

Typical Output Characteristics
Drain Current I D (A)
2.0
1.6
1.2
0.8
0.4
Pulse Test
5 V
4.5 V
4 V
3.5 V
3 V
VGS = 2.5 V
0
2
4
6
8
10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
0.5
0.4
0.3
0.2
0.1
V DS = 10 V
75 °C
25 °C
Ta = –25 °C
0
1
2
3
4
5
Gate to Source Voltage V GS (V)

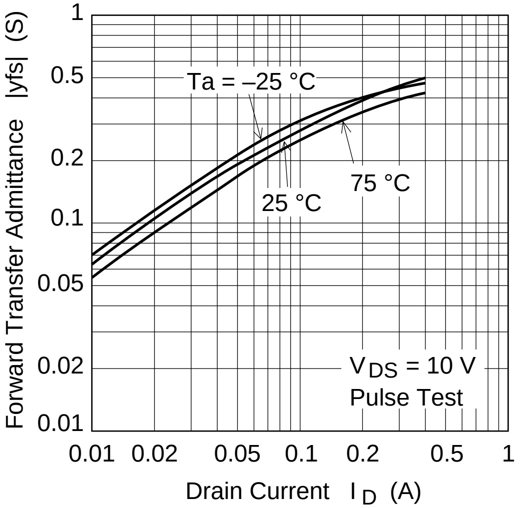
Drain to Source Saturation Voltage vs. Gate to Source Voltage



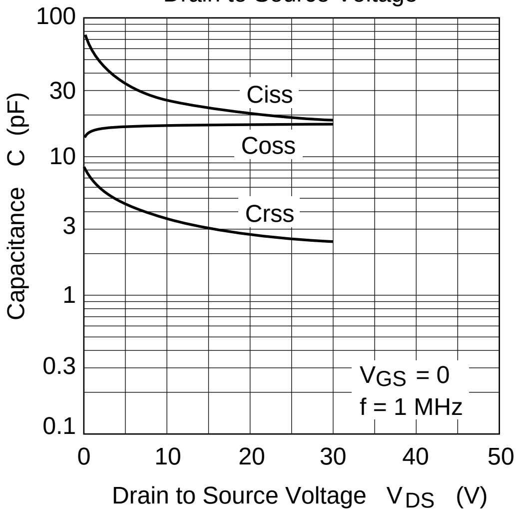
Static Drain to Source on State Resistance vs. Drain Current

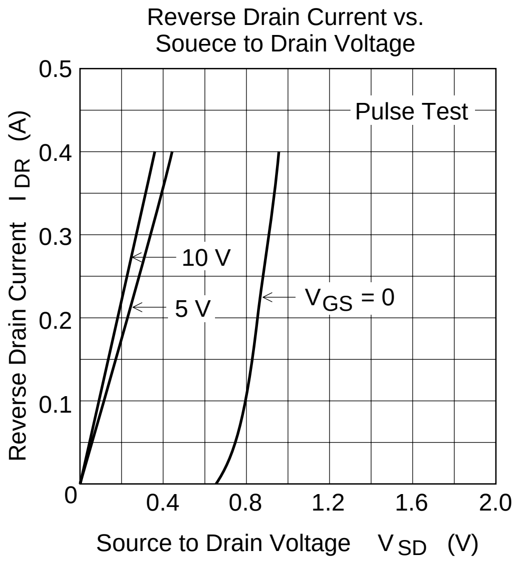


Forward Transfer Admittance vs. Drain Current



Typical Capacitance vs. Drain to Source Voltage




Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0
Reverse Drain Current I DR (A)
0.5
0.4
0.3
0.2
0.1
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage VSD (V)

2SK2390

Silicon N Channel MOS FET

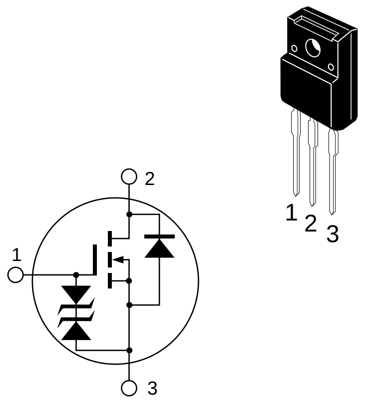
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

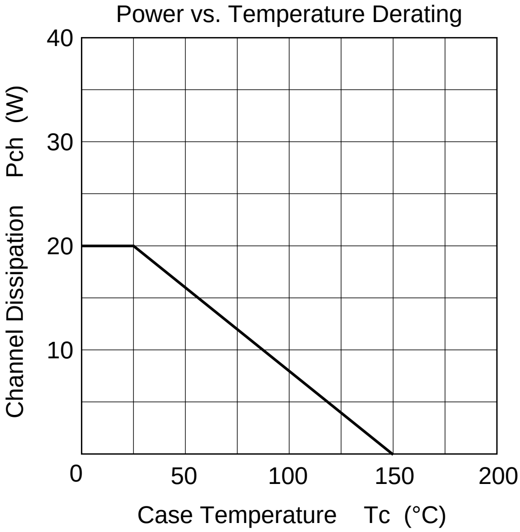
Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	12	A
Drain peak current	$I_{D(pulse)}$*	48	A
Body–drain diode reverse drain current	I_{DR}	12	A
Avalanche current	I_{AP}***	12	A
Avalanche energy	E_{AR}***	12	mJ
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

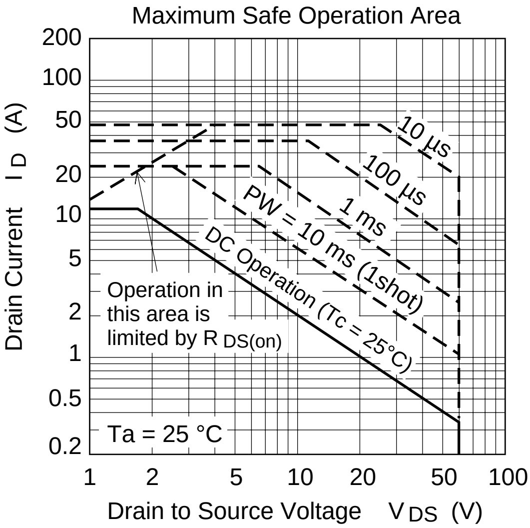
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

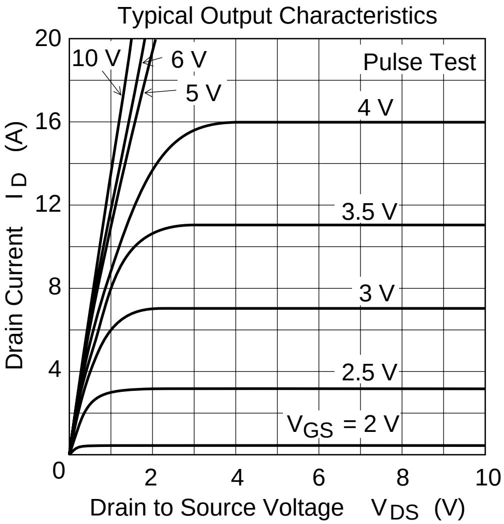
Table 2 Electrical Characteristics (Ta = 25°C)

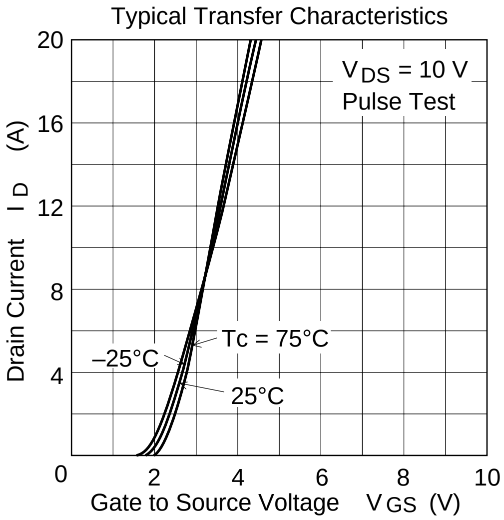
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.09	Ω	I_D = 6 A V_{GS} = 10 V *
		—	0.11	0.15	Ω	I_D = 6 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	4	8	—	S	I_D = 6 A V_{DS} = 10 V *
Input capacitance	Ciss	—	450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	240	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	60	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	10	—	ns	I_D = 6 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 5 Ω
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	I_F = 12 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	95	—	ns	I_F = 12 A, V_{GS} = 0, diF / dt = 50 A / µs

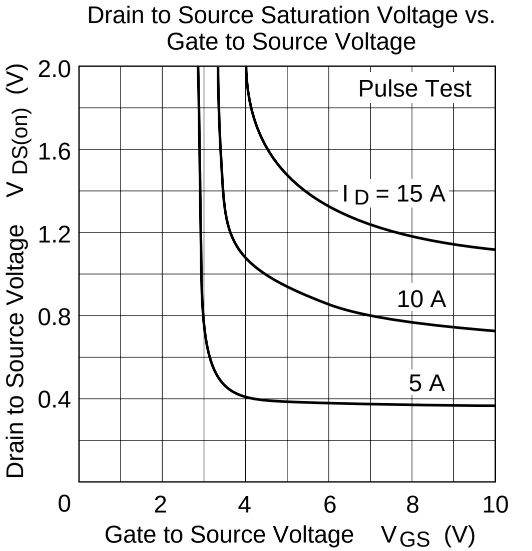
* Pulse Test

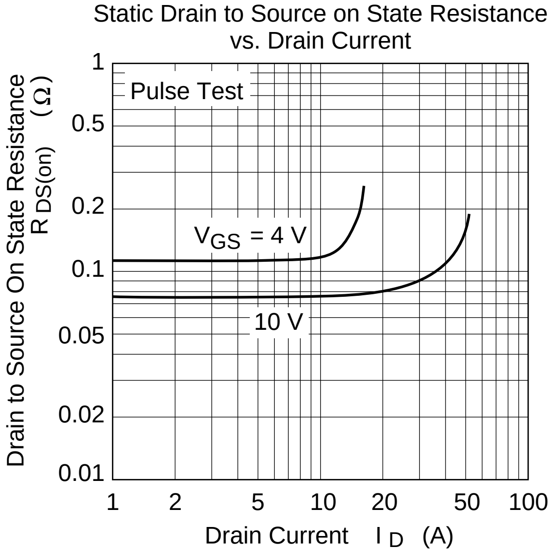

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)

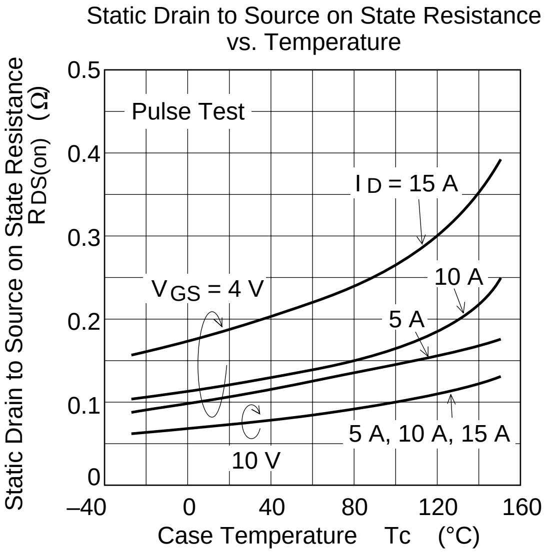

Maximum Safe Operation Area
Drain Current I D (A)
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
Drain to Source Voltage V DS (V)

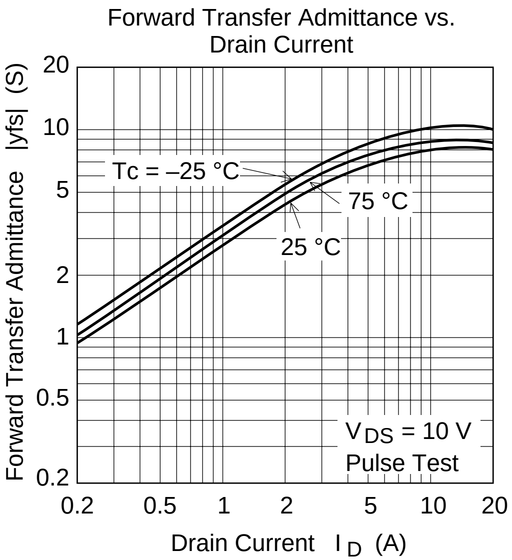

Typical Output Characteristics
Drain Current I D (A)
10 V
6 V
5 V
Pulse Test
4 V
3.5 V
3 V
2.5 V
VGS = 2 V
Drain to Source Voltage V DS (V)

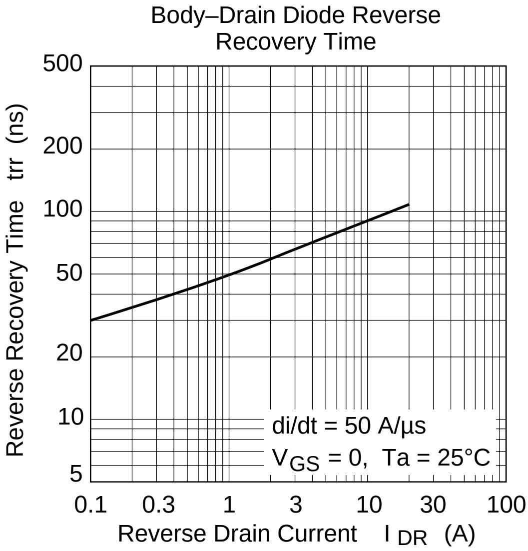

Typical Transfer Characteristics
Drain Current I D (A)
VDS = 10 V
Pulse Test
Tc = 75°C
–25°C
25°C
Gate to Source Voltage V GS (V)

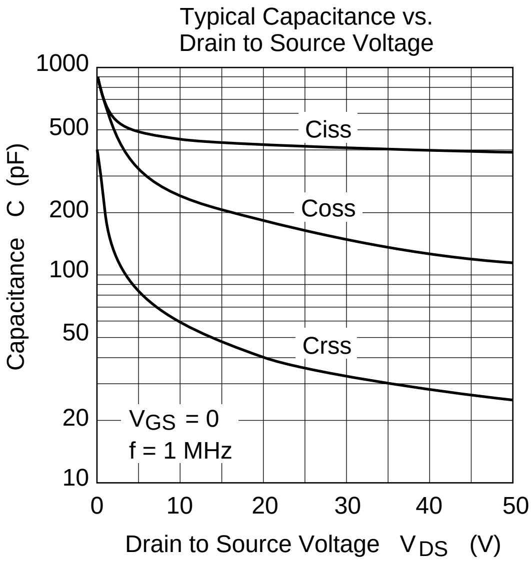

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 15 A
10 A
5 A
Drain to Source Voltage V DS(on) (V)
Gate to Source Voltage V GS (V)
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10

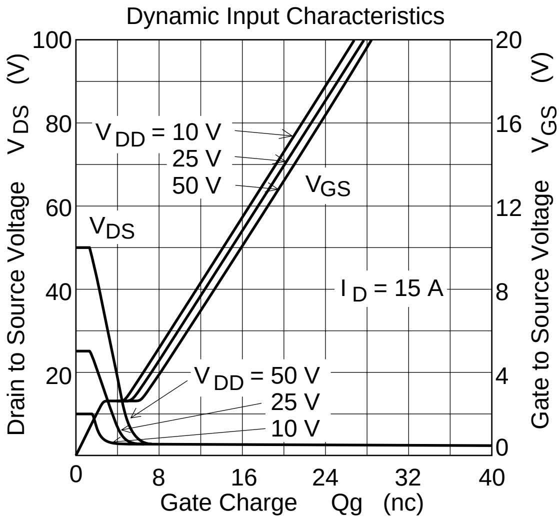

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
VGS = 4 V
10 V
Drain to Source On State Resistance R DS(on) (Ω)
Drain Current I D (A)
1
0.5
0.2
0.1
0.05
0.02
0.01
1
2
5
10
20
50
100

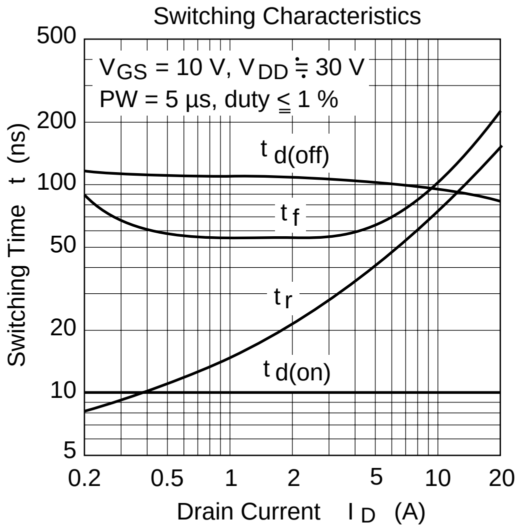

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 15 A
10 A
5 A
VGS = 4 V
5 A, 10 A, 15 A
10 V
Static Drain to Source on State Resistance RDS(on) (Ω)
Case Temperature Tc (°C)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160


Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
75 °C
25 °C
VDS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
20
10
5
2
1
0.5
0.2
0.2
0.5
1
2
5
10
20

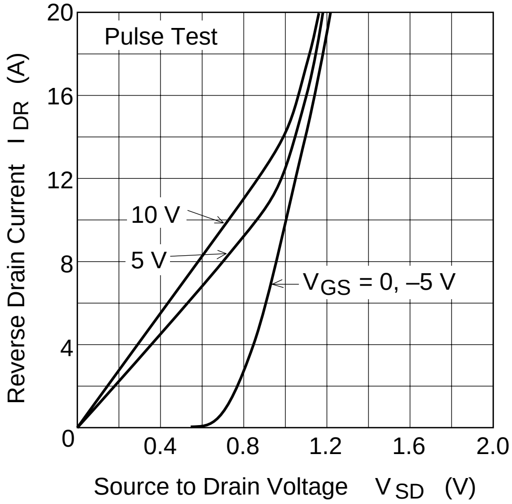

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)
di/dt = 50 A/μs
VGS = 0, Ta = 25°C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
1000
500
200
100
50
20
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

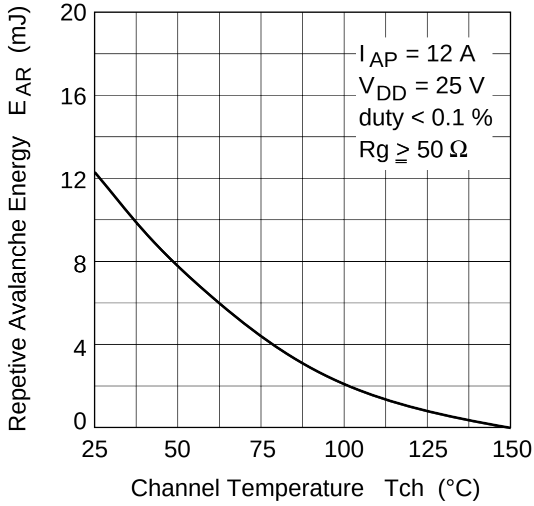

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
100
80
60
40
20
0
VDD = 10 V
25 V
50 V
VGS
VDS
ID = 15 A
VDD = 50 V
25 V
10 V
20
16
12
8
4
0
Gate to Source Voltage VGS (V)
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
VGS = 10 V, VDD ≒ 30 V
PW = 5 μs, duty ≦ 1 %
Switching Time t (ns)
500
200
100
50
20
10
5
td(off)
tf
tr
td(on)
0.2
0.5
1
2
5
10
20
Drain Current ID (A)

Reverse Drain Current vs.
Souece to Drain Voltage

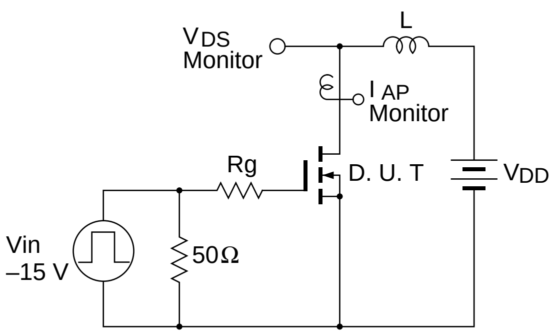


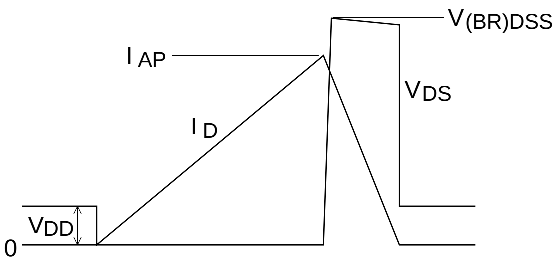
Maximun Avalanche Energy vs.
Channel Temperature Derating

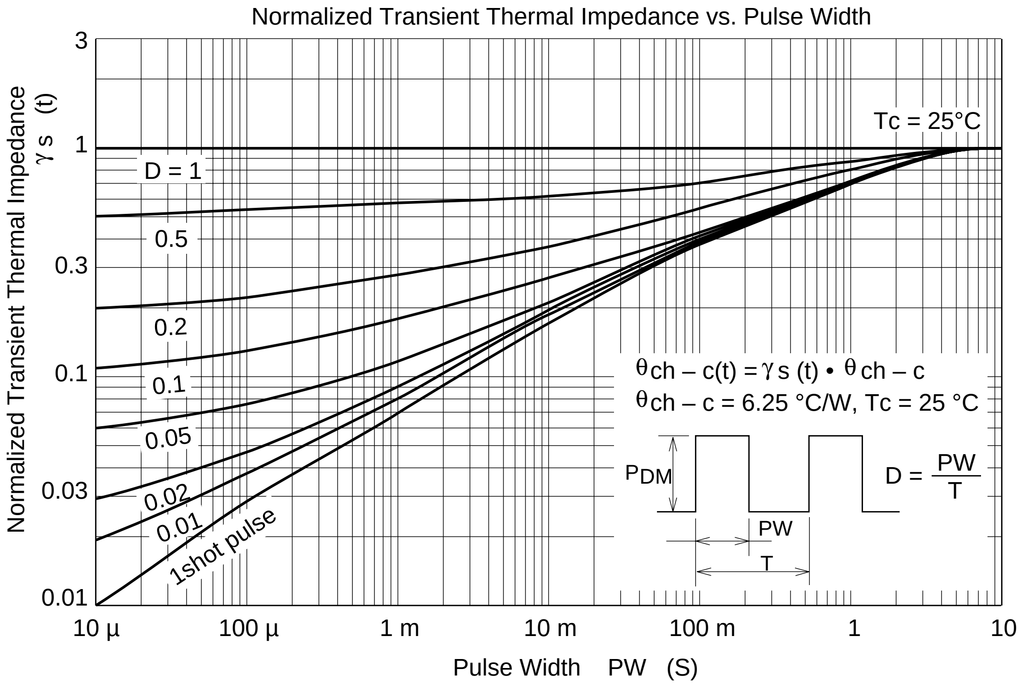


Avalanche Test Circuit and Waveform

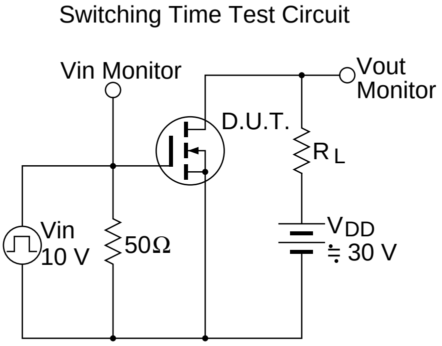
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}{}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



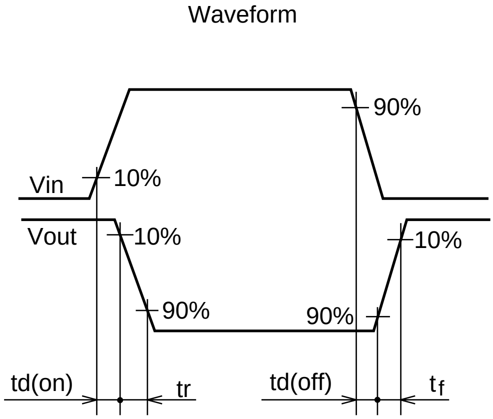




Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance
γs (t)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)



Switching Time Test Circuit
Vin Monitor
Vout
Monitor
D.U.T.
RL
Vin
10 V
50Ω
VDD
≒ 30 V



Waveform
90%
Vin
10%
Vout
10%
90%
90%
10%
td(on)
tr
td(off)
tf

2SK2393

Silicon N Channel MOS FET

Application

High voltage / High speed power switching

Features

- Low on–resistance, High breakdown voltage
- High speed switching
- Low Drive Current
- No Secondary Breakdown
- Suitable for Switching regulator, Motor Control

TO–3PL

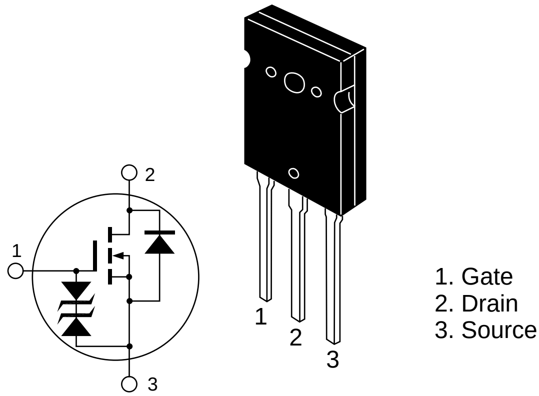


Table 1 Absolute Maximum Ratings (Ta = 25°C)

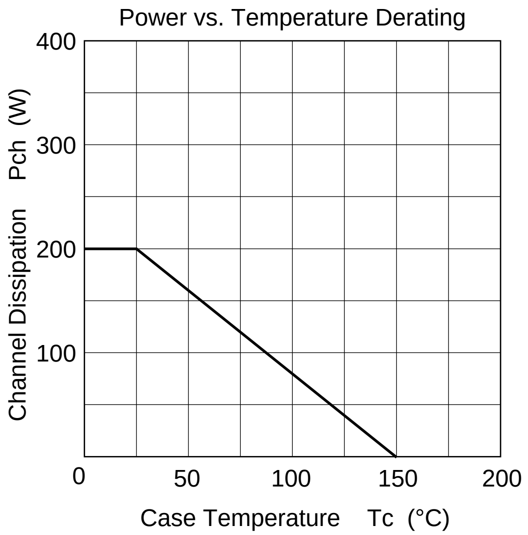
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1500	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}^*$	20	A
Body–drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	Pch**	200	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

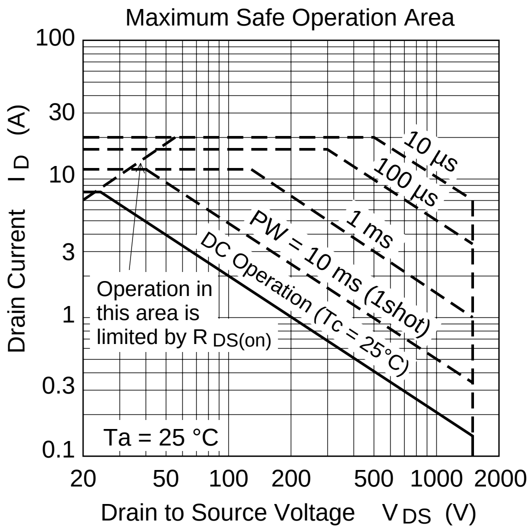
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

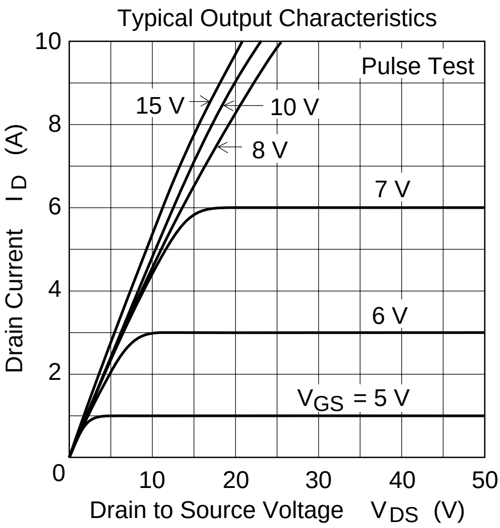
Table 2 Electrical Characteristics (Ta = 25°C)

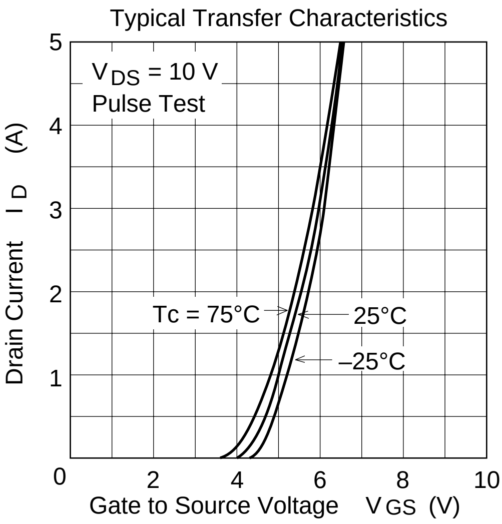
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1500	—	—	V	I_D = 10 mA, V_{GS} = 0*
Gate to source leak current	I_{GSS}	—	—	±1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	500	µA	V_{DS} = 1200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	1.9	2.8	Ω	I_D = 4 A V_{GS} = 15 V *
Forward transfer admittance	$\|y_{fs}\|$	1.8	3.0	—	S	I_D = 4 A V_{DS} = 20 V *
Input capacitance	Ciss	—	4370	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	560	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	200	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	75	—	ns	I_D = 4 A
Rise time	t_r	—	180	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	260	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	125	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	6.5	—	µs	I_F = 8 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

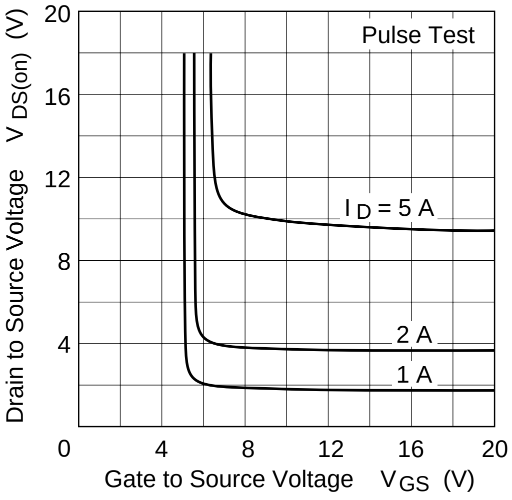

Power vs. Temperature Derating
Channel Dissipation Pch (W)
400
300
200
100
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
100
30
10
3
1
0.3
0.1
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
20
50
100
200
500
1000
2000
Drain to Source Voltage V DS (V)

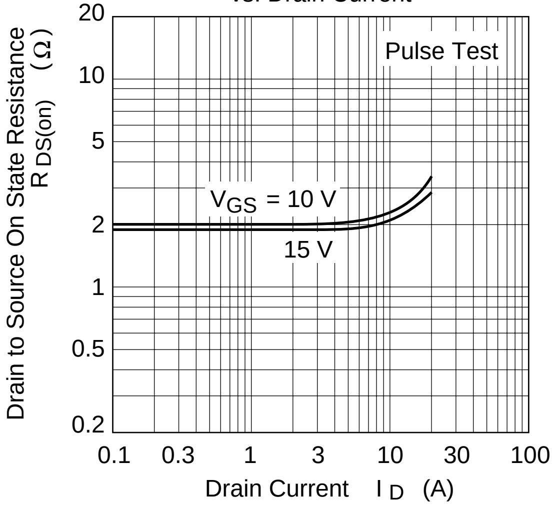

Typical Output Characteristics
Drain Current I D (A)
10
8
6
4
2
0
Pulse Test
15 V
10 V
8 V
7 V
6 V
VGS = 5 V
10
20
30
40
50
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
Drain Current I D (A)
5
4
3
2
1
0
V DS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
2
4
6
8
10
Gate to Source Voltage V GS (V)

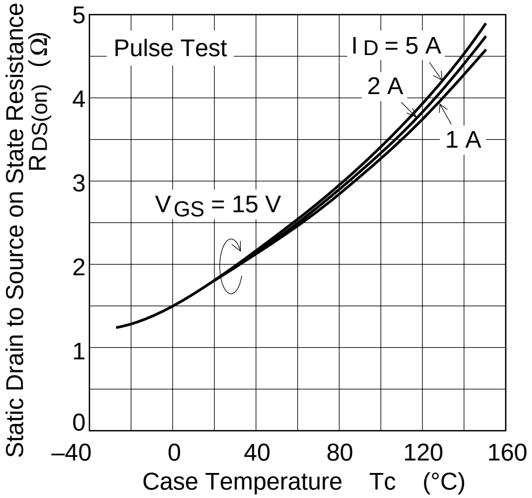
Drain to Source Saturation Voltage vs. Gate to Source Voltage



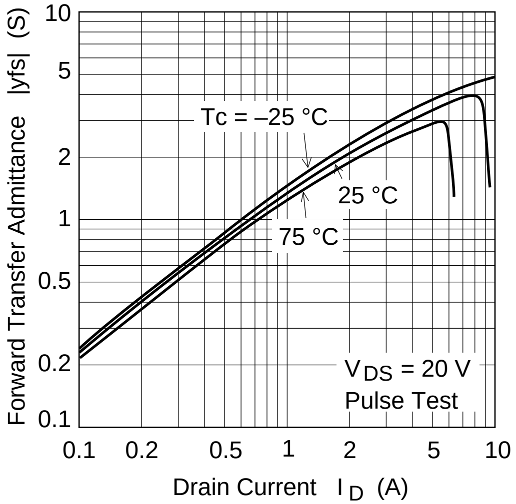
Static Drain to Source on State Resistance vs. Drain Current



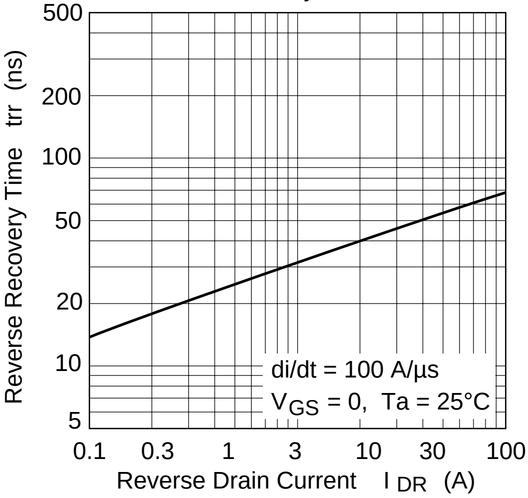
Static Drain to Source on State Resistance vs. Temperature



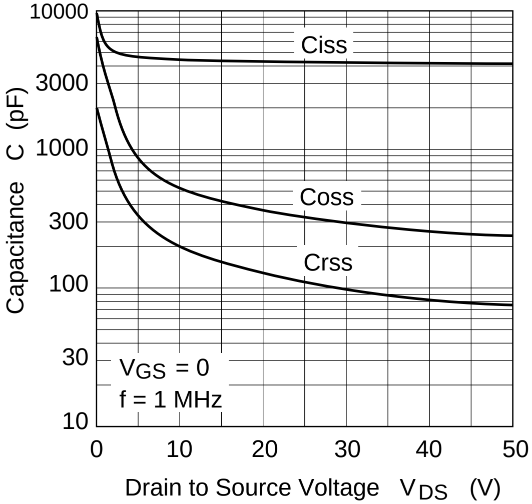
Forward Transfer Admittance vs. Drain Current



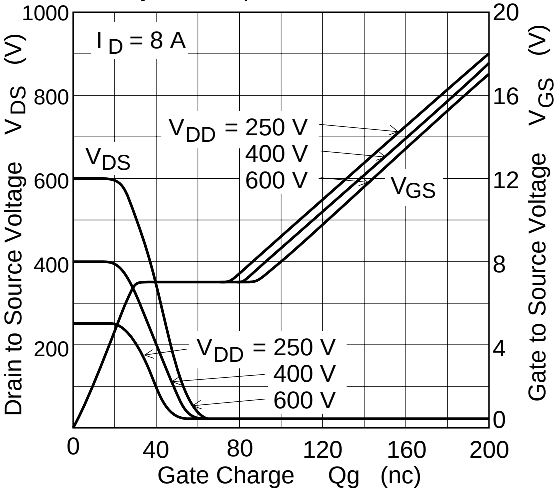
Body–Drain Diode Reverse Recovery Time



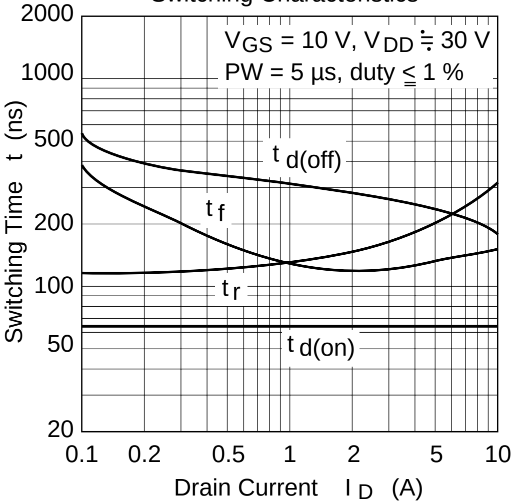
Typical Capacitance vs. Drain to Source Voltage

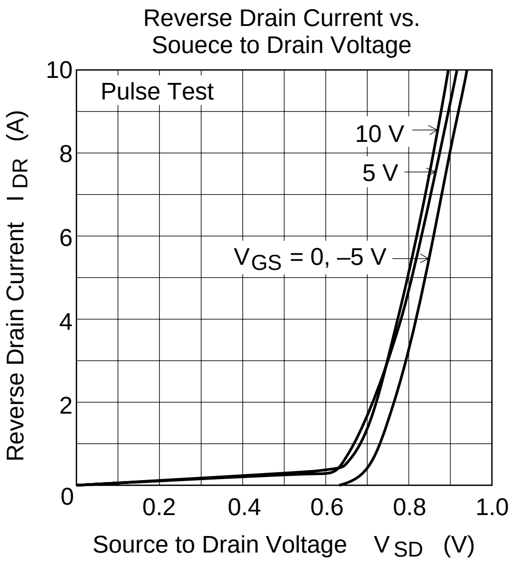


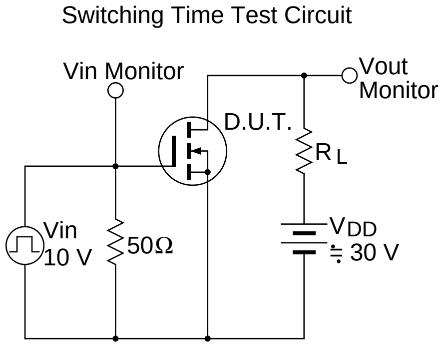
Dynamic Input Characteristics

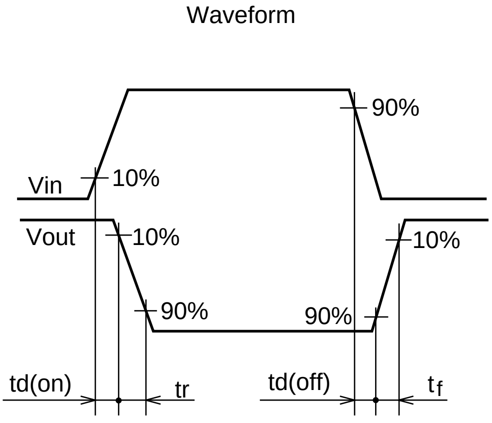


Switching Characteristics




Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
Reverse Drain Current I DR (A)
0
2
4
6
8
10
0.2
0.4
0.6
0.8
1.0
Source to Drain Voltage V SD (V)


Switching Time Test Circuit
Vin Monitor
Vout
Monitor
D.U.T.
R L
Vin
10 V
50Ω
VDD
≒ 30 V


Waveform
90%
Vin
10%
Vout
10%
90%
90%
10%
td(on)
tr
td(off)
tf

2SK2408

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- Built-in fast recovery diode (t_{rr} = 120 ns typ)
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, Motor control

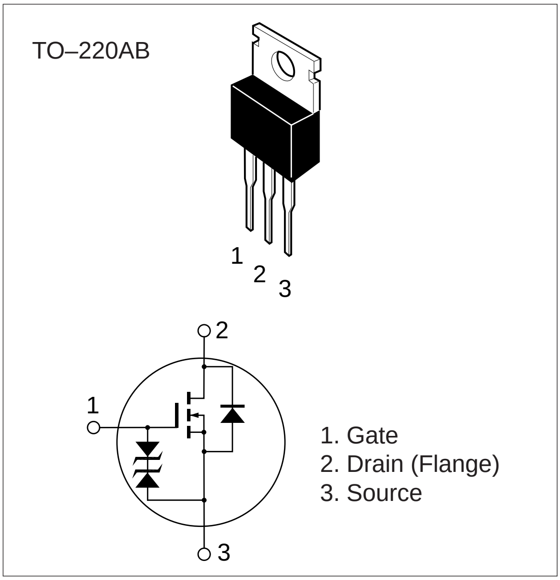


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	21	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

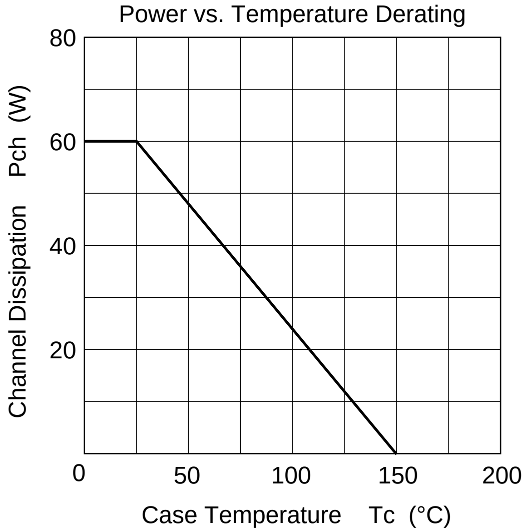
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

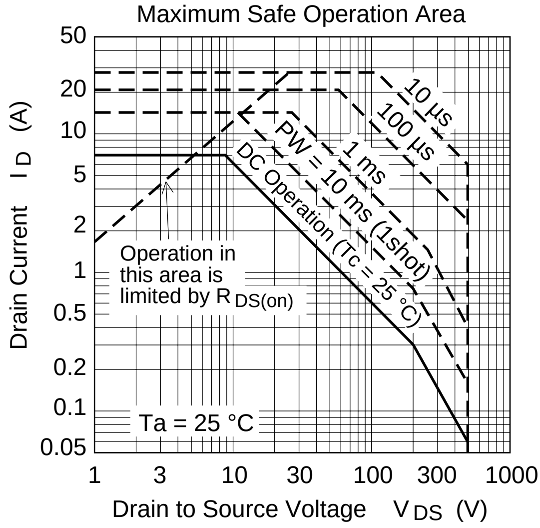
Table 2 Electrical Characteristics (Ta = 25°C)

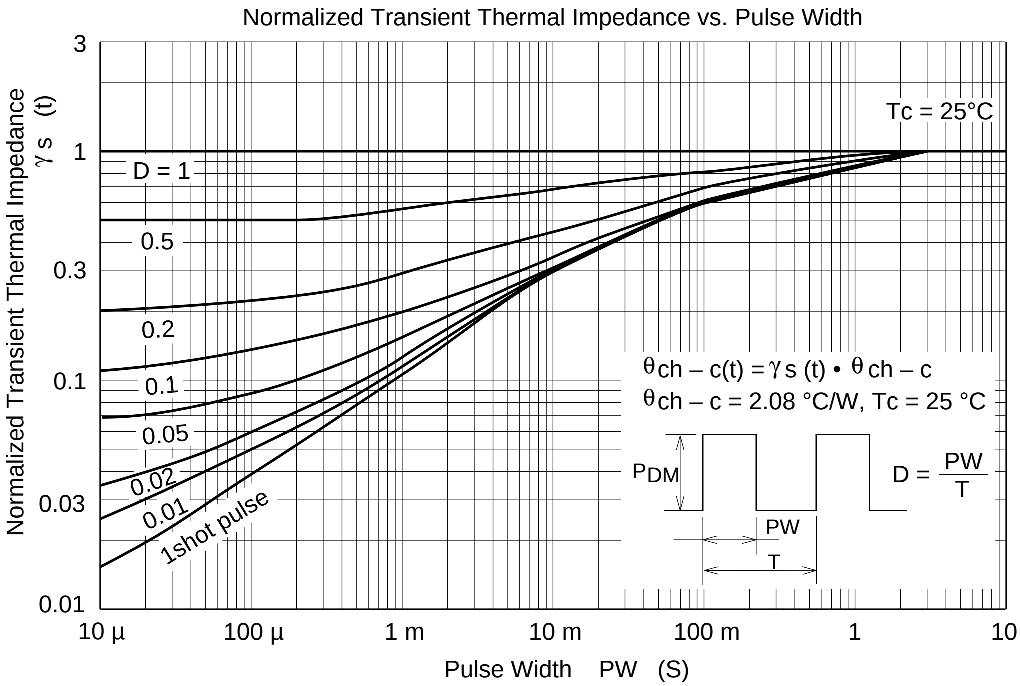
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.9	Ω	I_D = 4A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	6.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1100	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	310	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	50	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	48	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 7 A, V_{GS} = 0, di_F / dt = 100 A / μs

* Pulse Test

See characteristic curves of 2SK1516


Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
1
3
10
30
100
300
1000
Drain to Source Voltage V DS (V)
10 µs
100 µs
PW = 1 ms
10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C

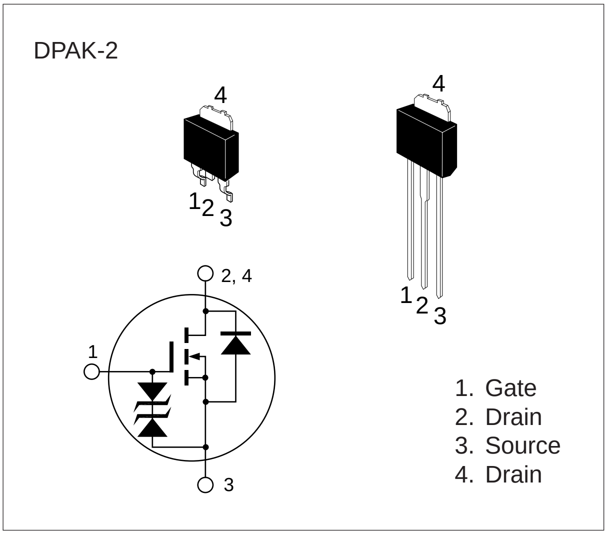

Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 2.08 °C/W, Tc = 25 °C
PDM
D = PW/T
PW
T

2SK2418(L), 2SK2418(S)

Silicon N Channel MOS FET

Application

High speed power switching



Features

- Low on–resistance
- High speed switching
- Low drive current
- 2.5 V gate drive device can be driven from 3 V source
- Suitable for Switching regulator, DC – DC converter

Table 1 Absolute Maximum Ratings (Ta = 25°C)

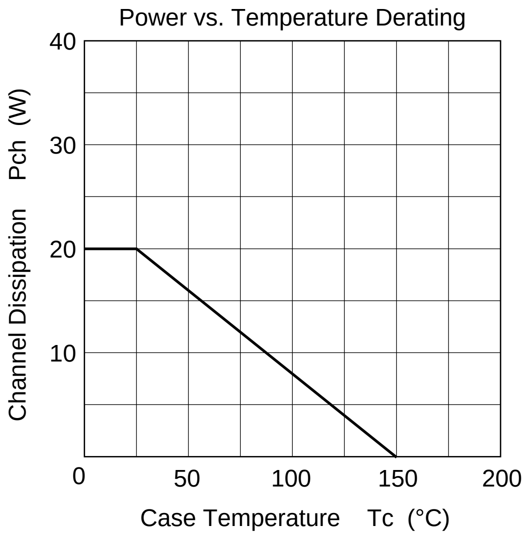
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

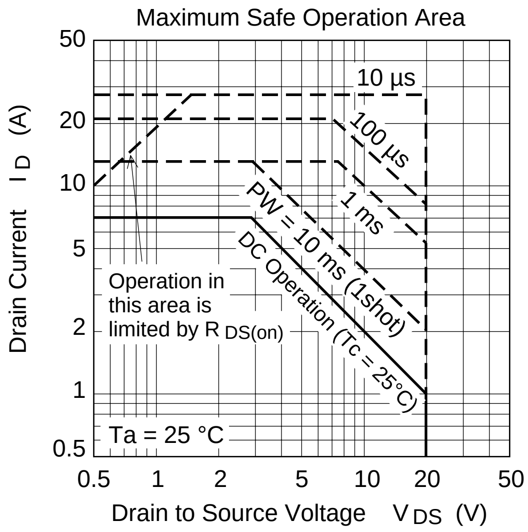
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

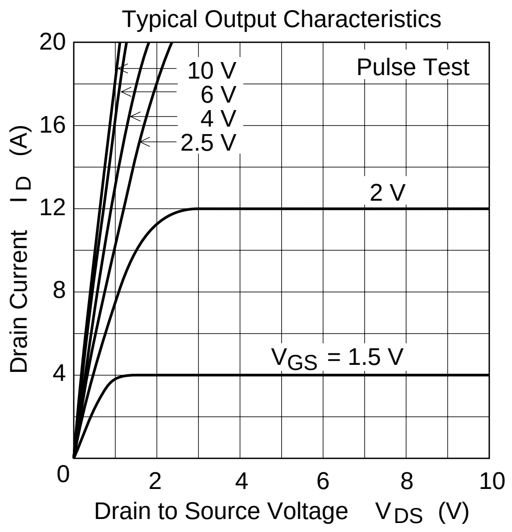
Table 2 Electrical Characteristics (Ta = 25°C)

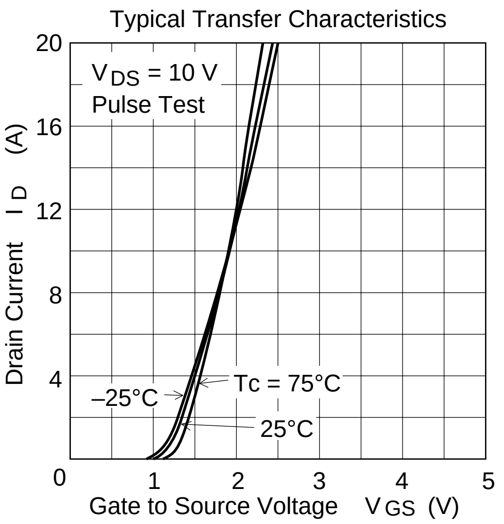
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 16 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.04	0.05	Ω	I_D = 4 A V_{GS} = 4 V *
		—	0.05	0.07	Ω	I_D = 4 A V_{GS} = 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	810	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	600	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	155	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 4 A
Rise time	t_r	—	90	—	ns	V_{GS} = 4 V
Turn–off delay time	$t_{d(off)}$	—	150	—	ns	R_L = 2.5 Ω
Fall time	t_f	—	120	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 20 A / µs

* Pulse Test

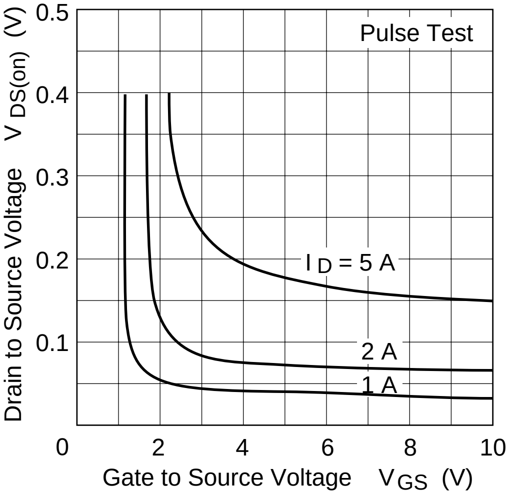

Power vs. Temperature Derating
Channel Dissipation Pch (W)
40
30
20
10
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.5
1
2
5
10
20
50
Drain to Source Voltage V DS (V)

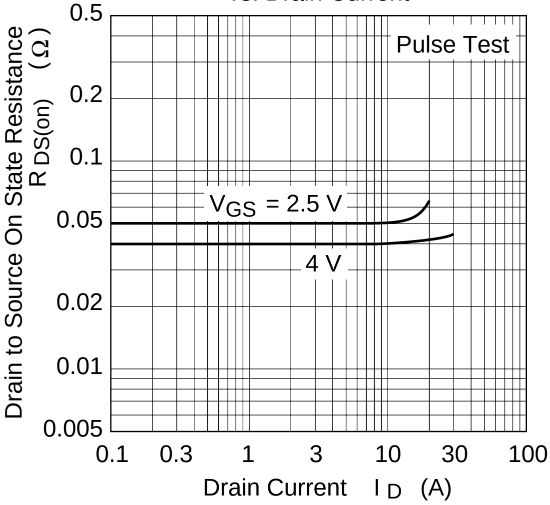

Typical Output Characteristics
Drain Current I D (A)
20
16
12
8
4
0
10 V
6 V
4 V
2.5 V
Pulse Test
2 V
VGS = 1.5 V
2
4
6
8
10
Drain to Source Voltage VDS (V)


Typical Transfer Characteristics
Drain Current I D (A)
20
16
12
8
4
0
VDS = 10 V
Pulse Test
Tc = 75°C
–25°C
25°C
1
2
3
4
5
Gate to Source Voltage V GS (V)

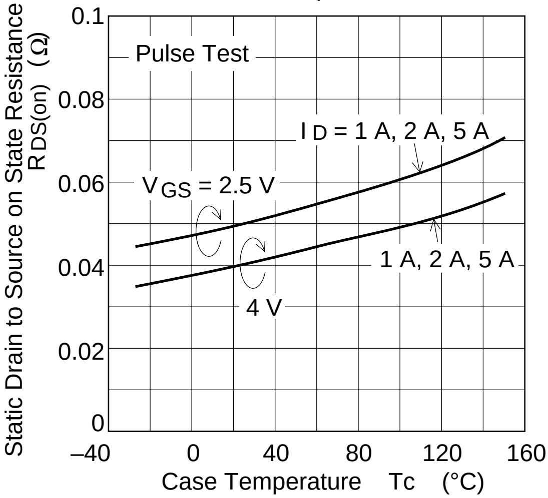
Drain to Source Saturation Voltage vs. Gate to Source Voltage



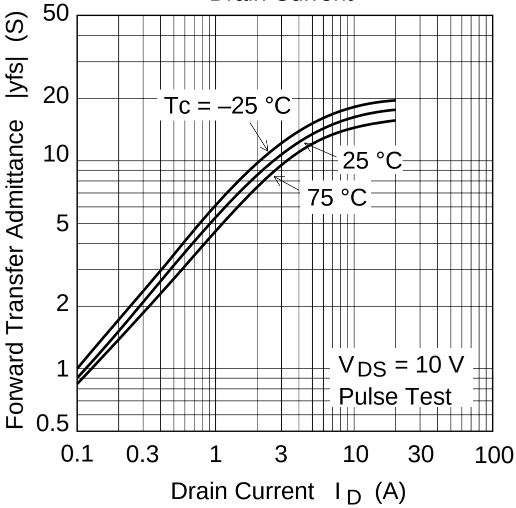
Static Drain to Source on State Resistance vs. Drain Current

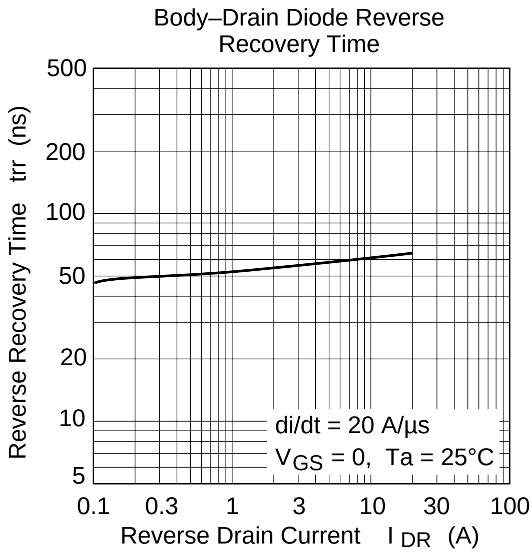


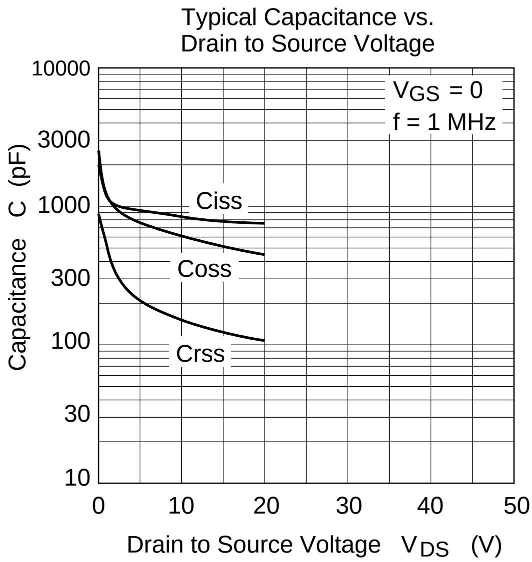
Static Drain to Source on State Resistance vs. Temperature

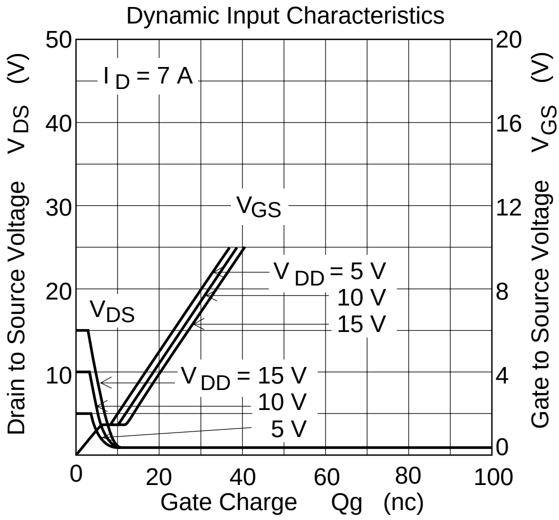


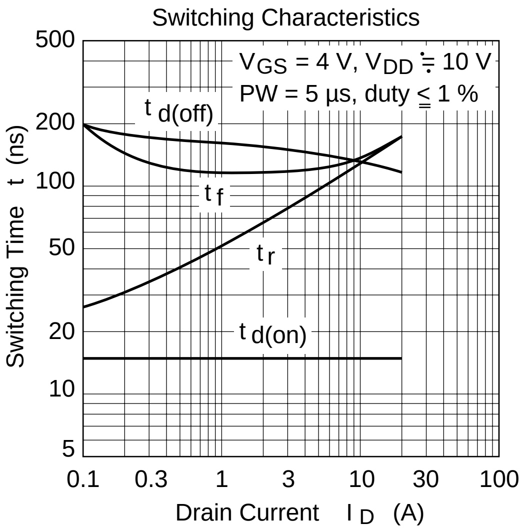
Forward Transfer Admittance vs. Drain Current

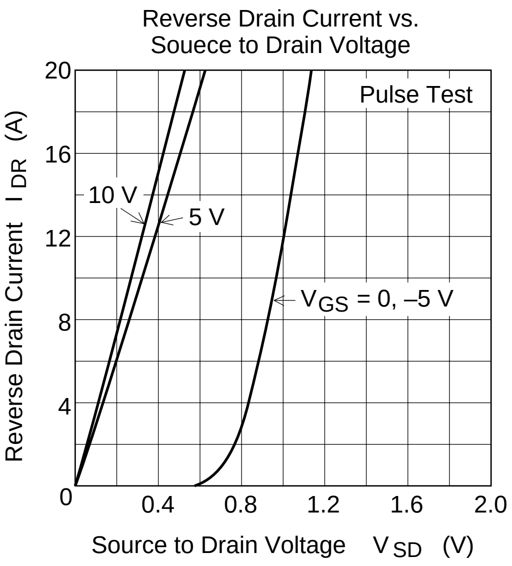


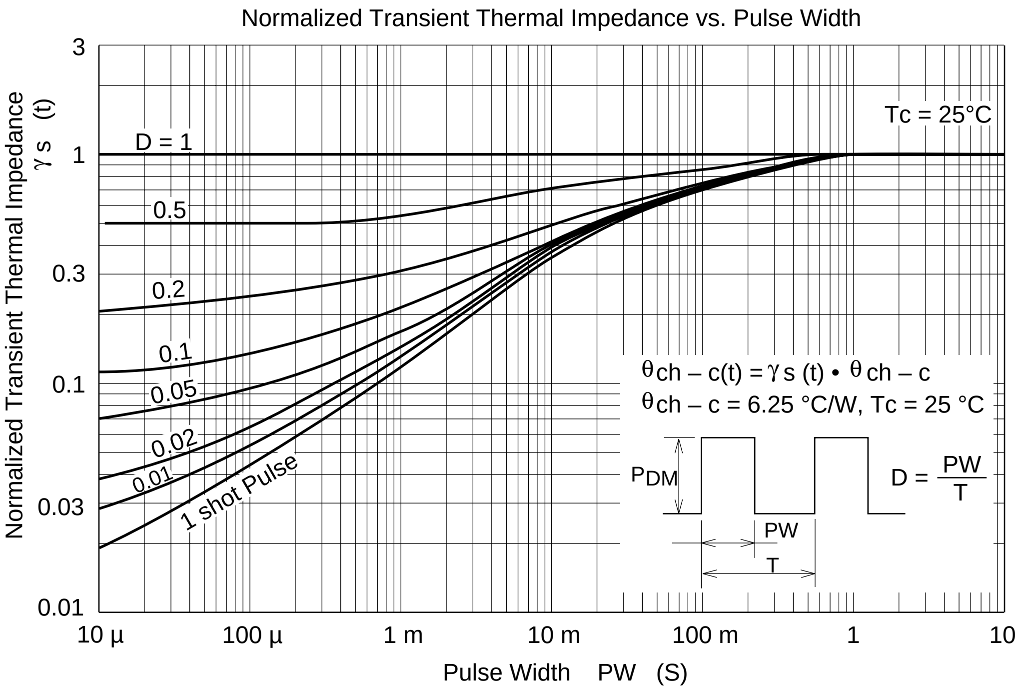

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
di/dt = 20 A/µs
VGS = 0, Ta = 25°C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage VDS (V)
VGS = 0
f = 1 MHz
Ciss
Coss
Crss

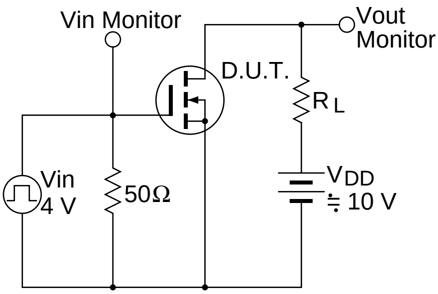

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
I D = 7 A
VGS
VDS
V DD = 5 V
10 V
15 V
V DD = 15 V
10 V
5 V


Switching Characteristics
Switching Time t (ns)
Drain Current I D (A)
VGS = 4 V, VDD ≒ 10 V
PW = 5 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)

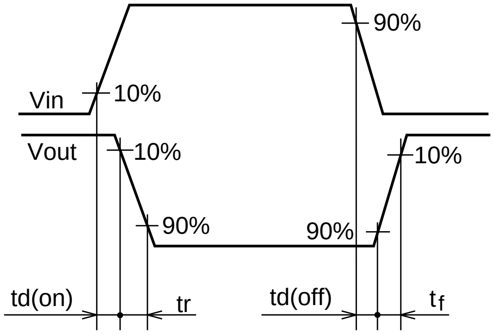

Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
20
16
12
8
4
0
0.4
0.8
1.2
1.6
2.0
Reverse Drain Current I DR (A)
Source to Drain Voltage V SD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot Pulse
θch – c(t) = γs (t) • θch – c
θch – c = 6.25 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)

Switching Time Test Circuit



Waveform



2SK2423

Silicon N Channel MOS FET

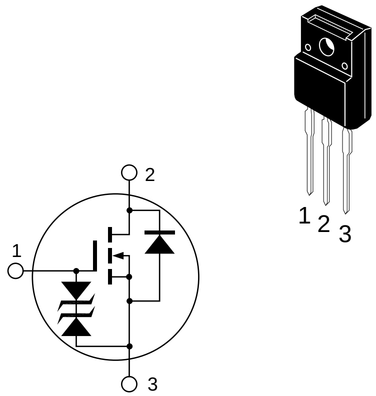
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter.

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	450	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =450 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.55	0.7	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	4.5	7.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1150	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	340	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	55	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	17	—	ns	I_D = 4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 7.5Ω
Fall time	t_f	—	45	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	330	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristics curves of 2SK1159.

2SK2424

Silicon N Channel MOS FET

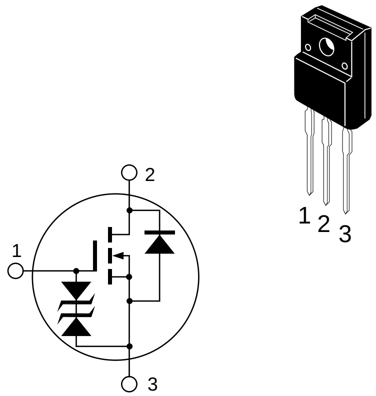
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	450	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}$*	32	A
Body–drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =450 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.4	0.55	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	7.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	410	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	55	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	130	—	ns	R_L = 7.5Ω
Fall time	t_f	—	50	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	380	—	ns	I_F = 8 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristics curves of 2SK1165.

2SK2425

Silicon N Channel MOS FET

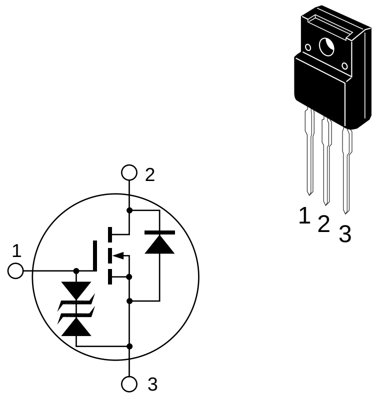
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =250 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.4	0.55	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	690	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	265	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	13	—	ns	I_D = 4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	65	—	ns	R_L = 7.5Ω
Fall time	t_f	—	37	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	180	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristics curve of 2SK1667, 2SK1668.

2SK2426

Silicon N Channel MOS FET

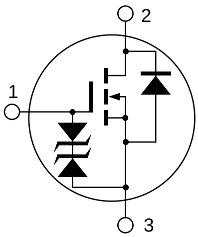
Application

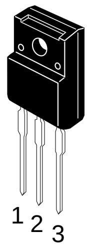
High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–220CFM





1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	12	A
Drain peak current	$I_{D(pulse)}$*	48	A
Body–drain diode reverse drain current	I_{DR}	12	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =250 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.23	0.35	Ω	I_D = 6 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	8.0	—	S	I_D = 6 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1100	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	68	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 6 A
Rise time	t_r	—	65	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 5Ω
Fall time	t_f	—	44	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 12 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = 12 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristics curve of 2SK1761, 2SK1762.

2SK2431

Silicon N Channel MOS FET

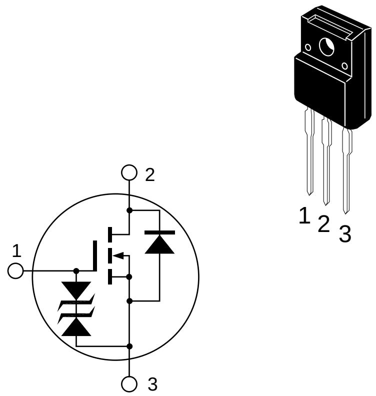
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	450	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$*	12	A
Body–drain diode reverse drain current	I_{DR}	3	A
Channel dissipation	Pch**	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =450 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	2.0	2.8	Ω	I_D = 2 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.5	2.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	330	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	90	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	15	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	7	—	ns	I_D = 2 A
Rise time	t_r	—	20	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	30	—	ns	R_L = 15Ω
Fall time	t_f	—	20	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 3 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	300	—	ns	I_F = 3 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristics curve of 2SK1153, 2SK1862.

2SK2529
Silicon N Channel MOS FET

HITACHI

6th. Edition
Jun. 1995

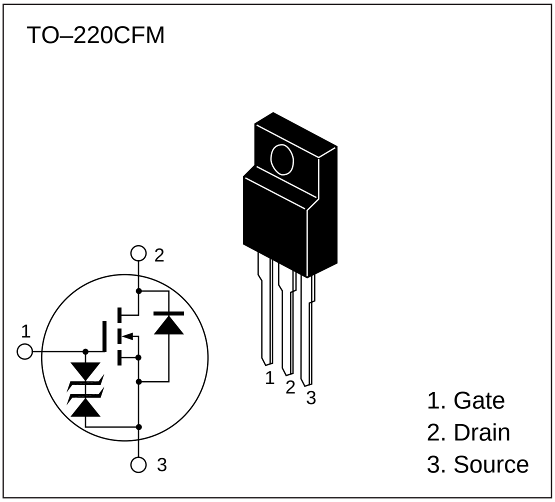
Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)}$ = 7 mΩ typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V souece

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$*	200	A
Body–drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP}***	45	A
Avalanche energy	E_{AR}***	174	mJ
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C
*** Value at Tch = 25°C, Rg ≥ 50 Ω

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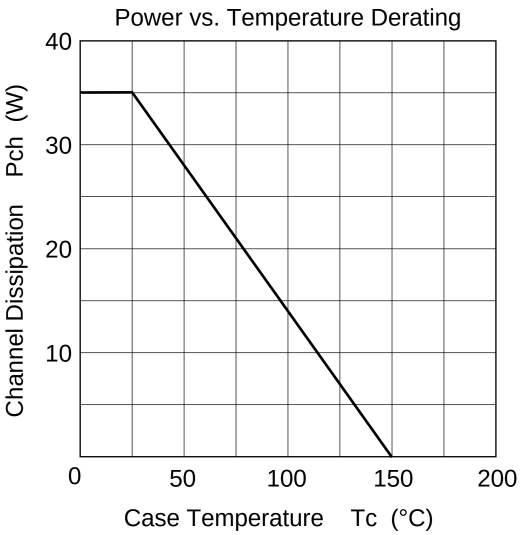
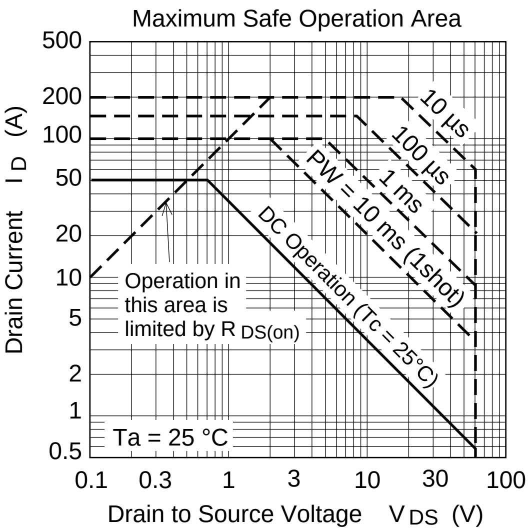
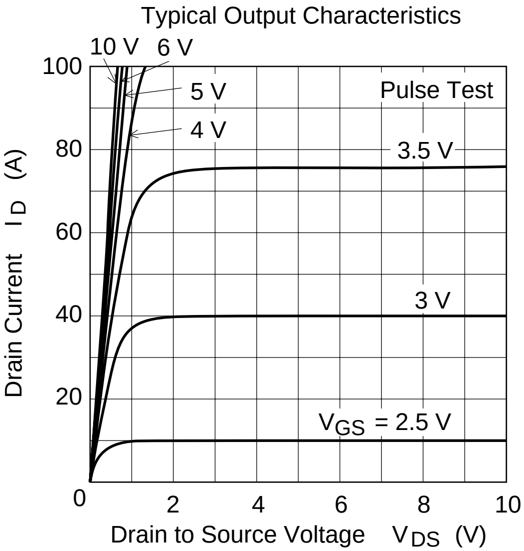
Table 2 Electrical Characteristics (Ta = 25°C)

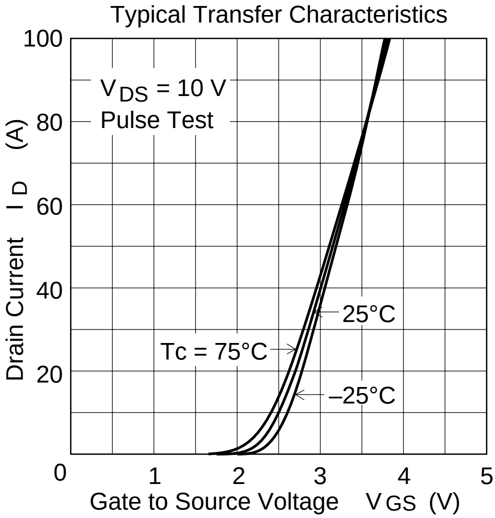
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	7	10	mΩ	I_D = 25 A V_{GS} = 10 V *
		—	10	16	mΩ	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	35	55	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3550	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1760	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	500	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	35	—	ns	I_D = 25 A
Rise time	t_r	—	230	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	470	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	360	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.85	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	145	—	ns	I_F = 50 A, V_{GS} = 0 diF / dt = 50 A / µs

* Pulse Test

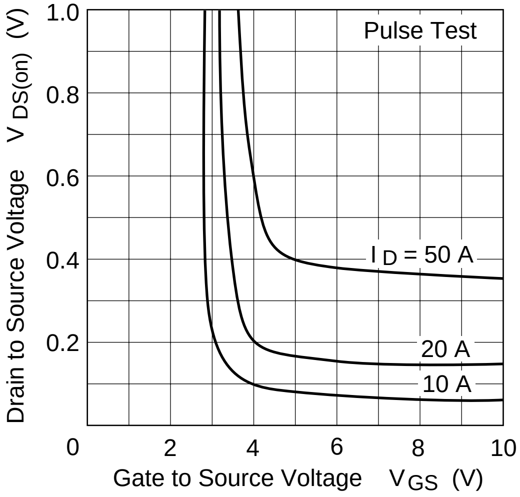

Power vs. Temperature Derating
40
30
20
10
0
50
100
150
200
Channel Dissipation Pch (W)
Case Temperature Tc (°C)


Maximum Safe Operation Area
500
200
100
50
20
10
5
2
1
0.5
0.1
0.3
1
3
10
30
100
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
Drain Current I D (A)
Drain to Source Voltage V DS (V)

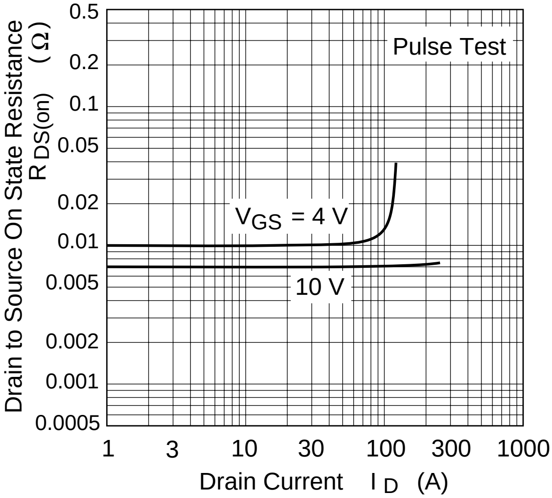

Typical Output Characteristics
10 V
6 V
5 V
4 V
Pulse Test
3.5 V
3 V
VGS = 2.5 V
100
80
60
40
20
0
2
4
6
8
10
Drain Current I D (A)
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
VDS = 10 V
Pulse Test
25°C
Tc = 75°C
–25°C
100
80
60
40
20
0
1
2
3
4
5
Drain Current I D (A)
Gate to Source Voltage V GS (V)

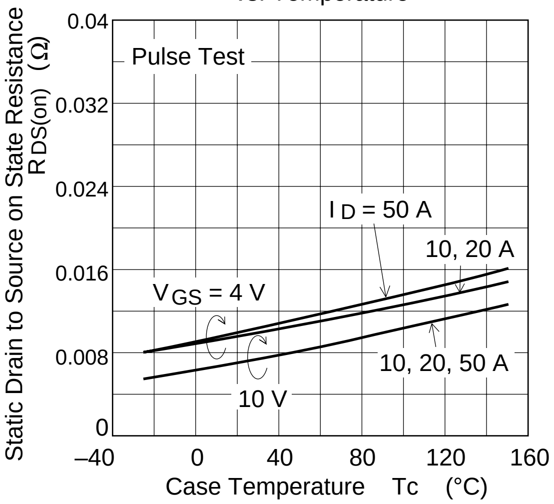
Drain to Source Saturation Voltage vs. Gate to Source Voltage



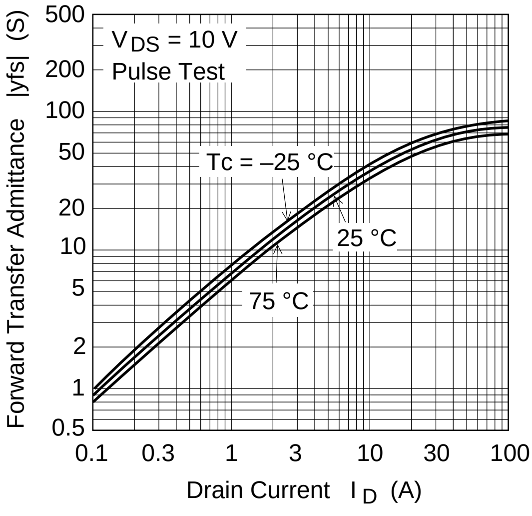
Static Drain to Source on State Resistance vs. Drain Current

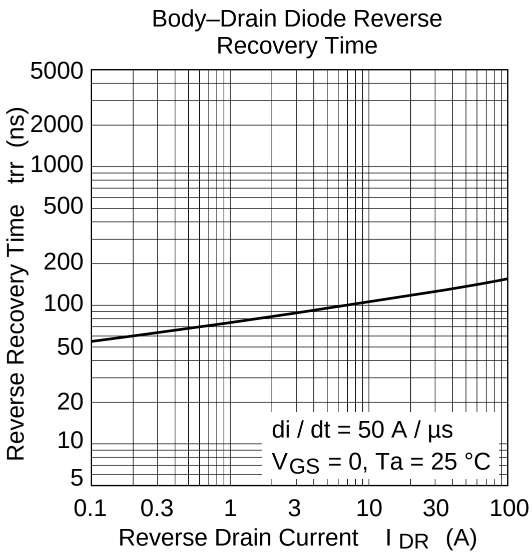


Static Drain to Source on State Resistance vs. Temperature

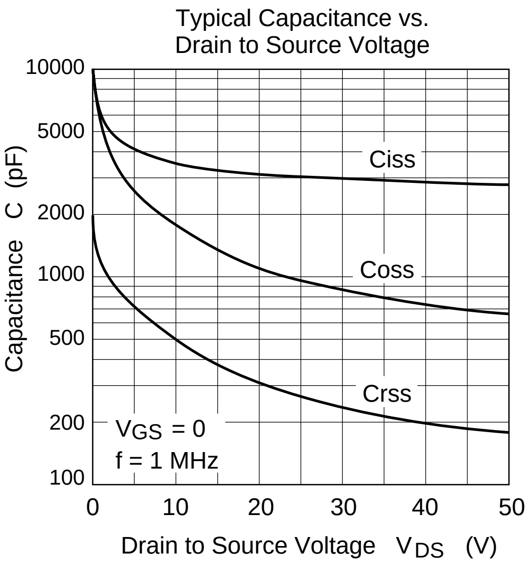


Forward Transfer Admittance vs. Drain Current

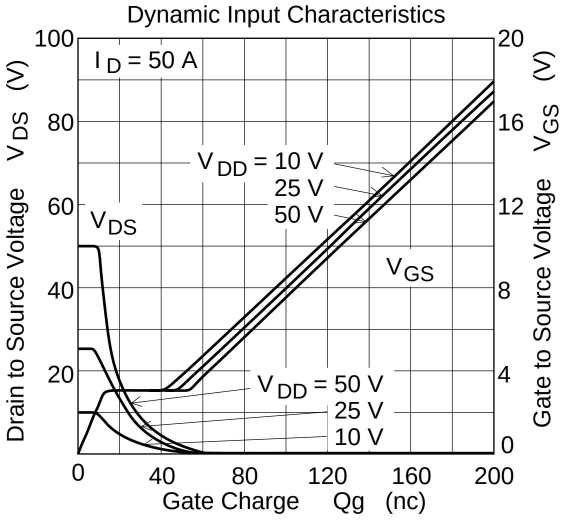




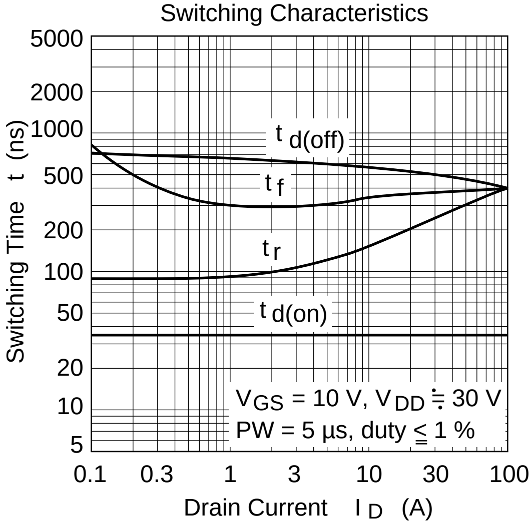
Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C



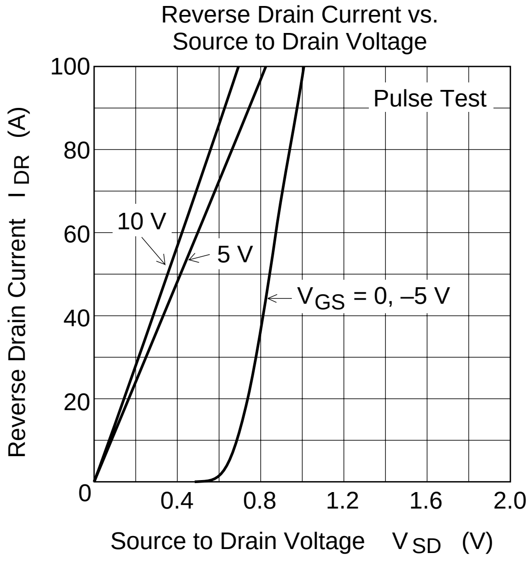
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

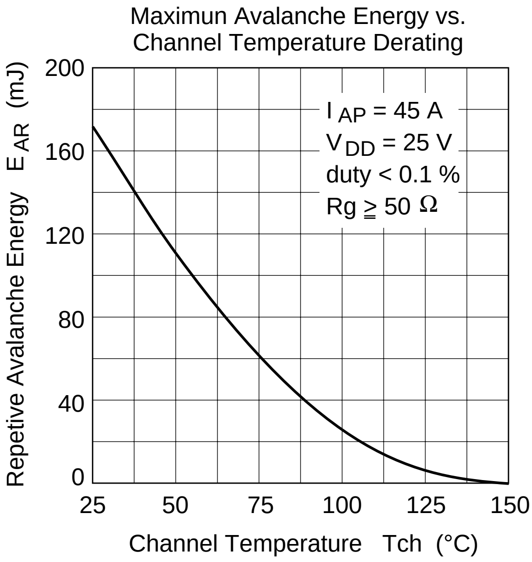


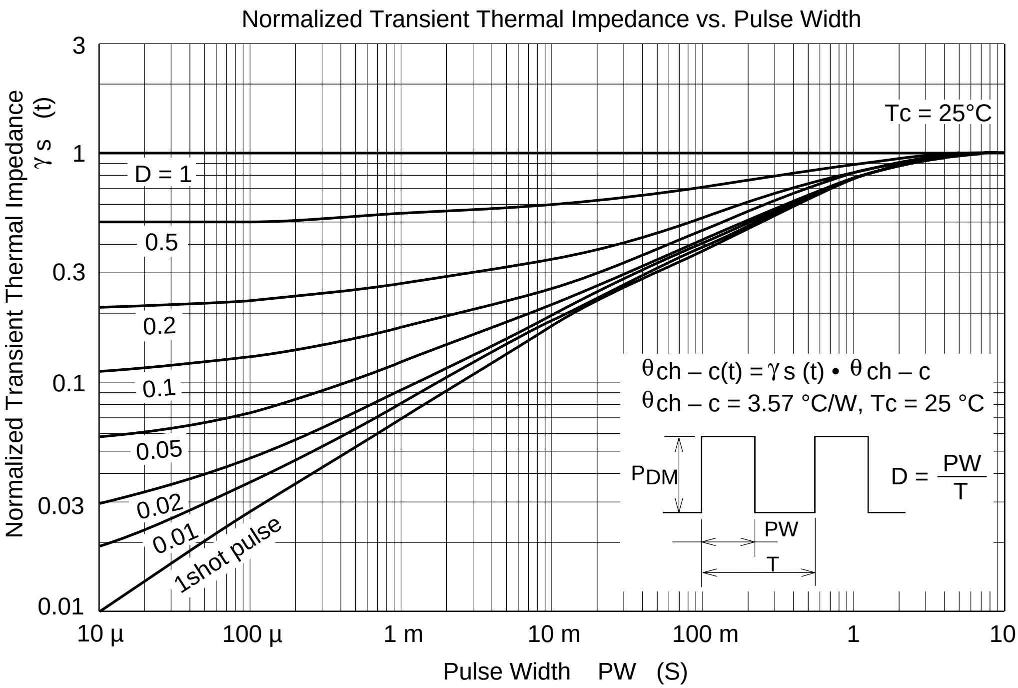
Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
I D = 50 A
VDD = 10 V
25 V
50 V
VDS
VGS
VDD = 50 V
25 V
10 V



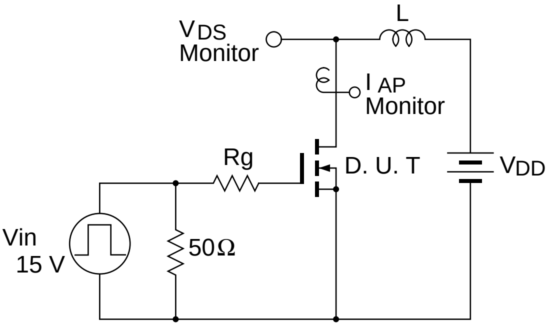
Switching Characteristics
Switching Time t (ns)
Drain Current I D (A)
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
10 V
5 V
VGS = 0, –5 V
Reverse Drain Current IDR (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage VSD (V)

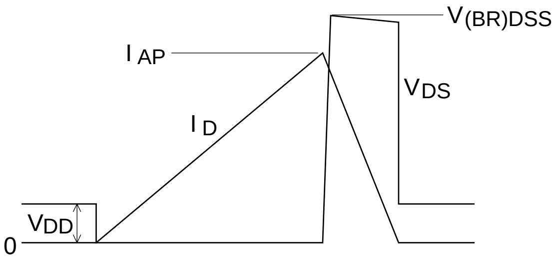

Maximun Avalanche Energy vs.
Channel Temperature Derating
I AP = 45 A
VDD = 25 V
duty < 0.1 %
Rg ≧ 50 Ω
Repetive Avalanche Energy EAR (mJ)
200
160
120
80
40
0
25
50
75
100
125
150
Channel Temperature Tch (°C)


Normalized Transient Thermal Impedance vs. Pulse Width
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 3.57 °C/W, Tc = 25 °C
PDM
PW
T
D = PW / T
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

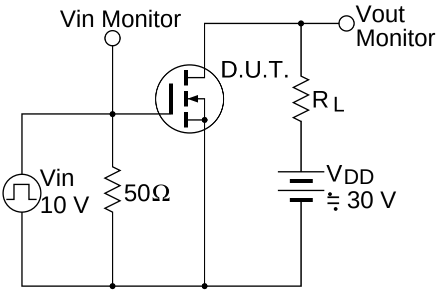
Avalanche Test Circuit and Waveform



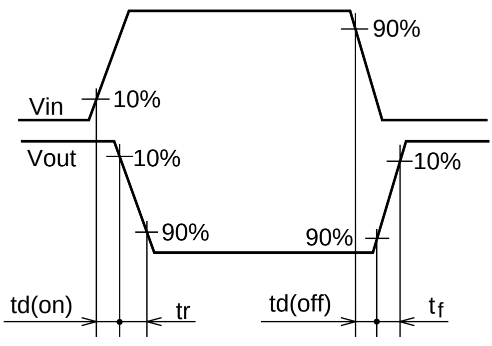
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



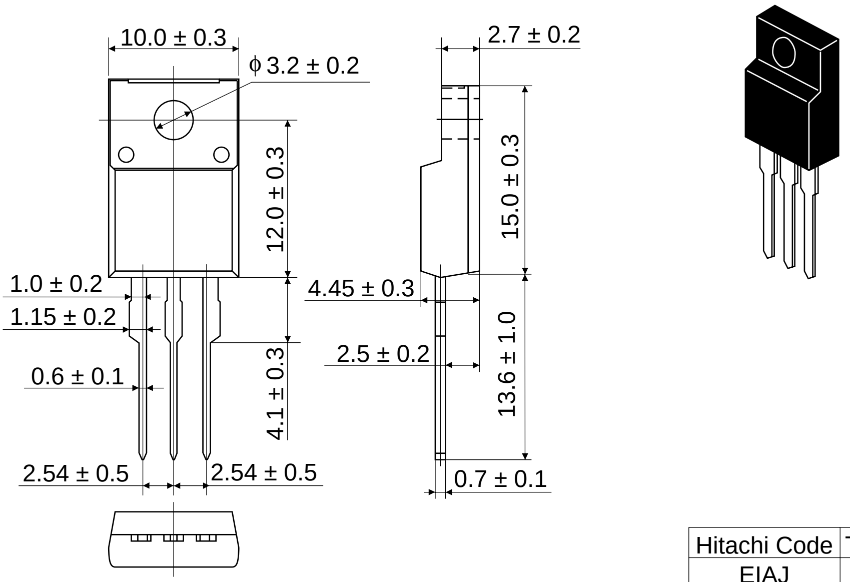
Waveform



Package Dimensions

Unit : mm

• TO–220CFM



Hitachi Code	TO–220CFM
EIAJ	—
JEDEC	—

2SK2553

Silicon N Channel MOS FET

HITACHI

7th. Edition
Jun. 1995

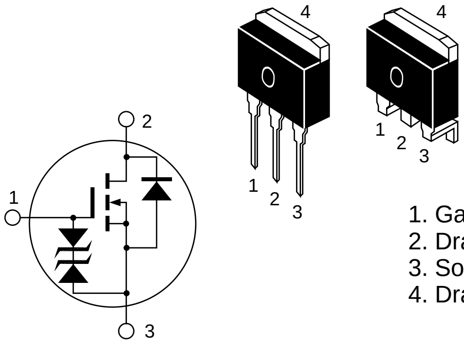
Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)}$ = 7 mΩ typ.
- High speed switching
- 4 V gate drive device can be driven from
  5 V souece

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$*	200	A
Body–drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP}***	45	A
Avalanche energy	E_{AR}***	174	mJ
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25°C
*** Value at Tch = 25°C, Rg ≥ 50 Ω

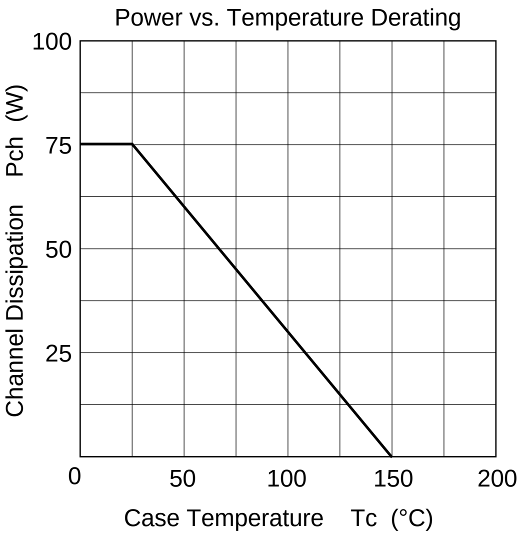
Hitachi semiconductor

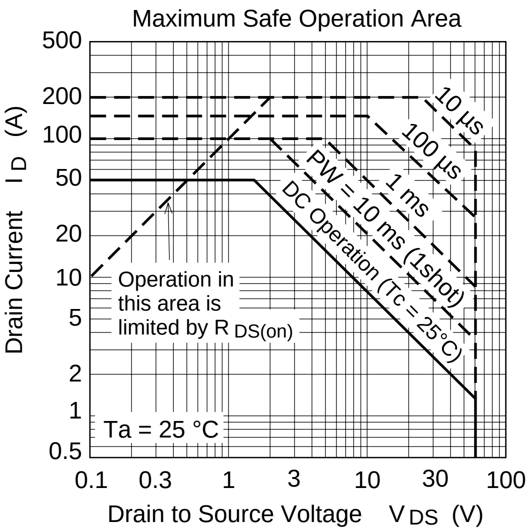
Table 2 Electrical Characteristics (Ta = 25°C)

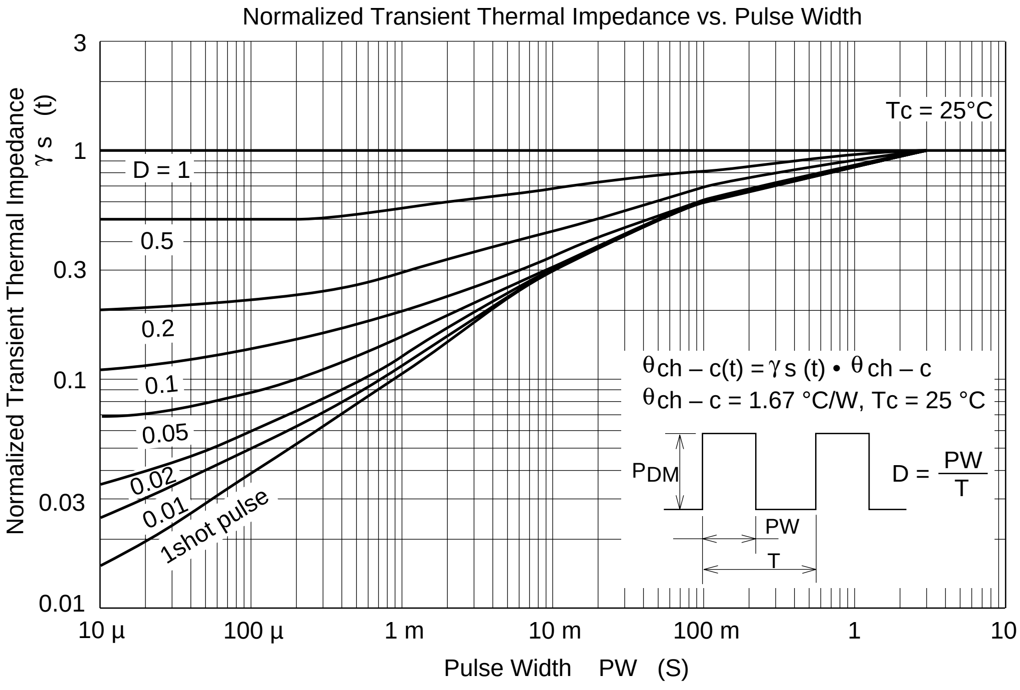
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	7	10	mΩ	I_D = 25 A V_{GS} = 10 V *
		—	10	16	mΩ	I_D = 25 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	35	55	—	S	I_D = 25 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3550	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1760	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	500	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	35	—	ns	I_D = 25 A
Rise time	t_r	—	230	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	470	—	ns	RL = 1.2 Ω
Fall time	t_f	—	360	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 50 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 50 A, V_{GS} = 0 diF / dt = 50 A / µs

* Pulse Test

■ See characteristic curves of 2SK2529.

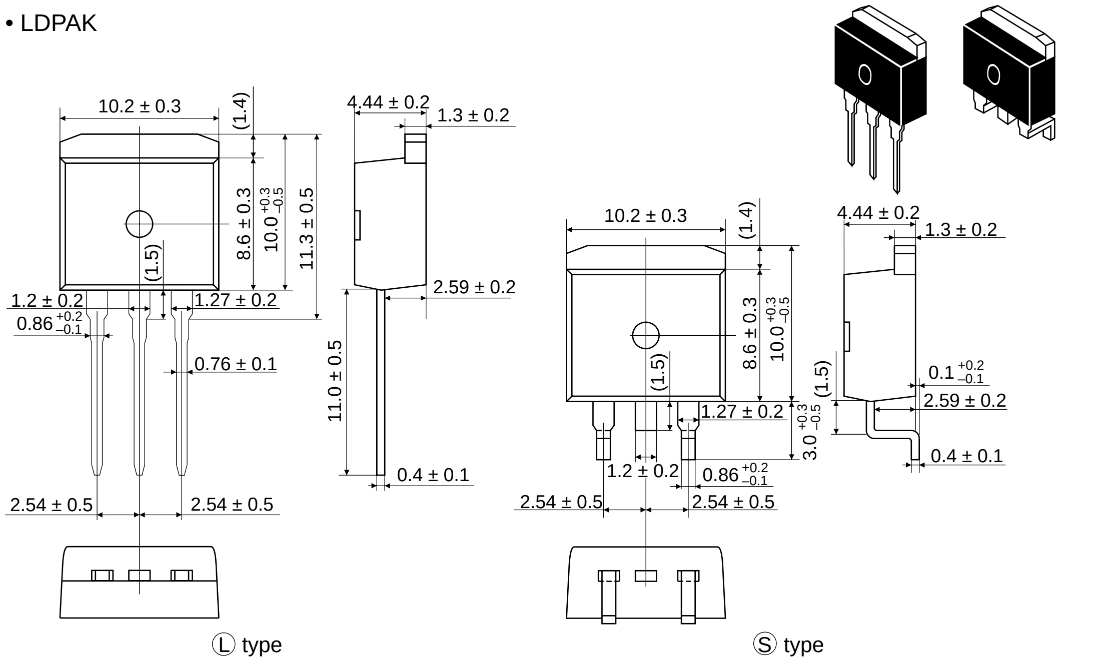

Power vs. Temperature Derating
Channel Dissipation Pch (W)
100
75
50
25
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ s (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γ s (t) • θ ch – c
θch – c = 1.67 °C/W, Tc = 25 °C
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Package Dimensions

Unit : mm



Hitachi Code	LDPAK
EIAJ	—
JEDEC	—

2SK2554
Silicon N Channel MOS FET

HITACHI

4th. Edition
Feb. 1995
Target Spec.

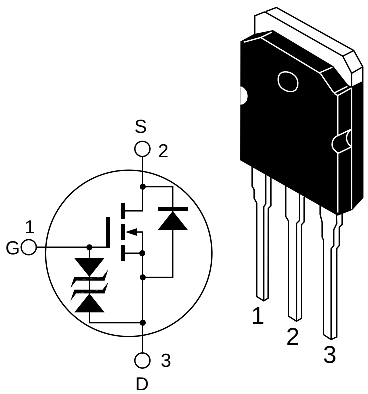
Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)}$ = 4.5 mΩ typ.
- High speed switching
- 4 V gate drive device can be driven from
  5 V souece

TO–3P



1. Gate
2. Drain
   (Flange)
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

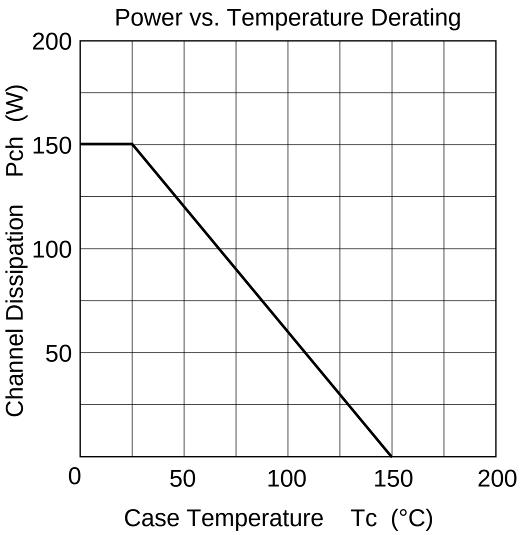
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D**	75	A
Drain peak current	$I_{D(pulse)}$*	300	A
Body–drain diode reverse drain current	I_{DR}**	75	A
Avalanche current	I_{AP}***	50	A
Avalanche energy	E_{AR}***	214	mJ
Channel dissipation	Pch**	150	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

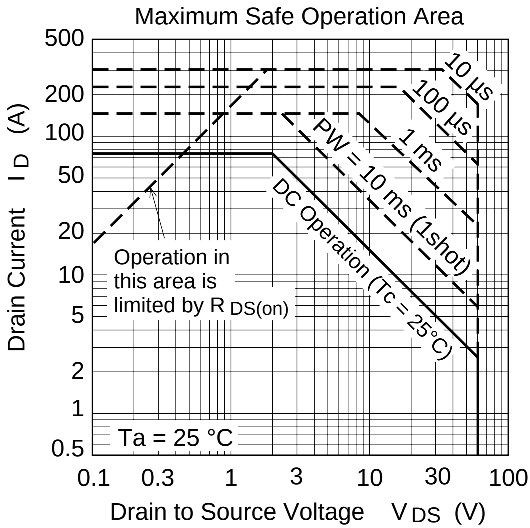
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25°C
*** Value at Tch = 25°C, Rg ≥ 50 Ω

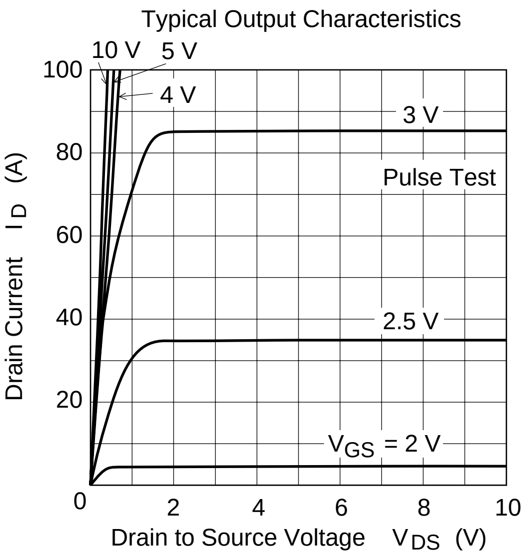
Table 2 Electrical Characteristics (Ta = 25°C)

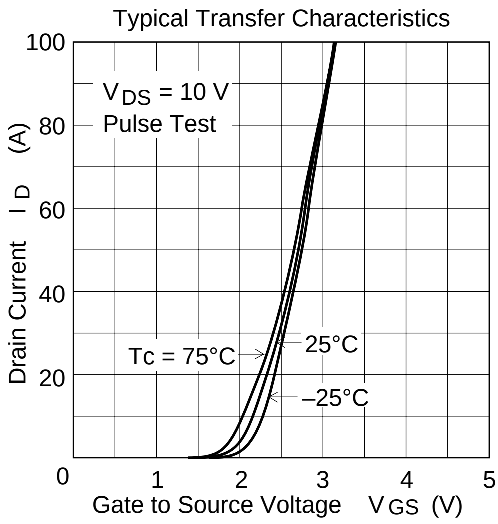
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	4.5	6	mΩ	I_D = 40 A V_{GS} = 10 V *
		—	5.8	10	mΩ	I_D = 40 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	50	80	—	S	I_D = 40 A V_{DS} = 10 V *
Input capacitance	Ciss	—	7700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	4100	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	760	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	60	—	ns	I_D = 40 A
Rise time	t_r	—	420	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	1200	—	ns	RL = 0.75 Ω
Fall time	t_f	—	900	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 75 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	105	—	ns	I_F = 75 A, V_{GS} = 0 diF / dt = 50 A / µs

* Pulse Test

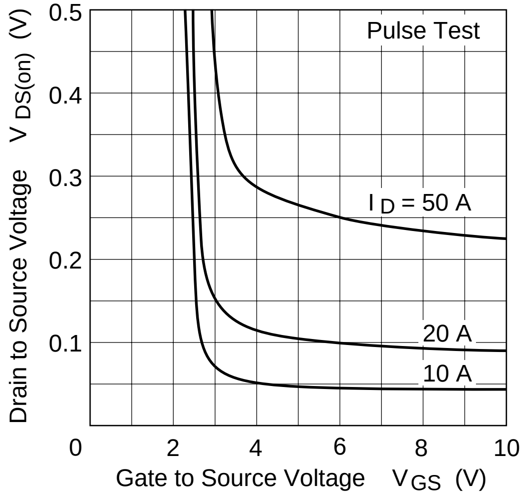

Power vs. Temperature Derating
Channel Dissipation Pch (W)
200
150
100
50
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
10 µs
100 µs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

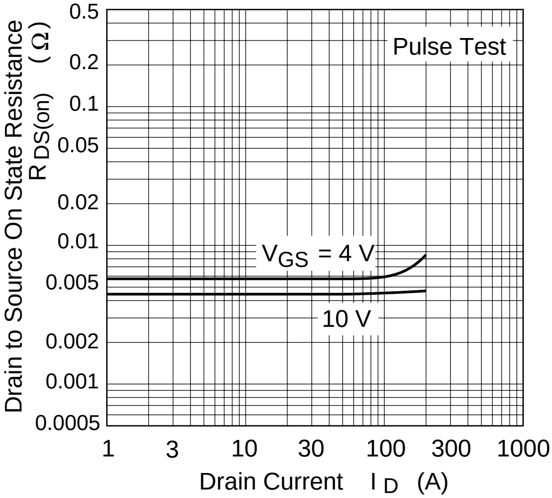

Typical Output Characteristics
10 V
5 V
4 V
3 V
Pulse Test
2.5 V
V GS = 2 V
Drain Current I D (A)
100
80
60
40
20
0
2
4
6
8
10
Drain to Source Voltage V DS (V)


Typical Transfer Characteristics
V DS = 10 V
Pulse Test
Drain Current I D (A)
100
80
60
40
20
0
Tc = 75°C
25°C
–25°C
1
2
3
4
5
Gate to Source Voltage V GS (V)

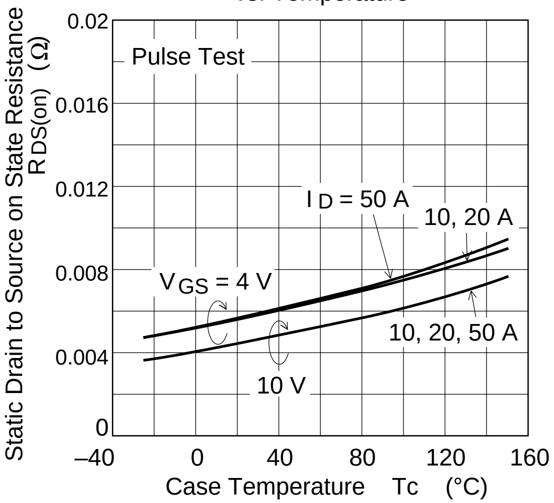
Drain to Source Saturation Voltage vs. Gate to Source Voltage



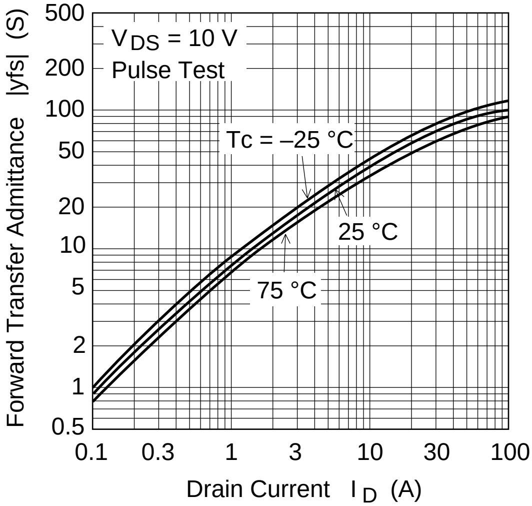
Static Drain to Source on State Resistance vs. Drain Current

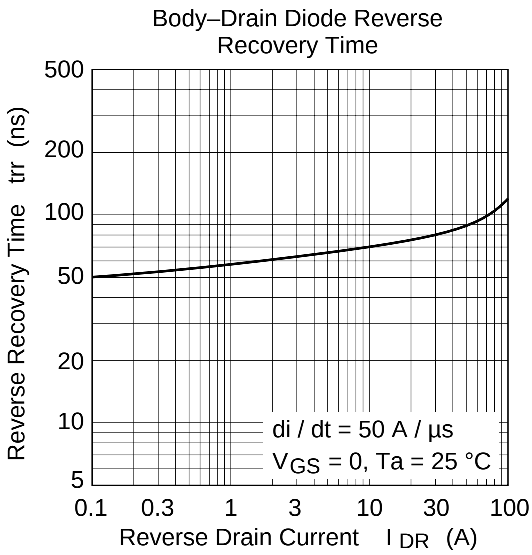


Static Drain to Source on State Resistance vs. Temperature

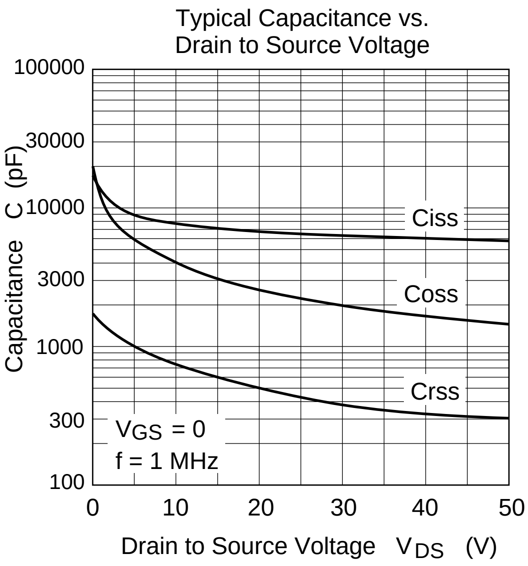


Forward Transfer Admittance vs. Drain Current

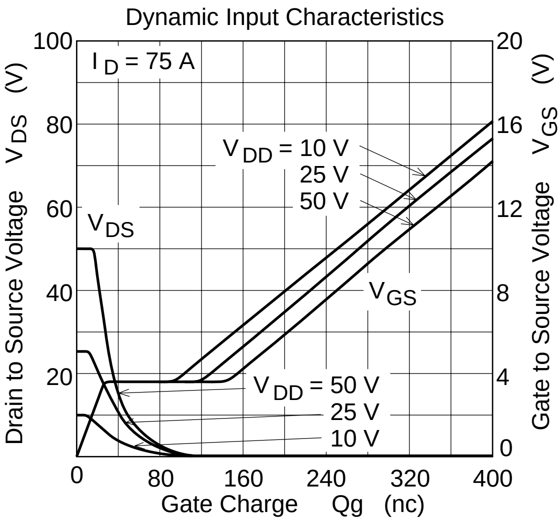




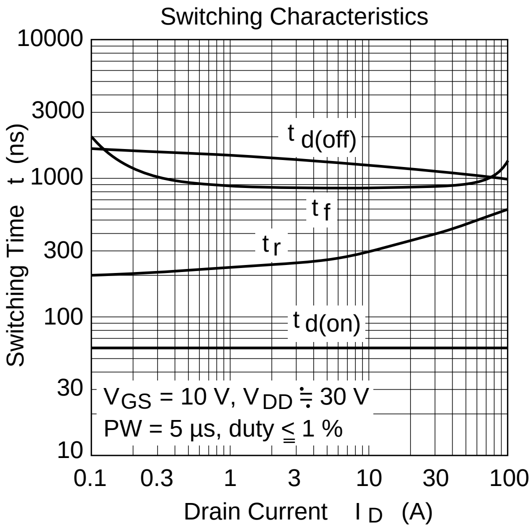
Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)



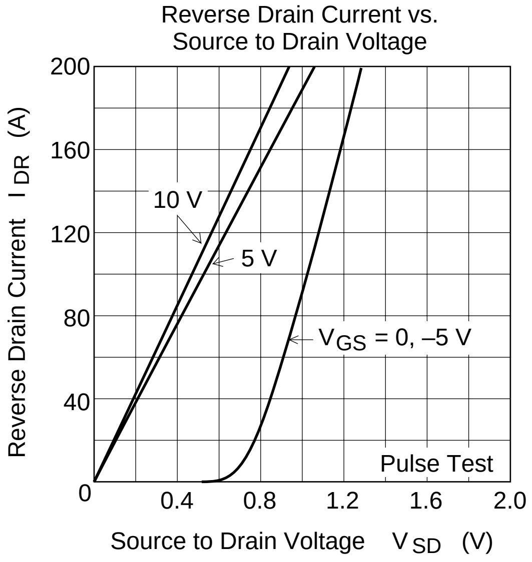
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
100000
30000
10000
3000
1000
300
100
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

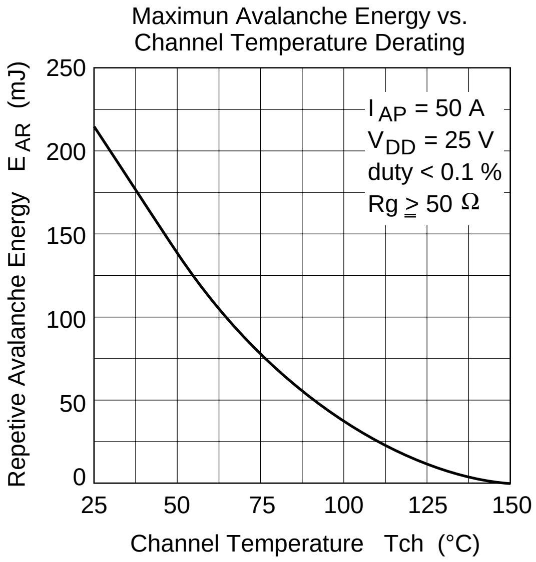


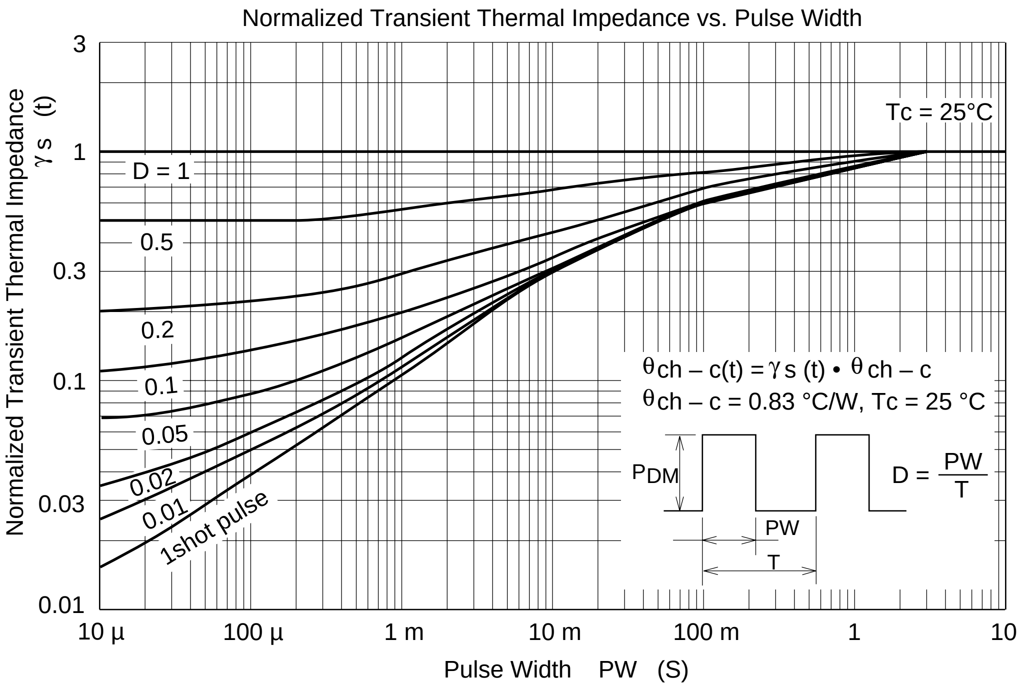
Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
I D = 75 A
VDD = 10 V
25 V
50 V
VDS
VGS
VDD = 50 V
25 V
10 V
100
80
60
40
20
0
20
16
12
8
4
0
80
160
240
320
400
Gate Charge Qg (nc)



Switching Characteristics
Switching Time t (ns)
10000
3000
1000
300
100
30
10
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
0.1
0.3
1
3
10
30
100
Drain Current I D (A)

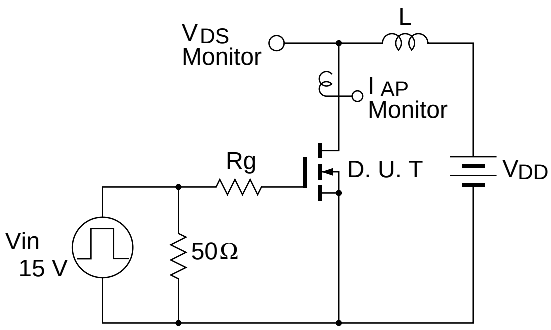

Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
200
160
120
80
40
0
0.4
0.8
1.2
1.6
2.0
10 V
5 V
V GS = 0, –5 V
Pulse Test
Source to Drain Voltage V SD (V)

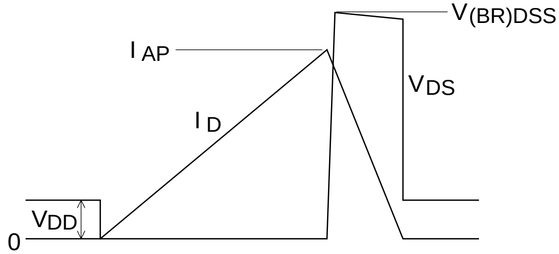

Maximun Avalanche Energy vs.
Channel Temperature Derating
Repetive Avalanche Energy E AR (mJ)
250
200
150
100
50
0
25
50
75
100
125
150
I AP = 50 A
V DD = 25 V
duty < 0.1 %
Rg ≧ 50 Ω
Channel Temperature Tch (°C)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ s (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θ ch – c(t) = γ s (t) • θ ch – c
θ ch – c = 0.83 °C/W, Tc = 25 °C
P DM
PW
T
D = PW / T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

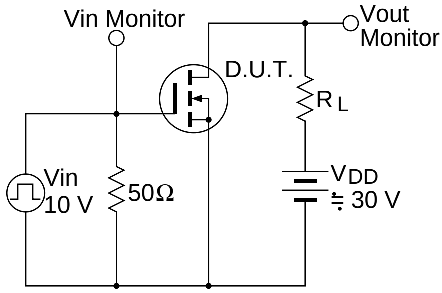
Avalanche Test Circuit and Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

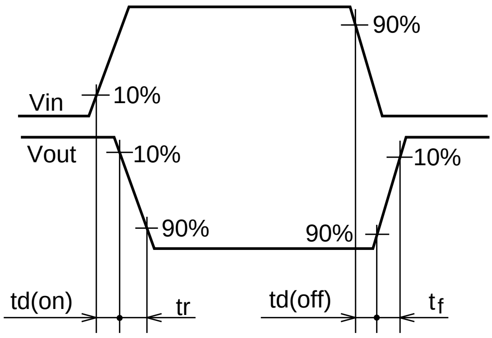




Switching Time Test Circuit

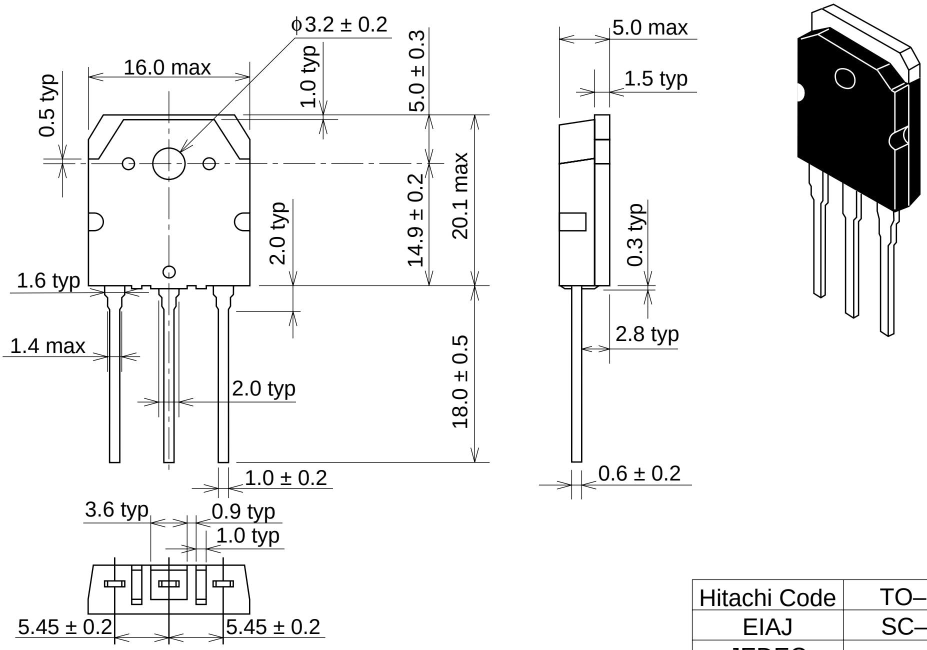


Waveform



Package Dimensions

Unit : mm



Hitachi Code	TO–3P
EIAJ	SC–65
JEDEC	—

2SK2568
Silicon N Channel MOS FET

HITACHI

1st. Edition
Jul. 1995
Preliminary

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- Suitable for switching regulator and DC–DC converter

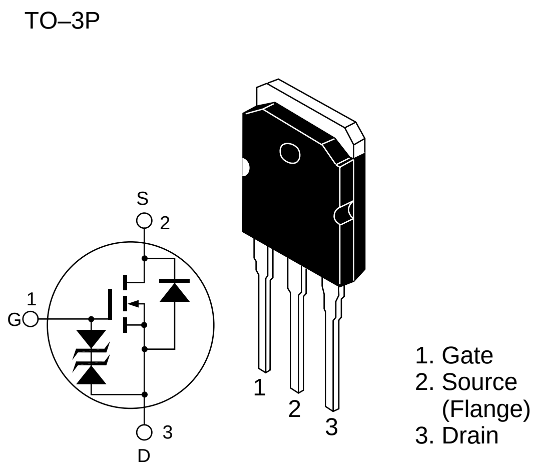


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D**	12	A
Drain peak current	$I_{D(pulse)}$*	48	A
Body–drain diode reverse drain current	I_{DR}**	12	A
Channel dissipation	Pch**	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

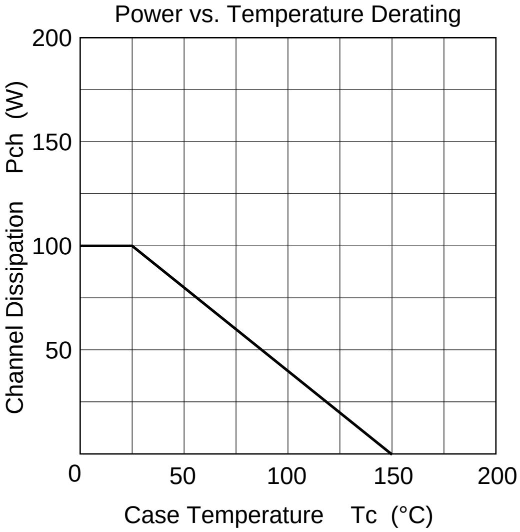
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25°C

Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.5	0.6	Ω	I_D = 6 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	6.0	10	—	S	I_D = 6 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(1560)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(450)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(72)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(22)	—	ns	I_D = 6 A
Rise time	t_r	—	(78)	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(140)	—	ns	RL = 5 Ω
Fall tiem	t_f	—	(60)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(1.1)	—	V	I_F = 12 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(105)	—	ns	I_F = 12 A, V_{GS} = 0 diF / dt = 100 A / µs

* Pulse Test


Power vs. Temperature Derating
Channel Dissipation Pch (W)
200
150
100
50
0
50
100
150
200
Case Temperature Tc (°C)

2SK2569

Silicon N Channel MOS FET

HITACHI

1st. Edition
Jun. 1995

Application

Low frequency power switching

Features

- Low on-resistance.
  $R_{DS(on)}$ = 2.6 Ω max.
  (at V_{GS} = 4 V, I_D = 100mA)
- 2.5V gate drive device.
- Small package (MPAK).

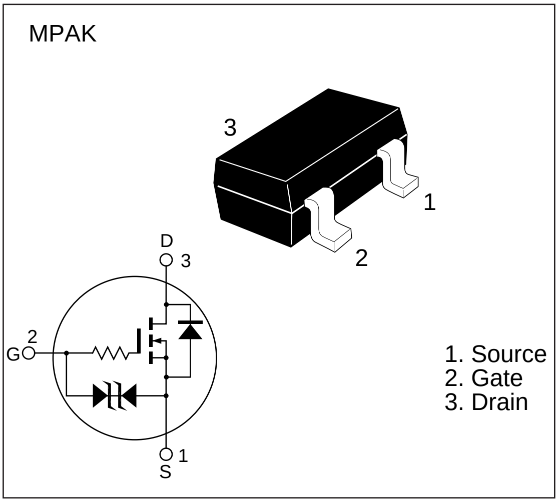


Table 1 Absolute Maximum Ratings (Ta = 25°C)

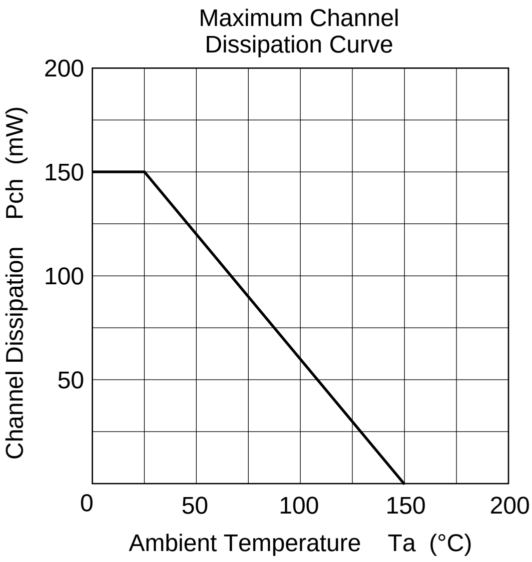
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	50	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}$*	0.4	A
Channel dissipation	Pch**	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	50	—	—	V	I_D = 100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1.0	µA	V_{DS} = 40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±2.0	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 10 µA, V_{DS} = 5 V
Static drain to source on state resistance	$R_{DS(on)}1$	—	2.0	2.6	Ω	I_D = –100 mA V_{GS} = –4 V *
Static drain to source on state resistance	$R_{DS(on)}2$	—	3.1	5.0	Ω	I_D = 40 mA V_{GS} = –2.5 V *
Foward transfer admittance	$\|y_{fs}\|$	0.13	0.23	—	S	I_D = 100 mA V_{DS} = 10 V
Input capacitance	Ciss	—	14.0	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	17.2	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	1.73	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	40	—	µs	V_{GS} = 10 V, I_D = 100 mA
Rise time	t_r	—	86	—	µs	R_L = 300 Ω
Turn–off delay tiem	$t_{d(off)}$	—	1120	—	µs	
Fall time	t_f	—	430	—	µs	

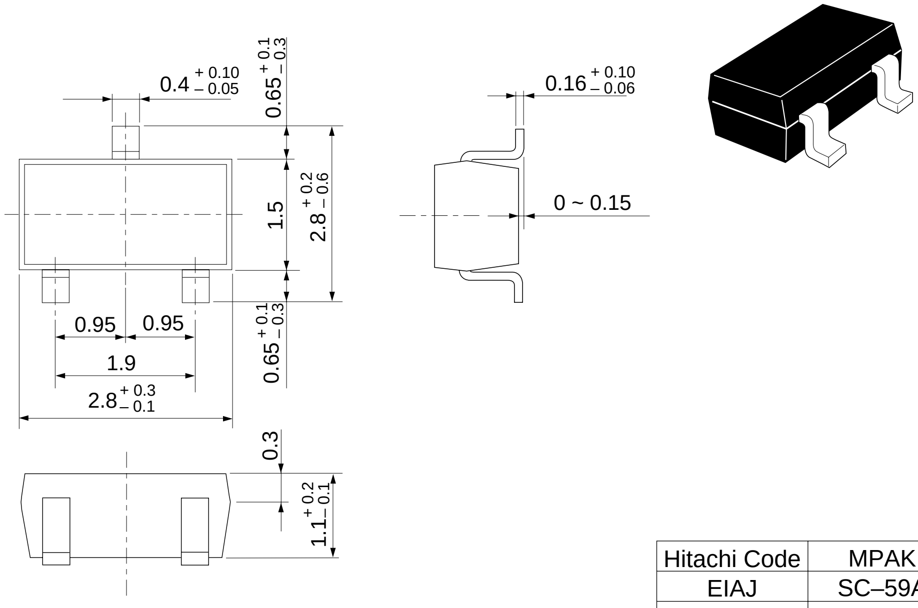
* Pulse Test
Marking is "ZN–"



Package Dimensions

Unit : mm

• MPAK



Hitachi Code	MPAK
EIAJ	SC–59A
JEDEC	—

2SK2582

Silicon N Channel MOS FET

HITACHI

1st. Edition
Jun. 1995
Preliminary

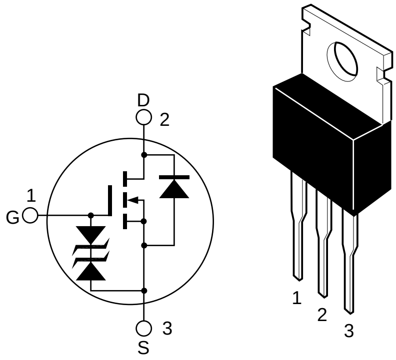
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter

TO–220AB



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	350	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	13	A
Drain peak current	$I_{D(pulse)}$*	52	A
Body–drain diode reverse drain current	I_{DR}	13	A
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

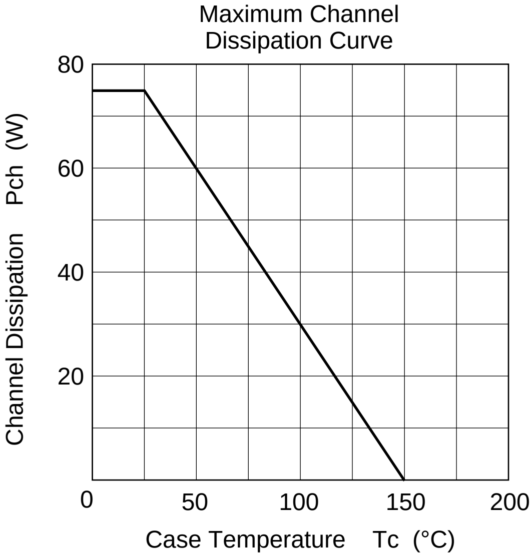
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

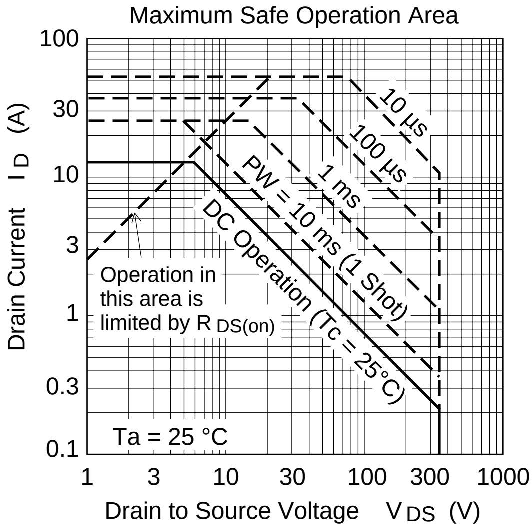
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	350	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =350 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.30	0.40	Ω	I_D = 7 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	9.0	—	S	I_D = 7 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1250	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	420	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	70	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 7 A
Rise time	t_r	—	70	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	R_L = 3.75Ω
Fall time	t_f	—	52	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 13 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	350	—	ns	I_F = 13 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

See characteristics curves of 2SK1401

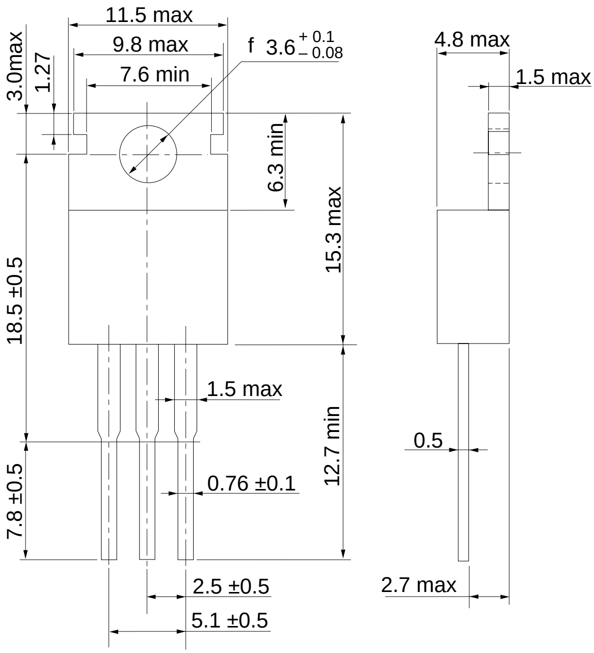


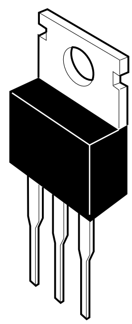


Package Dimensions

Unit : mm

• TO–220AB

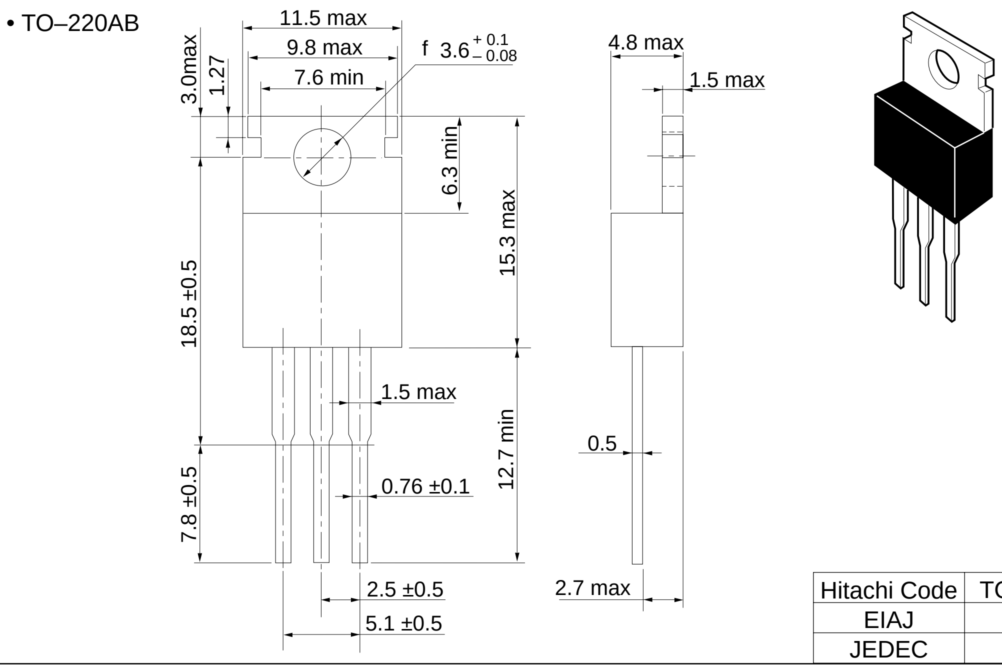




Hitachi Code	TO–220AB
EIAJ	SC–46
JEDEC	—

Package Dimensions

Unit : mm



Hitachi Code	TO–220AB
EIAJ	SC–46
JEDEC	—

2SK2586
Silicon N Channel MOS FET

HITACHI

3rd. Edition
Jun. 1995

Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)}$ = 7 mΩ typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V souece

TO–3P

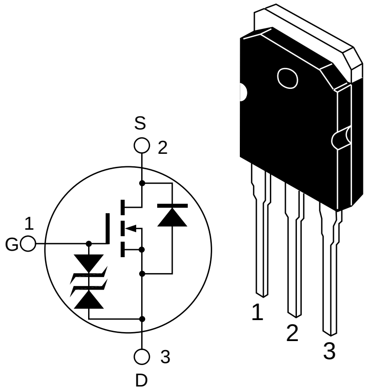


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D**	60	A
Drain peak current	$I_{D(pulse)}$*	240	A
Body–drain diode reverse drain current	I_{DR}**	60	A
Avalanche current	I_{AP}***	45	A
Avalanche energy	E_{AR}***	174	mJ
Channel dissipation	Pch**	125	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25°C
*** Value at Tch = 25°C, Rg ≥ 50 Ω

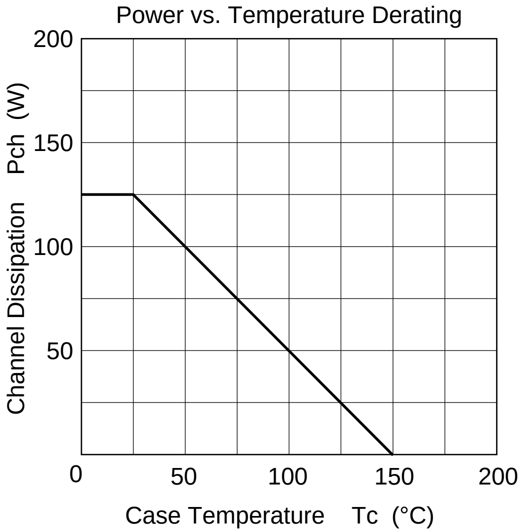
Hitachi semiconductor

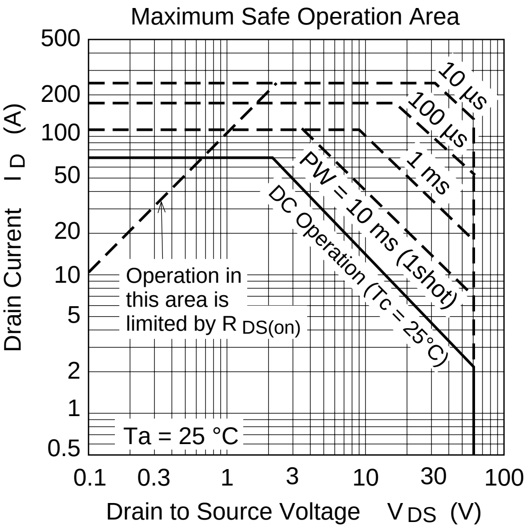
Table 2 Electrical Characteristics (Ta = 25°C)

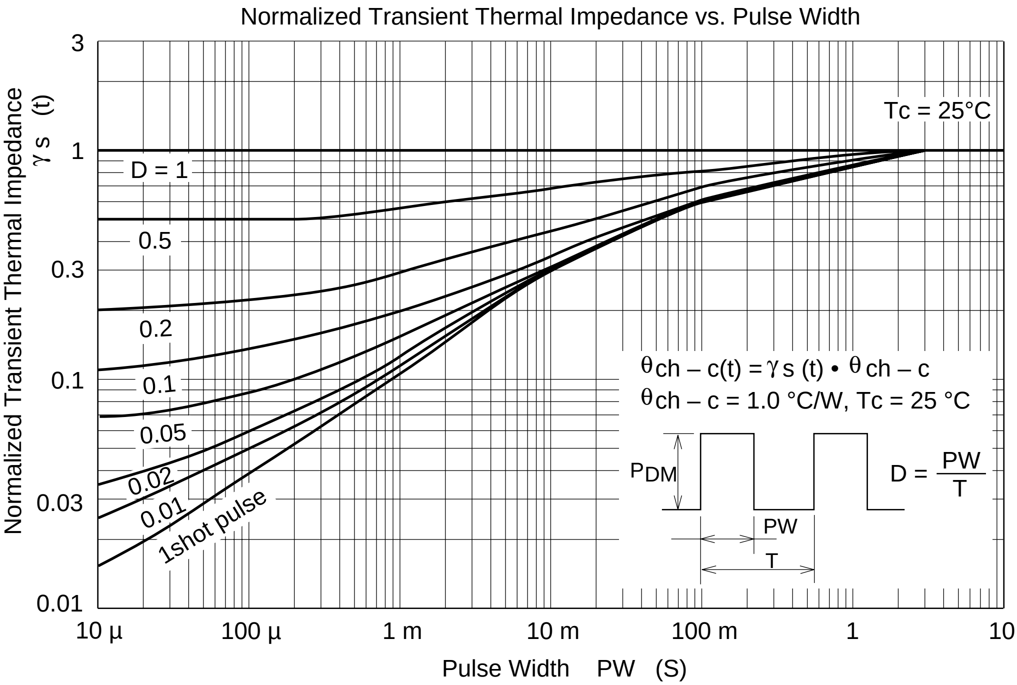
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	100	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	7	10	mΩ	I_D = 30 A V_{GS} = 10 V *
		—	10	16	mΩ	I_D = 30 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	35	60	—	S	I_D = 30 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3550	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1760	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	500	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	35	—	ns	I_D = 30 A
Rise time	t_r	—	260	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	480	—	ns	R_L = 1.0 Ω
Fall time	t_f	—	370	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.94	—	V	I_F = 60 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 60 A, V_{GS} = 0 diF / dt = 50 A / µs

* Pulse Test

■ See characteristic curves of 2SK2529.

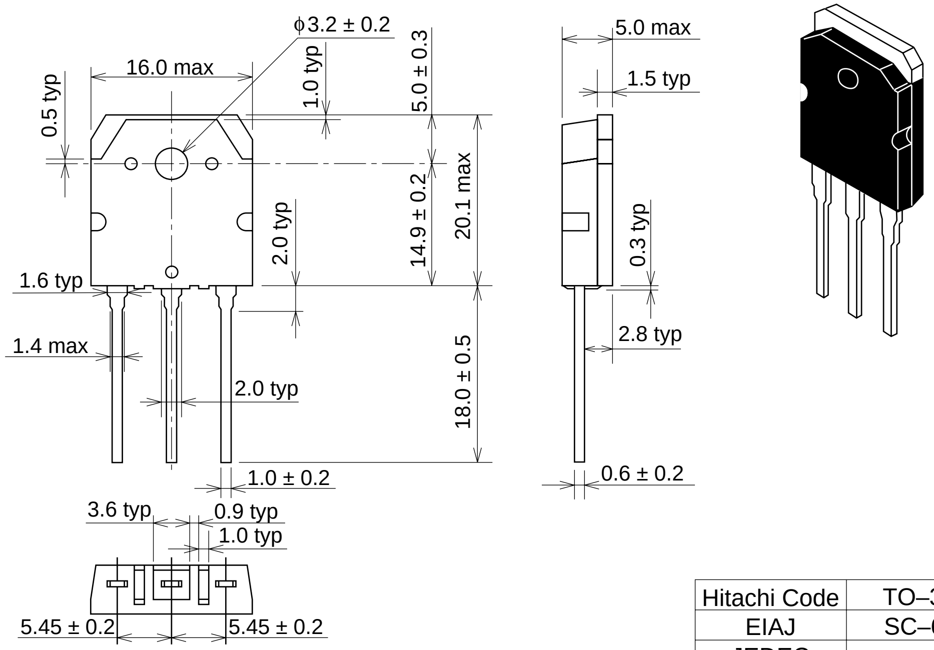

Power vs. Temperature Derating
Channel Dissipation Pch (W)
200
150
100
50
0
50
100
150
200
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25°C)
Operation in
this area is
limited by R DS(on)
Ta = 25 °C


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ s (t)
3
1
0.3
0.1
0.03
0.01
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γ s (t) • θ ch – c
θch – c = 1.0 °C/W, Tc = 25 °C
PDM
D = PW / T
PW
T

Package Dimensions

Unit : mm



Hitachi Code	TO–3P
EIAJ	SC–65
JEDEC	—

2SK2590
Silicon N Channel MOS FET

HITACHI

1st. Edition
Jun. 1995
Preliminary

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC – DC converter, Motor Control

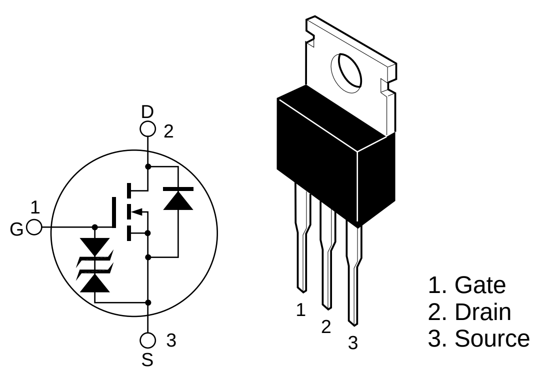


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

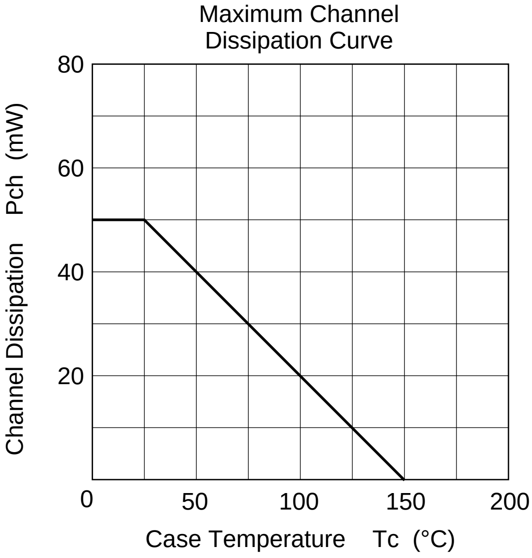
Hitachi semiconductor

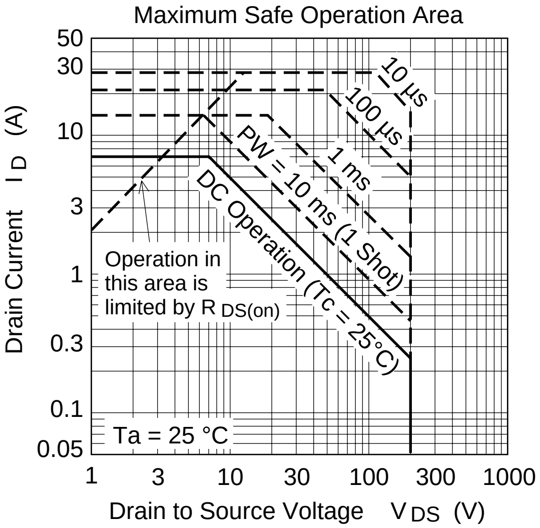
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} =160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.33	0.45	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	4.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	260	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 4 A
Rise time	t_r	—	45	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	50	—	ns	R_L = 7.5Ω
Fall time	t_f	—	35	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	150	—	ns	I_F = 7 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

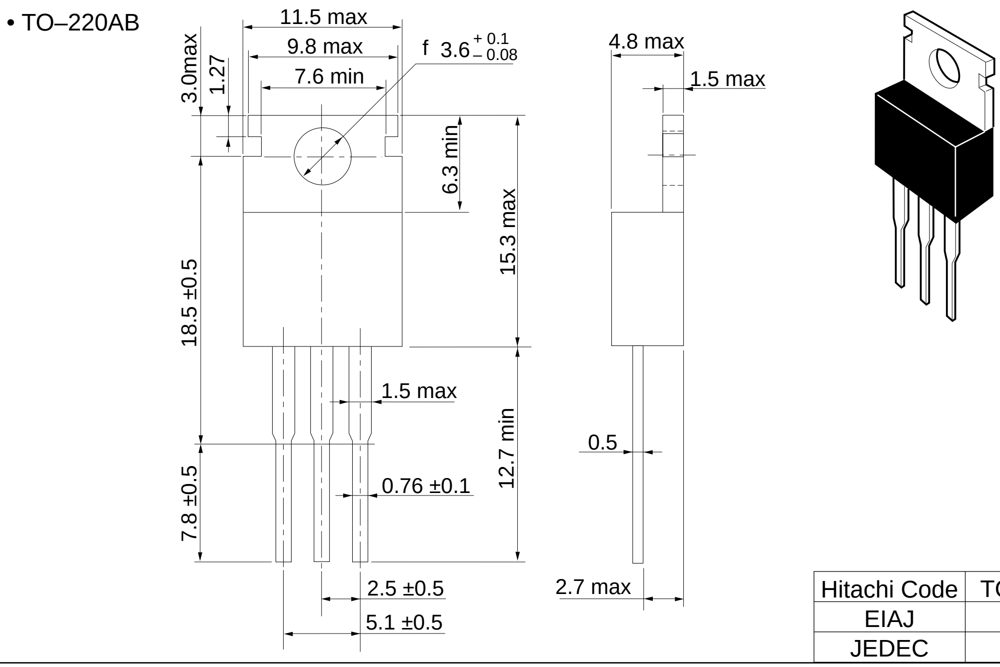
See characteristics curves of 2SK1957.





Package Dimensions

Unit : mm

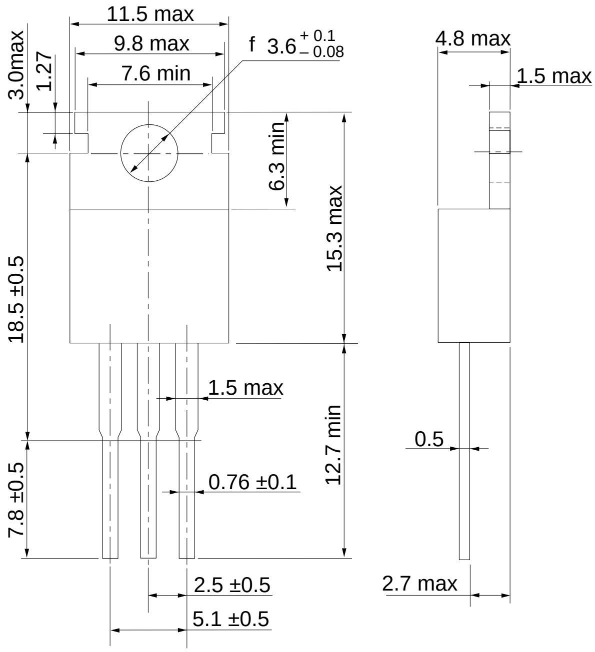


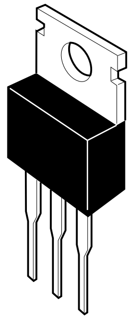
Hitachi Code	TO–220AB
EIAJ	SC–46
JEDEC	—

Package Dimensions

Unit : mm

• TO–220AB





Hitachi Code	TO–220AB
EIAJ	SC–46
JEDEC	—

2SK2591
Silicon N Channel MOS FET

HITACHI

1st. Edition
Jun. 1995
Preliminary

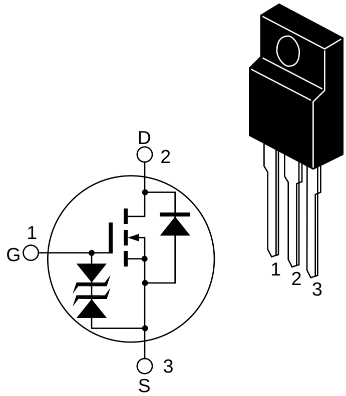
Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC–DC converter

TO–220CFM



1. Gate
2. Drain
3. Source

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}$*	32	A
Body–drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	Pch**	35	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at Tc = 25 °C

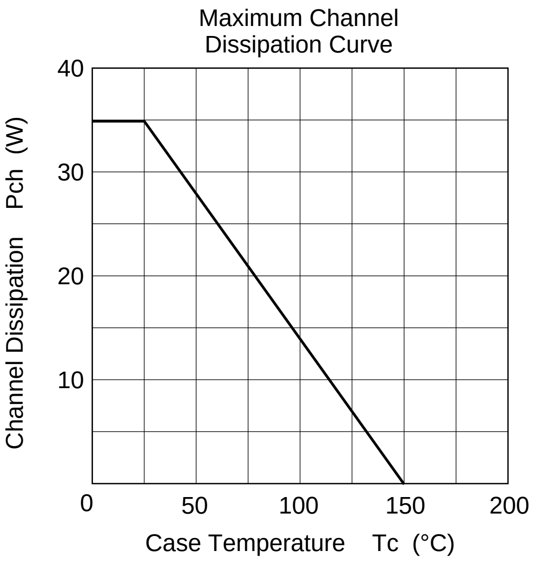
Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} =500 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	–3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.45	0.60	Ω	I_D = 4 A V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	7.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	410	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	55	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 4 A
Rise time	t_r	—	55	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	130	—	ns	R_L = 5Ω
Fall time	t_f	—	50	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	380	—	ns	I_F = 8 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test

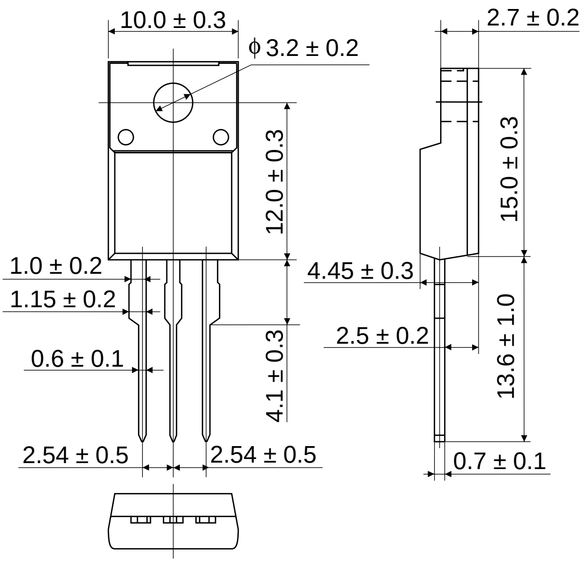
See characteristics curves of 2SK1166

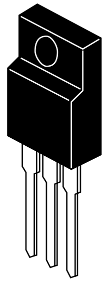


Package Dimensions

Unit : mm

• TO–220CFM





Hitachi Code	TO–220CFM
EIAJ	—
JEDEC	—

HAT1001F

Silicon P Channel Power MOS FET

HITACHI

2nd. Edition
Apr. 1995

Application

Power switching

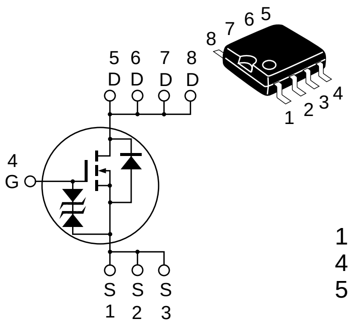
Features

- Low on–resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

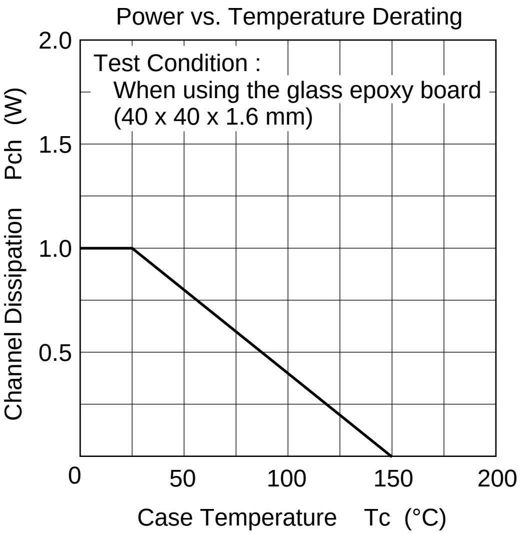
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–3.5	A
Drain peak current	$I_{D(pulse)}$*	–15	A
Body–drain diode reverse drain current	I_{DR}	–3.5	A
Channel dissipation	Pch**	1.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

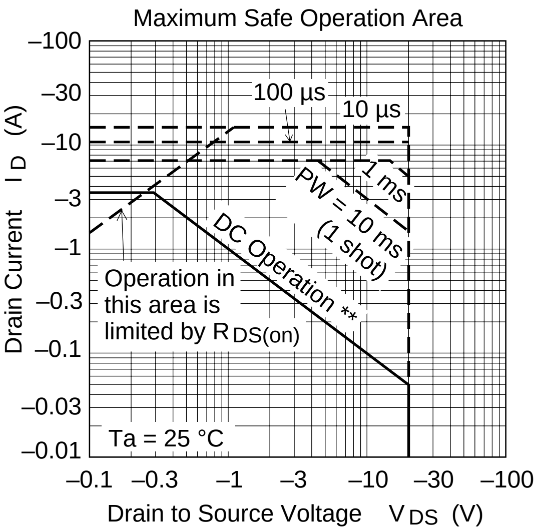
* PW ≤ 10 μs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

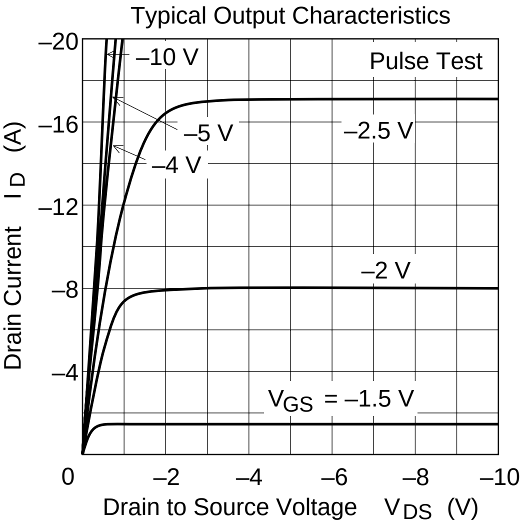
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.07	Ω	I_D = –2 A V_{GS} = –4 V *
		—	0.07	0.1	Ω	I_D = –2 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	8.0	—	S	I_D = –2 A V_{DS} = - 10 V *
Input capacitance	Ciss	—	1170	—	pF	V_{DS} = - 10 V
Output capacitance	Coss	—	860	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	310	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	240	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	360	—	ns	
Fall time	t_f	—	430	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = –3.5A, V_{GS} = 0 diF / dt = –20 A / µs

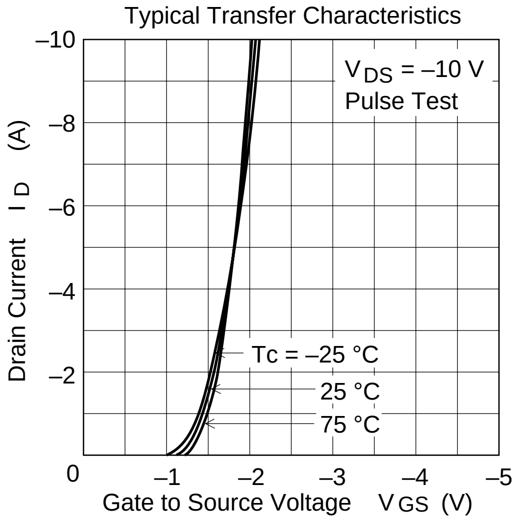
* Pulse Test



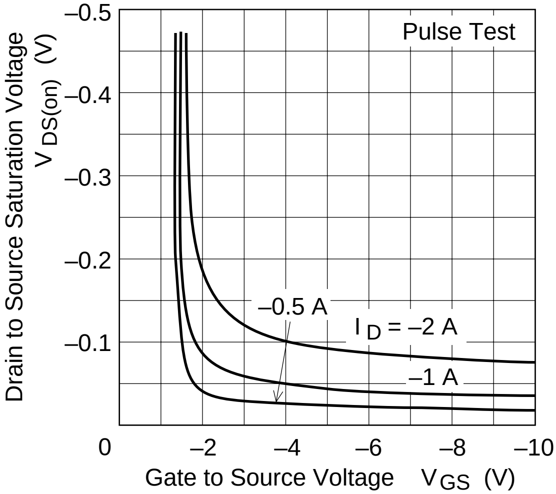


** When using the glass epoxy board
(40 x 40 x 1.6 mm)

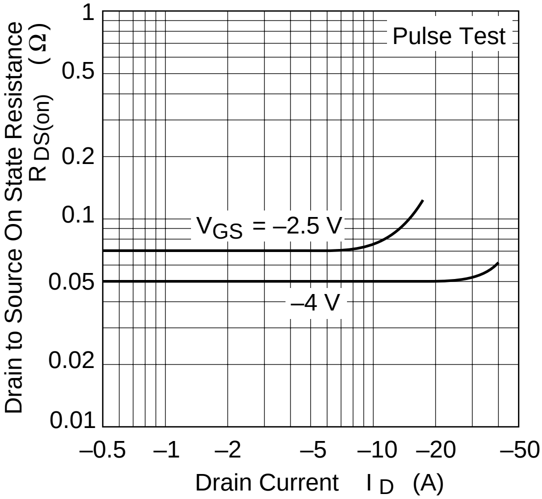




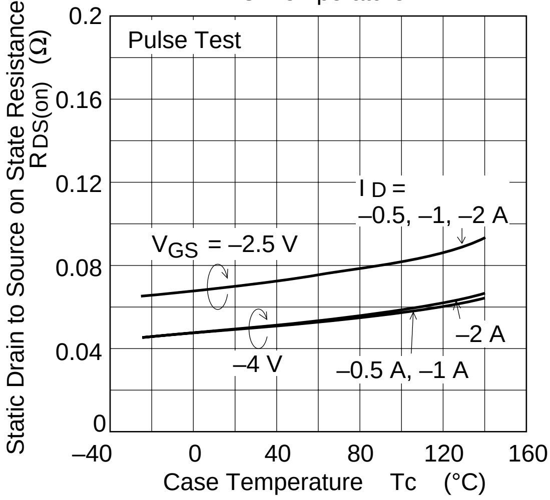
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



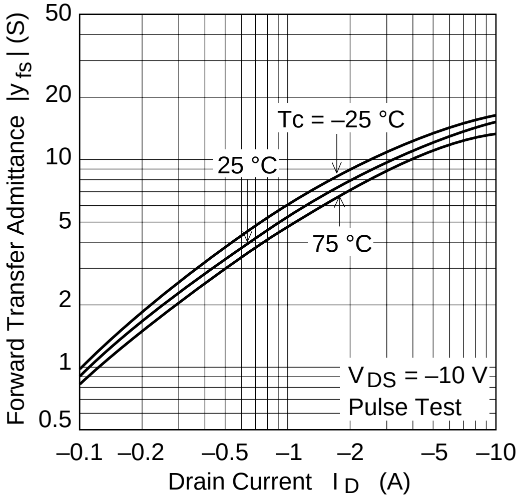
Static Drain to Source on State Resistance
vs. Drain Current

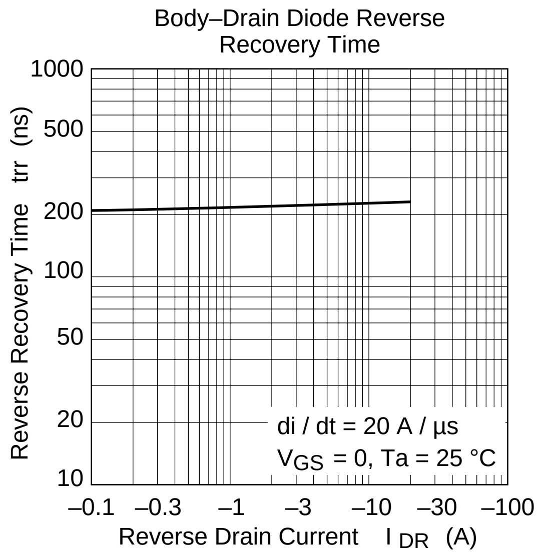


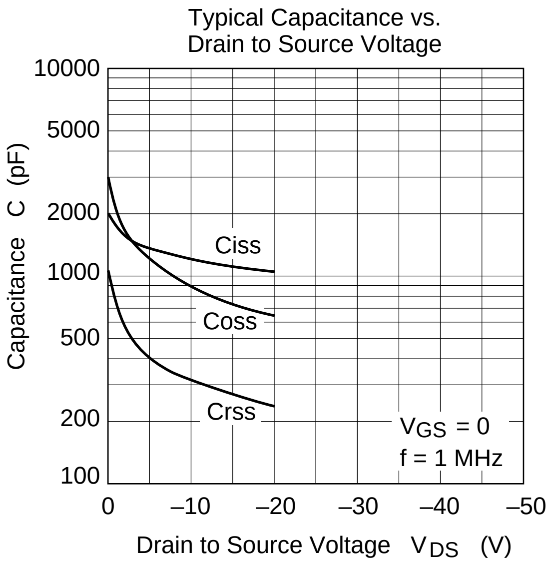
Static Drain to Source on State Resistance
vs. Temperature

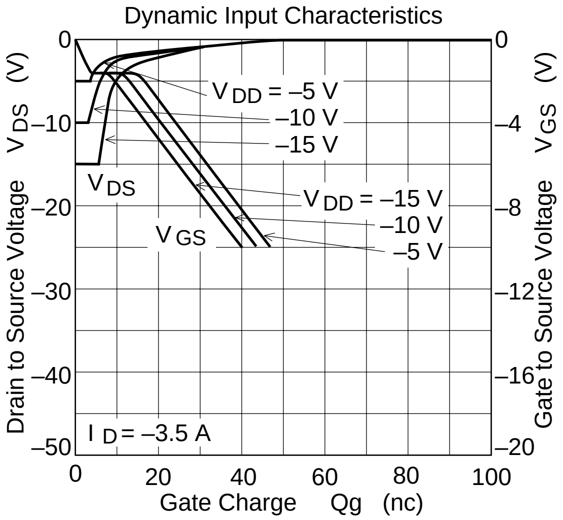


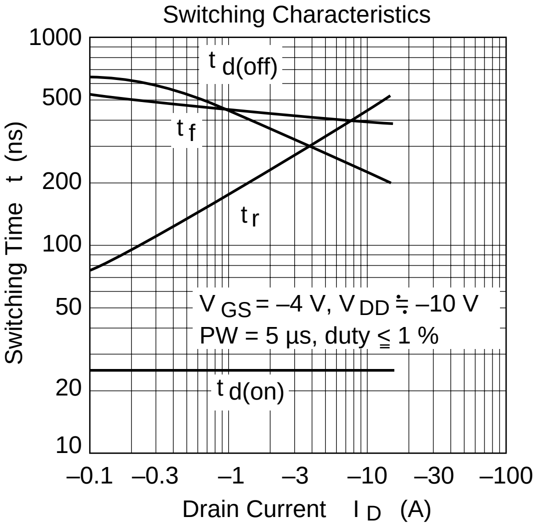
Forward Transfer Admittance vs.
Drain Current

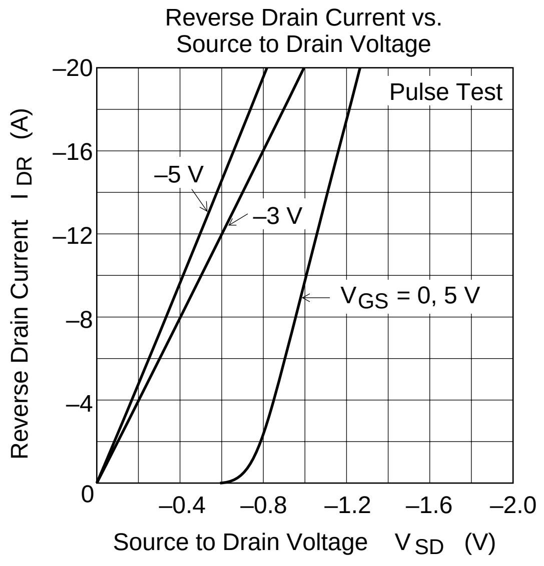



Body–Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.1
–0.3
–1
–3
–10
–30
–100
Reverse Drain Current I DR (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
5000
2000
1000
500
200
100
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)

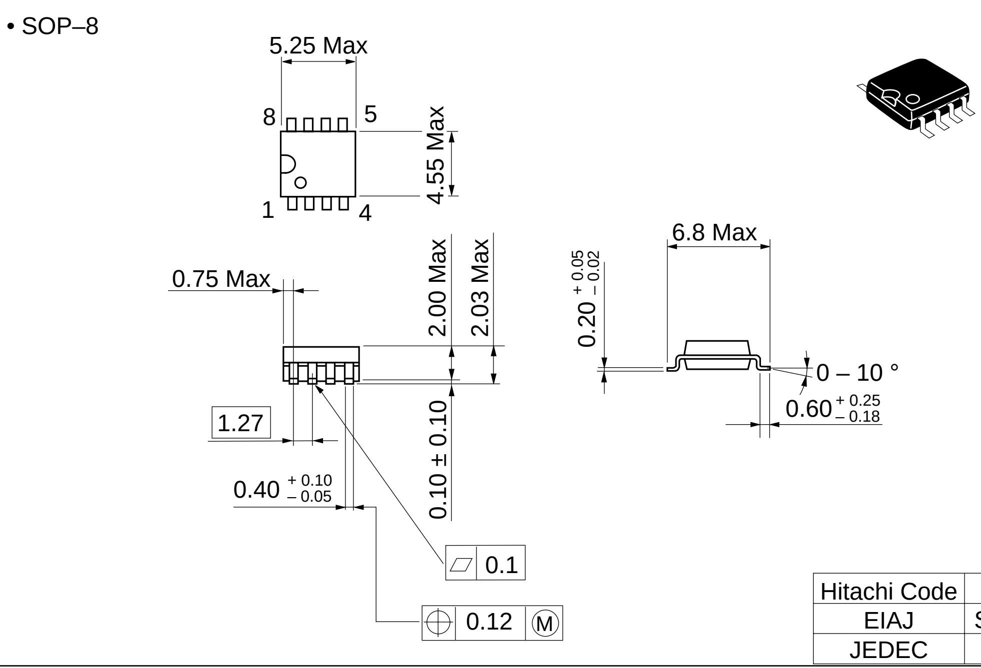

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
0
–10
–20
–30
–40
–50
0
–4
–8
–12
–16
–20
VDD = –5 V
–10 V
–15 V
VDS
VDD = –15 V
–10 V
–5 V
VGS
I D = –3.5 A
0
20
40
60
80
100
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
t d(off)
t f
t r
V GS = –4 V, V DD ≒ –10 V
PW = 5 µs, duty ≦ 1 %
t d(on)
–0.1
–0.3
–1
–3
–10
–30
–100
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1002F

Silicon P Channel Power MOS FET

HITACHI

2nd. Edition
Apr. 1995

Application

High speed power switching

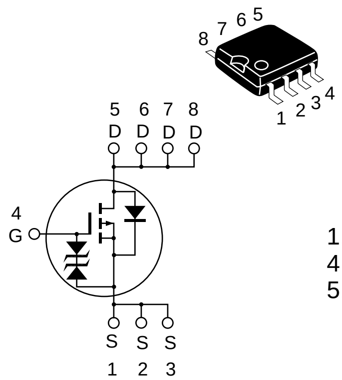
Features

- Low on–resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

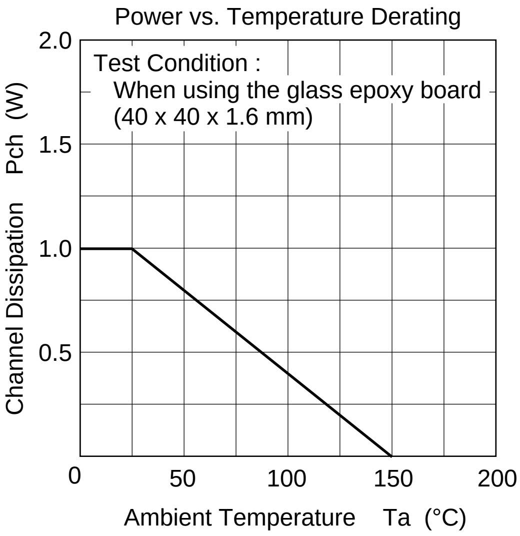
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–3.5	A
Drain peak current	$I_{D(pulse)}$*	–14	A
Body–drain diode reverse drain current	I_{DR}	–3.5	A
Channel dissipation	Pch**	1.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

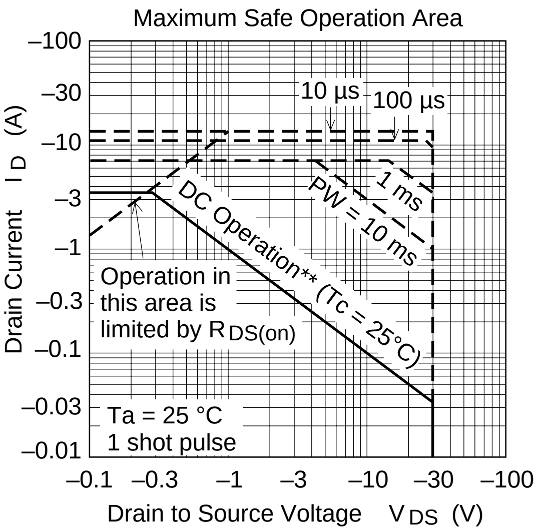
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

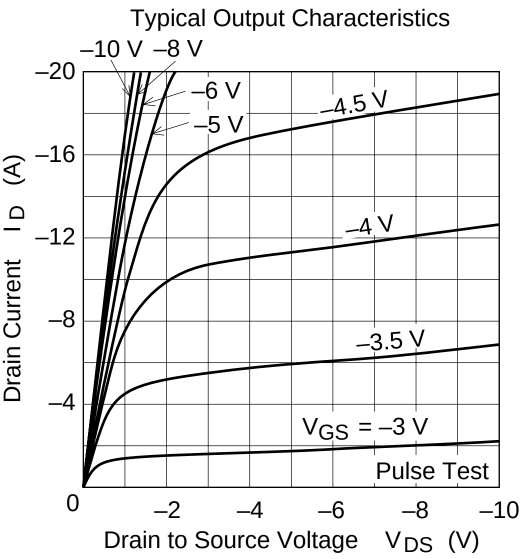
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.07	Ω	I_D = –2 A V_{GS} = –10 V *
		—	0.10	0.13	Ω	I_D = –2 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	6.0	—	S	I_D = –2 A V_{DS} = - 10 V *
Input capacitance	Ciss	—	960	—	pF	V_{DS} = - 10 V
Output capacitance	Coss	—	630	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	215	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	50	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	285	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	90	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.8	—	V	I_F = –3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	60	—	ns	I_F = –3.5 A, V_{GS} = 0 diF / dt = 20A / µs

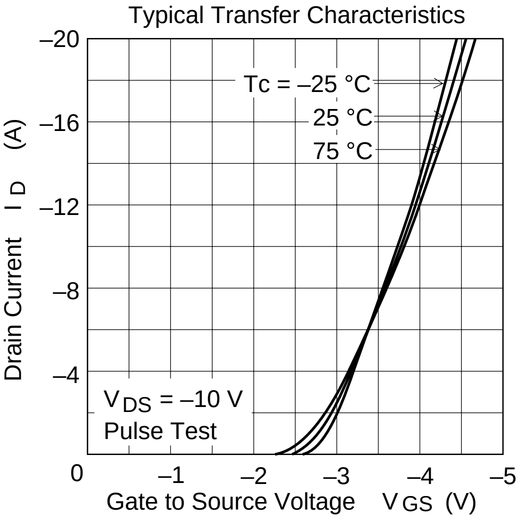
* Pulse Test

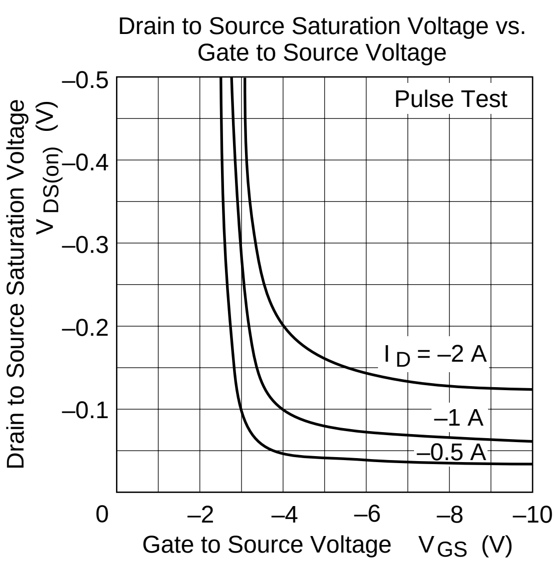


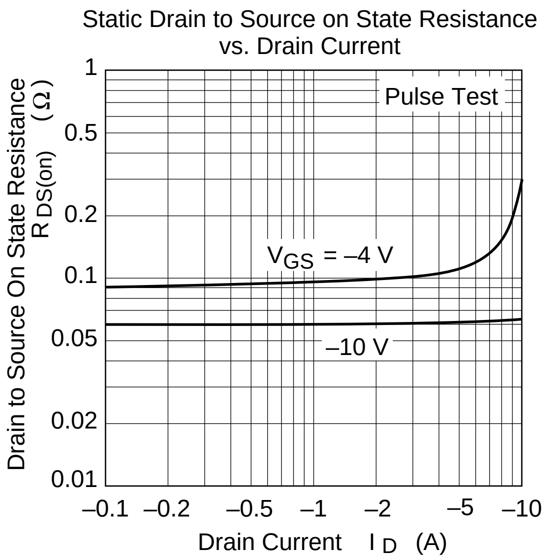


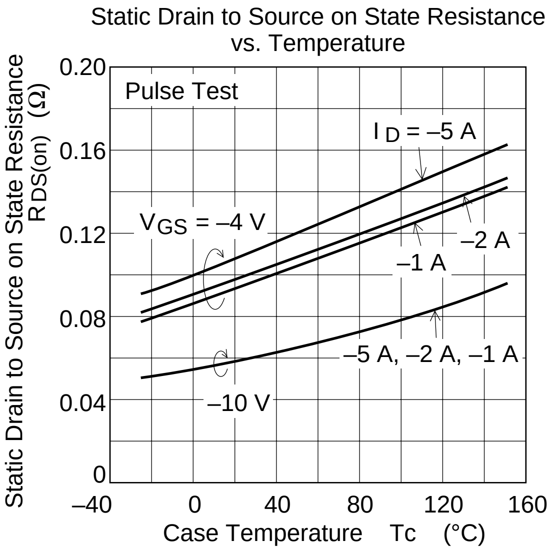
** When using the glass epoxy board
(40 x 40 x 1.6 mm)

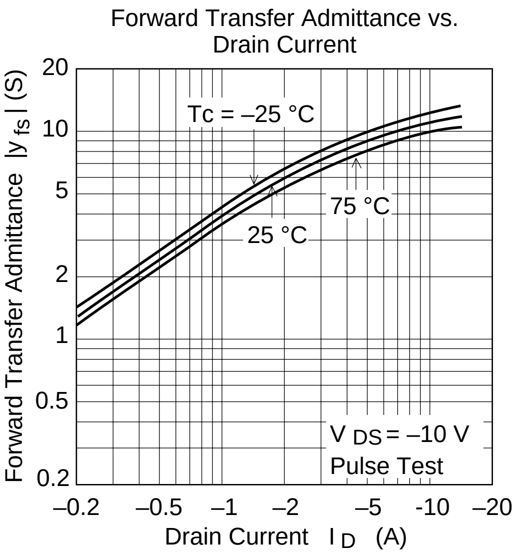


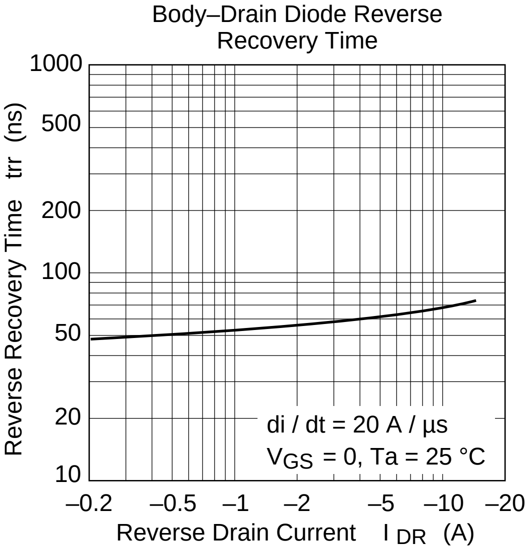


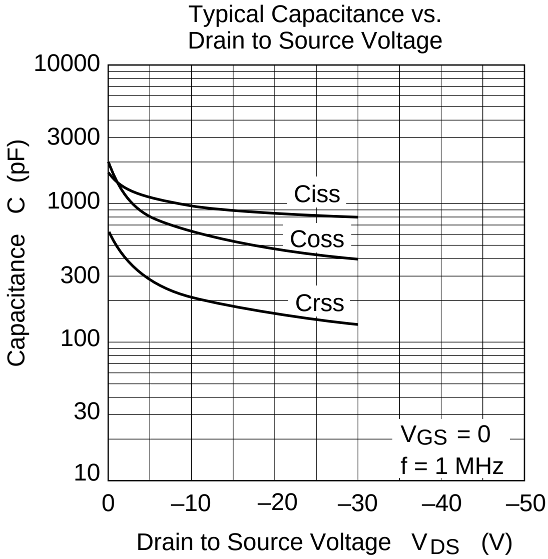

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –2 A
–1 A
–0.5 A
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)
Drain to Source Saturation Voltage
V DS(on) (V)

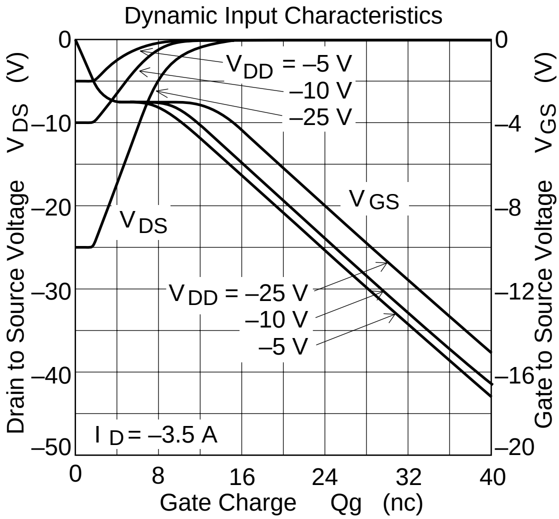

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
VGS = –4 V
–10 V
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)
Drain to Source On State Resistance
R DS(on) (Ω)

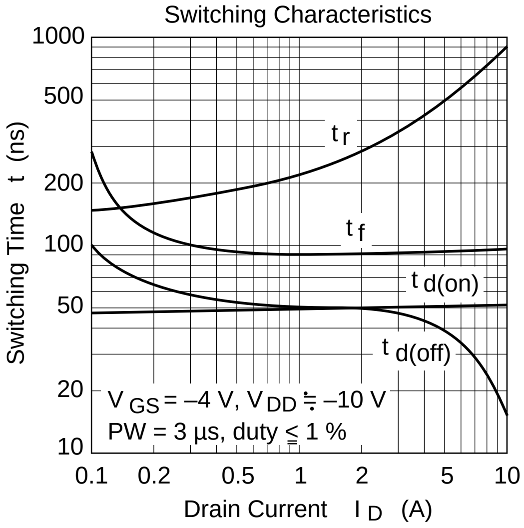

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –5 A
VGS = –4 V
–2 A
–1 A
–5 A, –2 A, –1 A
–10 V
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)
Static Drain to Source on State Resistance
R DS(on) (Ω)

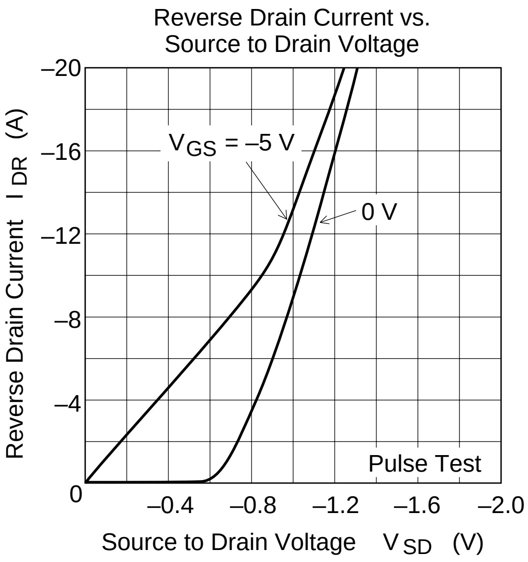

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
75 °C
25 °C
V DS = –10 V
Pulse Test
20
10
5
2
1
0.5
0.2
–0.2
–0.5
–1
–2
–5
-10
–20
Drain Current I D (A)
Forward Transfer Admittance |y fs | (S)


Body–Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.2
–0.5
–1
–2
–5
–10
–20
Reverse Drain Current I DR (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
–10
–20
–30
–40
–50
Drain to Source Voltage VDS (V)

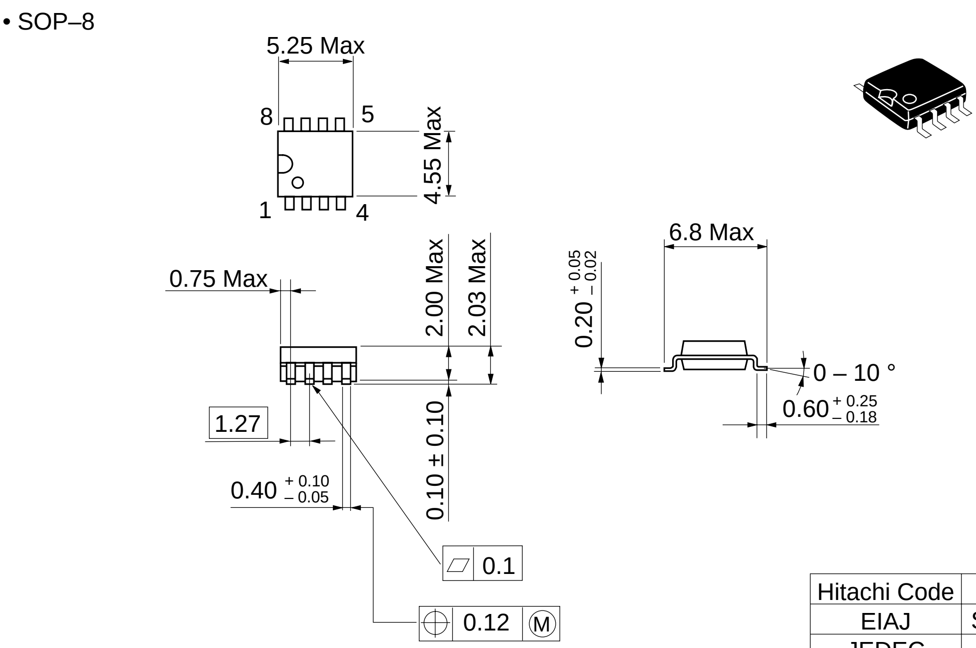

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
0
–10
–20
–30
–40
–50
0
–4
–8
–12
–16
–20
VDD = –5 V
–10 V
–25 V
VGS
VDS
VDD = –25 V
–10 V
–5 V
I D = –3.5 A
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
t r
t f
t d(on)
t d(off)
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≦ 1 %
0.1
0.2
0.5
1
2
5
10
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1004F Target Specification

Silicon P Channel Power MOS FET

2nd. Edition
Apr. 1995

HITACHI

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

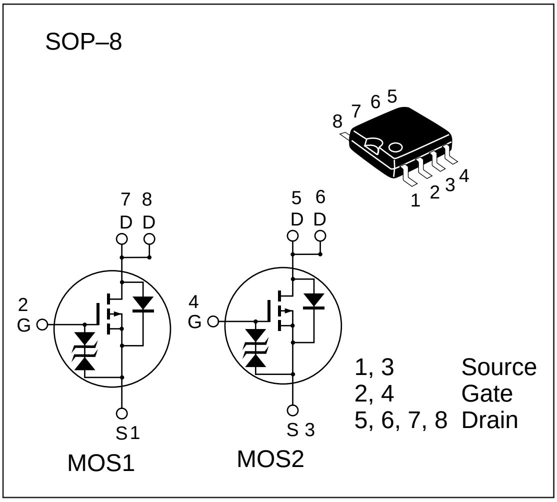


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–2.5	A
Drain peak current	$I_{D(pulse)}$*	–10	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

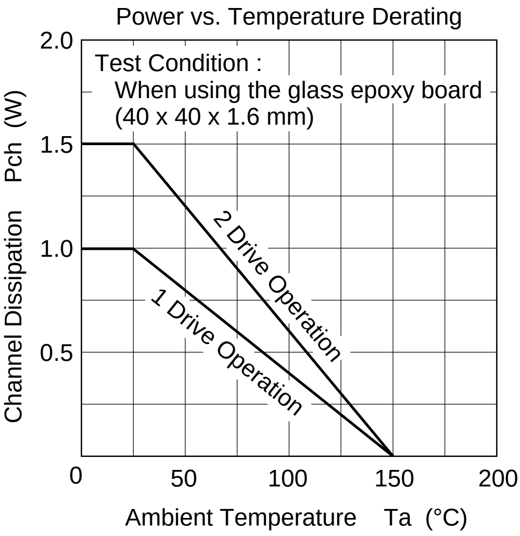
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

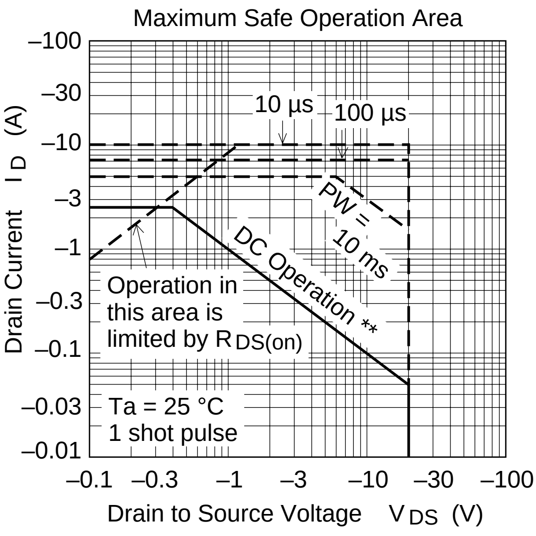
Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

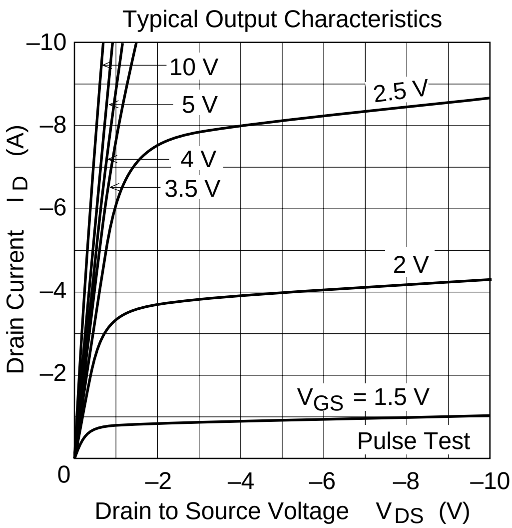
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.12	Ω	I_D = –2A V_{GS} = –4V *
		—	0.14	0.2	Ω	I_D = –2A V_{GS} = –2.5V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	5.5	—	S	I_D = –2 A V_{DS} = - 10 V *
Input capacitance	Ciss	—	750	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	500	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	190	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	28	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	125	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	135	—	ns	
Fall time	t_f	—	135	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –2.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	40	—	ns	I_F = –2.5 A, V_{GS} = 0 diF / dt = 20A / µs

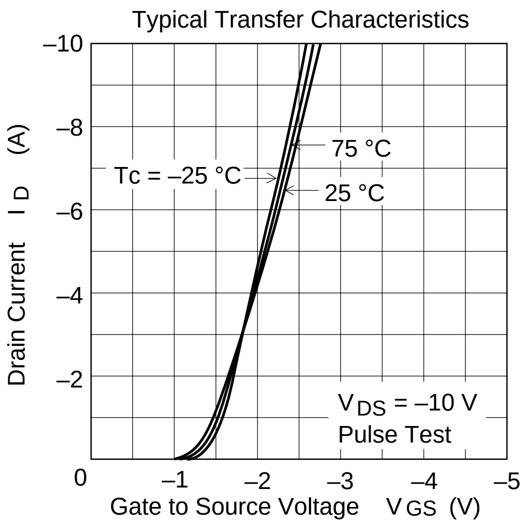
* Pulse Test

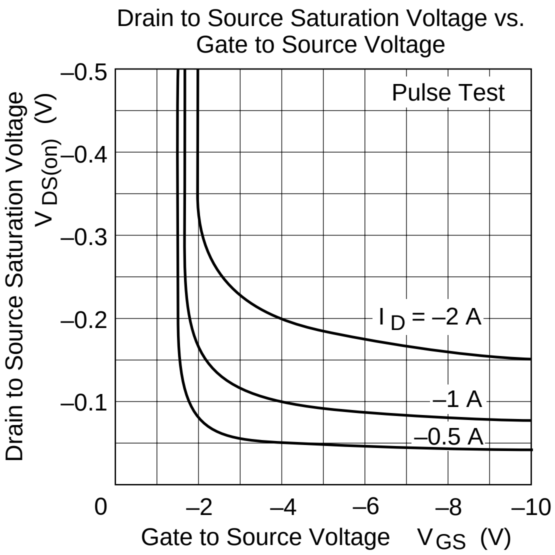


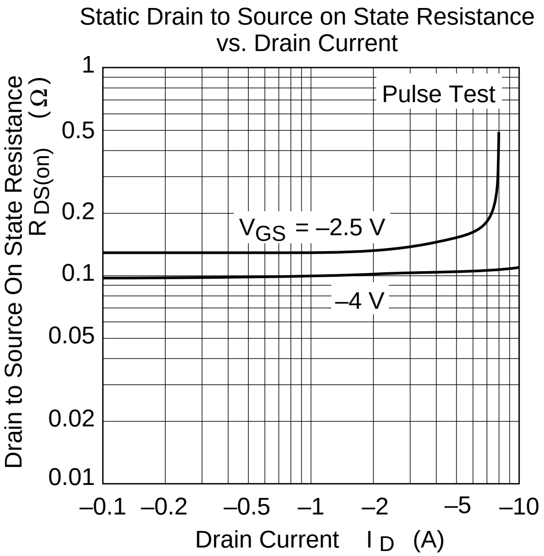


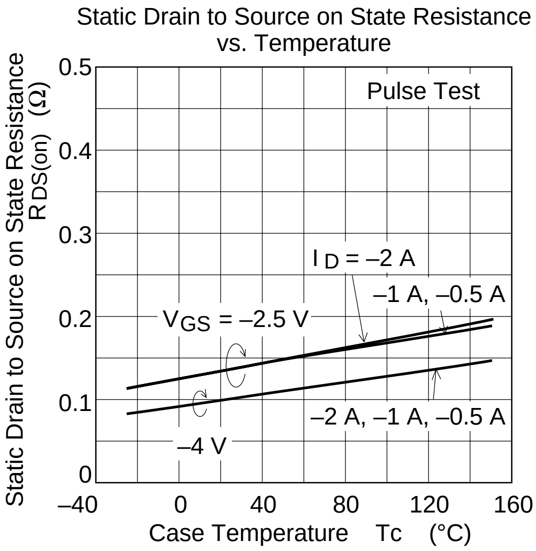
** 1 Drive operation
When using the glass epoxy board
(40 x 40 x 1.6 mm)

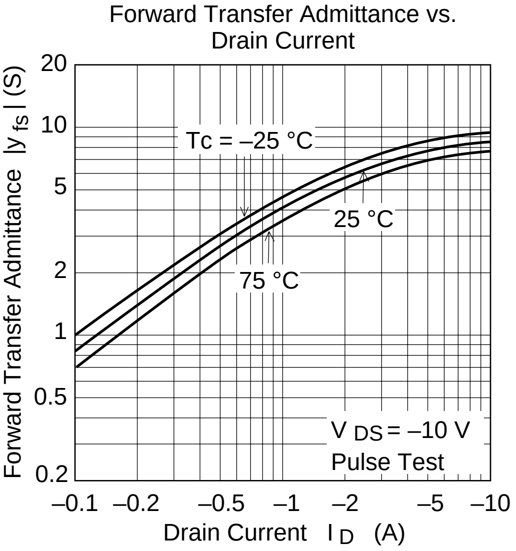


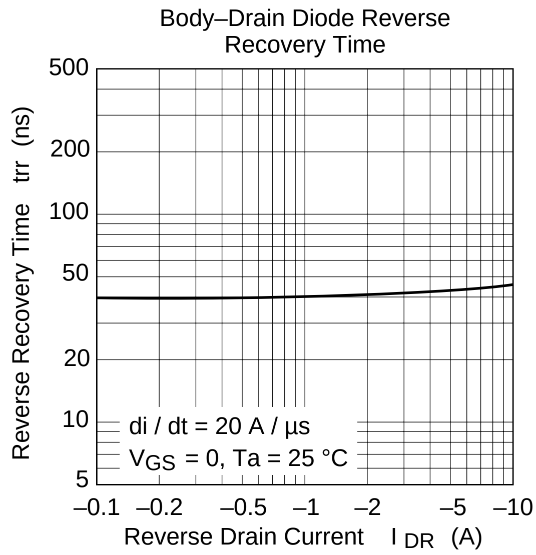


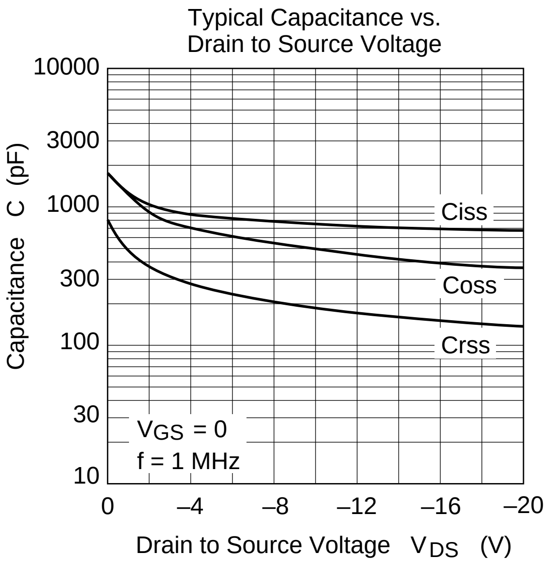

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –2 A
–1 A
–0.5 A
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)
Drain to Source Saturation Voltage
V DS(on) (V)

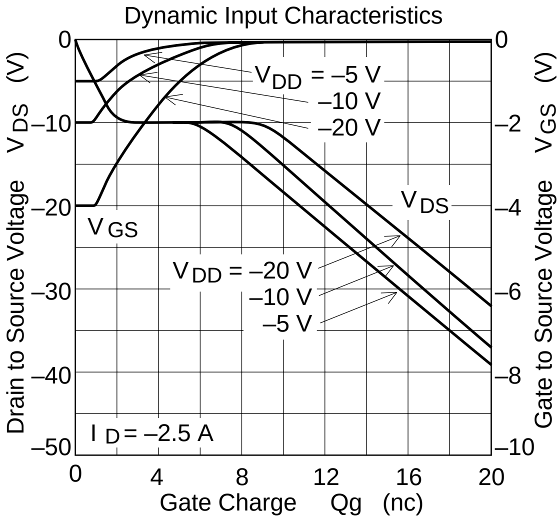

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –2.5 V
–4 V
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)
Drain to Source On State Resistance
R DS(on) (Ω)

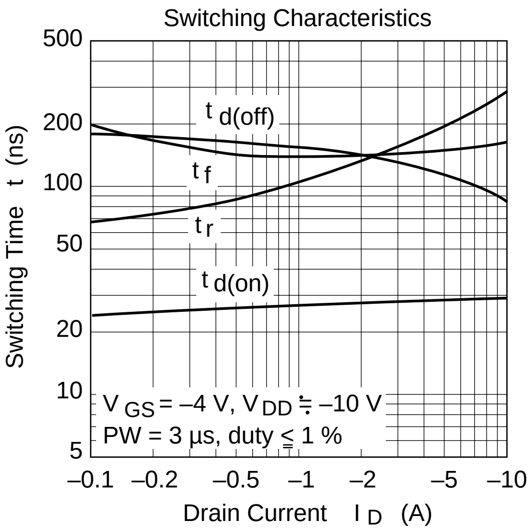

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –2 A
–1 A, –0.5 A
V GS = –2.5 V
–2 A, –1 A, –0.5 A
–4 V
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)
Static Drain to Source on State Resistance
R DS(on) (Ω)

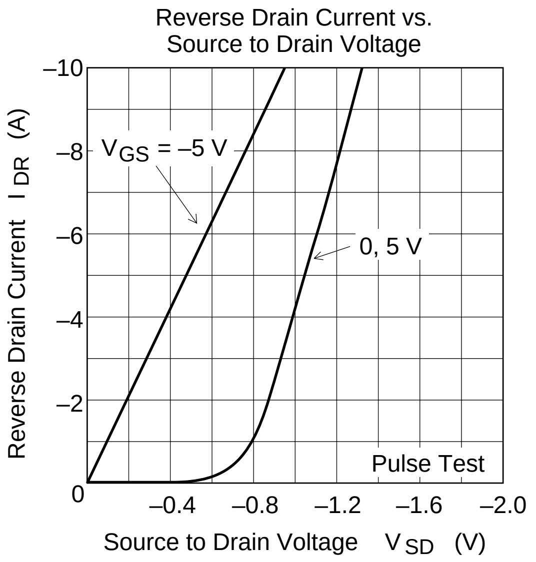

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
20
10
5
2
1
0.5
0.2
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)
Forward Transfer Admittance |y fs| (S)


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.2 –0.5 –1 –2 –5 –10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –4 –8 –12 –16 –20
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–10
–20
–30
–40
–50
Gate to Source Voltage VGS (V)
0
–2
–4
–6
–8
–10
VDD = –5 V
–10 V
–20 V
VDS
VGS
VDD = –20 V
–10 V
–5 V
I D = –2.5 A
0 4 8 12 16 20
Gate Charge Qg (nc)

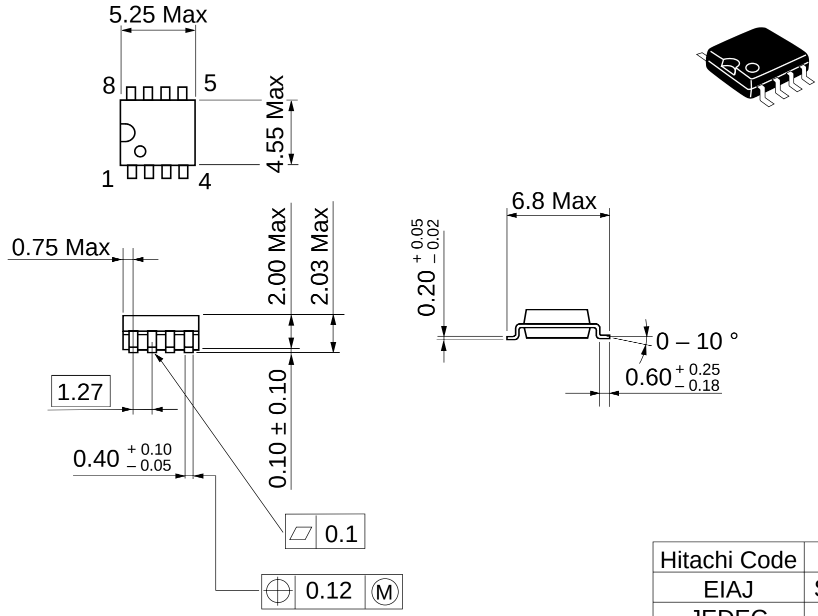

Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t d(off)
t f
t r
t d(on)
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≤ 1 %
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1005F

Silicon P Channel Power MOS FET

2nd Edition
Apr. 1995

HITACHI

Application

Power switching

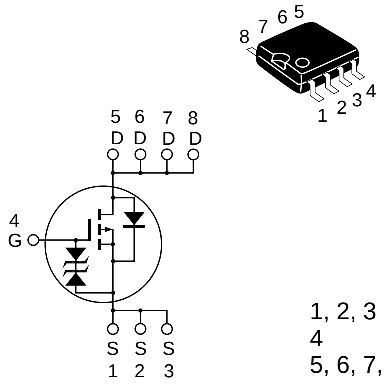
Features

- Low on–resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–3.5	A
Drain peak current	$I_{D(pulse)}$*	–14	A
Body–drain diode reverse drain current	I_{DR}	–3.5	A
Channel dissipation	Pch**	1.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

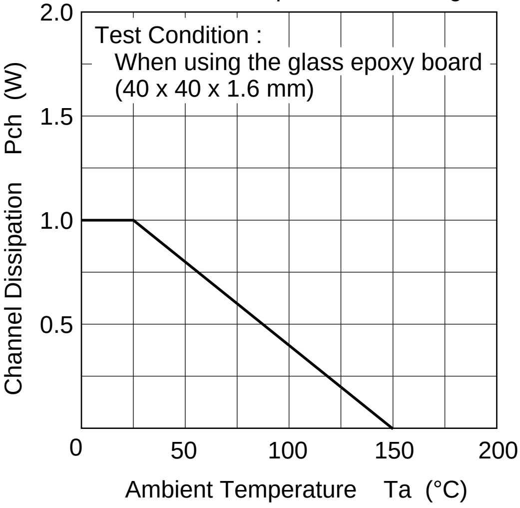
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

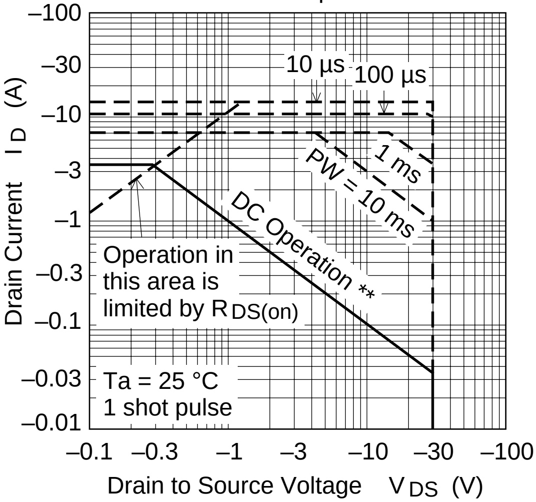
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.07	0.09	Ω	I_D = –2 A V_{GS} = –10 V *
		—	0.095	0.13	Ω	I_D = –2 A V_{GS} = –4 V *
		—	0.14	0.2	Ω	I_D = -0.7 A V_{GS} = - 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	6	—	S	I_D = –2 A V_{DS} = - 10 V *
Input capacitance	Ciss	—	840	—	pF	V_{DS} = - 10 V
Output capacitance	Coss	—	515	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	145	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	115	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	120	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.8	—	V	I_F = –3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	65	—	ns	I_F = –3.5 A, V_{GS} = 0 diF / dt = 20A / µs

* Pulse Test

Power vs. Temperature Derating

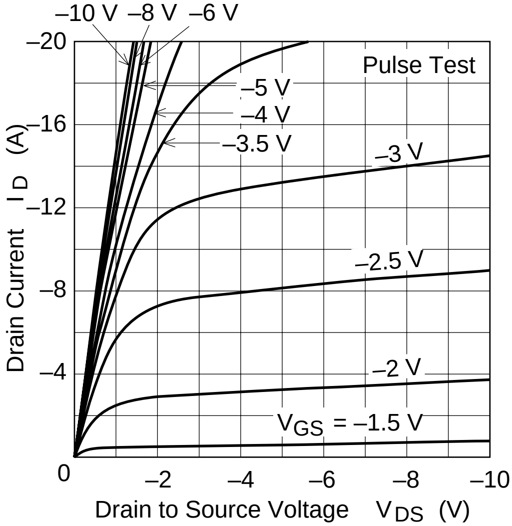


Maximum Safe Operation Area

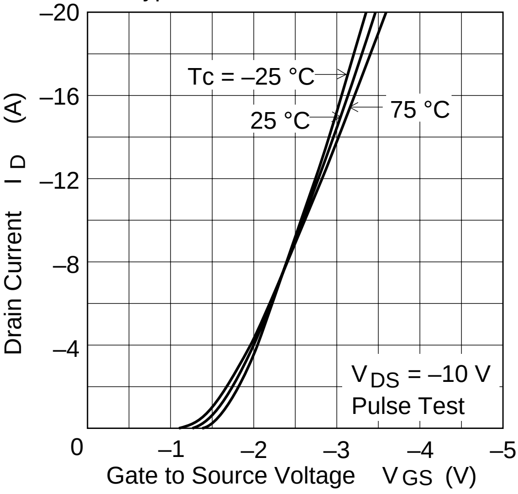


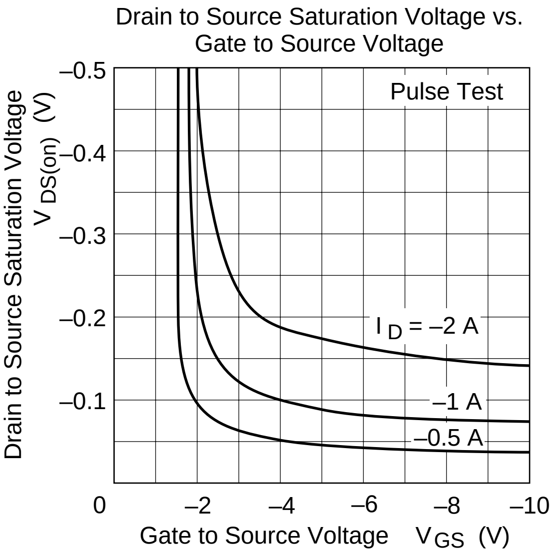
** When using the glass epoxy board
(40 x 40 x 1.6 mm)

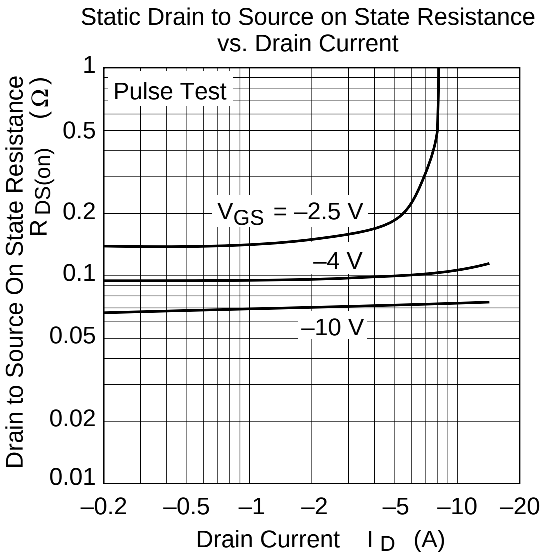
Typical Output Characteristics

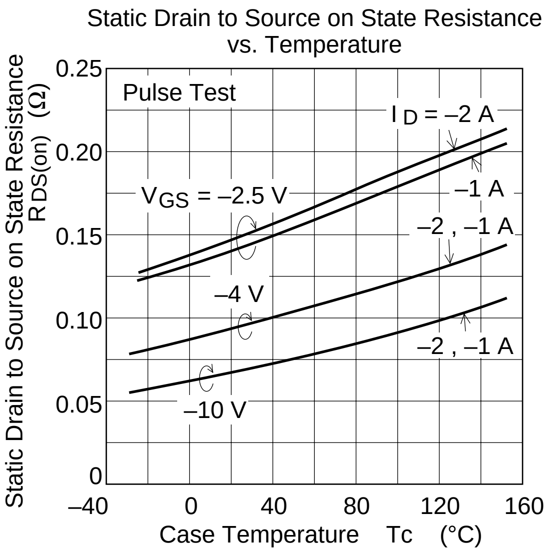


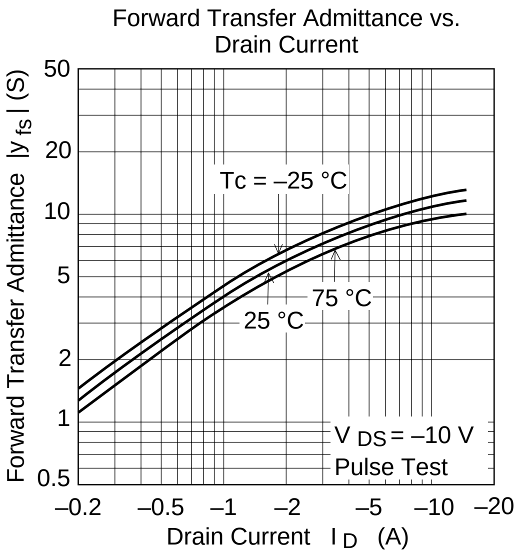
Typical Transfer Characteristics

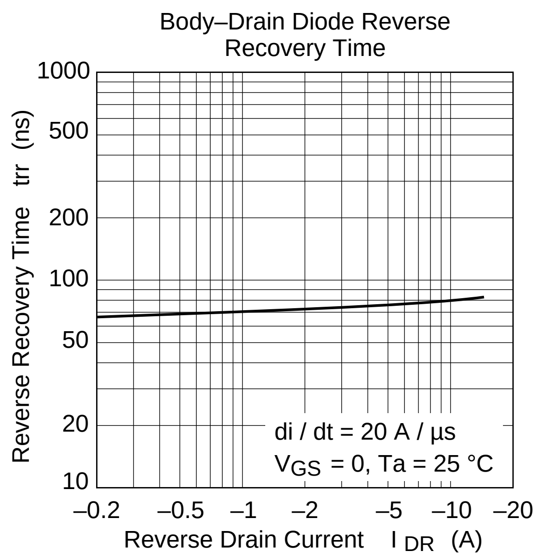


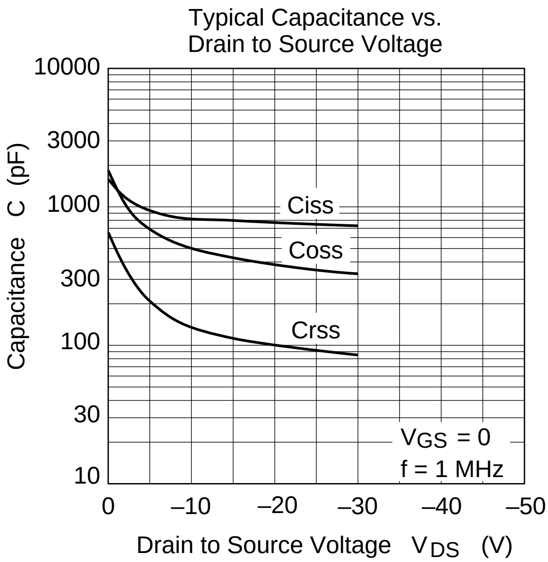

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –2 A
–1 A
–0.5 A
Drain to Source Saturation Voltage V DS(on) (V)
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

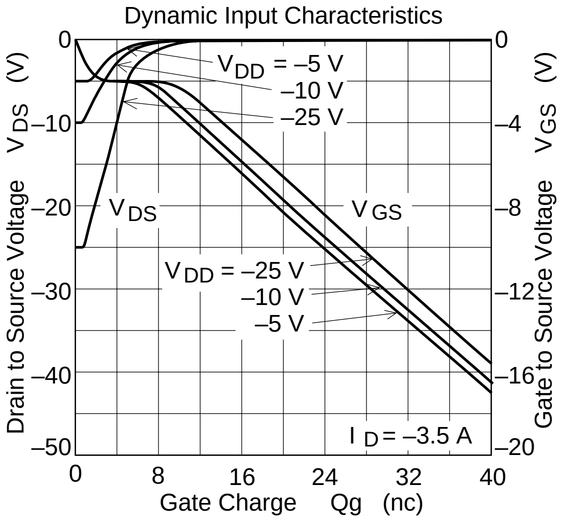

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –2.5 V
–4 V
–10 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)

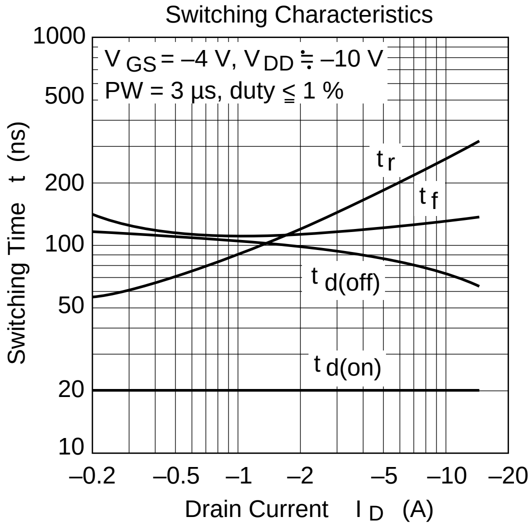

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –2 A
–1 A
V GS = –2.5 V
–2 , –1 A
–4 V
–2 , –1 A
–10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.25
0.20
0.15
0.10
0.05
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

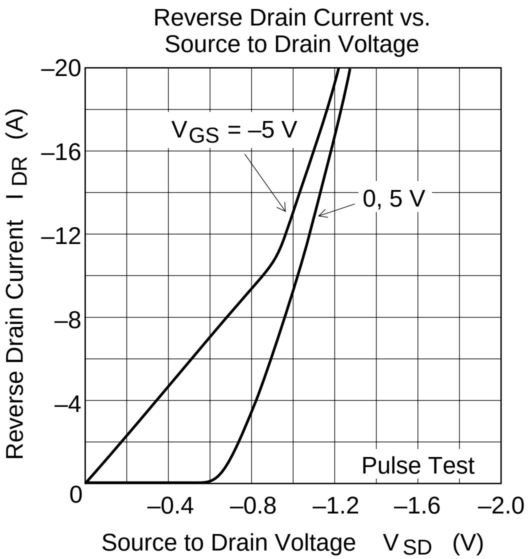

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
75 °C
25 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs| (S)
50
20
10
5
2
1
0.5
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)


Body–Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.2 –0.5 –1 –2 –5 –10 –20
Reverse Drain Current I DR (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 –40 –50
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–10
–20
–30
–40
–50
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
VDD = –5 V
–10 V
–25 V
VDS
VGS
VDD = –25 V
–10 V
–5 V
I D = –3.5 A
0 8 16 24 32 40
Gate Charge Qg (nc)

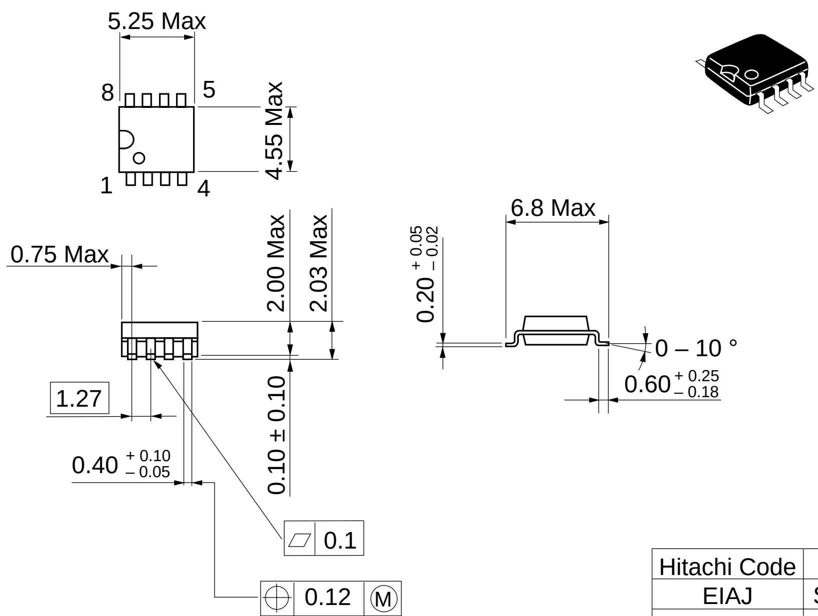

Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≦ 1 %
t r
t f
t d(off)
t d(on)
–0.2 –0.5 –1 –2 –5 –10 –20
Drain Current I D (A)



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1006F

Silicon P Channel Power MOS FET

HITACHI

1st. Edition
Apr. 1995

Application

Power switching

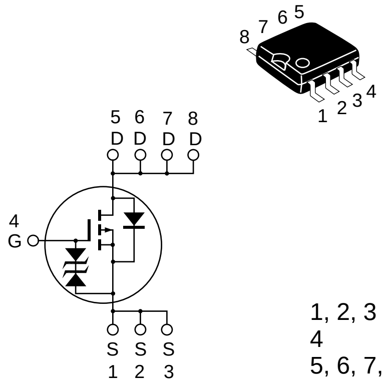
Features

- Low on–resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2.5	A
Drain peak current	$I_{D(pulse)}$*	–10	A
Body–drain diode reverse drain current	I_{DR}	–2.5	A
Channel dissipation	Pch**	1.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

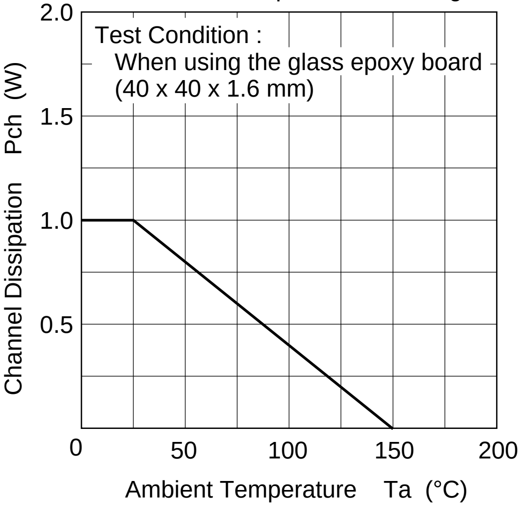
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

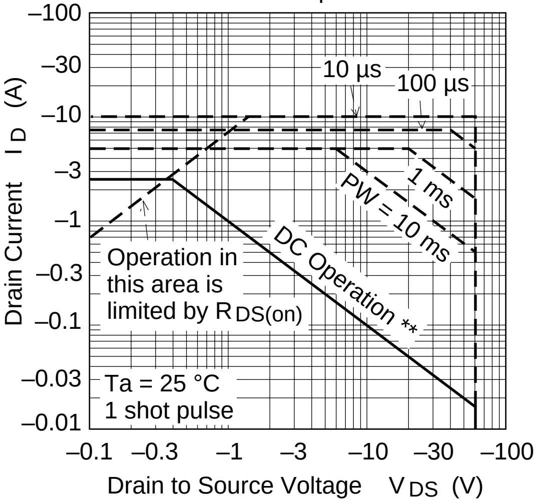
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.25	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.14	Ω	I_D = –2 A V_{GS} = –10 V *
		—	0.14	0.2	Ω	I_D = –2 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	5.5	—	S	I_D = –2 A V_{DS} = - 10 V *
Input capacitance	Ciss	—	910	—	pF	V_{DS} = - 10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	170	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	35	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	190	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	105	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.8	—	V	I_F = –2.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	130	—	ns	I_F = –2.5 A, V_{GS} = 0 diF / dt = 20A / µs

* Pulse Test

Power vs. Temperature Derating

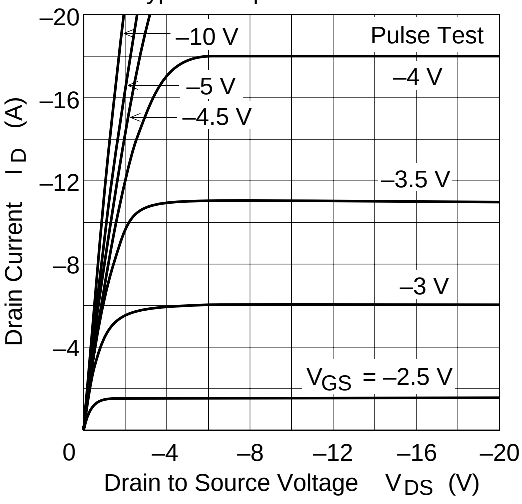


Maximum Safe Operation Area

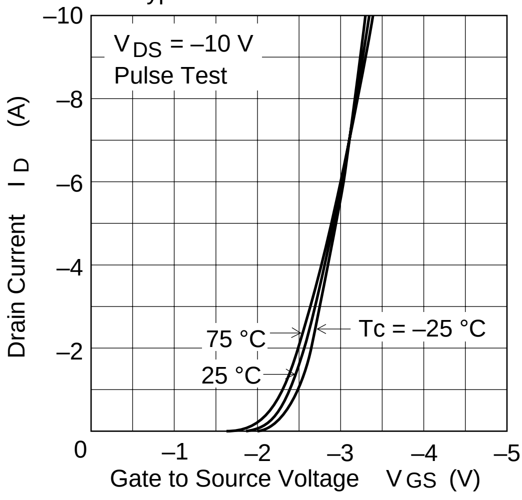


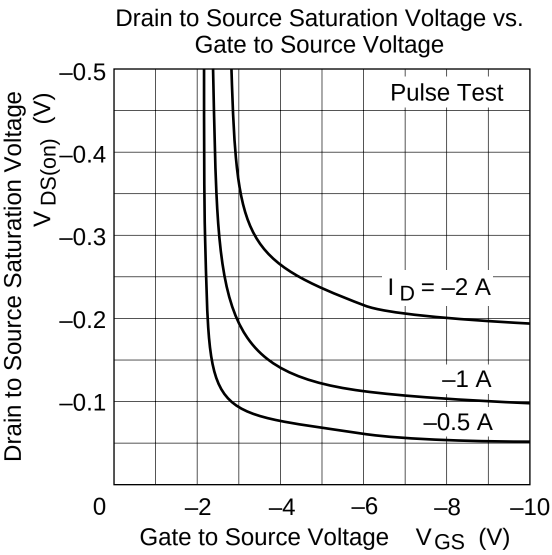
** When using the glass epoxy board (40 x 40 x 1.6 mm)

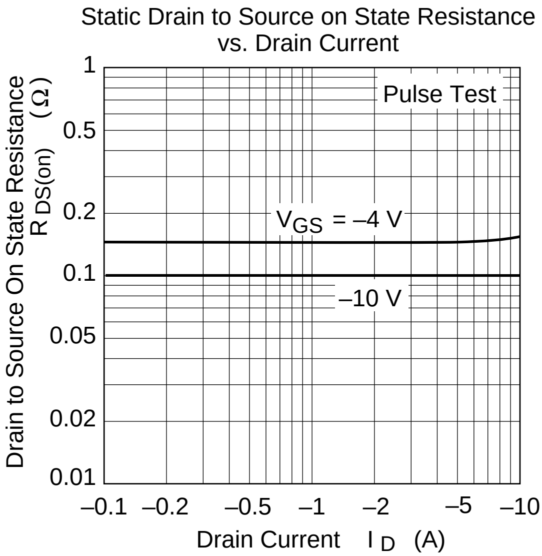
Typical Output Characteristics

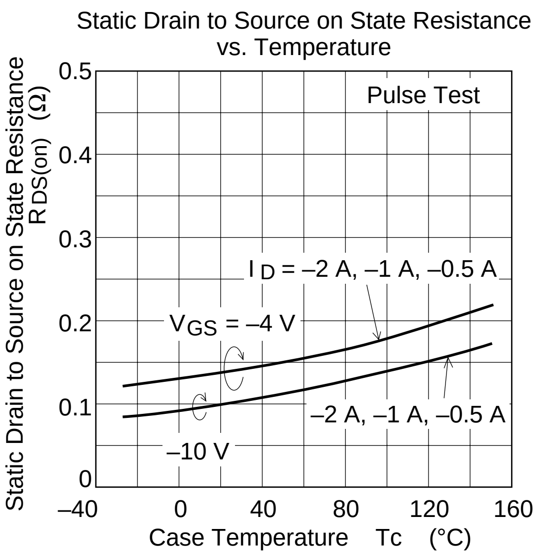


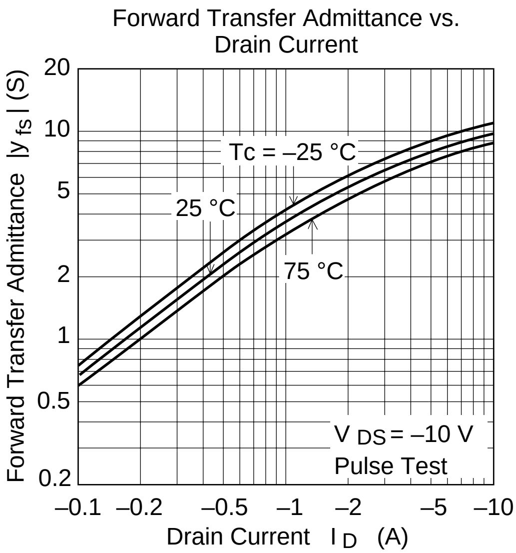
Typical Transfer Characteristics

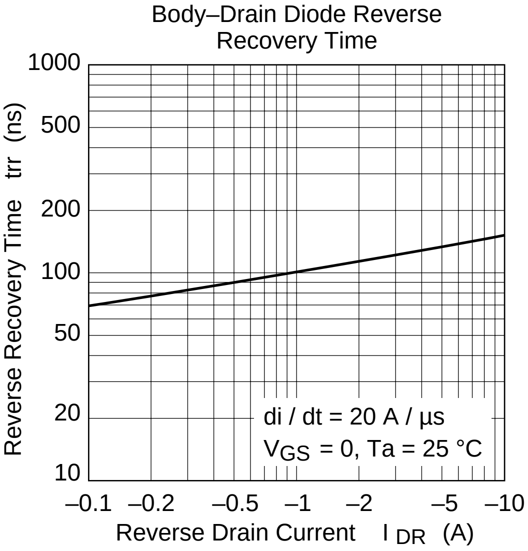


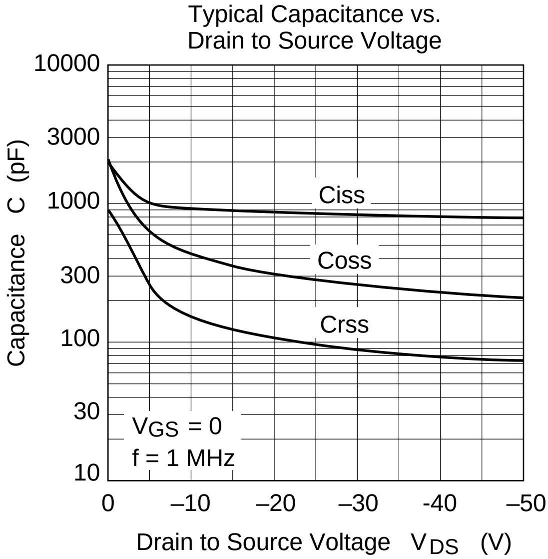

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –2 A
–1 A
–0.5 A
Drain to Source Saturation Voltage V DS(on) (V)
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

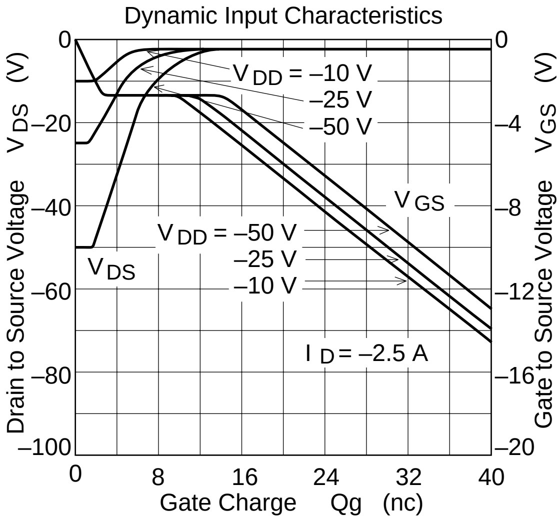

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
VGS = –4 V
–10 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

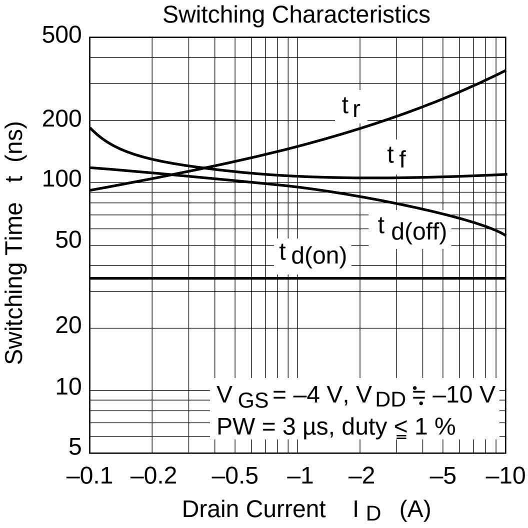

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –2 A, –1 A, –0.5 A
VGS = –4 V
–2 A, –1 A, –0.5 A
–10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

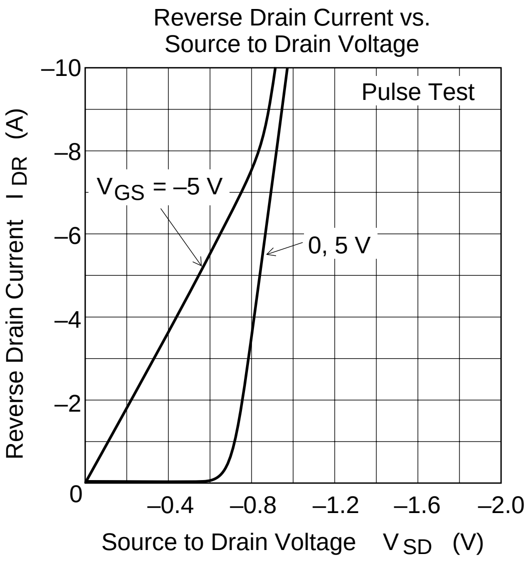

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs | (S)
20
10
5
2
1
0.5
0.2
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.2 –0.5 –1 –2 –5 –10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 -40 –50
Drain to Source Voltage VDS (V)

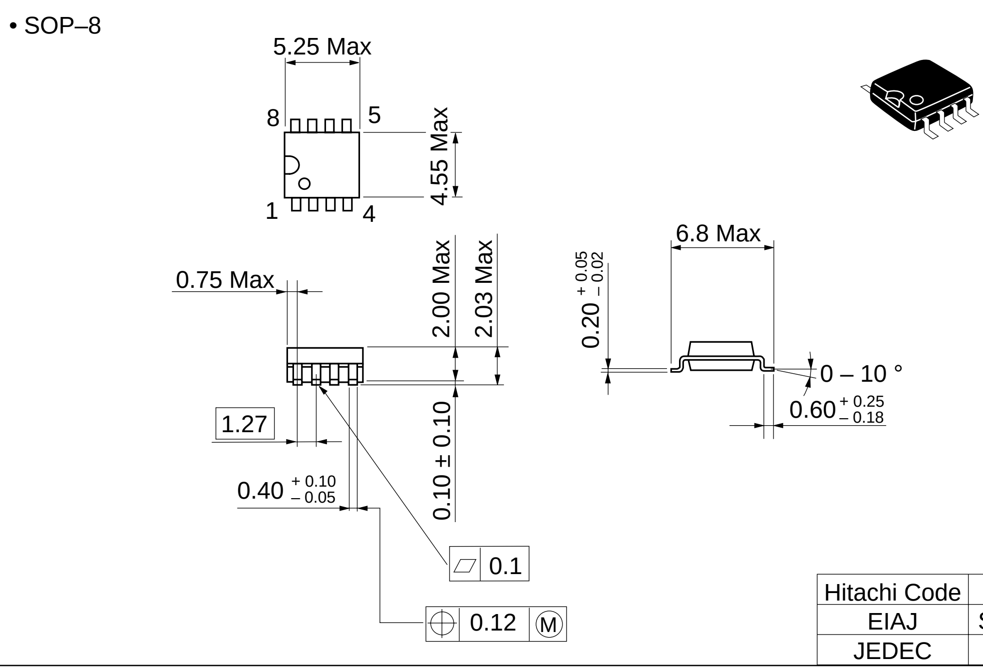

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–20
–40
–60
–80
–100
Gate to Source Voltage VGS (V)
0
–4
–8
–12
–16
–20
V DD = –10 V
–25 V
–50 V
VGS
V DD = –50 V
–25 V
–10 V
VDS
I D = –2.5 A
0 8 16 24 32 40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t r
t f
t d(off)
t d(on)
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≦ 1 %
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1007F

Silicon P Channel Power MOS FET

HITACHI

4th. Edition
Apr. 1995

Application

Power switching
Synchronously Rectifier

Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

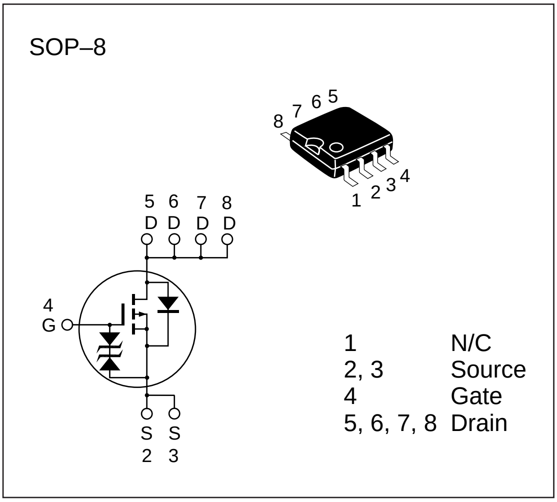


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–3.5	A
Drain peak current	$I_{D(pulse)}$*	–15	A
Body–drain diode reverse drain current	I_{DR}	–3.5	A
Channel dissipation	Pch**	1.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

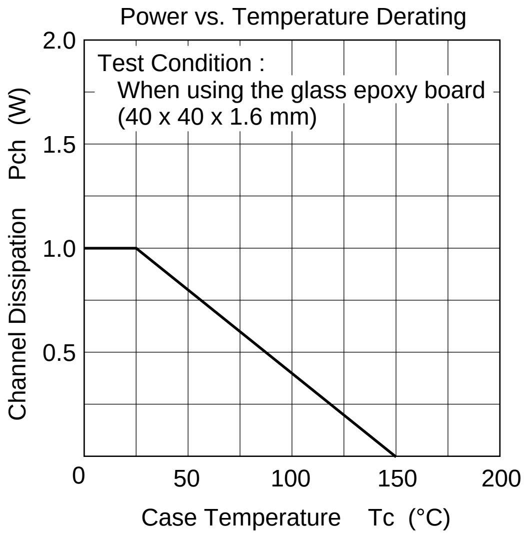
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

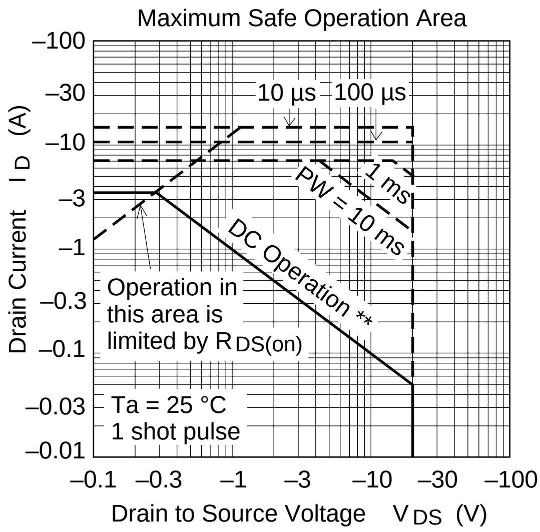
Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

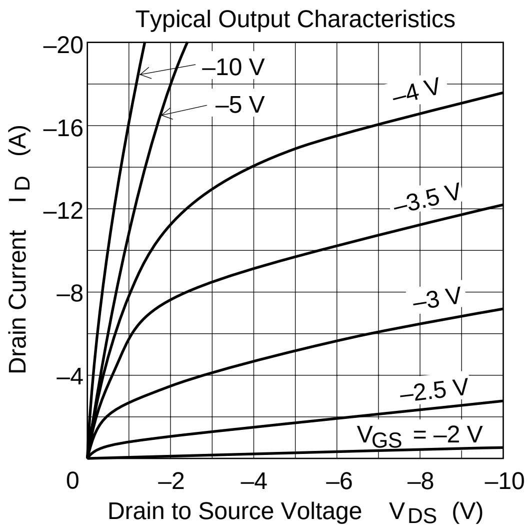
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.08	Ω	I_D = –2 A V_{GS} = –10 V *
		—	0.1	0.15	Ω	I_D = –2 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	730	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	680	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	250	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	28	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	165	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	45	—	ns	
Fall time	t_f	—	95	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	75	—	ns	I_F = –3.5 A, V_{GS} = 0 diF / dt = 20A / µs

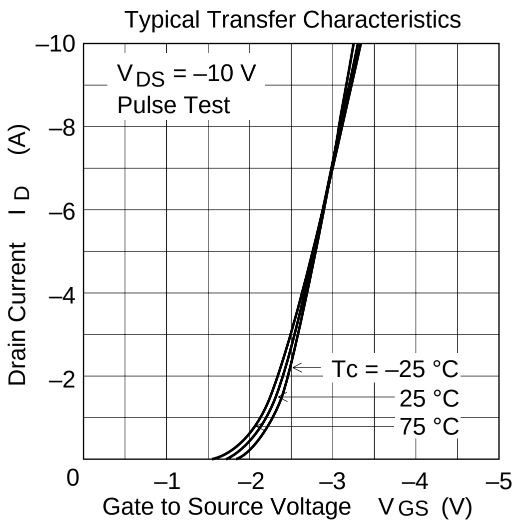
* Pulse Test

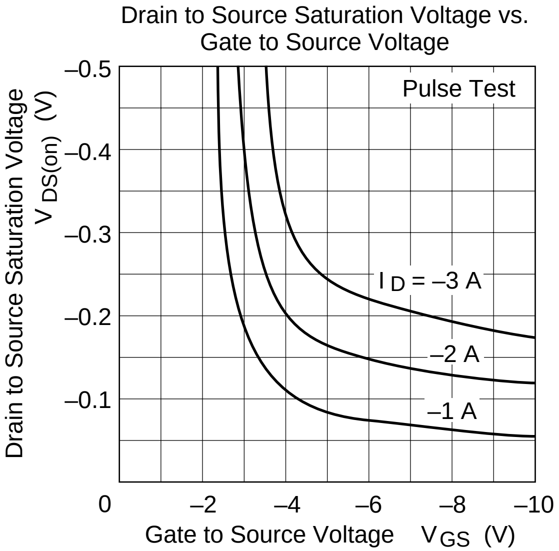


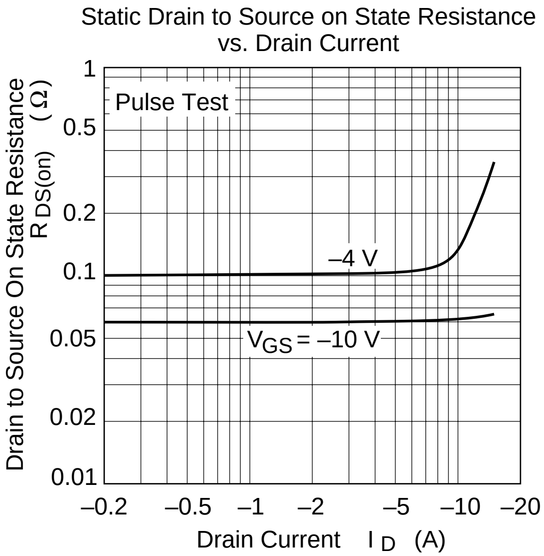


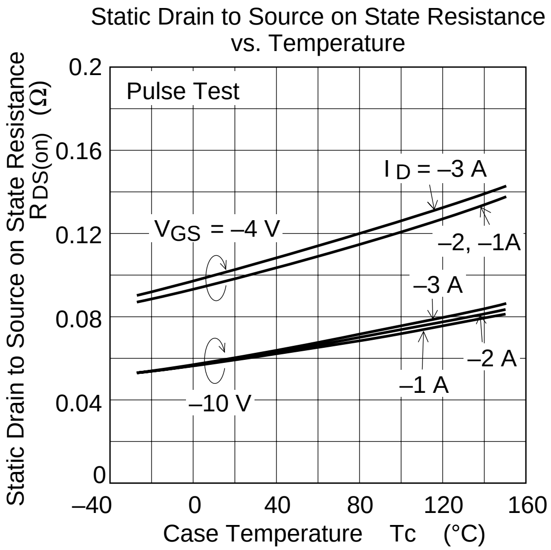
** When using the glass epoxy board (40 x 40 x 1.6 mm)

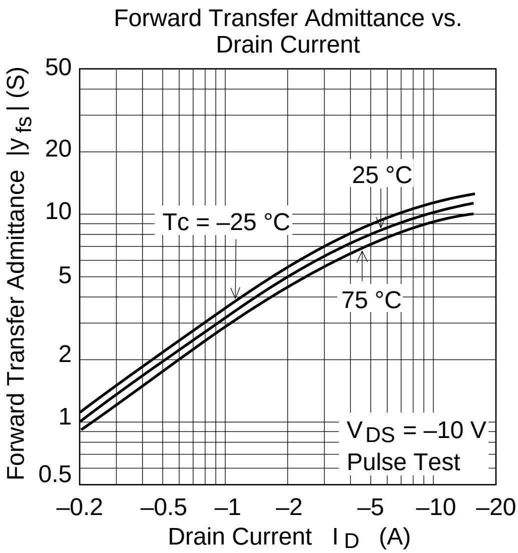


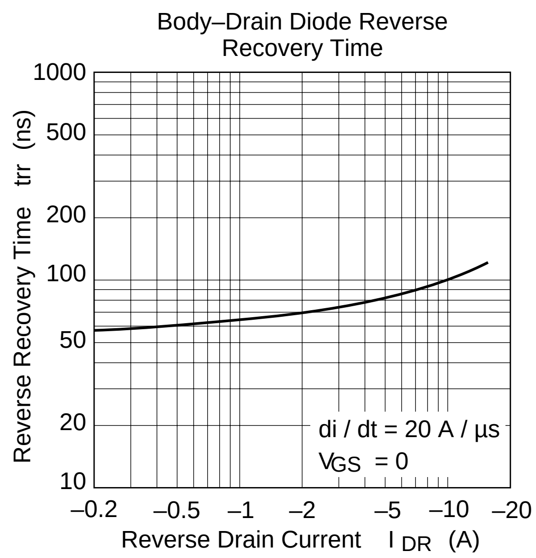


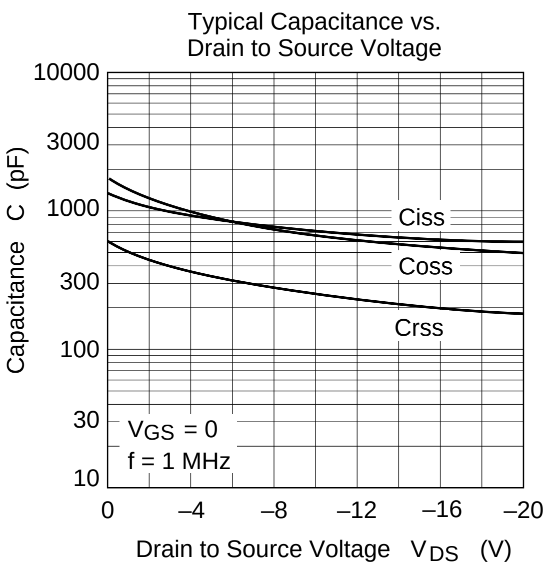

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –3 A
–2 A
–1 A
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)
Drain to Source Saturation Voltage V DS(on) (V)

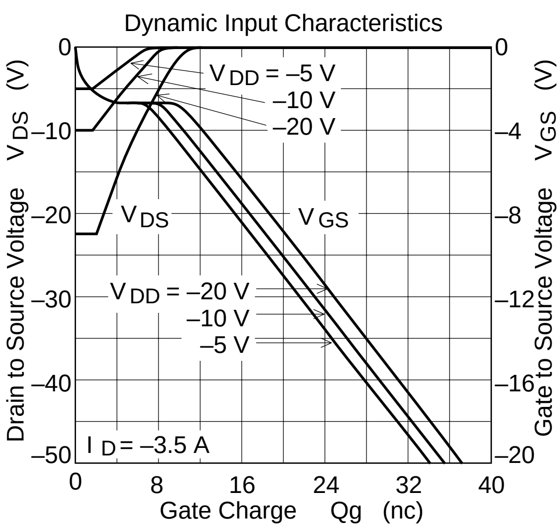

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
–4 V
VGS = –10 V
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)
Drain to Source On State Resistance R DS(on) (Ω)

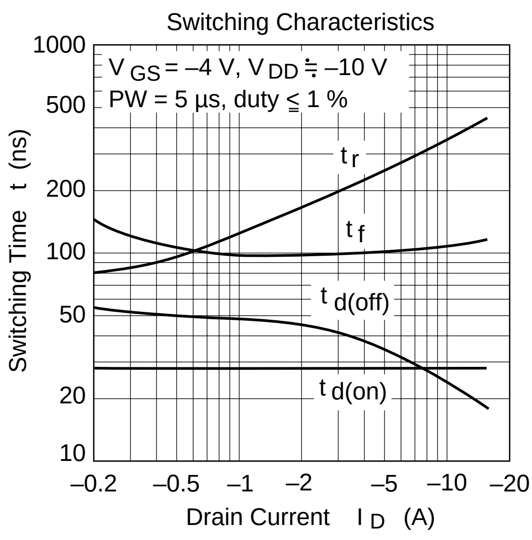

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –3 A
–2, –1A
VGS = –4 V
–3 A
–2 A
–1 A
–10 V
0.2
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)
Static Drain to Source on State Resistance R DS(on) (Ω)

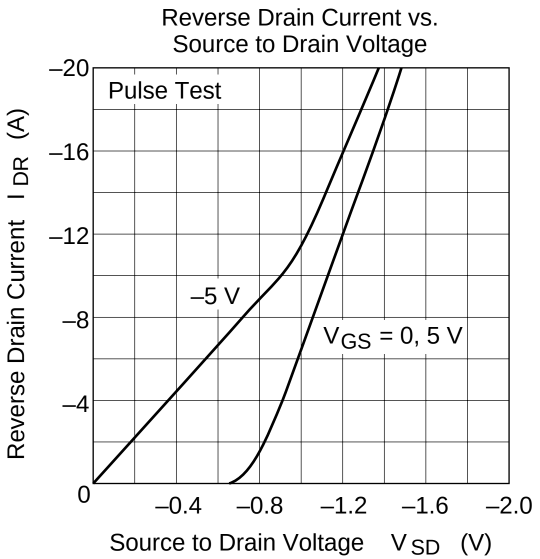

Forward Transfer Admittance vs.
Drain Current
25 °C
Tc = –25 °C
75 °C
V DS = –10 V
Pulse Test
50
20
10
5
2
1
0.5
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)
Forward Transfer Admittance |y fs | (S)


Body–Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0
–0.2
–0.5
–1
–2
–5
–10
–20
Reverse Drain Current I DR (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
–4
–8
–12
–16
–20
Drain to Source Voltage VDS (V)

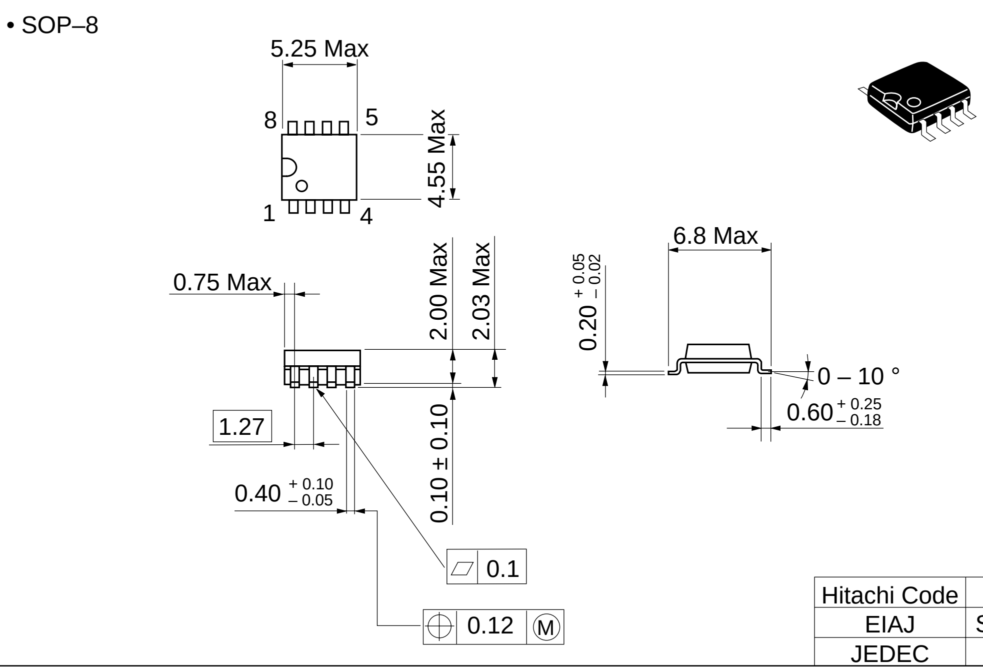

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
0
–10
–20
–30
–40
–50
–4
–8
–12
–16
–20
V DD = –5 V
–10 V
–20 V
V DS
V GS
V DD = –20 V
–10 V
–5 V
I D = –3.5 A
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
V GS = –4 V, V DD ≒ –10 V
PW = 5 µs, duty ≤ 1 %
t r
t f
t d(off)
t d(on)
–0.2
–0.5
–1
–2
–5
–10
–20
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1008F

Silicon P Channel Power MOS FET

HITACHI

1st. Edition
Apr. 1995

Application

Power switching
Synchronously Rectifier

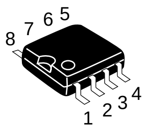
Features

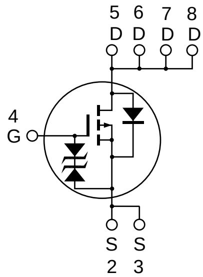
- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8





1	N/C
2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

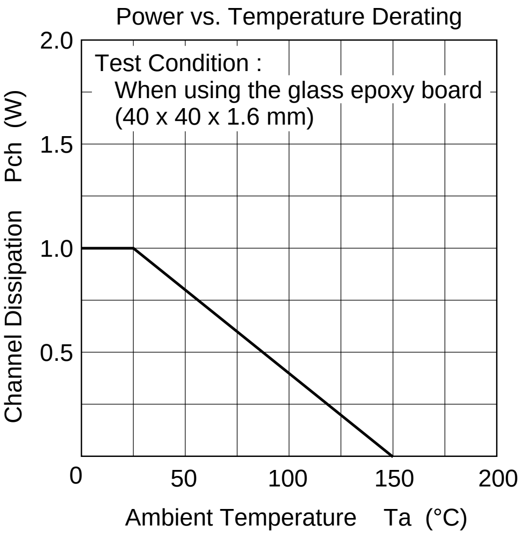
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2.5	A
Drain peak current	$I_{D(pulse)}$*	–10	A
Body–drain diode reverse drain current	I_{DR}	–2.5	A
Channel dissipation	Pch**	1.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

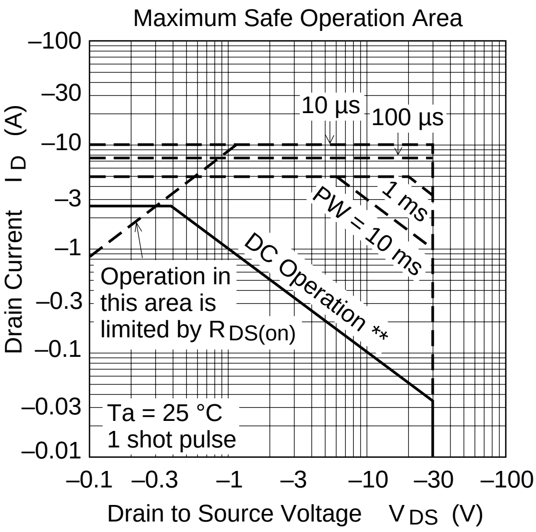
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

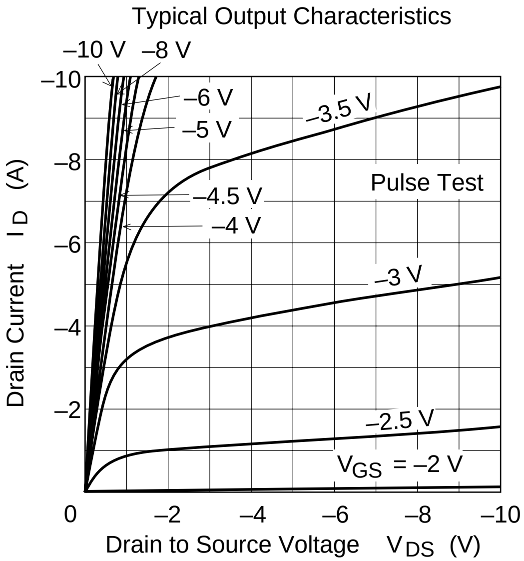
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.12	Ω	I_D = –2 A V_{GS} = –10 V *
		—	0.12	0.2	Ω	I_D = –2 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	4.5	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	670	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	495	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	165	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	24	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	155	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –2.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	75	—	ns	I_F = –2.5 A, V_{GS} = 0 diF / dt = 20A / µs

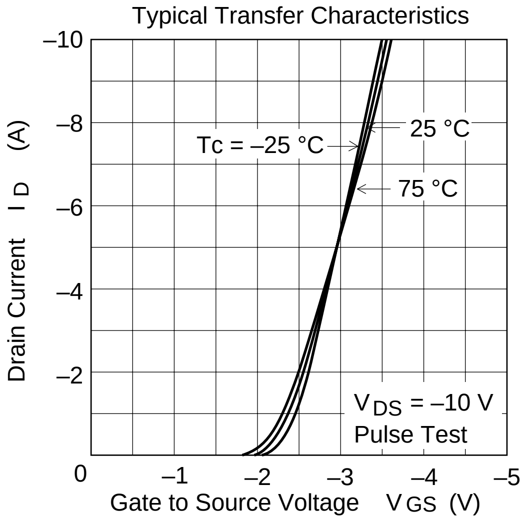
* Pulse Test

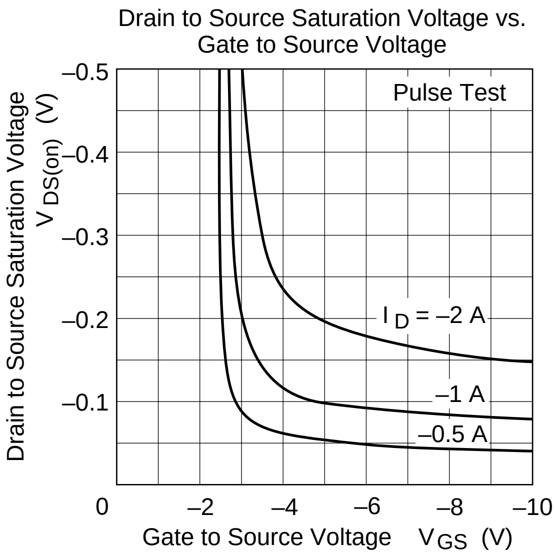


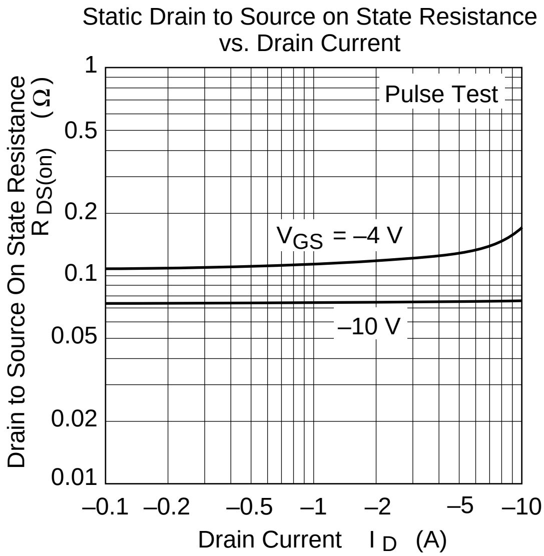


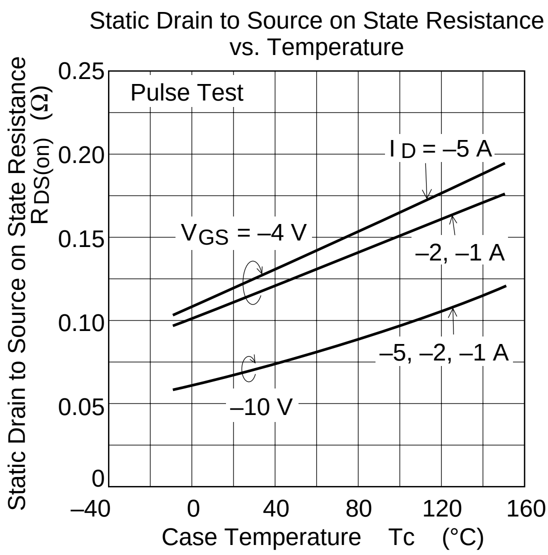
** When using the glass epoxy board (40 x 40 x 1.6 mm)

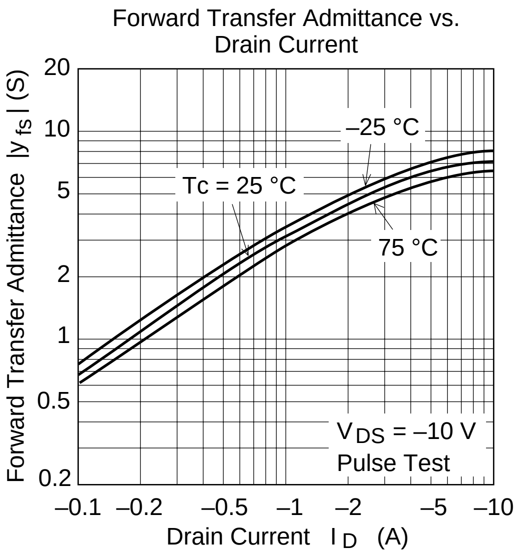


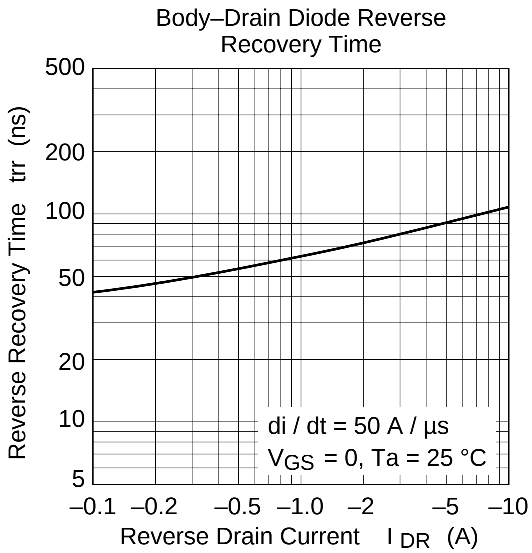


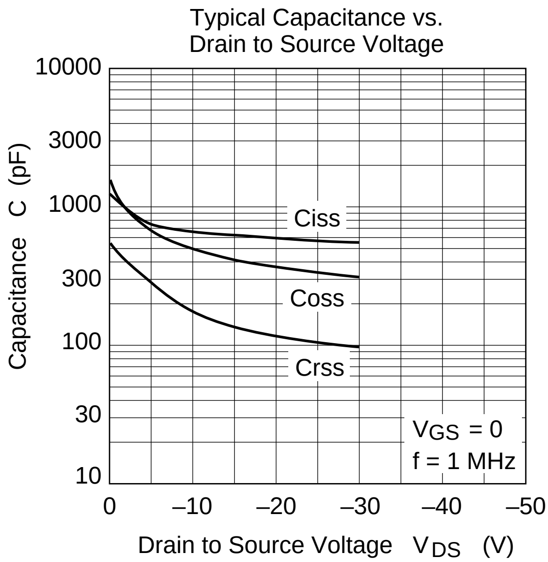

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –2 A
–1 A
–0.5 A
Drain to Source Saturation Voltage V DS(on) (V)
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

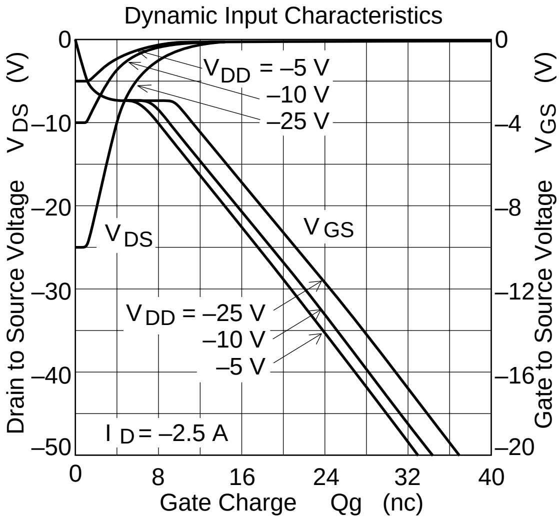

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = –4 V
–10 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

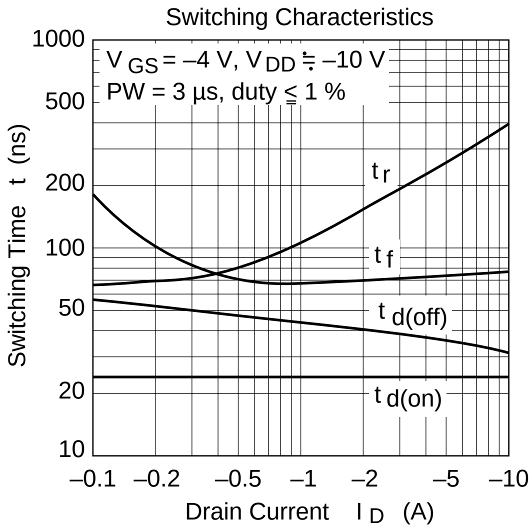

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –5 A
V GS = –4 V
–2, –1 A
–5, –2, –1 A
–10 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.25
0.20
0.15
0.10
0.05
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

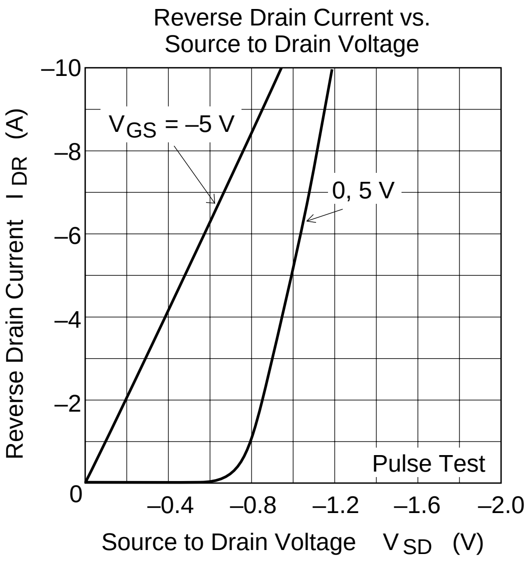

Forward Transfer Admittance vs.
Drain Current
–25 °C
Tc = 25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs| (S)
20
10
5
2
1
0.5
0.2
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.2 –0.5 –1.0 –2 –5 –10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 –40 –50
Drain to Source Voltage VDS (V)

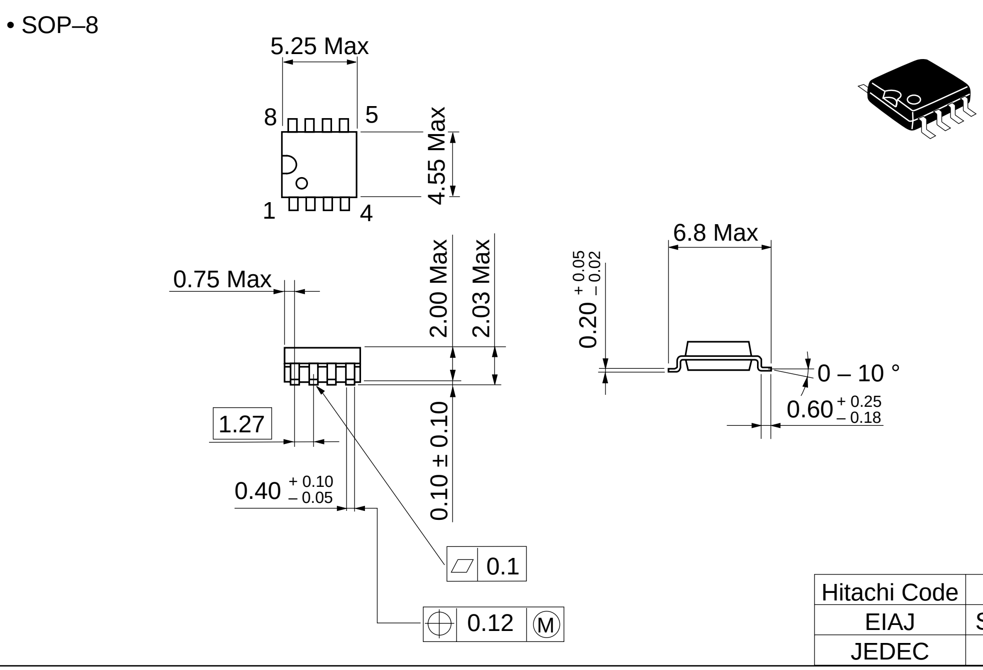

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–10
–20
–30
–40
–50
VDD = –5 V
–10 V
–25 V
VDS
VGS
VDD = –25 V
–10 V
–5 V
I D = –2.5 A
0
–4
–8
–12
–16
–20
Gate to Source Voltage VGS (V)
0 8 16 24 32 40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≦ 1 %
t r
t f
t d(off)
t d(on)
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1009F Target Specification

Silicon P Channel Power MOS FET

HITACHI

2nd. Edition
Jun. 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

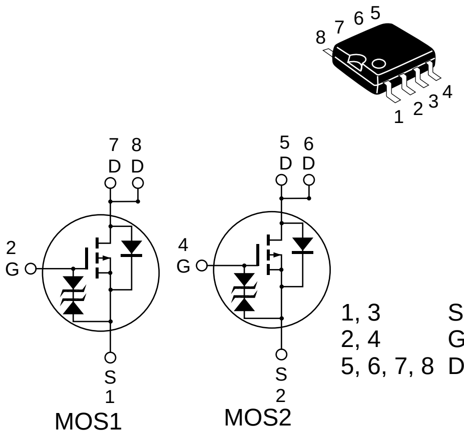


Table 1 Absolute Maximum Ratings (Ta = 25°C)

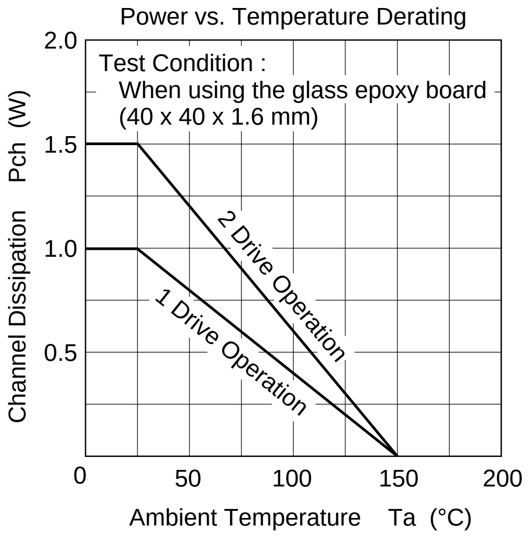
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–2.5	A
Drain peak current	$I_{D(pulse)}$*	–10	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

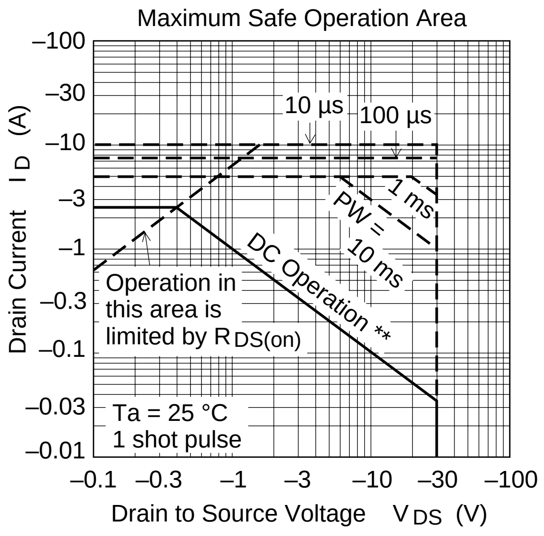
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

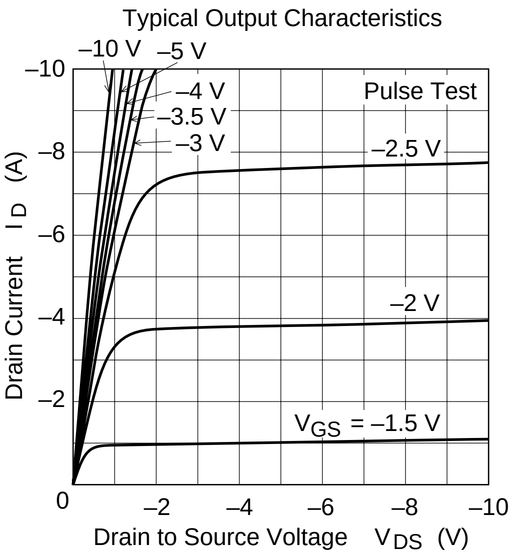
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	I_D = –2 A V_{GS} = –4 V *
		—	0.17	0.24	Ω	I_D = –2 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = –2 A V_{DS} = - 10 V *
Input capacitance	Ciss	—	720	—	pF	V_{DS} = - 10 V
Output capacitance	Coss	—	345	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	115	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	16	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	100	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	120	—	ns	
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –2.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = –2.5A, V_{GS} = 0 diF / dt = 20 A / µs

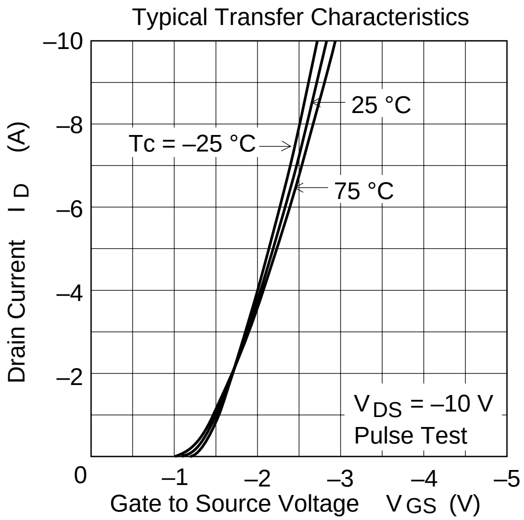
* Pulse Test

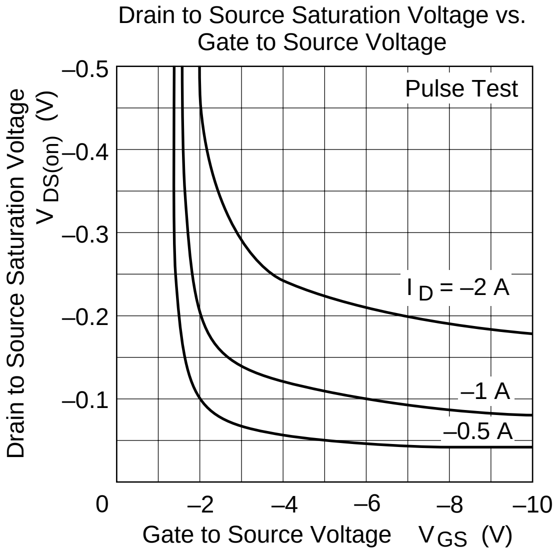


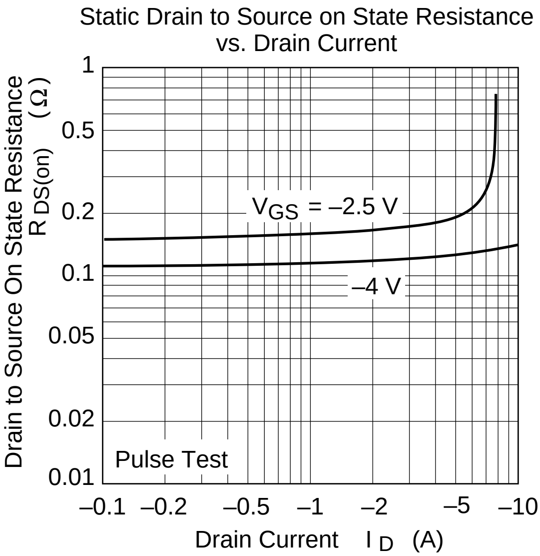


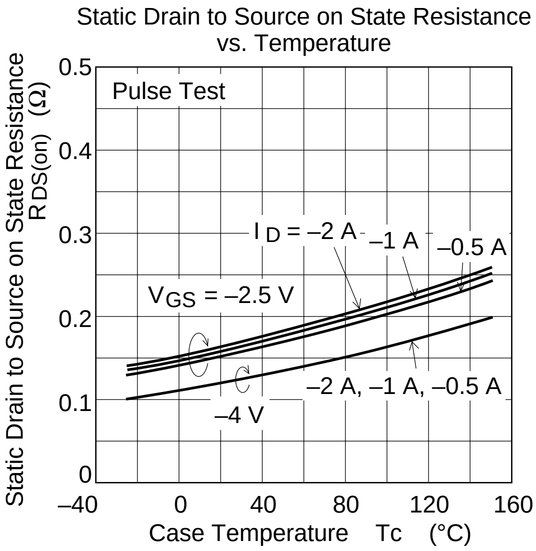
** 1 Drive operation
When using the glass epoxy board
(40 x 40 x 1.6 mm)

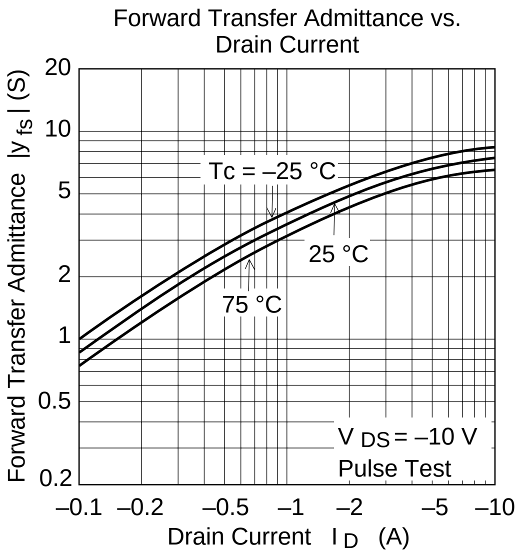


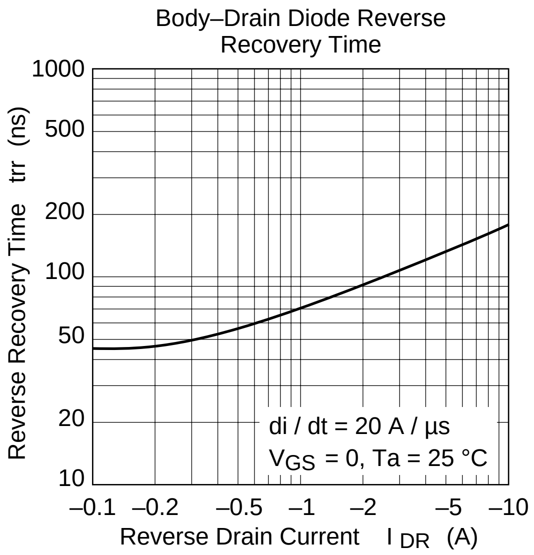


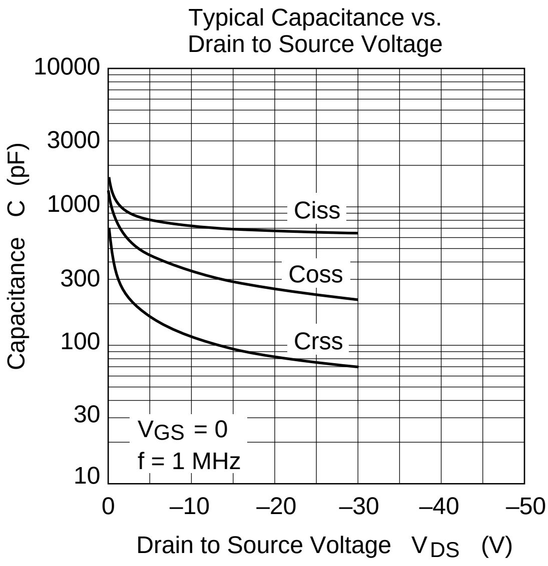

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = –2 A
–1 A
–0.5 A
Drain to Source Saturation Voltage V DS(on) (V)
–0.5
–0.4
–0.3
–0.2
–0.1
0
–2
–4
–6
–8
–10
Gate to Source Voltage V GS (V)

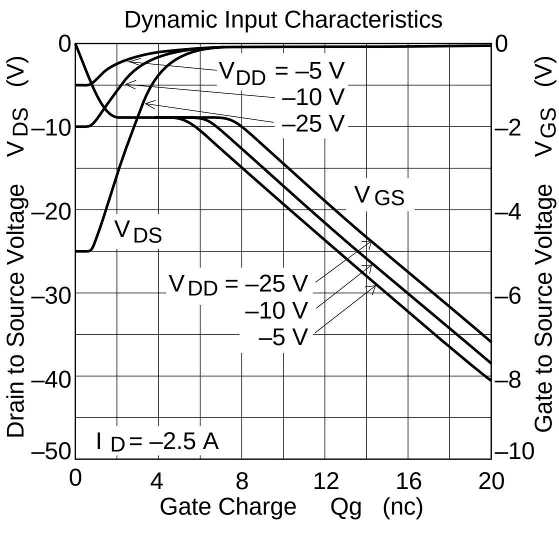

Static Drain to Source on State Resistance
vs. Drain Current
V GS = –2.5 V
–4 V
Pulse Test
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)

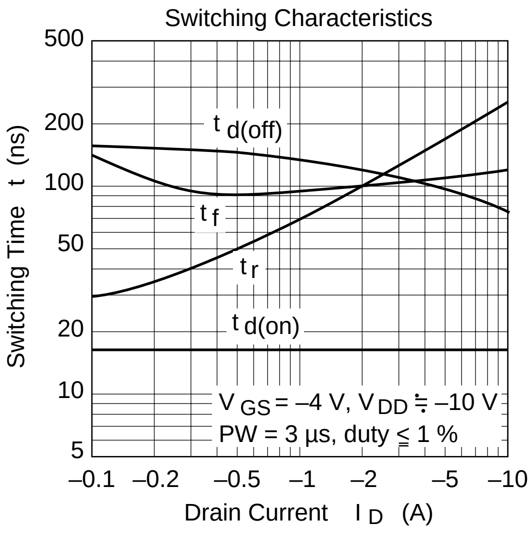

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = –2 A
–1 A
–0.5 A
V GS = –2.5 V
–4 V
–2 A, –1 A, –0.5 A
Static Drain to Source on State Resistance R DS(on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

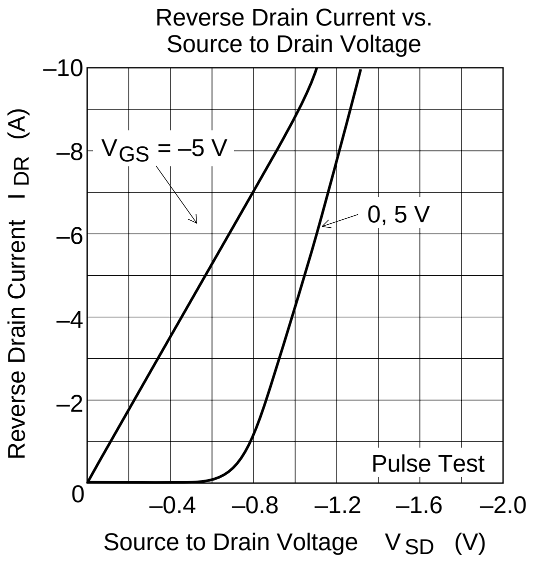

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = –10 V
Pulse Test
Forward Transfer Admittance |y fs| (S)
20
10
5
2
1
0.5
0.2
–0.1
–0.2
–0.5
–1
–2
–5
–10
Drain Current I D (A)


Body–Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
–0.1 –0.2 –0.5 –1 –2 –5 –10
Reverse Drain Current I DR (A)
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0 –10 –20 –30 –40 –50
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

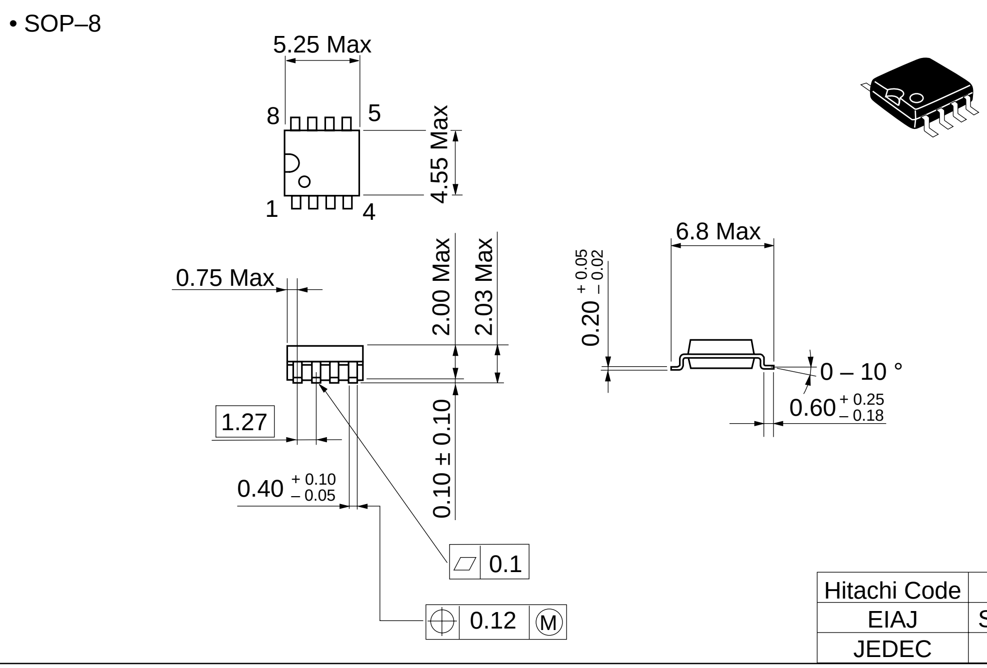

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
0
–10
–20
–30
–40
–50
Gate to Source Voltage VGS (V)
0
–2
–4
–6
–8
–10
0 4 8 12 16 20
Gate Charge Qg (nc)
VDD = –5 V
–10 V
–25 V
VGS
VDS
VDD = –25 V
–10 V
–5 V
I D = –2.5 A


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)
t d(off)
t f
t r
t d(on)
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≦ 1 %



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2001F

Silicon N Channel Power MOS FET

3rd. Edition
Apr. 1995

HITACHI

Application

Power switching

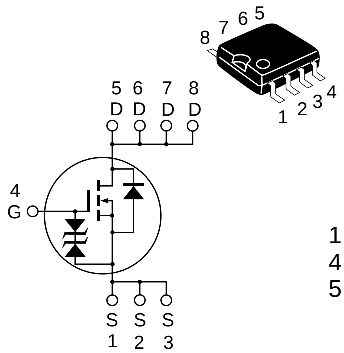
Features

- Low on–resistance
- Capable of2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

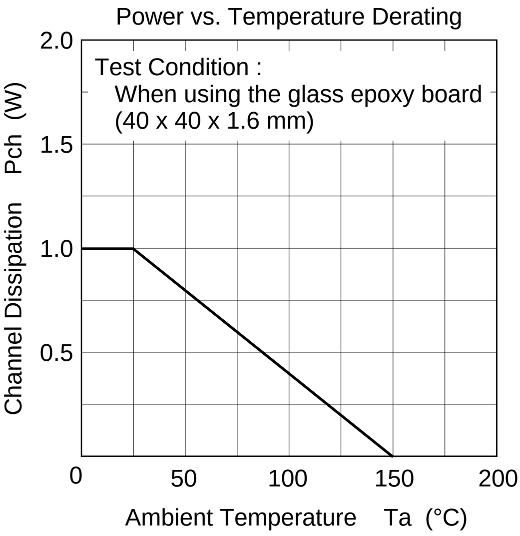
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	20	A
Body–drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

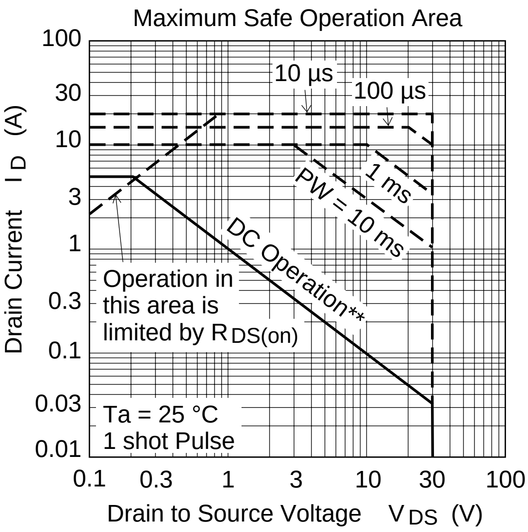
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

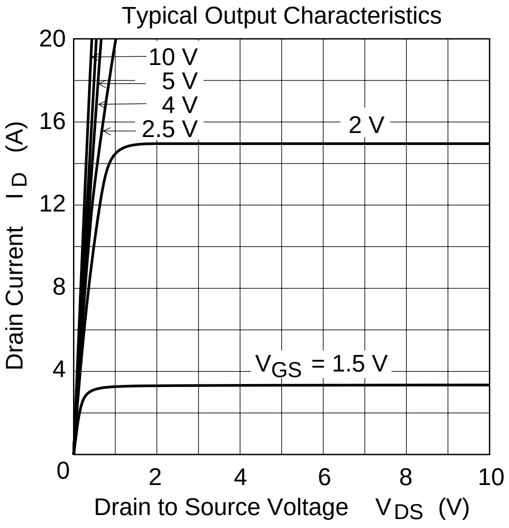
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.035	0.045	Ω	I_D = 3 A V_{GS} = 4V *
		—	0.045	0.06	Ω	I_D = 3 A V_{GS} = 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	7	12	—	S	I_D = 3 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1250	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	540	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	120	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = 4 V, I_D = 3 A
Rise time	t_r	—	100	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	210	—	ns	
Fall time	t_f	—	130	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	I_F = 5A, V_{GS} = 0 diF / dt = 20 A / µs

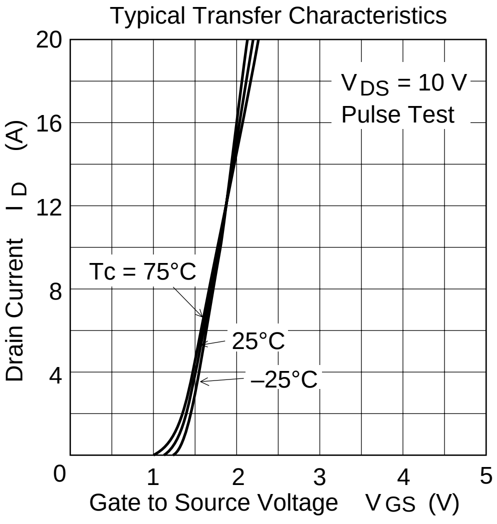
* Pulse Test

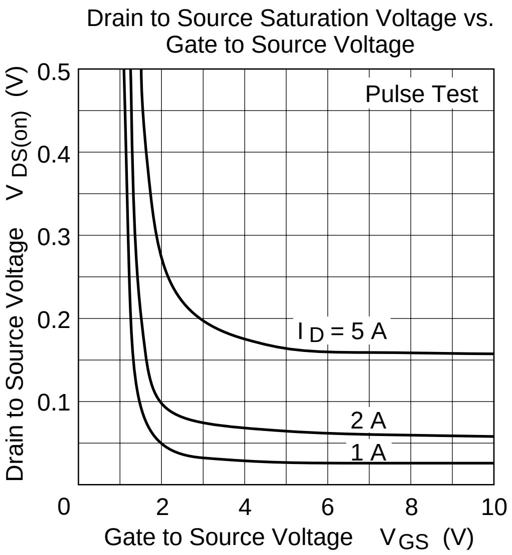


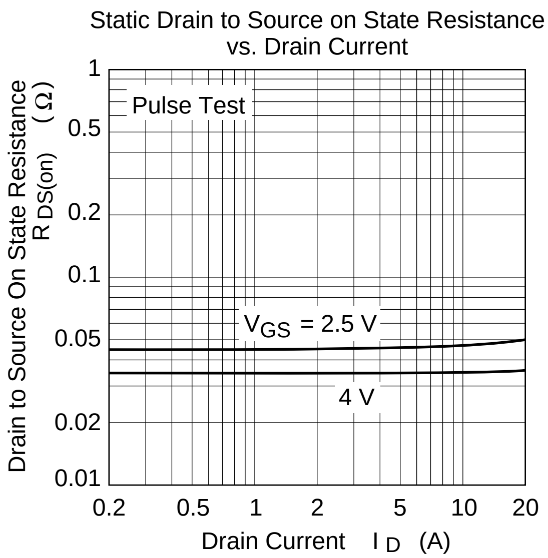


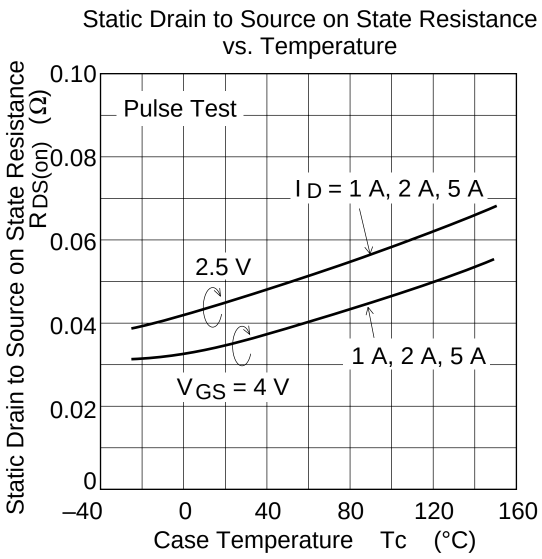
** When using the glass epoxy board (40 x 40 x 1.6 mm)

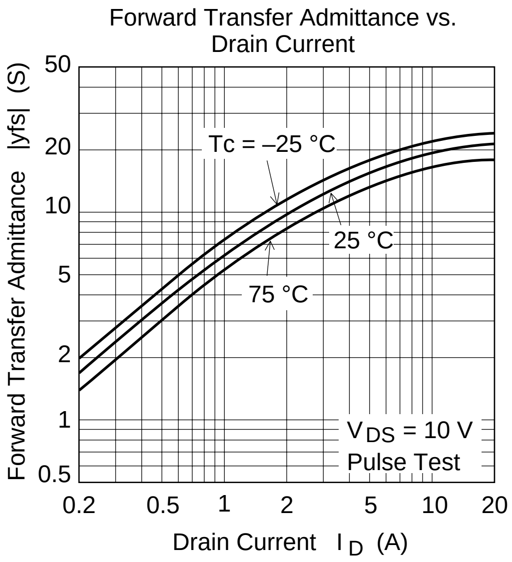


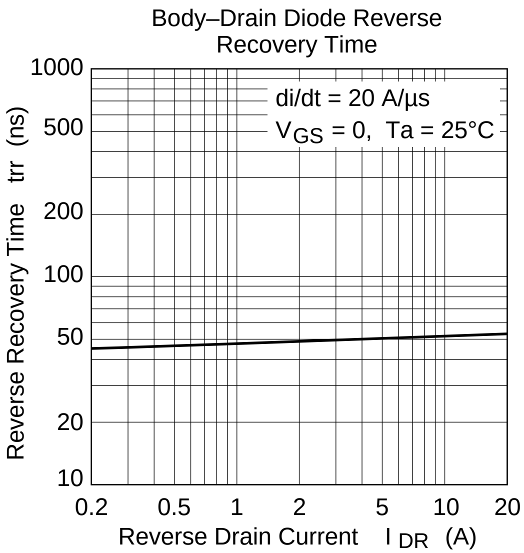


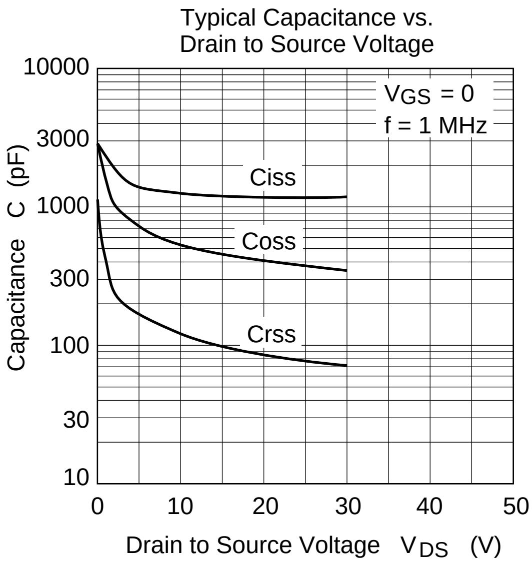

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 5 A
2 A
1 A
Drain to Source Voltage V DS(on) (V)
0.5
0.4
0.3
0.2
0.1
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

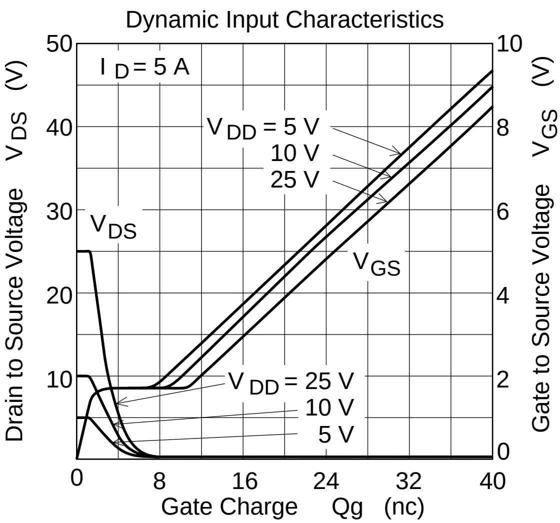

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = 2.5 V
4 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
0.2
0.5
1
2
5
10
20
Drain Current I D (A)

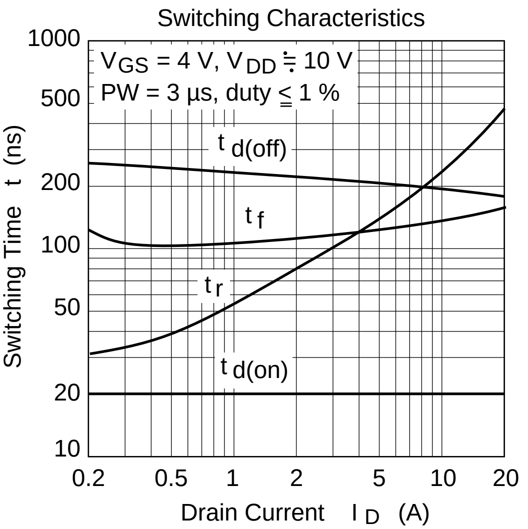

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I D = 1 A, 2 A, 5 A
2.5 V
1 A, 2 A, 5 A
V GS = 4 V
Static Drain to Source on State Resistance R DS(on) (Ω)
0.10
0.08
0.06
0.04
0.02
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

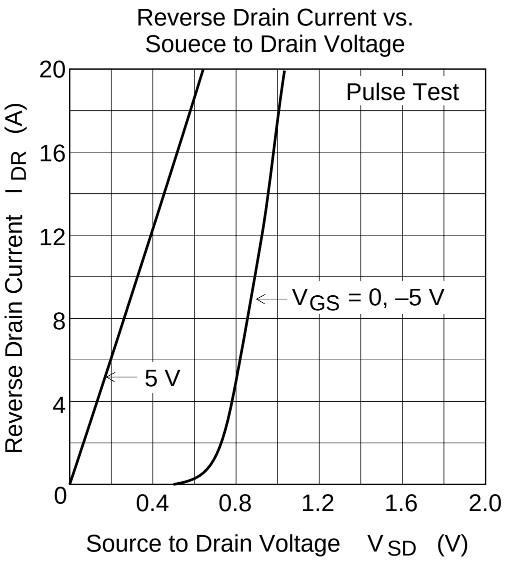

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
V DS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
0.2
0.5
1
2
5
10
20
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
di/dt = 20 A/µs
VGS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

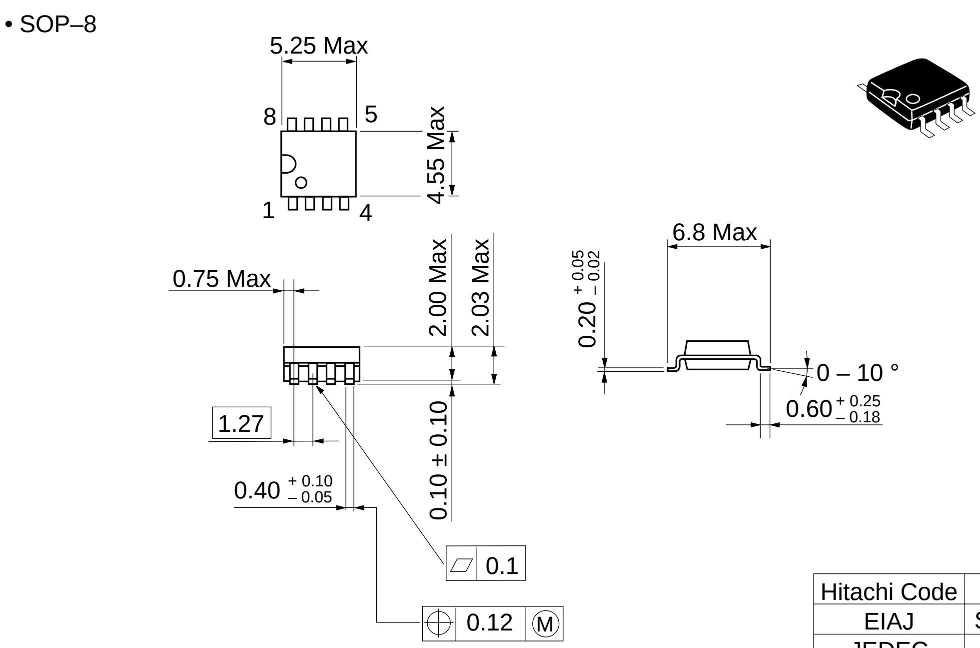

Dynamic Input Characteristics
I D = 5 A
VDD = 5 V
10 V
25 V
VDS
VGS
VDD = 25 V
10 V
5 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
50
40
30
20
10
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
Switching Time t (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2002F

Silicon N Channel Power MOS FET

HITACHI

2nd. Edition
Apr. 1995

Application

Power switching
Synchronously Rectifier

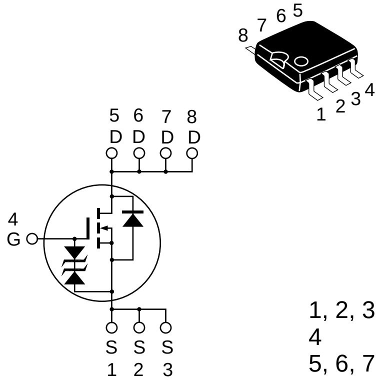
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	20	A
Body–drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

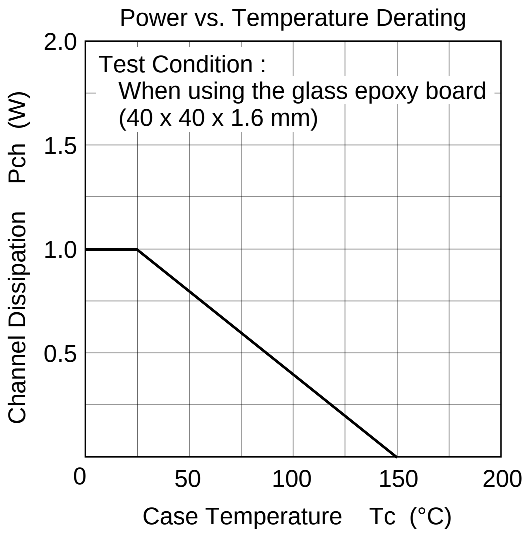
* PW ≤ 10 μs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

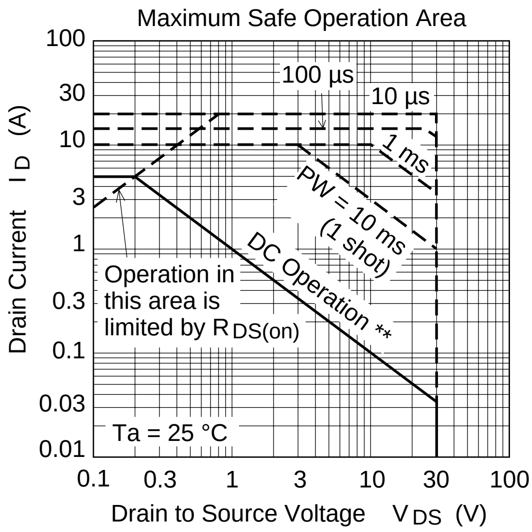
Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

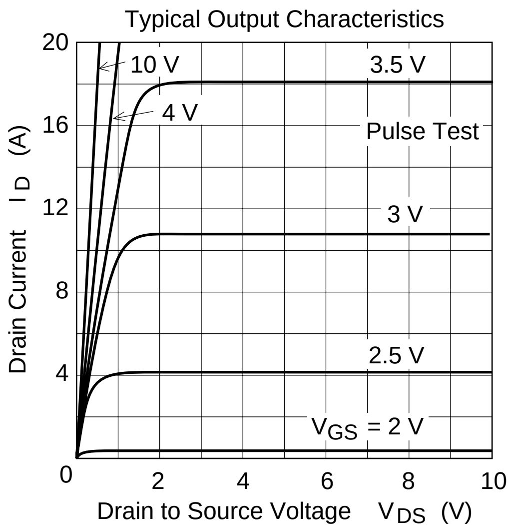
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.03	0.04	Ω	I_D = 3 A V_{GS} = 10V *
		—	0.05	0.06	Ω	I_D = 3 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	8.0	—	S	I_D = 3 A V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	560	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	150	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	V_{GS} = 4 V, I_D = 3 A
Rise time	t_r	—	190	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	75	—	ns	
Fall time	t_f	—	90	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = 5A, V_{GS} = 0 diF / dt = 20 A / µs

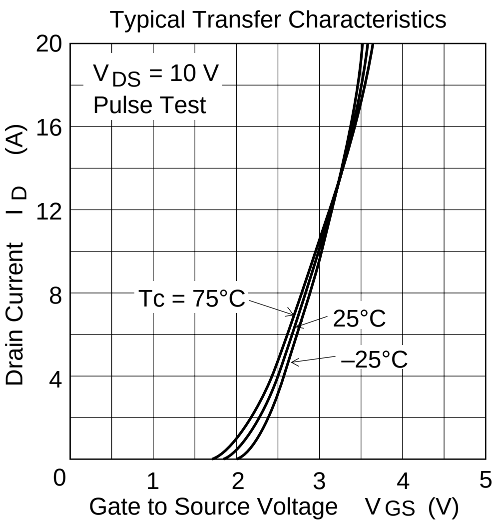
* Pulse Test

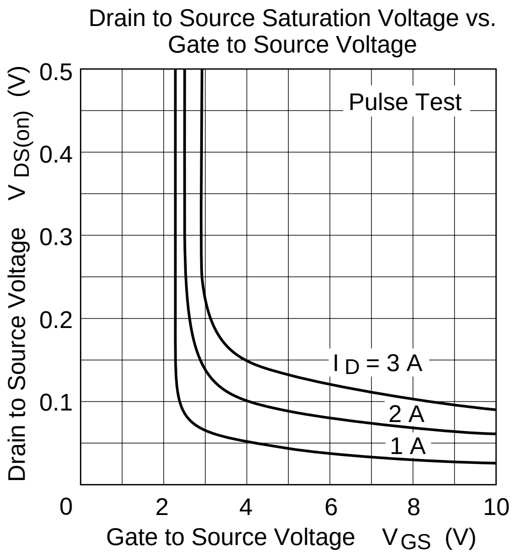


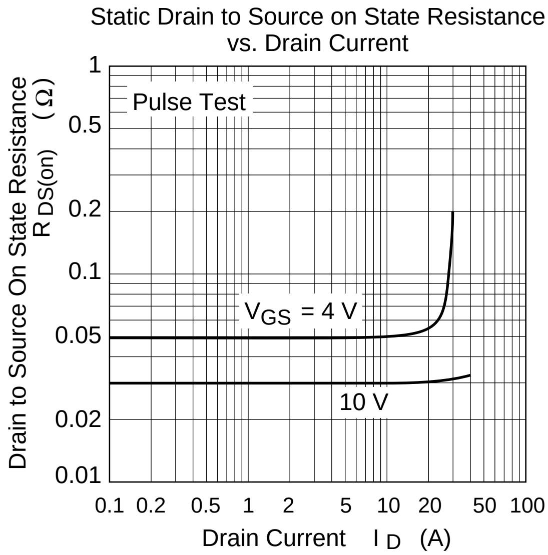


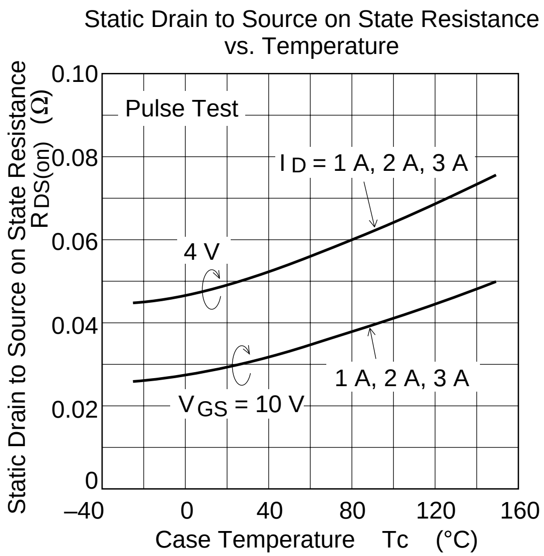
** When using the glass epoxy board
(40 x 40 x 1.6 mm)

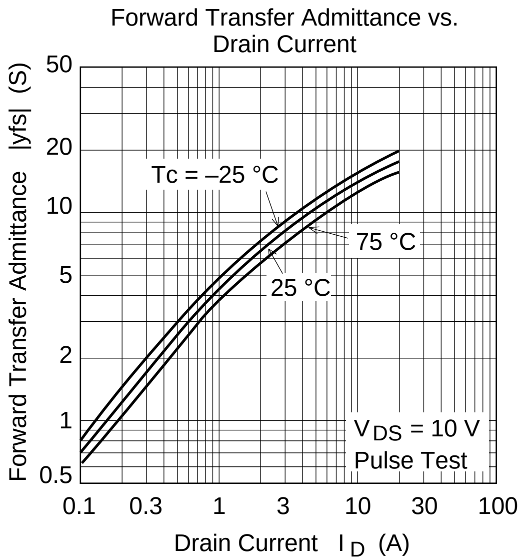


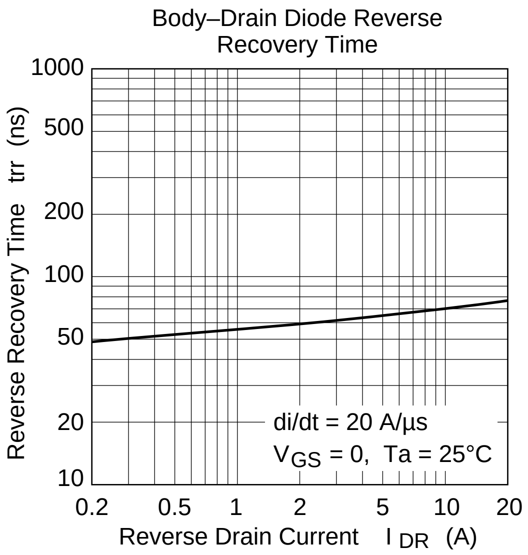


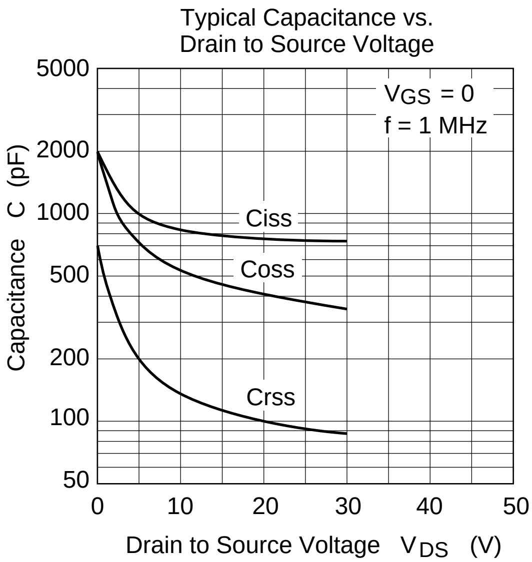

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Voltage V DS(on) (V)
Pulse Test
I D = 3 A
2 A
1 A
0.5
0.4
0.3
0.2
0.1
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

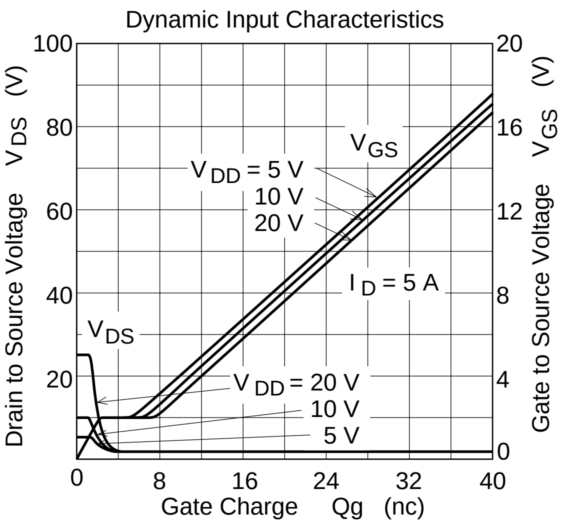

Static Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
Pulse Test
V GS = 4 V
10 V
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1 0.2 0.5 1 2 5 10 20 50 100
Drain Current I D (A)

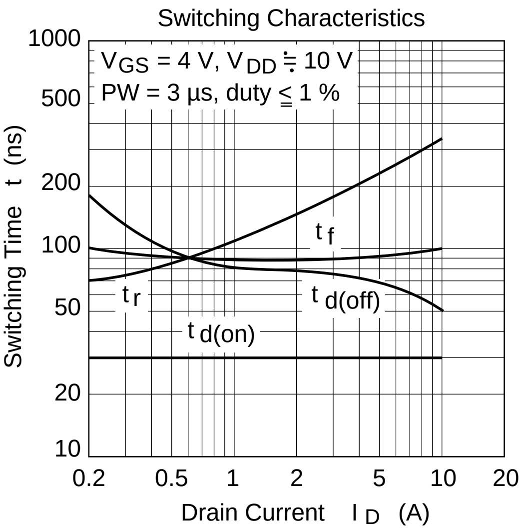

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance R DS(on) (Ω)
Pulse Test
I D = 1 A, 2 A, 3 A
4 V
1 A, 2 A, 3 A
V GS = 10 V
0.10
0.08
0.06
0.04
0.02
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

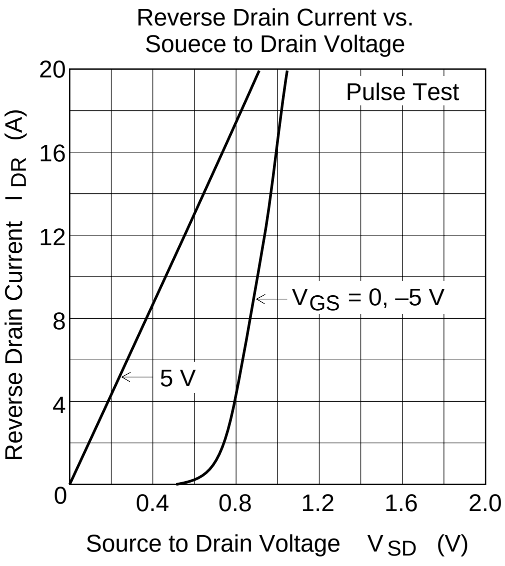

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
Tc = –25 °C
75 °C
25 °C
V DS = 10 V
Pulse Test
50
20
10
5
2
1
0.5
0.1 0.3 1 3 10 30 100
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)
di/dt = 20 A/µs
VGS = 0, Ta = 25°C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
VGS = 0
f = 1 MHz
Ciss
Coss
Crss

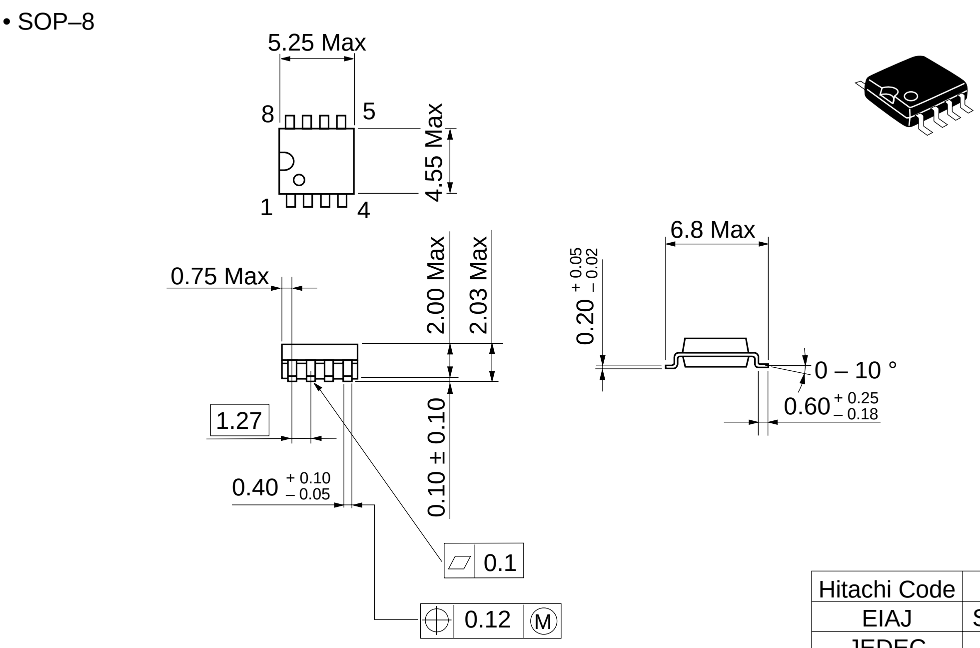

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
100
80
60
40
20
0
8
16
24
32
40
Gate Charge Qg (nc)
VGS
VDD = 5 V
10 V
20 V
ID = 5 A
VDS
VDD = 20 V
10 V
5 V
4
12


Switching Characteristics
Switching Time t (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Drain Current I D (A)
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
t f
t r
t d(off)
t d(on)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2003F

Silicon N Channel Power MOS FET

HITACHI

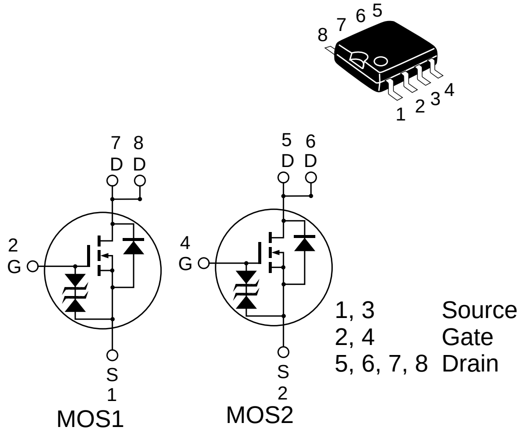
2nd. Edition
Apr. 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting



Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	SC–527–8A
JEDEC Code	—

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	2.5	A
Drain peak current	$I_{D(pulse)}$*	10	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

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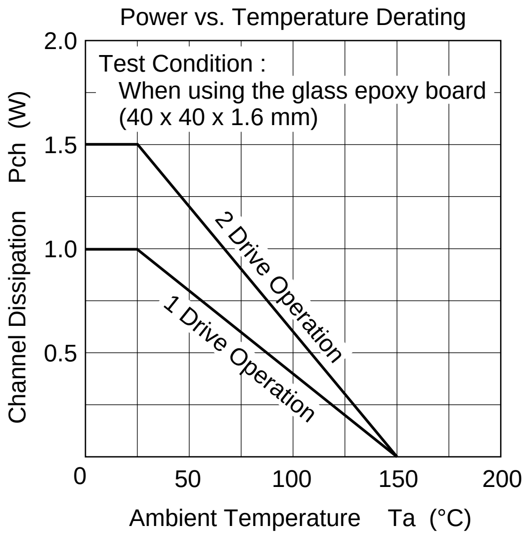
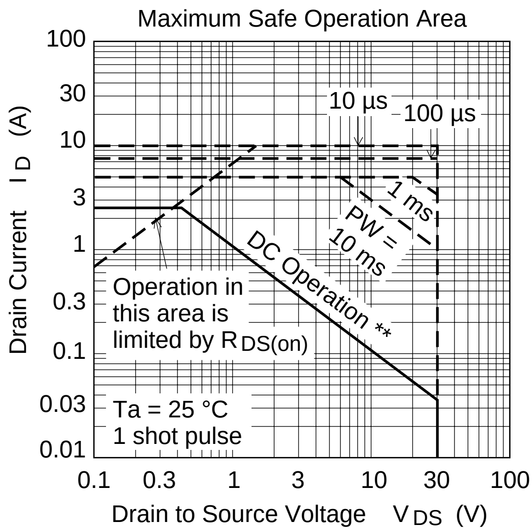
Table 2 Electrical Characteristics (Ta = 25°C)

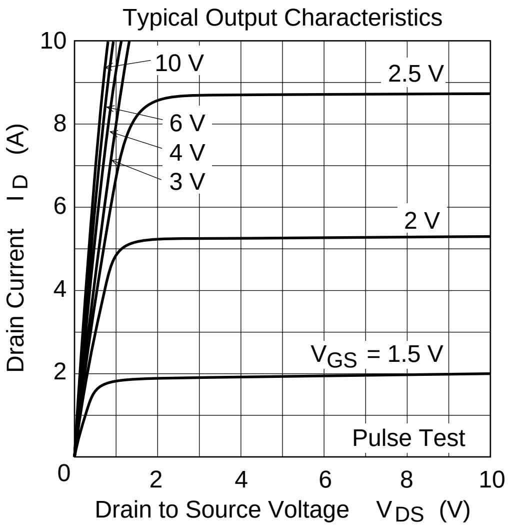
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.15	Ω	I_D = 2A, V_{GS} = 4V *
		—	0.13	0.22	Ω	I_D = 2A, V_{GS} = 2.5V *
Forward transfer admittance	$\|y_{fs}\|$	2	5	—	S	I_D = 2 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	380	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	200	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	70	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	80	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 2.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = 2.5A, V_{GS} = 0, diF / dt = 20 A / µs

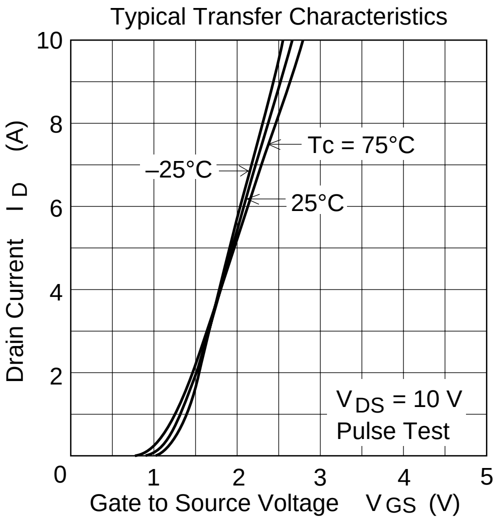
* Pulse Test

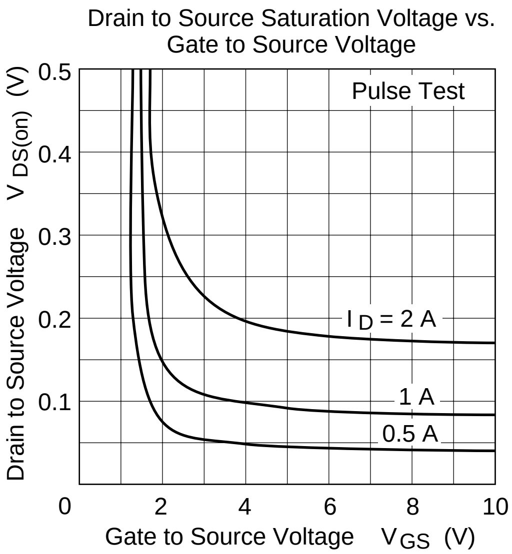


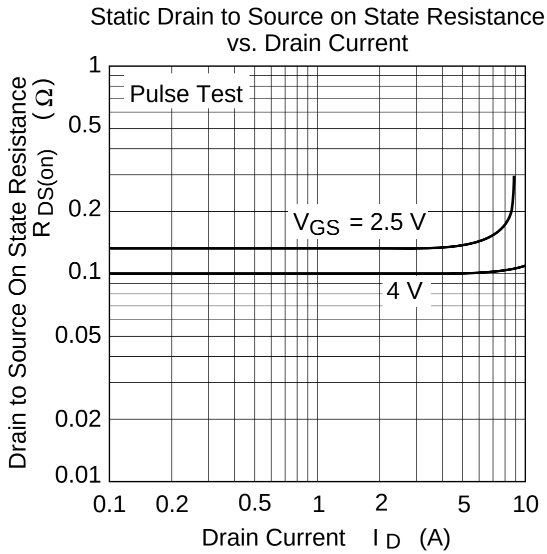


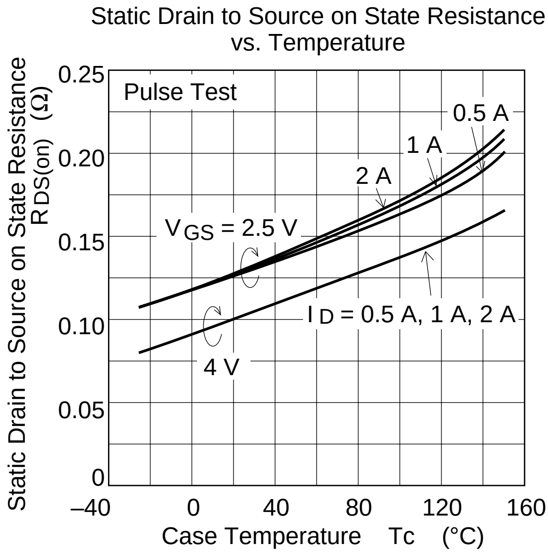
** 1 Drive Operation
When using the glass epoxy board
(40 x 40 x 1.6 mm)

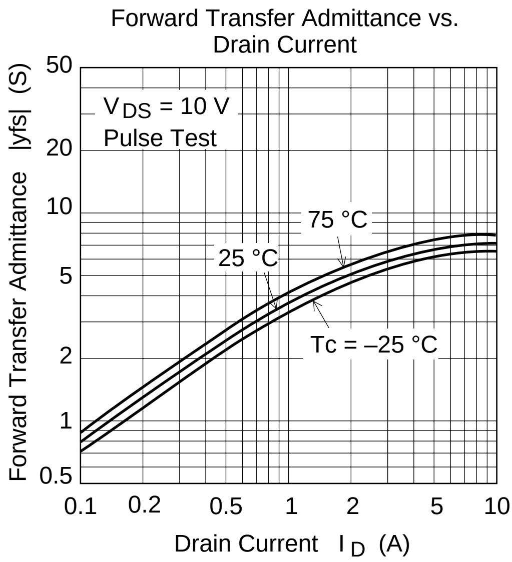


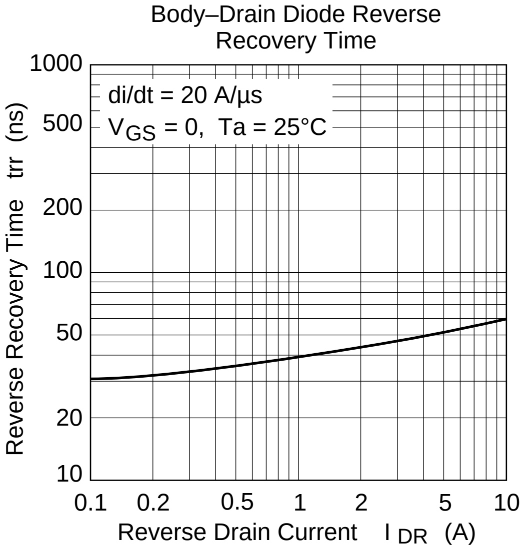


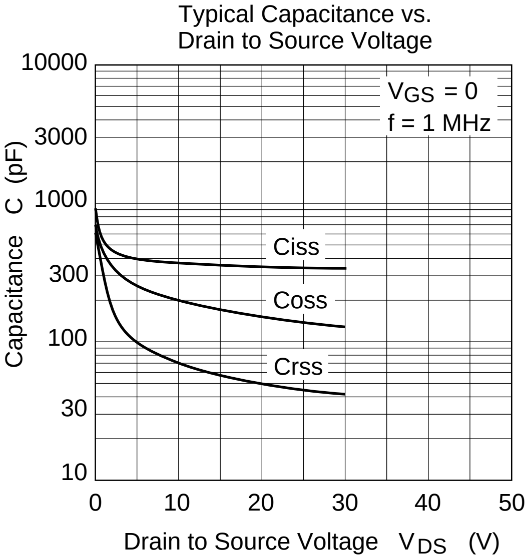

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 2 A
1 A
0.5 A
Drain to Source Voltage V DS(on) (V)
Gate to Source Voltage V GS (V)
0.5
0.4
0.3
0.2
0.1
0
2
4
6
8
10

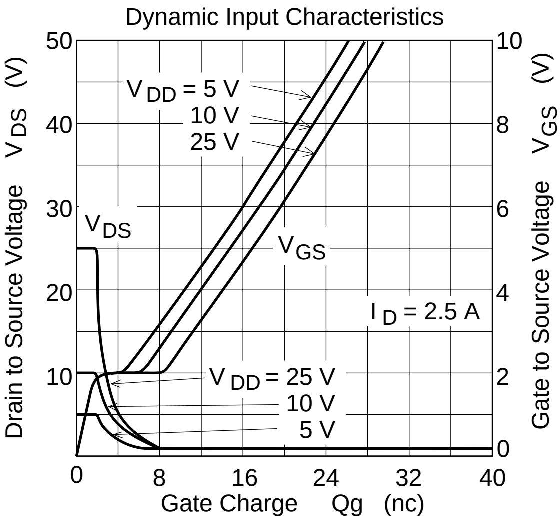

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
V GS = 2.5 V
4 V
Drain to Source On State Resistance R DS(on) (Ω)
Drain Current I D (A)
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1
0.2
0.5
1
2
5
10

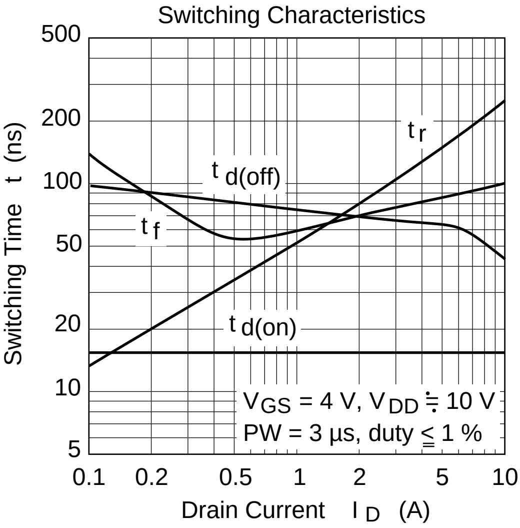

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
0.5 A
1 A
2 A
V GS = 2.5 V
I D = 0.5 A, 1 A, 2 A
4 V
Static Drain to Source on State Resistance R DS(on) (Ω)
Case Temperature Tc (°C)
0.25
0.20
0.15
0.10
0.05
0
–40
0
40
80
120
160

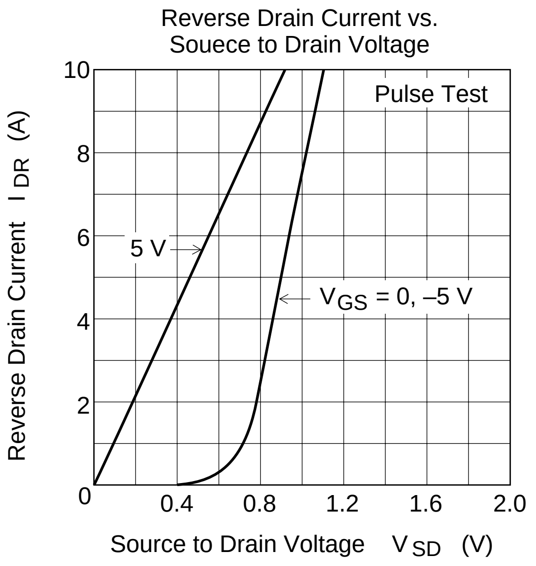

Forward Transfer Admittance vs.
Drain Current
V DS = 10 V
Pulse Test
75 °C
25 °C
Tc = –25 °C
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.1
0.2
0.5
1
2
5
10


Body–Drain Diode Reverse Recovery Time
di/dt = 20 A/µs
VGS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
VGS = 0
f = 1 MHz
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

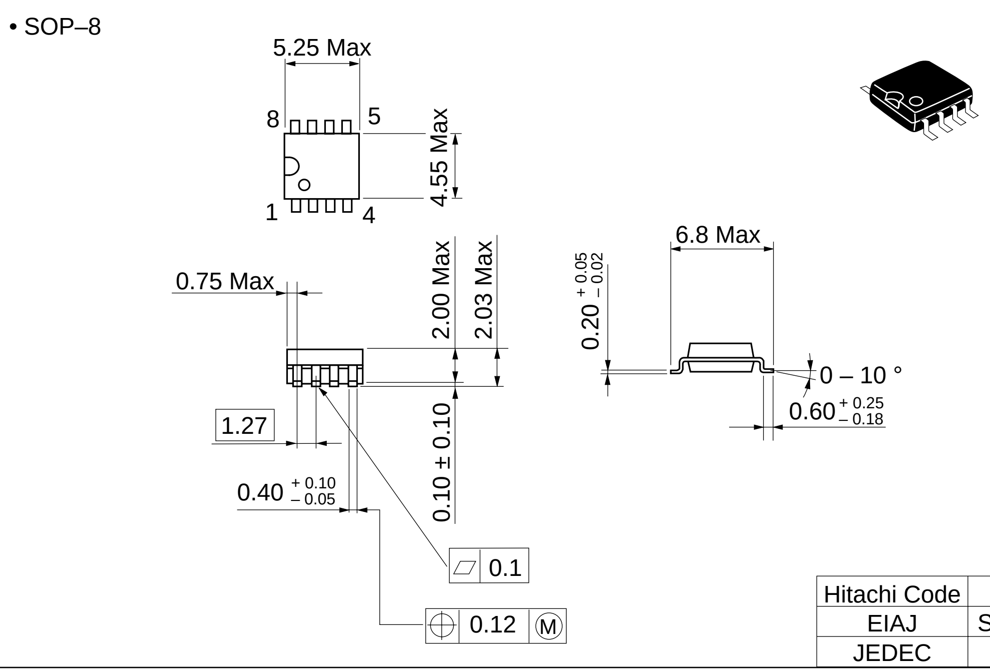

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
VDD = 5 V
10 V
25 V
VDS
VGS
ID = 2.5 A
VDD = 25 V
10 V
5 V
50
40
30
20
10
10
8
6
4
2
0
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
tr
td(off)
tf
td(on)
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
0.1
0.2
0.5
1
2
5
10
Drain Current ID (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2004F Target Specification

Silicon N Channel Power MOS FET

HITACHI

4th. Edition
Apr. 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8

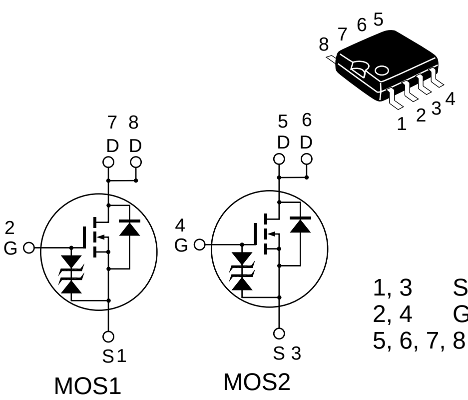


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	15	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	3.5	A
Drain peak current	$I_{D(pulse)}$*	14	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

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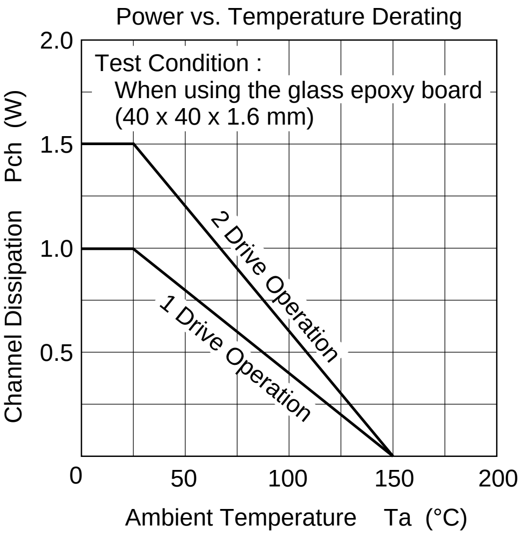
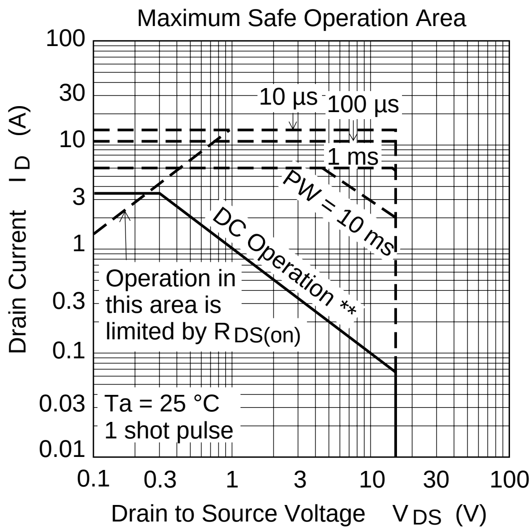
Table 2 Electrical Characteristics (Ta = 25°C)

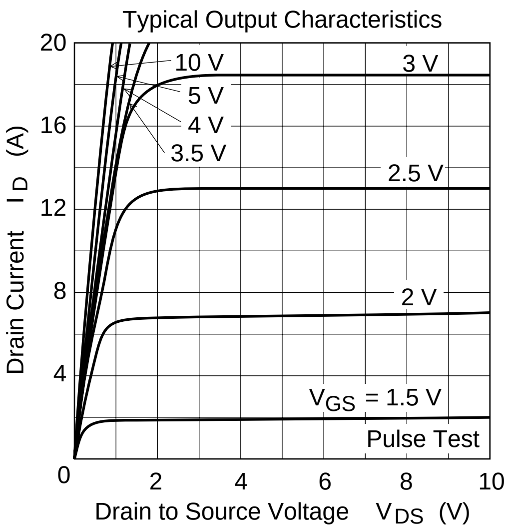
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	15	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 15 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.055	0.07	Ω	I_D = 2A V_{GS} = 4V *
		—	0.07	0.09	Ω	I_D = 2A V_{GS} =2.5V *
Forward tramsfer admittance	$\|y_{fs}\|$	4.5	7.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	620	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	460	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	155	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$*	—	22	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	90	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$*	—	110	—	ns	
Fall time	t_f	—	115	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	50	—	ns	I_F = 3.5 A, V_{GS} = 0 diF / dt = 20A / µs

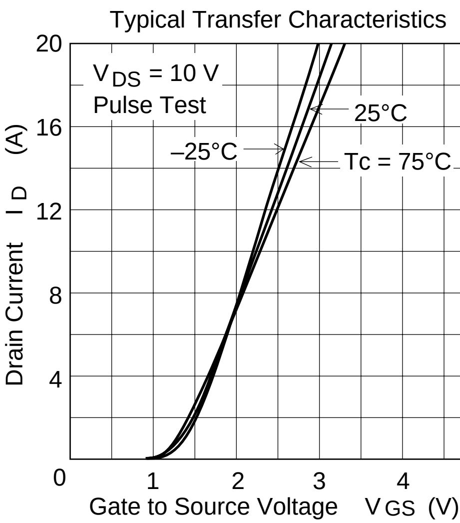
* Pulse Test



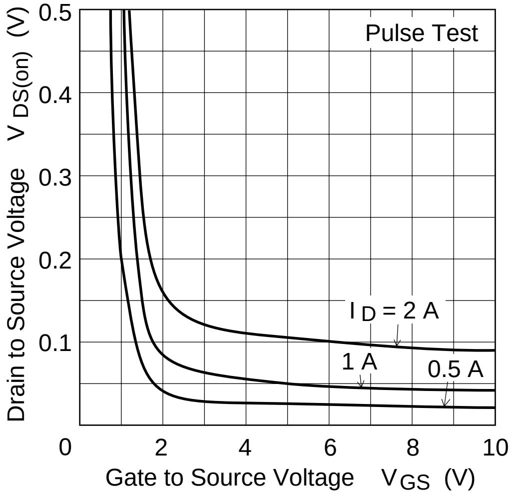


** 1 Drive Operation
When using the glass epoxy board
(40 x 40 x 1.6 mm)

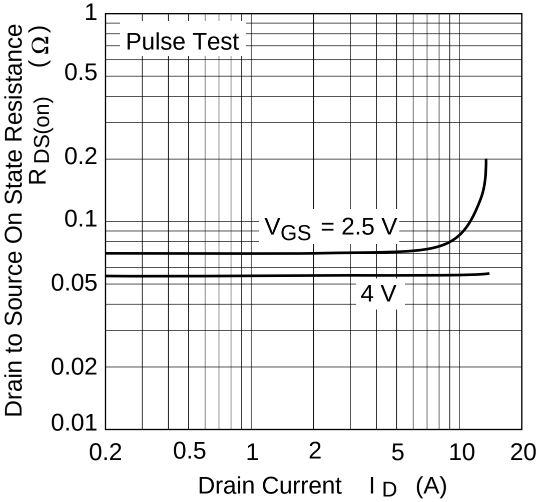




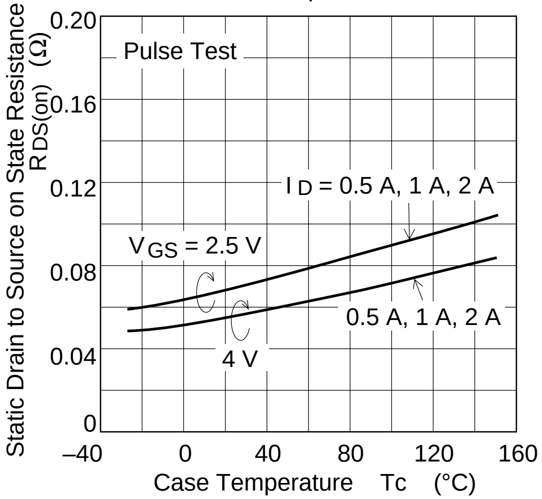
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



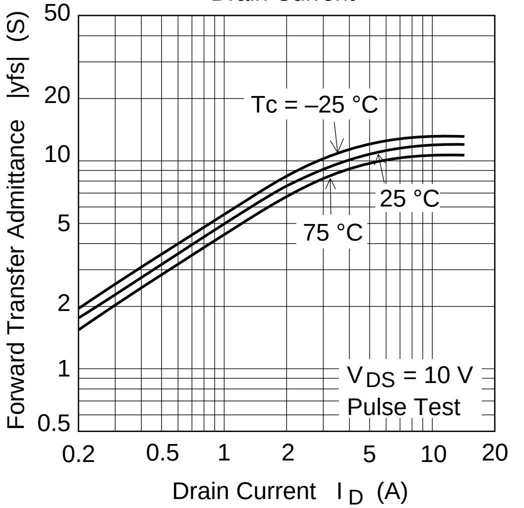
Static Drain to Source on State Resistance
vs. Drain Current

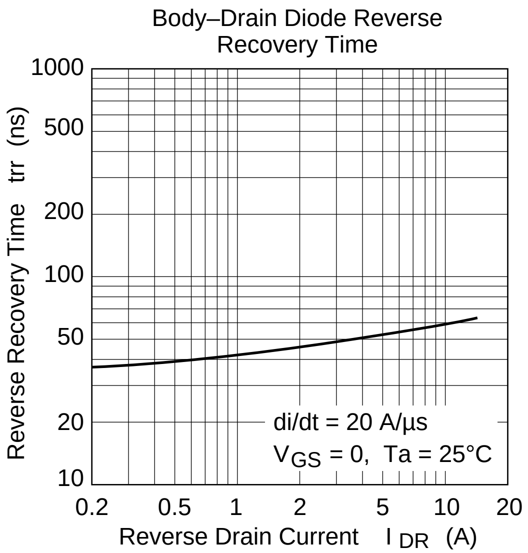


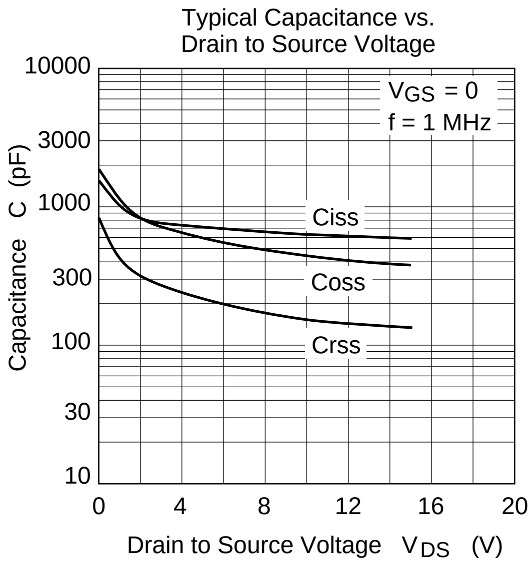
Static Drain to Source on State Resistance
vs. Temperature

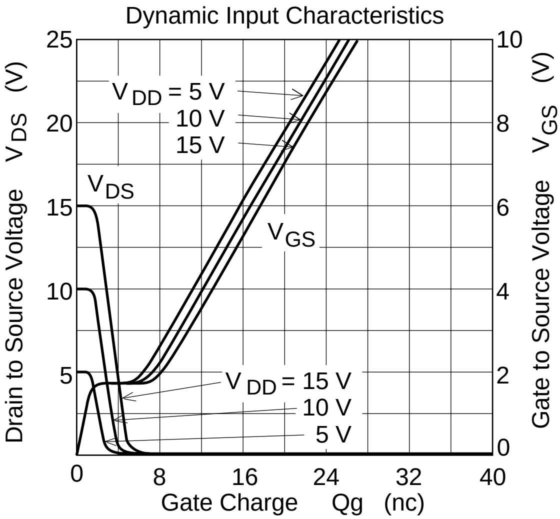


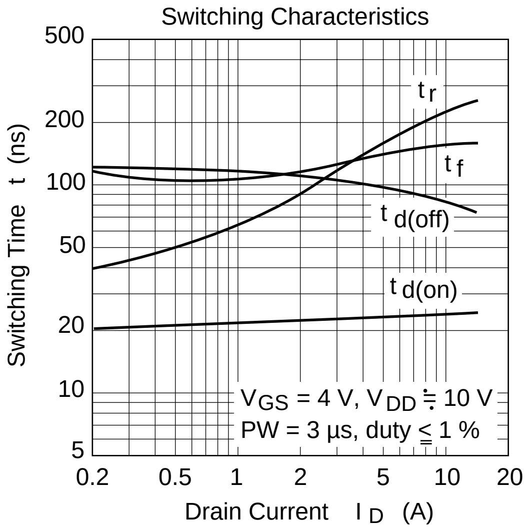
Forward Transfer Admittance vs.
Drain Current

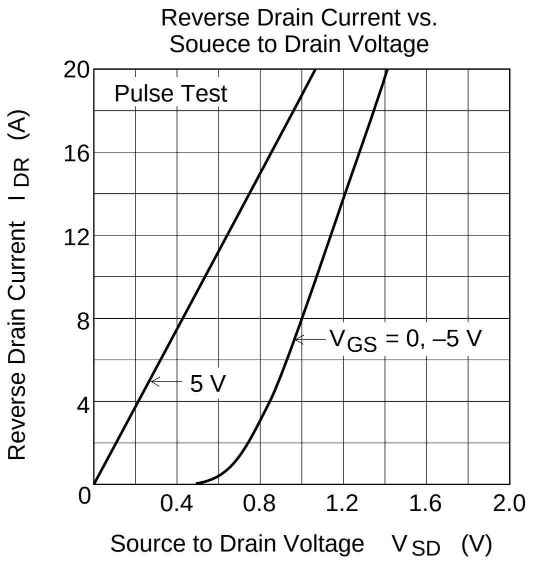



Body–Drain Diode Reverse
Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di/dt = 20 A/µs
VGS = 0, Ta = 25°C
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)


Typical Capacitance vs.
Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0
4
8
12
16
20
Drain to Source Voltage VDS (V)

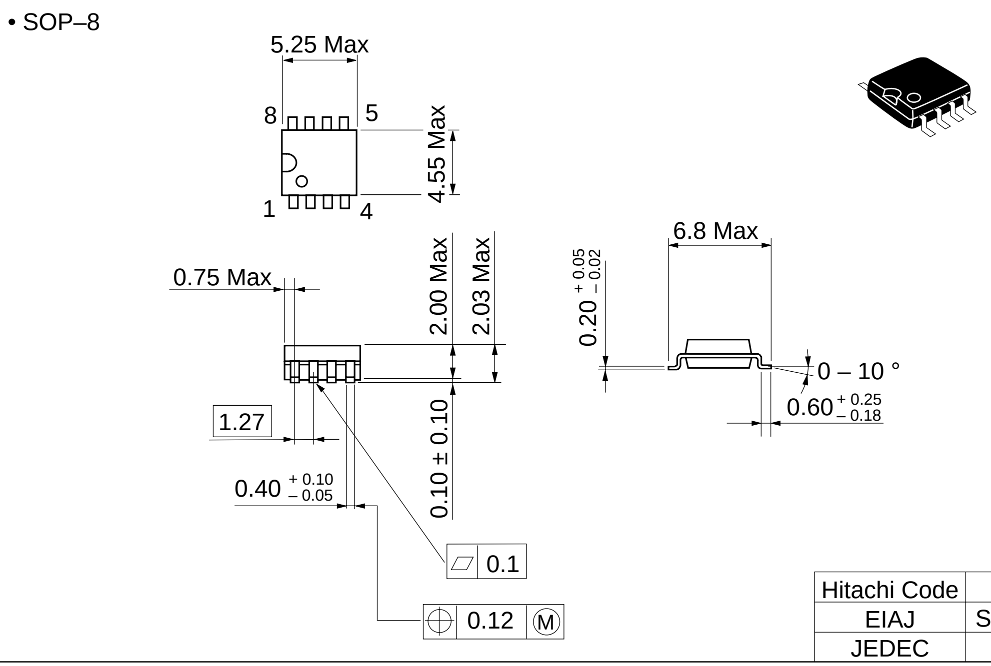

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
25
20
15
10
5
10
8
6
4
2
0
V DD = 5 V
10 V
15 V
VDS
VGS
V DD = 15 V
10 V
5 V
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t r
t f
t d(off)
t d(on)
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
0.2
0.5
1
2
5
10
20
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2005F

Silicon N Channel Power MOS FET

HITACHI

2nd. Edition
Jun. 1995

Application

Power switching

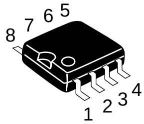
Features

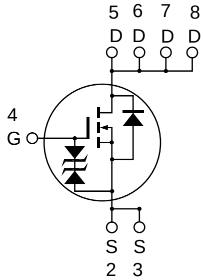
- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Cord	FP–8D
EIAJ Cord	SC–527–8A
JEDEC Cord	—

SOP–8





1	N/C
2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	3.5	A
Drain peak current	$I_{D(pulse)}$*	14	A
Body–drain diode reverse drain current	I_{DR}	3.5	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

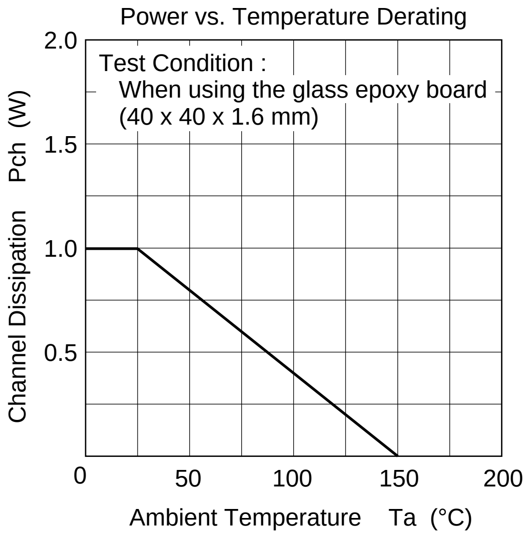
* PW ≤ 10 μs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

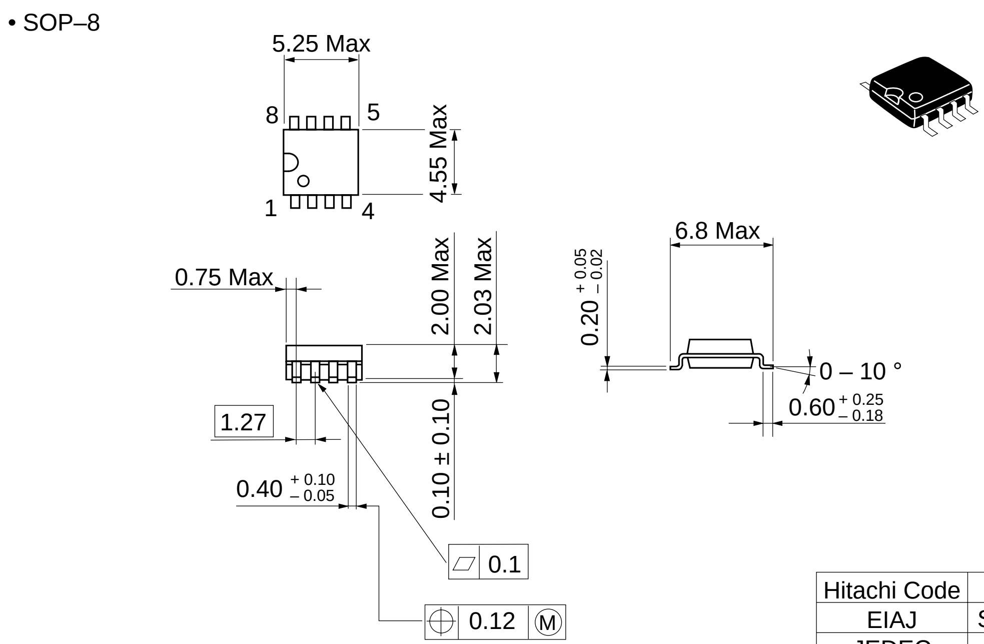
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.065	Ω	I_D = 2A V_{GS} = 4V *
		—	0.06	0.09	Ω	I_D = 2A V_{GS} = 2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	7	10	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	810	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	600	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	155	—	pF	f = 1 MHz
Turn–on time	t_{on}	—	100	—	ns	V_{GS} = 4 V, I_D = 2 A
Turn–off time	t_{off}	—	270	—	ns	V_{DD} = 10 V
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 3.5 A, V_{GS} = 0

* Pulse Test



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2006F

Silicon N Channel Power MOS FET

HITACHI

2nd. Edition
Jun. 1995

Application

Power switching

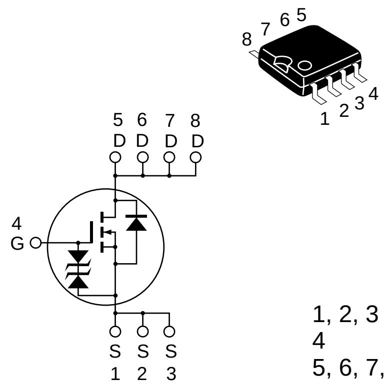
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Cord	FP–8D
EIAJ Cord	SC–527–8A
JEDEC Cord	—

SOP–8



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$*	16	A
Body–drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

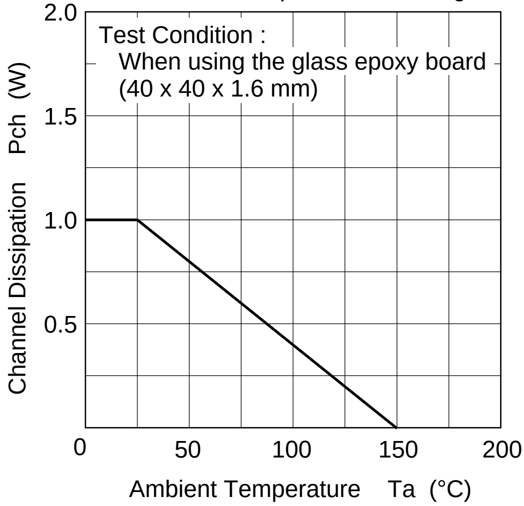
* PW ≤ 10 μs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics (Ta = 25°C)

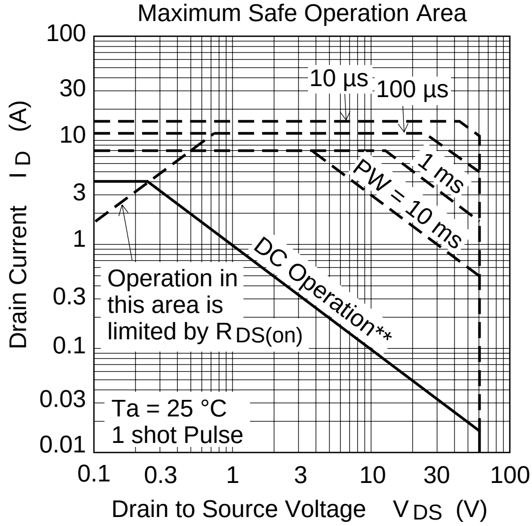
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.045	0.06	Ω	I_D = 2 A V_{GS} = 10V *
		—	0.065	0.075	Ω	I_D = 2 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	4	6.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	135	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	30	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	155	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	80	—	ns	
Fall time	t_f	—	80	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 4 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	90	—	ns	I_F = 4 A, V_{GS} = 0 diF / dt = 20A / µs

* Pulse Test

Power vs. Temperature Derating

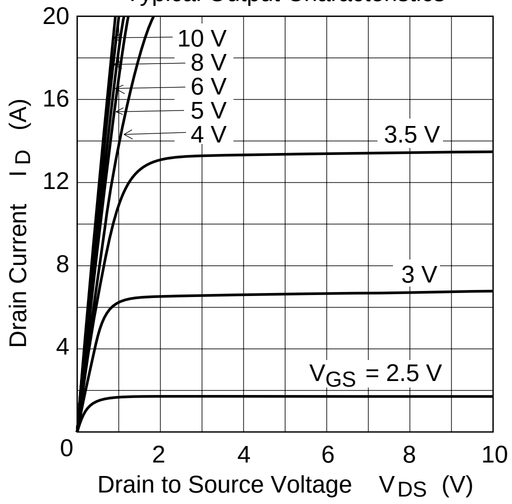


Maximum Safe Operation Area

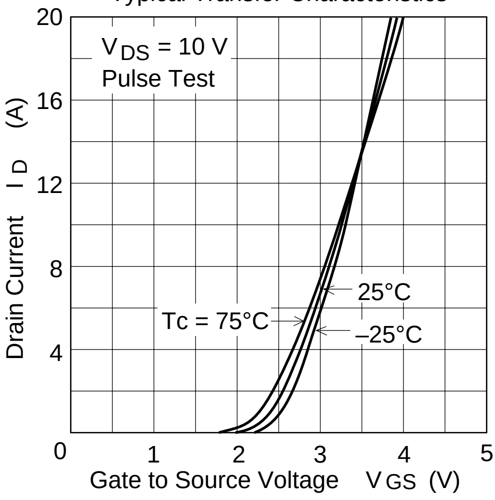


** When using the glass epoxy board (40 x 40 x 1.6 mm)

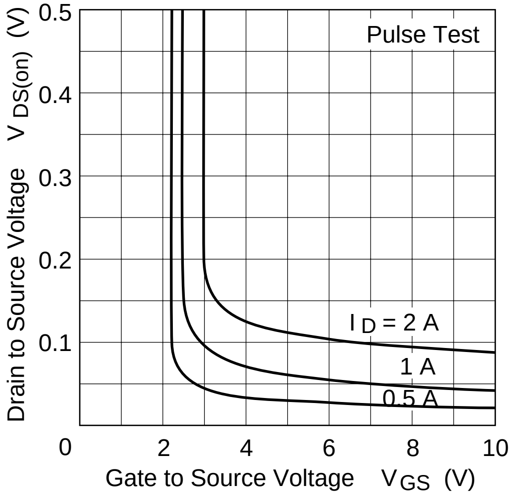
Typical Output Characteristics



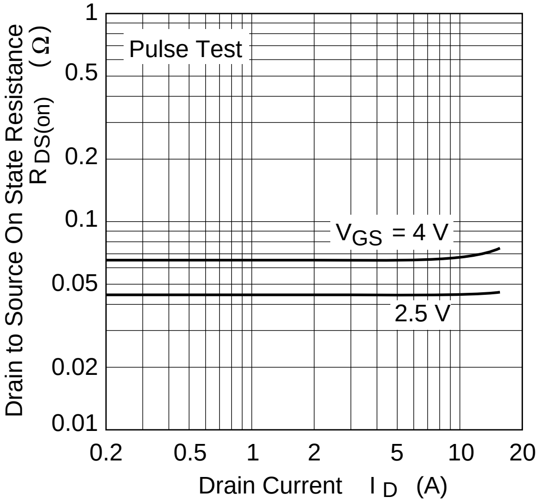
Typical Transfer Characteristics



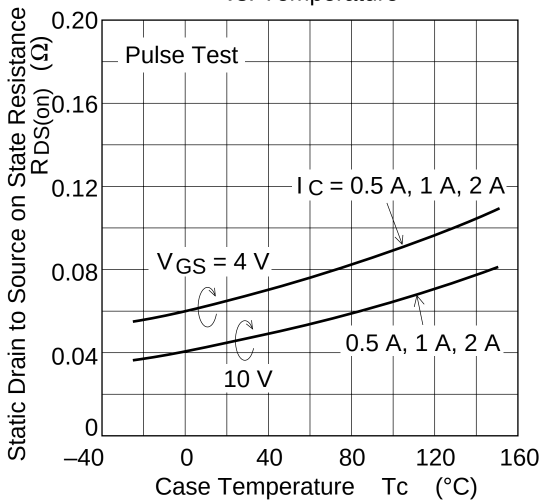
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



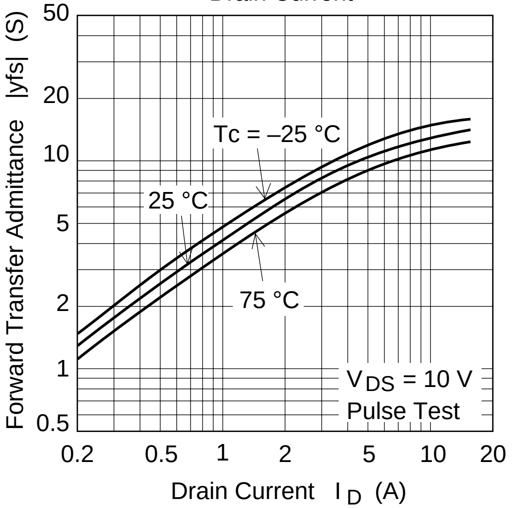
Static Drain to Source on State Resistance
vs. Drain Current

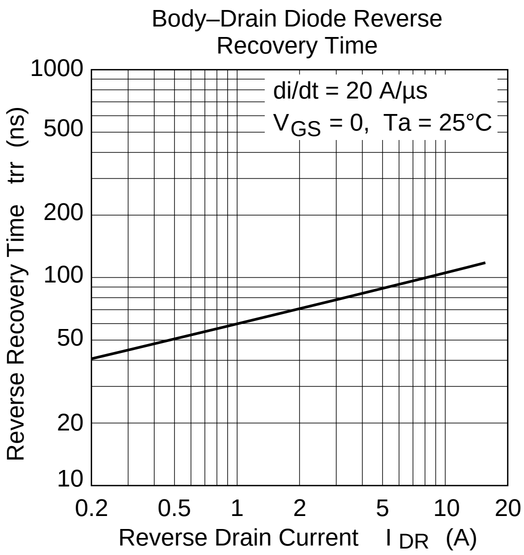


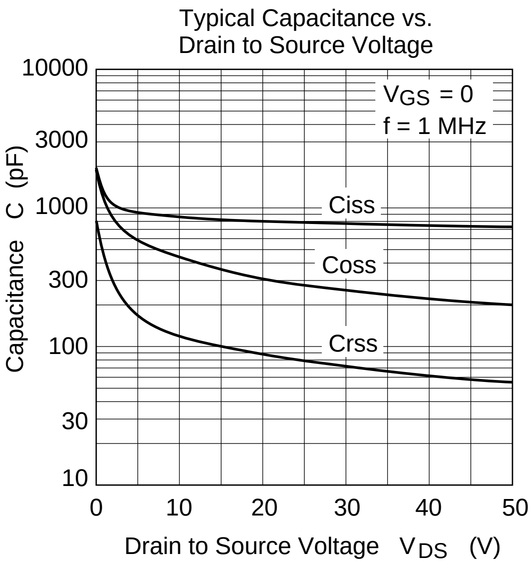
Static Drain to Source on State Resistance
vs. Temperature

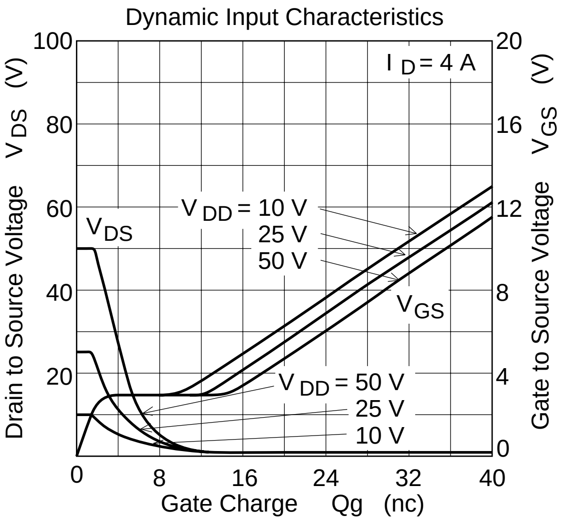


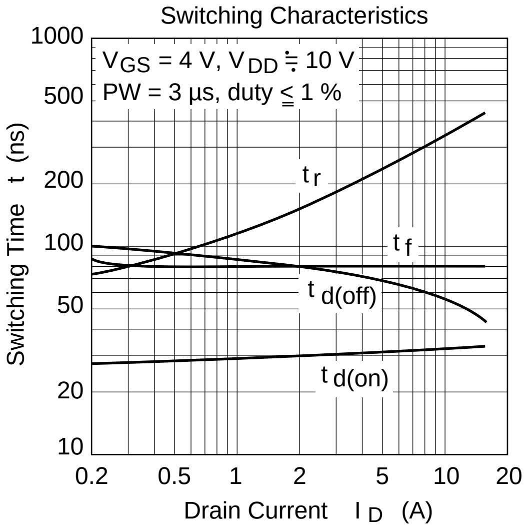
Forward Transfer Admittance vs.
Drain Current

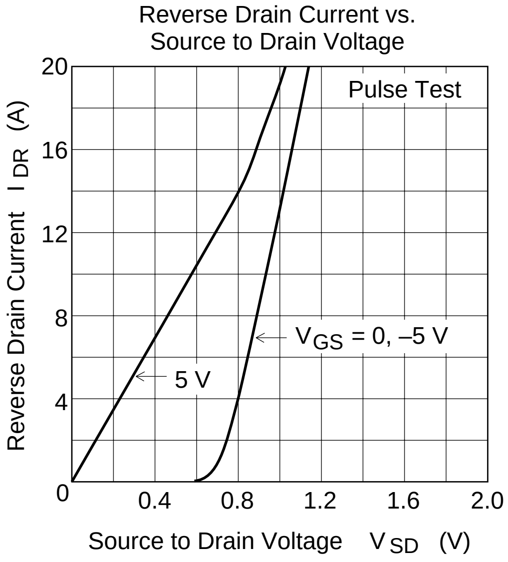



Body–Drain Diode Reverse Recovery Time
di/dt = 20 A/µs
V GS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
V GS = 0
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage V DS (V)

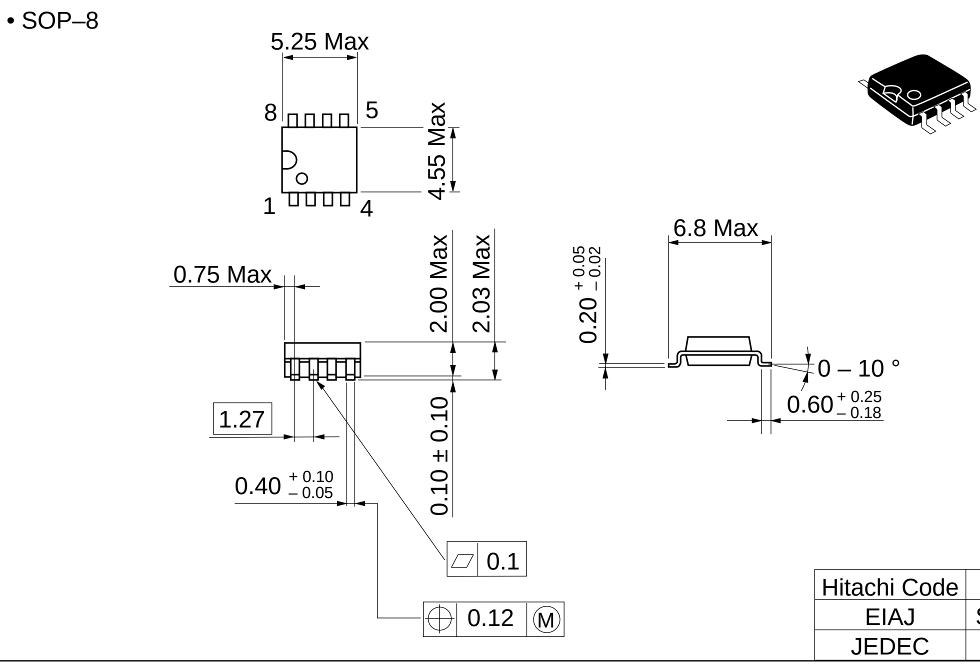

Dynamic Input Characteristics
I D = 4 A
V DS
V DD = 10 V
25 V
50 V
V GS
V DD = 50 V
25 V
10 V
Drain to Source Voltage V DS (V)
Gate to Source Voltage V GS (V)
100
80
60
40
20
20
16
12
8
4
0
0
8
16
24
32
40
Gate Charge Qg (nc)


Switching Characteristics
V GS = 4 V, V DD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
t r
t f
t d(off)
t d(on)
Switching Time t (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2007F

Silicon N Channel Power MOS FET

HITACHI

2nd. Edition
May 1995

Application

Power switching
synchronously Rectifier

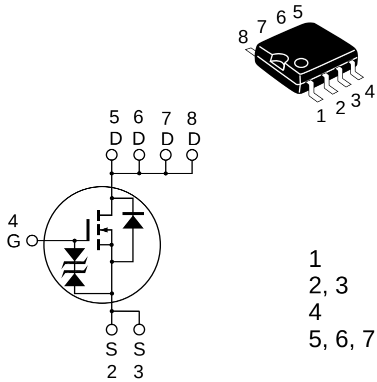
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

SOP–8



1	N/C
2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

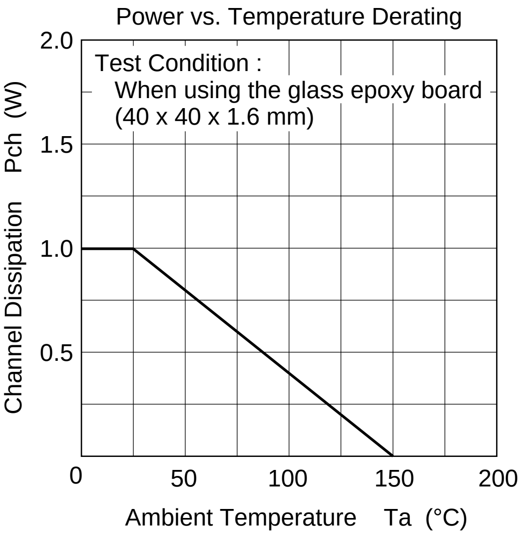
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$*	16	A
Body–drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

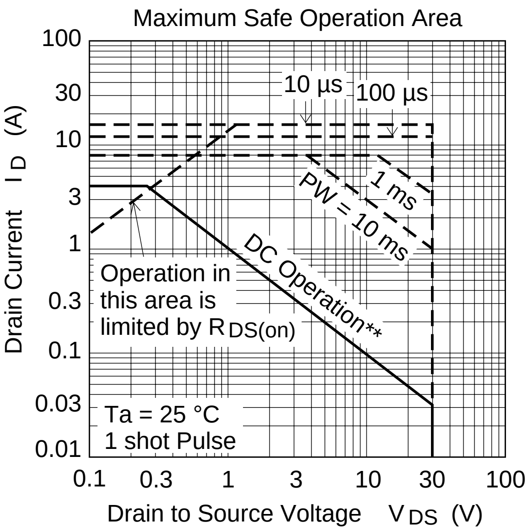
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using the glass epoxy board (40 x 40 x 1.6 mm)

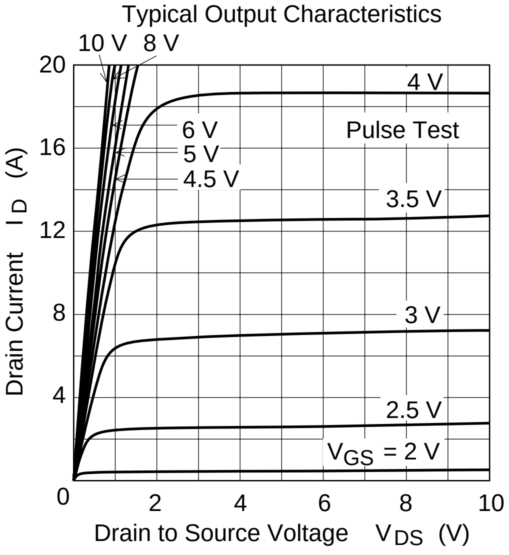
Table 2 Electrical Characteristics (Ta = 25°C)

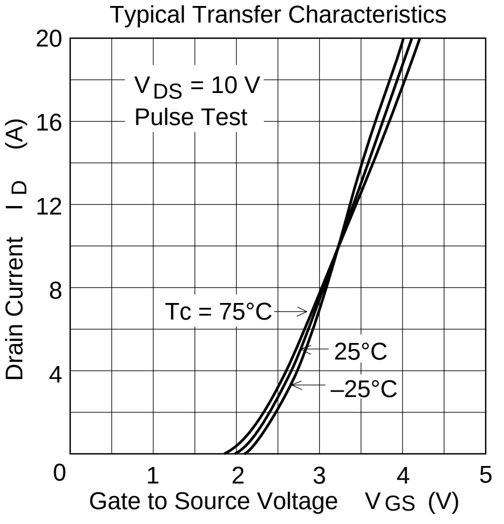
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.04	0.07	Ω	I_D = 2A V_{GS} = 10V *
		—	0.065	0.11	Ω	I_D = 2A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	2	5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	680	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	470	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	110	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	25	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	100	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	50	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 4A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	70	—	ns	I_F = 4A, V_{GS} = 0 diF / dt = 20 A / µs

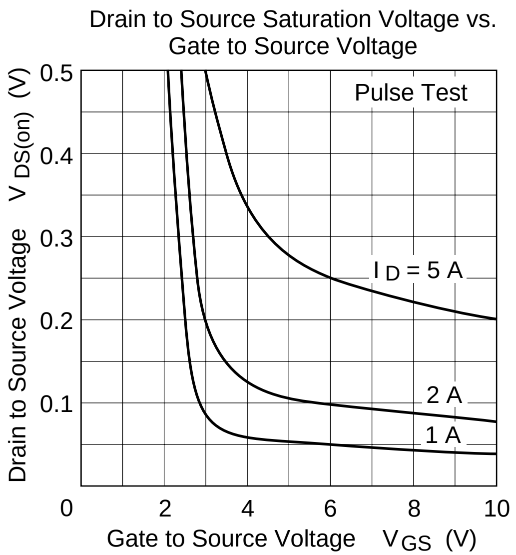
* Pulse Test

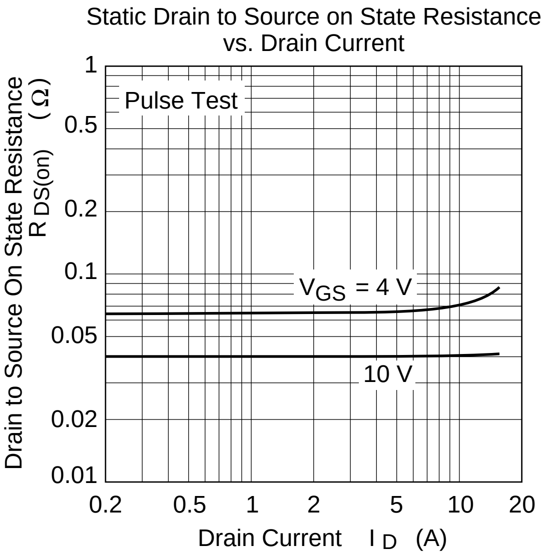

Power vs. Temperature Derating
Test Condition :
When using the glass epoxy board
(40 x 40 x 1.6 mm)
Channel Dissipation Pch (W)
2.0
1.5
1.0
0.5
0
50
100
150
200
Ambient Temperature Ta (°C)

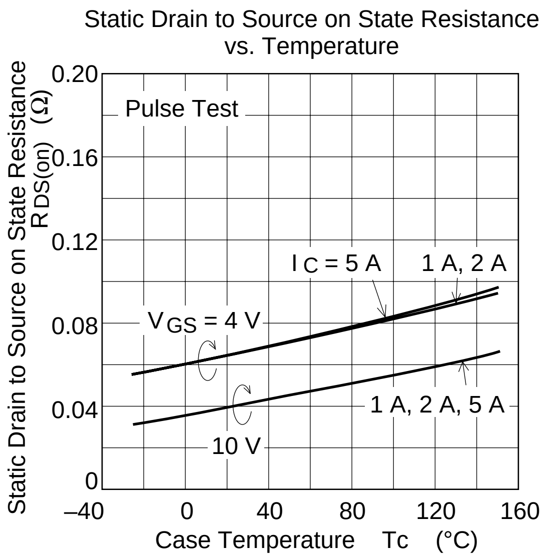

Maximum Safe Operation Area
10 μs
100 μs
1 ms
PW = 10 ms
DC Operation**
Operation in this area is limited by R DS(on)
Ta = 25 °C
1 shot Pulse
Drain Current I D (A)
100
30
10
3
1
0.3
0.1
0.03
0.01
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

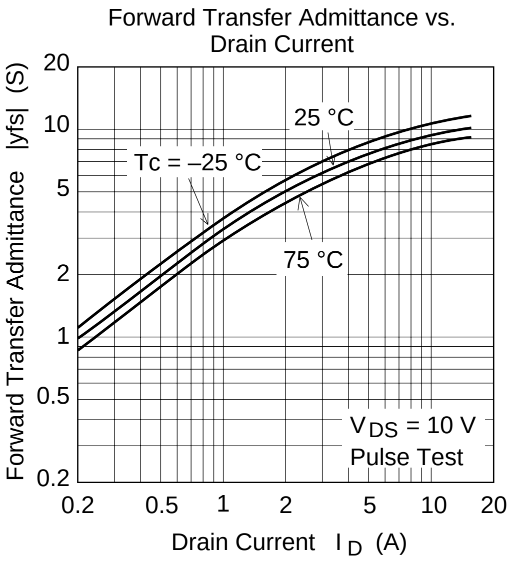

Typical Output Characteristics
10 V
8 V
6 V
5 V
4.5 V
4 V
Pulse Test
3.5 V
3 V
2.5 V
VGS = 2 V
Drain Current I D (A)
20
16
12
8
4
0
2
4
6
8
10
Drain to Source Voltage V DS (V)

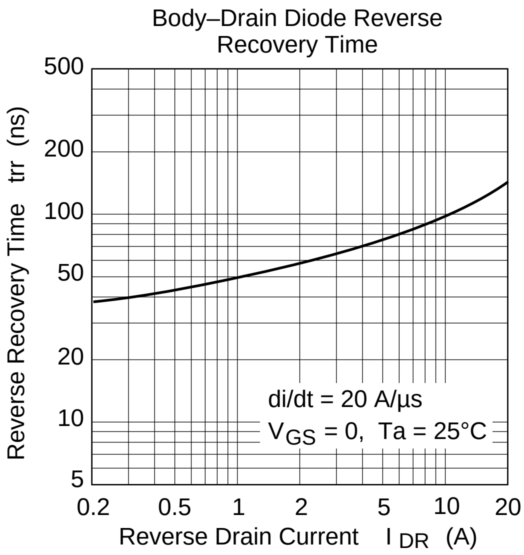

Typical Transfer Characteristics
V DS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
Drain Current I D (A)
20
16
12
8
4
0
1
2
3
4
5
Gate to Source Voltage V GS (V)

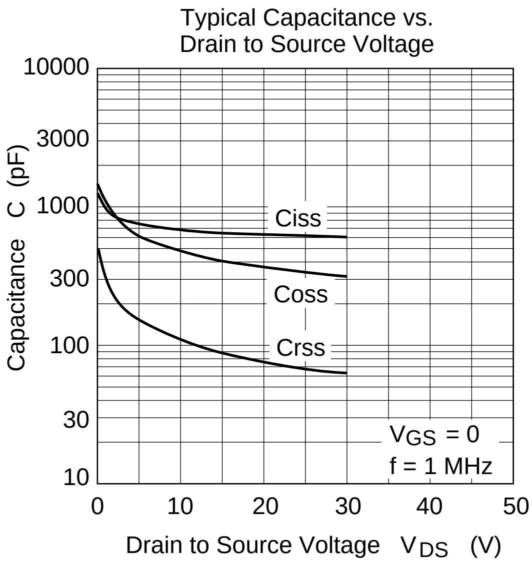

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 5 A
2 A
1 A
Drain to Source Voltage V DS(on) (V)
0.5
0.4
0.3
0.2
0.1
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

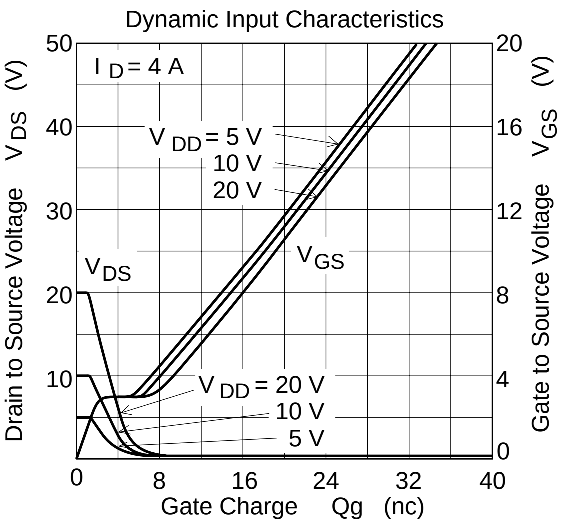

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
VGS = 4 V
10 V
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
0.2
0.5
1
2
5
10
20
Drain Current I D (A)

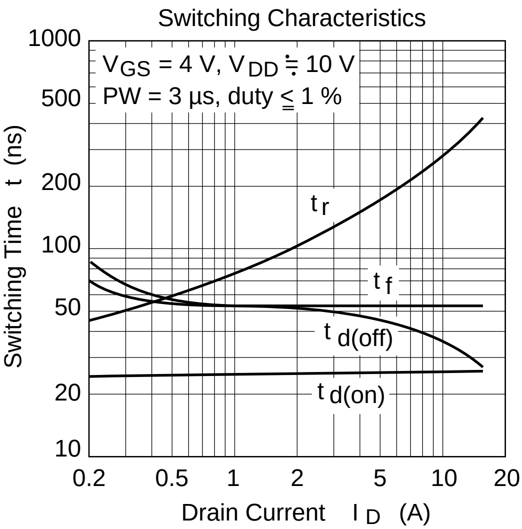

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I C = 5 A
1 A, 2 A
VGS = 4 V
10 V
1 A, 2 A, 5 A
Static Drain to Source on State Resistance RDS(on) (Ω)
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

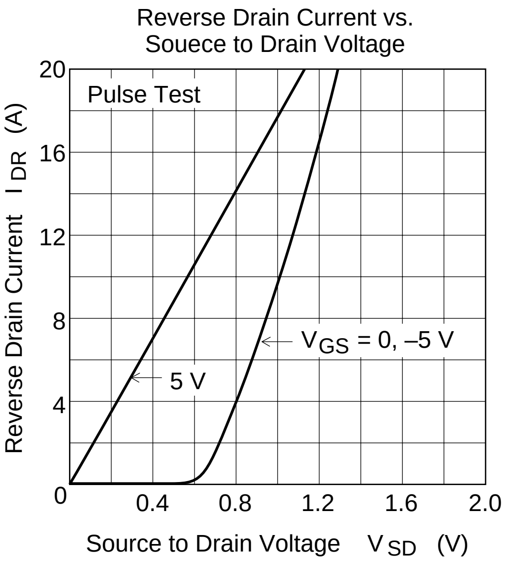

Forward Transfer Admittance vs.
Drain Current
25 °C
Tc = –25 °C
75 °C
VDS = 10 V
Pulse Test
Forward Transfer Admitance |yfs| (S)
20
10
5
2
1
0.5
0.2
0.2
0.5
1
2
5
10
20
Drain Current I D (A)


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)
di/dt = 20 A/µs
VGS = 0, Ta = 25°C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz

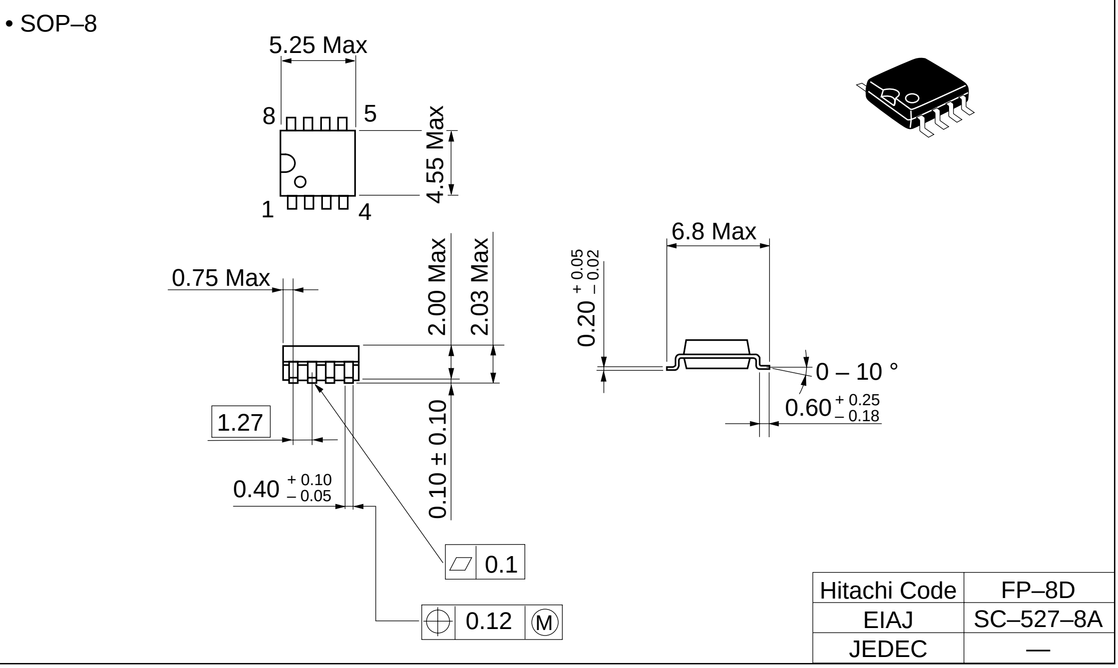

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
I D = 4 A
V DD = 5 V
10 V
20 V
VDS
VGS
V DD = 20 V
10 V
5 V
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≤ 1 %
t r
t f
t d(off)
t d(on)
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2008F Target Specification

Silicon N Channel Power MOS FET

HITACHI

1st. Edition
May 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Cord	FP–8D
EIAJ Cord	SC–527–8A
JEDEC Cord	—

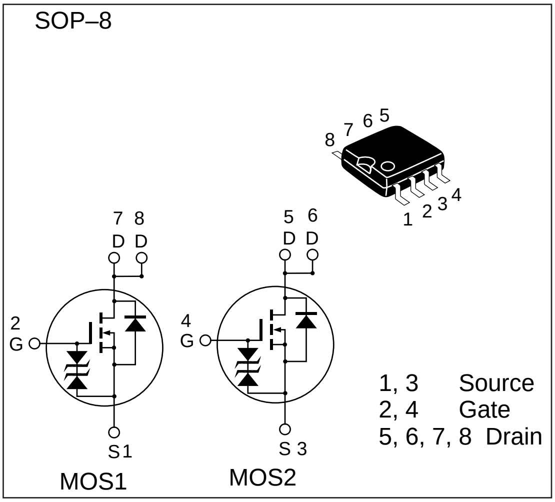


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	3.5	A
Drain peak current	$I_{D(pulse)}$*	14	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

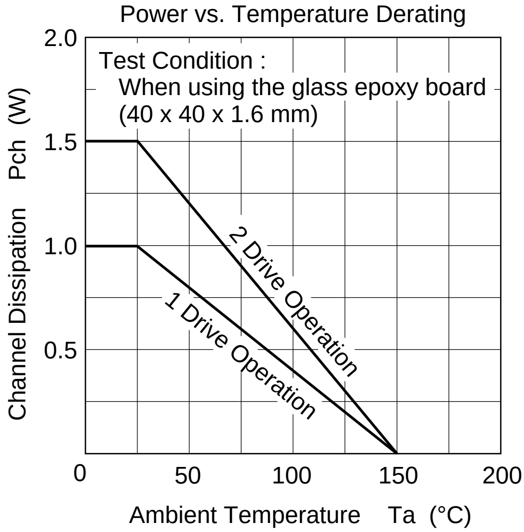
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

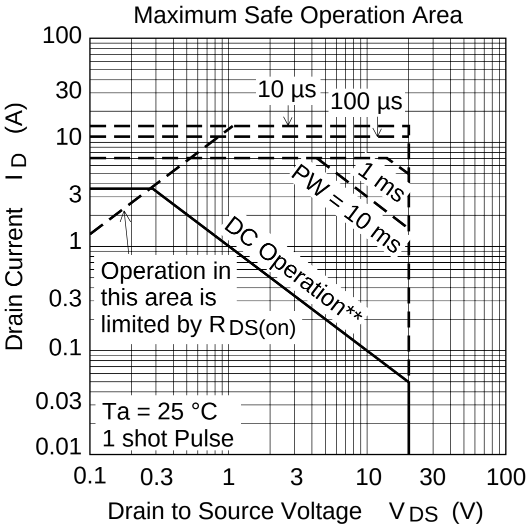
Hitachi semiconductor

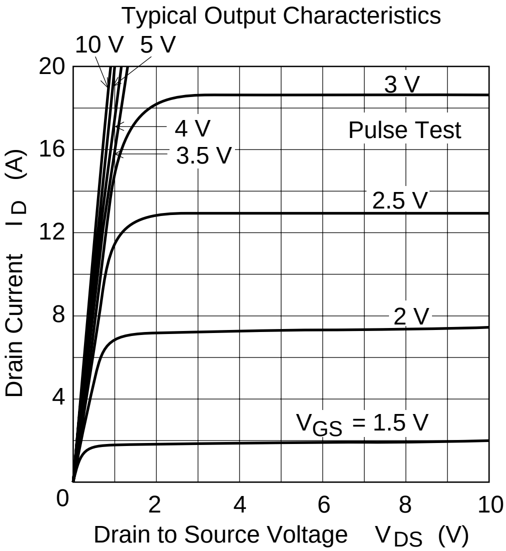
Table 2 Electrical Characteristics (Ta = 25°C)

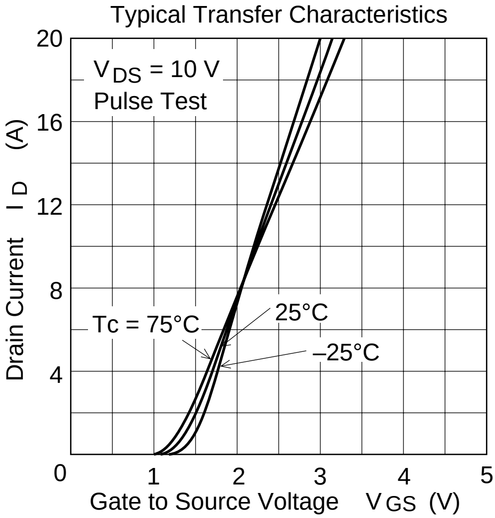
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.055	0.075	Ω	I_D = 2A V_{GS} = 4V *
		—	0.07	0.11	Ω	I_D = 2A V_{GS} =2.5V *
Forward tramsfer admittance	$\|y_{fs}\|$	5.0	7.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	620	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	420	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	140	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	18	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	85	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	45	—	ns	I_F = 3.5 A diF / dt = 20A / µs

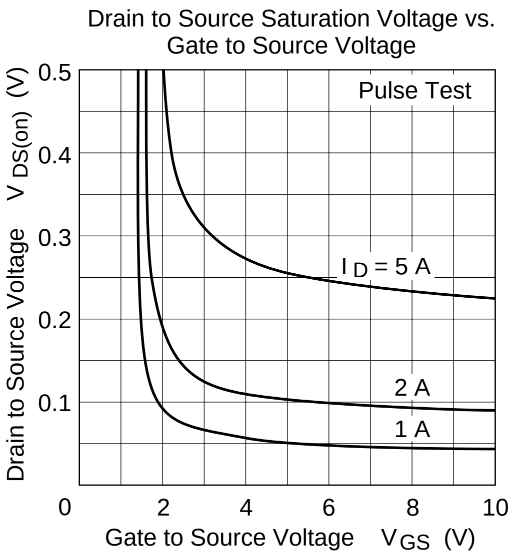
* Pulse Test

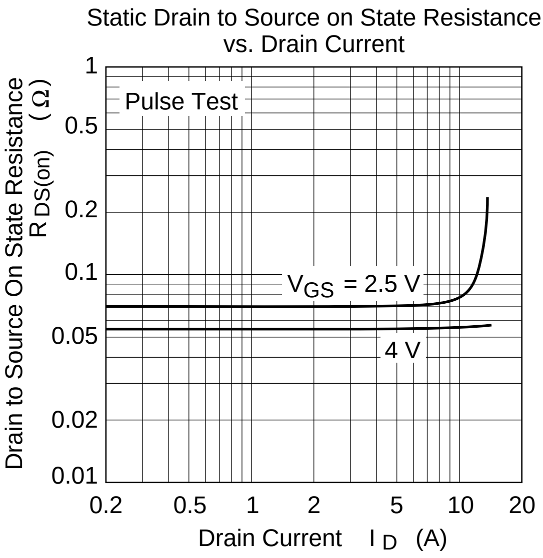

Power vs. Temperature Derating
Test Condition :
When using the glass epoxy board
(40 x 40 x 1.6 mm)
2 Drive Operation
1 Drive Operation
Channel Dissipation Pch (W)
2.0
1.5
1.0
0.5
0
50
100
150
200
Ambient Temperature Ta (°C)

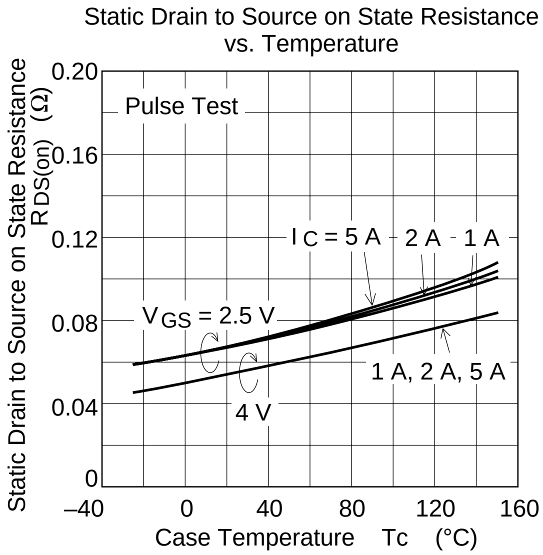

Maximum Safe Operation Area
10 µs
100 µs
1 ms
PW = 10 ms
DC Operation**
Operation in
this area is
limited by R DS(on)
Ta = 25 °C
1 shot Pulse
Drain Current I D (A)
100
30
10
3
1
0.3
0.1
0.03
0.01
0.1
0.3
1
3
10
30
100
Drain to Source Voltage V DS (V)

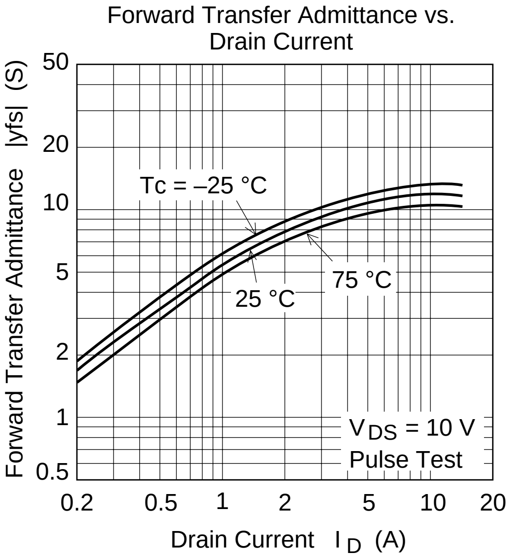

Typical Output Characteristics
10 V
5 V
3 V
4 V
3.5 V
Pulse Test
2.5 V
2 V
V GS = 1.5 V
Drain Current I D (A)
20
16
12
8
4
0
2
4
6
8
10
Drain to Source Voltage V DS (V)

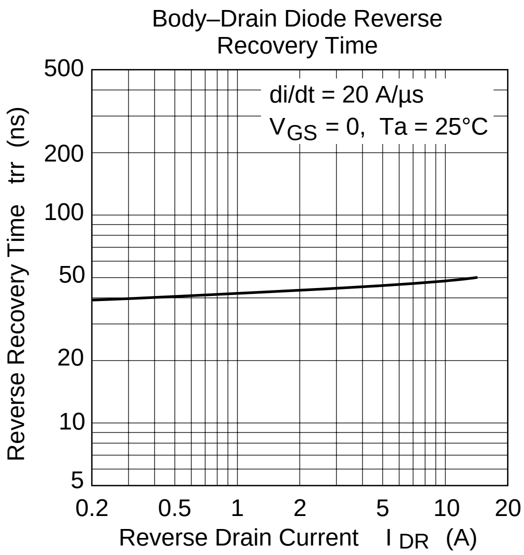

Typical Transfer Characteristics
V DS = 10 V
Pulse Test
Tc = 75°C
25°C
–25°C
Drain Current I D (A)
20
16
12
8
4
0
1
2
3
4
5
Gate to Source Voltage V GS (V)

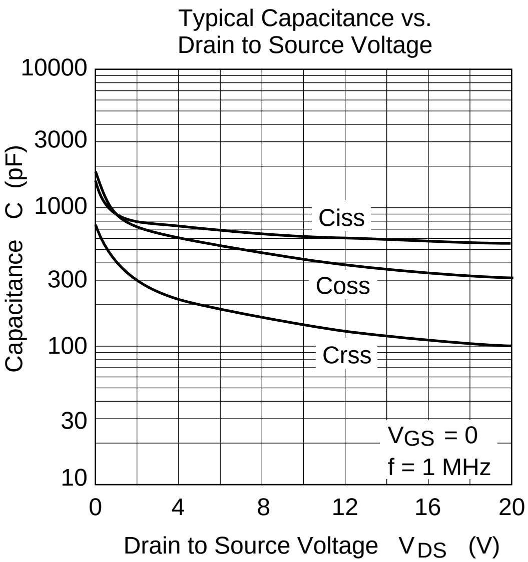

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Voltage V DS(on) (V)
Gate to Source Voltage V GS (V)
Pulse Test
I D = 5 A
2 A
1 A
0.5
0.4
0.3
0.2
0.1
0
2
4
6
8
10

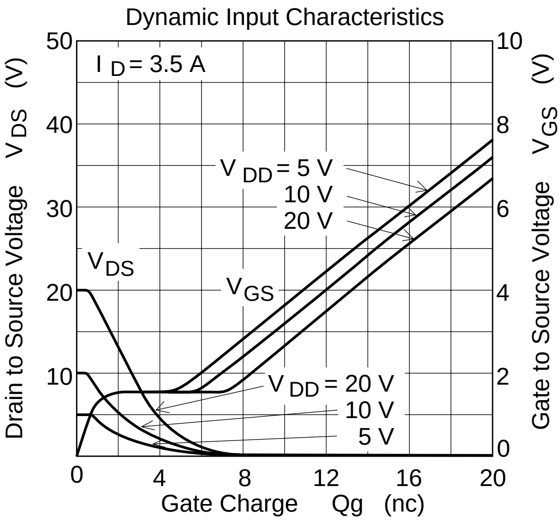

Static Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
Drain Current I D (A)
Pulse Test
VGS = 2.5 V
4 V
1
0.5
0.2
0.1
0.05
0.02
0.01
0.2
0.5
1
2
5
10
20

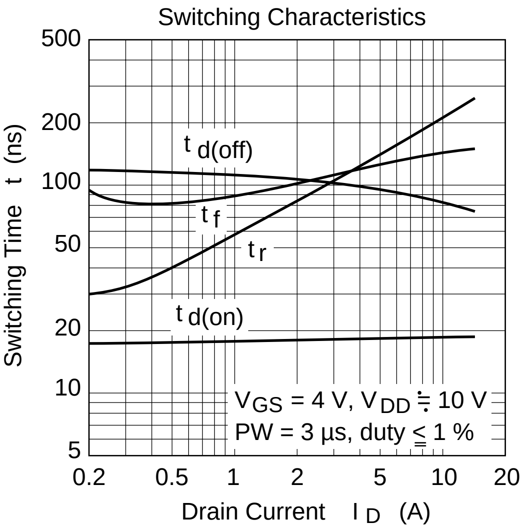

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance R DS(on) (Ω)
Case Temperature Tc (°C)
Pulse Test
I C = 5 A
2 A
1 A
VGS = 2.5 V
4 V
1 A, 2 A, 5 A
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160

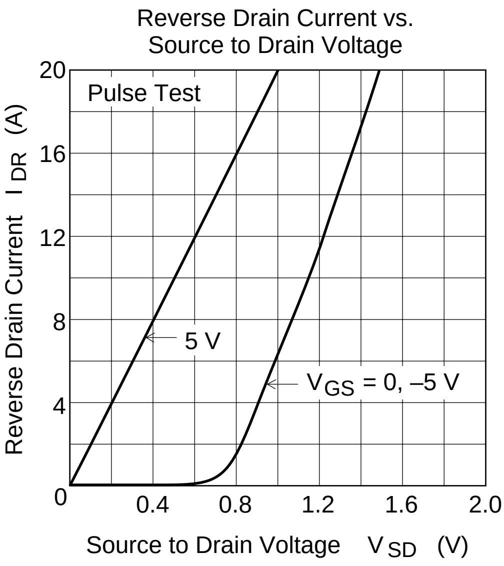

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
Tc = –25 °C
25 °C
75 °C
VDS = 10 V
Pulse Test
50
20
10
5
2
1
0.5
0.2
0.5
1
2
5
10
20


Body–Drain Diode Reverse Recovery Time
di/dt = 20 A/µs
VGS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0
4
8
12
16
20
Drain to Source Voltage VDS (V)


Dynamic Input Characteristics
I D = 3.5 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
50
40
30
20
10
10
8
6
4
2
0
V DD = 5 V
10 V
20 V
VDS
VGS
V DD = 20 V
10 V
5 V
0
4
8
12
16
20
Gate Charge Qg (nc)

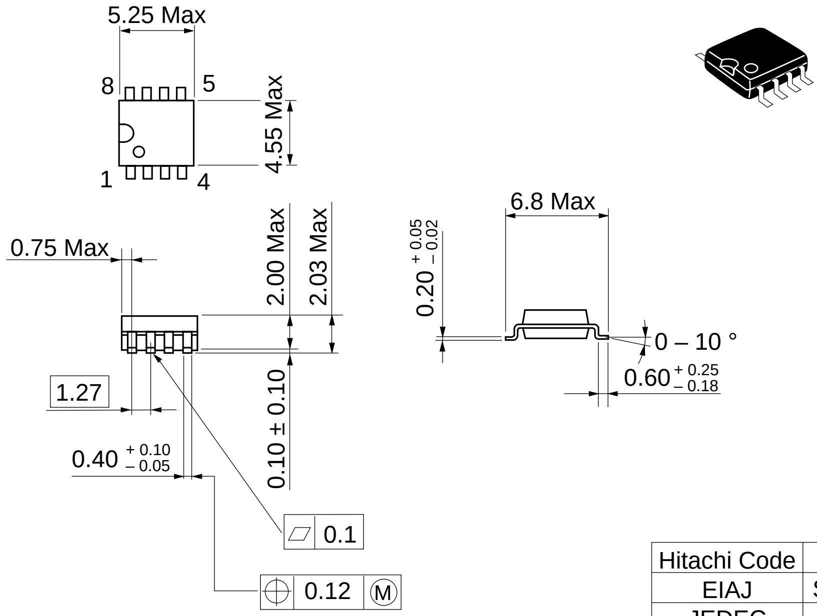

Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t d(off)
t f
t r
t d(on)
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
0.2
0.5
1
2
5
10
20
Drain Current I D (A)



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2009F Target Specification

Silicon N Channel Power MOS FET

HITACHI

1st. Edition
May 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

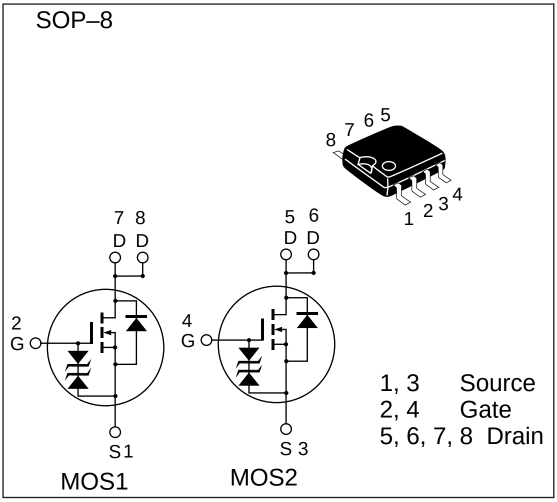


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	3.5	A
Drain peak current	$I_{D(pulse)}$*	14	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

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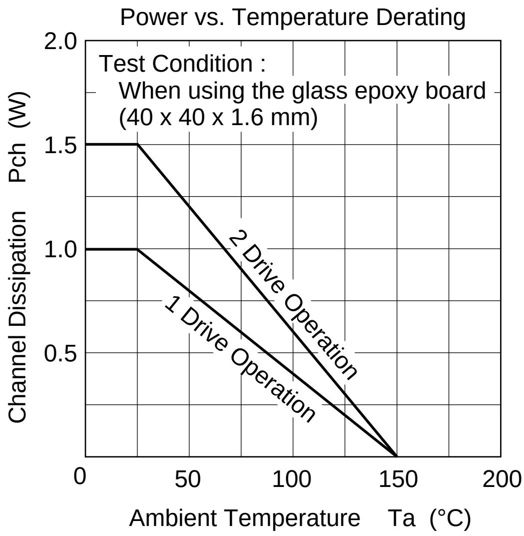
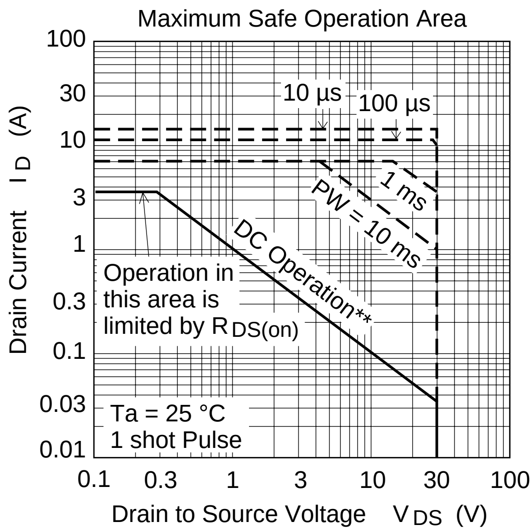
Table 2 Electrical Characteristics (Ta = 25°C)

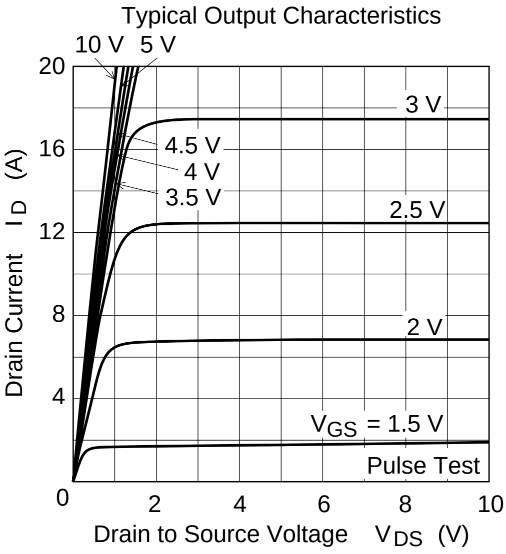
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.065	0.08	Ω	I_D = 2A V_{GS} = 4V *
		—	0.08	0.12	Ω	I_D = 2A V_{GS} =2.5V *
Forward tramsfer admittance	$\|y_{fs}\|$	4.5	7.0	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	610	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	330	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	105	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	17	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	80	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	t_f	—	90	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	50	—	ns	I_F = 3.5 A diF / dt = 20A / µs

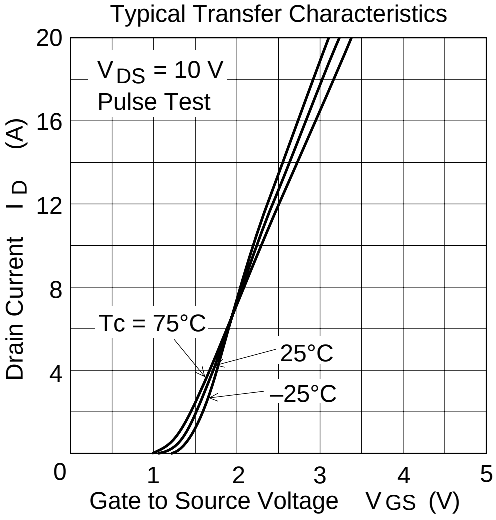
* Pulse Test

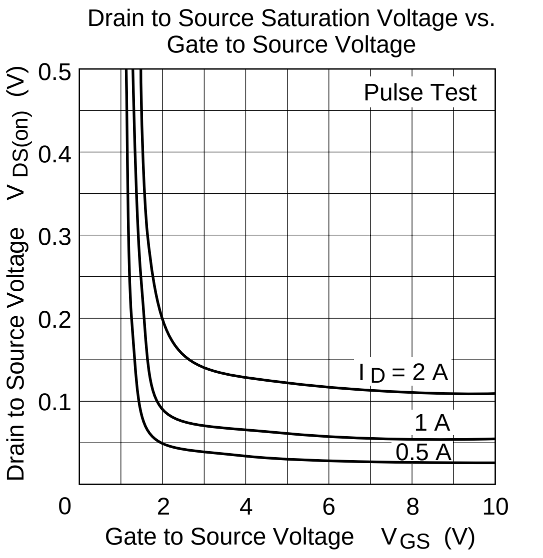


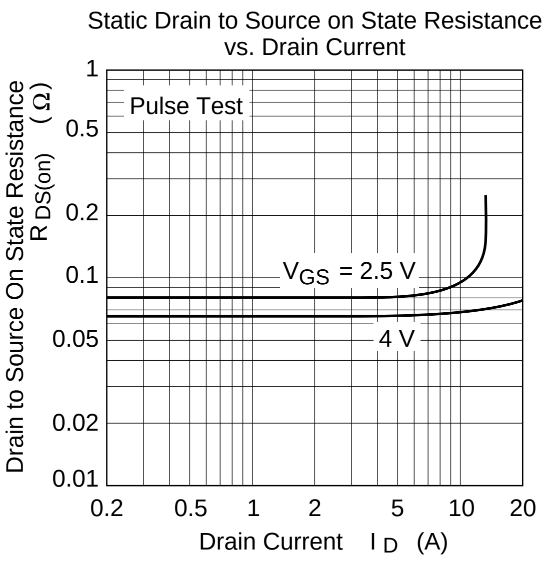


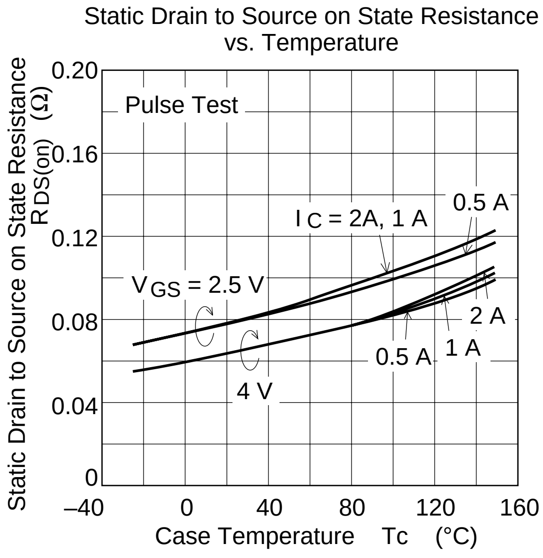
** When using the glass epoxy board (40 x 40 x 1.6 mm)

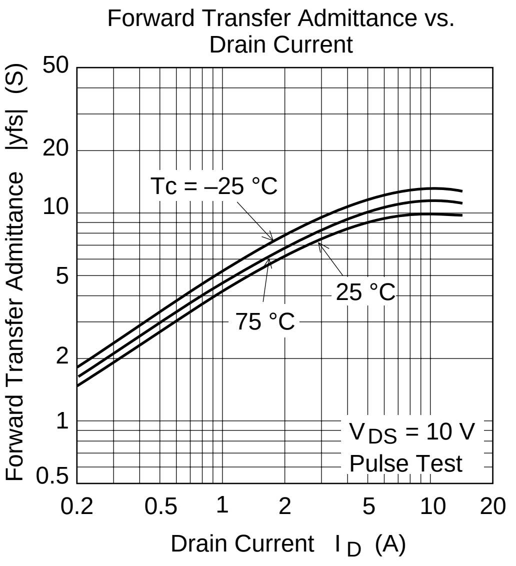


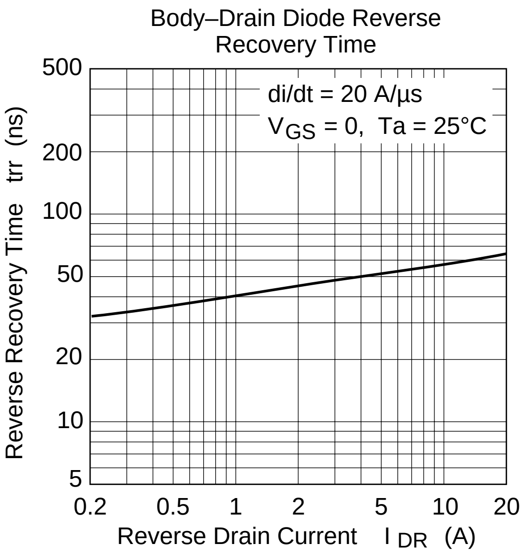


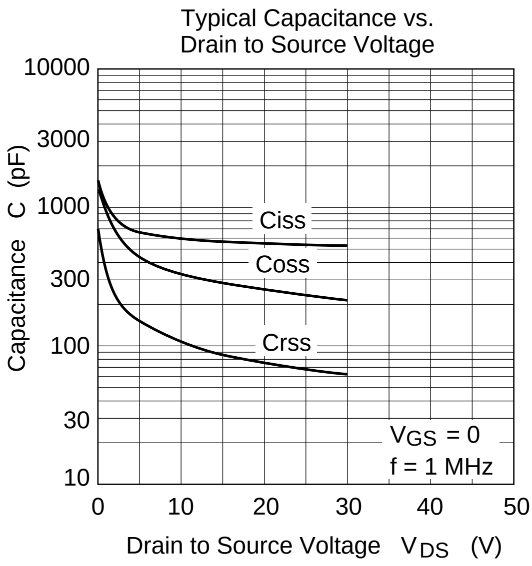

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Voltage V DS(on) (V)
0.5
0.4
0.3
0.2
0.1
Pulse Test
I D = 2 A
1 A
0.5 A
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

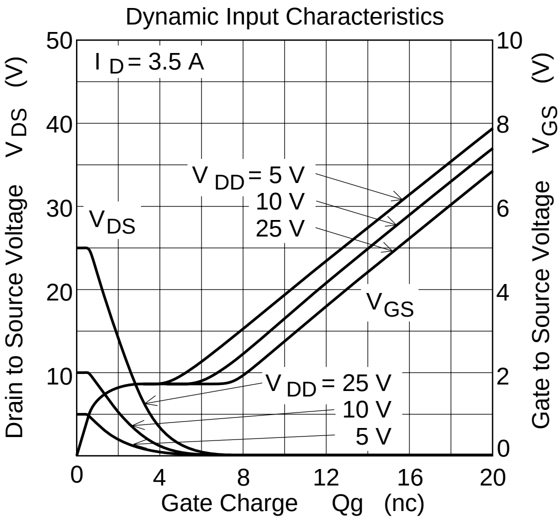

Static Drain to Source on State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
1
0.5
0.2
0.1
0.05
0.02
0.01
Pulse Test
VGS = 2.5 V
4 V
0.2
0.5
1
2
5
10
20
Drain Current I D (A)

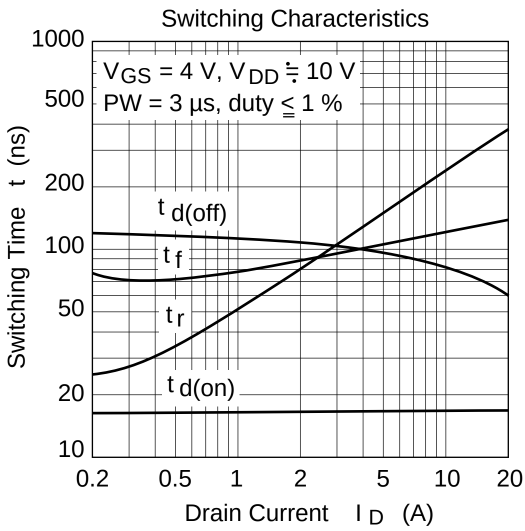

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance R DS(on) (Ω)
0.20
0.16
0.12
0.08
0.04
0
Pulse Test
I C = 2A, 1 A
0.5 A
VGS = 2.5 V
4 V
2 A
1 A
0.5 A
–40
0
40
80
120
160
Case Temperature Tc (°C)

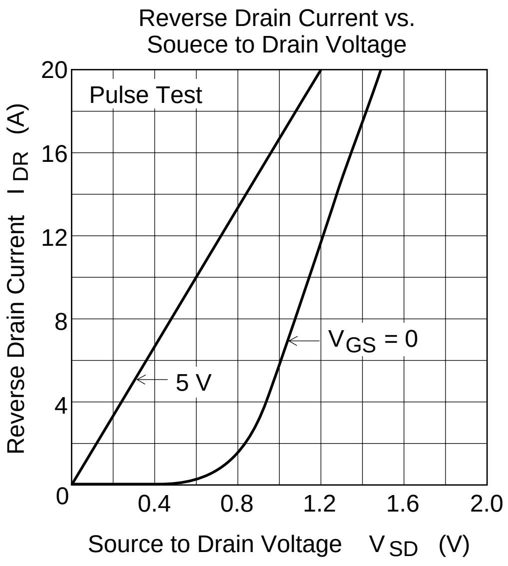

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
50
20
10
5
2
1
0.5
Tc = –25 °C
25 °C
75 °C
VDS = 10 V
Pulse Test
0.2
0.5
1
2
5
10
20
Drain Current I D (A)


Body–Drain Diode Reverse
Recovery Time
di/dt = 20 A/µs
VGS = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20
Reverse Drain Current I DR (A)


Typical Capacitance vs.
Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
10000
3000
1000
300
100
30
10
0
10
20
30
40
50
Drain to Source Voltage VDS (V)

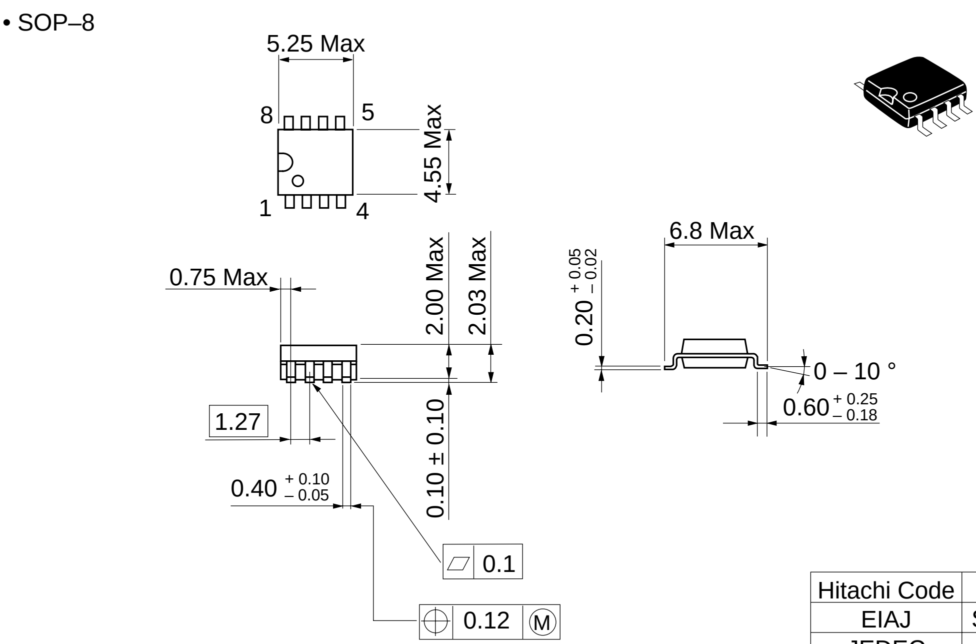

Dynamic Input Characteristics
I D = 3.5 A
V DD = 5 V
10 V
25 V
VDS
VGS
V DD = 25 V
10 V
5 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
50
40
30
20
10
0
4
8
12
16
20
Gate Charge Qg (nc)


Switching Characteristics
VGS = 4 V, VDD ≒ 10 V
PW = 3 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
Switching Time t (ns)
1000
500
200
100
50
20
10
0.2
0.5
1
2
5
10
20
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT2010F Target Specification

Silicon N Channel Power MOS FET

HITACHI

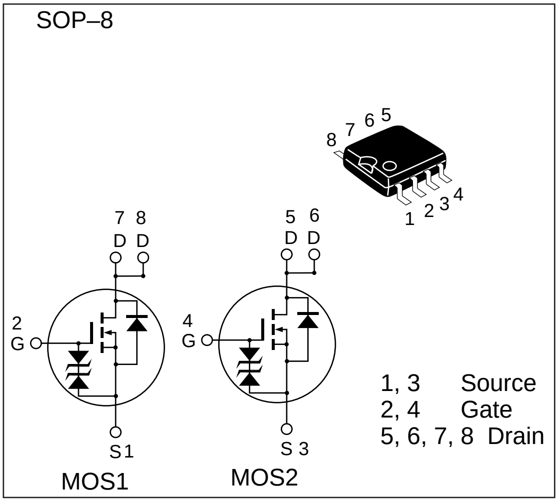
1st. Edition
May 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting



Ordering Information

Hitachi Code	FP–8D
EIAJ Code	SC–527–8A
JEDEC Code	—

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	3.5	A
Drain peak current	$I_{D(pulse)}$*	14	A
Channel dissipation	Pch***	1.5	W
Channel dissipation	Pch**	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

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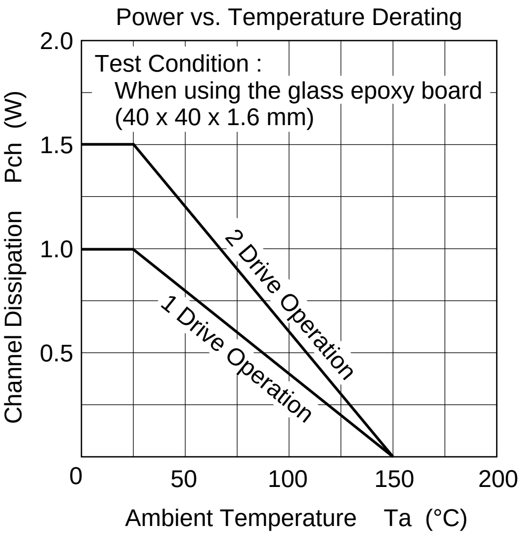
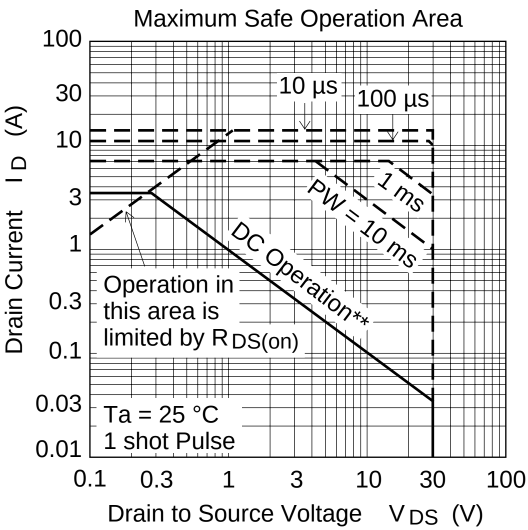
Table 2 Electrical Characteristics (Ta = 25°C)

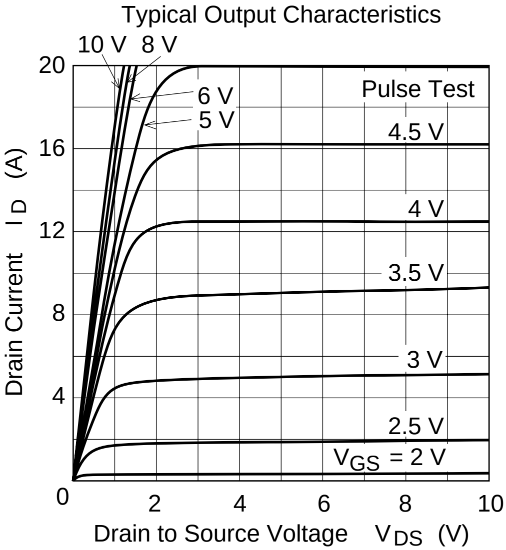
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.075	Ω	I_D = 2A V_{GS} = 10V *
		—	0.09	0.13	Ω	I_D = 2A V_{GS} =4V *
Forward tramsfer admittance	$\lvert y_{fs} \rvert$	3	4.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	470	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	330	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	95	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	90	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	45	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 3.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	45	—	ns	I_F = 3.5 A, V_{GS} = 0 diF / dt = 20A / µs

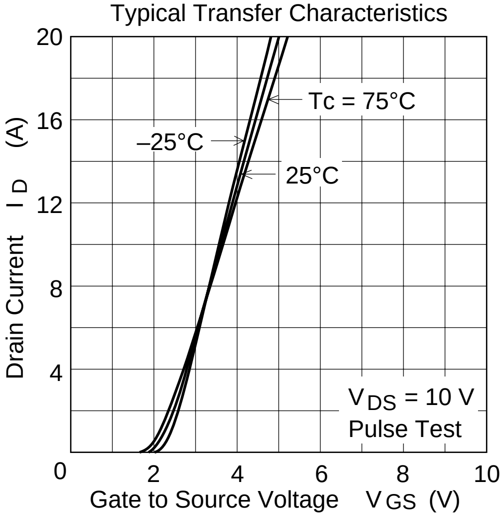
* Pulse Test

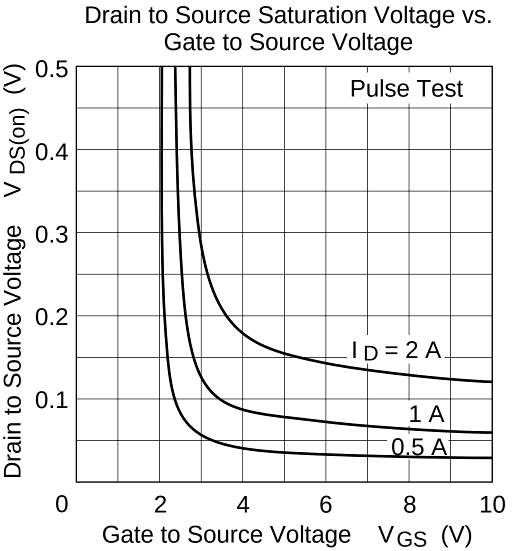


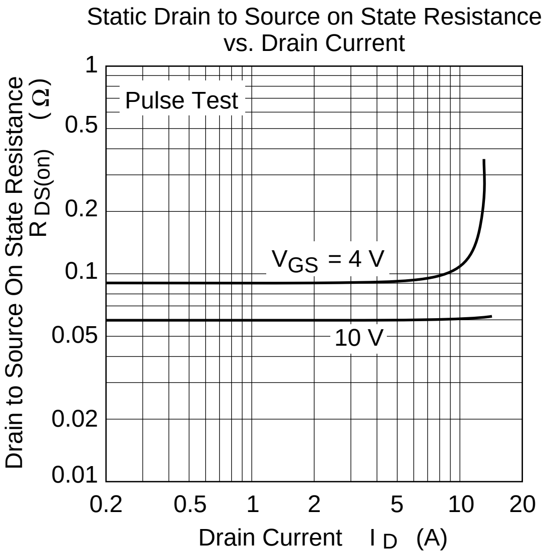


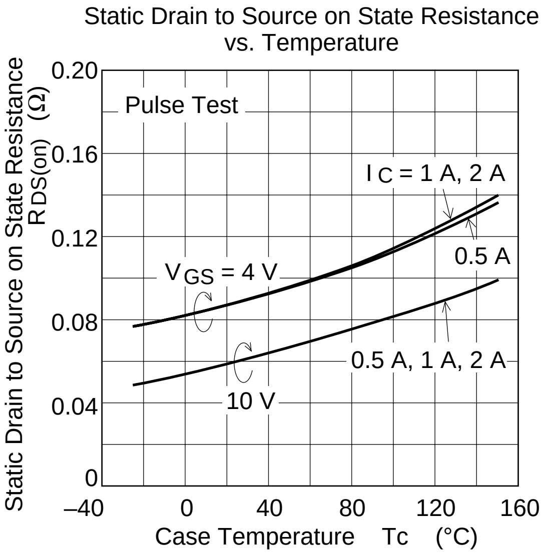
** 1 Drive Operation
When using the glass epoxy board
(40 x 40 x 1.6 mm)

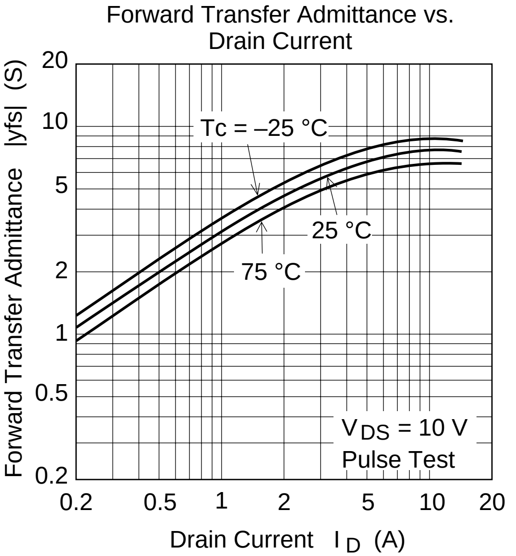


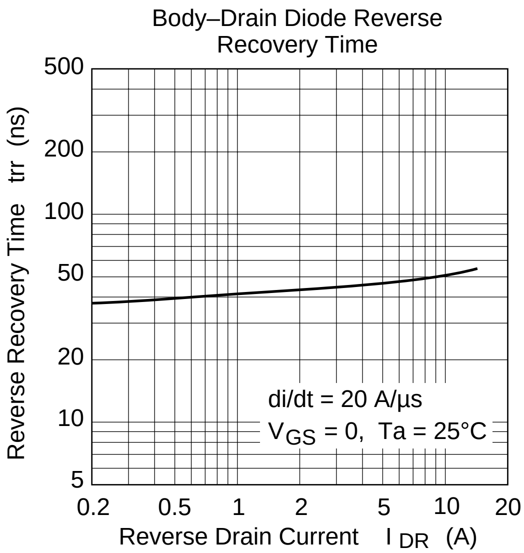


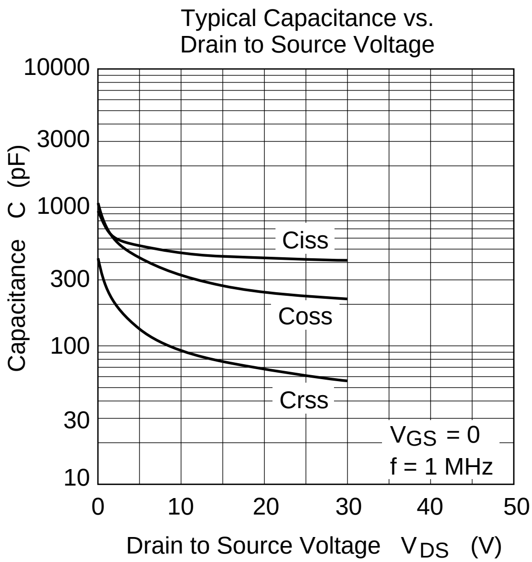

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Pulse Test
I D = 2 A
1 A
0.5 A
Drain to Source Voltage V DS(on) (V)
Gate to Source Voltage V GS (V)
0
0.1
0.2
0.3
0.4
0.5
2
4
6
8
10

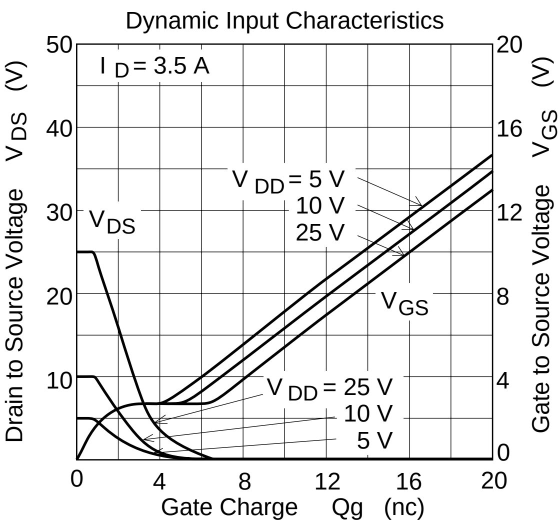

Static Drain to Source on State Resistance
vs. Drain Current
Pulse Test
VGS = 4 V
10 V
Drain to Source On State Resistance R DS(on) (Ω)
Drain Current I D (A)
1
0.5
0.2
0.1
0.05
0.02
0.01
0.2
0.5
1
2
5
10
20

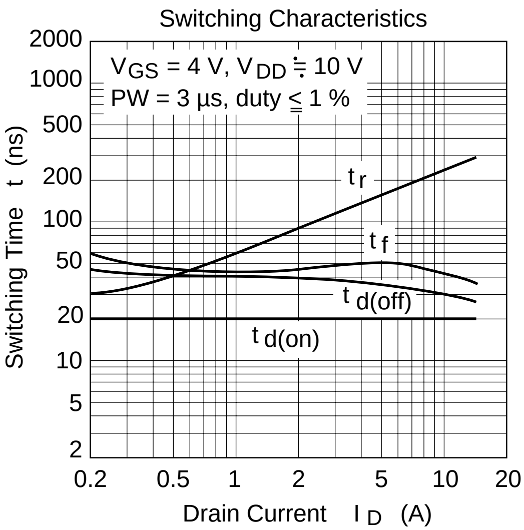

Static Drain to Source on State Resistance
vs. Temperature
Pulse Test
I C = 1 A, 2 A
0.5 A
VGS = 4 V
0.5 A, 1 A, 2 A
10 V
Static Drain to Source on State Resistance RDS(on) (Ω)
Case Temperature Tc (°C)
0.20
0.16
0.12
0.08
0.04
0
–40
0
40
80
120
160

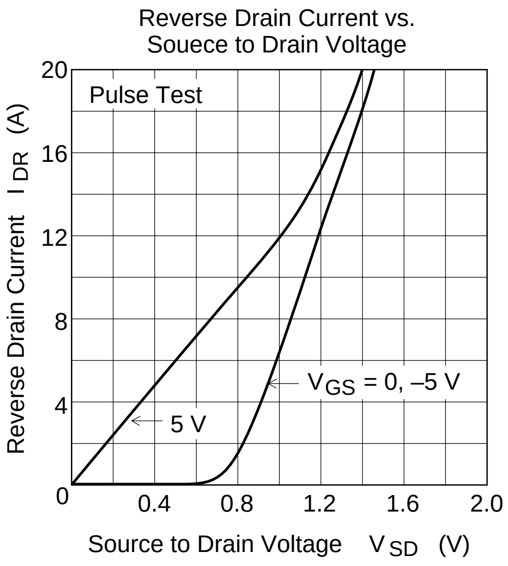

Forward Transfer Admittance vs.
Drain Current
Tc = –25 °C
25 °C
75 °C
VDS = 10 V
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I D (A)
20
10
5
2
1
0.5
0.2
0.2
0.5
1
2
5
10
20


Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
di/dt = 20 A/μs
VGS = 0, Ta = 25°C
500
200
100
50
20
10
5
0.2
0.5
1
2
5
10
20


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage VDS (V)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
10000
3000
1000
300
100
30
10
0
10
20
30
40
50


Dynamic Input Characteristics
I D = 3.5 A
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
VDS
VGS
V DD = 5 V
10 V
25 V
V DD = 25 V
10 V
5 V
50
40
30
20
10
0
4
8
12
16
20
20
16
12
8
4
0

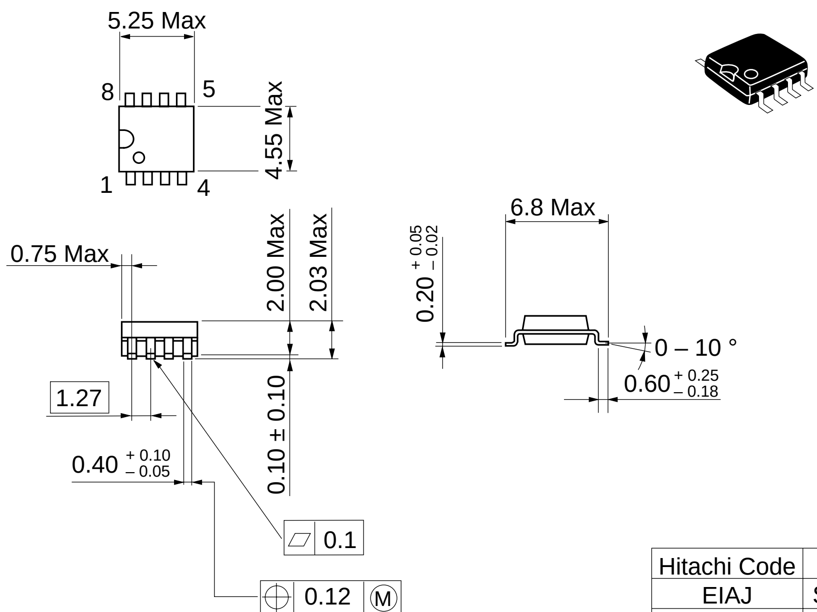

Switching Characteristics
VGS = 4 V, VDD ≒ 10 V
PW = 3 μs, duty ≤ 1 %
Switching Time t (ns)
Drain Current I D (A)
t r
t f
t d(off)
t d(on)
2000
1000
500
200
100
50
20
10
5
2
0.2
0.5
1
2
5
10
20



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT3001F

Silicon N Channel / P Channel Complementary Power MOS FET

HITACHI

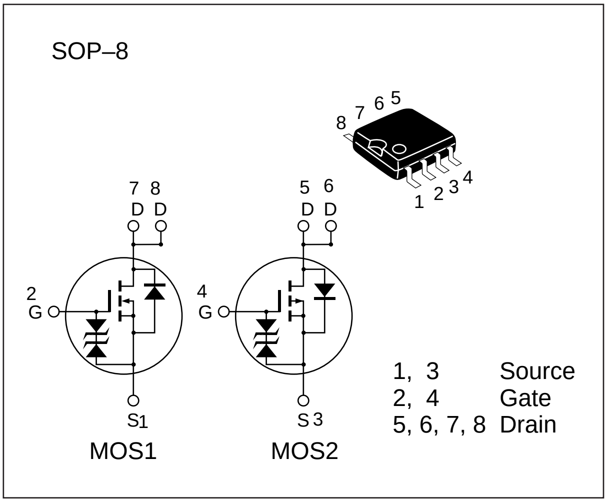
2nd Edition
Jun. 1995

Application

Power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting



Ordering Information

Hitachi Cord	FP–8D
EIAJ Cord	SC–527–8A
JEDEC Cord	—

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	30	–30	V
Gate to source voltage	V_{GSS}	±10	±10	V
Drain current	I_D	2.5	–2.5	A
Drain peak current	$I_{D(pulse)}$*	10	–10	A
Channel dissipation	Pch***	1.5		W
Channel dissipation	Pch**	1		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 1 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)
*** 2 Drive operation When using the glass epoxy board (40 x 40 x 1.6 mm)

Table 2 Electrical Characteristics N Channel (Ta = 25°C)

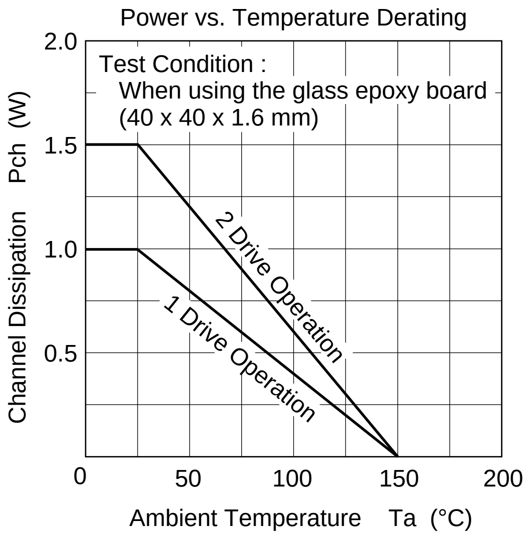
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.1	0.15	Ω	I_D = 2A V_{GS} = 4V *
		—	0.13	0.22	Ω	I_D = 2A V_{GS} = 2.5V *
Forward transfer admittance	$\|y_{fs}\|$	2	4	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	380	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	200	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	70	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	80	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	70	—	ns	
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	—	V	I_F = 2.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = 2.5A, V_{GS} = 0 diF / dt = 20 A / μs

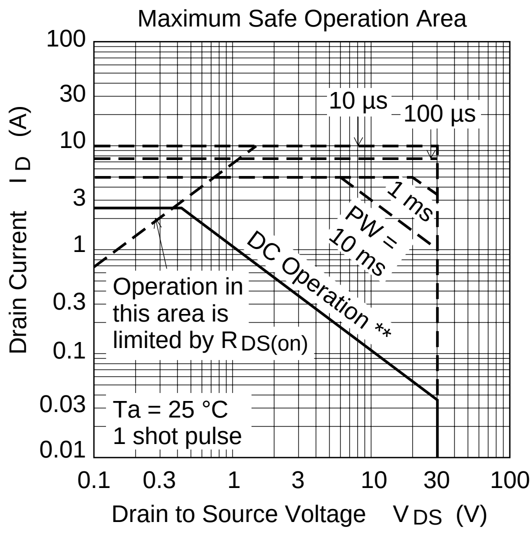
* Pulse Test

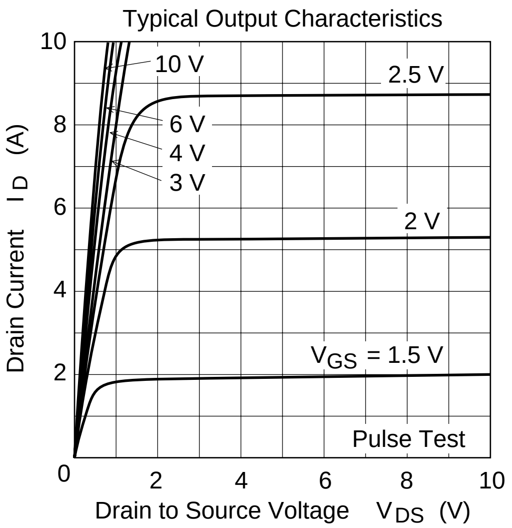
Table 2 Electrical Characteristics P Channel (Ta = 25°C)

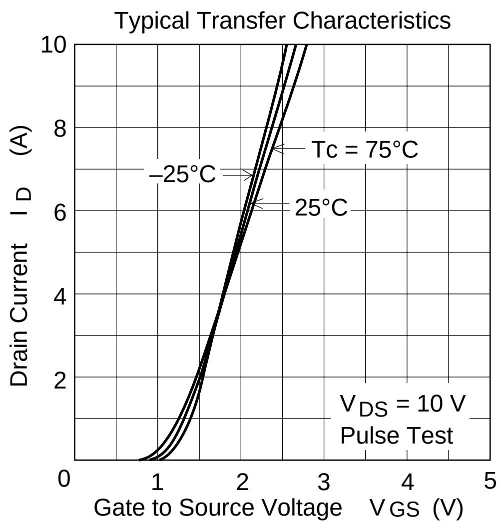
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	I_D = –2 A V_{GS} = –4 V *
		—	0.17	0.24	Ω	I_D = –2 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.0	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	720	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	345	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	115	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	16	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	100	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	120	—	ns	
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –2.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	100	—	ns	I_F = –2.5 A, V_{GS} = 0 diF / dt = 20A / µs

* Pulse Test

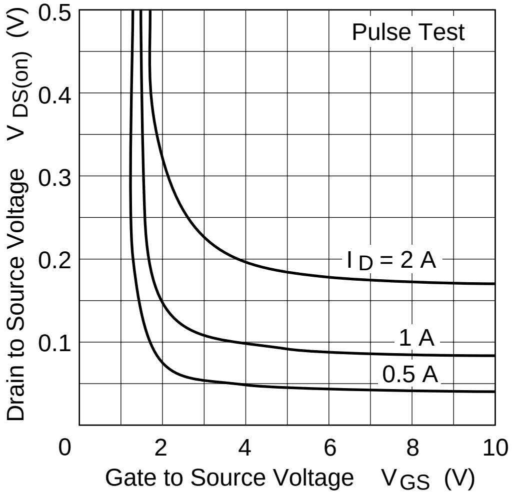

Power vs. Temperature Derating
Test Condition :
When using the glass epoxy board
(40 x 40 x 1.6 mm)
2 Drive Operation
1 Drive Operation
Channel Dissipation Pch (W)
Ambient Temperature Ta (°C)
2.0
1.5
1.0
0.5
0
50
100
150
200


Maximum Safe Operation Area
10 μs
100 μs
1 ms
PW = 10 ms
DC Operation **
Operation in this area is limited by R DS(on)
Ta = 25 °C
1 shot pulse
Drain Current I D (A)
Drain to Source Voltage V DS (V)
100
30
10
3
1
0.3
0.1
0.03
0.01
0.1
0.3
1
3
10
30
100

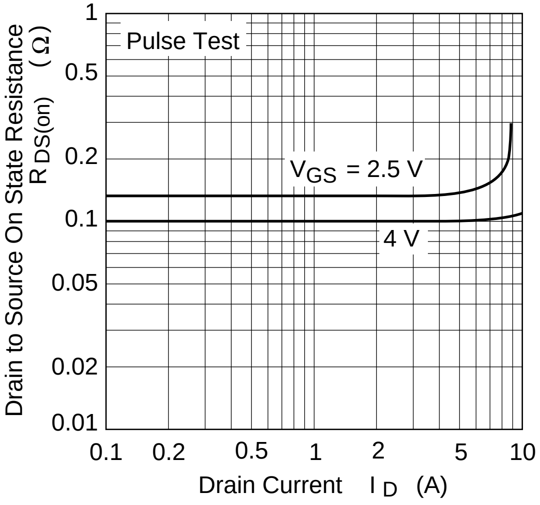

Typical Output Characteristics
10 V
6 V
4 V
3 V
2.5 V
2 V
VGS = 1.5 V
Pulse Test
Drain Current I D (A)
Drain to Source Voltage V DS (V)
10
8
6
4
2
0
2
4
6
8
10


Typical Transfer Characteristics
Tc = 75°C
–25°C
25°C
VDS = 10 V
Pulse Test
Drain Current I D (A)
Gate to Source Voltage V GS (V)
10
8
6
4
2
0
1
2
3
4
5

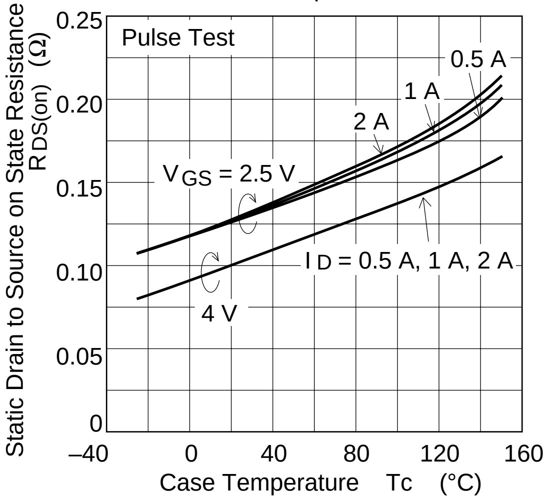
Drain to Source Saturation Voltage vs. Gate to Source Voltage



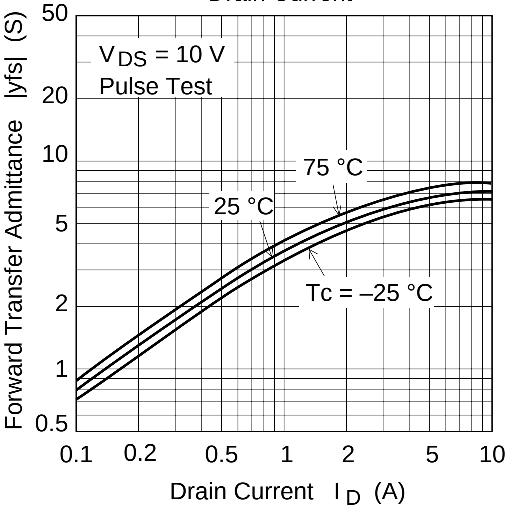
Static Drain to Source on State Resistance vs. Drain Current

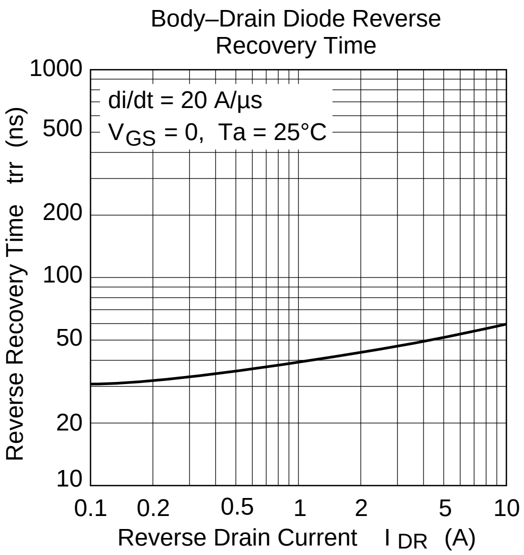


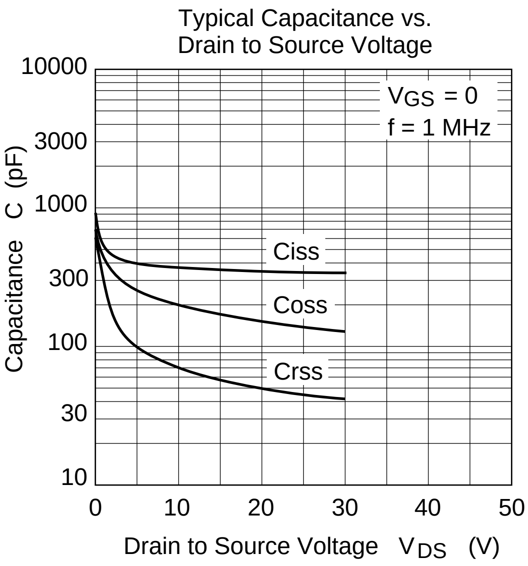
Static Drain to Source on State Resistance vs. Temperature

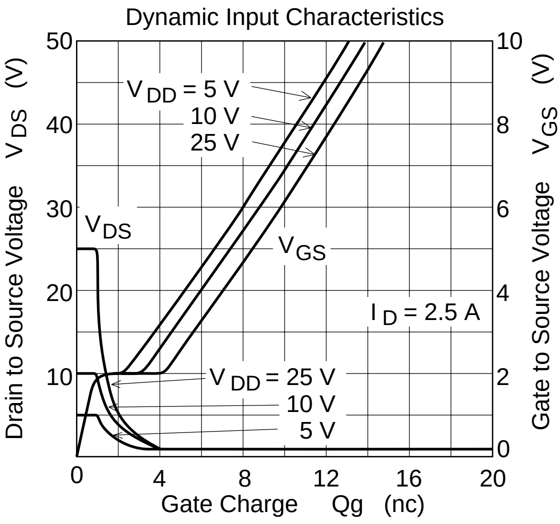


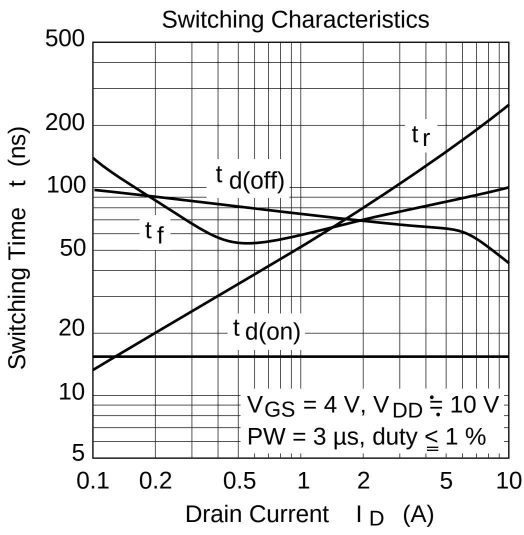
Forward Transfer Admittance vs. Drain Current

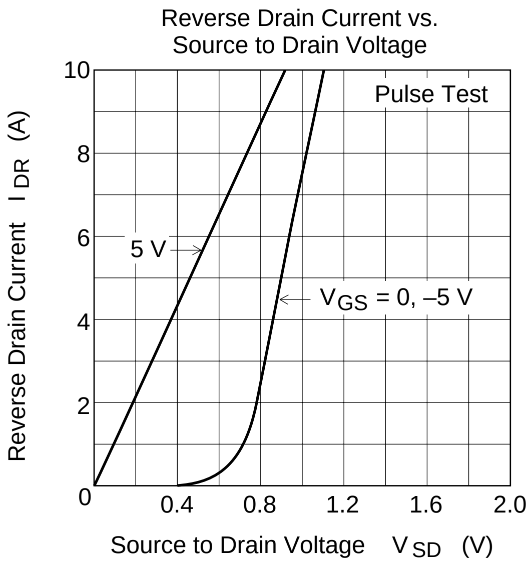


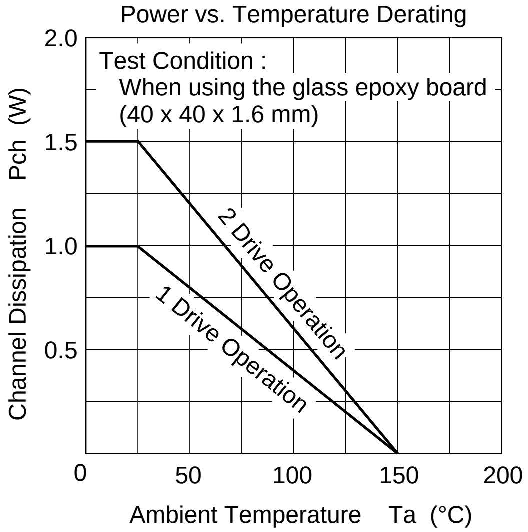

Body–Drain Diode Reverse
Recovery Time
di/dt = 20 A/µs
V_{GS} = 0, Ta = 25°C
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.2
0.5
1
2
5
10
Reverse Drain Current I_{DR} (A)

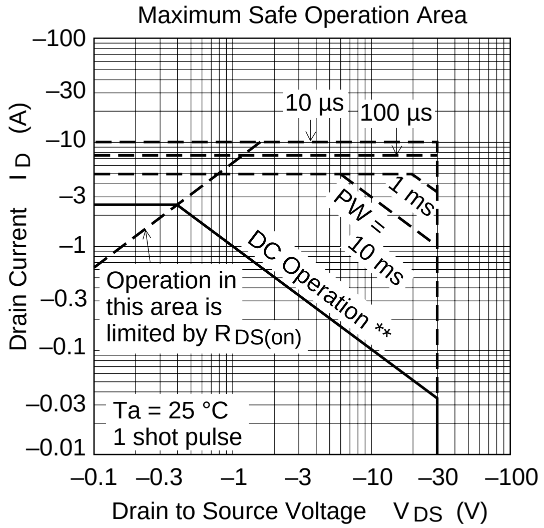

Typical Capacitance vs.
Drain to Source Voltage
V_{GS} = 0
f = 1 MHz
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
0
10
20
30
40
50
Drain to Source Voltage V_{DS} (V)

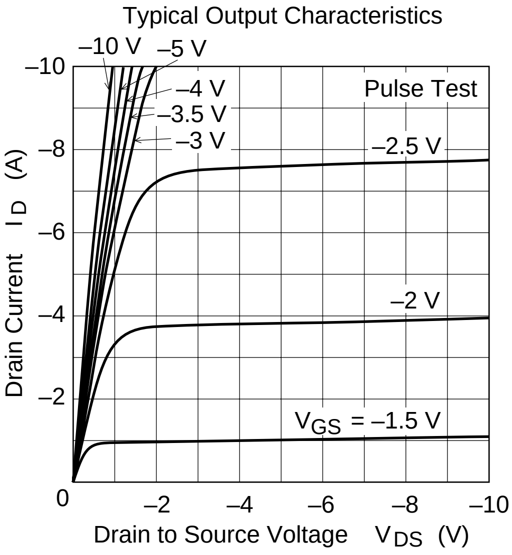

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
50
40
30
20
10
10
8
6
4
2
0
V_{DD} = 5 V
10 V
25 V
V_{DS}
V_{GS}
I_D = 2.5 A
V_{DD} = 25 V
10 V
5 V
0
4
8
12
16
20
Gate Charge Qg (nc)

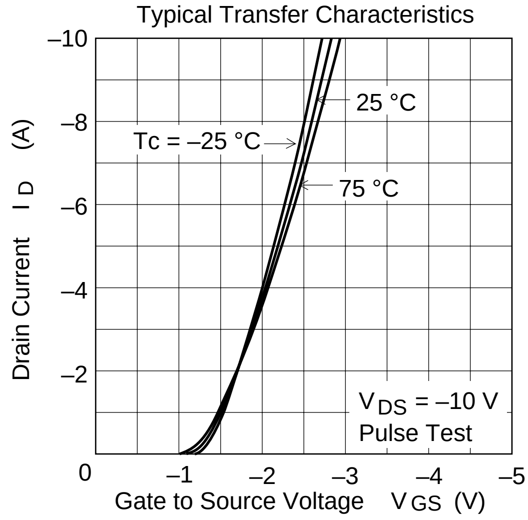

Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t_r
$t_{d(off)}$
t_f
$t_{d(on)}$
V_{GS} = 4 V, V_{DD} ≒ 10 V
PW = 3 µs, duty ≤ 1 %
0.1
0.2
0.5
1
2
5
10
Drain Current I_D (A)


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
5 V
VGS = 0, –5 V
Reverse Drain Current I DR (A)
Source to Drain Voltage V SD (V)
10
8
6
4
2
0
0.4
0.8
1.2
1.6
2.0

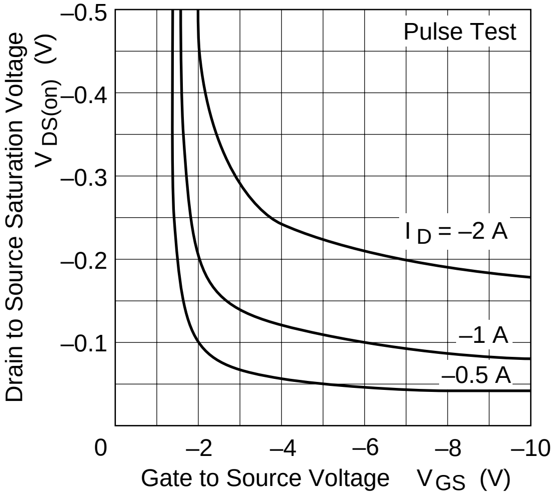

Power vs. Temperature Derating
Test Condition :
When using the glass epoxy board
(40 x 40 x 1.6 mm)
2 Drive Operation
1 Drive Operation
Channel Dissipation Pch (W)
Ambient Temperature Ta (°C)
2.0
1.5
1.0
0.5
0
50
100
150
200


Maximum Safe Operation Area
10 μs
100 μs
1 ms
PW = 10 ms
DC Operation **
Operation in this area is limited by R DS(on)
Ta = 25 °C
1 shot pulse
Drain Current I D (A)
Drain to Source Voltage V DS (V)
–100
–30
–10
–3
–1
–0.3
–0.1
–0.03
–0.01
–0.1
–0.3
–1
–3
–10
–30
–100

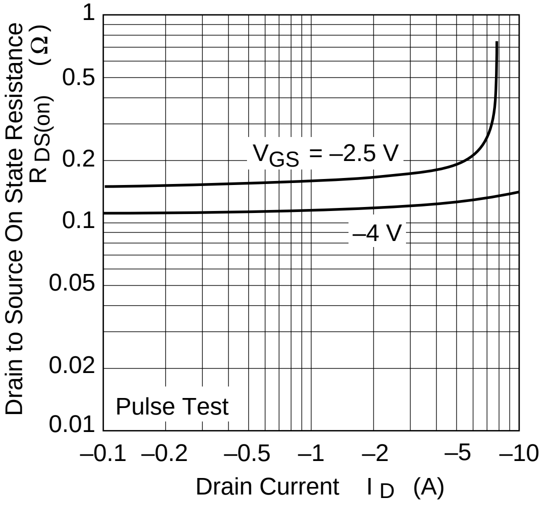

Typical Output Characteristics
–10 V
–5 V
–4 V
–3.5 V
–3 V
Pulse Test
–2.5 V
–2 V
VGS = –1.5 V
Drain Current I D (A)
Drain to Source Voltage V DS (V)
–10
–8
–6
–4
–2
0
–2
–4
–6
–8
–10


Typical Transfer Characteristics
25 °C
Tc = –25 °C
75 °C
VDS = –10 V
Pulse Test
Drain Current I D (A)
Gate to Source Voltage V GS (V)
–10
–8
–6
–4
–2
0
–1
–2
–3
–4
–5

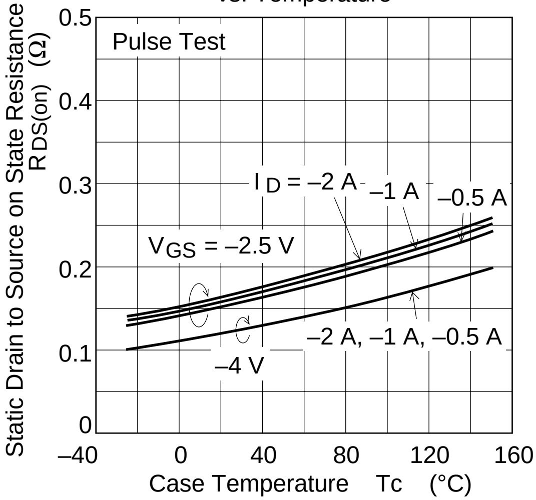
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



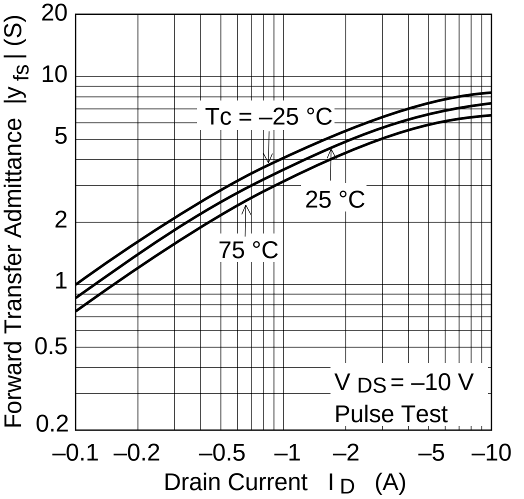
Static Drain to Source on State Resistance
vs. Drain Current

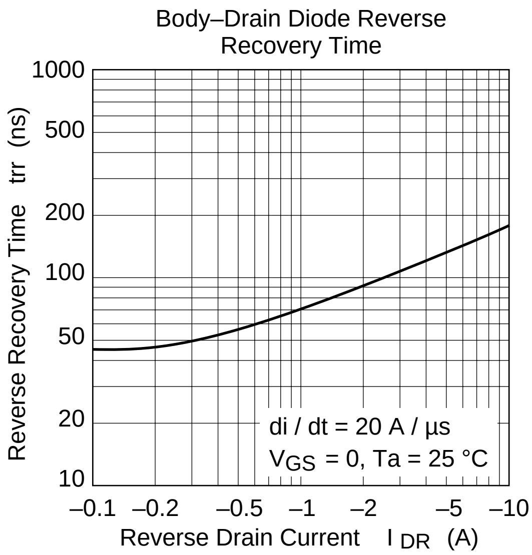


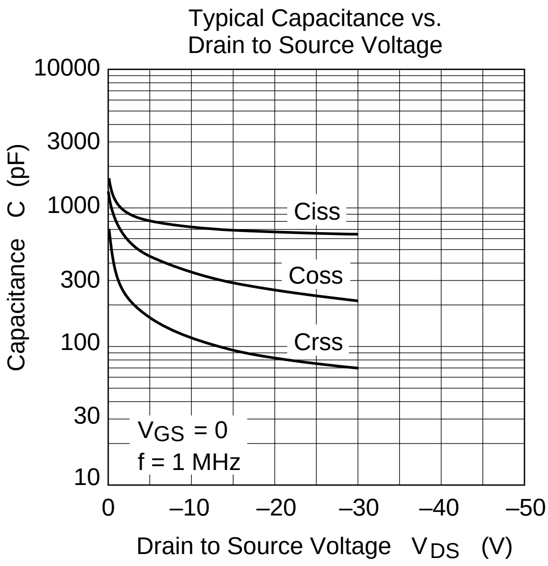
Static Drain to Source on State Resistance
vs. Temperature

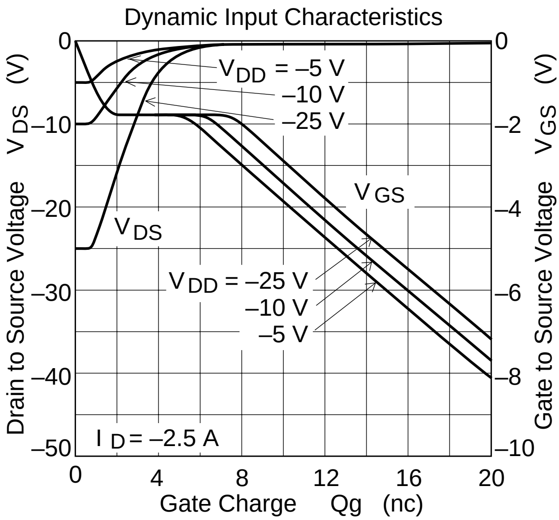


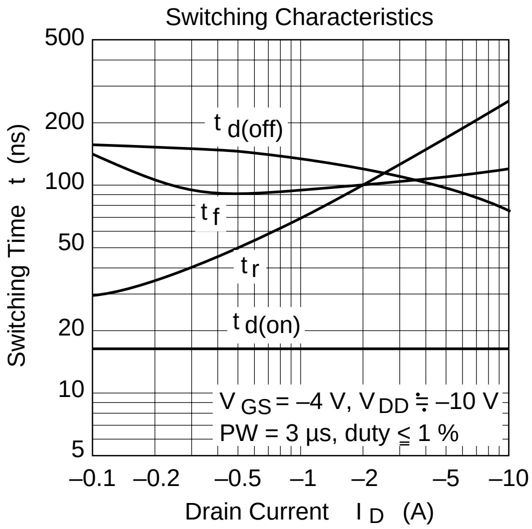
Forward Transfer Admittance vs.
Drain Current

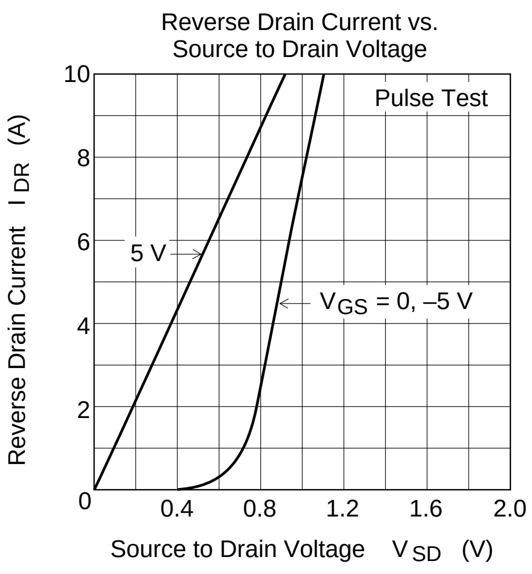



Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
di / dt = 20 A / µs
VGS = 0, Ta = 25 °C
–0.1 –0.2 –0.5 –1 –2 –5 –10
Reverse Drain Current I DR (A)


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
0 –10 –20 –30 –40 –50
Drain to Source Voltage VDS (V)

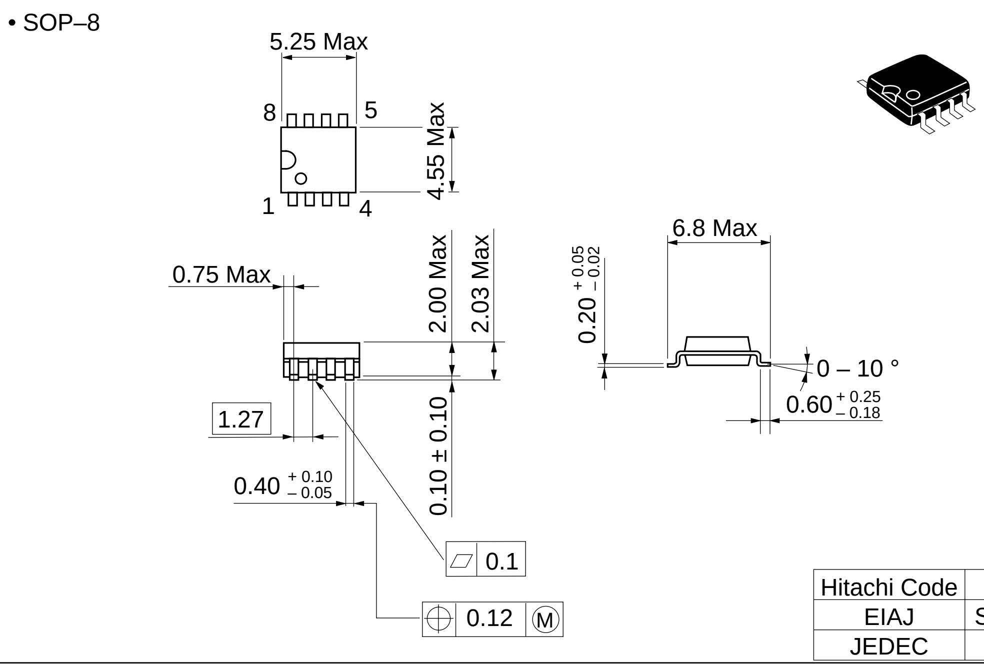

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
0
–10
–20
–30
–40
–50
0
–2
–4
–6
–8
–10
VDD = –5 V
–10 V
–25 V
VGS
VDS
VDD = –25 V
–10 V
–5 V
I D = –2.5 A
0 4 8 12 16 20
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
500
200
100
50
20
10
5
t d(off)
t f
t r
t d(on)
V GS = –4 V, V DD ≒ –10 V
PW = 3 µs, duty ≦ 1 %
–0.1 –0.2 –0.5 –1 –2 –5 –10
Drain Current I D (A)



Package Dimensions

Unit : mm



Hitachi Code	FP–8D
EIAJ	SC–527–8A
JEDEC	—

HAT1020R Target Specification

Silicon P Channel Power MOS FET

HITACHI

2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

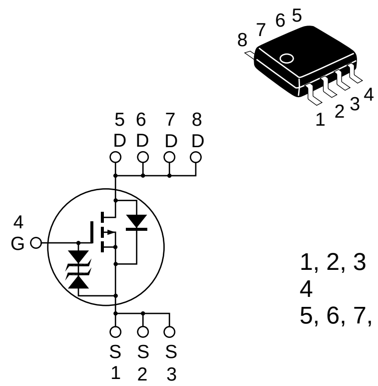
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–4.5	A
Drain peak current	$I_{D(pulse)}$*	–18	A
Body–drain diode reverse drain current	I_{DR}	–4.5	A
Channel dissipation	Pch**	2.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

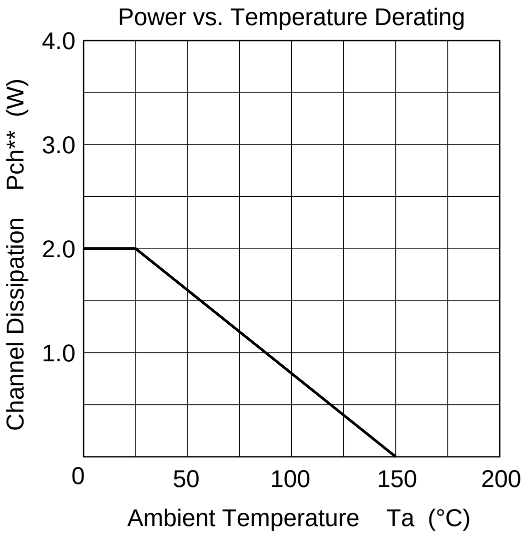
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using surface mounted on FR4 board

Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.05)	0.07	Ω	I_D = –3A V_{GS} = –10V *
		—	(0.09)	0.13	Ω	I_D = –3A V_{GS} = –4V *
Forward transfer admittance	$\|y_{fs}\|$	(5.0)	(8.0)	—	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(670)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(440)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(170)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(35)	—	ns	V_{GS} = –4 V, I_D = –3 A
Rise time	t_r	—	(200)	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(35)	—	ns	
Fall time	t_f	—	(60)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(–0.8)	—	V	I_F = –4.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(60)	—	ns	I_F = –4.5A, V_{GS} = 0 diF / dt = 20 A / µs

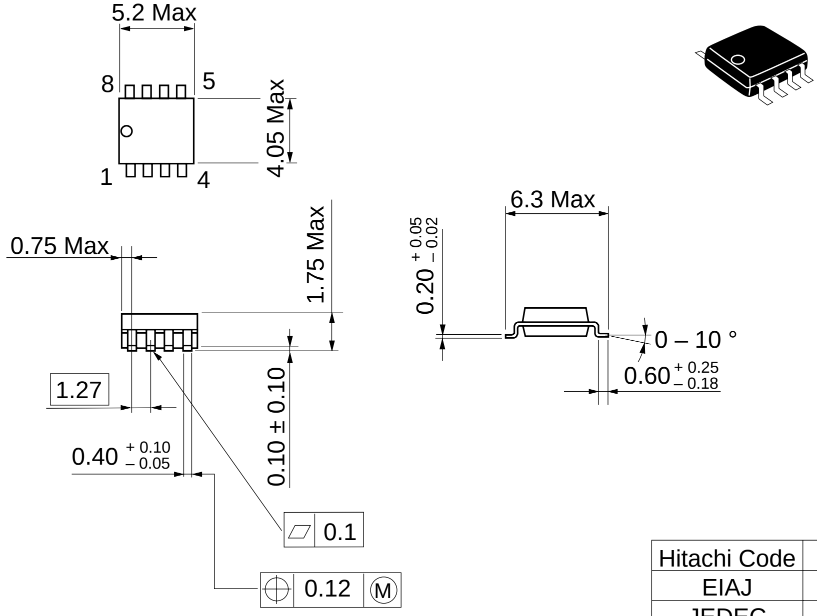
* Pulse Test



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT1023R Target Specification

Silicon P Channel Power MOS FET

HITACHI

2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

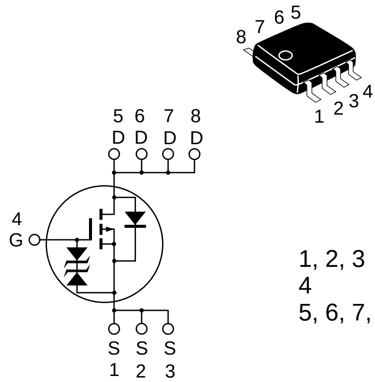
Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

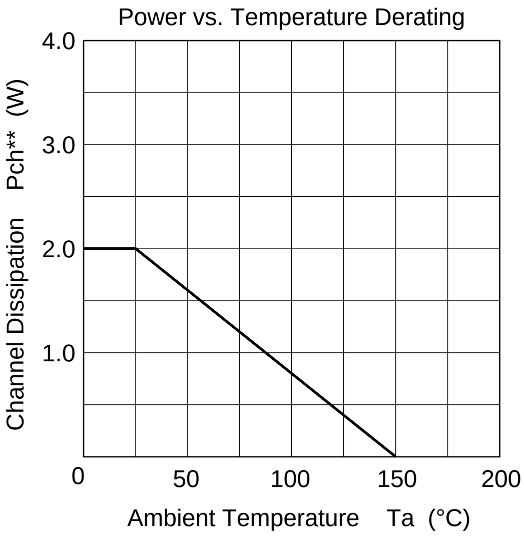
Item	**Symbol**	**Ratings**	**Unit**
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–6.5	A
Drain peak current	$I_{D(pulse)}$*	–26	A
Body–drain diode reverse drain current	I_{DR}	–6.5	A
Channel dissipation	Pch**	2.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** When using surface mounted on FR4 board

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.023)	0.04	Ω	I_D = –3A V_{GS} = –4V *
		—	(0.04)	0.06	Ω	I_D = –3A V_{GS} = –2.5V *
Forward transfer admittance	$\|y_{fs}\|$	(6)	(10)	—	S	I_D = –3 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(1200)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(900)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(350)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(20)	—	ns	V_{GS} = –4 V, I_D = –3 A
Rise time	t_r	—	(300)	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(350)	—	ns	
Fall time	t_f	—	(400)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(–0.8)	—	V	I_F = –6.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(200)	—	ns	I_F = –6.5A, V_{GS} = 0 diF / dt = 20 A / µs

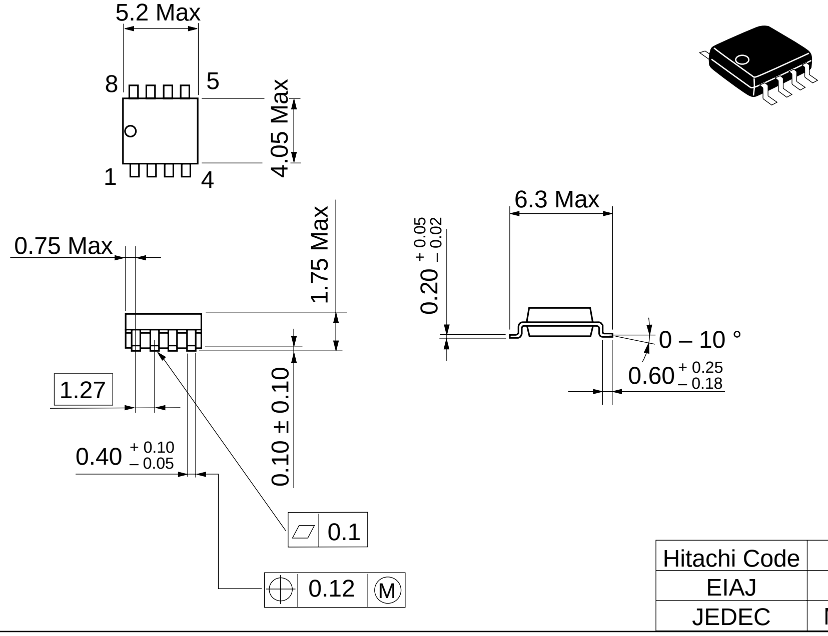
* Pulse Test



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT1024R Target Specification
Silicon P Channel Power MOS FET

HITACHI

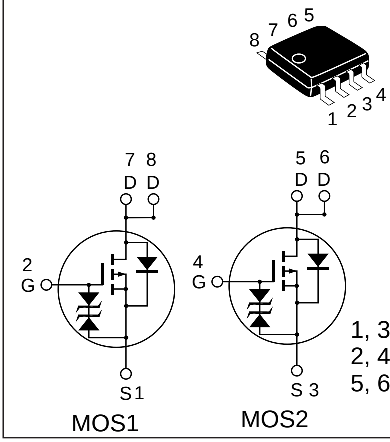
2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting



Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–2.5	A
Drain peak current	$I_{D(pulse)}$*	–10	A
Channel dissipation	Pch***	2.0	W
Channel dissipation	Pch**	1.3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

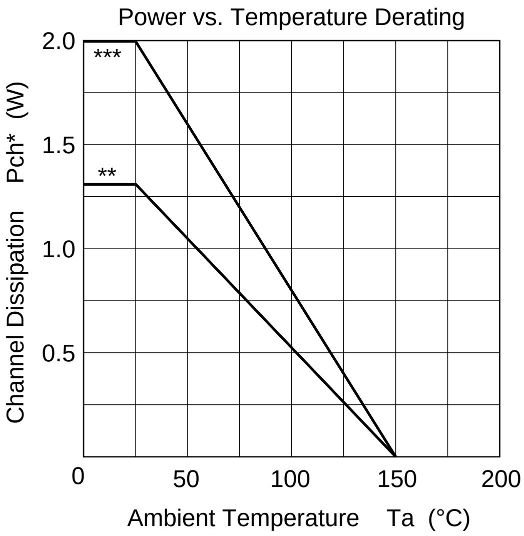
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 1 Drive operation : *** 2 Drive operation When using surface mounted on FR4 board

Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.18)	0.25	Ω	I_D = –2A V_{GS} = –10V *
		—	(0.25)	0.4	Ω	I_D = –2A V_{GS} = –4V *
Forward transfer admittance	$\|y_{fs}\|$	(2.5)	(4.0)	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(250)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(150)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(60)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(10)	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	(70)	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(15)	—	ns	
Fall time	t_f	—	(20)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(–0.9)	—	V	I_F = –2.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	I_F = –2.5A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test

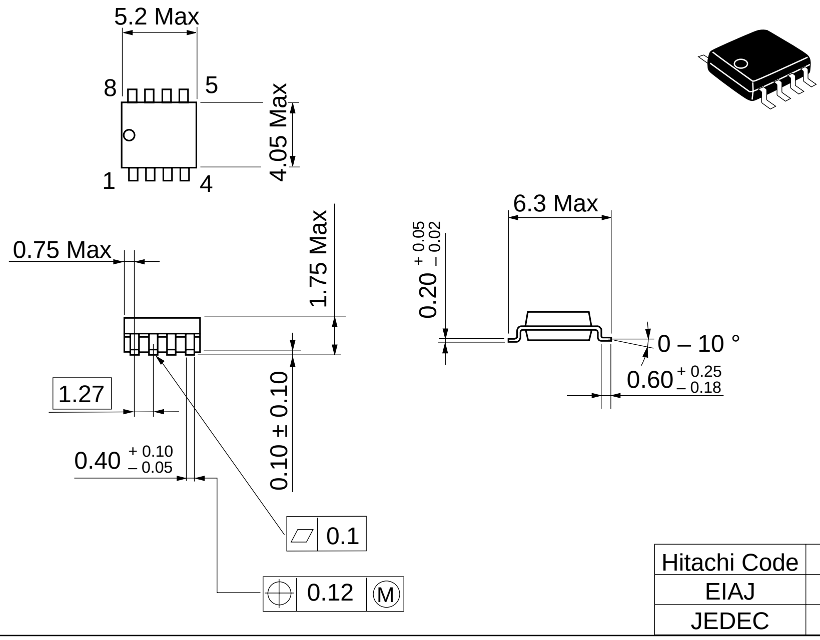


*	When using surface mounted on FR4 board
**	1 Drive Operation
***	2 Drive Operation

Package Dimensions

Unit : mm

• SOP–8



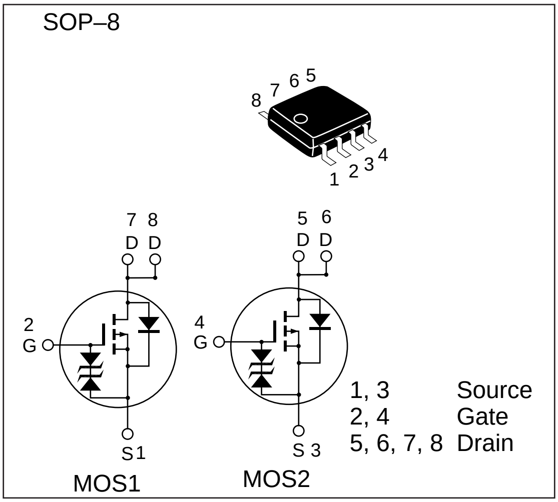
Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT1025R Target Specification

Silicon P Channel Power MOS FET

HITACHI

2nd. Edition
May. 1995
Preliminary



Application

High speed power switching

Features

- Low on–resistance
- Capable of 2.5V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

Table 1 Absolute Maximum Ratings (Ta = 25°C)

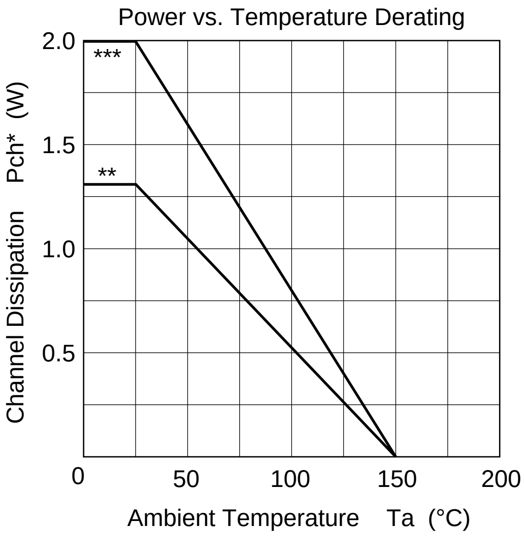
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	–4	A
Drain peak current	$I_{D(pulse)}$*	–16	A
Channel dissipation	Pch***	2.0	W
Channel dissipation	Pch**	1.3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation : *** 2 Drive operation When using surface mounted on FR4 board

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –20 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.09)	0.11	Ω	I_D = –2A V_{GS} = –4V *
		—	(0.135)	0.19	Ω	I_D = –2A V_{GS} = –2.5V *
Forward transfer admittance	$\lvert y_{fs} \rvert$	(4.0)	(6.0)	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(530)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(350)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(150)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(20)	—	ns	V_{GS} = –4 V, I_D = –2 A
Rise time	t_r	—	(90)	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(110)	—	ns	
Fall time	t_f	—	(100)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(–0.9)	—	V	I_F = –4A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(150)	—	ns	I_F = –4A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test

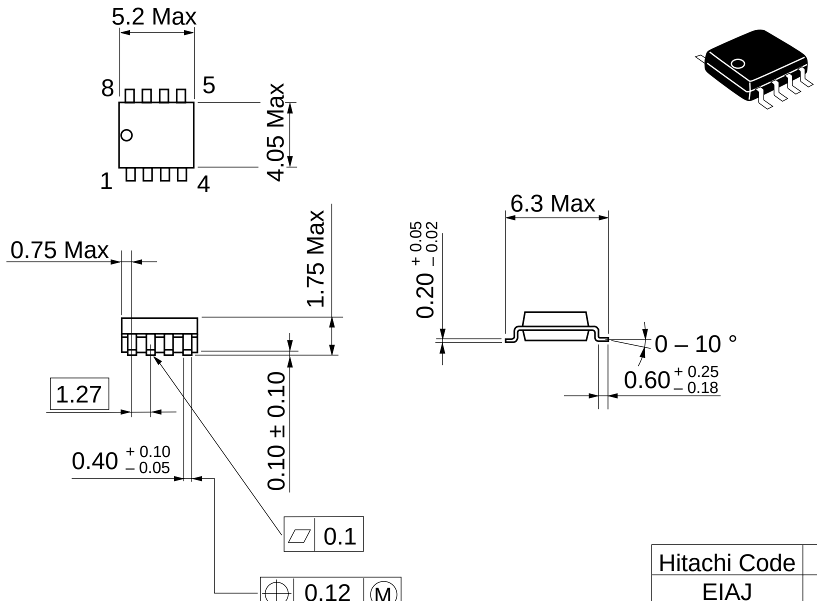


* When using surface mounted on FR4 board
** 1 Drive Operation
*** 2 Drive Operation

Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT2016R Target Specification

Silicon N Channel Power MOS FET

HITACHI

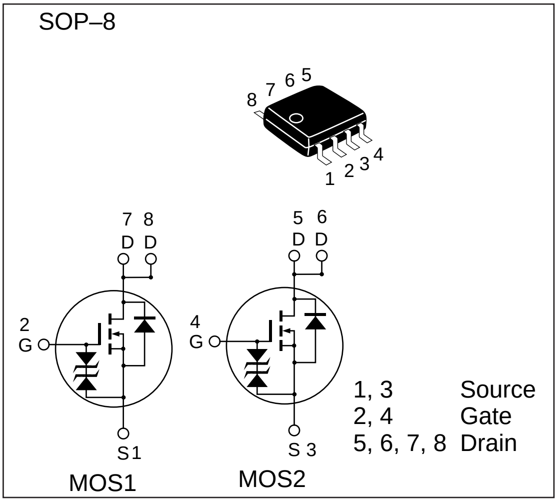
2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting



Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

Table 1 Absolute Maximum Ratings (Ta = 25°C)

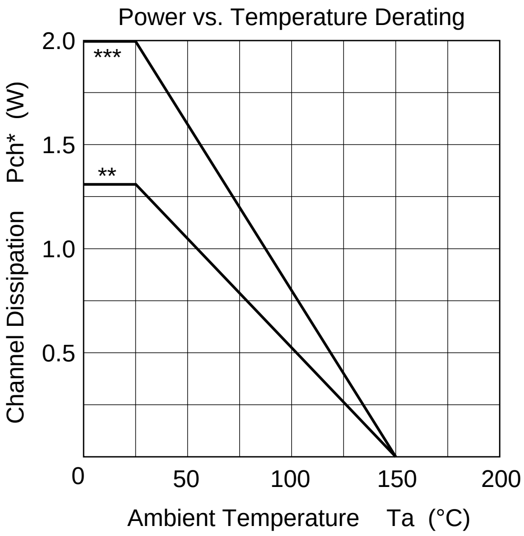
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	20	A
Channel dissipation	Pch***	2.0	W
Channel dissipation	Pch**	1.3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation : *** 2 Drive operation When using surface mounted on FR4 board

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.04)	0.05	Ω	I_D = 3A V_{GS} = 10V *
		—	(0.055)	0.08	Ω	I_D = 3A V_{GS} = 4V *
Forward transfer admittance	$\|y_{fs}\|$	(4.0)	(6.5)	—	S	I_D = 3 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(350)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(220)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(85)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(15)	—	ns	V_{GS} = 4 V, I_D = 3 A
Rise time	t_r	—	(100)	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(40)	—	ns	
Fall time	t_f	—	(35)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(0.8)	—	V	I_F = 5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	I_F = 5A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test

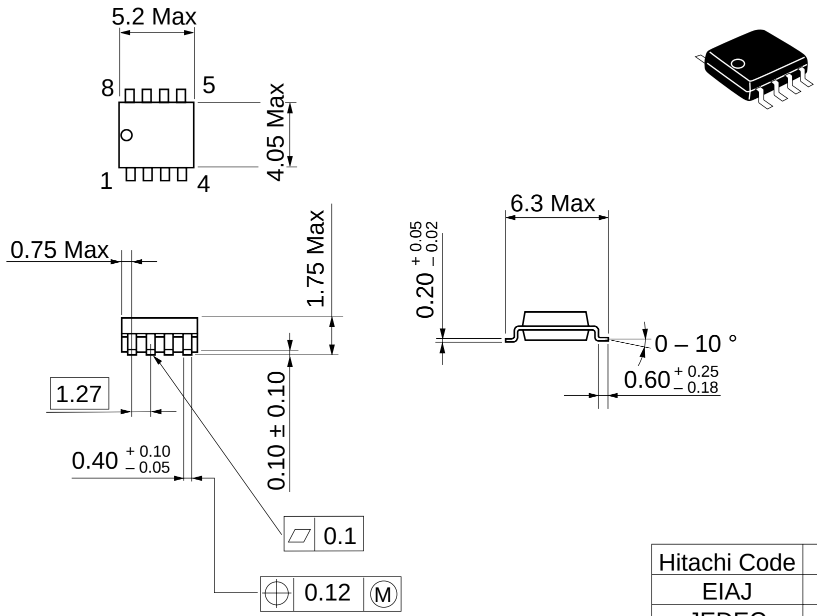


* When using surface mounted on FR4 board
** 1 Drive Operation
*** 2 Drive Operation

Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT2020R Target Specification

Silicon N Channel Power MOS FET

HITACHI

2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

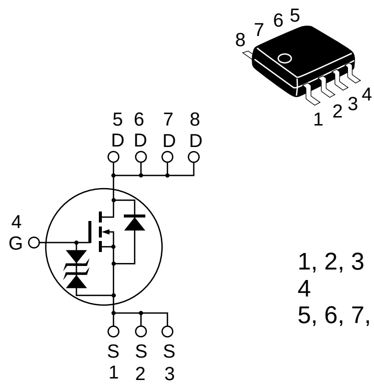
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

SOP–8



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D(pulse)}$*	28	A
Body–drain diode reverse drain current	I_{DR}	7	A
Channel dissipation	Pch**	2	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

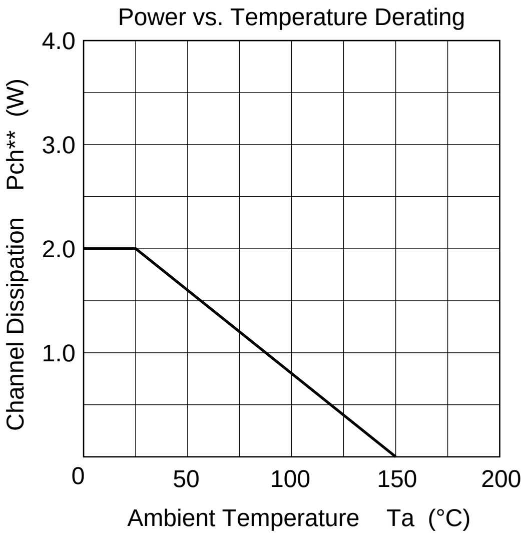
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using surface mounted on FR4 board

Hitachi semiconductor

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.026)	0.03	Ω	I_D = 4A V_{GS} = 10V *
		—	(0.04)	0.05	Ω	I_D = 4A V_{GS} = 4V *
Forward transfer admittance	$\|y_{fs}\|$	(6)	(10)	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(570)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(370)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(140)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(20)	—	ns	V_{GS} = 4 V, I_D = 4 A
Rise time	t_r	—	(160)	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(65)	—	ns	
Fall time	t_f	—	(60)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(0.8)	—	V	I_F = 7A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(60)	—	ns	I_F = 7A, V_{GS} = 0 diF / dt = 20 A / µs

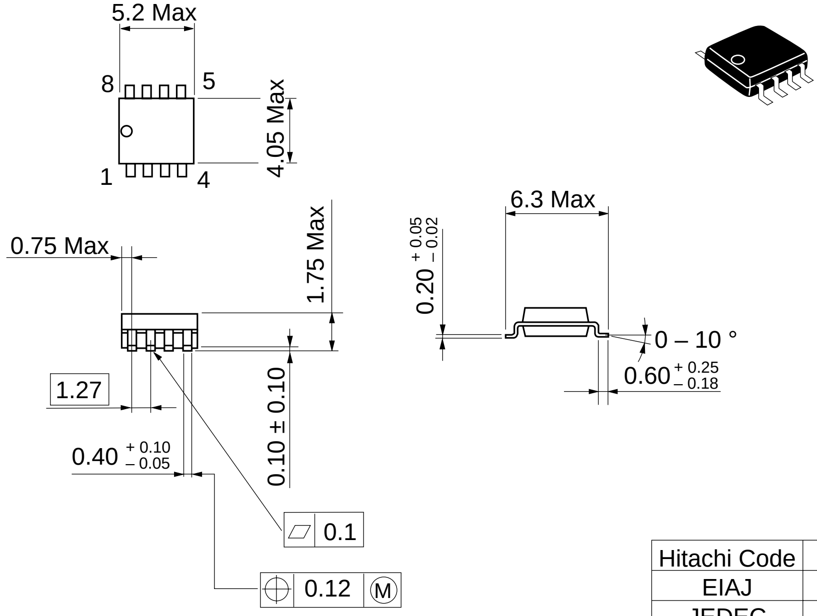
* Pulse Test



Package Dimensions

Unit : mm

• SOP–8



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT2022R Target Specification

Silicon N Channel Power MOS FET

HITACHI

2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

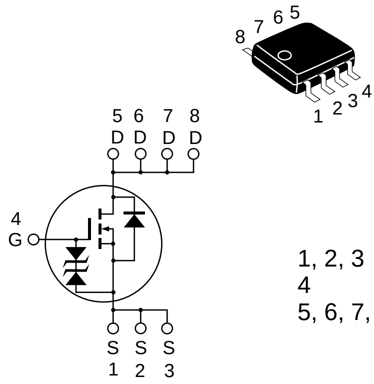
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

SOP–8



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body–drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch**	2.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

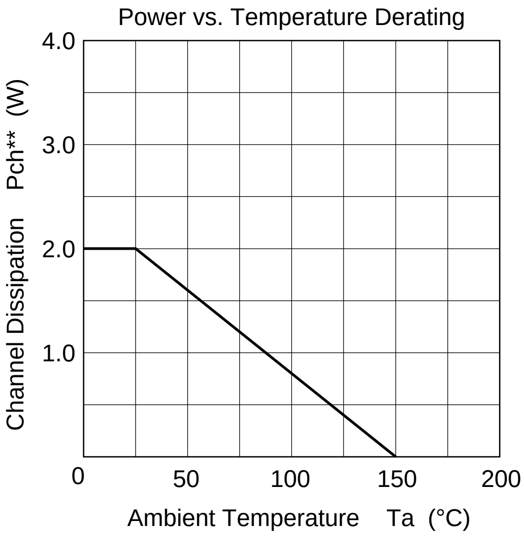
* PW ≤ 10 µs, duty cycle ≤ 1 %
** When using surface mounted on FR4 board

Hitachi

Table 2 Electrical Characteristics (Ta = 25°C)

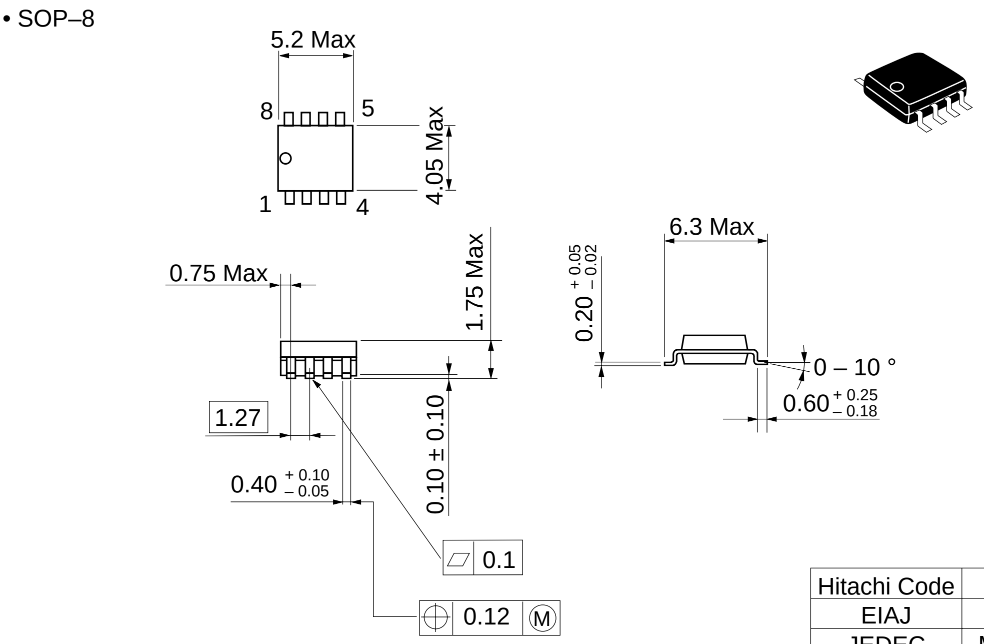
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.011)	0.0135	Ω	I_D = 5A V_{GS} = 10V *
		—	(0.016)	0.02	Ω	I_D = 5A V_{GS} = 4V *
Forward transfer admittance	$\|y_{fs}\|$	(11)	(18)	—	S	I_D = 5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(1250)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(820)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(300)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(35)	—	ns	V_{GS} = 4 V, I_D = 5 A
Rise time	t_r	—	(250)	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(140)	—	ns	
Fall time	t_f	—	(120)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(0.8)	—	V	I_F = 10A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(90)	—	ns	I_F = 10A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test



Package Dimensions

Unit : mm



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

HAT3004R Target Specification

Silicon N and P Channel Power MOS FET

HITACHI

2nd. Edition
May. 1995
Preliminary

Application

High speed power switching

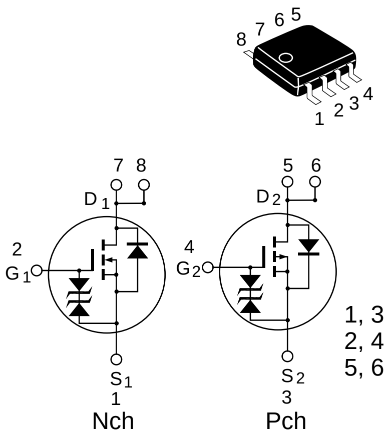
Features

- Low on–resistance
- Capable of 4V gate drive
- Low drive current
- High density mounting

Ordering Information

Hitachi Code	FP–8DA
EIAJ Code	—
JEDEC Code	MS–012AA

SOP–8



1, 3 Source
2, 4 Gate
5, 6, 7, 8 Drain

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	30	–30	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	3.5	–2.5	A
Drain peak current	$I_{D(pulse)}$*	14	–10	A
Channel dissipation	Pch***	2.0		W
Channel dissipation	Pch**	1.3		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** 1 Drive operation : *** 2 Drive operation When using surface mounted on FR4 board

HAT3004R (N channel)

Table 2 Electrical Characteristics N Channel (Ta = 25°C)

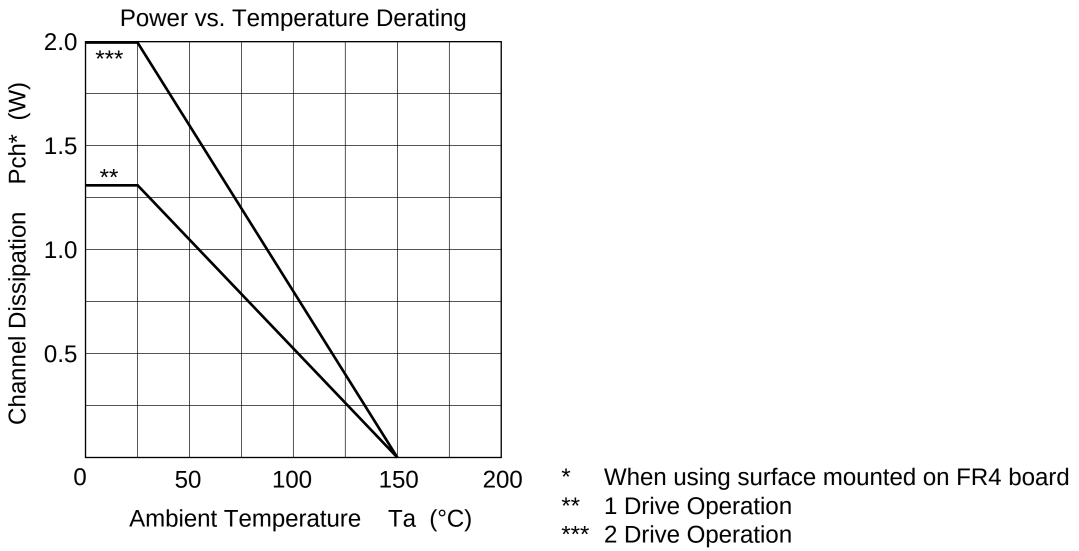
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.08)	0.1	Ω	I_D = 2A V_{GS} = 10V *
		—	(0.11)	0.15	Ω	I_D = 2A V_{GS} = 4V *
Forward transfer admittance	$\|y_{fs}\|$	(2.0)	(3.0)	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	(180)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(110)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(45)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(10)	—	ns	V_{GS} = 4 V, I_D = 2 A
Rise time	t_r	—	(60)	—	ns	V_{DD} = 10 V
Turn–off delay time	$t_{d(off)}$	—	(25)	—	ns	
Fall time	t_f	—	(20)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(0.8)	—	V	I_F = 3.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	I_F = 3.5A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test

Table 2 Electrical Characteristics P Channel (Ta = 25°C)

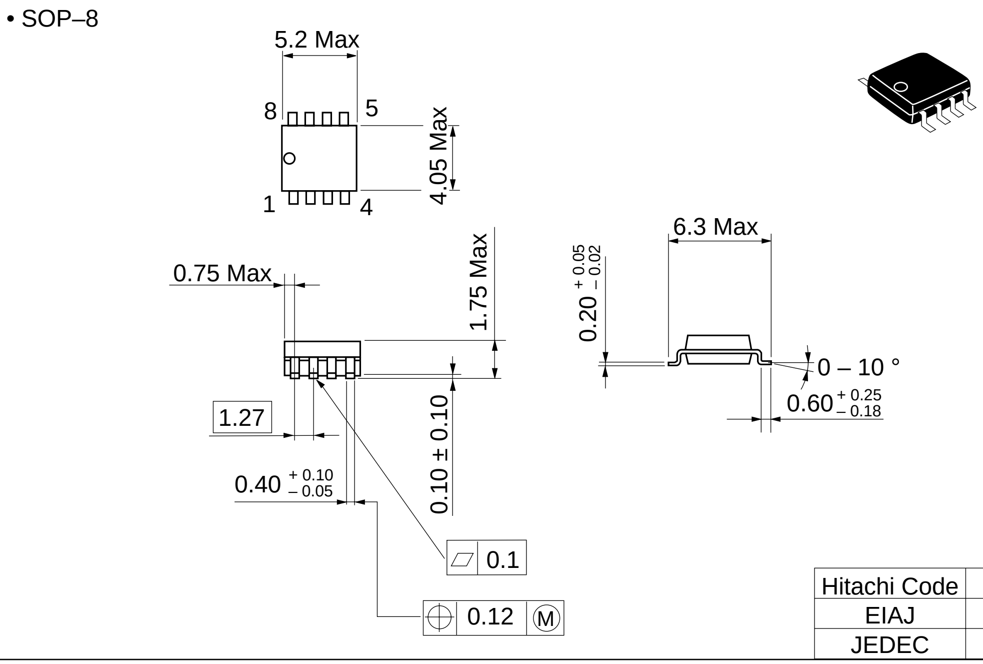
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.13)	0.25	Ω	I_D = –1 A V_{GS} = –10 V *
		—	(0.2)	0.4	Ω	I_D = –1 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	(2.0)	(3.0)	—	S	I_D = –1 A V_{DS} = –10 V *
Input capacitance	Ciss	—	(250)	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	(150)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(60)	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	(10)	—	ns	V_{GS} = –4 V, I_D = –1 A
Rise time	t_r	—	(60)	—	ns	V_{DD} = –10 V
Turn–off delay time	$t_{d(off)}$	—	(20)	—	ns	
Fall time	t_f	—	(25)	—	ns	
Body–drain diode forward voltage	V_{DF}	—	(–0.8)	—	V	I_F = –2.5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	(50)	—	ns	I_F = –2.5A, V_{GS} = 0 diF / dt = 20 A / µs

* Pulse Test



Package Dimensions

Unit : mm



Hitachi Code	FP–8DA
EIAJ	—
JEDEC	MS-012AA

4AJ11

Silicon P Channel Power MOS FET Array

Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)} \leq 0.13\Omega$, $V_{GS} = -10V$, $I_D = -4A$
  $R_{DS(on)} \leq 0.17\Omega$, $V_{GS} = -4V$, $I_D = -4A$
- Capable of 4V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for motor driver and solenoid driver and lamp driver
- Discrete packaged devices of same die
  2SJ173, 2SJ176, 2SJ219 L , 2SJ219 S

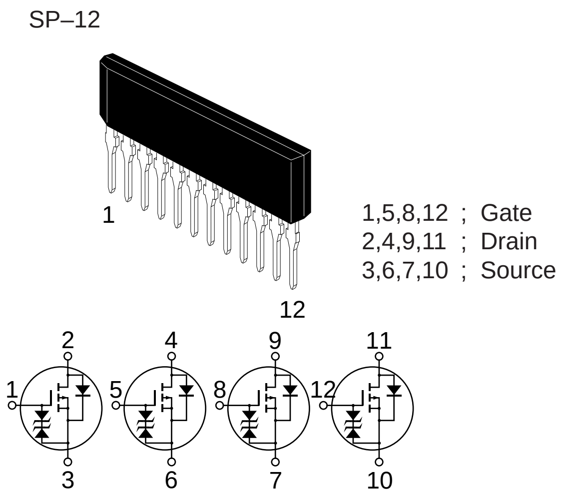


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–8	A
Drain peak current	$I_{D(pulse)}$*	–32	A
Body–drain diode reverse drain current	I_{DR}	–8	A
Channel dissipation	Pch(Tc = 25 °C)**	28	W
Channel dissipation	Pch**	4	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

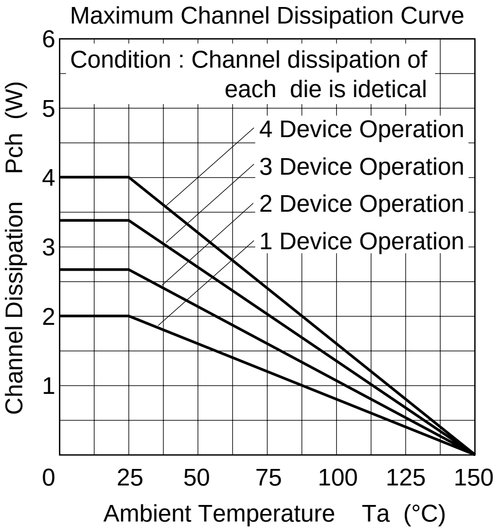
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 Devices operation

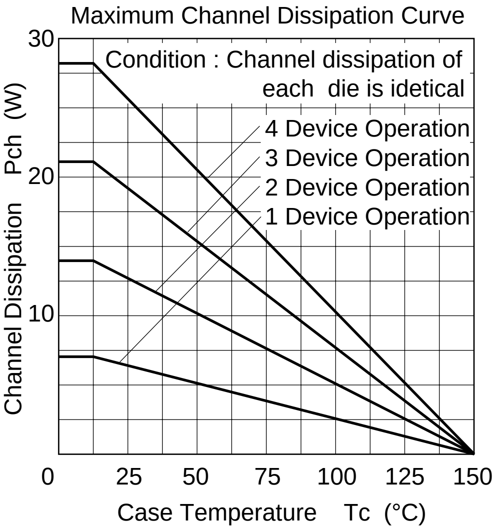
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.09	0.13	Ω	I_D = –4 A V_{GS} = –10 V *
		—	0.12	0.17	Ω	I_D = –4 A V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	5.5	7.7	—	S	I_D = –4 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	720	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	220	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = –8 A
Rise time	t_r	—	120	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	220	—	ns	R_L = 3.75 Ω
Fall time	t_f	—	160	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.05	—	V	I_F = –8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	190	—	µs	I_F = –8 A, V_{GS} = 0, dIF / dt = 50 A / µs

* Pulse Test

■ See characteristic curves of 2SJ173, 2SJ176.


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is idetical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
6
5
4
3
2
1
0
25
50
75
100
125
150
Ambient Temperature Ta (°C)


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is idetical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
30
20
10
0
25
50
75
100
125
150
Case Temperature Tc (°C)

4AK23

Silicon N Channel Power MOS FET Array

Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)} \leq 0.25\Omega$, V_{GS} = 10V, I_D = 2.5A
- Low drive current
- High speed switching
- High density mounting
- Suitable for H–bridged motor driver

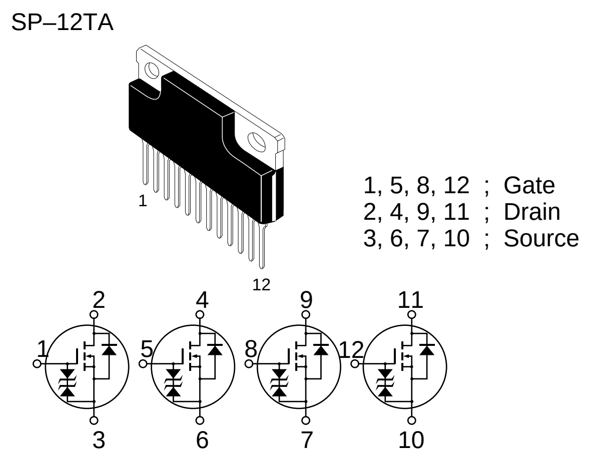


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$*	20	A
Body–drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	Pch(Tc = 25 °C)**	32	W
Channel dissipation	Pch**	4	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

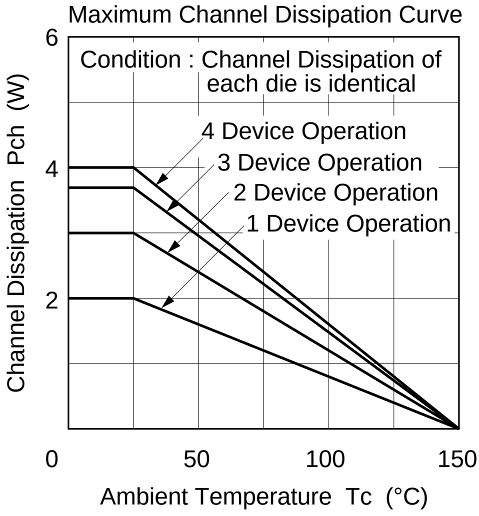
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 Devices operation

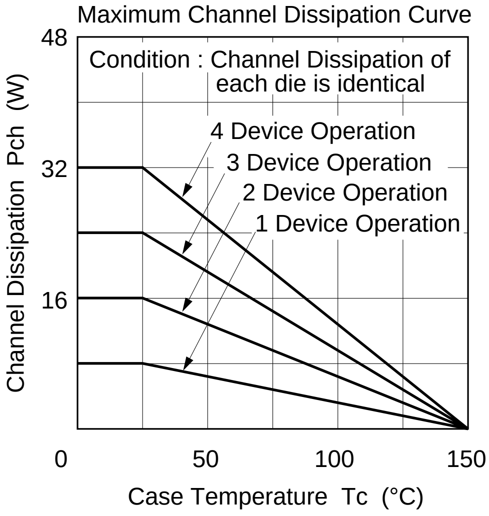
Table 2 Electrical Characteristics (Ta = 25°C)

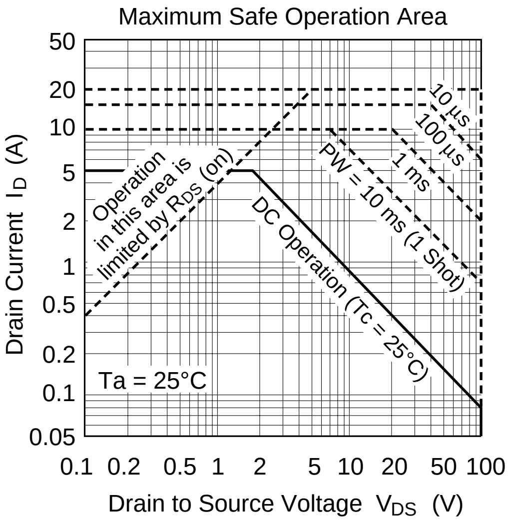
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 80 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.25	Ω	I_D = 2.5A V_{GS} = 10 V *
		—	0.25	0.35	Ω	I_D = 2.5 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	3	5	—	S	I_D = 2.5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	525	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	205	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	60	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 2.5 A
Rise time	t_r	—	30	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	180	—	ns	R_L = 12 Ω
Fall time	t_f	—	65	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	170	—	µs	I_F = 5 A, V_{GS} = 0, dIF / dt = 50 A / µs

* Pulse Test

See characteristeic Curves of 2SK1300


Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
6
4
2
0
50
100
150
Ambient Temperature Tc (°C)


Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
48
32
16
0
50
100
150
Case Temperature Tc (°C)


Maximum Safe Operation Area
Drain Current I D (A)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
Operation in this area is limited by RDS (on)
DC Operation (Tc = 25°C)
Ta = 25°C
0.1 0.2 0.5 1 2 5 10 20 50 100
Drain to Source Voltage VDS (V)

4AK25

Silicon N Channel Power MOS FET Array

Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)} \le 0.45\Omega$, V_{GS} = 10V, I_D = 1A
- Low drive current
- High speed switching
- High density mounting

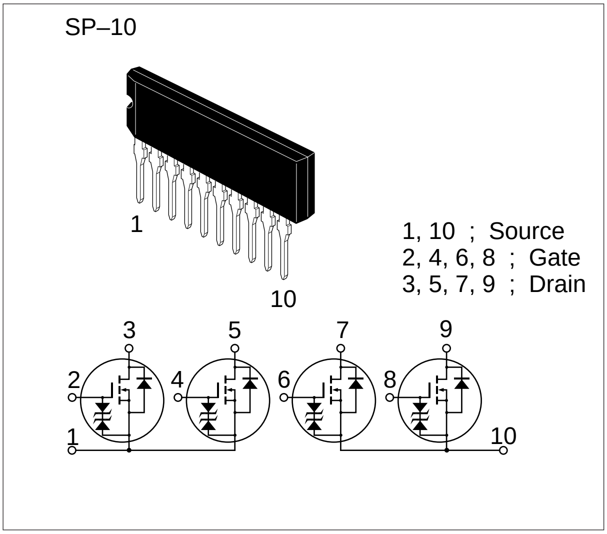


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	1.5	A
Drain peak current	$I_{D(pulse)}$*	4.5	A
Body–drain diode reverse drain current	I_{DR}	1.5	A
Channel dissipation	Pch(Tc = 25 °C)**	2.4	W
Channel dissipation	Pch**	3.6	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

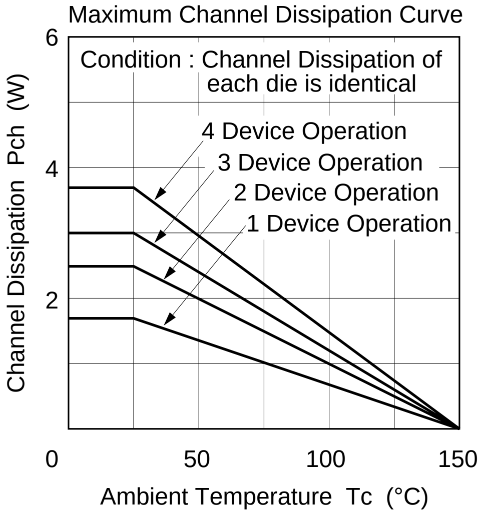
* PW ≤ 10 μs, duty cycle ≤ 1 %
** 4 Devices operation

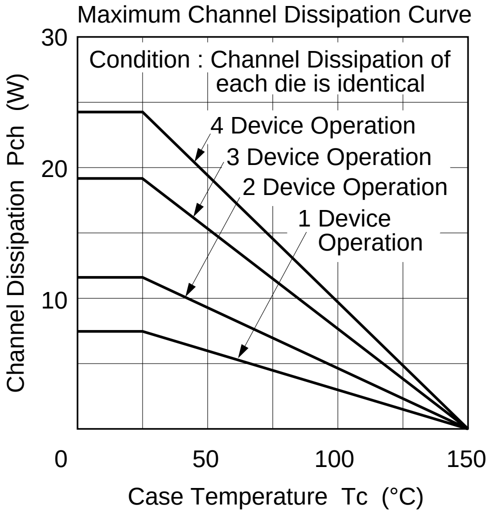
Table 2 Electrical Characteristics (Ta = 25°C)

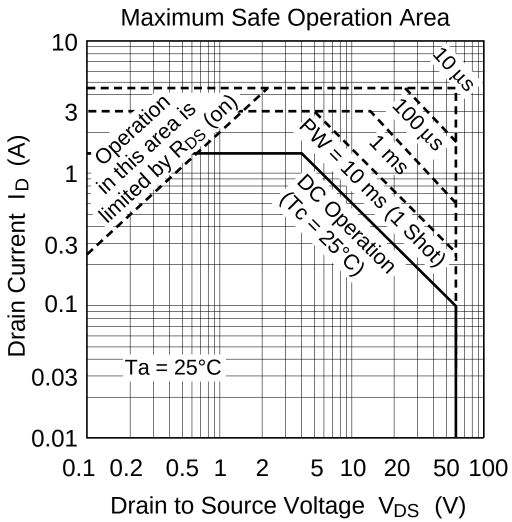
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.35	0.45	Ω	I_D = 1A V_{GS} = 10 V *
		—	0.47	0.65	Ω	I_D = 1 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	0.9	1.5	—	S	I_D = 1 A V_{DS} = 10 V *
Input capacitance	Ciss	—	140	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	70	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	20	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	3	—	ns	I_D = 1 A
Rise time	t_r	—	12	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	50	—	ns	R_L = 30 Ω
Fall time	t_f	—	30	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	V	I_F = 1.5 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	70	—	μs	I_F = 1.5 A, V_{GS} = 0, dIF / dt = 50 A / μs

* Pulse Test

See characteristeic Curves of 2SK975


Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
Ambient Temperature Tc (°C)
0
2
4
6
50
100
150


Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
Case Temperature Tc (°C)
0
10
20
30
50
100
150


Maximum Safe Operation Area
Operation in this area is limited by R_{DS} (on)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation
(Tc = 25°C)
Ta = 25°C
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10
3
1
0.3
0.1
0.03
0.01
0.1
0.2
0.5
1
2
5
10
20
50
100

4AK26

Silicon N Channel Power MOS FET Array

Application

High speed power switching

Features

- Low on–resistance
  $R_{DS(on)} \leq 0.06\Omega$, V_{GS} = 10V, I_D = 5A
  $R_{DS(on)} \leq 0.075\Omega$, V_{GS} = 4V, I_D = 5A
- Capable of 4V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for motor driver and solenoid driver and lamp driver

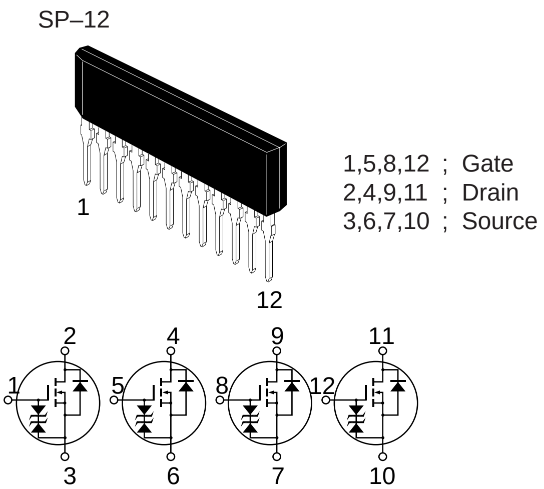


Table 1 Absolute Maximum Ratings (Ta = 25°C)

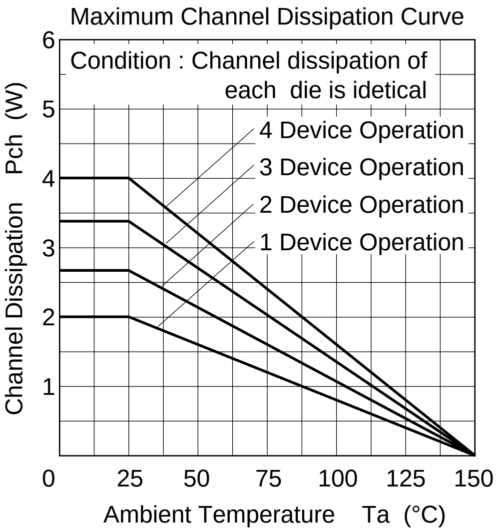
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*	32	A
Body–drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch(Tc = 25 °C)**	28	W
Channel dissipation	Pch**	4	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

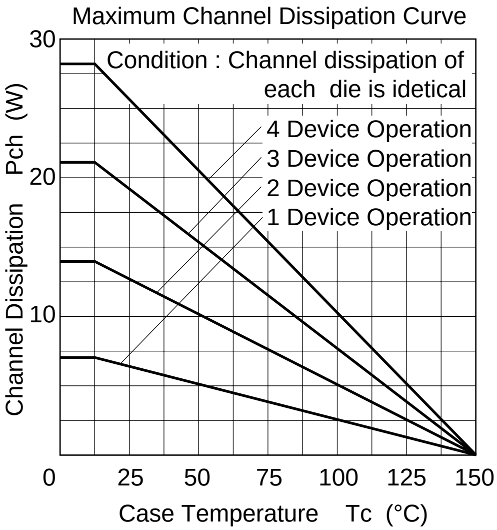
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 Devices operation

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.045	0.06	Ω	I_D = 5A V_{GS} = 10 V *
		—	0.056	0.075	Ω	I_D = 5 A V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	10	12	—	S	I_D = 5 A V_{DS} = 10 V *
Input capacitance	Ciss	—	1400	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	720	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	220	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	I_D = 10 A
Rise time	t_r	—	95	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	300	—	ns	R_L = 3 Ω
Fall time	t_f	—	170	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	110	—	µs	I_F = 10 A, V_{GS} = 0, dIF / dt = 50 A / µs

* Pulse Test


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is idetical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
6
5
4
3
2
1
0
25
50
75
100
125
150
Ambient Temperature Ta (°C)


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is idetical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
30
20
10
0
25
50
75
100
125
150
Case Temperature Tc (°C)

4AM14

Silicon N Channel/P Channel Complementary Power MOS FET Array

Application

High speed power switching

Features

- Low on-resistance
  N-channel: R_{DS} (on) ≤ 0.17 Ω, V_{GS} = 10 V
  I_D = 4 A
  P-channel: R_{DS} (on) ≤ 0.2 Ω, V_{GS} = –10 V
  I_D = –4 A
- Capable of 4 V gate drive
- Low drive current
- Hight speed switching
- High density mounting
- Suitable for H-bridged motor driver
- Discrete packaged devices of same die
  N-channel: 2SK970 (TO-220AB),
  2SK1093 (TO-220FM)
  P-channel: 2SJ172 (TO-220AB),
  2SJ175 (TO-220FM)

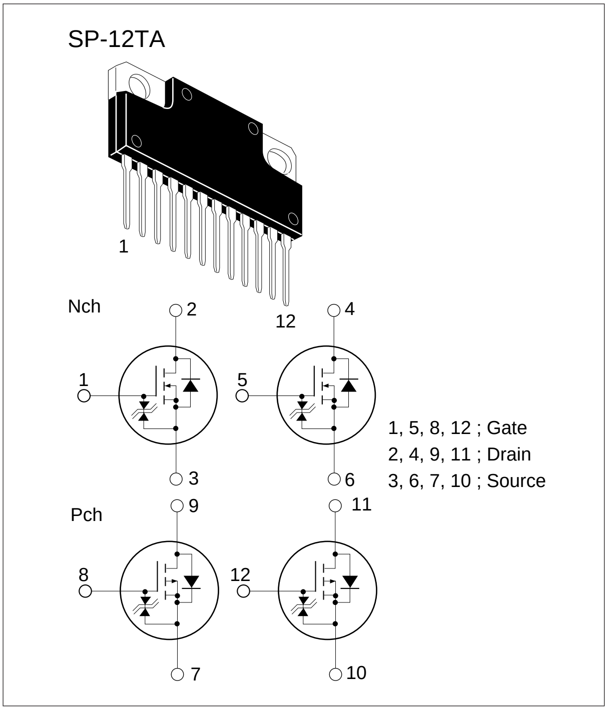


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	8	–8	A
Drain peak current	$I_{D(pulse)}$*	32	–32	A
Body–drain diode reverse drain current	I_{DR}	8	–8	A
Channel dissipation	Pch (Tc =25°C)**	32		W
Channel dissipation	Pch**	4		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 devices operation

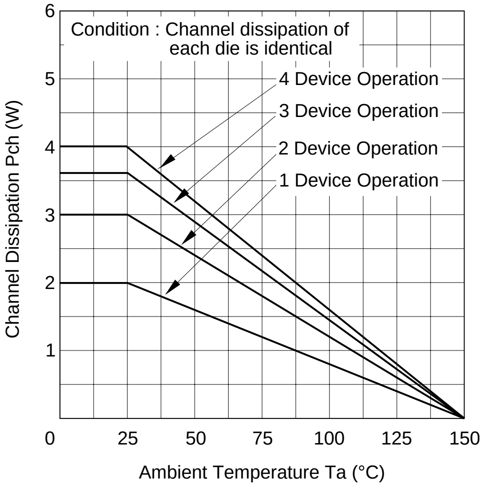
Table 2 Electrical Characteristics (Ta = 25°C) (1 Unit)

Item	Symbol	N channel Min	N channel Typ	N channel Max	P channel Min	P channel Typ	P channel Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17	—	0.15	0.2	Ω	I_D = 4 A, V_{GS} = 10 V *
		—	0.18	0.24		0.20	0.27	Ω	I_D = 4 A, V_{GS} = 4 V *
Forward transfer admittance	|yfs|	3.5	5.5	—	3.5	6.0	—	S	I_D = 4 A *V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	—	900	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	220	—	—	460	—	pF	
Reverse transfer capacitance	Crss	—	60	—	—	130	—	pF	
Turn–on delay time	$td_{(on)}$	—	5	—	—	8	—	ns	I_D = 4 A, V_{GS} = 10 V, R_L = 7.5 Ω
Rise time	tr	—	45	—	—	50	—	ns	
Turn–off delay time	$td_{(off)}$	—	150	—	—	180	—	ns	
Fall time	tf	—	85	—	—	95	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	—	–1.2	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	120	—	—	185	—	ns	I_F = 8 A, V_{GS} = 0, dI_F/dt = 50 A/µs

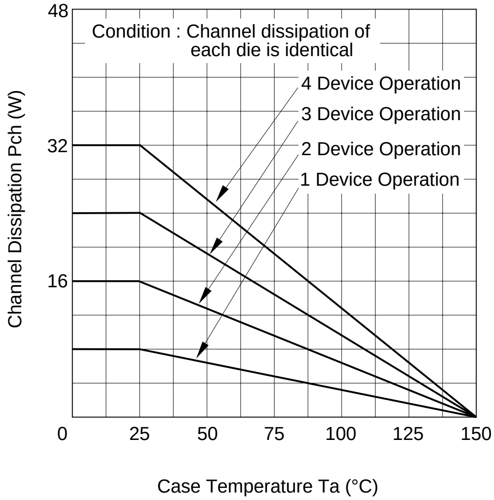
* Pulse Test
Note: Polarity of test conditions for P channel device is reversed.

■ Nch : See characteristeic curves of 2SK970
■ Pch : See characteristeic curves of 2SJ172

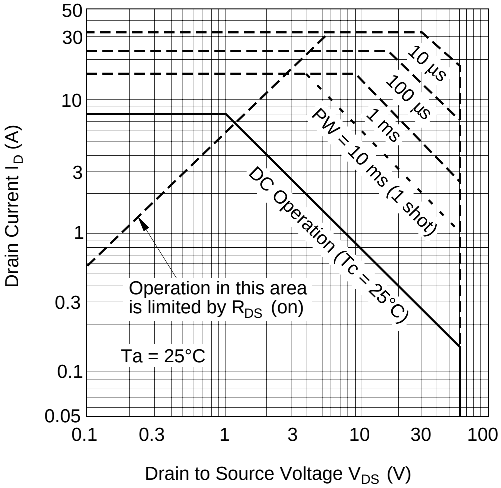
Maximum Channel Dissipation Curve



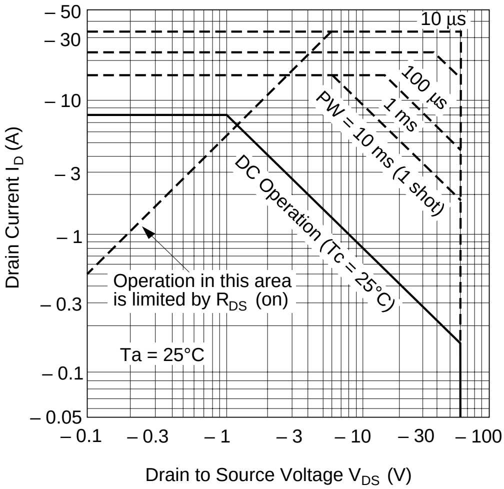
Maximum Channel Dissipation Curve



Maximum Safe Operation Area
(N-channel)



Maximum Safe Operation Area
(P-channel)

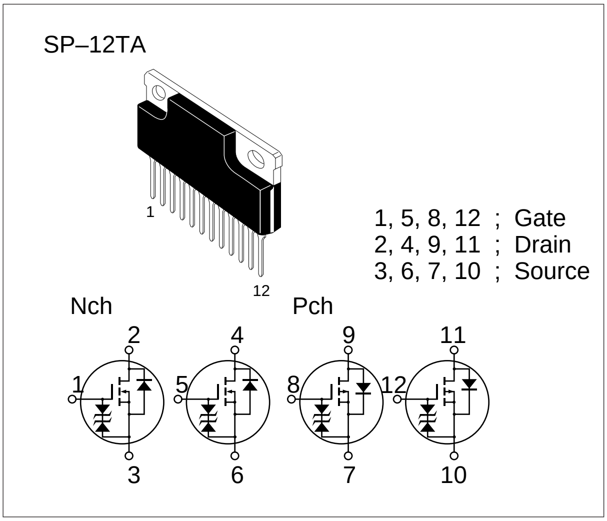


4AM15

Silicon N Channel/P Channel Power MOS FET Array

Application

High speed power switching



Features

- Low on–resistance
  N Channel : $R_{DS(on)} \leq 0.5\Omega$,
  $V_{GS} = 10V$, $I_D = 2A$
  P Channel : $R_{DS(on)} \leq 0.9\Omega$,
  $V_{GS} = -10V$, $I_D = -2A$
- Low drive current
- High speed switching
- High density mounting
- Suitable for H–bridged motor driver

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	200	–200	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	4	–4	A
Drain peak current	$I_{D(pulse)}$*	16	–16	A
Body–drain diode reverse drain current	I_{DR}	4	–4	A
Channel dissipation	Pch** (Tc = 25 °C)	32		W
	Pch**	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 Device Operation

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	N Channel Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.33	0.5	Ω	I_D = 2 A, V_{GS} = 10 V *
Forward transfer admittance	$\|y_{fs}\|$	1.5	2.5	—	S	I_D = 2 A V_{DS} = 10 V *
Input capacitance	Ciss	—	750	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	260	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	40	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	19	—	ns	I_D = 2 A
Rise time	t_r	—	26	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	45	—	ns	R_L = 15 Ω
Fall time	t_f	—	24	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	125	—	ns	I_F =4 A, V_{GS} = 0, diF / dt = 100 A / µs

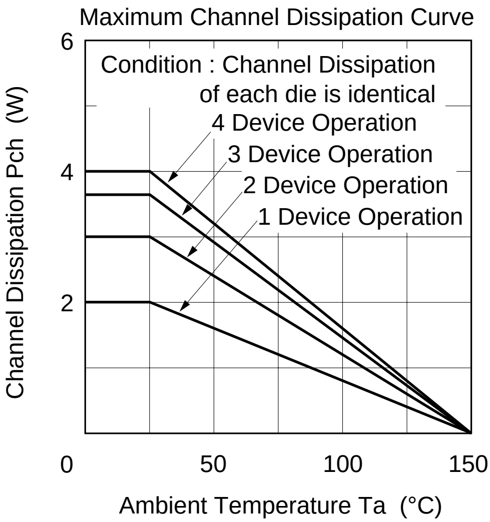
* Pulse Test

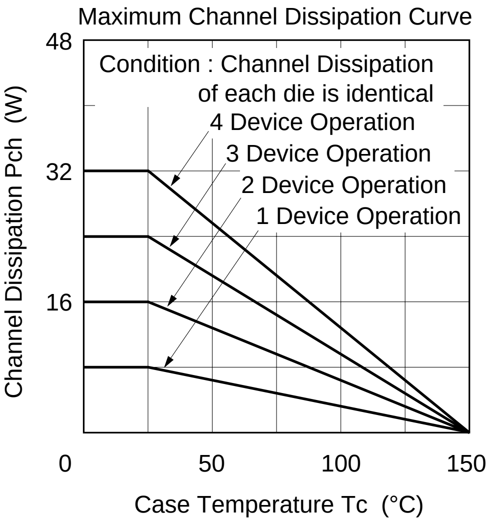
■ See characteristic curve of 2SK1957 and 2SJ410

Table 3 Electrical Characteristics (Ta = 25°C)

Item	Symbol	P Channel Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–200	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–2.0	—	–4.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.9	Ω	I_D = –2 A, V_{GS} = –10 V *
Forward transfer admittance	$\lvert y_{fs} \rvert$	2.0	3.0	—	S	I_D = –2 A V_{DS} = –10 V *
Input capacitance	Ciss	—	920	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	290	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	70	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	17	—	ns	I_D = –2 A
Rise time	t_r	—	40	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	85	—	ns	R_L = 15 Ω
Fall time	t_f	—	45	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –4 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	170	—	ns	I_F =–4 A, V_{GS} = 0, diF / dt = 100 A / µs

* Pulse Test


Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
6
4
2
0
50
100
150
Ambient Temperature Ta (°C)

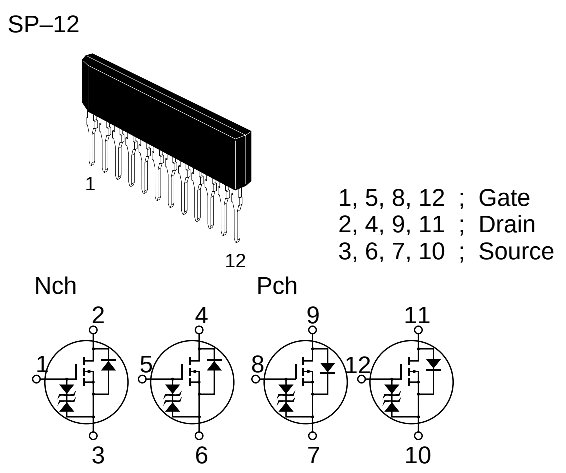

Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
48
32
16
0
50
100
150
Case Temperature Tc (°C)

4AM16

Silicon N Channel/P Channel Power MOS FET Array

Application

High speed power switching



Features

- Low on–resistance
  N Channel : $R_{DS(on)} \leq 0.17\Omega$,
  $V_{GS} = 10V$, $I_D = 4A$
  P Channel : $R_{DS(on)} \leq 0.2\Omega$,
  $V_{GS} = -10V$, $I_D = -4A$
- High speed switching
- High density mounting
- Suitable for H–brided motor driver

Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	-60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	8	-8	A
Drain peak current	$I_{D(pulse)}$*	32	-32	A
Body–drain diode reverse drain current	I_{DR}	8	-8	A
Channel dissipation	Pch** (Tc = 25 °C)	28		W
	Pch**	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 Device Operation

Table 2 Electrical Characteristics (Ta = 25°C)

		N Channel				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state	$R_{DS(on)}$	—	0.13	0.17	Ω	I_D = 4 A, V_{GS} = 10 V *
resistance		—	0.18	0.24		I_D = 4 A, V_{GS} = 4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	5.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	220	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	60	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	5	—	ns	I_D = 4 A
Rise time	t_r	—	45	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	150	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	85	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F =8 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

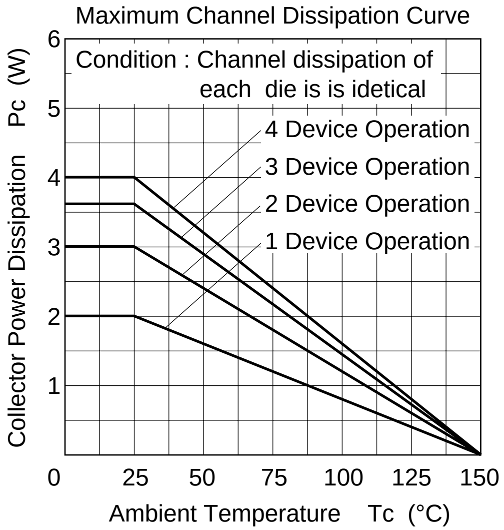
See characteristic curves of 2SK970

Table 3 Electrical Characteristics (Ta = 25°C)

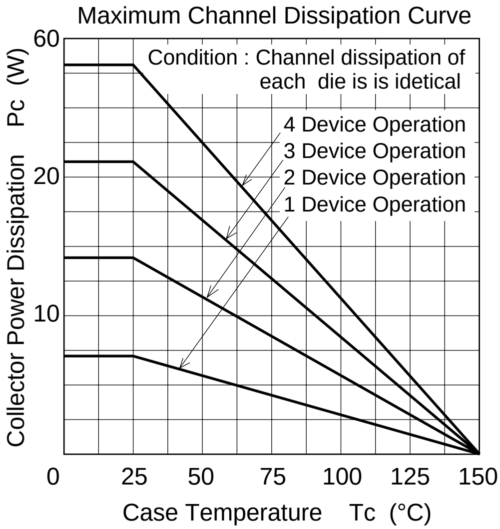
Item	Symbol	P Channel Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state	$R_{DS(on)}$	—	0.15	0.20	Ω	I_D = –4 A, V_{GS} = –10 V *
resistance		—	0.20	0.27		I_D = –4 A, V_{GS} = –4 V *
Forward transfer admittance	$\|y_{fs}\|$	3.5	6.0	—	S	I_D = –4 A V_{DS} = –10 V *
Input capacitance	Ciss	—	900	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	460	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	130	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	8	—	ns	I_D = –4 A
Rise time	t_r	—	50	—	ns	V_{GS} = –10 V
Turn–off delay time	$t_{d(off)}$	—	180	—	ns	R_L = 7.5 Ω
Fall time	t_f	—	95	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.2	—	V	I_F = –8 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	185	—	ns	I_F =–8 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

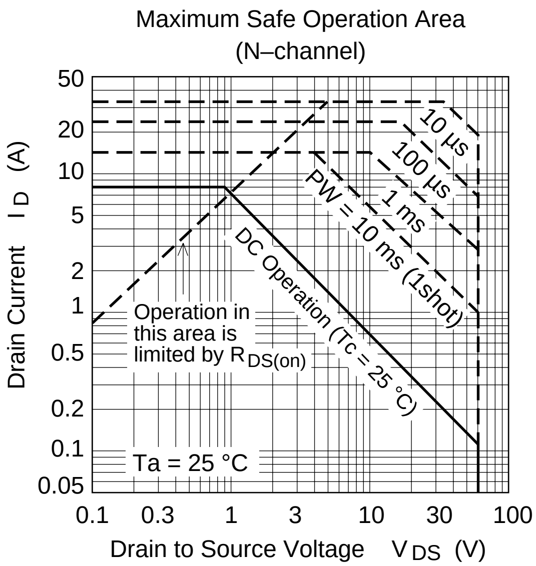
See characteristics curves of 2SJ172



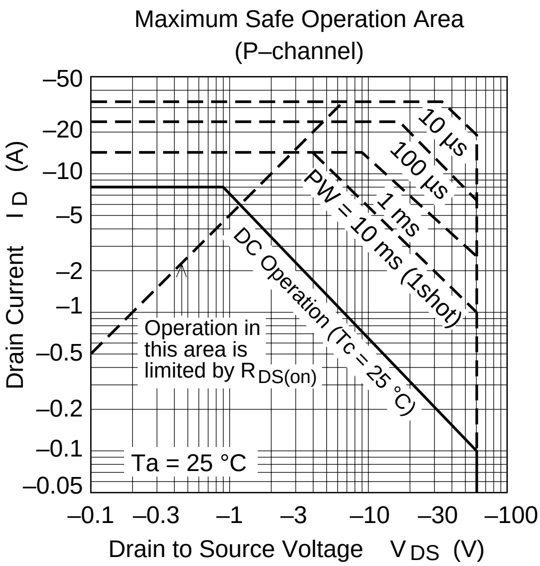
Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is is idetical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Collector Power Dissipation Pc (W)
Ambient Temperature Tc (°C)
0
1
2
3
4
5
6
25
50
75
100
125
150



Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is is idetical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Collector Power Dissipation Pc (W)
Case Temperature Tc (°C)
0
10
20
60
25
50
75
100
125
150



Maximum Safe Operation Area
(N–channel)
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
Drain Current I D (A)
Drain to Source Voltage V DS (V)
50
20
10
5
2
1
0.5
0.2
0.1
0.05
0.1
0.3
1
3
10
30
100



Maximum Safe Operation Area
(P–channel)
10 μs
100 μs
1 ms
PW = 10 ms (1shot)
DC Operation (Tc = 25 °C)
Operation in this area is limited by R DS(on)
Ta = 25 °C
Drain Current I D (A)
Drain to Source Voltage V DS (V)
–50
–20
–10
–5
–2
–1
–0.5
–0.2
–0.1
–0.05
–0.1
–0.3
–1
–3
–10
–30
–100

6AM12

Silicon N Channel/P Channel Complementary Power MOS FET Array

Application

High speed power switching

Features

- Low on-resistance
  N-channel: R_{DS} (on) ≤ 0.17 Ω, V_{GS} = 10 V
  I_D = 4 A
  P-channel: R_{DS} (on) ≤ 0.2 Ω, V_{GS} = –10 V
  I_D = –4 A
- Capable of 4 V gate drive
- Low drive current
- Hight speed switching
- High density mounting
- Suitable for H-bridged motor driver
- Discrete packaged devices of same die
  N-channel: 2SK970 (TO-220AB),
  2SK1093 (TO-220FM)
  P-channel: 2SJ172 (TO-220AB),
  2SJ175 (TO-220FM)

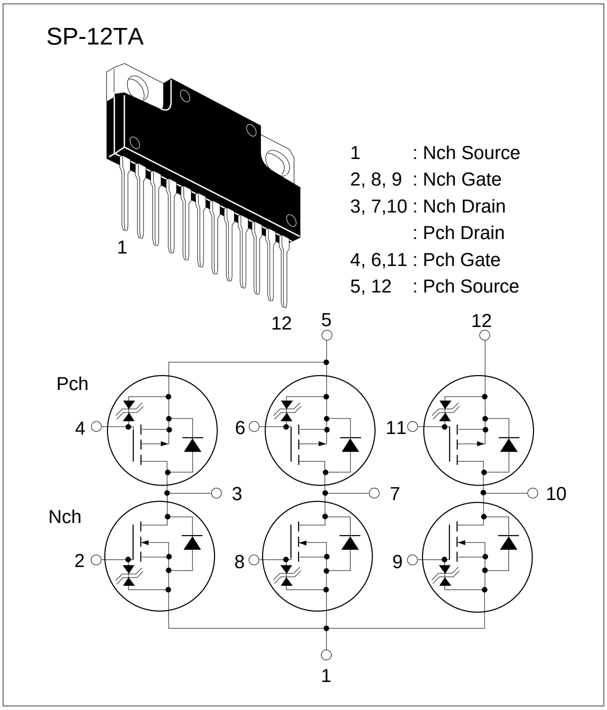


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	7	–7	A
Drain peak current	$I_{D(pulse)}$*	28	–28	A
Body–drain diode reverse drain current	I_{DR}	7	–7	A
Channel dissipation	Pch (Tc =25°C)**	42		W
Channel dissipation	Pch**	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

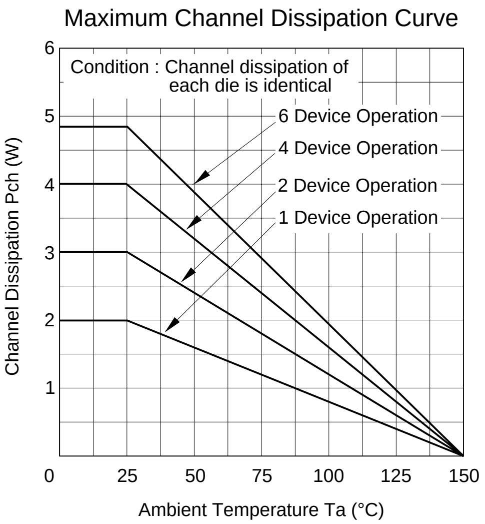
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 6 devices operation

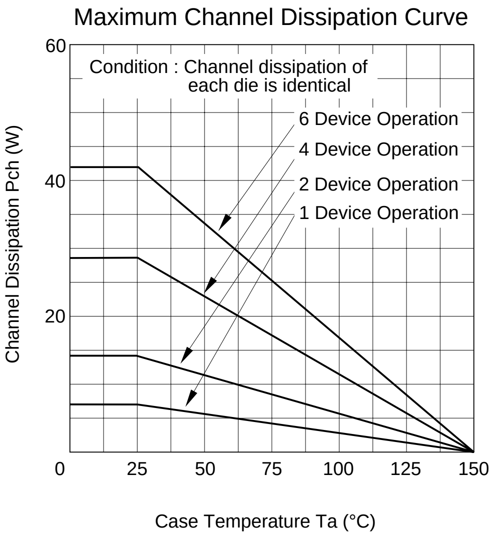
Table 2 Electrical Characteristics (Ta = 25°C) (1 Unit)

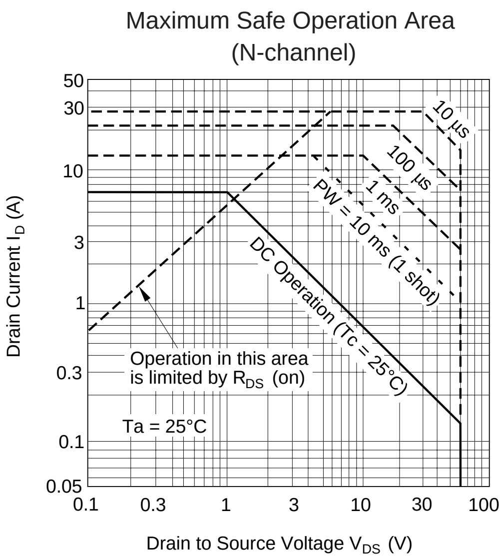
Item	Symbol	N channel Min	N channel Typ	N channel Max	P channel Min	P channel Typ	P channel Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17	—	0.15	0.2	Ω	I_D = 4 A, V_{GS} = 10 V *
		—	0.19	0.24	—	0.20	0.27	Ω	I_D = 4 A, V_{GS} = 4 V *
Forward transfer admittance	|yfs|	3.5	5.5	—	3.5	6.0	—	S	I_D = 4 A *V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	—	900	—	pF	V_{DS} = 10 V, V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	220	—	—	460	—	pF	
Reverse transfer capacitance	Crss	—	60	—	—	130	—	pF	
Turn–on delay time	$t_{d(on)}$	—	5	—	—	8	—	ns	I_D = 4 A, V_{GS} = 10 V, R_L = 7.5 Ω
Rise time	tr	—	45	—	—	50	—	ns	
Turn–off delay time	$t_{d(off)}$	—	150	—	—	170	—	ns	
Fall time	tf	—	80	—	—	95	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.1	—	—	–1.05	—	V	I_F = 7 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	110	—	—	180	—	ns	I_F = 7 A, V_{GS} = 0, dI_F/dt = 50 A/µs

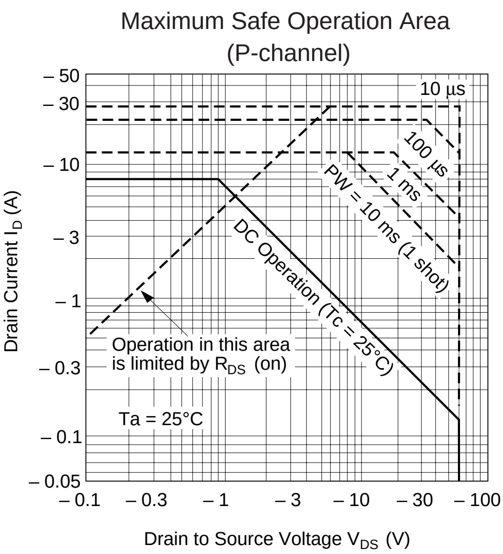
Note: Polarity of test conditions for P channel device is reversed.
* Pulse Test

■ Nch : See characteristic curves of 2SK970
■ Pch : See characteristic curves of 2SJ172


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is identical
6 Device Operation
4 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
Ambient Temperature Ta (°C)


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is identical
6 Device Operation
4 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
Case Temperature Ta (°C)


Maximum Safe Operation Area
(N-channel)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by RDS (on)
Ta = 25°C
Drain Current ID (A)
Drain to Source Voltage VDS (V)


Maximum Safe Operation Area
(P-channel)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by RDS (on)
Ta = 25°C
Drain Current ID (A)
Drain to Source Voltage VDS (V)

6AM13

Silicon N Channel/P Channel Complementary Power MOS FET Array

Application

High speed power switching

Features

- Low on-resistance
  N-channel: R_{DS} (on) ≤ 0.075 Ω, V_{GS} = 10 V
  I_D = 5 A
  P-channel: R_{DS} (on) ≤ 0.12 Ω, V_{GS} = –10 V
  I_D = –5 A
- Capable of 4 V gate drive
- Low drive current
- Hight speed switching
- High density mounting
- Suitable for H-bridged motor driver
- Discrete packaged devices of same die
  N-channel: 2SK971 (TO-220AB),
  2SK1094 (TO-220FM)
  P-channel: 2SJ173 (TO-220AB),
  2SJ176 (TO-220FM)

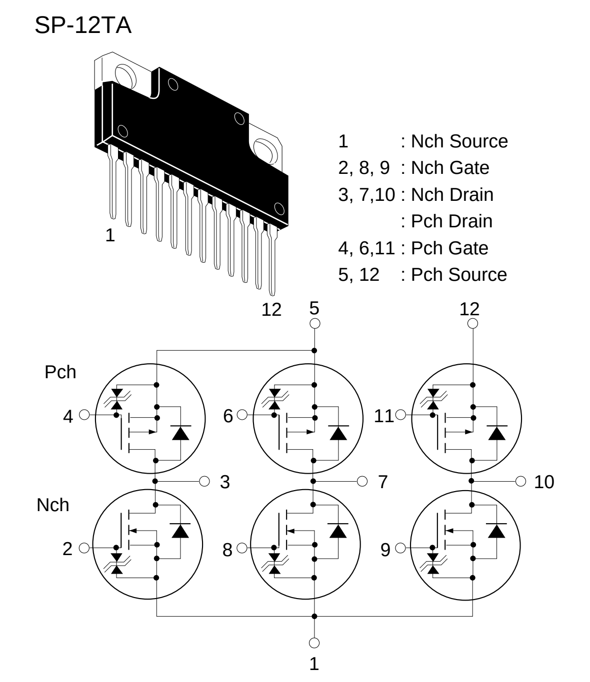


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	10	–10	A
Drain peak current	$I_{D(pulse)}$*	40	–40	A
Body–drain diode reverse drain current	I_{DR}	10	–10	A
Channel dissipation	Pch (Tc =25°C)**	42		W
Channel dissipation	Pch**	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

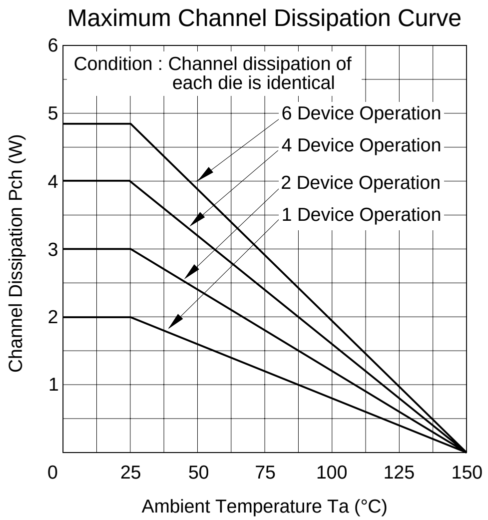
* PW ≤ 10 µs, duty cycle ≤ 1 %
** 6 devices operation

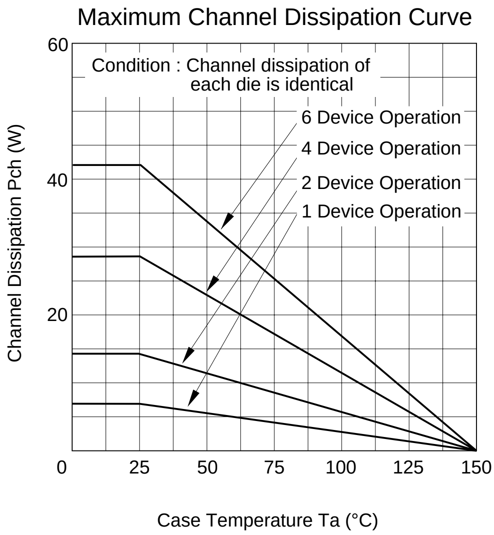
Table 2 Electrical Characteristics (Ta = 25°C) (1 Unit)

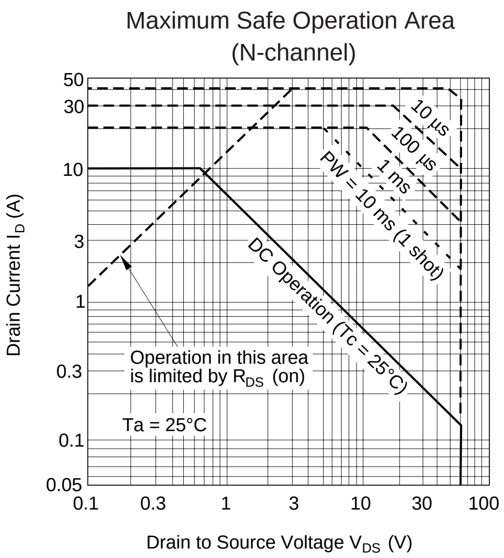
Item	Symbol	N channel Min	N channel Typ	N channel Max	P channel Min	P channel Typ	P channel Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.075	—	0.09	0.12	Ω	I_D = 5 A, V_{GS} = 10 V *
		—	0.08	0.11	—	0.12	0.18	Ω	I_D = 5 A, V_{GS} = 4 V *
Forward transfer admittance	|yfs|	6	9.5	—	5	8	—	S	I_D = 5 A, V_{DS} = 10 V *
Input capacitance	Ciss	—	860	—	—	1400	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	450	—	—	720	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Reverse transfer capacitance	Crss	—	140	—	—	220	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Turn–on delay time	$td_{(on)}$	—	10	—	—	15	—	ns	I_D = 5 A, V_{GS} = 10 V, R_L = 6 Ω
Rise time	tr	—	50	—	—	100	—	ns	I_D = 5 A, V_{GS} = 10 V, R_L = 6 Ω
Turn–off delay time	$td_{(off)}$	—	180	—	—	250	—	ns	I_D = 5 A, V_{GS} = 10 V, R_L = 6 Ω
Fall time	tf	—	110	—	—	160	—	ns	I_D = 5 A, V_{GS} = 10 V, R_L = 6 Ω
Body–drain diode forward voltage	V_{DF}	—	1.0	—	—	–1.0	—	V	I_F = 10 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	120	—	—	200	—	ns	I_F = 10 A, V_{GS} = 0, di_F/dt = 50 A/µs

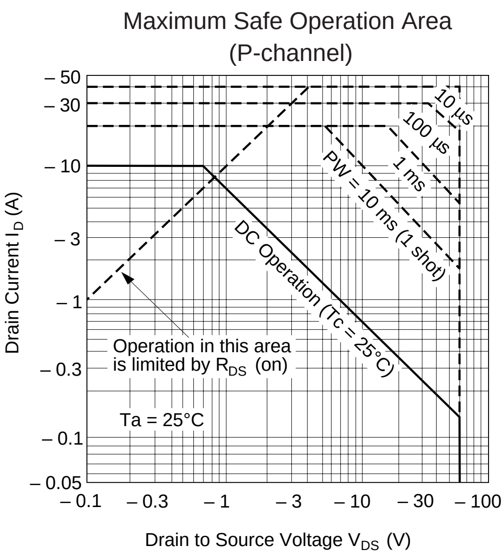
* Pulse Test
Note: Polarity of test conditions for P channel device is reversed.

■ Nch : See characteristic curves of 2SK971
■ Pch : See characteristic curves of 2SJ173


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is identical
6 Device Operation
4 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
Ambient Temperature Ta (°C)


Maximum Channel Dissipation Curve
Condition : Channel dissipation of each die is identical
6 Device Operation
4 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
Case Temperature Ta (°C)


Maximum Safe Operation Area
(N-channel)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_DS (on)
Ta = 25°C
Drain Current I_D (A)
Drain to Source Voltage V_DS (V)


Maximum Safe Operation Area
(P-channel)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (Tc = 25°C)
Operation in this area is limited by R_DS (on)
Ta = 25°C
Drain Current I_D (A)
Drain to Source Voltage V_DS (V)

6AM14

Silicon N Channel / P Channel Power MOS FET Array

HITACHI

1st. Edition
Jun. 1995

Application

Hgh speed power switching

Features

- Low on–resistance
- Low drive current
- High speed switching
- High density mounting

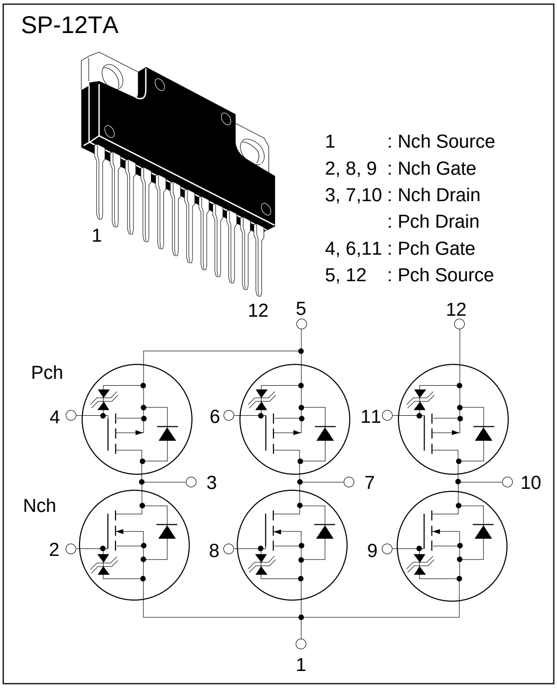


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	7	–7	A
Drain peak current	$I_{D(pulse)}$*	28	–28	A
Reverse drain current	I_{DR}	7	–7	A
Channel dissipation	Pch**	42		W
Channel dissipation	Pch**	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at 6 Drive operation

Table 2 Electrical Characteristics N Channel (Ta = 25°C)

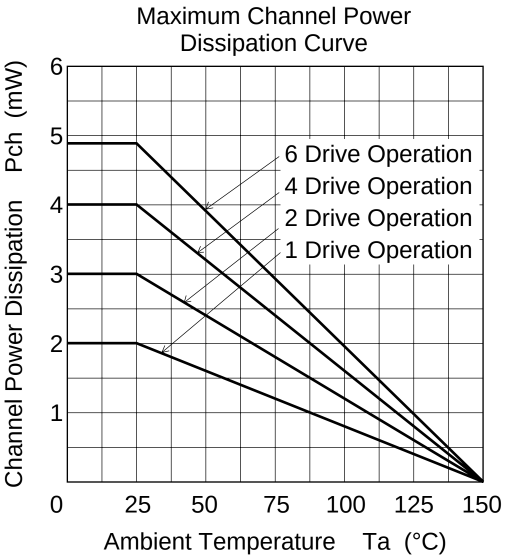
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.14	0.2	Ω	I_D = 4A V_{GS} = 4V *
		—	0.22	0.5	Ω	I_D = 2A V_{GS} = 2.5V *
Forward transfer admittance	$\|y_{fs}\|$	4.0	6.5	—	S	I_D = 4 A V_{DS} = 10 V *
Input capacitance	Ciss	—	500	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	240	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	30	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 10 V, I_D = 4 A
Rise time	t_r	—	90	—	ns	R_L = 7.5 Ω
Turn–off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	t_f	—	250	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 7A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	170	—	ns	I_F = 7A, V_{GS} = 0 diF / dt = 50 A / µs

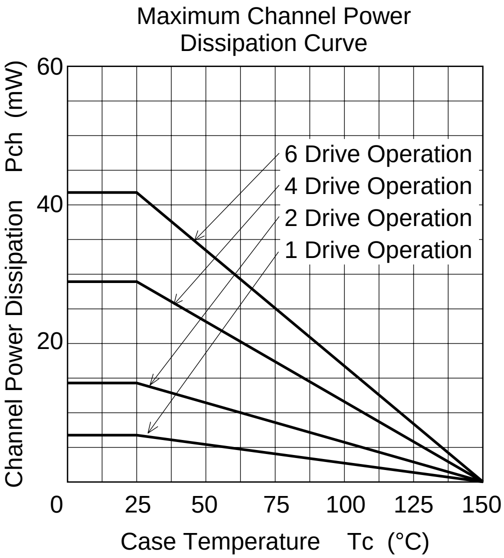
* Pulse Test

Table 2 Electrical Characteristics P Channel (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	I_D = –4 A V_{GS} = –4 V *
		—	0.16	0.3	Ω	I_D = –2 A V_{GS} = –2.5 V *
Forward transfer admittance	$\|y_{fs}\|$	5.0	8.0	—	S	I_D = –4 A V_{DS} = –10 V *
Input capacitance	Ciss	—	1450	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	590	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	120	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = –10 V, I_D = –4 A
Rise time	t_r	—	75	—	ns	R_L = 7.5 Ω
Turn–off delay time	$t_{d(off)}$	—	240	—	ns	
Fall time	t_f	—	180	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –7 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	210	—	ns	I_F = –7 A, V_{GS} = 0 diF / dt = 50A / µs

* Pulse Test


Maximum Channel Power
Dissipation Curve
Channel Power Dissipation Pch (mW)
6
5
4
3
2
1
0
25
50
75
100
125
150
6 Drive Operation
4 Drive Operation
2 Drive Operation
1 Drive Operation
Ambient Temperature Ta (°C)


Maximum Channel Power
Dissipation Curve
Channel Power Dissipation Pch (mW)
60
40
20
0
25
50
75
100
125
150
6 Drive Operation
4 Drive Operation
2 Drive Operation
1 Drive Operation
Case Temperature Tc (°C)

THERMAL FET HAF2001

Silicon N Channel MOS FET Series

HITACHI

1st. Edition
Jun 1995

Application

Power switching
Over temperature shut–down capability

Features

This FET has the over temperature shut–down capability sensing to the junction temperature. This FET has the built–in over temperature shut–down circuit in the gate area. And this ciruit operation to shut–down the gate voltage in case of high junction temperature like applying over power consumption, over curretn etc.

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built–in the over temperature shut–down circuit
- Latch type shut–down operation (Need 0 voltage recovery)

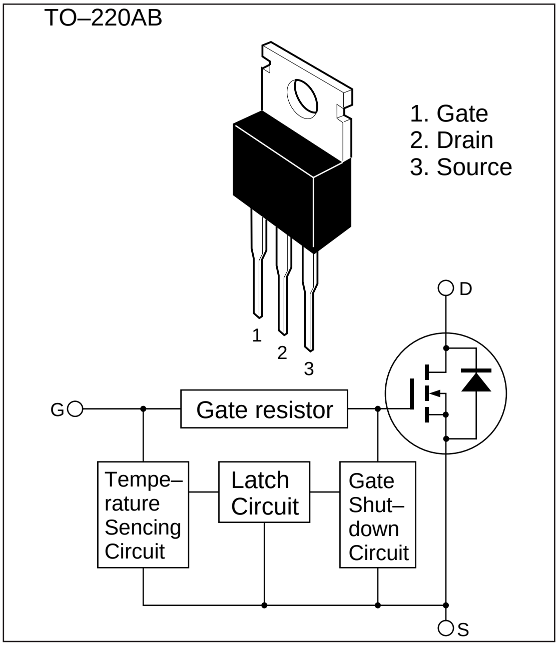


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS+}	16	V
Gate to source voltage	V_{GSS-}	–2.8	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$*	40	A
Body–drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch**	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10µs, duty cycle < 1 %
** Value at Tc = 25°C

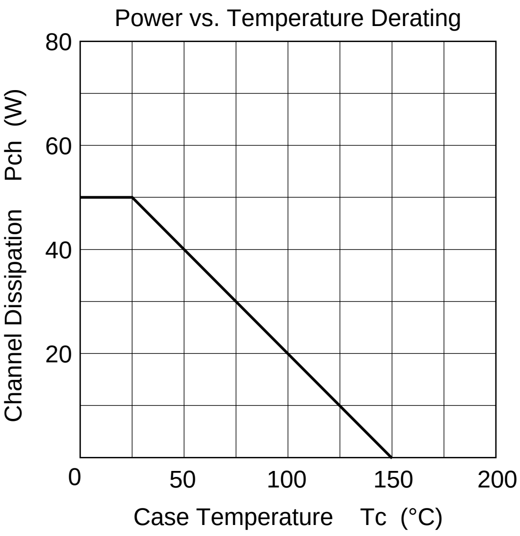
Table 2 Typical Operation Characteristics

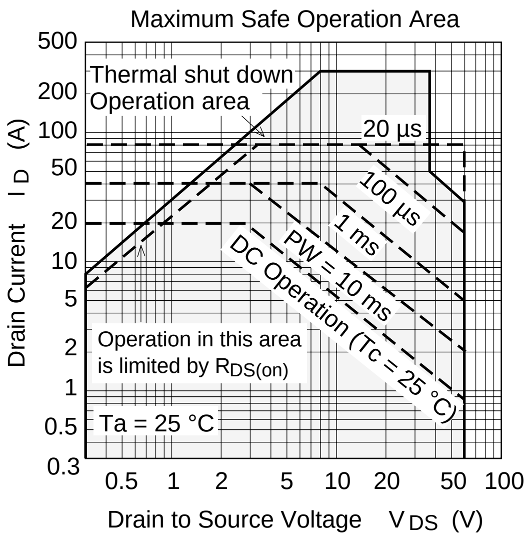
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH}	—	—	100	µA	V_i = 8 V, V_{DS} = 0
	I_{IL}	—	—	50	µA	V_i = 3.5 V, V_{DS} = 0
	I_I	—	—	1	µA	V_i = 1.2 V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH(sd)1}$	—	0.3	—	mA	V_i = 8 V, V_{DS} = 0
	$I_{IH(sd)2}$	—	0.1	—	mA	V_i = 3.5 V, V_{DS} = 0
Shut down temperature	T_{sd}	—	175	—	°C	Channel temperature

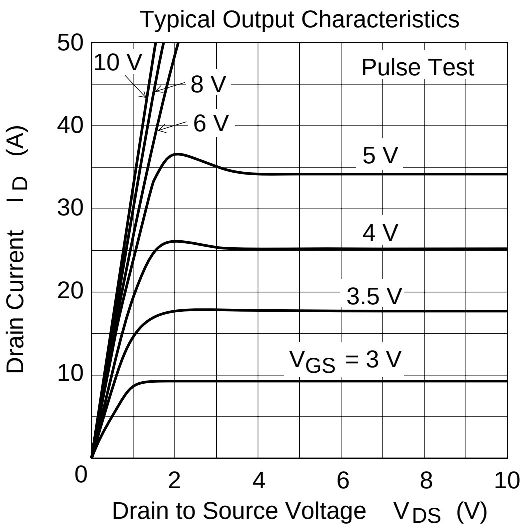
Table 3 Electrical Characteristics (Ta = 25°C)

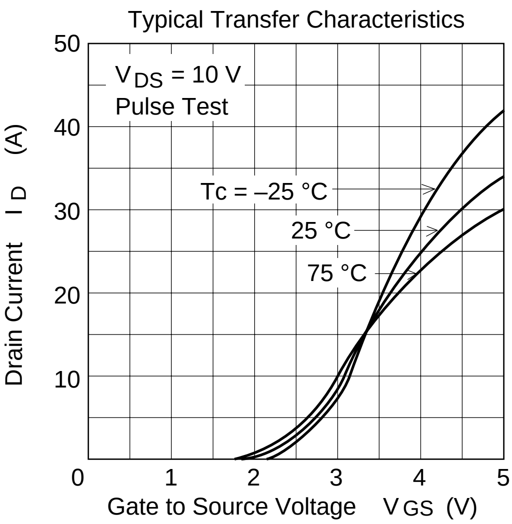
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain current	I_{D1}	10	—	—	A	V_{GS} = 3.5 V, V_{DS} = 10 V
Drain current	I_{D2}	—	—	10	mA	V_{GS} = 1.2 V, V_{DS} = 10 V
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS+}$	16	—	—	V	I_G = 300 µA, V_{DS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS-}$	–2.8	—	—	V	I_G = –100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS+1}	—	—	100	µA	V_{GS} = 8 V, V_{DS} = 0
	I_{GSS+2}	—	—	50	µA	V_{GS} = 3.5 V, V_{DS} = 0
	I_{GSS+3}	—	—	1	µA	V_{GS} = 1.2 V, V_{DS} = 0
	I_{GSS-}	—	—	–100	µA	V_{GS} = –2.4 V, V_{DS} = 0
Input current (shut down)	$I_{GS(op)1}$	—	0.3	—	mA	V_{GS} = 8 V, V_{DS} = 0
	$I_{GS(op)2}$	—	0.1	—	mA	V_{GS} = 3.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cut off voltage	$V_{GS(off)}$	1.2	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	50	65	mΩ	I_D = 10 A , V_{GS} = 4 V
	$R_{DS(on)}$	—	30	43	mΩ	I_D = 10 A , V_{GS} = 10 V
Forward transfer admittance	$\|y_{fs}\|$	6	12	—	S	I_D = 10 A V_{DS} = 10 V
Output capacitance	Coss	—	630	—	pF	V_{DS} = 10 V , V_{GS} = 0 f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	7.5	—	µs	I_D = 5 A
Rise time	t_r	—	29	—	µs	V_{GS} = 5 V
Turn–off delay time	$t_{d(off)}$	—	34	—	µs	R_L = 6 Ω
Fall time	t_f	—	26	—	µs	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 20 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	110	—	ns	I_F = 20 A, V_{GS} = 0, diF / dt = 50 A / µs
Over load shut down operation time (Note 1)	t_{os1}	—	1.8	—	ms	V_{GS} = 5 V, V_{DD} = 12 V
	t_{os2}	—	0.7	—	ms	V_{GS} = 5 V, V_{DD} = 24 V

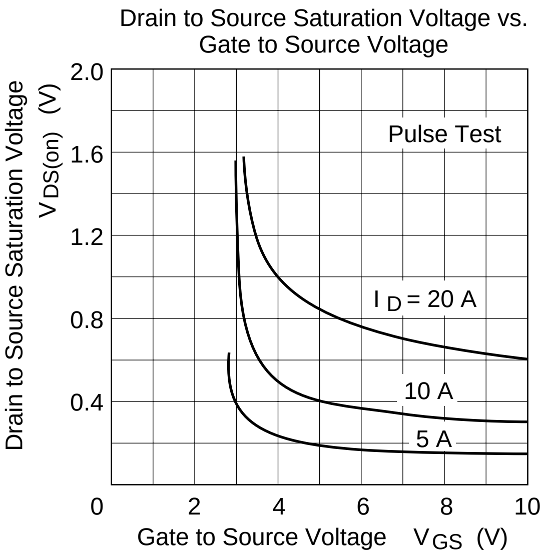
(Note 1) Including the junction temperature taise of the over loaded condition.

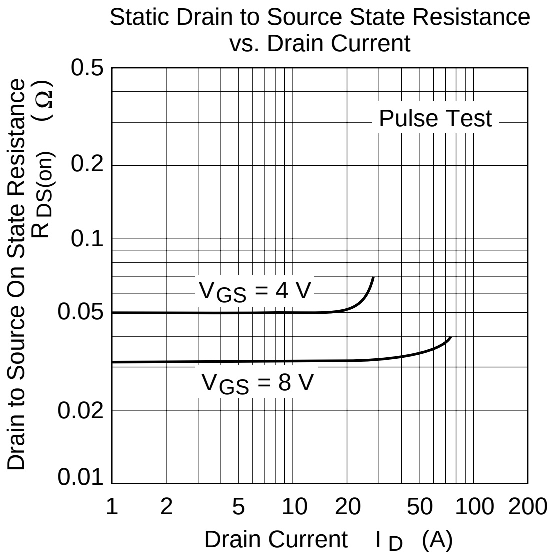

Power vs. Temperature Derating
Channel Dissipation Pch (W)
80
60
40
20
0
50
100
150
200
Case Temperature Tc (°C)

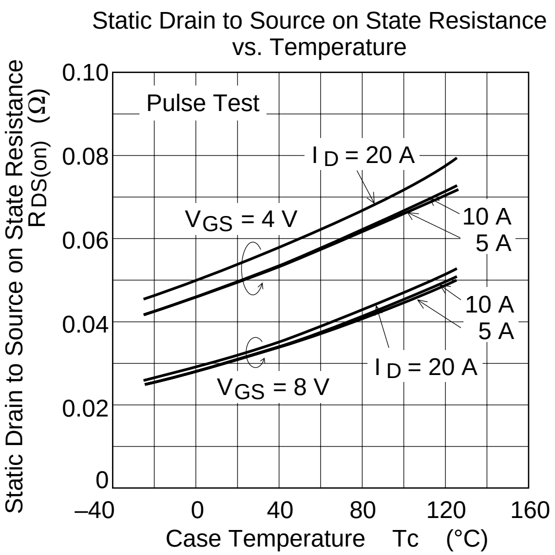

Maximum Safe Operation Area
Thermal shut down
Operation area
20 µs
100 µs
1 ms
PW = 10 ms
DC Operation (Tc = 25 °C)
Operation in this area
is limited by RDS(on)
Ta = 25 °C
Drain Current I D (A)
500
200
100
50
20
10
5
2
1
0.5
0.3
0.5
1
2
5
10
20
50
100
Drain to Source Voltage V DS (V)

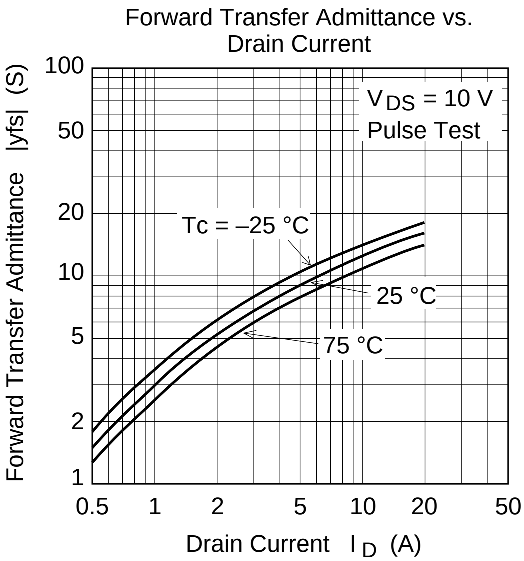

Typical Output Characteristics
Pulse Test
10 V
8 V
6 V
5 V
4 V
3.5 V
VGS = 3 V
Drain Current I D (A)
50
40
30
20
10
0
2
4
6
8
10
Drain to Source Voltage VDS (V)

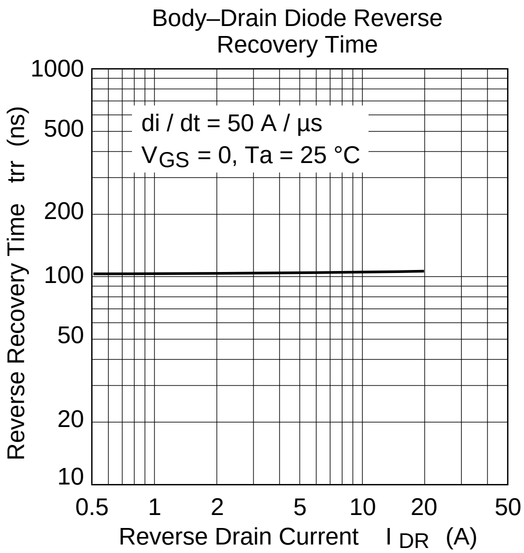

Typical Transfer Characteristics
VDS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
Drain Current I D (A)
50
40
30
20
10
0
1
2
3
4
5
Gate to Source Voltage VGS (V)

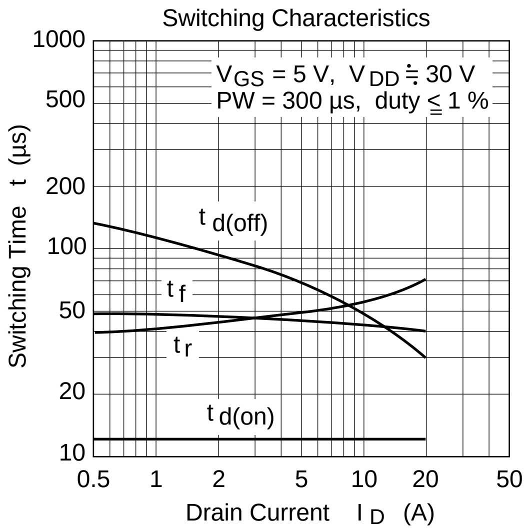

Drain to Source Saturation Voltage vs.
Gate to Source Voltage
Drain to Source Saturation Voltage V DS(on) (V)
Pulse Test
I D = 20 A
10 A
5 A
2.0
1.6
1.2
0.8
0.4
0
2
4
6
8
10
Gate to Source Voltage V GS (V)

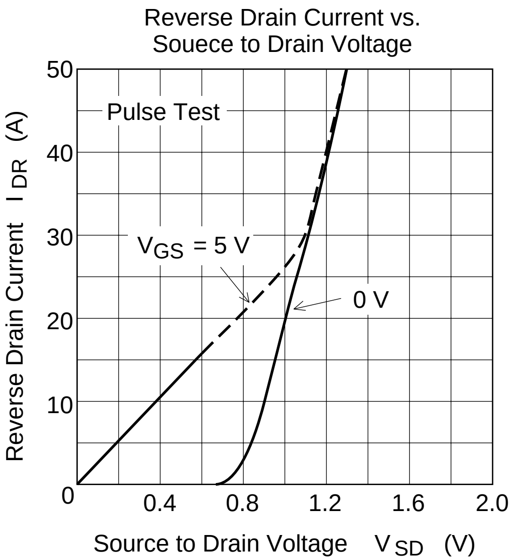

Static Drain to Source State Resistance
vs. Drain Current
Drain to Source On State Resistance R DS(on) (Ω)
Pulse Test
V GS = 4 V
V GS = 8 V
0.5
0.2
0.1
0.05
0.02
0.01
1
2
5
10
20
50
100
200
Drain Current I D (A)

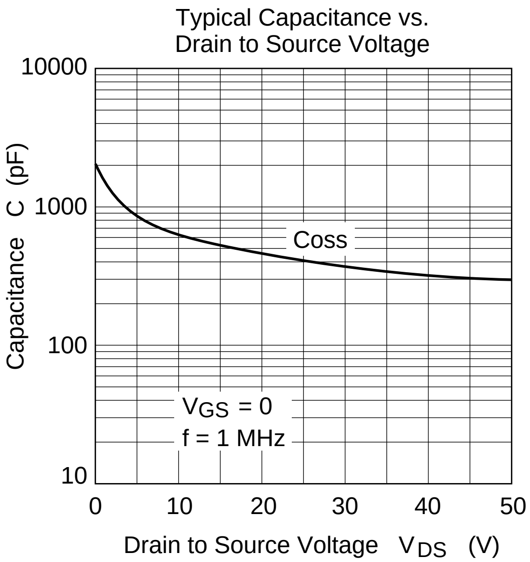

Static Drain to Source on State Resistance
vs. Temperature
Static Drain to Source on State Resistance R DS(on) (Ω)
Pulse Test
I D = 20 A
V GS = 4 V
10 A
5 A
10 A
5 A
I D = 20 A
V GS = 8 V
0.10
0.08
0.06
0.04
0.02
0
–40
0
40
80
120
160
Case Temperature Tc (°C)

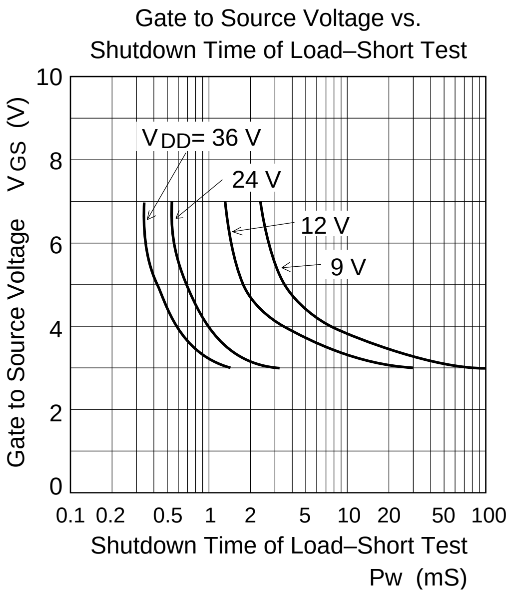

Forward Transfer Admittance vs.
Drain Current
Forward Transfer Admittance |yfs| (S)
V DS = 10 V
Pulse Test
Tc = –25 °C
25 °C
75 °C
100
50
20
10
5
2
1
0.5
1
2
5
10
20
50
Drain Current I D (A)

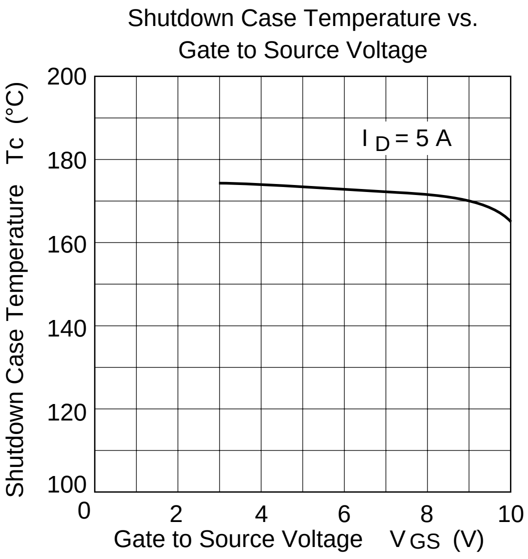

Body–Drain Diode Reverse
Recovery Time
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50

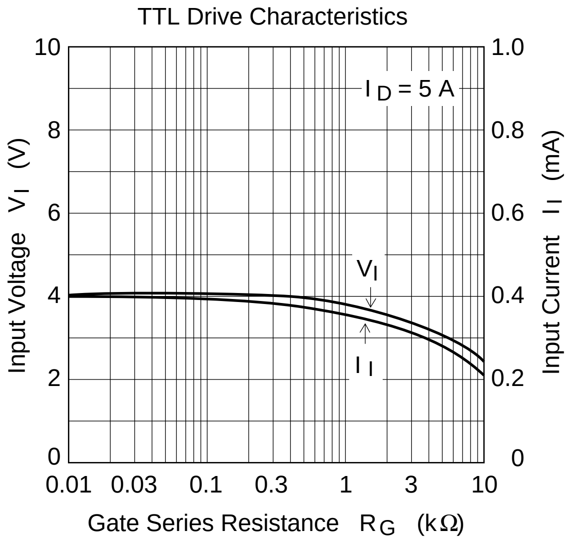

Switching Characteristics
VGS = 5 V, VDD ≒ 30 V
PW = 300 µs, duty ≦ 1 %
t d(off)
t f
t r
t d(on)
Switching Time t (µs)
Drain Current I D (A)
1000
500
200
100
50
20
10
0.5
1
2
5
10
20
50

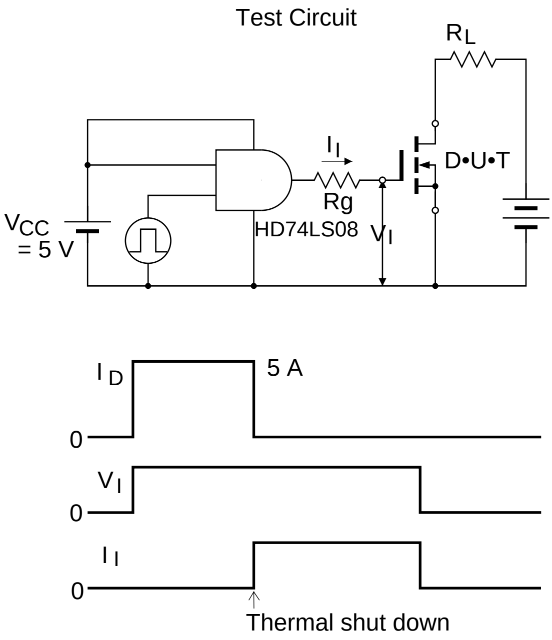

Reverse Drain Current vs.
Souece to Drain Voltage
Pulse Test
VGS = 5 V
0 V
Reverse Drain Current I DR (A)
Source to Drain Voltage V SD (V)
50
40
30
20
10
0
0.4
0.8
1.2
1.6
2.0


Typical Capacitance vs.
Drain to Source Voltage
Coss
VGS = 0
f = 1 MHz
Capacitance C (pF)
Drain to Source Voltage VDS (V)
10000
1000
100
10
0
10
20
30
40
50

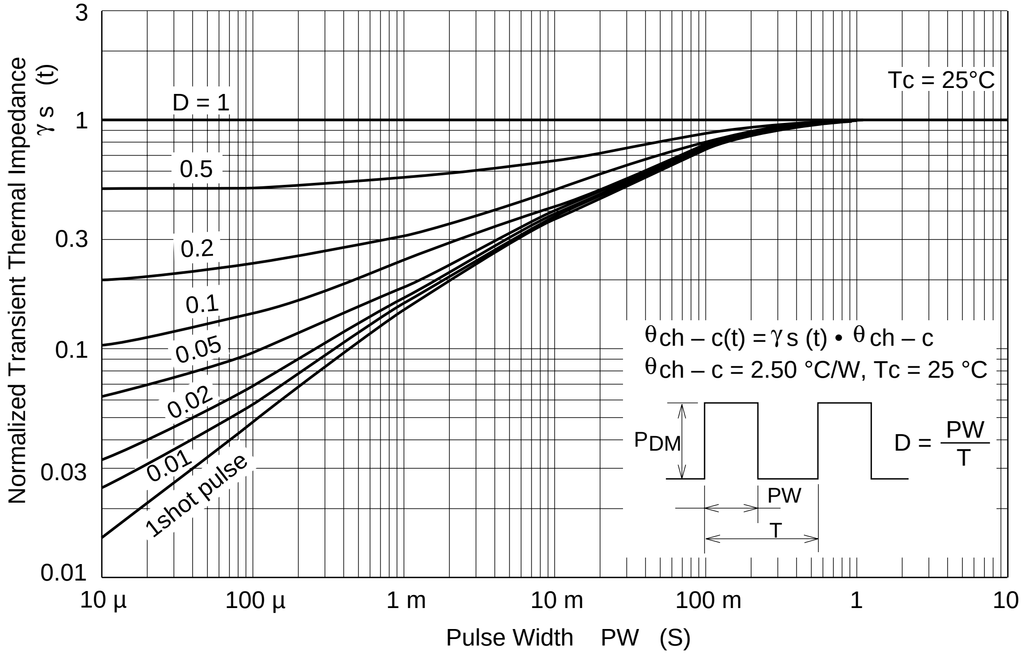

Gate to Source Voltage vs.
Shutdown Time of Load–Short Test
Gate to Source Voltage VGS (V)
VDD = 36 V
24 V
12 V
9 V
0 2 4 6 8 10
0.1 0.2 0.5 1 2 5 10 20 50 100
Shutdown Time of Load–Short Test
Pw (mS)


Shutdown Case Temperature vs.
Gate to Source Voltage
Shutdown Case Temperature Tc (°C)
ID = 5 A
100 120 140 160 180 200
0 2 4 6 8 10
Gate to Source Voltage VGS (V)

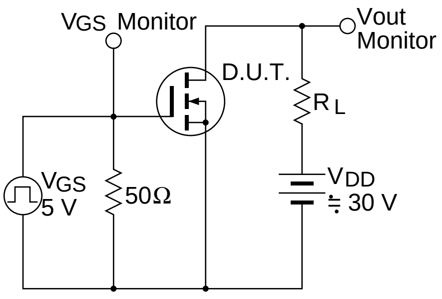

TTL Drive Characteristics
Input Voltage VI (V)
Input Current II (mA)
ID = 5 A
VI
II
0 2 4 6 8 10
0 0.2 0.4 0.6 0.8 1.0
0.01 0.03 0.1 0.3 1 3 10
Gate Series Resistance RG (kΩ)


Test Circuit
RL
II
D•U•T
Rg
VCC
= 5 V
HD74LS08
VI
ID
5 A
0
VI
0
II
0
Thermal shut down

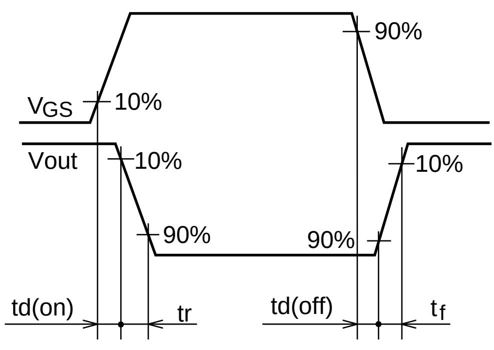
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



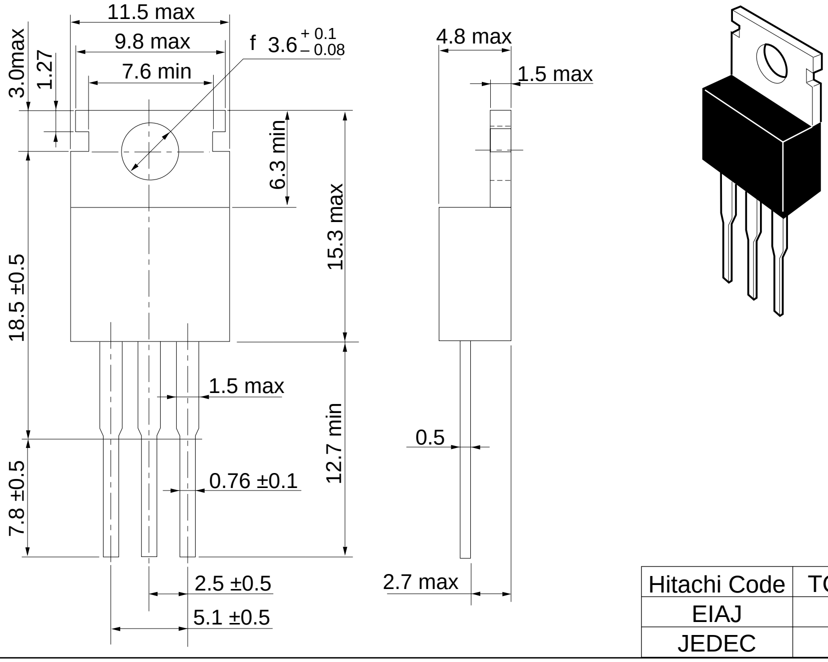
Waveform



Package Dimensions

Unit : mm

• HDPAK



Hitachi Code	TO–220AB
EIAJ	SC–46
JEDEC	—

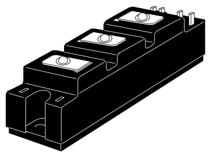
PM4550J

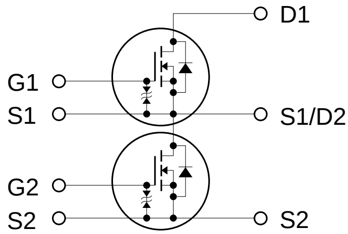
Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	450	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	50	A
Drain peak current	$I_{D(peak)}$	120	A
Body-drain diode reverse drain current	I_{DR}	50	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	120	A
Channel dissipation	Pch*1	250	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

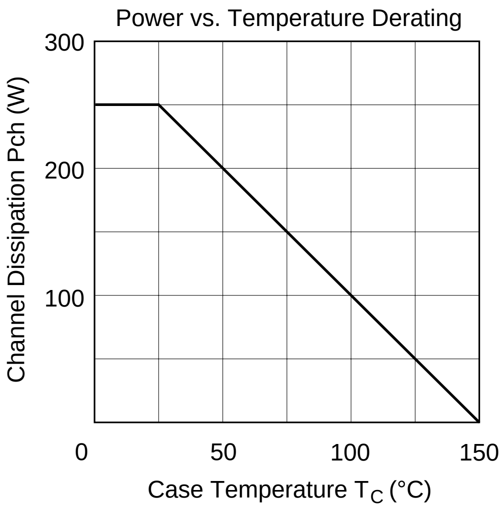
Electrical Characteristics (Ta = 25°C) (Per FET chip)

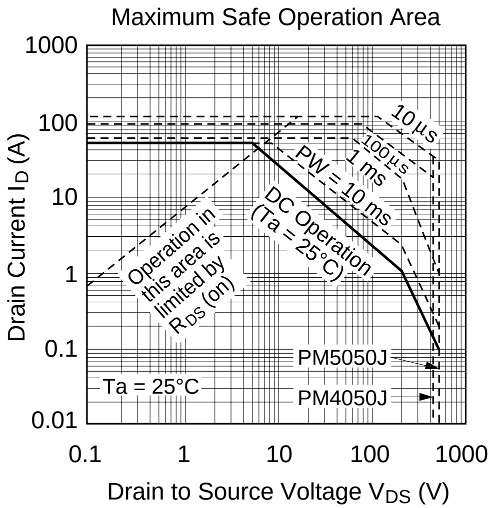
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	500	µA	V_{DS} = 360 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	3.5	4.5	V	I_D = 25 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.14	0.18	Ω	I_D = 25 A, V_{GS} = 10 V*1
Forward transfer admittance	$\|y_{fs}\|$	—	30	—	S	I_D = 25 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	6600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	1550	—		
Reverse transfer capacitance	Crss	—	250	—		
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	I_D = 25 A, V_{GS} = 10 V Rg = 50 Ω R_L = 1.2 Ω
Rise time	t_r	—	270	—		
Turn-off delay time	$t_{d(off)}$	—	250	—		
Fall time	t_f	—	140	—		
Body-drain diode forward voltage	V_{DF}	—	1.6	—	V	I_F = 50 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 50 A, V_{GS} = 0 V di/dt = 100 A/µs

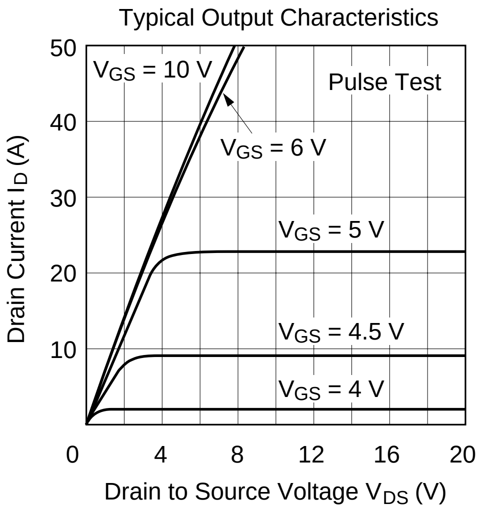
Note: 1. Pulse Test

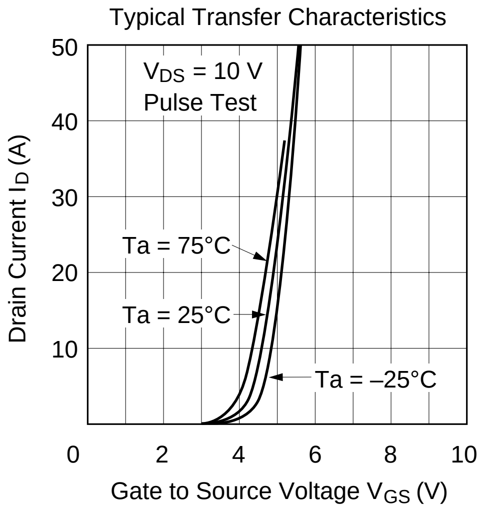
Mechanical characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	200	g

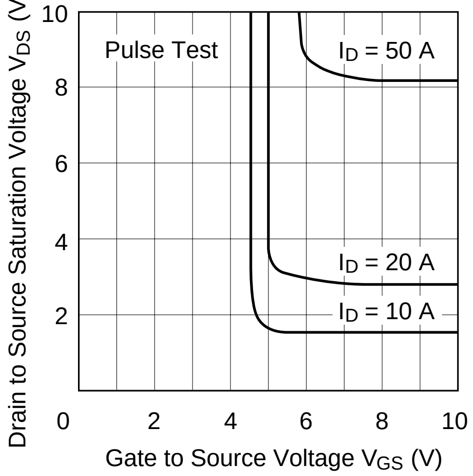

Power vs. Temperature Derating
Channel Dissipation Pch (W)
300
200
100
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
1000
100
10
1
0.1
0.01
10 μs
100 μs
1 ms
PW = 10 ms
DC Operation
(Ta = 25°C)
Operation in this area is limited by R_{DS} (on)
PM5050J
PM4050J
Ta = 25°C
0.1
1
10
100
1000
Drain to Source Voltage V_{DS} (V)

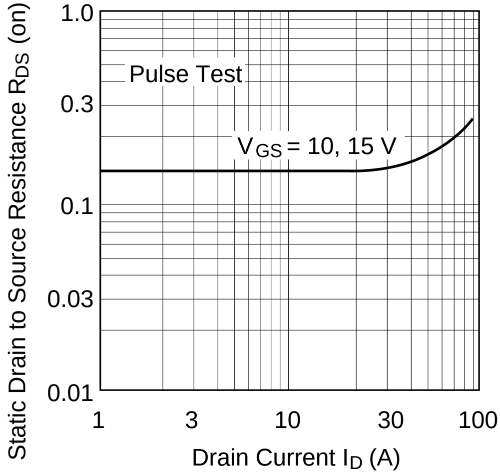

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
V_{DS} = 10 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

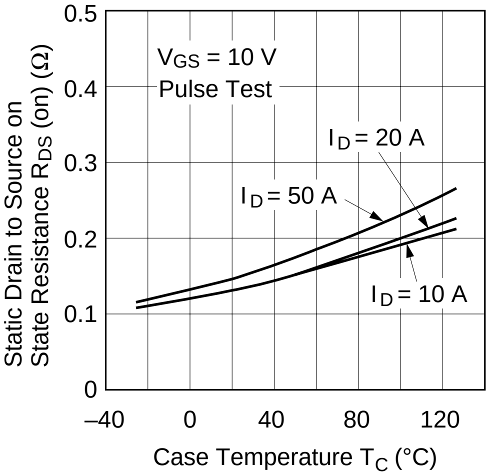
Drain to Source Saturation Voltage vs. Gate to Source Voltage



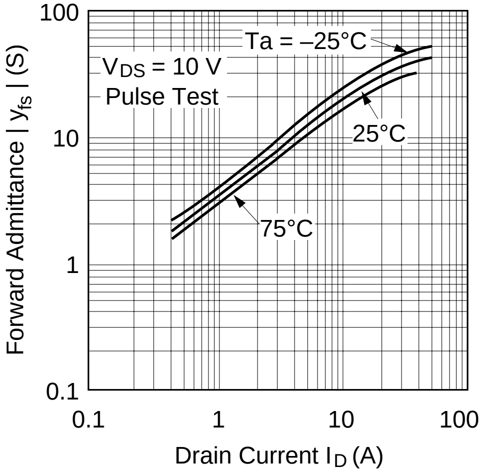
Static Drain to Source on State Resistance vs. Drain Current

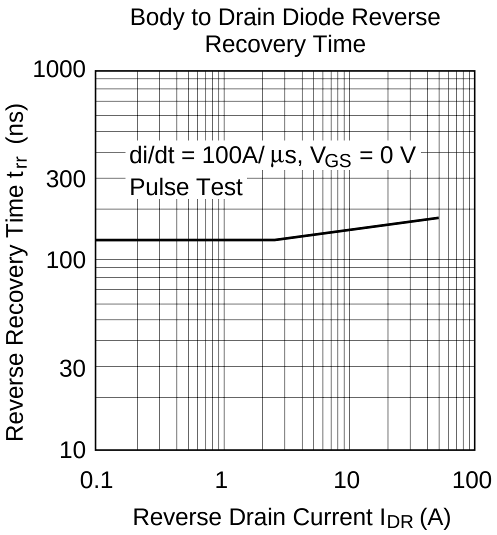


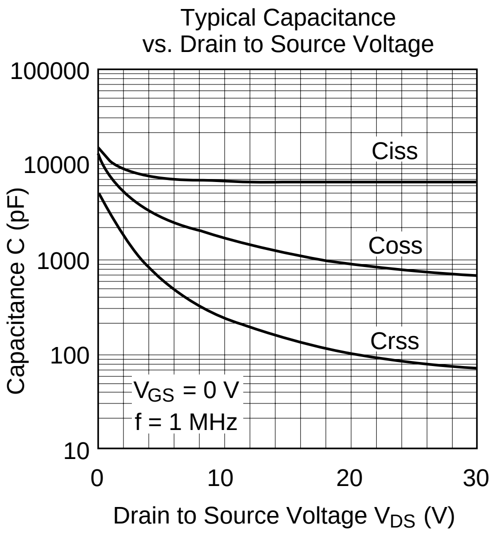
Static Drain to Source on State Resistance vs. Temperature

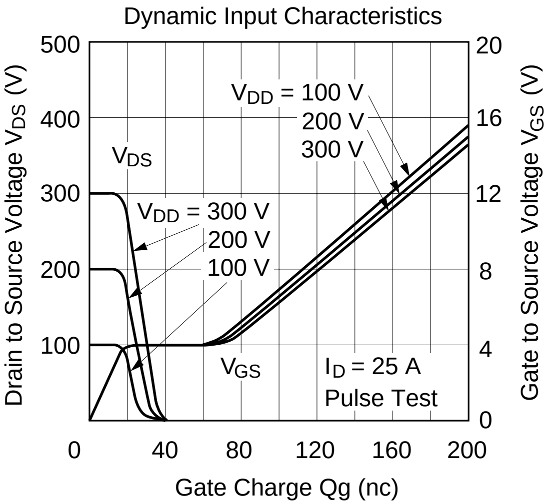


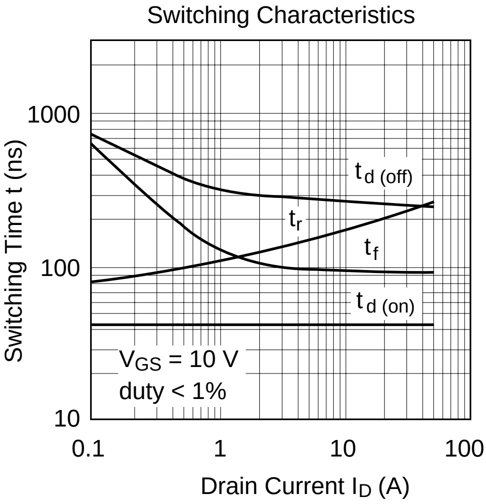
Forward Transfer Admittance vs. Drain Current

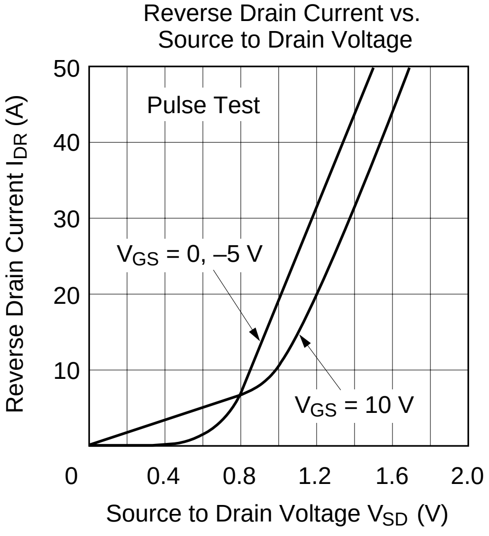


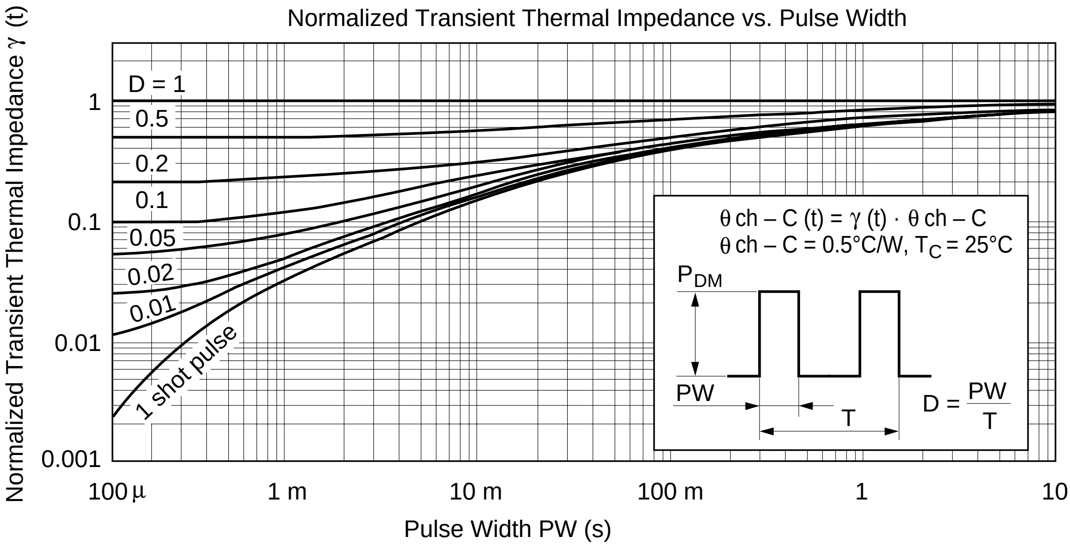

Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
Reverse Drain Current I_{DR} (A)
di/dt = 100A/ μs, V_{GS} = 0 V
Pulse Test
1000
300
100
30
10
0.1
1
10
100


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage V_{DS} (V)
Ciss
Coss
Crss
V_{GS} = 0 V
f = 1 MHz
100000
10000
1000
100
10
0
10
20
30

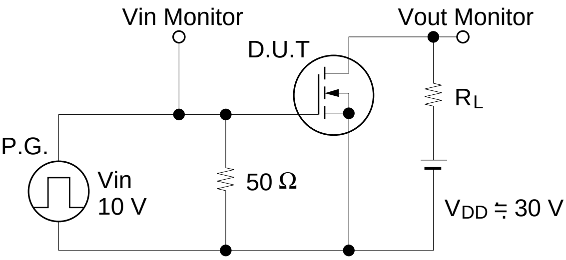

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
Gate Charge Qg (nc)
V_{DD} = 100 V
200 V
300 V
V_{DS}
V_{DD} = 300 V
200 V
100 V
V_{GS}
I_D = 25 A
Pulse Test
500
400
300
200
100
20
16
12
8
4
0
0
40
80
120
160
200


Switching Characteristics
Switching Time t (ns)
Drain Current I_D (A)
$t_{d\ (off)}$
t_r
t_f
$t_{d\ (on)}$
V_{GS} = 10 V
duty < 1%
1000
100
10
0.1
1
10
100

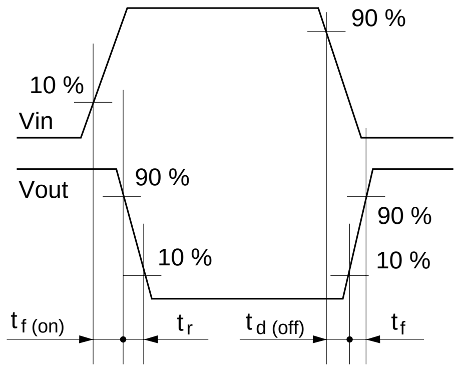

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
0
10
20
30
40
50
0.4
0.8
1.2
1.6
2.0


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
θ ch – C (t) = γ (t) · θ ch – C
θ ch – C = 0.5°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
Normalized Transient Thermal Impedance γ (t)
1
0.1
0.01
0.001
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit

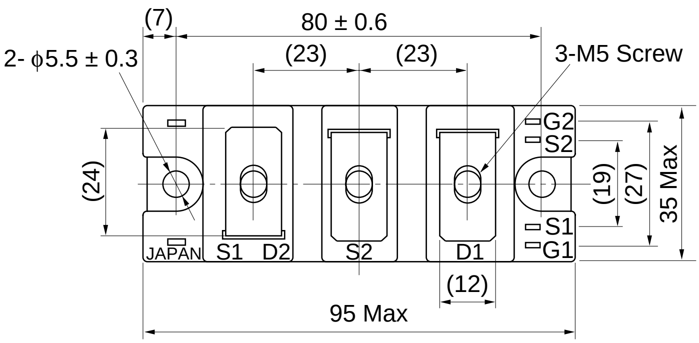


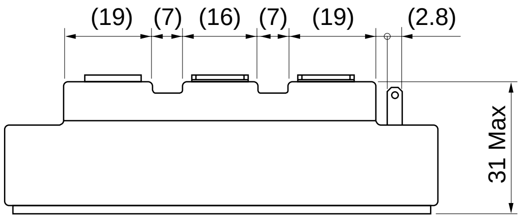
Wave Forms



Package Dimensions

Unit: mm





PM4575J

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

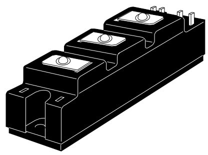
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

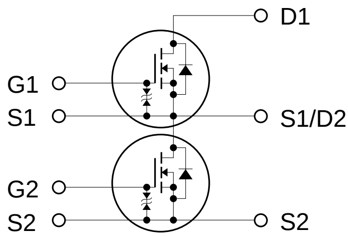
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	450	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	75	A
Drain peak current	$I_{D(peak)}$	180	A
Body-drain diode reverse drain current	I_{DR}	75	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	180	A
Channel dissipation	Pch*1	300	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

Electrical Characteristics (Ta = 25°C) (Per FET chip)

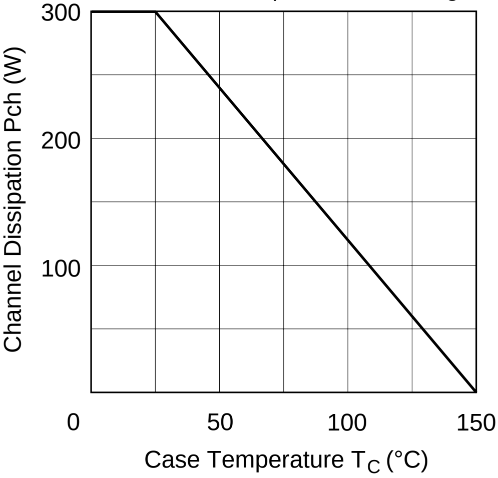
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	500	µA	V_{DS} = 360 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	3.7	4.44	V	I_D = 37 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.10	0.12	Ω	I_D = 37 A, V_{GS} = 10 V*1
Forward transfer admittance	$\lvert y_{fs} \rvert$	—	45	—	S	I_D = 37 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	9600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	2300	—		
Reverse transfer capacitance	Crss	—	330	—		
Turn-on delay time	$t_{d(on)}$	—	100	—	ns	I_D = 37 A, V_{GS} = 10 V Rg = 50 Ω R_L = 1 Ω
Rise time	t_r	—	310	—		
Turn-off delay time	$t_{d(off)}$	—	550	—		
Fall time	t_f	—	135	—		
Body-drain diode forward voltage	V_{DF}	—	1.8	—	V	I_F = 75 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 75 A, V_{GS} = 0 V di/dt = 100 A/µs

Note: 1. Pulse Test

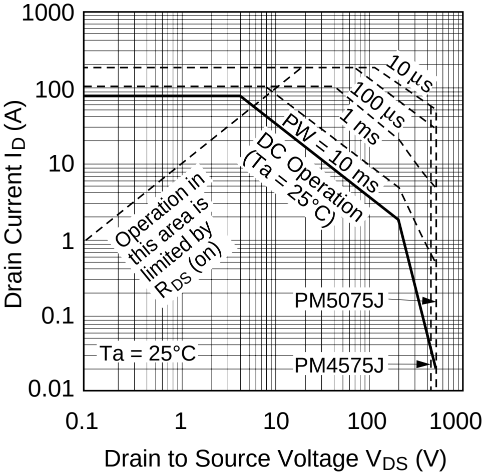
Mechanical characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	200	g

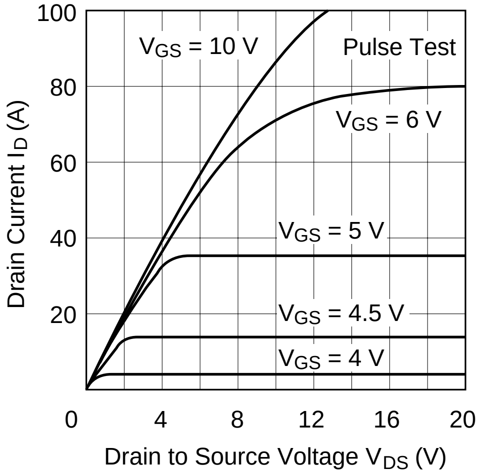
Power vs. Temperature Derating



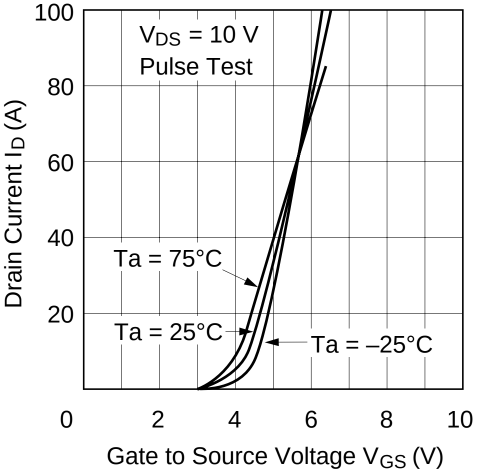
Maximum Safe Operation Area



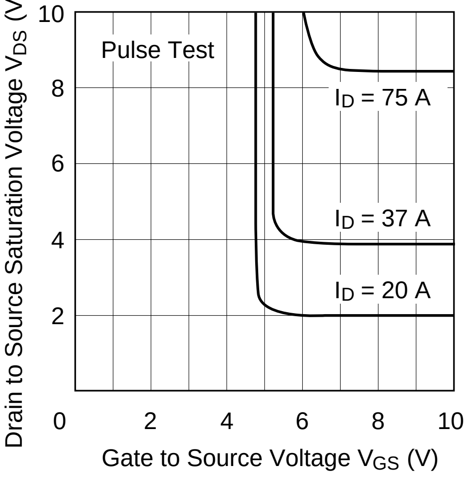
Typical Output Characteristics



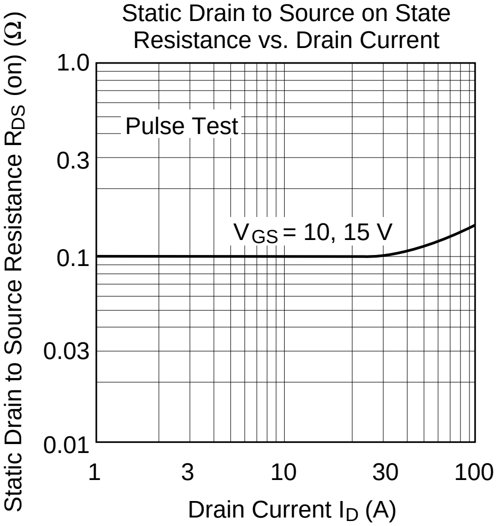
Typical Transfer Characteristics



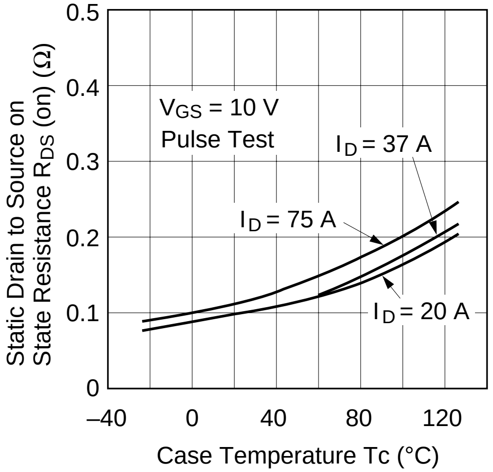
Drain to Source Saturation Voltage vs. Gate to Source Voltage



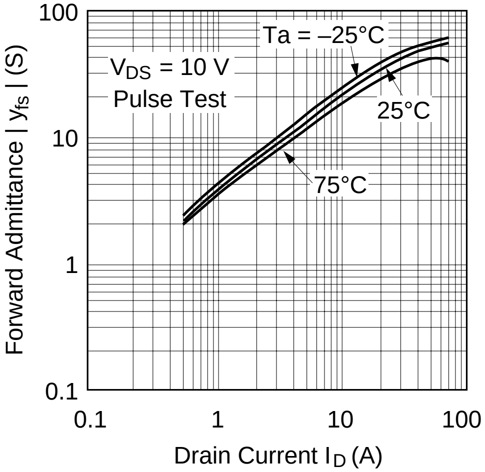
Static Drain to Source on State Resistance vs. Drain Current

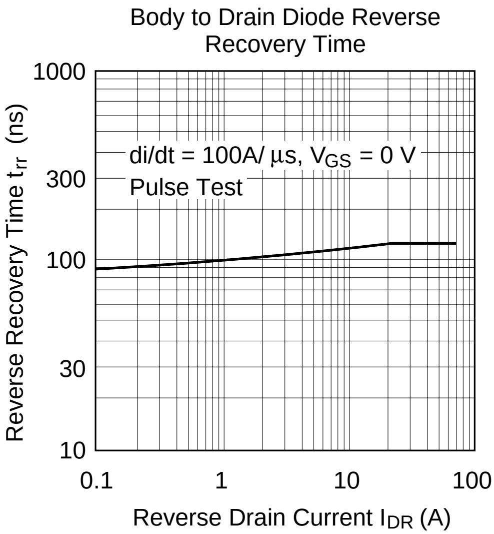


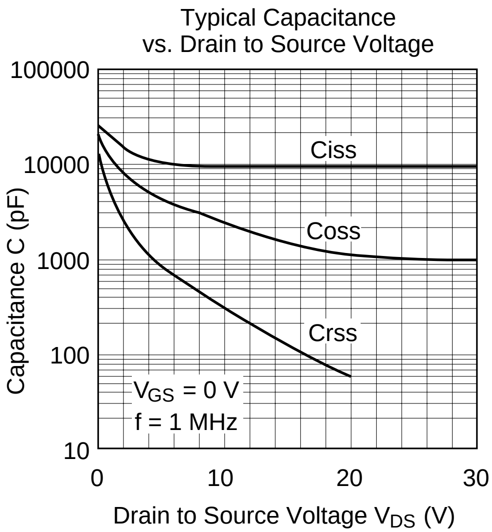
Static Drain to Source on State Resistance vs. Temperature

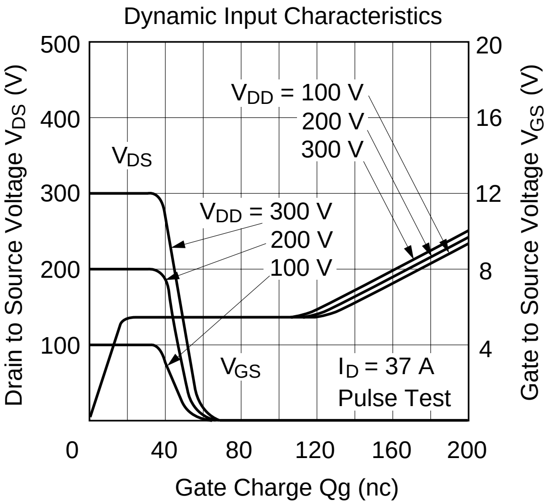


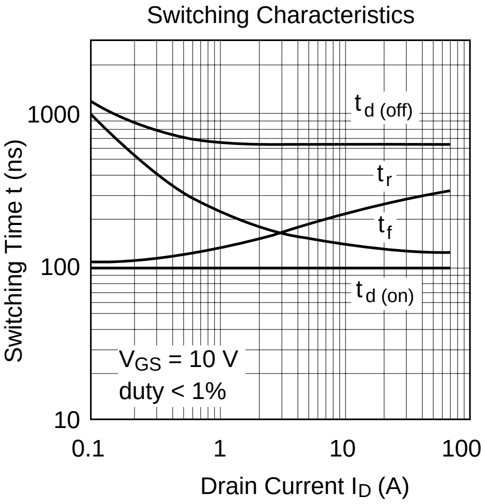
Forward Transfer Admittance vs. Drain Current

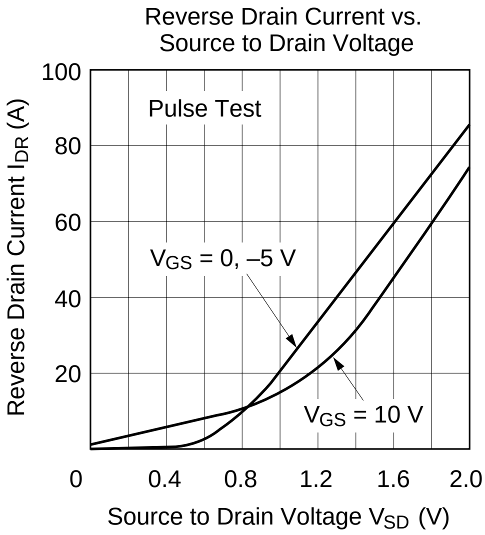


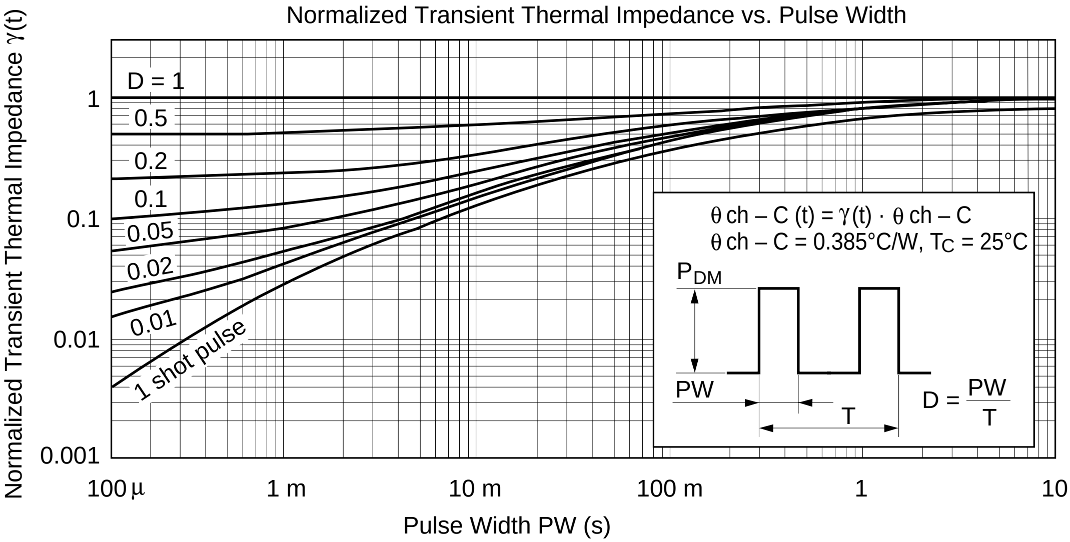

Body to Drain Diode Reverse
Recovery Time
Reverse Recovery Time t_{rr} (ns)
1000
300
100
30
10
di/dt = 100A/ μs, V_{GS} = 0 V
Pulse Test
0.1
1
10
100
Reverse Drain Current I_{DR} (A)


Typical Capacitance
vs. Drain to Source Voltage
Capacitance C (pF)
100000
10000
1000
100
10
Ciss
Coss
Crss
V_{GS} = 0 V
f = 1 MHz
0
10
20
30
Drain to Source Voltage V_{DS} (V)

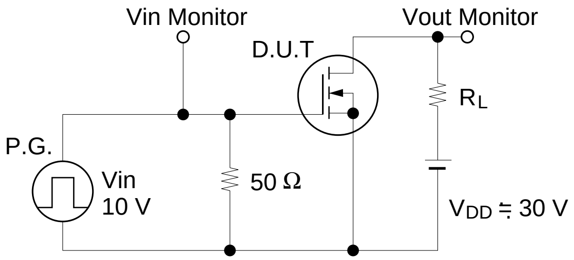

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
500
400
300
200
100
20
16
12
8
4
V_{DS}
V_{DD} = 100 V
200 V
300 V
V_{DD} = 300 V
200 V
100 V
V_{GS}
I_D = 37 A
Pulse Test
0
40
80
120
160
200
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
1000
100
10
$t_{d\ (off)}$
t_r
t_f
$t_{d\ (on)}$
V_{GS} = 10 V
duty < 1%
0.1
1
10
100
Drain Current I_D (A)

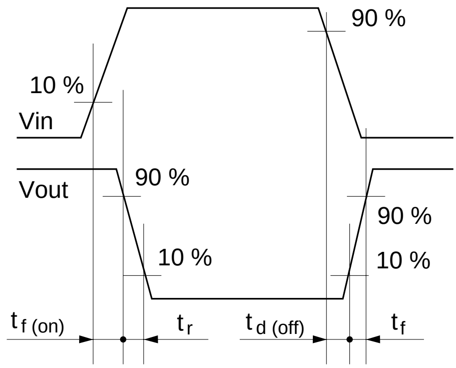

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ(t)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
1
0.1
0.01
0.001
θ ch – C (t) = γ(t) · θ ch – C
θ ch – C = 0.385°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit

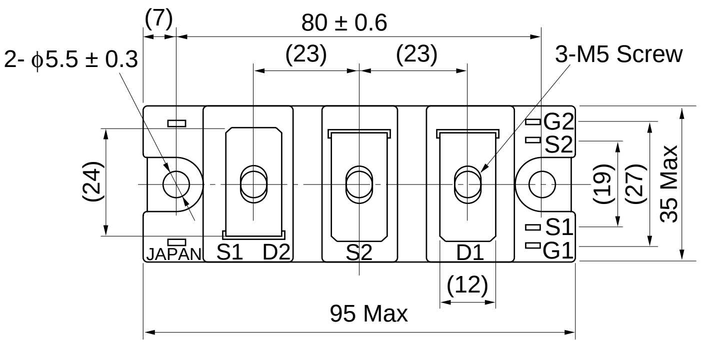


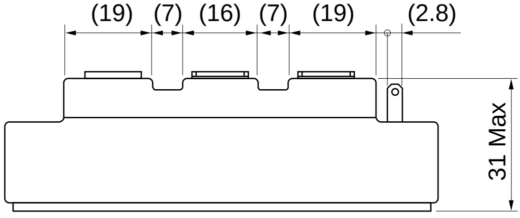
Wave Forms



Package Dimensions

Unit: mm





PM45100K

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

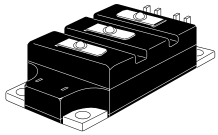
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

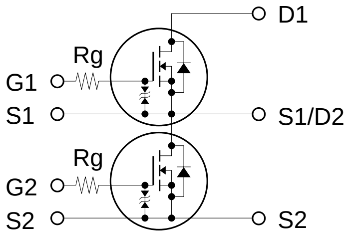
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	450	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	100	A
Drain peak current	$I_{D(peak)}$	240	A
Body-drain diode reverse drain current	I_{DR}	100	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	240	A
Channel dissipation	Pch*1	400	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

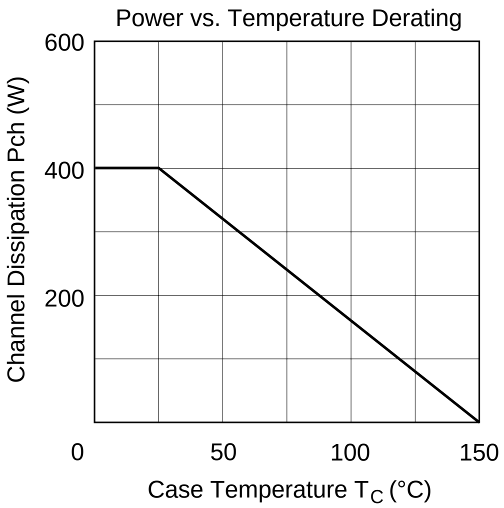
Electrical Characteristics (Ta = 25°C) (Per FET chip)

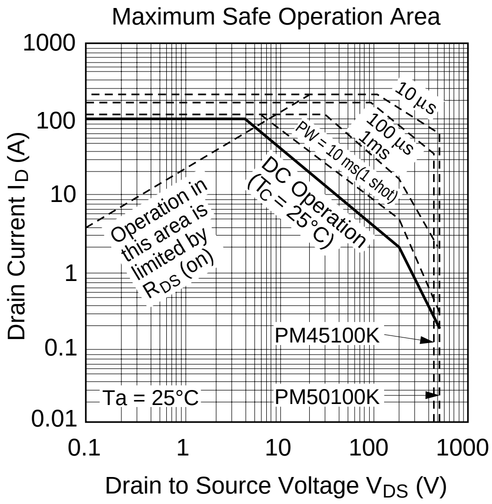
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	1	mA	V_{DS} = 360 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	4.0	5.0	V	I_D = 50 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.08	0.10	Ω	I_D = 50 A, V_{GS} = 10 V*1
Forward transfer admittance	$\|y_{fs}\|$	—	55	—	S	I_D = 50 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	14600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	3500	—		
Reverse transfer capacitance	Crss	—	650	—		
Turn-on delay time	$t_{d(on)}$	—	200	—	ns	I_D = 50 A, V_{GS} = 10 V Rg = 50 Ω R_L = 0.6 Ω
Rise time	t_r	—	690	—		
Turn-off delay time	$t_{d(off)}$	—	760	—		
Fall time	t_f	—	260	—		
Body-drain diode forward voltage	V_{DF}	—	1.6	—	V	I_F = 100 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 100 A, V_{GS} = 0 V di/dt = 100 A/µs

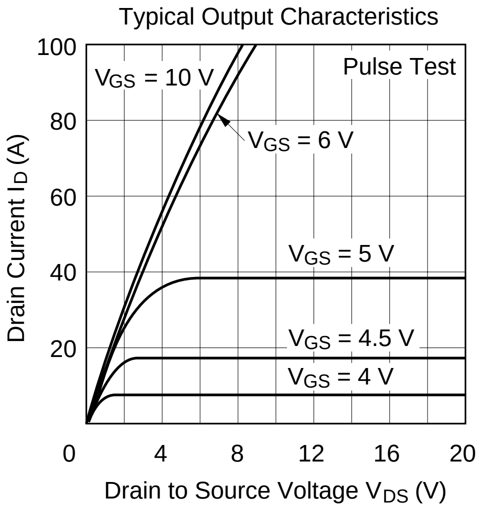
Note: 1 Pulse Test

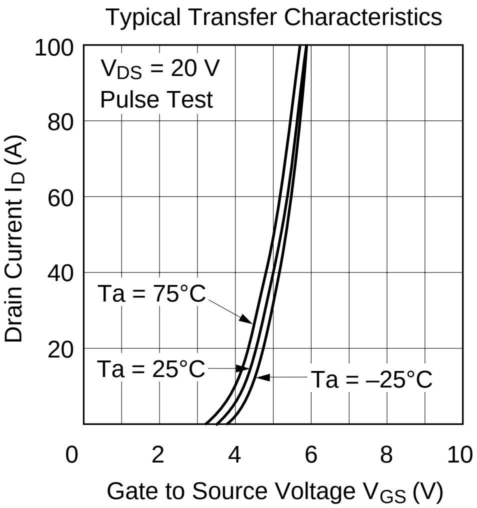
Mechanical characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	380	g

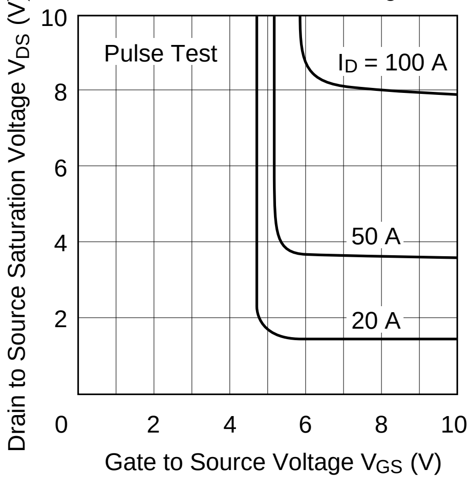

Power vs. Temperature Derating
Channel Dissipation Pch (W)
600
400
200
0
50
100
150
Case Temperature T_C (°C)


Maximum Safe Operation Area
Drain Current I_D (A)
1000
100
10
1
0.1
0.01
0.1
1
10
100
1000
Drain to Source Voltage V_{DS} (V)
10 μs
100 μs
1ms
PW = 10 ms(1 shot)
DC Operation (T_C = 25°C)
Operation in this area is limited by R_{DS} (on)
PM45100K
PM50100K
Ta = 25°C

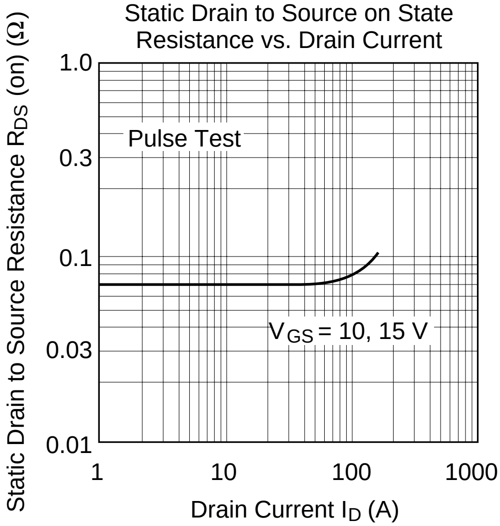

Typical Output Characteristics
Drain Current I_D (A)
100
80
60
40
20
0
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V


Typical Transfer Characteristics
Drain Current I_D (A)
100
80
60
40
20
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)
V_{DS} = 20 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C

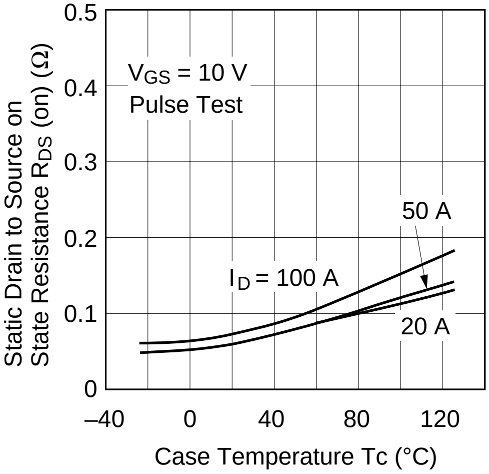
Drain to Source Saturation Voltage vs. Gate to Source Voltage



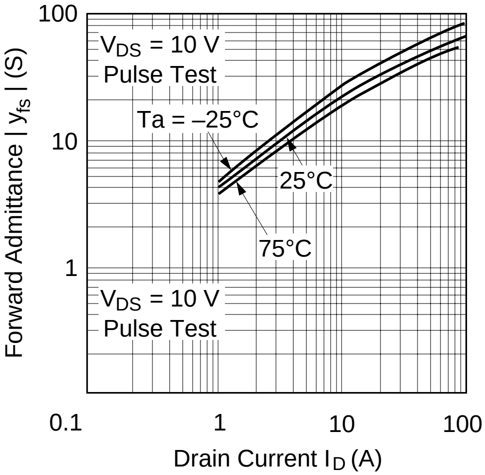
Static Drain to Source on State Resistance vs. Drain Current



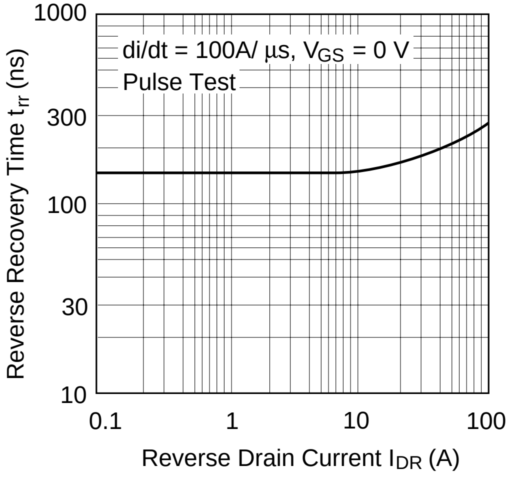
Static Drain to Source on State Resistance vs. Temperature



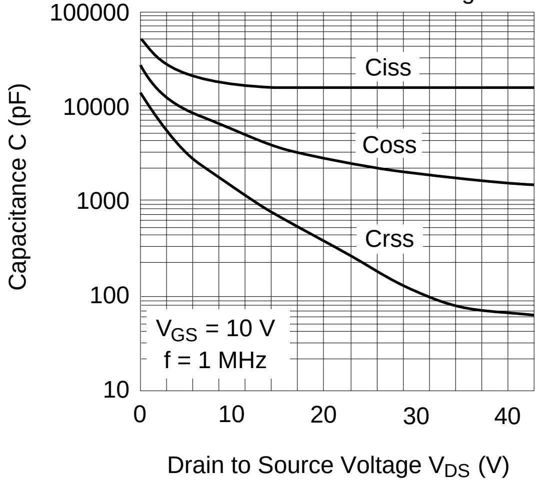
Forward Transfer Admittance vs. Drain Current



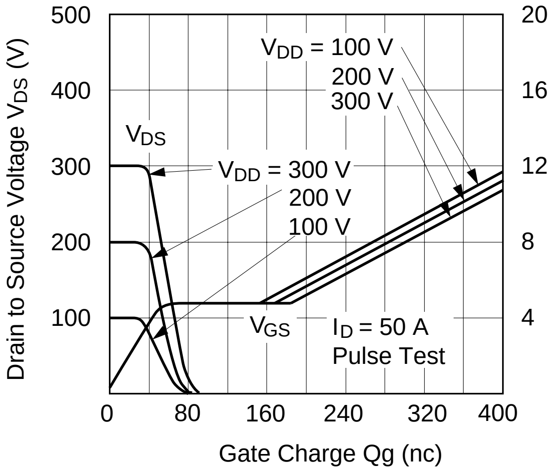
Body to Drain Diode Reverse Recovery Time



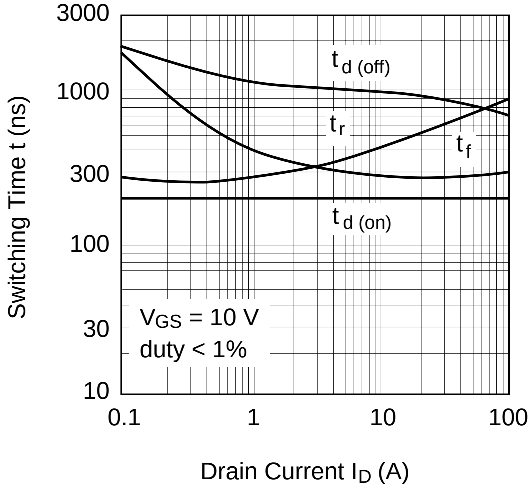
Typical Capacitance vs. Drain to Source Voltage

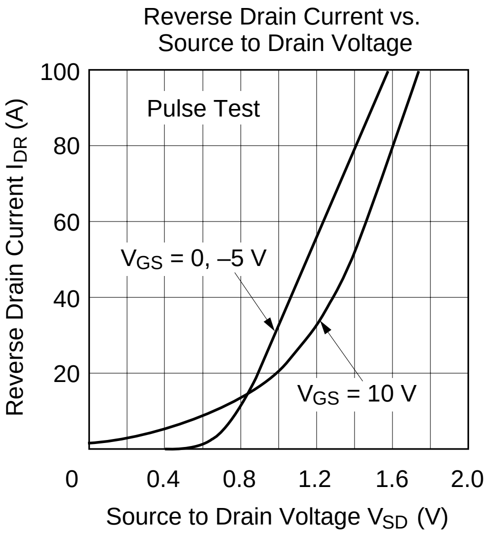


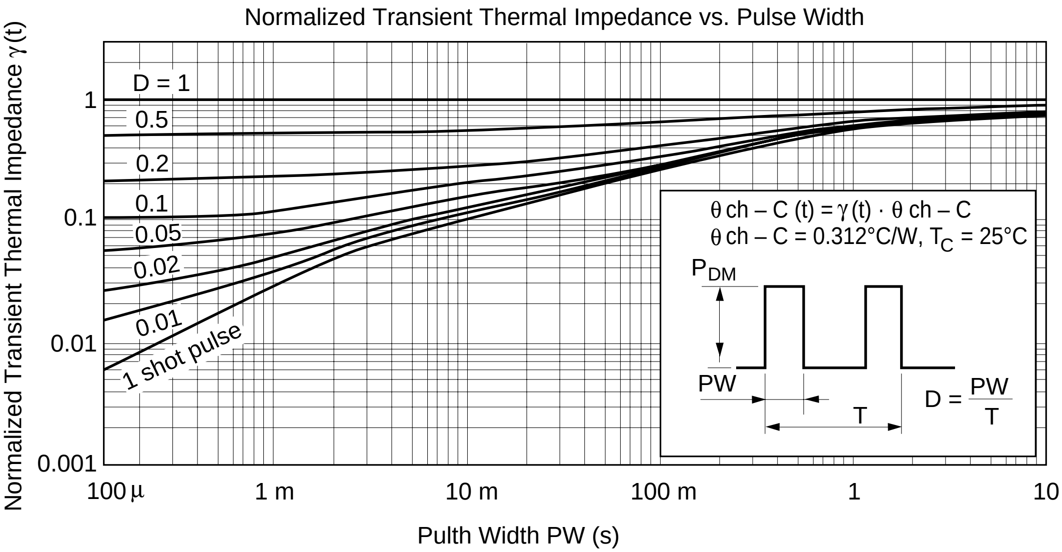
Dynamic Input Characteristics



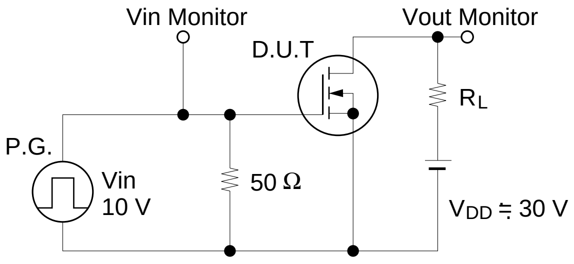
Switching Characteristics



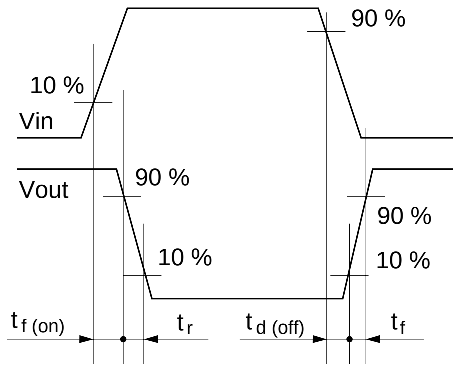

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
θ ch – C (t) = γ (t) · θ ch – C
θ ch – C = 0.312°C/W, T_C = 25°C
P_{DM}
PW
T
D = PW / T
Normalized Transient Thermal Impedance γ(t)
1
0.1
0.01
0.001
100 µ
1 m
10 m
100 m
1
10
Pulth Width PW (s)

Switching Time Test Circuit

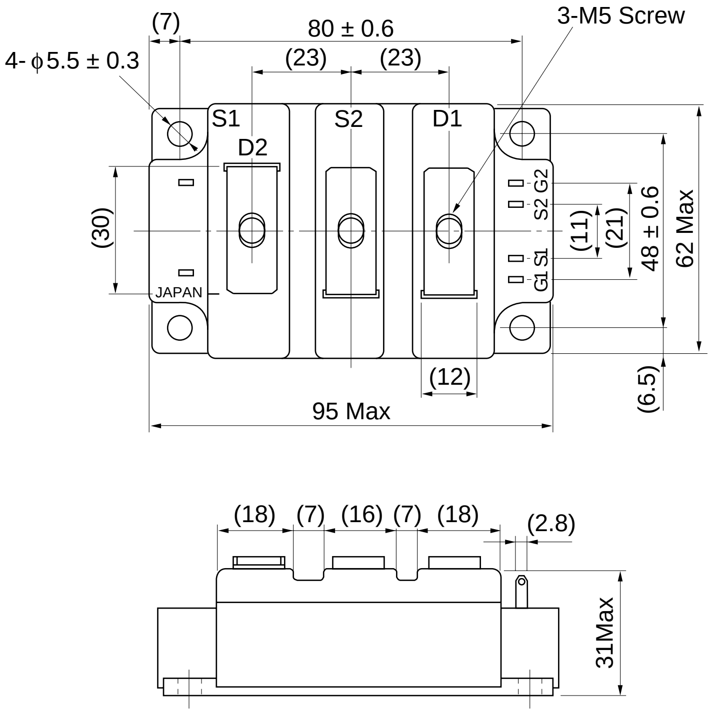


Wave Forms



Package Dimensions

Unit: mm



PM45150K

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

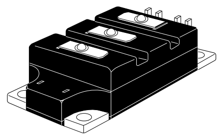
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

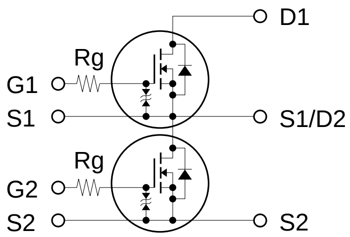
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	450	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	150	A
Drain peak current	$I_{D(peak)}$	360	A
Body-drain diode reverse drain current	I_{DR}	150	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	360	A
Channel dissipation	Pch*1	500	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dissipation	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

Electrical Characteristics (Ta = 25°C) (Per FET chip)

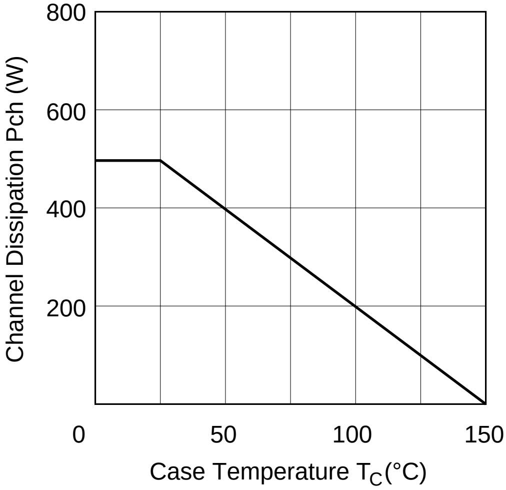
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	1	mA	V_{DS} = 360 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	4.5	6.0	V	I_D = 75 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.06	0.08	Ω	I_D = 75 A, V_{GS} = 10 V*1
Forward transfer admittance	$\|y_{fs}\|$	—	80	—	S	I_D = 75 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	22600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V
Output capacitance	Coss	—	4600	—		f = 1 MHz
Reverse transfer capacitance	Crss	—	580	—		
Turn-on delay time	$t_{d(on)}$	—	280	—	ns	I_D = 75 A, V_{GS} = 10 V
Rise time	t_r	—	820	—		Rg = 50 Ω
Turn-off delay time	$t_{d(off)}$	—	1190	—		R_L = 0.4 Ω
Fall time	t_f	—	400	—		
Body-drain diode forward voltage	V_{DF}	—	2.0	—	V	I_F = 150 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 150 A, V_{GS} = 0 V di/dt = 100 A/µs

Note: 1. Pulse Test

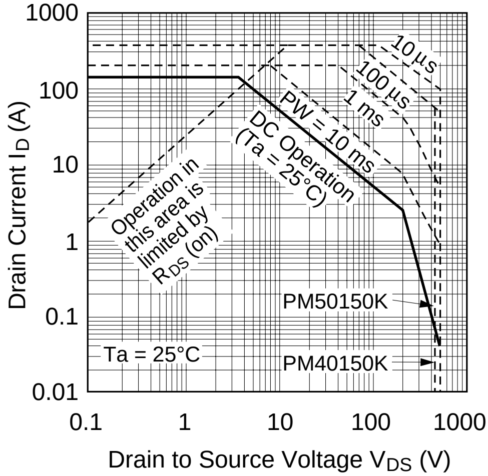
Mechanical characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	380	g

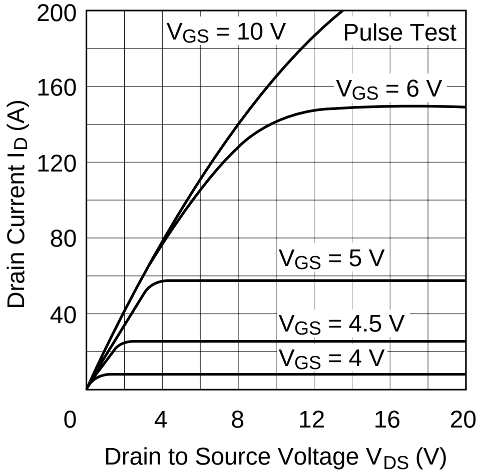
Power vs. Temperature Derating



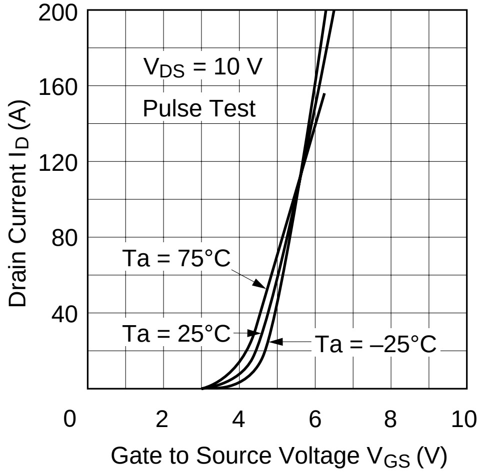
Maximum Safe Operation Area

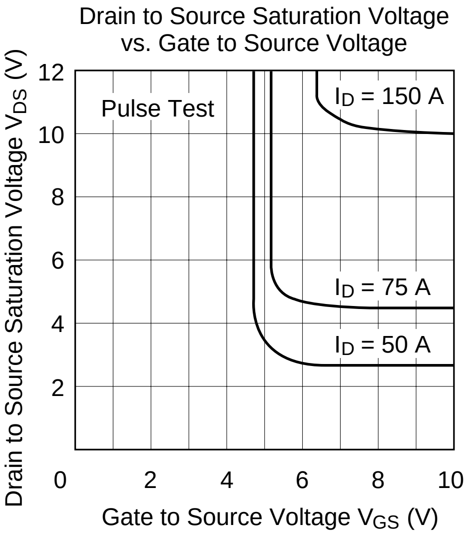


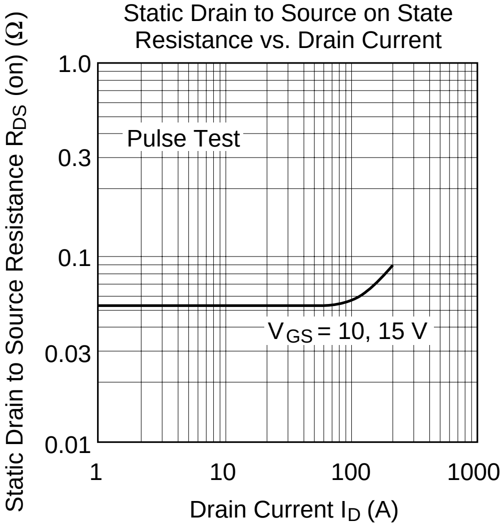
Typical Output Characteristics

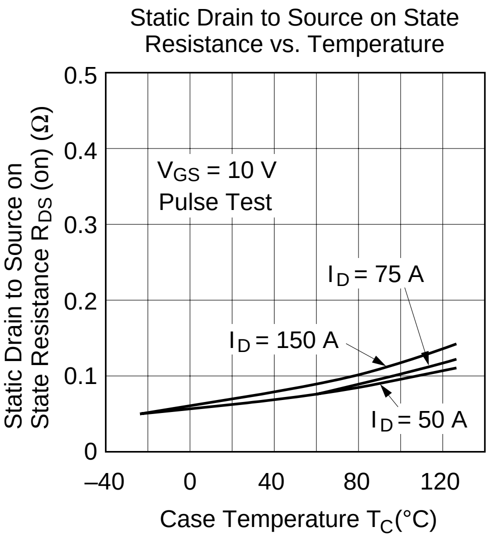


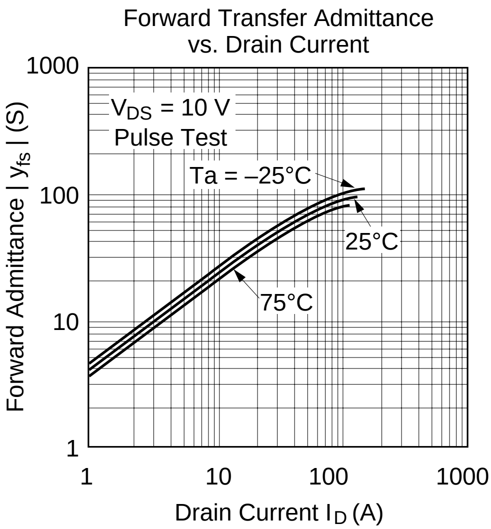
Typical Transfer Characteristics

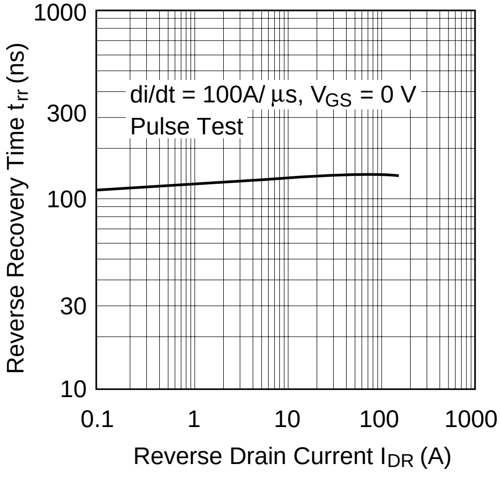



Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 150 A
I_D = 75 A
I_D = 50 A
Drain to Source Saturation Voltage V_{DS} (V)
12
10
8
6
4
2
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)

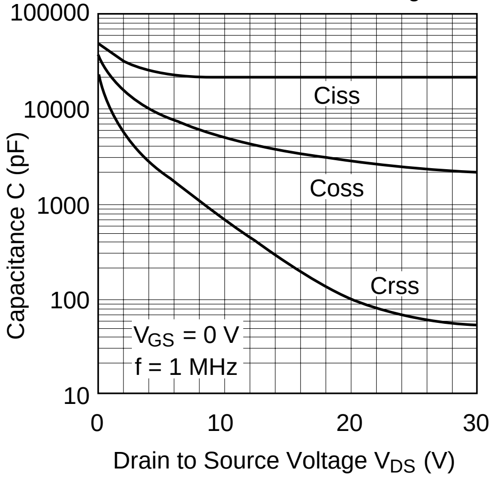

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 10, 15 V
Static Drain to Source Resistance R_{DS} (on) (Ω)
1.0
0.3
0.1
0.03
0.01
1
10
100
1000
Drain Current I_D (A)


Static Drain to Source on State
Resistance vs. Temperature
V_{GS} = 10 V
Pulse Test
I_D = 75 A
I_D = 150 A
I_D = 50 A
Static Drain to Source on
State Resistance R_{DS} (on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
Case Temperature T_C(°C)

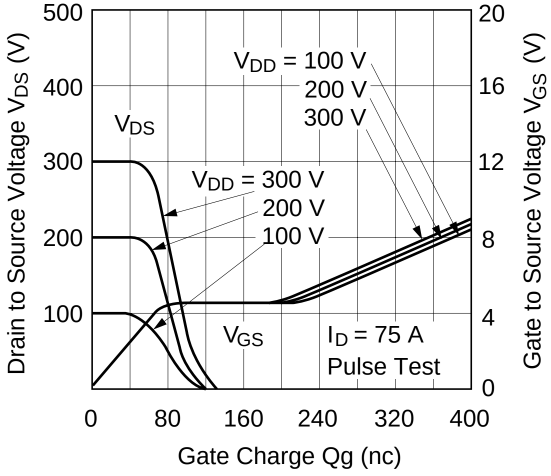

Forward Transfer Admittance
vs. Drain Current
V_{DS} = 10 V
Pulse Test
Ta = –25°C
25°C
75°C
Forward Admittance | y_{fs} | (S)
1000
100
10
1
1
10
100
1000
Drain Current I_D (A)



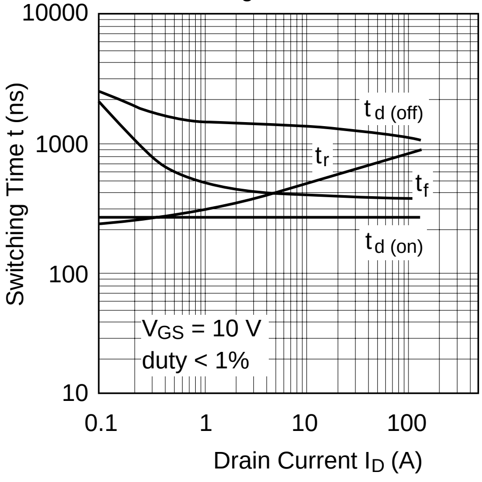
Body to Drain Diode Reverse Recovery Time



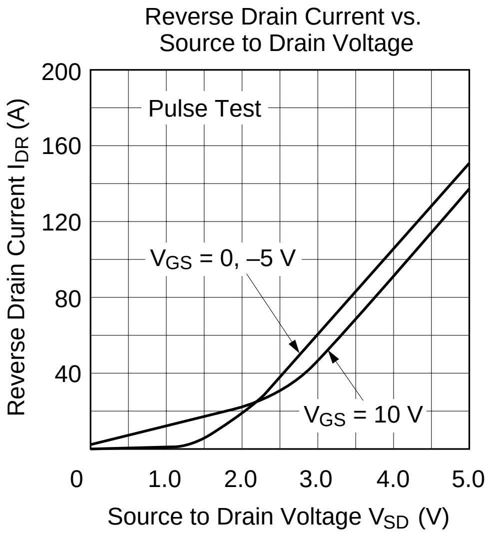
Typical Capacitance vs. Drain to Source Voltage

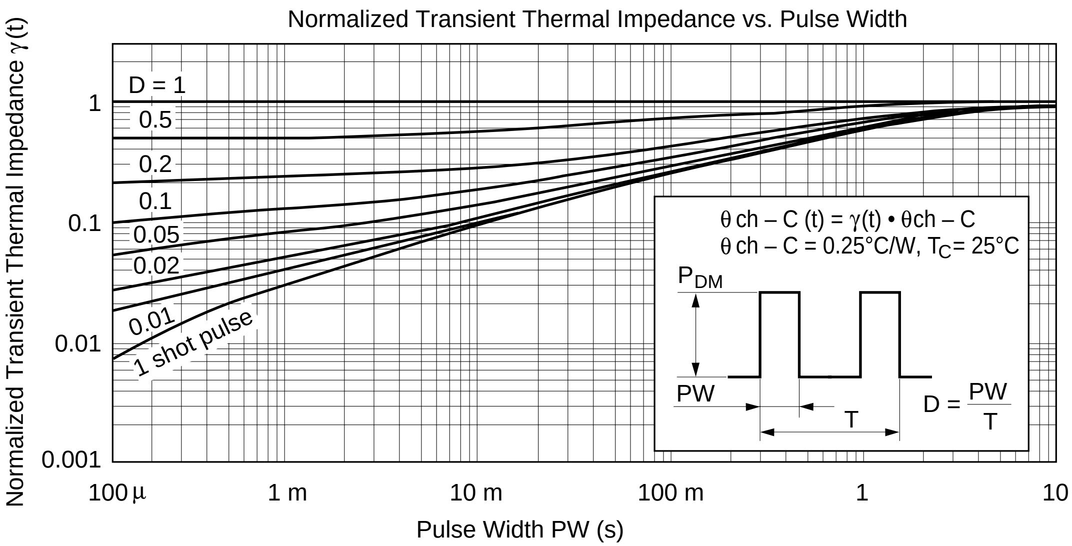


Dynamic Input Characteristics

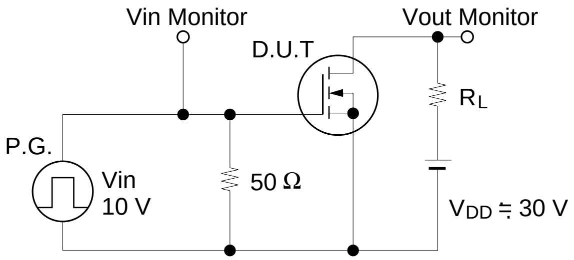


Switching Characteristics

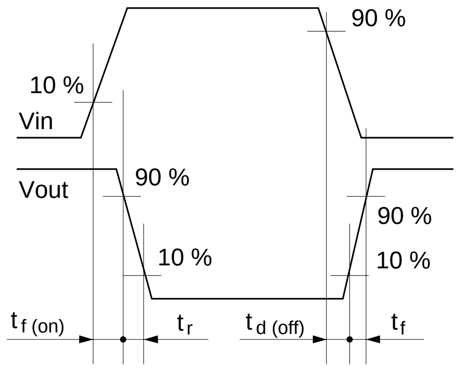

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_GS = 0, –5 V
V_GS = 10 V
Reverse Drain Current I_DR (A)
200
160
120
80
40
0
1.0
2.0
3.0
4.0
5.0
Source to Drain Voltage V_SD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ(t)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
θ ch – C (t) = γ(t) • θch – C
θ ch – C = 0.25°C/W, T_C = 25°C
P_DM
PW
T
D = PW / T
1
0.1
0.01
0.001
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit

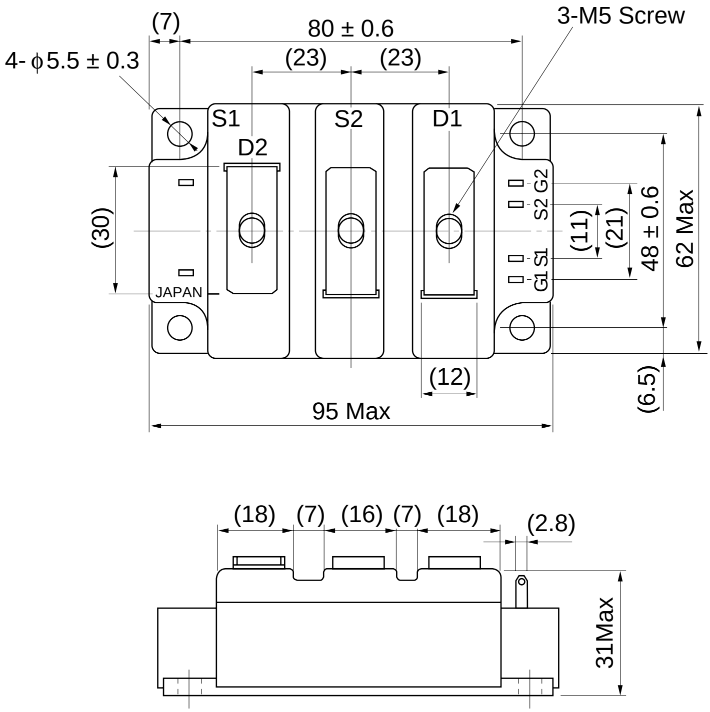


Wave Forms



Package Dimensions

Unit: mm



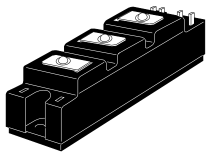
PM5050J

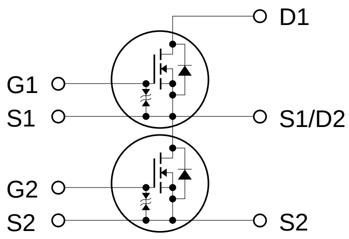
Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	500	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	50	A
Drain peak current	$I_{D(peak)}$	120	A
Body-drain diode reverse drain current	I_{DR}	50	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	120	A
Channel dissipation	Pch[*1]	250	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso[*2]	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

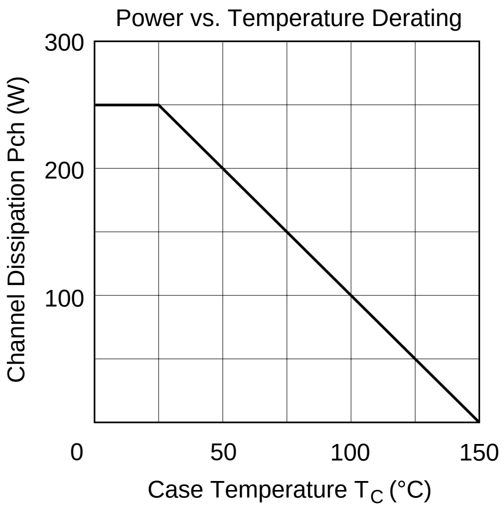
Electrical Characteristics (Ta = 25°C) (Per FET chip)

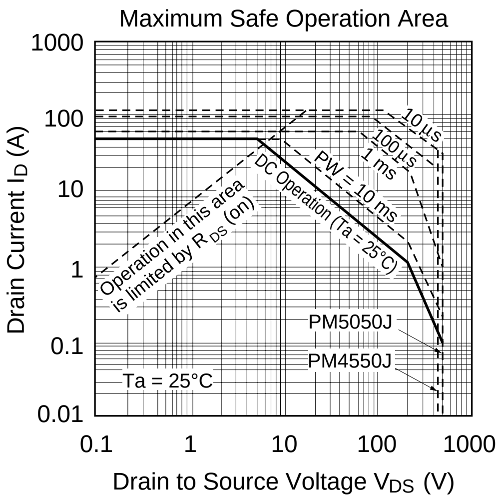
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	500	µA	V_{DS} = 400 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	3.5	4.5	V	I_D = 25 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.14	0.18	Ω	I_D = 25 A, V_{GS} = 10 V*1
Forward transfer admittance	$\lvert y_{fs} \rvert$	—	30	—	S	I_D = 25 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	6600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	1550	—		
Reverse transfer capacitance	Crss	—	250	—		
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	I_D = 25 A, V_{GS} = 10 V Rg = 50 Ω R_L = 1.2 Ω
Rise time	t_r	—	270	—		
Turn-off delay time	$t_{d(off)}$	—	250	—		
Fall time	t_f	—	140	—		
Body-drain diode forward voltage	V_{DF}	—	1.6	—	V	I_F = 50 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 50 A, V_{GS} = 0 V di/dt = 100 A/µs

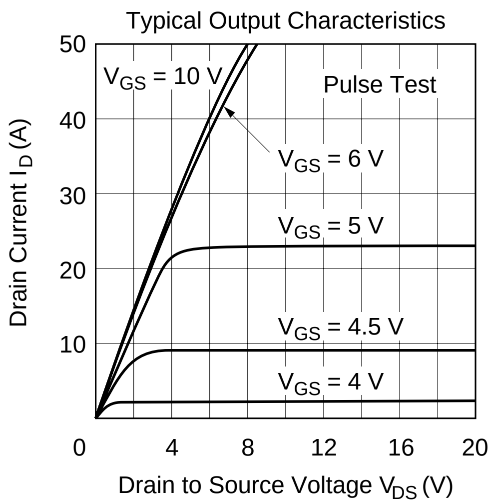
Note: 1. Pulse Test

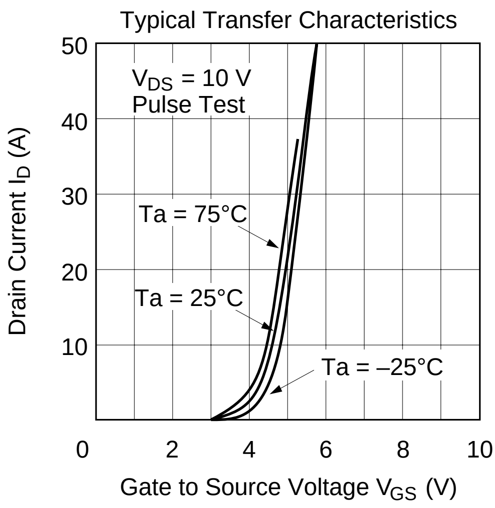
Mechanical characteristics

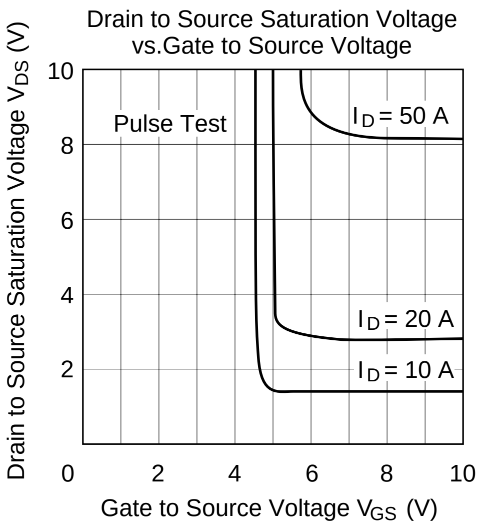
Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	200	g

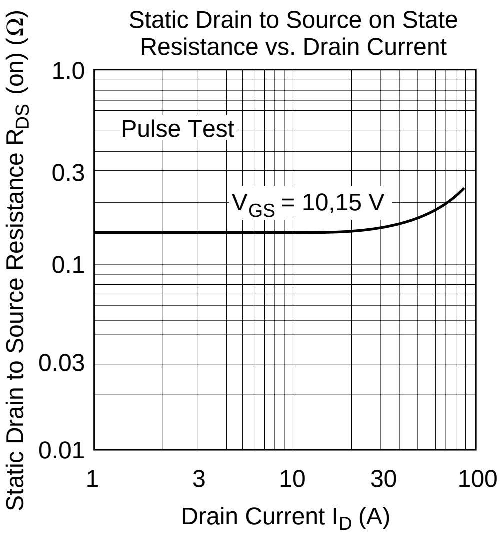

Power vs. Temperature Derating
Channel Dissipation Pch (W)
300
200
100
0
50
100
150
Case Temperature T_C (°C)

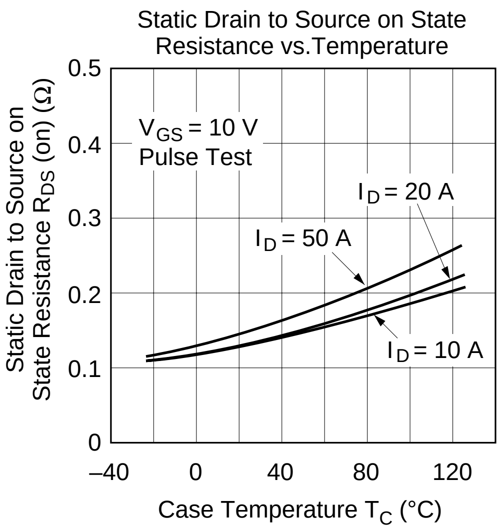

Maximum Safe Operation Area
Drain Current I_D (A)
1000
100
10
1
0.1
0.01
0.1
1
10
100
1000
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1 ms
PW = 10 ms
DC Operation (Ta = 25°C)
Operation in this area is limited by R_{DS} (on)
PM5050J
PM4550J
Ta = 25°C

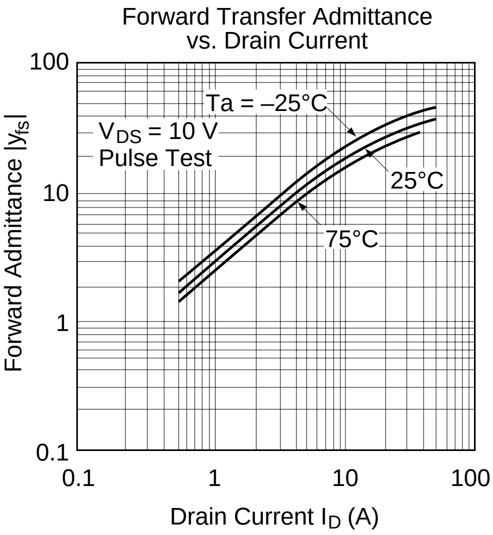

Typical Output Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
4
8
12
16
20
Drain to Source Voltage V_{DS} (V)
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V


Typical Transfer Characteristics
Drain Current I_D (A)
50
40
30
20
10
0
2
4
6
8
10
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C

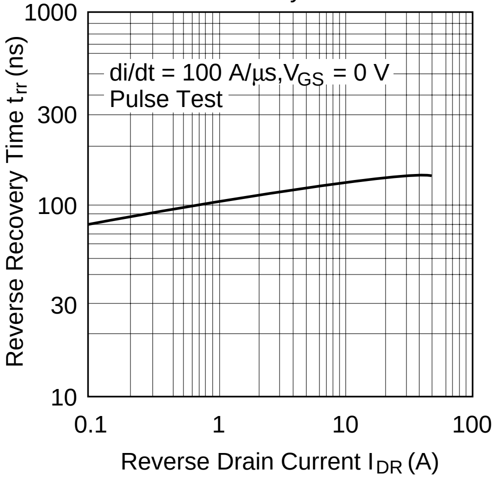

Drain to Source Saturation Voltage
vs.Gate to Source Voltage
Drain to Source Saturation Voltage V_{DS} (V)
Pulse Test
I_D = 50 A
I_D = 20 A
I_D = 10 A
0 2 4 6 8 10
10 8 6 4 2
Gate to Source Voltage V_{GS} (V)


Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source Resistance R_{DS} (on) (Ω)
Pulse Test
V_{GS} = 10,15 V
1.0 0.3 0.1 0.03 0.01
1 3 10 30 100
Drain Current I_D (A)

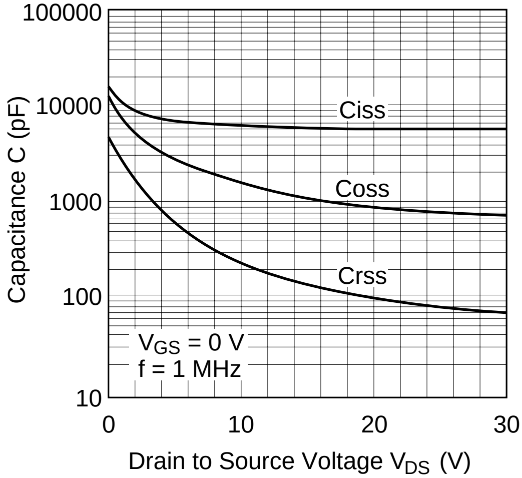

Static Drain to Source on State
Resistance vs.Temperature
Static Drain to Source on
State Resistance R_{DS} (on) (Ω)
V_{GS} = 10 V
Pulse Test
I_D = 20 A
I_D = 50 A
I_D = 10 A
0.5 0.4 0.3 0.2 0.1 0
–40 0 40 80 120
Case Temperature T_C (°C)


Forward Transfer Admittance
vs. Drain Current
Forward Admittance $|y_{fs}|$
Ta = –25°C
V_{DS} = 10 V
Pulse Test
25°C
75°C
100 10 1 0.1
0.1 1 10 100
Drain Current I_D (A)

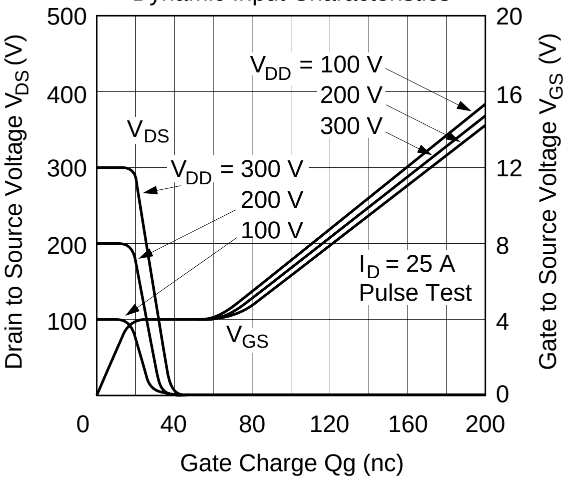
Body to Drain Diode Reverse Recovery Time



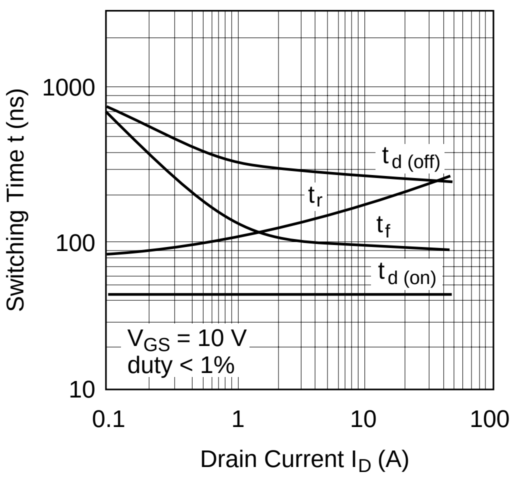
Typical Capacitance vs. Drain to Source Voltage

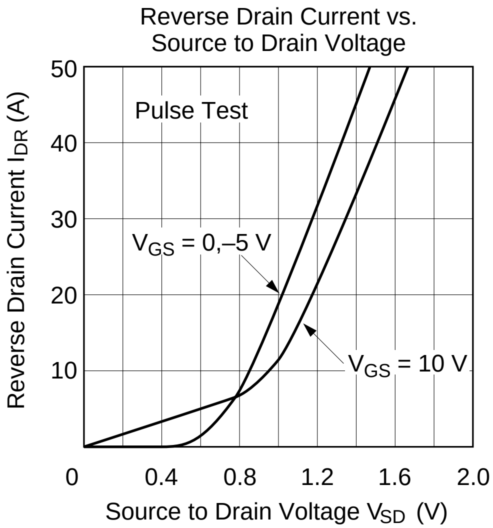


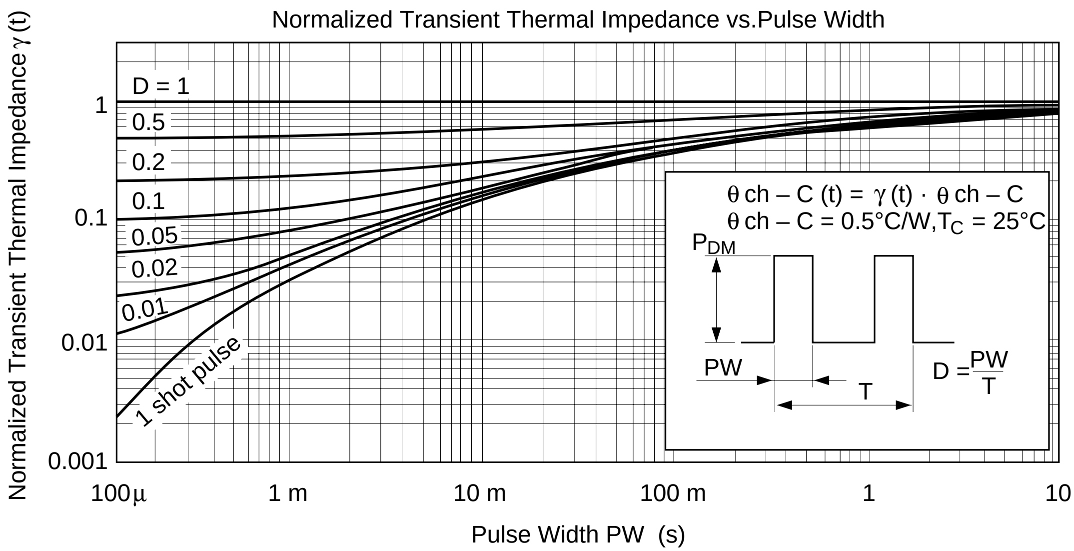
Dynamic Input Characteristics



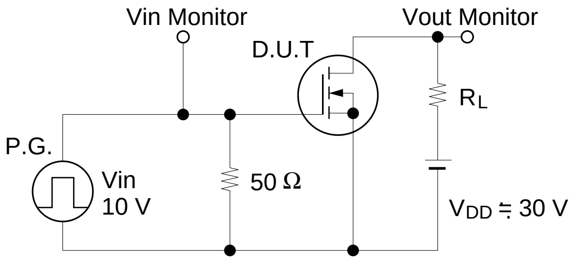
Switching Characteristics



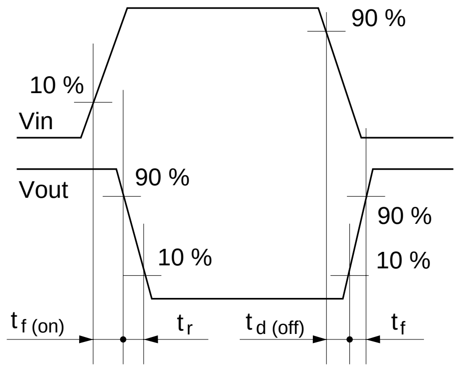

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_GS = 0,–5 V
V_GS = 10 V
Reverse Drain Current I_DR (A)
Source to Drain Voltage V_SD (V)
0
0.4
0.8
1.2
1.6
2.0
10
20
30
40
50


Normalized Transient Thermal Impedance vs.Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
θ ch – C (t) = γ (t) · θ ch – C
θ ch – C = 0.5°C/W,T_C = 25°C
P_DM
PW
T
D = PW/T
Normalized Transient Thermal Impedance γ (t)
Pulse Width PW (s)
100µ
1 m
10 m
100 m
1
10
1
0.1
0.01
0.001

Switching Time Test Circuit

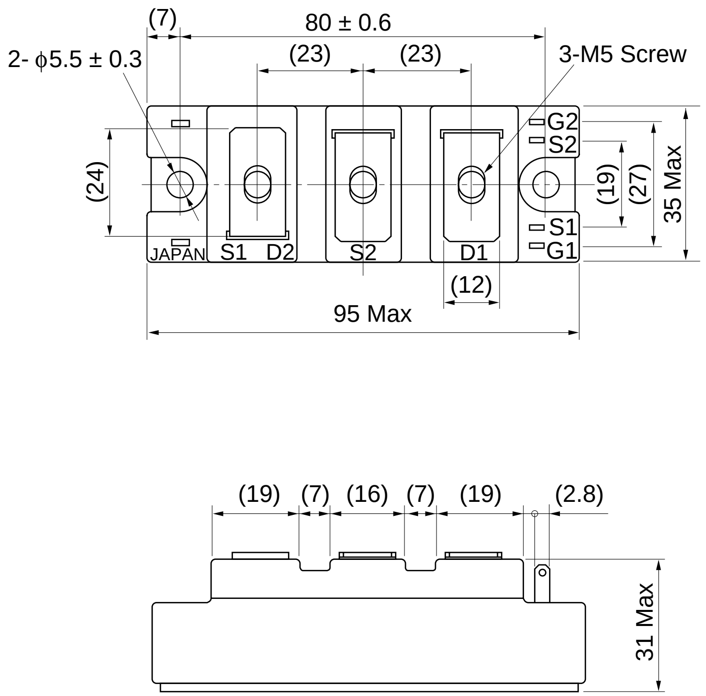


Wave Forms



Package Dimensions

Unit: mm



PM5075J

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

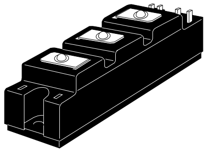
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

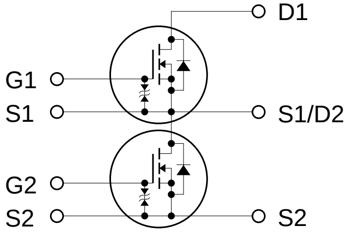
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	500	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	75	A
Drain peak current	$I_{D(peak)}$	180	A
Body-drain diode reverse drain current	I_{DR}	75	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	180	A
Channel dissipation	Pch*1	300	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

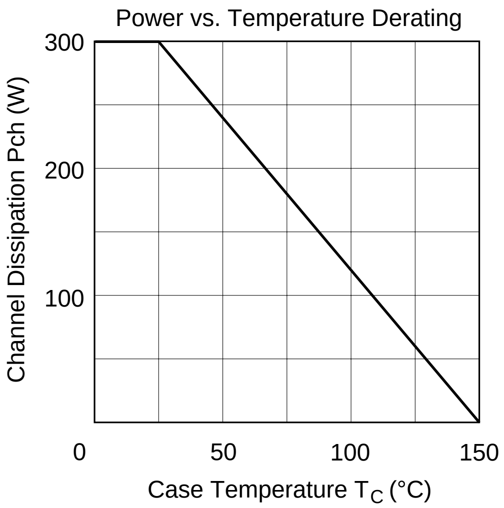
Electrical Characteristics (Ta = 25°C) (Per FET chip)

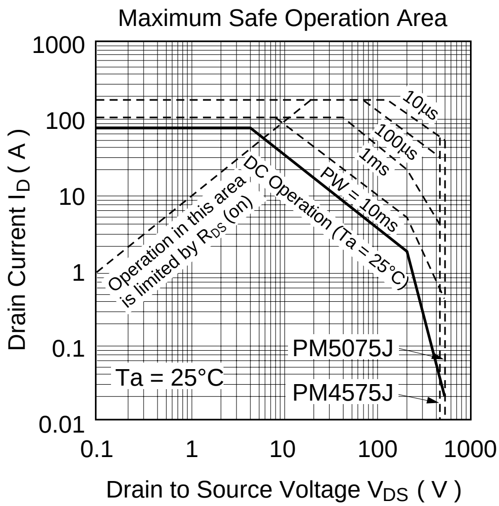
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	500	µA	V_{DS} = 400 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	3.7	4.44	V	I_D = 37 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.10	0.12	Ω	I_D = 37 A, V_{GS} = 10 V*1
Forward transfer admittance	$\vert y_{fs}\vert$	—	45	—	S	I_D = 37 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	9600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	2300	—		
Reverse transfer capacitance	Crss	—	330	—		
Turn-on delay time	$t_{d(on)}$	—	100	—	ns	I_D = 37 A, V_{GS} = 10 V Rg = 50 Ω R_L = 1 Ω
Rise time	t_r	—	310	—		
Turn-off delay time	$t_{d(off)}$	—	550	—		
Fall time	t_f	—	135	—		
Body-drain diode forward voltage	V_{DF}	—	1.8	—	V	I_F = 75 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 75 A, V_{GS} = 0 V di/dt = 100 A/µs

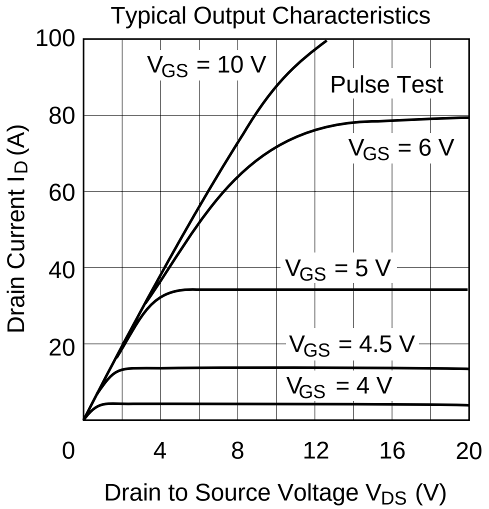
Note: 1. Pulse Test

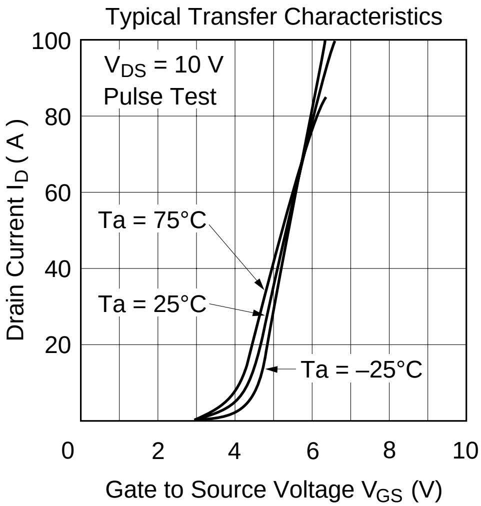
Mechanical characteristics

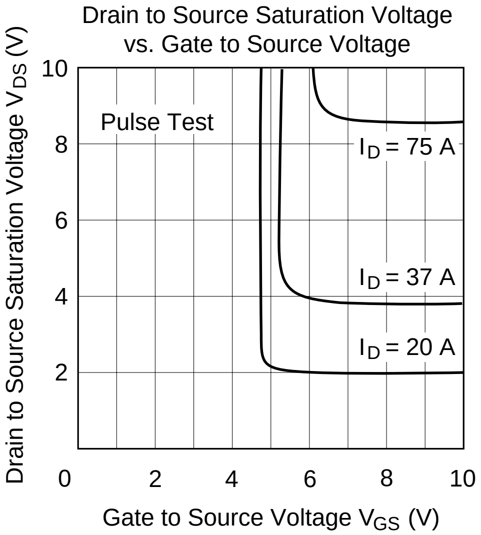
Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	200	g

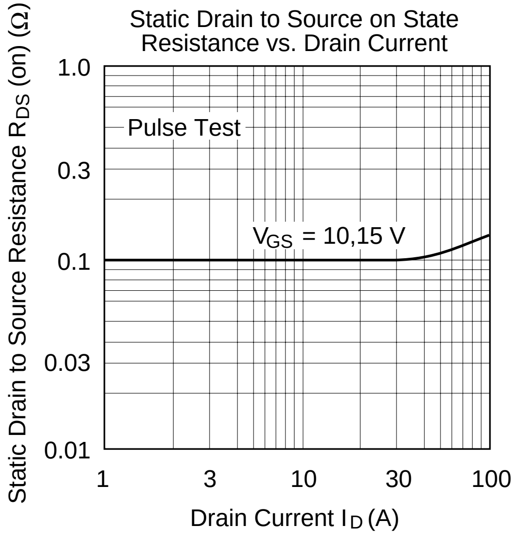

Power vs. Temperature Derating
300
200
100
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

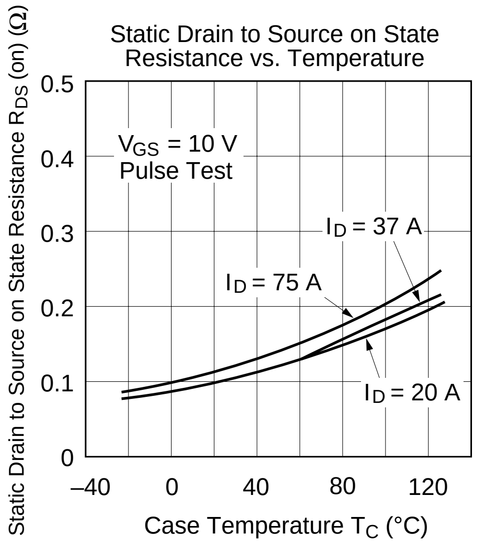

Maximum Safe Operation Area
1000
100
10
1
0.1
0.01
0.1
1
10
100
1000
10μs
100μs
1ms
PW = 10ms
DC Operation (Ta = 25°C)
Operation in this area is limited by R_{DS} (on)
PM5075J
PM4575J
Ta = 25°C
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)

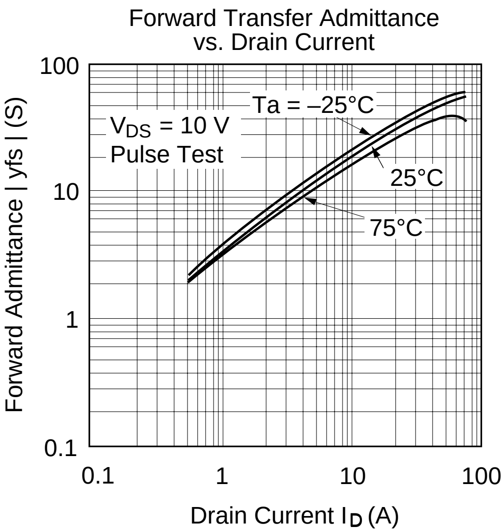

Typical Output Characteristics
100
80
60
40
20
0
4
8
12
16
20
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)


Typical Transfer Characteristics
100
80
60
40
20
0
2
4
6
8
10
V_{DS} = 10 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)

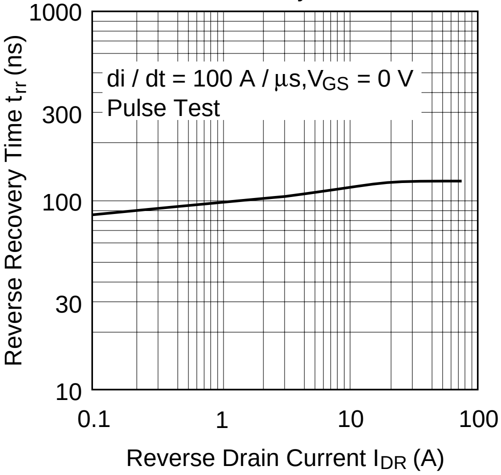

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
Pulse Test
I_D = 75 A
I_D = 37 A
I_D = 20 A
0
2
4
6
8
10


Static Drain to Source on State
Resistance vs. Drain Current
Static Drain to Source Resistance R_{DS} (on) (Ω)
Drain Current I_D (A)
Pulse Test
V_{GS} = 10,15 V
1.0
0.3
0.1
0.03
0.01
1
3
10
30
100

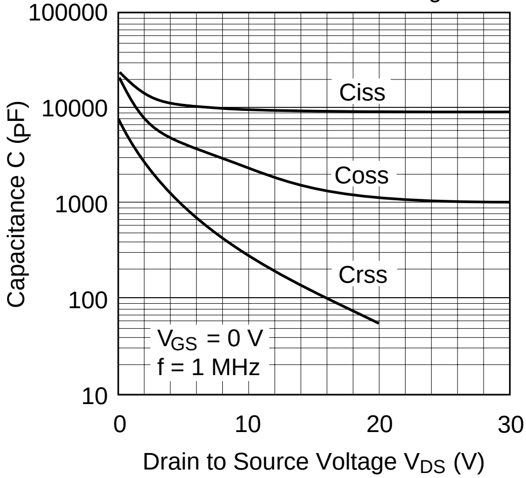

Static Drain to Source on State
Resistance vs. Temperature
Static Drain to Source on State Resistance R_{DS} (on) (Ω)
Case Temperature T_C (°C)
V_{GS} = 10 V
Pulse Test
I_D = 37 A
I_D = 75 A
I_D = 20 A
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120


Forward Transfer Admittance
vs. Drain Current
Forward Admittance | yfs | (S)
Drain Current I_D (A)
V_{DS} = 10 V
Pulse Test
Ta = –25°C
25°C
75°C
100
10
1
0.1
0.1
1
10
100

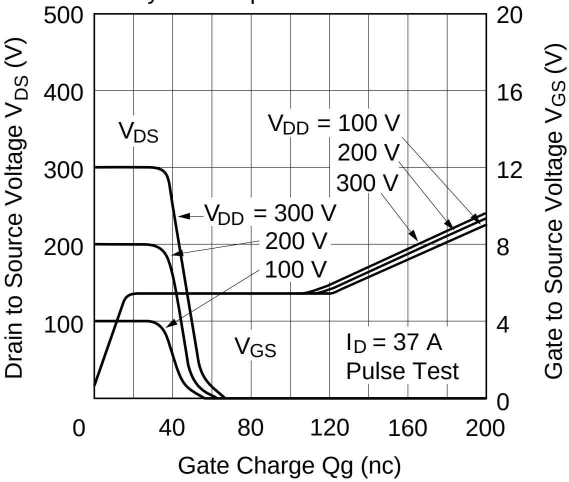
Body to Drain Diode Reverse Recovery Time



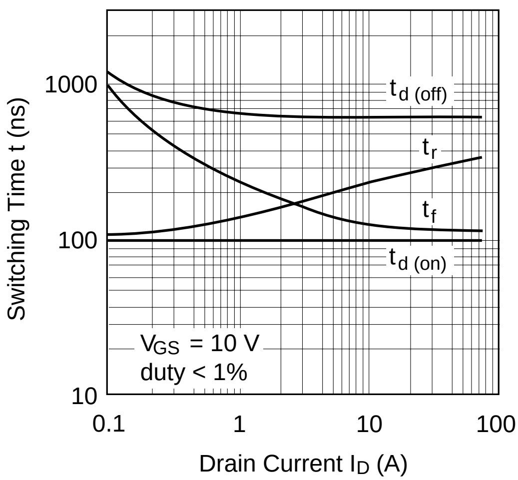
Typical Capacitance vs. Drain to Source Voltage

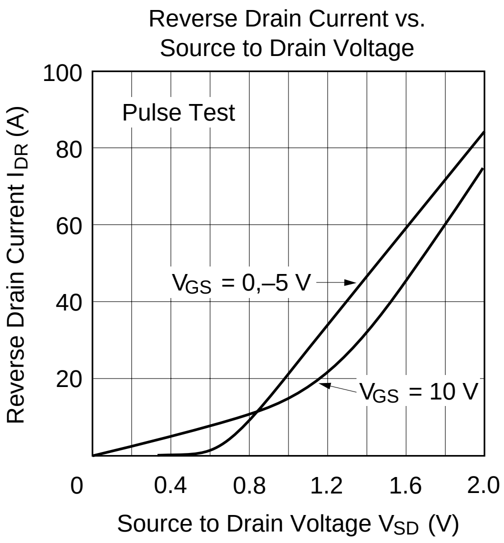


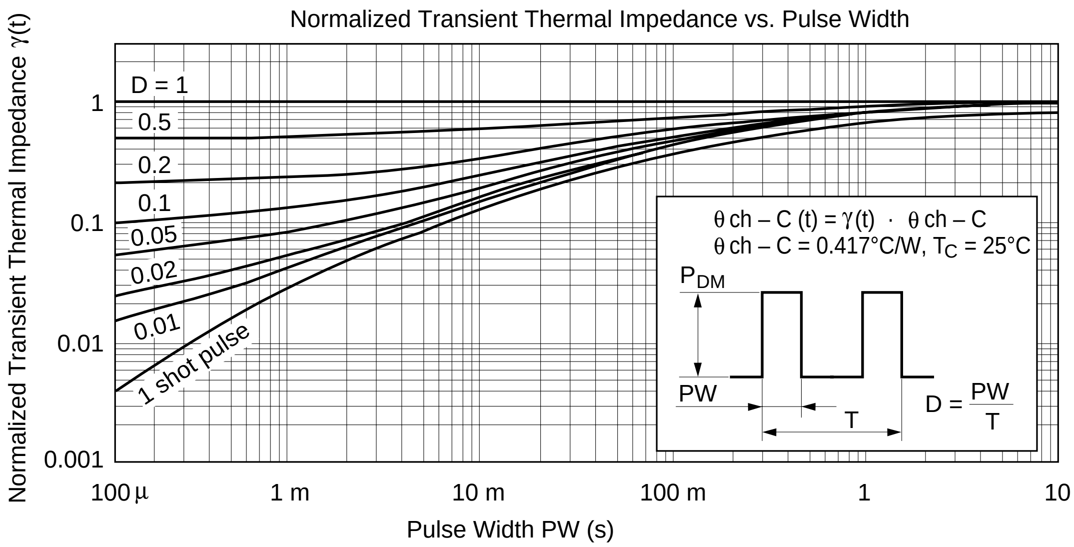
Dynamic Input Characteristics



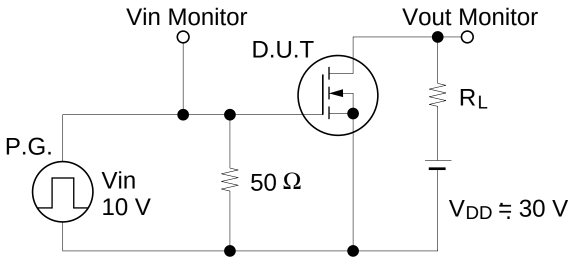
Switching Characteristics



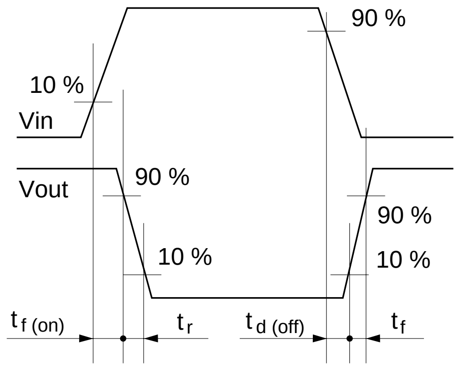

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0,–5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ(t)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
1
0.1
0.01
0.001
$\theta ch - C (t) = \gamma(t) \cdot \theta ch - C$
$\theta ch - C$ = 0.417°C/W, T_C = 25°C
P_{DM}
PW
T
$D = \frac{PW}{T}$
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit

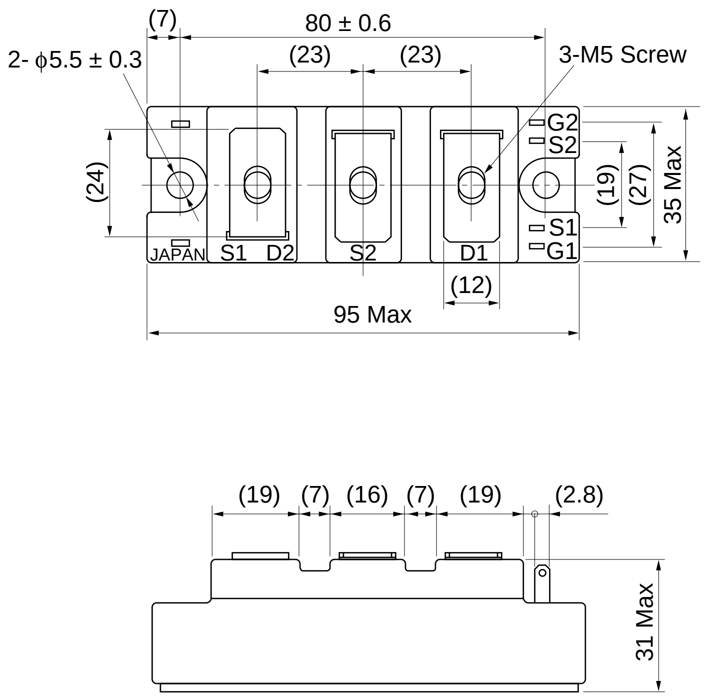


Wave Forms



Package Dimensions

Unit: mm



PM50100K

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

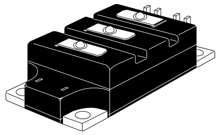
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

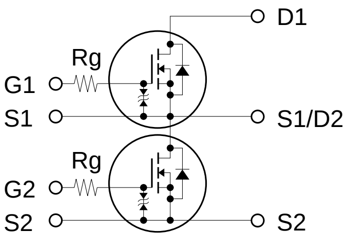
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	500	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	100	A
Drain peak current	$I_{D(peak)}$	240	A
Body-drain diode reverse drain current	I_{DR}	100	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	240	A
Channel dissipation	Pch*1	400	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*2	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

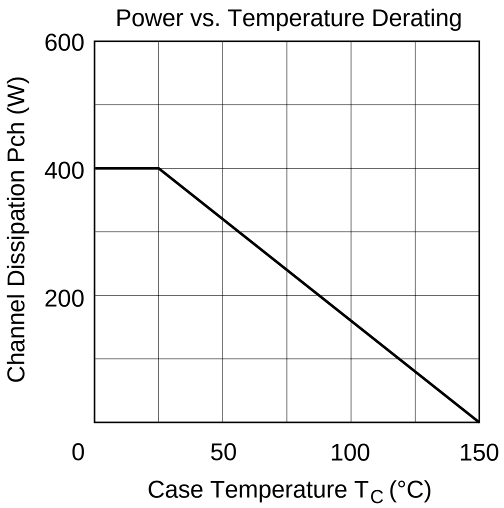
Electrical Characteristics (Ta = 25°C) (Per FET chip)

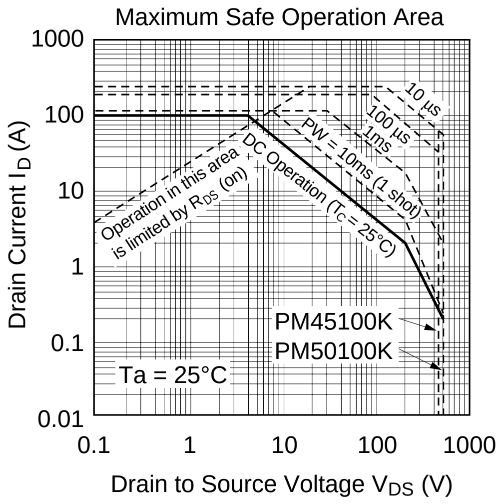
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	1	mA	V_{DS} = 400 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	4.0	5.0	V	I_D = 50 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.08	0.10	Ω	I_D = 50 A, V_{GS} = 10 V*1
Forward transfer admittance	$\|y_{fs}\|$	—	55	—	S	I_D = 50 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	14600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	3500	—		
Reverse transfer capacitance	Crss	—	650	—		
Turn-on delay time	$t_{d(on)}$	—	200	—	ns	I_D = 50 A, V_{GS} = 10 V Rg = 50 Ω R_L = 0.6 Ω
Rise time	t_r	—	690	—		
Turn-off delay time	$t_{d(off)}$	—	760	—		
Fall time	t_f	—	260	—		
Body-drain diode forward voltage	V_{DF}	—	1.6	—	V	I_F = 100 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 100 A, V_{GS} = 0 V di/dt = 100 A/µs

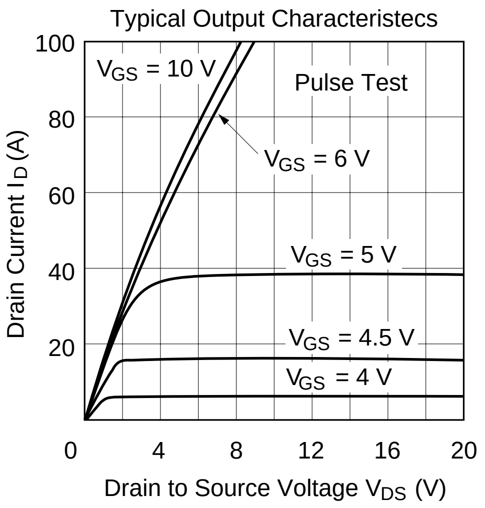
Note: 1. Pulse Test

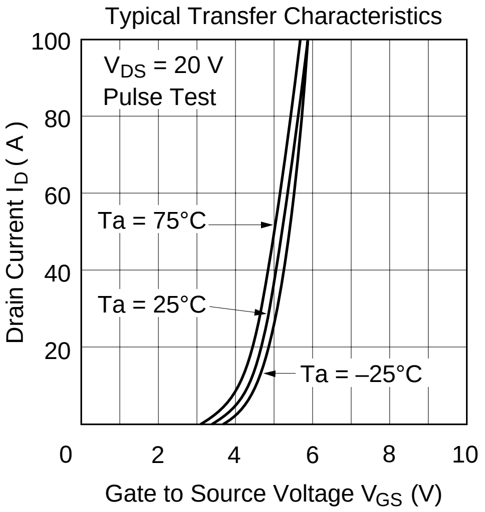
Mechanical characteristics

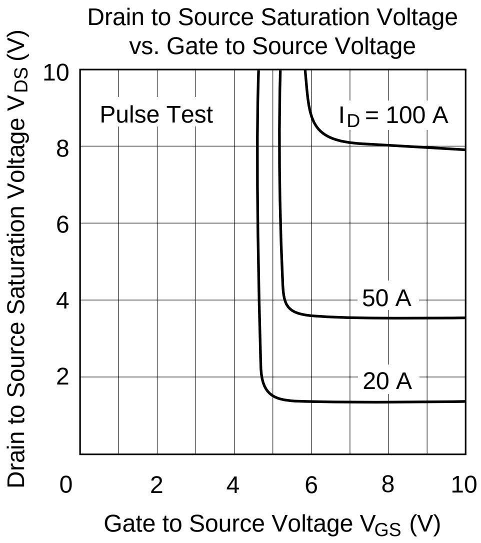
Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	380	g

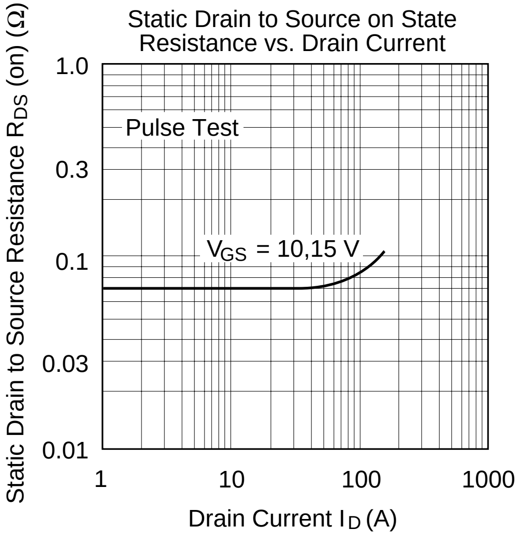

Power vs. Temperature Derating
600
400
200
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C (°C)

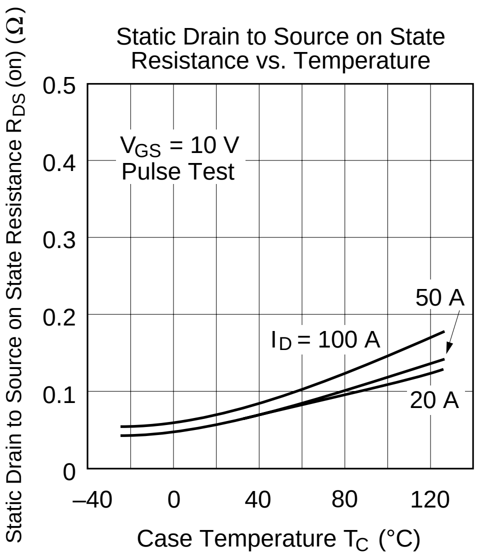

Maximum Safe Operation Area
1000
100
10
1
0.1
0.01
0.1
1
10
100
1000
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10 µs
100 µs
1ms
PW = 10ms (1 shot)
DC Operation (T_C = 25°C)
Operation in this area is limited by R_{DS} (on)
PM45100K
PM50100K
Ta = 25°C

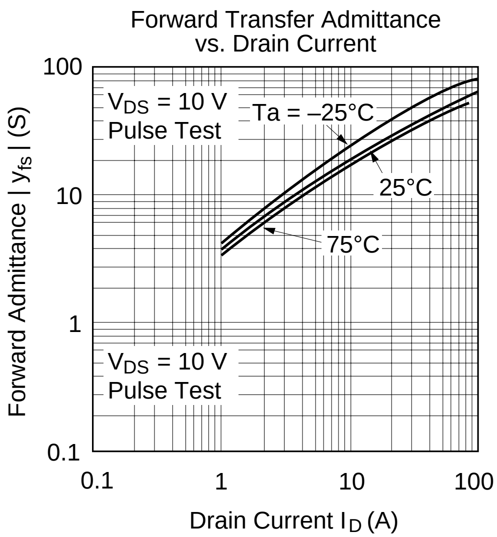

Typical Output Characteristecs
100
80
60
40
20
0
4
8
12
16
20
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V

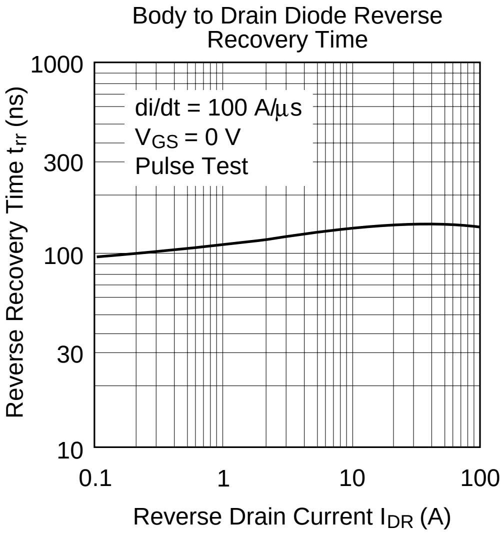

Typical Transfer Characteristics
100
80
60
40
20
0
2
4
6
8
10
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)
V_{DS} = 20 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C

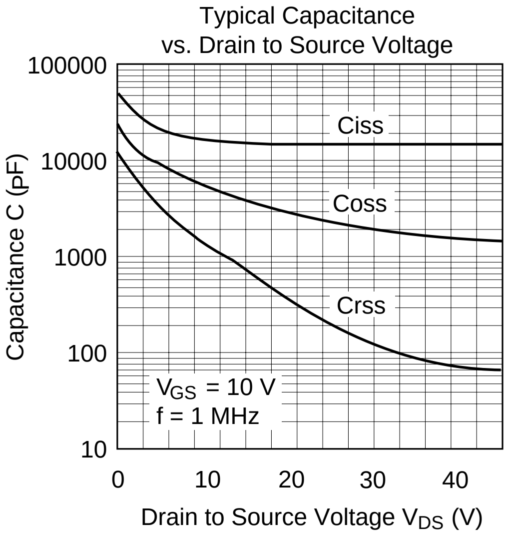

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 100 A
50 A
20 A
Drain to Source Saturation Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
0
2
4
6
8
10

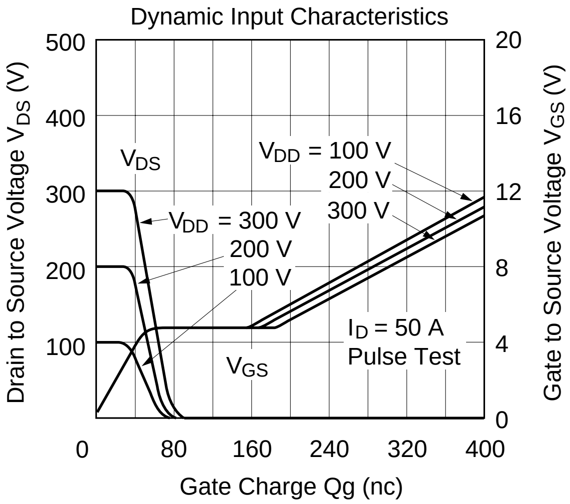

Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_{GS} = 10,15 V
Static Drain to Source Resistance R_{DS} (on) (Ω)
1.0
0.3
0.1
0.03
0.01
1
10
100
1000
Drain Current I_D (A)

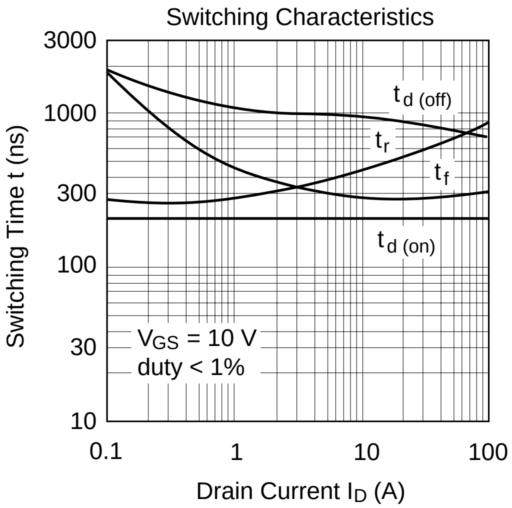

Static Drain to Source on State
Resistance vs. Temperature
V_{GS} = 10 V
Pulse Test
I_D = 100 A
50 A
20 A
Static Drain to Source on State Resistance R_{DS} (on) (Ω)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120
Case Temperature T_C (°C)

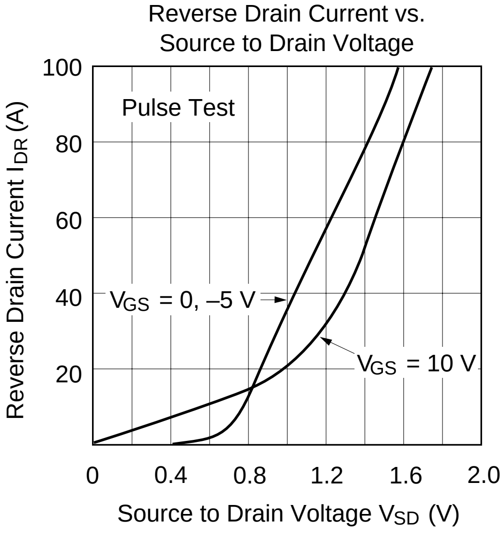

Forward Transfer Admittance
vs. Drain Current
V_{DS} = 10 V
Pulse Test
Ta = –25°C
25°C
75°C
V_{DS} = 10 V
Pulse Test
Forward Admittance | y_{fs} | (S)
100
10
1
0.1
0.1
1
10
100
Drain Current I_D (A)

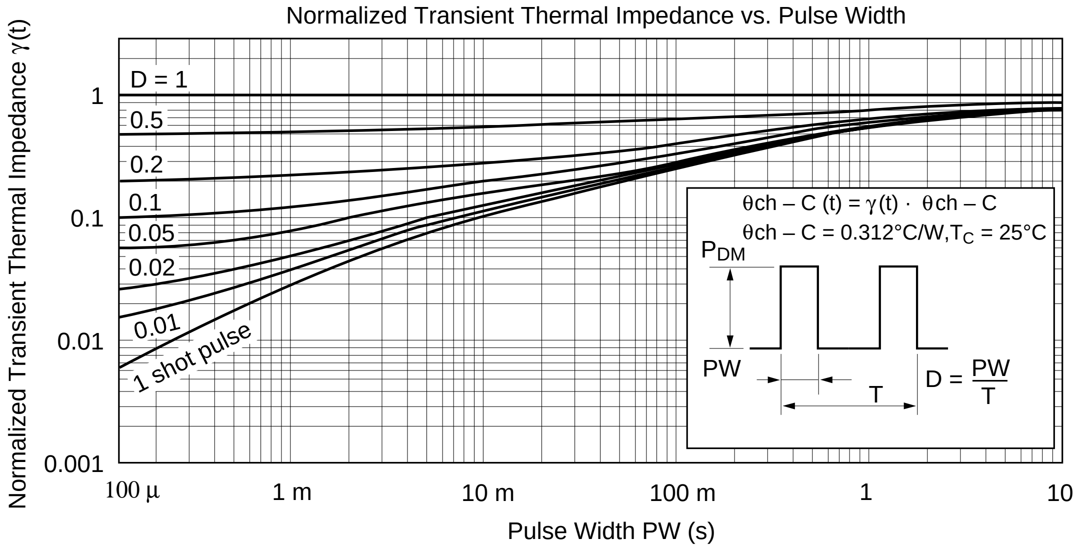

Body to Drain Diode Reverse
Recovery Time
Reverse Recovery Time t_{rr} (ns)
1000
300
100
30
10
di/dt = 100 A/µs
V_{GS} = 0 V
Pulse Test
0.1
1
10
100
Reverse Drain Current I_{DR} (A)


Typical Capacitance
vs. Drain to Source Voltage
Capacitance C (pF)
100000
10000
1000
100
10
Ciss
Coss
Crss
V_{GS} = 10 V
f = 1 MHz
0
10
20
30
40
Drain to Source Voltage V_{DS} (V)

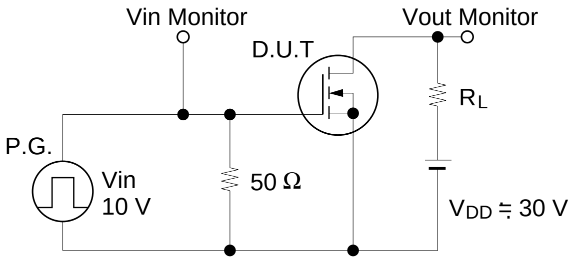

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
500
400
300
200
100
Gate to Source Voltage V_{GS} (V)
20
16
12
8
4
0
V_{DS}
V_{DD} = 100 V
200 V
300 V
V_{DD} = 300 V
200 V
100 V
I_D = 50 A
Pulse Test
V_{GS}
0
80
160
240
320
400
Gate Charge Qg (nc)


Switching Characteristics
Switching Time t (ns)
3000
1000
300
100
30
10
$t_{d\ (off)}$
t_r
t_f
$t_{d\ (on)}$
V_{GS} = 10 V
duty < 1%
0.1
1
10
100
Drain Current I_D (A)

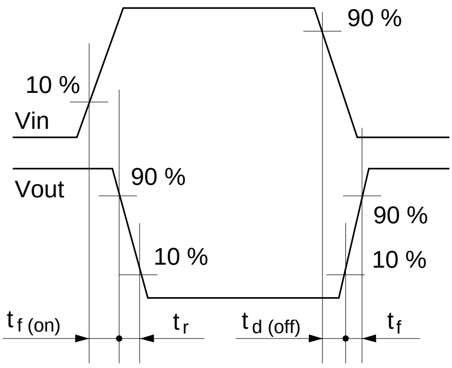

Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
Reverse Drain Current I_{DR} (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γ(t)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
θch – C (t) = γ(t) · θch – C
θch – C = 0.312°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
1
0.1
0.01
0.001
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit

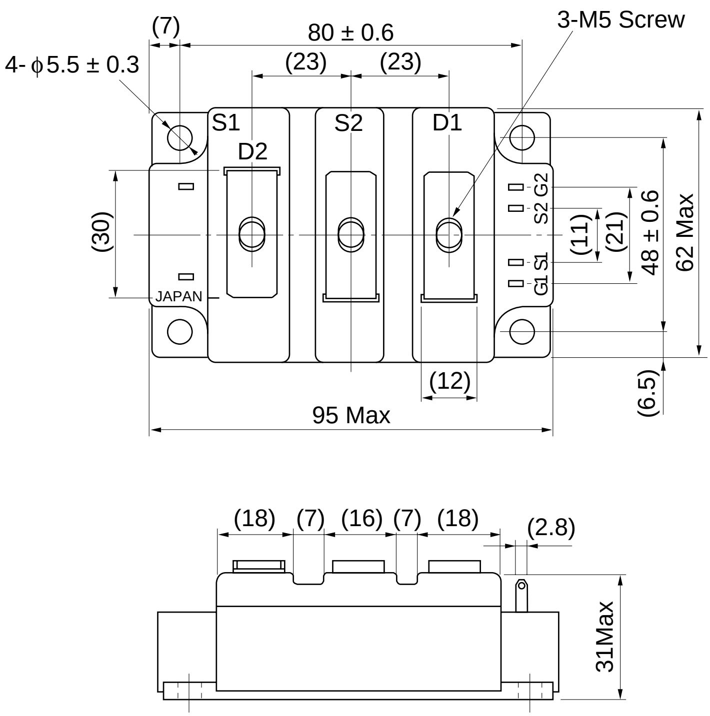


Wave Forms



Package Dimensions

Unit: mm



PM50150K

Silicon N-Channel Power MOS FET Module for High-Speed Power Switching

Features

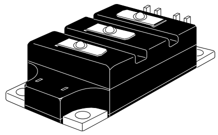
- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

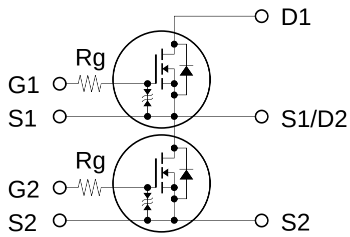
Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	500	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	150	A
Drain peak current	$I_{D(peak)}$	360	A
Body-drain diode reverse drain current	I_{DR}	150	A
Body-drain diode reverse peak current	$I_{DR(peak)}$	360	A
Channel dissipation	Pch[*1]	500	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso[*2]	2000	Vrms

Notes: 1. Value at Ta = 25 °C
2. Base to terminals AC minute

Pin Arrangement





Symbol	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	Power terminal
S2	Source 2	M5 screw	Power terminal
D2	Drain 2	M5 screw	Power terminal
G1	Gate 1	# 110	Signal terminal
S1	Source 1	# 110	Signal terminal
G2	Gate 2	# 110	Signal terminal
S2	Source 2	# 110	Signal terminal

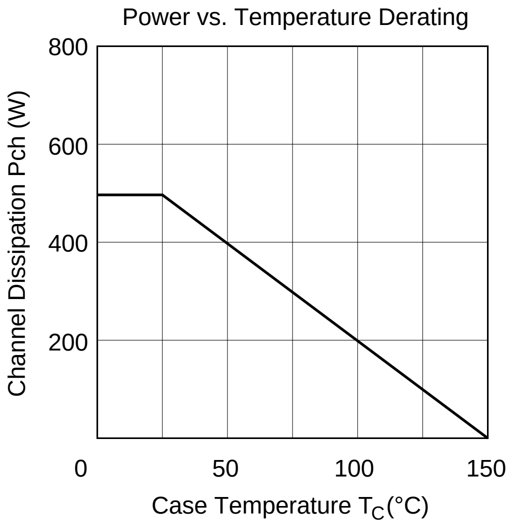
Electrical Characteristics (Ta = 25°C) (Per FET chip)

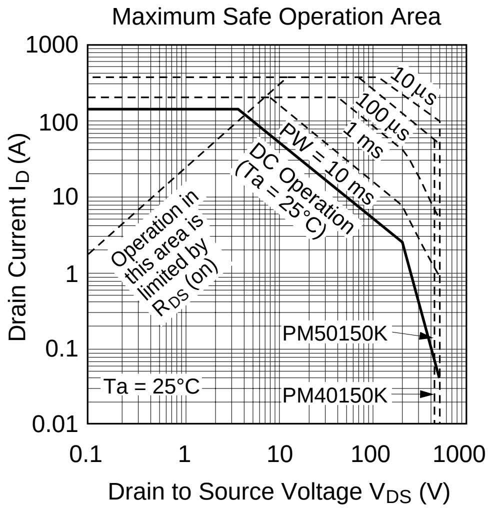
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	I_D = 10 mA, V_{GS}= 0 V
Gate-source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate-source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 μA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	1	mA	V_{DS} = 400 V, V_{GS} = 0 V
Gate-source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain-source saturation voltage	$V_{DS(on)}$	—	4.5	6.0	V	I_D = 75 A, V_{GS} = 10 V*1
Static Drain-source on state resistance	$R_{DS(on)}$	—	0.06	0.08	Ω	I_D = 75 A, V_{GS} = 10 V*1
Forward transfer admittance	$\lvert y_{fs} \rvert$	—	80	—	S	I_D = 75 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	22600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	4600	—		
Reverse transfer capacitance	Crss	—	580	—		
Turn-on delay time	$t_{d(on)}$	—	280	—	ns	I_D = 75 A, V_{GS} = 10 V Rg = 50 Ω R_L = 0.4 Ω
Rise time	t_r	—	820	—		
Turn-off delay time	$t_{d(off)}$	—	1190	—		
Fall time	t_f	—	400	—		
Body-drain diode forward voltage	V_{DF}	—	2.0	—	V	I_F = 150 A, V_{GS} = 0 V
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	I_F = 150 A, V_{GS} = 0 V di/dt = 100 A/μs

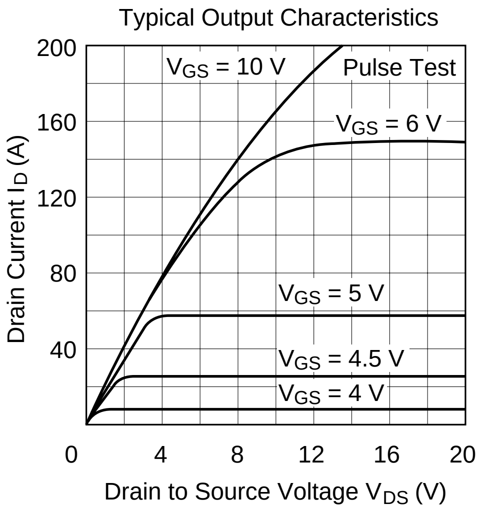
Note: 1. Pulse Test

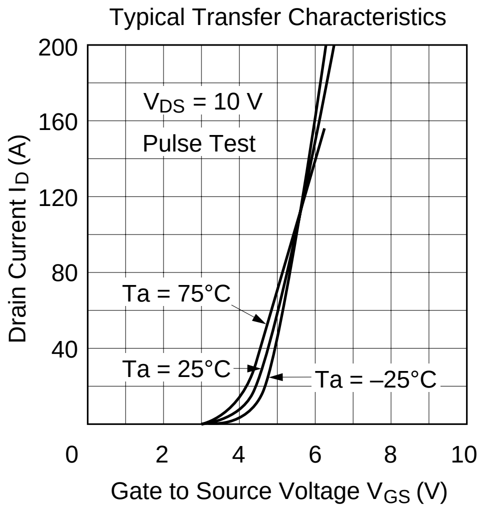
Mechanical characteristics

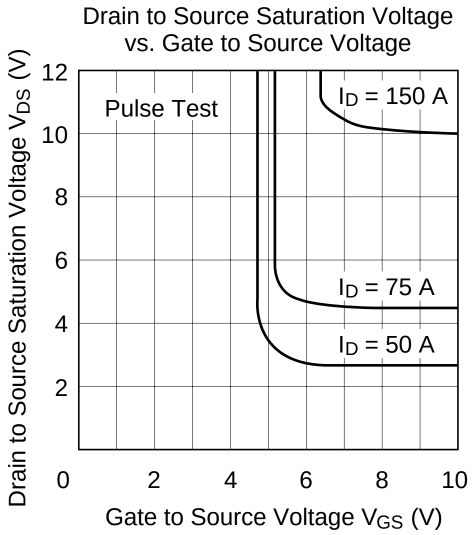
Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	380	g

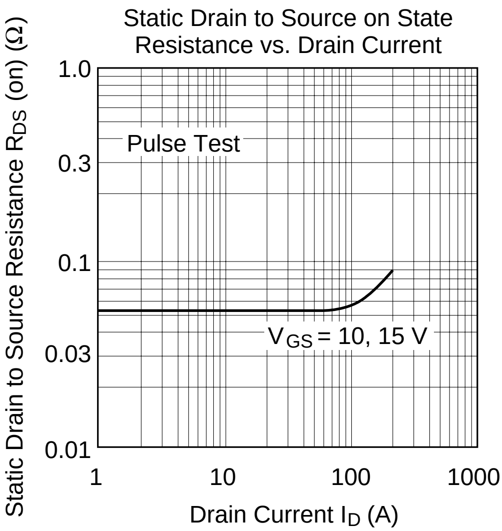

Power vs. Temperature Derating
800
600
400
200
0
50
100
150
Channel Dissipation Pch (W)
Case Temperature T_C(°C)

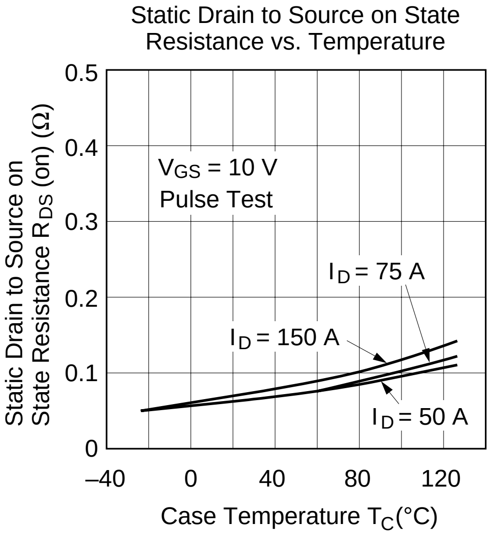

Maximum Safe Operation Area
1000
100
10
1
0.1
0.01
0.1
1
10
100
1000
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10 μs
100 μs
1 ms
PW = 10 ms
DC Operation
(Ta = 25°C)
Operation in this area is limited by R_{DS} (on)
PM50150K
PM40150K
Ta = 25°C

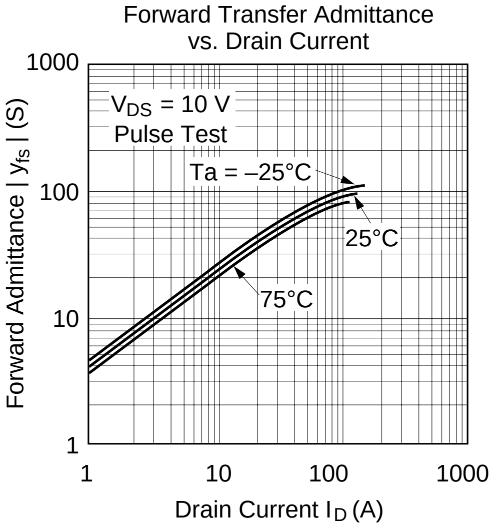

Typical Output Characteristics
200
160
120
80
40
0
4
8
12
16
20
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
V_{GS} = 10 V
Pulse Test
V_{GS} = 6 V
V_{GS} = 5 V
V_{GS} = 4.5 V
V_{GS} = 4 V


Typical Transfer Characteristics
200
160
120
80
40
0
2
4
6
8
10
Drain Current I_D (A)
Gate to Source Voltage V_{GS} (V)
V_{DS} = 10 V
Pulse Test
Ta = 75°C
Ta = 25°C
Ta = –25°C

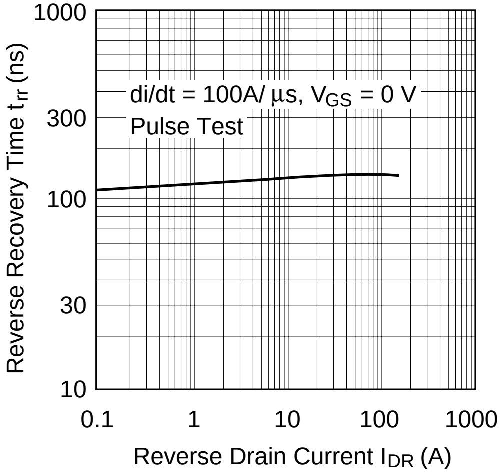

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
I_D = 150 A
I_D = 75 A
I_D = 50 A
Drain to Source Saturation Voltage V_DS (V)
Gate to Source Voltage V_GS (V)
0
2
4
6
8
10
12


Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
V_GS = 10, 15 V
Static Drain to Source Resistance R_DS (on) (Ω)
Drain Current I_D (A)
1.0
0.3
0.1
0.03
0.01
1
10
100
1000

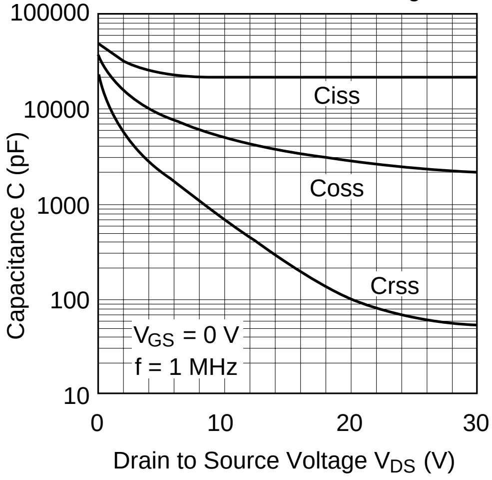

Static Drain to Source on State
Resistance vs. Temperature
V_GS = 10 V
Pulse Test
I_D = 75 A
I_D = 150 A
I_D = 50 A
Static Drain to Source on
State Resistance R_DS (on) (Ω)
Case Temperature T_C(°C)
0.5
0.4
0.3
0.2
0.1
0
–40
0
40
80
120


Forward Transfer Admittance
vs. Drain Current
V_DS = 10 V
Pulse Test
Ta = –25°C
25°C
75°C
Forward Admittance | y_fs | (S)
Drain Current I_D (A)
1000
100
10
1
1
10
100
1000

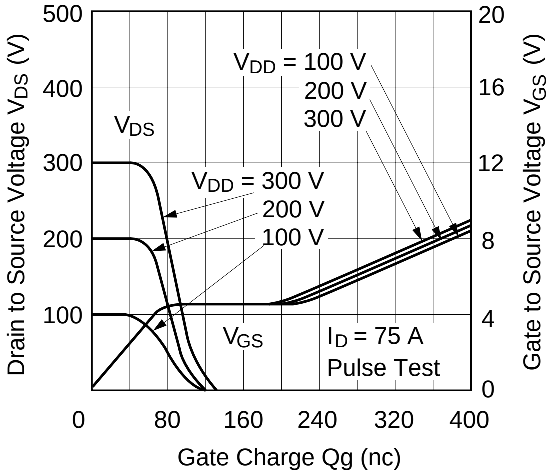
Body to Drain Diode Reverse Recovery Time



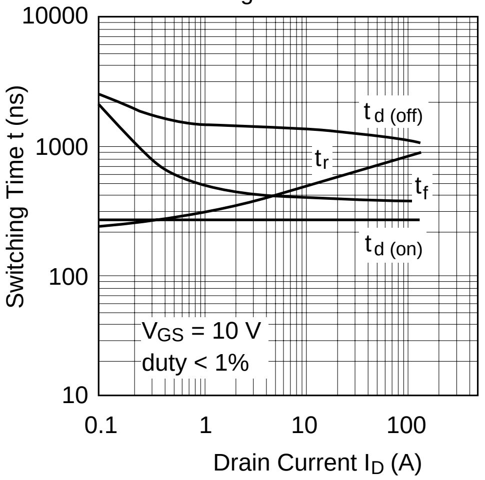
Typical Capacitance vs. Drain to Source Voltage

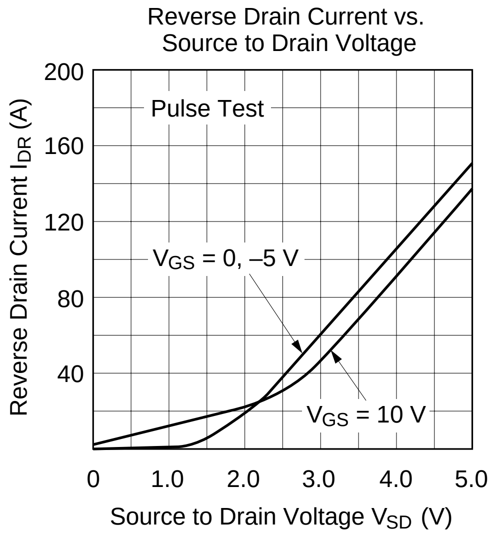


Dynamic Input Characteristics

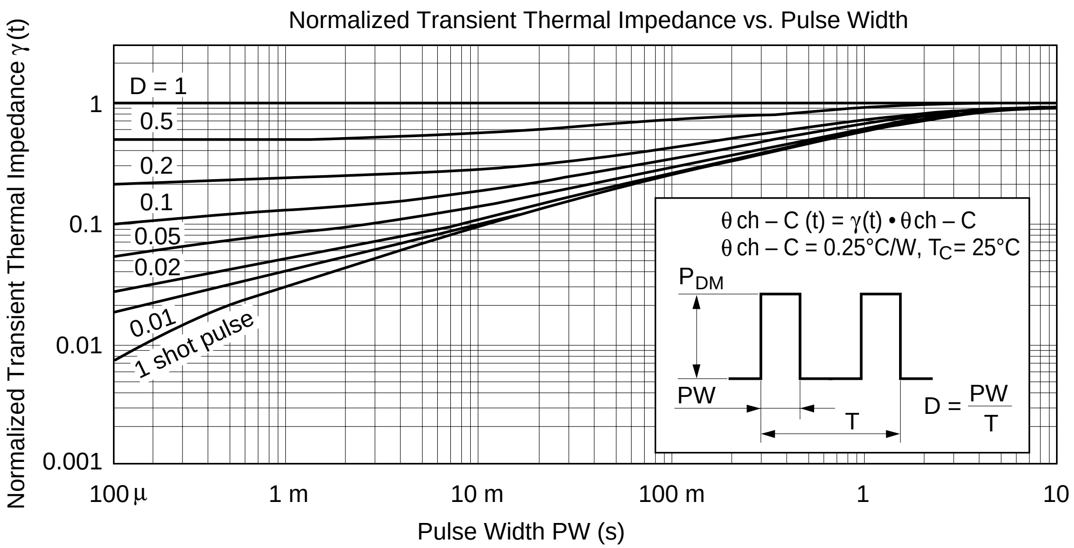


Switching Characteristics



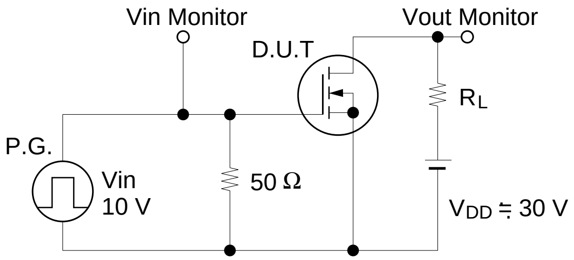


Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
V_{GS} = 0, –5 V
V_{GS} = 10 V
200
160
120
80
40
0
1.0
2.0
3.0
4.0
5.0
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)

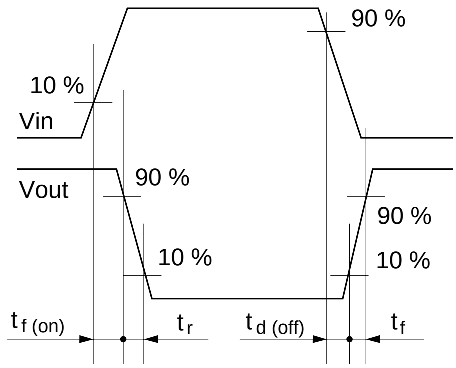


Normalized Transient Thermal Impedance vs. Pulse Width
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 shot pulse
$\theta ch – C (t) = \gamma(t) \bullet \theta ch – C$
$\theta ch – C$ = 0.25°C/W, T_C = 25°C
P_{DM}
PW
T
D = $\frac{PW}{T}$
1
0.1
0.01
0.001
100 µ
1 m
10 m
100 m
1
10
Normalized Transient Thermal Impedance γ(t)
Pulse Width PW (s)

Switching Time Test Circuit



Wave Forms



Package Dimensions

Unit: mm