

EVALUATION KIT  
AVAILABLE

# MAXIM

## +3.6V, 1W Autoramping Power Amplifier for 900MHz Applications

MAX2235

### General Description

The MAX2235 low-voltage, silicon RF power amplifier (PA) is designed for use in the 900MHz frequency band. It operates directly from a single +2.7V to +5.5V supply, making it suitable for use with 3-cell NiCd or 1-cell Li-Ion batteries. The device delivers +30dBm (1W) typical output power from a +3.6V supply or +28dBm from a +2.7V supply.

The MAX2235's gain is adjustable over a 37dB range. A power-control pin controls gain and bias to maintain optimum efficiency, even at lower output power levels, thus extending the operating life of the battery. At +30dBm output power, efficiency is typically 47%. An additional power-saving feature is a shutdown mode that typically reduces supply current below 1 $\mu$ A.

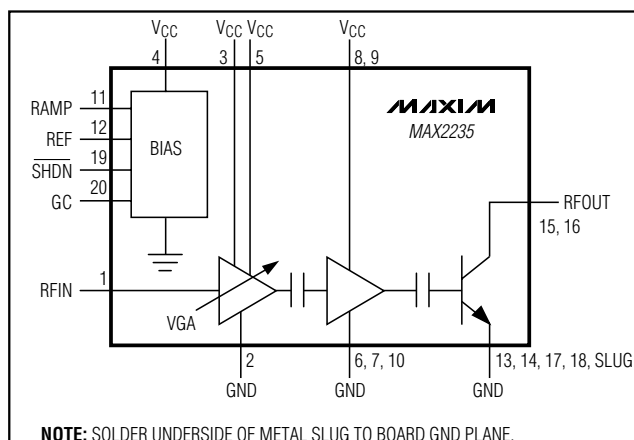
A key feature of this PA is its autoramping capability. During turn-on and turn-off periods, the RF envelope is controlled to approximate a raised cosine on the rising and falling edge, thereby minimizing transient noise and spectral splatter. The ramp time is set by selecting the value of an external capacitor.

The MAX2235 is intended for use in constant envelope applications such as AMPS, two-way paging, or FSK-based communications in the 900MHz ISM band. The device is available in a thermally enhanced 20-pin TSSOP package with a heat slug.

### Applications

900MHz ISM-Band Applications  
Two-Way Pagers  
Analog Cellular Phones  
Microcellular GSM (Power Class 5)  
Wireless Data Networks

### Functional Diagram



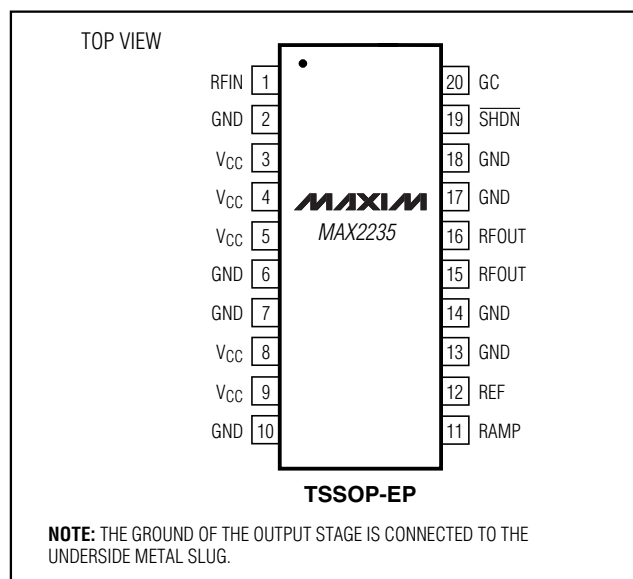
### Features

- ◆ 800MHz to 1000MHz Operation
- ◆ High Output Power at 836MHz
  - +32.5dBm at +5.0V
  - +30dBm at +3.6V
  - +29dBm at +3.0V
  - +28dBm at +2.7V
- ◆ +2.7V to +5.5V Single-Supply Operation
- ◆ Automatic Power-Up/Power-Down Ramp
- ◆ Direct On/Off Keying (OOK) without Intersymbol Interference or VCO Pulling
- ◆ 37dB Power-Control Range
- ◆ 47% Efficiency
- ◆ <1 $\mu$ A Supply Current in Shutdown Mode
- ◆ Small 20-Pin TSSOP Package with Heat Slug

### Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2235EUP	-40°C to +85°C	20 TSSOP-EP

### Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	-0.3V to +6.5V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
SHDN to GND	-0.3V to (V <sub>CC</sub> + 0.3V)	TSSOP (derate 80mW/°C above T <sub>A</sub> = +70°C)
GC to GND	-0.3V to (V <sub>CC</sub> + 0.3V)	Operating Temperature Range
RF Input Power	+13dBm (20mW)	Junction Temperature
Maximum Load Mismatch without Damage, V <sub>CC</sub> = +2.7V to +3.4V, Any Load Phase Angle, Any Duration	20:1	Storage Temperature Range
Maximum Load Mismatch without Damage, V <sub>CC</sub> = +3.4V to +5.5V, Any Load Phase Angle, Any Duration	8:1	Lead Temperature (soldering, 10s)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +2.7V to +5.5V, GC = RAMP = REF = unconnected, no input signal applied, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +3.6V and T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SHDN Logic High	V <sub>IH</sub>	(Note 1)	2.0			V
SHDN Logic Low	V <sub>IL</sub>				0.5	V
Shutdown Supply Current	I <sub>SHDN</sub>	$\overline{\text{SHDN}} = \text{GND}$		0.5	100	μA
		2.7V < V <sub>CC</sub> < 3.4V, $\overline{\text{SHDN}} = \text{GND}$ , T <sub>A</sub> = +55°C			2	
Standby Supply Current	I <sub>STBY</sub>	V <sub>GC</sub> < 0.4			20	mA
$\overline{\text{SHDN}}$ Input Current	I <sub>INSHDN</sub>	V $\overline{\text{SHDN}}$ = 2.0V			0.5	μA
		V $\overline{\text{SHDN}}$ < 0.5V	-0.5		0.5	
GC Input Current	I <sub>GC</sub>	V $\overline{\text{SHDN}}$ < 0.5V, V <sub>GC</sub> < 0.4V	-0.5		0.5	μA
		V $\overline{\text{SHDN}}$ > 2.3V, V <sub>GC</sub> > 0.6V	-10		1.0	
GC Open-Circuit Voltage	V <sub>GCNOM</sub>	(Note 2)	2.0	2.2	2.4	V

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## AC ELECTRICAL CHARACTERISTICS

(MAX2235 Evaluation Kit, GC = unconnected, PRFIN adjusted to give PRFOUT = +30dBm, fRFIN = 836MHz, VCC = VSHDN = +3.6V, TA = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operational Frequency Range (Note 4)	fRFIN		800		1000	MHz
Minimum Output Power	PRFOUT	VCC = 5.0V		32.5		dBm
		VCC = 3.6V		30.3		
		VCC = 3.0V (Note 4)	27.0	28.7		
		VCC = 3.0V, TA = TMIN to TMAX	25.5			
		VCC = 2.7V		28.0		
Power Added Efficiency	PAE			47		%
Average Supply Current	ICC	PRFOUT = +30dBm		610		mA
		PRFIN adjusted to give PRFOUT = +24dBm		315		
		PRFIN = 0dBm, VGC adjusted to give PRFOUT = 24dBm		305		
Power Gain	GP		24	26		dB
Gain-Control Range (Note 5)		0.6V < VGC < 2.3V		37		dB
Auto-Power Ramping-Up Maximum Slope (Note 6)	dP/dt			1.6		mW/μs
Auto-Power Ramping-Down Minimum Slope (Note 6)	dP/dt			-1.3		mW/μs
Input VSWR	VSWR	50Ω source impedance		1.5:1		
Standby Mode Input VSWR Change	ΔVSWR	Input VSWR relative to input impedance in operating mode		1.5:1		
Maximum Nonharmonic Spurious Output Due to Load Mismatch		VCC = 2.7V to 5.5V, 6:1 VSWR at any phase angle		-60		dBc
Noise Power		30kHz BW at offset = 45MHz		-90		dBm
Harmonic Suppression (Note 7)		PRFIN = +7dBm	30	38		dBc
Off-Isolation		PRFIN = 0dBm	VSHDN = 0.5V	40	48	dB
			GC = GND	25	36	

**Note 1:** ≥ +25°C guaranteed by production test, <+25°C guaranteed by design and characterization.

**Note 2:** MAX guaranteed by production test, MIN guaranteed by design and characterization.

**Note 3:** Guaranteed by design and characterization.

**Note 4:** For optimum performance at a given frequency, design the output matching network for maximum output power.

**Note 5:** Gain is monotonic with VGC.

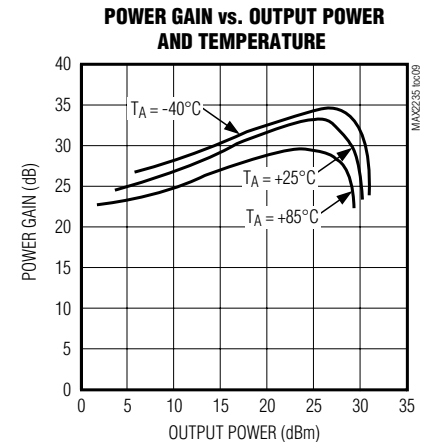
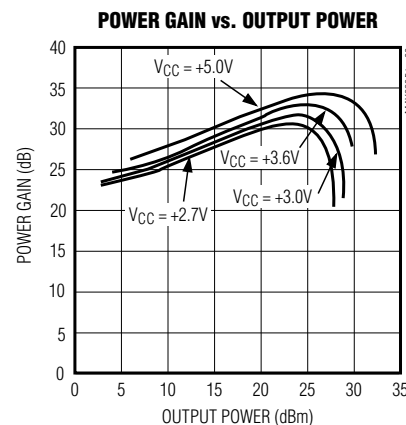
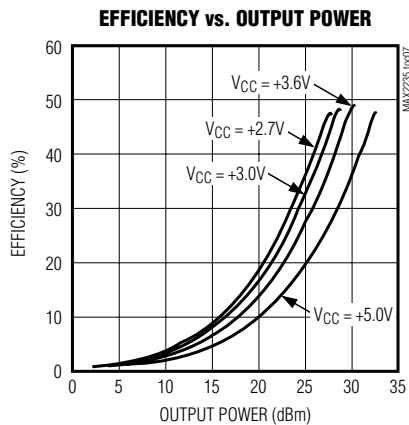
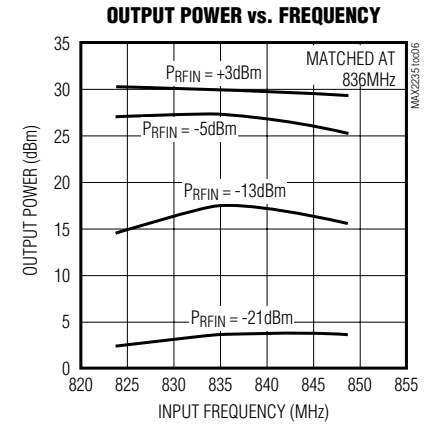
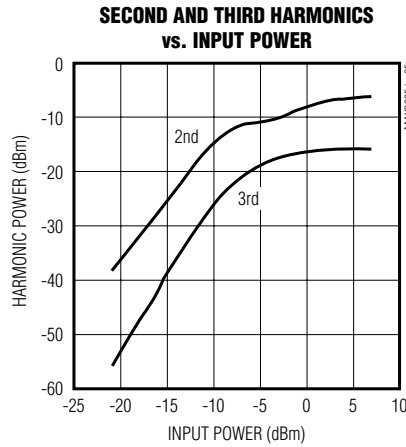
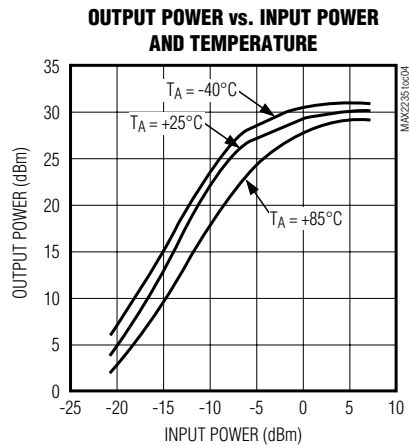
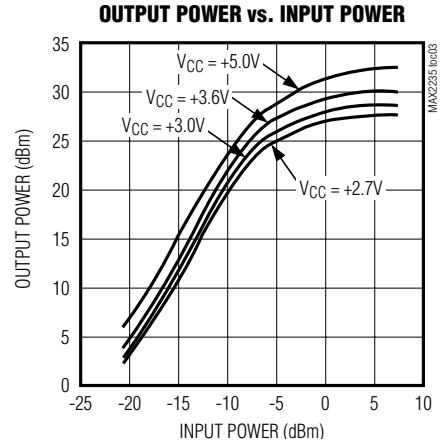
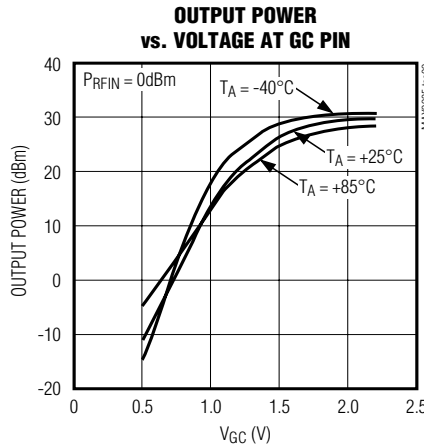
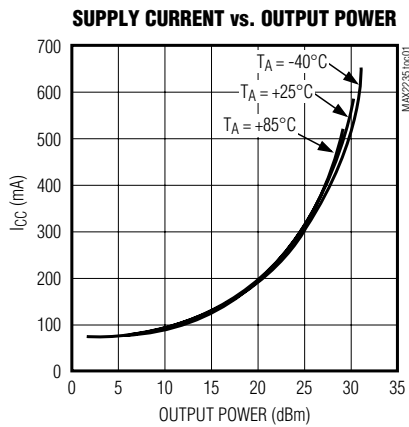
**Note 6:** 0.068μF capacitor from RAMP to REF. Time is measured from SHDN low-to-high transition to +29dBm output power, or from SHDN high-to-low transition to -25dBm output power.

**Note 7:** Harmonics measured on the evaluation kit, which provides some harmonic attenuation in addition to the rejection provided by the IC. The combined suppression is specified.

# +3.6V, 1W Autoramping Power Amplifier for 900MHz Applications

## Typical Operating Characteristics

(MAX2235 Evaluation Kit, GC = unconnected,  $f_{RFIN} = 836\text{MHz}$ ,  $V_{CC} = V_{SHDN} = +3.6\text{V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

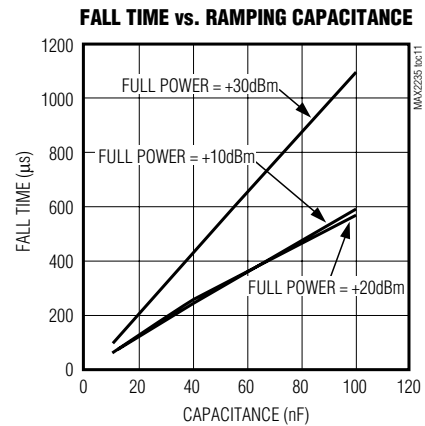
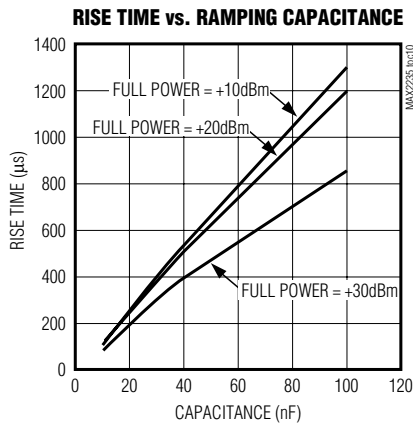


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## Typical Operating Characteristics (continued)

(MAX2235 Evaluation Kit, GC = unconnected,  $f_{RFIN} = 836\text{MHz}$ ,  $V_{CC} = V_{SHDN} = +3.6\text{V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

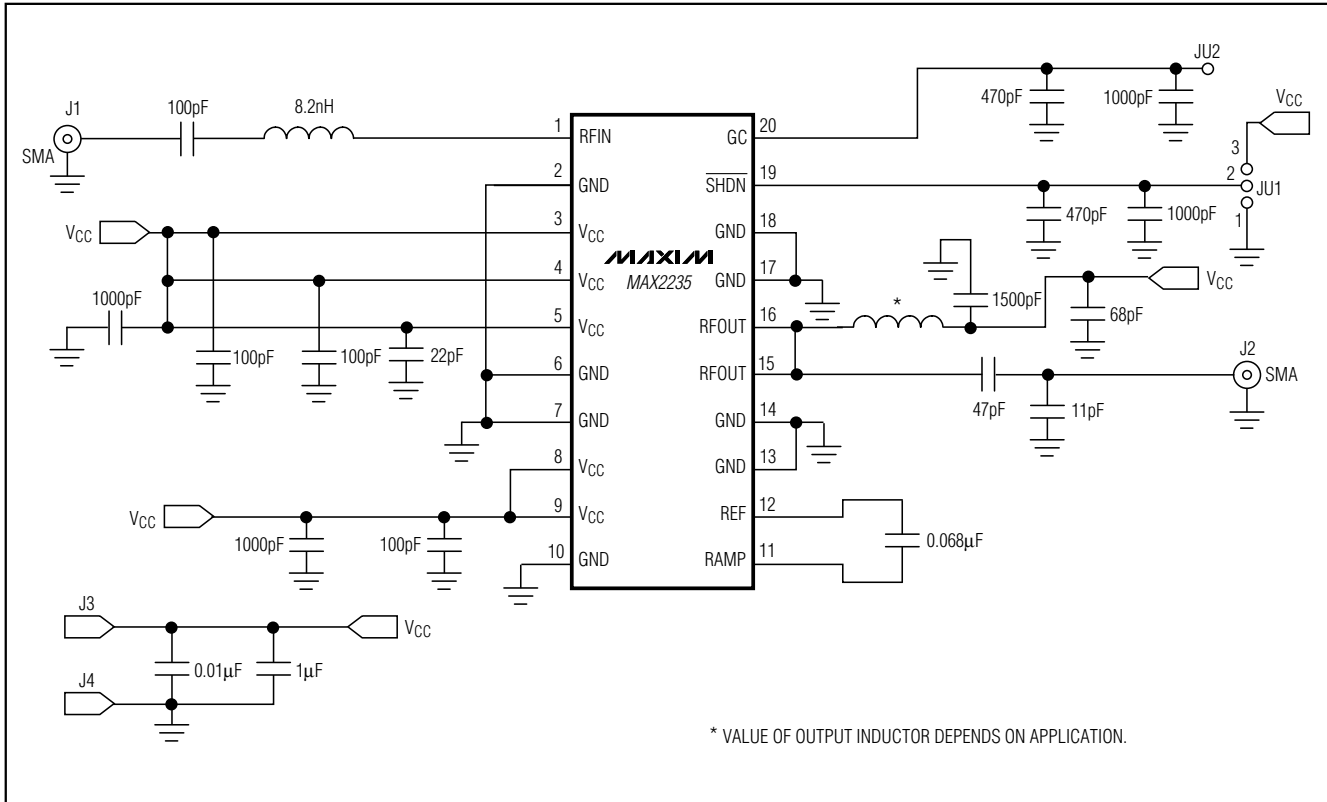


## Pin Description

PIN	NAME	FUNCTION
1	RFIN	RF Input. A DC blocking capacitor in series with RFIN is required. The value of the capacitor depends on the operating frequency.
2	GND	GND connection for the input stage (variable-gain amplifier). Connect to the circuit board ground plane with a <i>separate</i> low-inductance path (via).
3	V <sub>CC</sub>	Supply Voltage Input for the Input Stage. Bypass with its own 100pF low-inductance capacitor to GND.
4	V <sub>CC</sub>	Supply Voltage Input for Bias Circuitry. Bypass with its own 100pF low-inductance capacitor and a 1000pF capacitor to GND, to minimize RF signal coupling into the bias circuits.
5	V <sub>CC</sub>	Supply Voltage Input for the Input Stage. Bypass with its own 22pF low-inductance capacitor to pins 6 and 7.
6, 7, 10	GND	GND Connection for the Second-Stage Amplifier (driver). Connect to the circuit board ground plane with a <i>separate</i> low-inductance path (via).
8	V <sub>CC</sub>	Supply Voltage Input for the Second Stage. Bypass with its own 220pF and 1000pF low-inductance capacitors to GND.
9	V <sub>CC</sub>	Supply Voltage Input for the Second Stage. Connect to pin 8.
11	RAMP	Power Ramp Pin. Connect a capacitor between RAMP and REF to provide a gradual linear power-up/down ramp. See <i>Detailed Description</i> .
12	REF	Reference Voltage for RAMP Capacitor. The reference is internally set to 1.9V.
13, 14, 17, 18, SLUG	GND	GND Connection for the Power Stage. Solder the slug to the circuit board ground plane. Connect pins 13, 14, 17, and 18 to the slug with a straight board trace under the chip.
15	RFOUT	Power Amplifier Output. See <i>Typical Operating Circuit</i> for an example of a matching network, which provides optimal output power at 836MHz. Connect to pin 16.
16	RFOUT	Power Amplifier Output. Connect to pin 15.
19	SHDN	Shutdown Pin. Drive SHDN low to turn the device off. Drive above 2.0V to turn the device on. Drive $V_{SHDN} > 2.0\text{V}$ and $V_{GC} < 0.4\text{V}$ for standby mode.
20	GC	Gain-Control Pin. Apply $V_{GC}$ between 0.6V and 2.3V to control the output power with a monotonic dB/V relationship. See the <i>Typical Operating Characteristics</i> for a typical relationship.

# +3.6V, 1W Autoramping Power Amplifier for 900MHz Applications

## Typical Operating Circuit



### Detailed Description

The MAX2235 power amplifier (PA) operates over a wide frequency range of 800MHz to 1000MHz. The signal path consists of three stages: the input stage, the driver stage, and the power stage. There are matching circuits between the first and second stages, and between the second and third stages. The bias circuits process external commands to control the device's power-up/down and the gain of the PA.

#### Input Stage

The first stage is a variable-gain amplifier with 37dB gain-control range. The input transistor acts as a transconductor with constant bias current. Gain control is achieved by steering the signal current from the input transistor to the first output matching network (to drive the second stage) or to a separate supply pin. This

stage operates in class A and remains on in standby mode to ensure that the VSWR at the input does not vary more than 1.5:1 compared with normal operation. The input stage typically requires an external inductor to achieve an optimum input VSWR.

#### Second Stage (Driver)

The driver produces a signal large enough to drive the power stage into saturation. The driver stage operates in Class C and is off during standby.

#### Second- and Third-Stage Matching

The interstage matching networks provide optimal loading and power transfer. The circuits are on-chip to save board space. The bandwidths of the matching networks allow the PA to operate over a wide frequency range.

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## Third Stage (Power Stage)

This last stage delivers 30dBm to a 50Ω load. It operates in Class E to achieve a high power-added efficiency (PAE). Proper output matching is required for optimal output power. The output of the power stage requires a low-series-resistance pull-up inductor with a minimum current rating of 1.5A. See the *Typical Operating Circuit* for an example of an output matching circuit.

## Biasing and Power Control

$\overline{\text{SHDN}}$ , GC, RAMP, and REF are bias and power-control pins. Drive  $\overline{\text{SHDN}}$  below 0.5V to turn off the entire chip, and drive  $\overline{\text{SHDN}}$  above 2.0V to turn on the device. When  $\overline{\text{SHDN}}$  is high, a  $V_{\text{GC}}$  from 0.6V to 2.3V continuously controls the gain in the first stage (VGA) and the output power.

Drive GC below 0.4V to put the device in standby mode with only the first stage on. If GC is unconnected and  $V_{\overline{\text{SHDN}}} > 2.0\text{V}$ , the device is set to maximum gain. Table 1 summarizes these operating modes.

## Power Ramping Control

A capacitor connected between RAMP and REF controls the output power rise/fall time to reduce transient noise when  $\overline{\text{SHDN}}$  turns the device on and off. Because the ramp is approximately a raised cosine, this device can be used in direct On/Off Keying (OOK) applications with minimum intersymbol interference. The value of the ramping capacitor is determined from the Rise/Fall Time vs. Ramping Capacitance curves in the *Typical Operating Characteristics*.

Table 1. Operating Modes

$\overline{\text{SHDN}}$	GC	MODE
>2.0V	>0.6V	On
>2.0V	<0.4V	Standby
<0.5V	Don't care	Shutdown

## Board Assembly Precaution

Solder the underside metal slug evenly to the board ground plane for optimal performance. Fill all vias in the area under the slug. For maximum power gain and saturated output power, ensure that the entire slug makes contact with the board ground.

## Chip Information

TRANSISTOR COUNT: 668

# +3.6V, 1W Autoramping Power Amplifier for 900MHz Applications

## Package Information

**COMMON DIMENSIONS**

Symbol	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	—	.043
A <sub>1</sub>	0.05	0.15	.002	.006
A <sub>2</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c <sub>1</sub>	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
alpha	0°	8°	0°	8°

JEDEC	N	VARIATIONS				
		MILLIMETERS		INCHES		
		MIN.	MAX.	MIN.	MAX.	
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

**NOTES:**  
 1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.  
 3. CONTROLLING DIMENSION: MILLIMETER.  
 4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.  
 5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.  
 6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

TSSOP-EP

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