

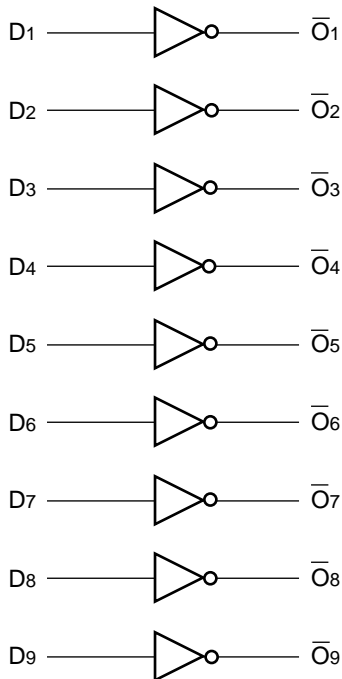
**FEATURES**

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than Fairchild 300K at lower power
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

**DESCRIPTION**

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

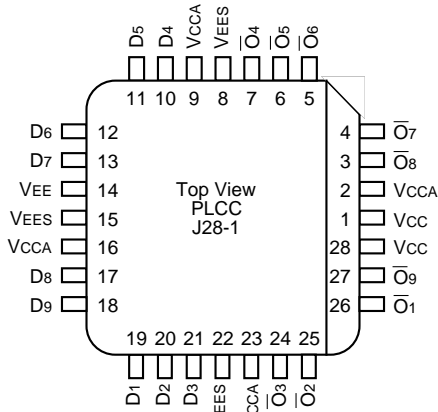
**BLOCK DIAGRAM**



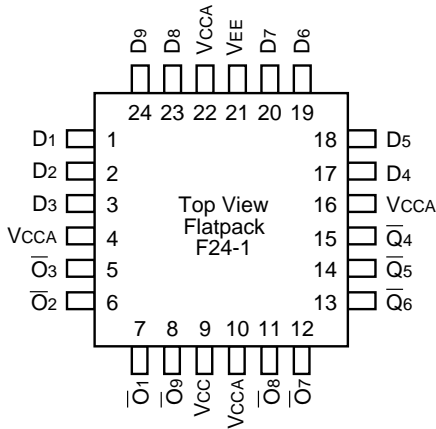
**PIN NAMES**

Pin	Function
D1 – D9	Data Inputs
$\bar{Q}_1 – \bar{Q}_9$	Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**



**24-Pin Cerpack (F24-1)**

**Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S321FC	F24-1	Commercial	SY100S321FC	Sn-Pb
SY100S321FCTR <sup>(1)</sup>	F24-1	Commercial	SY100S321FC	Sn-Pb
SY100S321JC	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JZ <sup>(2)</sup>	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S321JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current	—	—	200	μA	$V_{IN} = V_{IH} (Max.)$
I <sub>EE</sub>	Power Supply Current	-55	-41	-25	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS****CERPACK**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup> Data to Output	300	800	300	800	300	800	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time <sup>(1)</sup> 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>S, G-G</sub>	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

**NOTE:**

- Reference figures 1 and 2

**PLCC**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay <sup>(1)</sup> Data to Output	300	700	300	700	300	700	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time <sup>(1)</sup> 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>S, G-G</sub>	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

**NOTE:**

- Reference figures 1 and 2

**TEST CIRCUITRY<sup>(1)</sup>**

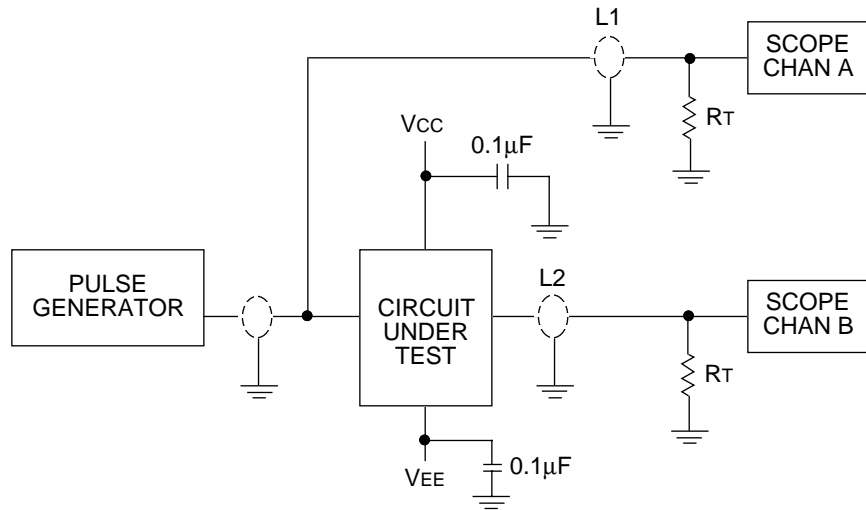


Figure 1. AC Test Circuit

**Note:**

- 1. VCC, VCCA = +2V, VEE = -2.5V.
- L1 and L2 = equal length 50Ω impedance lines.
- RT = 50Ω terminator internal to scope.
- Decoupling 0.1µF from GND to VCC and VEE.
- All unused outputs are loaded with 50Ω to GND.
- CL = Fixture and stray capacitance ≤ 3pF.

**SWITCHING WAVEFORMS**

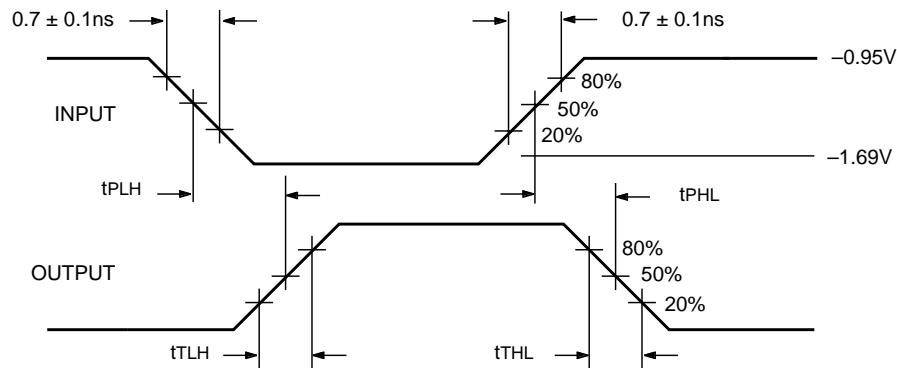
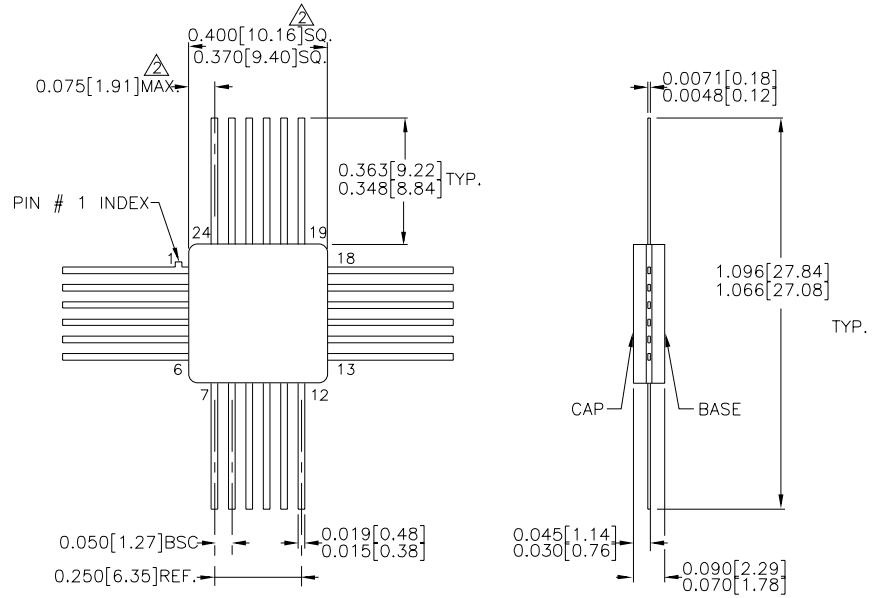


Figure 2. Propagation Delay and Transition Times

**Note:**

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

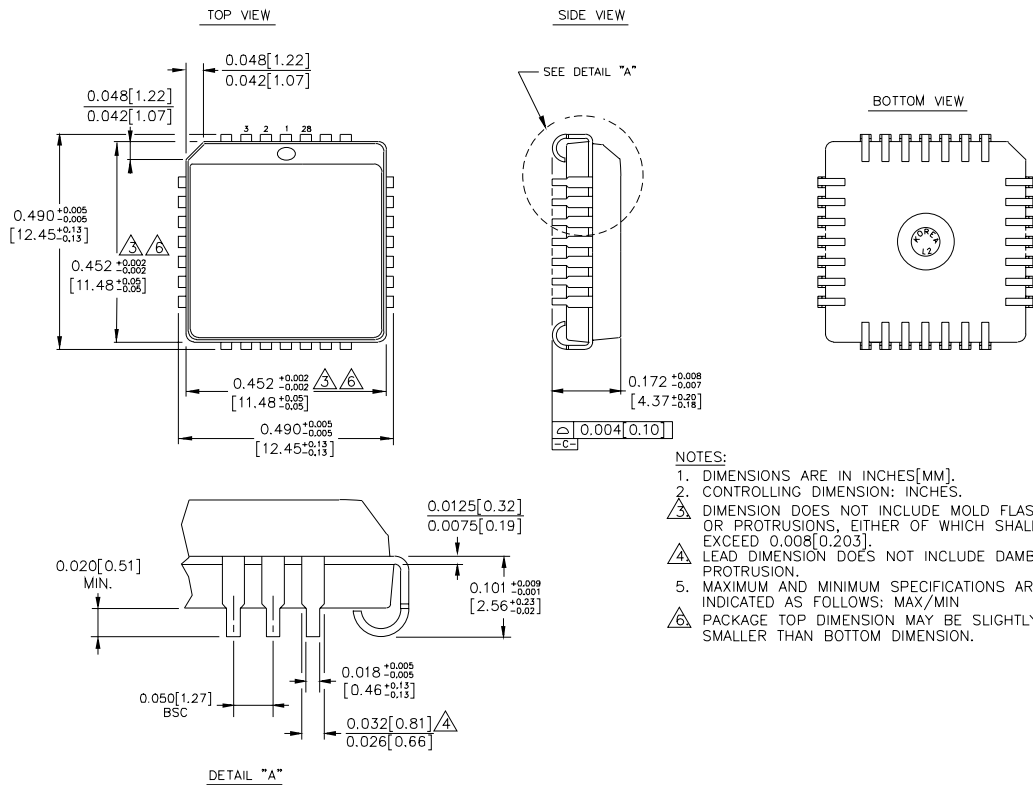
**24-PIN CERPACK (F24-1)**



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

**28-PIN PLCC (J28-1)**



Rev. 03

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