

FEATURES

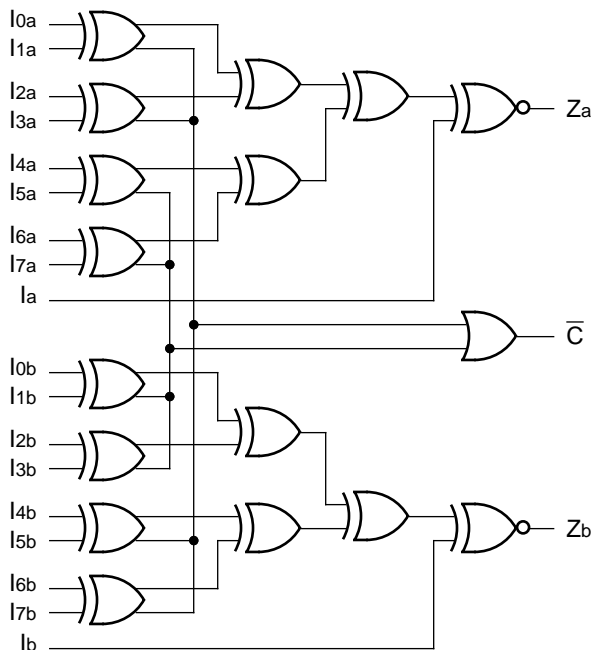
- Max. propagation delay of 2200ps
- IEE min. of -70mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 15% faster than Fairchild 300K
- Approximately 30% lower power than Fairchild 300K
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPAC and 28-pin PLCC packages

DESCRIPTION

The SY100S360 is a dual parity checker/generator and is designed for use in high-performance ECL systems. The inputs are segmented into two groups of nine inputs each and the parity output is at a logic LOW when an even number of inputs are at a logic HIGH. In each group, one of the nine inputs (Ia, Ib) has a shorter propagation delay and, therefore, is ideal as the expansion input for parity generation of wider data.

A Compare output (C) is also provided which allows comparison of two 8-bit words. A logic LOW on the C output indicates a match. The inputs on this device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



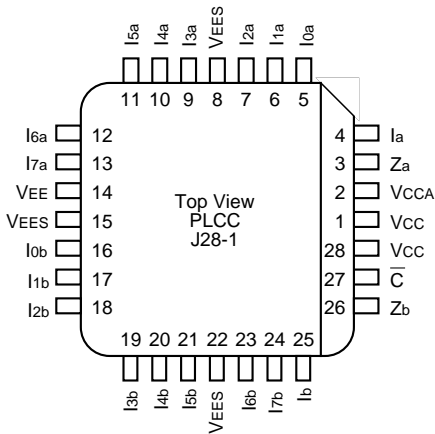
PACKAGE/ORDERING INFORMATION

Ordering Information

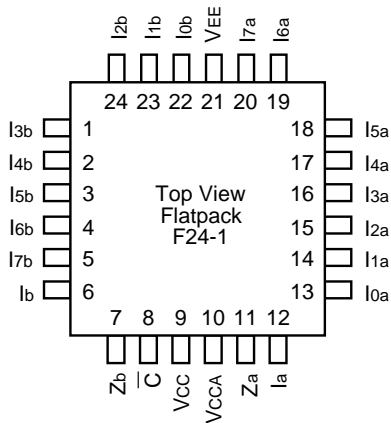
Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S360FC	F24-1	Commercial	SY100S360FC	Sn-Pb
SY100S360FCTR ⁽¹⁾	F24-1	Commercial	SY100S360FC	Sn-Pb
SY100S360JC	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JCTR ⁽¹⁾	J28-1	Commercial	SY100S360JC	Sn-Pb
SY100S360JZ ⁽²⁾	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S360JZTR ^(1, 2)	J28-1	Commercial	SY100S360JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

PIN NAMES

Pin	Function
Ia, Ib, Ina, Inb	Data Inputs (n = 1...7)
Za – Zb	Parity Odd Outputs
\bar{C}	Compare Output
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

TRUTH TABLE⁽¹⁾

Sum of High Inputs	Output Z
Even	HIGH
Odd	LOW

Note:

1. Comparator Function:

$$\bar{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current Ia, Ib Ina, Inb	—	—	300 200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-70	-45	-30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

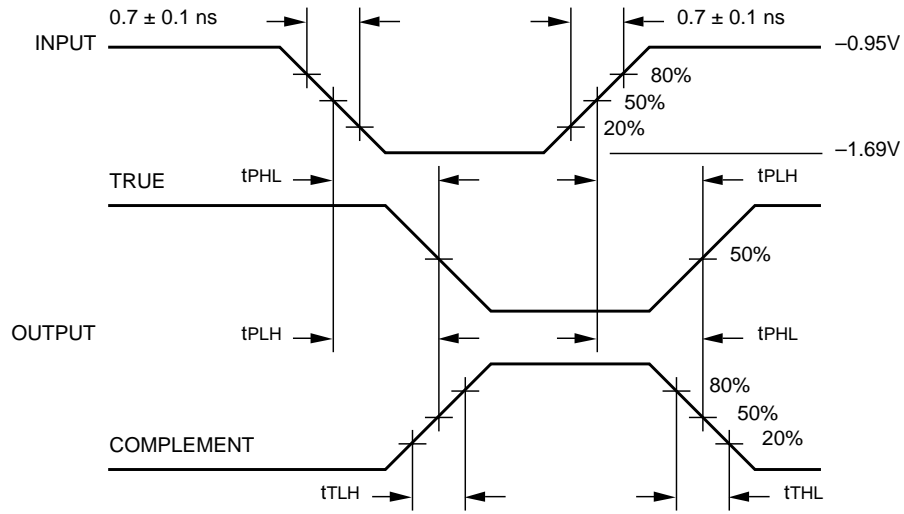
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Ina, Inb to Za, Zb	500	2300	500	2300	500	2300	ps	
t _{PLH} t _{PHL}	Propagation Delay Ina, Inb to \bar{C}	500	1800	500	1800	500	1800	ps	
t _{PLH} t _{PHL}	Propagation Delay Ia, Ib to Za, Zb	300	1000	300	1000	300	1000	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Ina, Inb to Za, Zb	500	2200	500	2200	500	2200	ps	
t _{PLH} t _{PHL}	Propagation Delay Ina, Inb to \bar{C}	500	1700	500	1700	500	1700	ps	
t _{PLH} t _{PHL}	Propagation Delay Ia, Ib to Za, Zb	300	900	300	900	300	900	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

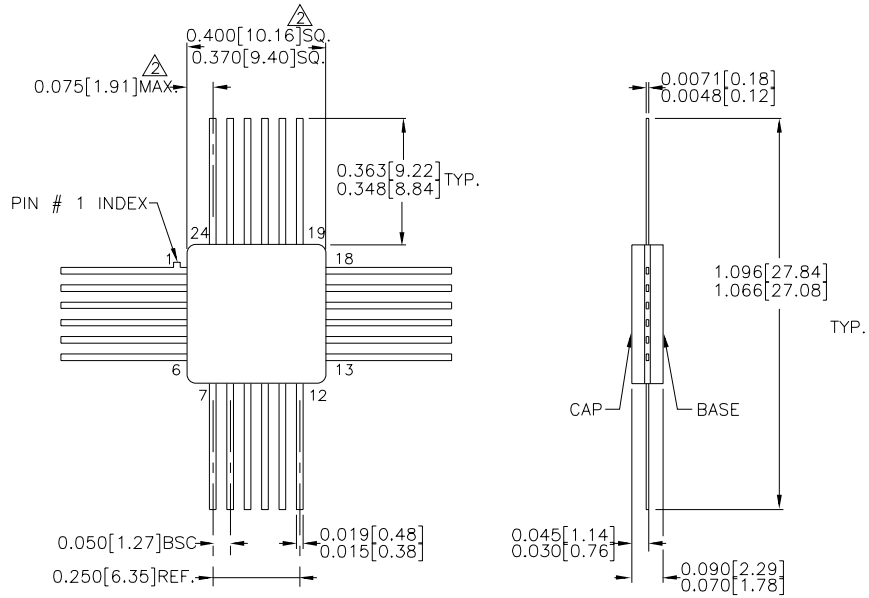


Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

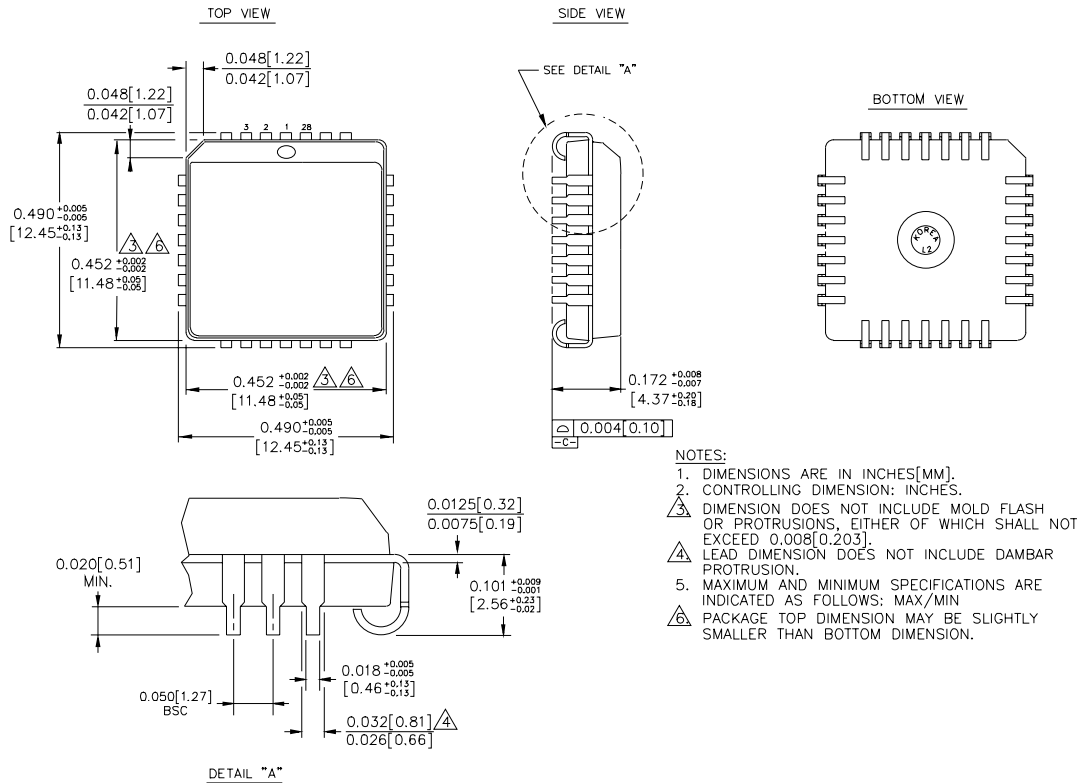
24-PIN CERPACK (F24-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev.03

28-PIN PLCC (J28-1)



Rev. 03

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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