

MCRF355/360

13.56 MHz Passive RFID Device with Anticollision

FEATURES

- Frequency of operation: 13.56 MHz
- Built-in anticollision algorithm for reading up to 50 tags in the same RF field
- "Cloaking" feature minimizes the detuning effects of adjacent tags
- Manchester coding protocol
- Data modulation frequency: 70 kHz
- 154 bits of user-programmable memory
- Contact programming or factory-programmed options
- Very low power CMOS design
- Die, wafer, PDIP or SOIC package options
- On-chip 100 pF resonance capacitor (MCRF360)
- · Read-only device after programming

APPLICATION



PACKAGE TYPE



DESCRIPTION

The MCRF355 and MCRF360 are Microchip's newest additions to the microIDTM family of RFID tagging devices. They are uniquely designed read-only passive Radio Frequency Identification (RFID) devices with an advanced anticollision feature, operating at 13.56 Mhz. The device is powered remotely by rectifying RF magnetic fields that are transmitted from an interrogator (reader).

The device has a total of six pads (see Die Layout). Three are used to connect the external resonant circuit elements. The additional three pads are used for programming and testing of the device. The device needs two external antenna coils (L1 and L2) to pick up the RF magnetic fields and also to send back encoded (modulated) data to the reader. The two antenna coils are connected in series. The first coil (L1) is connected between Antenna Pad A and Antenna Pad B. The second coil (L2) is connected between Antenna Pad B and Vss. The MCRF355 requires an external capacitor to form a resonant circuit along with the antenna coils.

The MCRF360 has 100 pF of internal resonance capacitor between the Antenna Pad A and Vss (across the coils). This capacitance can be utilized to form a tuned LC circuit along with the external antenna coils. See Section 2.2 for external resonant circuits.

The device includes a modulation transistor that is located between Antenna Pad B and Vss. This modulation gate is used to send data to the reader. The modulation transistor is designed to result in approximately 2Ω of resistance between Drain, which is connected to Antenna Pad B, and Source, which is connected to Vss, when it is turned-on.

The LC circuit is tuned to the operating frequency (13.56 MHz) of the reader when the modulation transistor is in a turned-off condition. This condition is called uncloaking.

As the modulation transistor turns on, there will be a shorting effect across L2 due to the 2Ω resistance across it. This results in a change of the inductance of the antenna coil, and, therefore, the circuit no longer resonates at 13.56 MHz. This condition is called cloaking.

The occurrence of the cloaking and uncloaking of the device is controlled by the modulation signal that turns the modulation transistor on and off, resulting in communication from the device to the reader.

The data stream consists of 154 bits of Manchesterencoded data. The code waveforms are shown in Figure 2-3. The data is sent to the reader by modulating (AM) the carrier signal (13.56 MHz). After completion of the data transmission, the device goes into sleep mode for 100 ms \pm 40%. The device repeats the transmitting and sleep cycles as long as it is energized.

Sleep time is determined by a built-in low-current timer. The variation of sleep time is approximately $\pm 20\%$. The variation of sleep time between each device results in a randomness of the time slot. Each device wakes up and transmits its data in a different time slot with

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respect to each other. Based on this scenario, the reader is able to read many tags that are in the same RF field.

The device has a total of 154 bits of contact reprogrammable memory. All bits are reprogrammable by a contact programmer. A contact programmer (part number PG103003) is available from Microchip Technology Inc. Factory programming prior to shipment, known as SQTP (Serialized Quick Turn Programming), is also available. The device is available in die form or packaged in SOIC or PDIP.

Note: Information provided herein is preliminary and subject to change without notice.

DIE LAYOUT



Ded Name	Lower	Lower	Upper	Upper	Passivatio	Pad	Pad	
Pau Name	Left X	Left Y	Right X	Right Y	Pad Width	Pad Height	Center X	Center Y
Ant. Pad A	-610.0	489.2	-521.0	578.2	89	89	-565.5	533.7
Ant. Pad B	-605.0	-579.8	-516.0	-490.8	89	89	-560.5	-535.3
Vss	-605.0	-58.2	-516.0	30.8	89	89	-560.5	-13.7
Vdd	463.4	-181.4	552.4	-92.4	89	89	507.9	-136.9
CLK	463.4	496.8	552.4	585.8	89	89	507.9	541.3
Vprg	463.4	157.6	552.4	246.6	89	89	507.9	202.1

PAD COORDINATES (MICRONS)

Note 1: All coordinates are referenced from the center of the die. The minimum distance between pads (edge to edge) is 10 mil.

2: Die Size = 1.417 mm x 1.513 mm

1.0 ELECTRICAL CHARACTERISTICS

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PAD FUNCTION TABLE

Name	Function					
Ant. A	Connected to antenna coil L1					
Ant. B	Connected to antenna coils L1 and L2					
Vss	Connected to antenna coil L2. Device ground during test mode.					
Vdd	DC voltage supply for programming					
CLD	Main clock pulse for device					
Vprg	Input/Output for programming and read test.					

TABLE 1-2:DC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Commercial (C): Tamb = -20°C to 50°C						
Parameters	Symbol	Min	Тур	Max	Units	Conditions	
Reading voltage	Vddr	2.4	—	I	V	VDD voltage for reading	
Hysteresis voltage	VHYST		TBD		TBD		
Operating current	Iddr	-	7	10	μA	VDD = 2.4V during reading at 25°C	
Testing voltage	Vddt	_	4	_	V		
Programming voltage: High level input voltage Low level input voltage High voltage	Vih Vil Vhh	 0.7*Vddt 	 20	 0.3 * Vddt 	V V V	External DC voltage for program- ming and testing	
Current leakage during sleep time	IDD_OFF	_	10	_	nA	Note	
Modulation resistance	Rм	—	2	4	Ω	DC resistance between Drain and Source gates of the modulation transistor (when it is turned on)	
Pull-Down resistor	Rpdw	5	8	_	KΩ	CLK and VPRG internal pull-down resistor	
Internal resonant capacitor (MCRF360)	CRES	90	100	110	pF	Internal resonant capacitor between Antenna Pad A and Vss (at 13.56 MHz)	
Resonant frequency (MCRF360)	FR	12.93	13.56	14.30	MHz	with L = 1.377 μ H	
Note: This parameter is not tested in production.							

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Commercial (C): Tamb = -20°C to 50°C							
Parameters	Symbol	Min	Тур	Max	Units	Conditions		
Operating frequency	F _c	13.5598	13.56	13.5602	MHz	Carrier frequency		
Modulation frequency	F _M	58	70	82	kHz	Manchester		
Coil voltage during reading	VPP_AC	4			Vpp	Peak-to-Peak AC voltage across the coil during reading		
Coil clamp voltage	VCLMP_AC	—	32		Vpp	Peak -to-Peak coil clamp voltage		
Test mode clock frequency	F _{clk}		115	500	kHz	25°C		
Sleep time	Toff	60	100	140	ms	Off time for anticollision feature, at 25°C		
Write/Erase pulse width	Twc	_	2	10	ms	Time to program bit, at 25°C		
Clock high time	Thigh		4.4		μS	25°C		
Clock low time	TLOW	—	4.4	_	μS	25°C		
Stop condition pulse width	TPW:STO	—	1000	_	nS	25°C		
Stop condition setup time	Tsu:sto	—	200	_	nS	25°C		
Setup time for high voltage	TSU:HH	—	800	_	nS	25°C		
High voltage delay time	TDL:HH	—	800		nS	Delay time before the next clock, at 25°C		
Data input setup time	TSU:DAT		200		nS	25°C		
Data input hold time	THD:DAT	—	800	_	nS	25°C		
Output valid from clock	Таа	_	200	_	nS	25°C		
Data retention	—	200		—	Years	For T < 120°C		

TABLE 1-4: ABSOLUTE MAXIMUM/MINIMUM RATINGS

Parameters	Symbol	Min	Max	Units	Conditions
Coil current	IPP_AC		40	mA	Peak-to-Peak coil current
Maximum Power Dissipation	Pmpd		1	W	
Assembly temperature	TASM		300	°C	< 10 sec
Storage temperature	TSTORE	-65	150	°C	

2.0 FUNCTIONAL DESCRIPTION

The device contains three major sections. The first one is the RF Front-End section, second is the Controller Logic, and third is the Memory section. Figure 2-1 shows the block diagram of the device.

2.1 <u>RF Front-End Section</u>

The RF Front-End section includes power supply, power-on-reset, and data modulation circuits.

2.1.1 POWER SUPPLY

The power supply circuit generates DC voltage (VDD) by rectifying induced AC coil voltage. The power supply circuit includes high voltage clamping diodes to prevent excessive voltage development across the antenna coil.

2.1.2 POWER ON RESET (POR)

This circuit generates a power-on-reset when the tag first enters the reader field. The reset releases when sufficient power has developed on the VDD regulator to allow for correct operation.

2.1.3 DATA MODULATION

The data modulation circuit consists of a modulation transistor (MOSFET) and a 1-turn antenna coil (L2). The two are connected in parallel. The transistor is designed to result in less than two ohms (RM) between Antenna Pad B and VSS. As the transistor turns on, the transistor shorts L2 and, therefore, the external LC circuit is detuned (cloaking).

Cloaking and uncloaking occur by driving the transistor on and off, respectively. Therefore, since the data is encoded by a Manchester format, data bit '1' will be sent by uncloaking and cloaking the transistor for 7 μ s, each. Similarly, data bit '0' will be sent by cloaking and uncloaking the transistor for 7 μ s, each.



FIGURE 2-1: BLOCK DIAGRAM

2.2 Antenna

The MCRF360 requires an external inductor of 1.377 μ H for 13.56 MHz resonance frequency. About one-fourth of the turns of the inductor should be connected between Antenna Pad B and Vss; remaining turns should be connected between Antenna Pad A and Antenna Pad B. The MCRF355 requires this inductor plus 100 pF of external capacitance in order to resonate at 13.56 MHz.

Figure 2-2(a) shows a configuration of an external circuit for the MCRF355. Two external antenna coils (L1 and L2) in series and a capacitor that is connected across the two inductors form a parallel resonant circuit to pick up incoming RF signals and also send back modulated signals to the reader. The first coil (L1) is connected between Antenna Pad A and Antenna Pad B. The second coil (L2) is connected between Antenna Pad B and Vss. The capacitor is connected between Antenna Pad A and Vss.

Figure 2-2 (b) shows another configuration of an external circuit for the MCRF355. In this case, the resonant circuit is formed by two capacitors (C1 and C2) and one inductor.

Figure 2-2(c) shows a configuration of an external circuit for MCRF360.



FIGURE 2-2: CONFIGURATION OF EXTERNAL RESONANT CIRCUITS

2.3 <u>Controller Logic</u>

2.3.1 CLOCK PULSE GENERATOR

This circuit generates a clock pulse (CLK). The clock pulse is generated by an on-board time base oscillator. The clock pulse is used for baud rate timing, data modulation rate, etc.

2.3.2 MODULATION LOGIC

This logic acts upon the serial data (154 bits) being read from the memory array. The data is then converted to Manchester code. The code waveforms are shown in Figure 2-3. The encoded data is then fed to the modulation gate in the RF Front-End section. 2.3.3 SLEEP TIMER

This circuit generates a sleep time (100 ms \pm 40%) for the anticollision feature. During this sleep time (TOFF), the modulation transistor remains in a turned-on condition (cloaked) which detunes the LC resonant circuit away from the operating frequency (13.56 MHz).

2.3.4 READ/WRITE LOGIC

This logic controls the reading and programming of the memory array.



FIGURE 2-3: CODE WAVEFORMS

3.0 DEVICE PROGRAMMING

MCRF355/360 is a contact programmable device. The device has 154 bits of programmable memory. It can be programmed in the following procedure. (A programmer, part number PG103003, is also available from Microchip.)

3.0.1 PROGRAMMING LOGIC

Programming logic is enabled by applying power to the device and clocking the device via the CLK pad while loading the mode code via the VPRG pad (See Examples 3-1 through 3-4 for test definitions). Both the CLK and the VPRG pads have internal pull-down resistors.

3.1 Pin Configuration

Connect antenna pads A, B, and Vss to ground.

3.2 <u>Pin Timing</u>

- 1. Apply VDDT voltage to VDD. Leave VSS, CLK, and VPRG at ground.
- 2. Load mode code into the VPRG pad. The VPRG is sampled at CLK low to high edge.
- 3. The above mode function (3.2.2) will be executed when the last bit of code is entered.
- 4. Power the device off (VDD = VSS) to exit programming mode.
- 5. An alternative method to exit the programming mode is to bring CLK logic "High" before VPRG to VHH (high voltage).
- 6. Any programming mode can be entered after exiting the current function.

3.3 Programming Mode

- 1. Erase EE Code: 0111010100
- 2. Program EE Code: 0111010010
- **3.** Read EE Code: 0111010110
- Note: '0' means logic "Low" (VIL) and '1' means logic "High" (VIH).

3.4 Signal Timing

Examples 3-1 through 3-4 show the timing sequence for programming and reading of the device.



EXAMPLE 3-1: PROGRAMMING MODE 1: ERASE EE

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EXAMPLE 3-2: **PROGRAMMING MODE 2: PROGRAM EE**

EXAMPLE 3-3: **PROGRAMMING MODE 3: READ EE**







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MCRF355/360 GUIDE PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, please refer to the factory or the listed sales office.



NOTES:



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Microchip received ISO 9001 Quality System certification for its worldwide headquarters, design, and wafer fabrication facilities in January, 1997. Our field-programmable PICmicro[®] 8bit MCUs, KEELOQ[®] code hopping devices, Serial EEPROMs, related specialty memory products and development systems conform to the stringent quality standards of the International Standard Organization (ISO).

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